Technologies for the integration of Through Silicon Vias in MEMS packages

Dissertation

zur Erlangung des akademischen Grades
Doktor der Ingenieurwissenschaften
(Dr.-Ing.)
der Technischen Fakultät
der Christian-Albrechts-Universität zu Kiel

Stephan Warnat

Flintbek
2009

1. Gutachter: Prof. Dr. rer. nat. H. Föll

2. Gutachter: Prof. Dr.-Ing. B. Wagner

Datum der mündlichen Prüfung : 18.12.2009

Contents

List of Figures

List of Tables

Table of Abbreviations and Symbols

Abbreviations

Abbreviations	Explanation
ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
BKIN	Bilinear Kinematic Hardening
BOE	Buffered Oxide Etch
C2C	Chip to Chip
CMLS	Chip multi-layer stack
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CupraSelect	Copper-hexafluoroacetylacetonate-thrimetylviniylsilane ($C_{10}H_{13}CuF_6O_2Si$)
CVD	Chemical Vapor deposition
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
DRIE	Deep Reactive Ion Etching
EPMA	Electron Probe Micro-Analysis
ESD	Electro-Static Discharge
DAVID	Downscaled Assembly of Vertical Interconnects
GFS	Gas low sputtering
GPE	Gas Phase Etching
(hfac)Cu(TMVS)	CupraSelect
ISIT	Fraunhofer Institute for Silicon Technology
HW-CVD	Hot chemical vapor deposition
IC	Integrated circuit
IMD	Inter-metallic dielectric

Abbreviations	Explanation
LP-CVD	Low Pressure Chemical Vapor Deposition
LTO	Low Temperature Oxide
MAF	Mass Flow Sensor
MEMS	Microelectro-Mechanical Systems
MO-CVD	Metalorganic Chemical Vapor Deposition
MOS	Metal Oxide-Semiconductor Structure
PCB	Printed Circuit Boards
PE-CVD	Plasma Enhanced Chemical Vapor Deposition
PICS	Passive Integration and Connecting Substrates
PMD	Pre Metal Dielectric
Poly-Si	Poly-Crystalline Silicon
PSG	Phosphorus Silicate Glass
PVD	Physical Vapor Deposition
PWS	80% phosphoric acid, 16% water, 4% nitric acid + tenside
SPE	Silicon Package Efficiency
PoP	Package on Package
PiP	Package in Package
RIE	Reactive Ion Etching
SOI	Silicon on Isolator
SiP	System in the Package
TDMAT	Tetrakisdimethylaminotitan
TEOS	Tetraethylorthosilicate $C_8H_{20}O_4Si$
TSV	Through Silicon Vias
W2W	Wafer to Wafer

Symbols

Symbol	Explanation
α	TSV hole slope [°]
ϵ	Permittivity [F m^{-1}]
$\epsilon_{Isolation}$	Relative permetivity of the isolating material inside the TSV [1]
ϵ_0	Dielectric constant $8.854 \cdot 10^{-12}$ F m^{-1}
λ	$\frac{1}{\tau}$ [m^-1]
ν	Vibration frequency of an atom on the surface [Hz]
ρ	Specific electrical resistivity [Sm^{-1}]
σ	Principal stress [MPa]
τ	Film thickness when 63% of the decay is reached [m]
τ_s	residence time [s]
θ	Angle variation of the incoming flux [°]
ω	impinge rate [$m^{-2}s^{-1}$]
a	Safety distance between chip corner and TSV hole edge [m]
$A_{Isolation}$	Surface area of the insulating material inside the TSV [m^2]
b	Backside chipping [m]
c	Distance between pad corner and dicing line [m]
$C_{Depletion}$	Semiconductor depletion-layer capacitance [F]
C_{TSV}	TSV capacitance [F]
d	TSV contact opening [m]
d_0	Initial film thickness of the isolating material at the TSV hole orifice [m]
E_{Des}	Desorption energy [J]
F_i	Material flux [m s^{-1}]
L	TSV hole depth [m]
$\dot{N}$	Nucleation rate [m^{-3} s^{-1}]
N^*	Equilibrium concentration of stable nuclei [cm^{-3}]
N_B	Bulk concentration of dopants [cm^{-3}]
n_i	Intrinsic carrier concentration [cm^{-3}]
k	Boltzmann constant $1.3807 \cdot 10^{-23}$ J/K

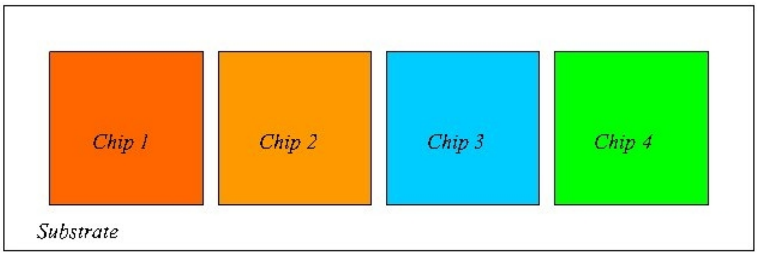
Symbol	Explanation
q	Elementary charge [C]
$R_{Barrier}$	Barrier resistance [Ω]
R_{Bottom}	TSV hole bottom resistance [Ω]
r_{in}	TSV hole radius subtracted by the isolating film thickness [m]
R_{Metal}	TSV metallization material resistance [Ω]
R_{Ring}	Ring metallization resistance [Ω]
r_{out}	TSV hole radius [m]
r(x)	r_{in} in dependence of the film thickness gradiend [m]
S_C	Sticking coefficient [1]
T	Temperature [K]
T_M	Melting temperature [K]
$t_{Isolation}$	Isolator thickness [m]
u_z	z-displacement [m]
V	Bias voltage [V]

1 Integration of Through Silicon Vias (TSV) in MEMS

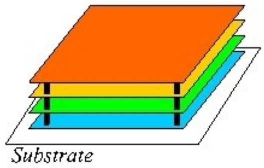
The number of electronic devices available on the market is increasing. In addition they are becoming more complex and the demand for smaller devices is increasing. For instance, a cellular phone in 1990 weighed around 2.4kg and was approximately 25cm by 17cm by 8cm. Today's smallest cellular phone weighs only 55g and is 5.7cm by 2.1cm by 1.3cm. One can perform office applications, take pictures or even browse the Internet in addition to placing a call. In order to keep the requested higher system performance the transistor density inside the electronic device must increase. Gordon Moore predicted 1965 that the implemented transistors on a chip would roughly double every two years [1], whereas the device size should remain the same. This prediction is called 'Moore's Law'.

The conduction line width and the spacing between two conduction lines are important in order to maximize the transistor density. The first integrated circuits were produced with a line width of 25μm (25μm node) [2], whereas the present processor generation is fabricated in the 32nm node [3]. This change in the node allows placement of several thousand transistors effectively increasing the transistor density. The fabrication technologies used must be improved in order to realize a change between the nodes. Technological solutions to change technology nodes were found despite enormous investment cost. Nevertheless, Thompson et al. have shown that the transistor costs decreased by seven order of magnitudes from 1970 to 2000 despite an increase of the investment costs [4]. A chip production with a high throughput and yield is still economically useful in big foundries. Moore's Law can be followed up probably straight forward for another decade by decreasing the line width [5]. Physical device limits are reached if the line width size reduction is continued [6]. For instance, the electron mobility inside the metallization is reduced in smaller conduction lines due to a higher surface scattering. The device performance will be limited in the future. Other ways of increasing the transistor density must be found in order to follow the demand of higher system performances.

G. Moore predicted 2001 that there is certainly no end of technological creativity to follow Moore's law in the future [5]. New technologies like multi-gate transistors are under development [7], but there are still issues regarding the quality and reliability. There are so far no technological solutions to solve this problem during the chip fabrication. Therefore, the process flow must be changed after the fabrication of the chips in order to increase the transistor density. A change of the system architecture solves this problem. The electronic devices are placed next to each other in actual system designs and require a large foot print on the electronic board. A 3D integration allows a reduction of the foot print by the number of stacked devices. Memory stacks of eight dies are realized and will be commercialized in the near future [8]. A stack of different devices allows a spreading of „Moore's Law", because different devices can be placed on top of each other and improve the system performance. Figure 1.1 shows a comparison of a conventional lateral and 3D integration of four dies in respect to the required board.



(a) 10-25%



(b) >100%

Figure 1.1: Lateral and 3D integration approaches.(a) Lateral chip integration (b) 3D integration approach of four electronic chips on a substrate. The given SPEs are typical values of each approach.

The silicon packaging efficiency (SPE) describes quantitatively how many chips are placed on a certain board area. The SPE is given by the ratio of the silicon area used for all implemented chips in respect to the required board area

$$SPE = \frac{\sum_i Si\,Area_i}{Board\,Area} \tag{1.1}$$

Figure 1.1 shows typical SPE values of the integration approaches. This definition allows SPE-values above 100% for multi stacks. Different integration approaches are possible with vertical interconnects. The Chip-to-Chip technology (C2C) describes a stacking of two or more distinct chips. High system flexibility is possible, because different chips can be assembled at certain stack levels. This technology is called Chip-to-Wafer (C2W), if the first layer is replaced by a wafer. A high yield processing is possible for C2C and C2W, because only functional chips or wafers are used. International research projects like the European Union founded project „Downscaled Assembly of Vertical Interconnect Devices" [9] are developing key technologies for these stacking approaches. A stacking of complete wafers (W2W) is an other way to increase the system density. The system flexibility is

limited, because only wafers of the same size and chip type are possible to stack with this W2W technology. Samsung has shown stacks of eight memory dies with this technology [8] as mentioned before.
Vertical interconnects, also called through silicon vias (TSV) [10], are the key element in all described 3D integration approaches. TSV connect the front-side and back side of a wafer by a hole etched through the wafer and subsequent deposition and structuring of suitable films (isolation, metallization and passivation) as shown in figure 1.2. This configuration allows not only better SPE values, but improvements in the

- Electrical performance
- Power consumption
- Noise generation
- Functionality

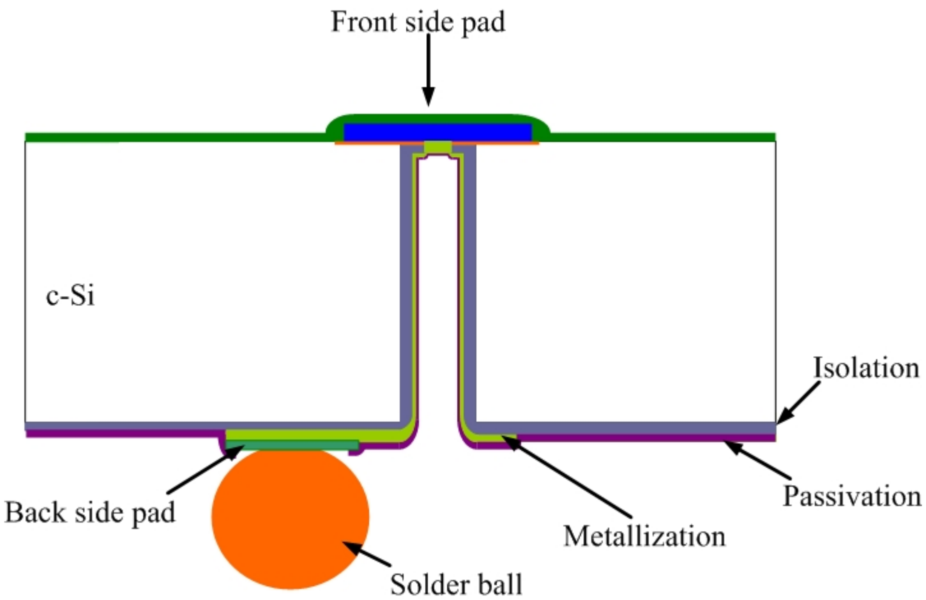


Figure 1.2: Basic concept and elements of a Through Silicon Via.

The electrical resistance, capacitance and inductance (parasitic effects) of TSVs are lower compared to wire bond based packages. For instance, the electrical resistance of the wire bond is ten times higher than comparable TSV [11]. The signal propagation time between two devices such as a microprocessor and a memory is shorter in vertical stacks. In addition, systems with a high data transfer between components can change from sequential

(through bond wires) to a parallel (through TSV) signal processing and improve the real time performance of the system [12]. Camera sensors (imagers) and memory devices are the drivers for TSV development, because both applications require fast processing of numerous data. Both devices allow a wafer thinning, which reduces also the parasitic effects and simplifies the TSV fabrication. The required technologies for the TSV fabrication like etching or metal deposition are easier to perform for $<50\mu$m deep TSVs compared to TSV for full thick wafers.
Micro-electro-mechanical systems (MEMS) gain also from TSV integrated inside their packages. The MEMS concept is based on the realization of devices in which electrical and mechanical components are integrated within a single silicon chip. Systems like sensors, actuators, power producing devices, chemical reactors and biomedical devices are realized on this concept by using a high volume production based on established technologies of the microelectronics industry. Actual MEMS packages like shown in Figure 1.3 are based on wire bond processes between the MEMS, ICs and lead frames, respectively. This arrangement consumes large areas on electronic boards. A preferable approach is a direct placement of the MEMS on top of the IC. Figure 1.3 shows that the sensor chip is much smaller then the IC. This size mismatch allows a placement of several sensor chips on top of the IC, if the IC operating capacity is large enough to handle several sensor signals. A maximum number of MEMS is placeable if TSV are integrated inside MEMS. The placing accuracy of the bond tool defines the distance between two MEMS and therefore the package density or the SPE value. A proper connection between all MEMS and the IC requires a planarization of the IC topography and an implemented redistribution layer. An additional TSV integration inside the IC increases also the SPE value. A solder ball process on the IC wafer back-side and a molding process create a compact ball grid array package (BGA) of an multi sensor module. Literature calls this stacking approach also „More than Moore“ [13].
In addition, TSV enhance MEMS performance in several designs. For instance, capacitive operating devices like accelerometers are sensitive for parasitic effects caused by connection wires. The electrical parasitics are minimized by a TSV implementation as mentioned earlier [11]. Mass flow sensors for liquid or gaseous medias are a second example which implies a better system performance by a TSV implementation. The flow sensor functionality is described in chapter 2.2.4. The actual sensor design from the Fraunhofer Institute for Silicon Technology is connected by wire bonds with the electronics. Wires and the complete interconnect area are covered by an organic protection material (globtop). Sensor structures and the protected interconnect area are in a direct connection with the media investigated during measurements. A diffusion of the media investigated between

Figure 1.3: MEMS package of an inertial measurement unit (Source: SensorDynamics).

the globtop and the substrate was observed during field tests resulting in bond pad corrosion. Thus, measurements of liquid and gaseous media prefer a separation of active MEMS sides and interconnect areas [14]. Connection pads formed on the wafer back-side are protected from the media investigated and a possible corrosion is eliminated. Figure 1.4 shows schematically a TSV integration in mass flow sensor.

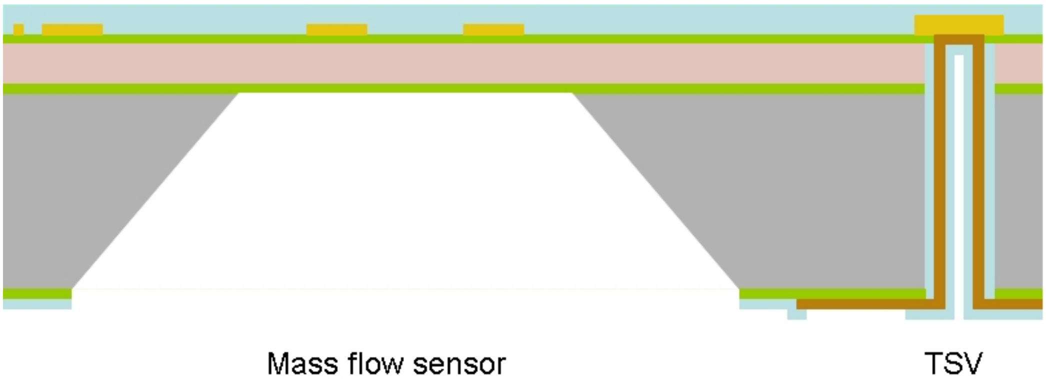


Figure 1.4: Example of Through Silicon Vias in a MEMS package, which allows an operation in harsh environments without a direct contact of the interconnects with the media investigated.

Wafer thicknesses of $<50\mu$m would change the performance of MEMS significantly due to their high sensitivity to bending stress effects . These effects will even increase with decreasing the wafer thickness. Thus, MEMS require a TSV implementation in thick wafer ($> 300\mu$m). Different fabrication technologies and process sequences are necessary for a TSV integration in MEMS packages compared to TSV for electronic devices like memories.

Aim of the thesis

The previous paragraph showed the requirements of new packaging technologies in order to follow the demand of higher transistor densities in new devices. 3D stacking and thinning of chips allow an integration of several devices by using small foot prints. Through Silicon Vias (TSV) are key elements inside these new technologies. Several approaches were developed or investigated for integrated circuits (IC). The functionality of MEMS is increasing by TSV integration inside MEMS-packages. The challenges of TSV integration approaches in MEMS packages are different compared to TSV in IC and can be summarized as followed:

- MEMS are stress sensitive. Wafer thinning changes the MEMS device performance. Thus, TSV must be integrated inside wafer with a full wafer thickness or in moderately thinned wafers ($> 300\mu m$), whereas pad sizes of $100\mu m$ are common. The required processes or process parameters for these TSV geometries in MEMS are not comparable to processes used in TSV approaches for IC. In addition, TSV integrated in hybrid chip scale packages (CSP) of MEMS chips and ASIC wafer require a TSV implementation in IC wafer. Wafer molding of the CSP must be performed during the assembly and puts the system under high pressures. TSV structures inside the IC must resist these forces. Thus, thick IC wafers should be targeted in order to increase the reliability of TSV and consequently of the CSP.

- Several MEMS like resonant sensors require vacuum environments for their proper functionality. The process flow must be designed in such a way that no open holes are created during processing. TSV formed in MEMS packages must show a hermetic barrier against several gases or liquids during device lifetimes.

Some requirements for TSV in IC are also valid for MEMS packages. The core challenges are:

- Maximum process temperatures used are limited by the IC itself. IC metalization layers are commonly AlCu or AlSiCu. A chemical reaction between theses materials and the Si substrate can arise at process temperatures above 400°C. A development of a post-CMOS compatible TSV process sequence results from this temperature specification.

- Some devices are sensitive regarding parasitics effects like the electrical resistance of the TSV formed. A small electrical resistance of the TSV should be targeted for MEMS.

These specific requirements for a TSV integration in MEMS packages define the aim of the thesis:

Development and characterization of fabrication technologies for an integration of hermetic Through Silicon Vias in MEMS packages where post-CMOS compatible processes are used.

Structure of the thesis

The thesis is divided in four major parts. The first part explains basic concepts for a 3D integration of chips based on existing packaging technologies and possible TSV implementation in IC. Existing TSV approaches in MEMS packages are presented and possible TSV approaches for MEMS packages at the Fraunhofer Institute for Silicon Technology are discussed.
The second part shows specification for the TSV targeted. Functional elements of the TSV are discussed and a test design for the TSV development is presented.
The third part evaluates fabrication technologies required for the TSV development. Common IC and MEMS technologies are shown and their applicability for post-CMOS compatible TSV is evaluated.
The fourth part shows a process sequence for a TSV integration in MEMS packages. Implementation aspects of TSV in a CSP package and in a mass flow sensor are discussed.
Lastly the thesis is summarized and an outlook of further work for a TSV implantation in MEMS packages is given.

2 3D advanced packaging

2.1 3D packaging

Packaging is an key technology in all fields of micro-electronics and MEMS. Devices need always an electrical connection path to other elements. Different techniques like wire or flip chip bonding were developed and are commercially used. These techniques are based on a lateral device placement on substrates. The combination of devices placed and the electrical connection paths between these devices form functional systems. This arrangement is characterized by silicon package efficiencies (SPE) of 10% ... 25%. A 3D placement of chips on top of each other allow higher SPE values.
Chip stacking began with mounting of smaller chips onto larger chips. This first approach of increasing SPE-values on chip level was limited due to system and tool complexity. Bond wires provide the electrical paths between chips and boards. Routing of these bond wires between chip levels is challenging especially for those chips with high interconnect densities. In addition, chip sizes in higher levels must be smaller compared to lower levels. Thus, the system flexibility is limited by chip geometries. Chip arrangements like shown in Figure 2.1 (Die stacking) are not always possible for systems targeted. A placement of larger chips on top of smaller chips requires an implementation of passive chips (interposer chips). The vertical distance between two chips increases by the implementation of these interposer chips, which allows the use of bond wires for interconnect purposes between two layers. This 3D integration approach needs larger interposer chip thicknesses compared to bond loop heights. Chip multi-layer stacks (CMLS) have been archived using these variations and are now available in high-volume productions.
Package stacking is a second way to increase SPE-values. Two or more CMLS are stacked on top of each other and form a new package in this 3D stacking technology. Connectors recognize the electrical conduction paths between stacking level. Each CMLS is tested before finally assembled. This testing allows high system yields and low cost production of high-volume products even when additional costs for connectors increase. Figure 2.1 shows two different package assembly methods. Package in a package (PiP) assemblies use a face to face orientation between two CLMS and a back to face orientation is used for package on package (PoP) architectures. The described approaches have the following disadvantages:

- All presented 3D stacks are based on wire bonds. Typical electrical resistances of bond wires are in the range of $150m\Omega$. This value is too high for several modern systems. It is not possible to obtain a fast signal propagation.
- Final packages are molded before they are used as an electronic device on electronic boards. Package molding introduces stress to wire bonds and the reliability risk increases during the device life time.
- Chips (silicon) and adhesive bond materials (organic based) have linear thermal expansion coefficients of $2 \cdot 10^{-6}K^{-1}$ and $60 \ldots 100 \cdot 10^{-6}K^{-1}$, respectively. This mismatch puts thermal stress on the system and operating temperatures are limited.

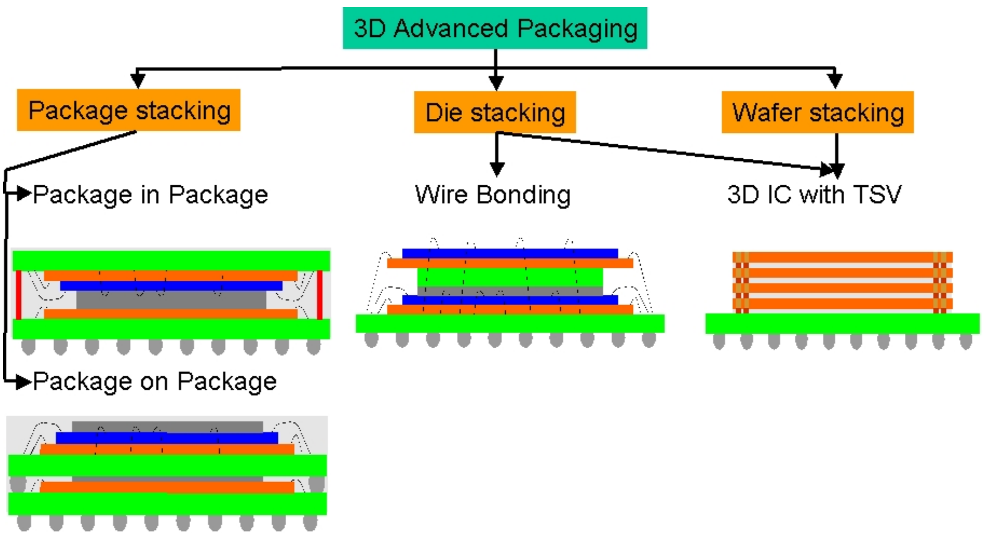


Figure 2.1: Advanced 3D stacking technologies. The text describes the technologies in detail.

2.2 Through Silicon Vias

Vertical interconnects through chips, also called Through Silicon Vias (TSV), can overcome the described problems in chapter 2.1. Basic concepts for packages with TSV will be discussed in chapter 2.2.1. However, TSV must have simultaneously several advantages over CMLS and package stacking technologies before semiconductor vendors change their chip assembly. Key factors for a possible technology change are summarized below and the advantages of TSV are discussed [12].

- The electrical performance is driven by the gate and interconnect delay at chip level. Interconnect delays (RC-delay), which are given by interconnect wires between transistors, device pads and bond wires, dominate in actual technology nodes used compared to transistor gate delays due to small gate dimensions of modern technology nodes. RC-delays decrease by TSV integration, because the interconnect length is shorter in TSV based packages compared to wire bond based packages. Linder showed that electrical resistances of TSV are 10 times smaller compared to similar wire bonds [11].

- Interconnect wires consume a significant portion of the electrical power. The power loss is reduced by TSV, since TSV shortens interconnect lengths. In addition, shorter wires reduce noise, which allows handling of low signal levels.

- Modern applications have a higher demand to integrate more functions in one device. In addition, package footprints should not be changed or even be reduced. Stacked chips reduce foot prints on boards by the number of stacked levels. The SPE increases to values above 100% by TSV integration.

- The access time between logic devices and memories is the bottleneck in several modern devices. The limited number of bond wires does not allow a parallel processing of all data between these two devices. The sequential data transmission, which is alternatively used, reduces the system performance. TSV allow a parallel processing between the two devices and the system gains functionality.

2.2.1 Concepts

TSV based 3D-integration approaches are divided in a prearrangement of the substrate, the TSV fabrication itself and a final assembly in a package. Technologies used are mostly independent from the developed concepts. First, wafer thinning is performed depending on the concept after the TSV formation or beforehand (wafer prearrangement). A hole is formed inside the wafer and is followed by a subsequent deposition of an isolation and metallization layer. Processes needed are discussed in chapter 4. Wafers or chips with integrated TSV are aligned to each other and bonded in a final assembly step.

Developed TSV concepts use different process flows. A simultaneous processing of TSV and IC structures is a first method of TSV integration. No temperature limits arise for processes used, because TSV are integrated before metallic layers are present. Process temperatures above 400°C result in a reaction of the metal used (mostly Al) and the substrate (Si). Fabricated TSV with a maximum process temperature used of 400°C are also called *post-CMOS TSV*. Thus, the electrical conducting material is doped poly-crystalline silicon (Poly-Si). Poly-Si shows a higher electrical resistance compared to metals, which limits the application area of this technology. However, research groups and companies have developed process flows for this TSV technology.

Garrou and Bower [15] discuss several post-CMOS TSV process sequences. They divided the technologies in „pre via“ and „post via“ sequences. TSV are formed in IC wafer before a thinning and bonding to other IC or handle wafer in „pre via“ approaches. Wafers are first bonded to handle wafers and thinned before TSV are implemented in „post via“ flows. Figure 2.2 shows an overview of different TSV technologies. Detailed process flows are shown in figure 2.3. Garrou and Bower show a total of nine different TSV approaches. Kröninger [16] and Joly [17] show summaries about wafer thinning and bonding technologies, respectively. These processes are not in the scope of this thesis.

2.2.2 Commercial Activities

Imager chips and memories are key drivers of TSV developments. The demand of imaging devices (imager) has increased during the last decade due to the integration of cameras in cellular phones. Only conventional CMLS packages are used in camera packages so far, because the sensing side of imagers must be oriented to the outside of the package. Sanyo and Toshiba introduced a glass wafer bonding to the active imager side [18]. The glass wafer was used as a handle wafer during TSV processing and was afterwards a part of the camera package.

First, Toshiba bonded imager wafers to glass wafers by using organic adhesives. Then, imager wafers are thinned with standard back-grinding and polishing processes to thicknesses around $100\mu m$. TSV holes were formed by laser ablation. A 15μm thick organic isolation was deposited and opened only at the hole bottom also by laser ablation. 10μm thick Cu liners formed the metalization layer.

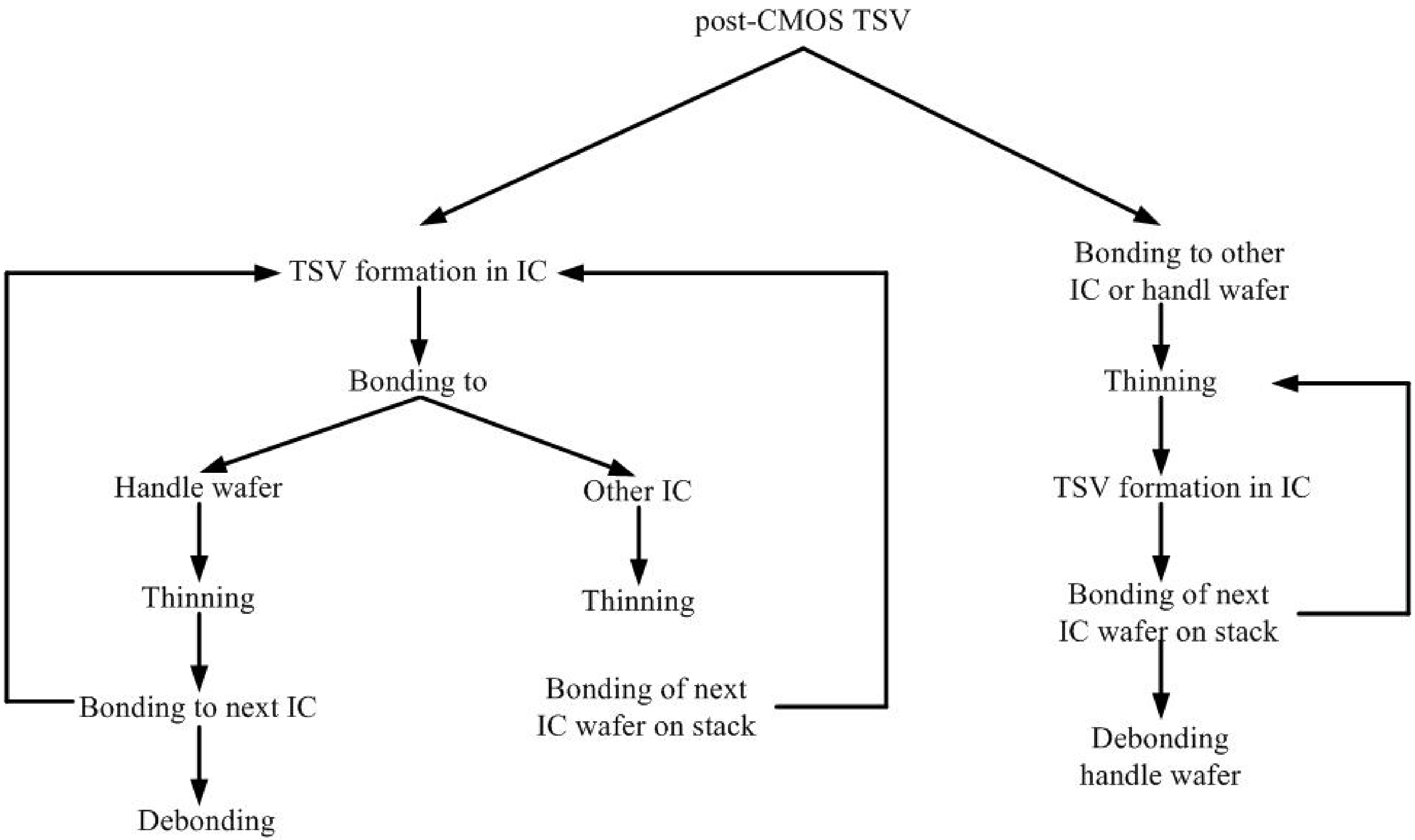


Figure 2.2: TSV integration approaches in IC wafer. The key processes are TSV formation, bonding and thinning, which can be repeated n-times until the required stack height is reached

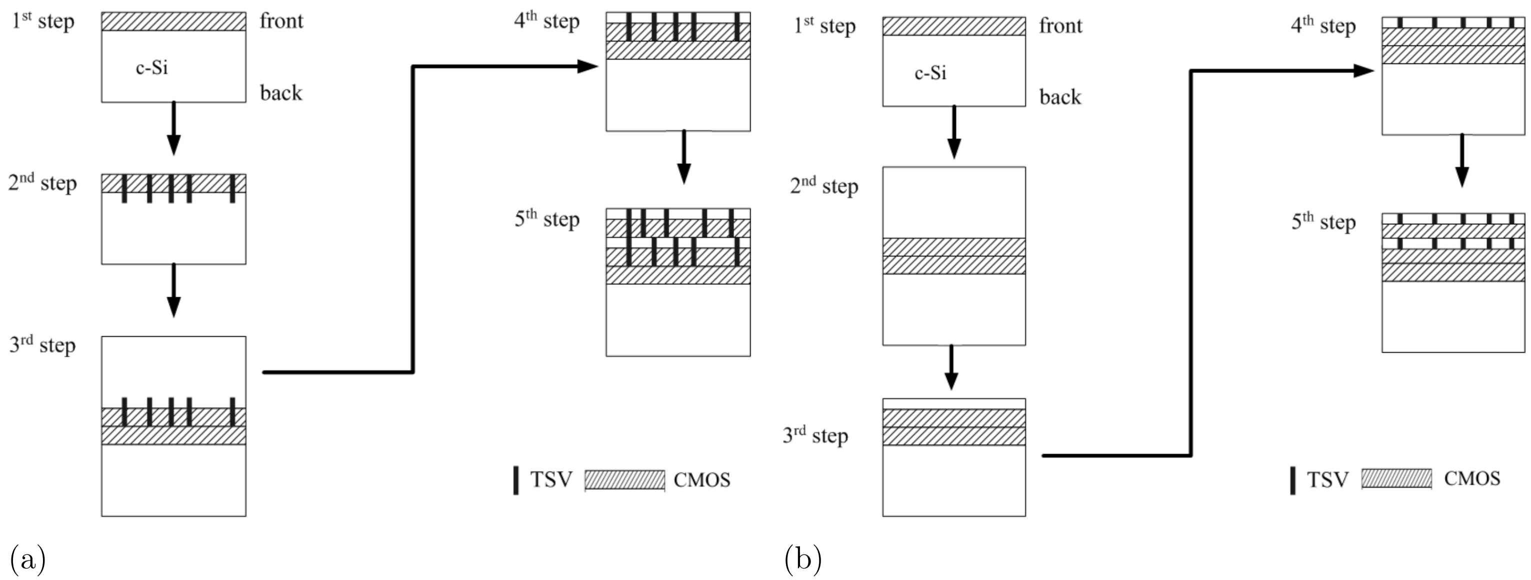


Figure 2.3: Examples of post-CMOS TSV integration approaches (redrawn from [15]).
(a) 1^{st} step: The sequence starts with a fabricated IC; 2^{nd} step: TSV are formed from the front side; 3^{rd} step: Face to face bonding to a second IC; 4^{th} step: wafer thinning and back side processing; 5^{th} step: Back to Face bonding of other IC like 3^{rd} and 4^{th} step.
(b) 1^{st} step: The sequence starts with a fabricated IC; 2^{nd} step: Face to Face bonding to other IC; 3^{rd} step: wafer thinning and back side processing; 4^{th} step: TSV fabrication from wafer back side. This approach stops at the first metalization level of the IC; 5^{th} step: Back to Face bonding of other IC like 3^{rd} and 4^{th} step.

Sanyo used different technologies and materials for a similar TSV process sequence. Wafer thinning was performed in the same way as the Toshiba's approach. Holes were formed by physical etching of Si. An inorganic isolator (SiO_x) was deposited twice in order to maintain the required film thickness. The isolator was opened by an anisotropic etching of the isolator. A seed and barrier layer was deposited inside the holes and on wafer backsides followed by a 5μm thick Cu-liner. Other companies have developed similar sequences for TSV in imager wafer [19][20].
The space is limited in new applications like cellular phones, whereas the same or even more data must be processed. Several memory producers develop memory stacks based on TSV in order to solve this problem. Samsung was the first company which announced in 2006 that they had developed a TSV technology for NAND flash memories. A memory stack of eight memories was shown in [8]. They showed in 2007 that their TSV technology was transferable to DRAM memories [21]. The foot print of TSV based memory stacks is 15% smaller compared to conventional packages and the stacks are 30% thinner compared to wire bond solutions [18]. Cellular phones are potential markets for these memory stacks made to height limitations inside the phone. Holes were formed by laser ablation and completely filled with Cu. Wafers were bonded to a carrier wafer before thinned to 50μm and an etch back exposed the deposited Cu. Wafers with the same dimensions and chip sizes were bonded on top of the exposed Cu.
Other companies like Tezzaron & Chartered, Micron and NEC are also developing TSV technologies [18]. NEC used a via first technology. A passivation and Poly-Si were deposited in holes with diameters of 2μm and a depth of 50μm. This hole dimensions allowed a fast and complete filling with Poly-Si. Chemical mechanical polishing (CMP) provided a smooth surface for subsequent memory fabrication.
IBM [22] and INTEL [23] introduce TSV in their next generation of microprocessors or wireless communication devices. Latency times between microprocessors and memories was Intel's driver for their TSV development. TSV reduce this time as mentioned before. Their approach was based on a via last sequence. Intel's TSV have a diameter of approximately 5μ and a depth of 10μm. Lower power consumption in TSV based packages is a driver for IBM. A detailed TSV process flow of IBM is up to now not known.
NXP implemented TSV in passive integration and connecting substrates (PICS) [24]. Different devices were bonded in a C2W process on both sides of PICS in order to overcome size mismatches. Signal routing between devices was achieved through lateral and vertical (TSV) interconnections. This 3D integration approach was also called interposer-wafer approach. PICS allowed also an integration of passive components like resistors and capacitors (RC-elements) close to devices like microprocessors by forming these elements directly

on the interposer wafer. RC-elements are required to stabilize device functionalities or set certain device parameters. The interconnect length in CMLS architectures is much longer compared to these interposer solution. In addition, the fabrication technologies of available SMD RC-elements show variances up to 20%. IC technology processes have a much better process robustness and minimize the value variation. Thus, systems based on this PICS technology gain performance and the SPE value increases.

2.2.3 TSV in MEMS packages

Micro-electromechanical systems (MEMS) benefit from TSV, too. Several MEMS devices measure capacitance variations. The signal level is relatively low and is noise sensitive. The parasitic capacitance resulting from interconnects is reduced by using TSV. In addition, a better signal to noise ratio is predicted [12]. Process sequences for TSV in MEMS devices are not comparable to TSV in IC devices like shown in previous chapters. Wafer thinning during the TSV fabrication is limited due to the stress sensitivity of MEMS. The MEMS functionality changes by stress introduced by wafer thinning.
SINTEF introduced TSV in cap-wafers, which are mandatory for resonant working MEMS due to their vacuum requirement (see also chapter 2.2.4). Holes were formed through the entire wafer and a 1μm thick thermal oxide was grown afterwards. Poly-Si was deposited by LP-CVD on both wafer sides simultaneously and doped in the gas phase with phosphorus. The electrical resistance of these TSV formed were in the order of 5 to 15 Ω. Deposited Al on both wafer sides improved the contact to the Poly-Si. Al and Poly-Si are patterned by dry etching using dry resists. This process sequence of a TSV formation in a cap wafer allowed a hermetic capsulation of the MEMS [25]. In addition, they placed a logic device on top of the cap wafer by conventional wire bond processes.
Heschel et al formed only one hole by wet etching (KOH) and patterned Al inside this cavity. He called this Si-wafer an intermediate structure. MEMS and IC's were bonded to this intermediate structure subsequently [26]. Kutchoukov et al presented a similar intermediate structure [27]. Linder showed the capability of wet etched cavities for TSV and presented a comparison between wire bond based packages with equivalent TSV [11].
Silex prearranged Si-wafers before MEMS are fabricated. Highly doped Si wafers were used as substrates. Dry etched cylindrical or rectangular rings defined the TSV structure. The rings formed were completely filled with an isolator. A final CMP process defined the Si surface on which MEMS can be fabricated. A metallic redistribution layer on the MEMS wafer back-side allowed solder balling to substrates or bonding directly on top of logic devices [28]. The doping level defines the electrical resistance of the TSV formed.

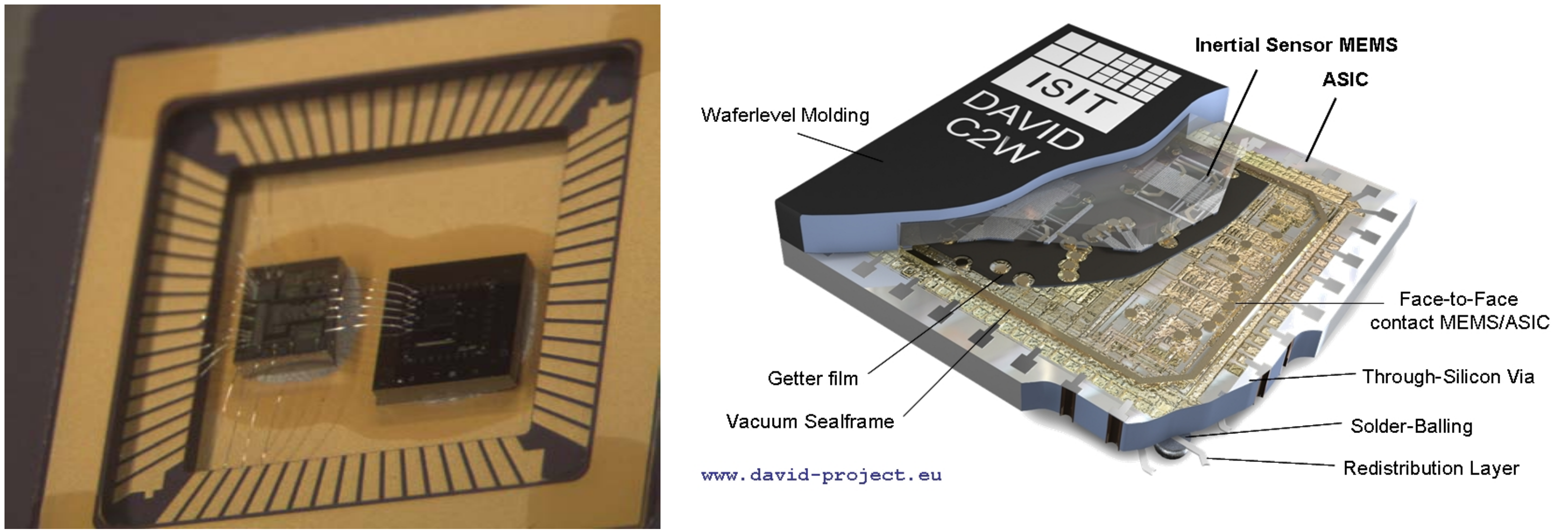
Lin et al presented TSV in silicon on isolator (SOI) MEMS. MEMS layers were deposited and structured but not yet released. Holes of a diameter up to 300μm were formed by laser ablation through the entire wafer. A thermal oxide was grown for isolation purposes. This SOI wafer was glued to a handle wafer, on which a metallic seed layer was already deposited. Then the hole was completely filled by a metal electroplating process in a so called bottom up process. A back-side contact was also formed by electroplating after the handle wafer was removed [29]. This approach allows similar to the Silex approach a high SPE value and short interconnects. A value of the electrical TSV resistance was not reported.
Rasmussen presented a TSV process flow for use in hearing aids [30]. 100μm wide and 380μm deep holes were formed through the entire wafer by wet etching or dry etching. 5μm of Parylene was deposited in the gas phase and was used as isolation material. A TiN (200nm), Cu (1μm) metalization was deposited by metal organic CVD and patterned by wet etching using electrophoretic resists. An electrical resistance value of 160mΩ was obtained. TSV formed by this process flow are not hermetic.

2.2.4 Application examples

Example A Several MEMS modes of operation require vacuum environments. Resonant oscillating structures do not work under ambient atmosphere due to a high damping of the sensor structure. Therefore, an encapsulation of these MEMS structures is mandatory to achieve proper device function. Encapsulation processes on wafer-level are developed and several MEMS products using this technology are commercially available [31]. A MEMS wafer is bonded to a cap-wafer in this technology, whereas standard cap-wafers are electrically passive. They protect the MEMS structures during the following processes like dicing and maintain vacuum levels inside the cavity formed during the device lifetime. Detailed explanations of bond processes are presented in [32]. Bond wires form the electrical contacts between MEMS, ICs and lead frames. Figure 2.4(a) shows an actual design realized at Fraunhofer ISIT. Interconnect lengths and SPE-values are critical for several new applications planned.
The Fraunhofer Institute for Silicon Technology (ISIT) develops new processes in order to improve MEMS functionalities. The project Downscaled Assembly of Vertical Interconnect Devices (DAVID) [33], which is founded by the European Union, targets a direct placement of MEMS devices on top of an application specific integrated circuit (ASIC). This direct stacking allows a realization of short interconnects between MEMS and ASIC. The cap-wafer is not passive anymore, which results in a higher SPE value. A direct bonding of a

MEMS wafer to an ASIC wafer (W2W) is a promising process for high volume products due the fully developed bonding process. Costs of this process are manageable for new devices, because wire bonds are replaced and the system gains performance. A bonding of MEMS chips to ASIC wafer in a C2W process is very challenging. The technologies required are still under research [9]. However, C2W technology is an interesting technique to bond MEMS and ASIC wafer in prototype phases, low volume products or for costly MEMS. Electrical testing of MEMS and ASIC before bonding allows a 100% production yield.

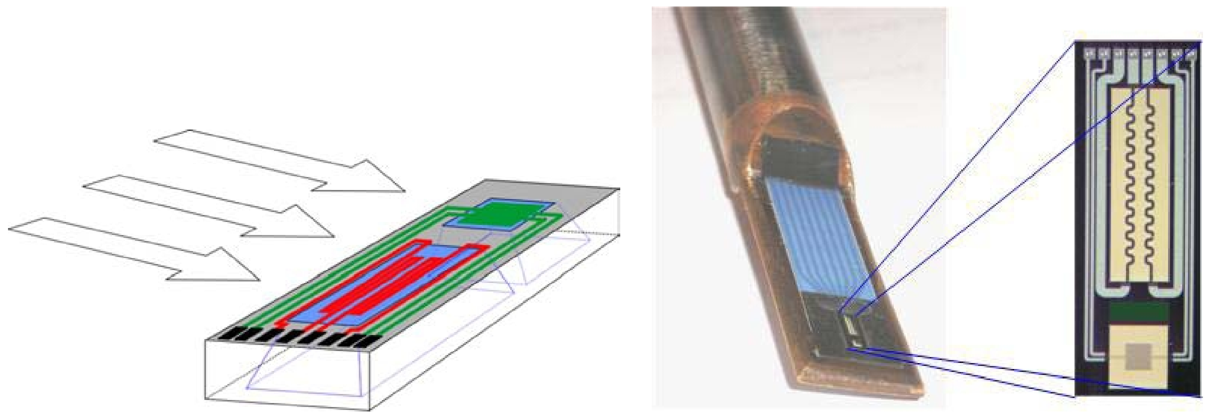
In addition, TSV integration inside ASICs improves the performance for systems creating using the DAVID approach. The TSV formation must be performed before MEMS chips are bonded to ASICs. A signal redistribution on the ASIC back allows an integration of solder balling processes. Wafer molding [34] and device separation allow an integration of this so called *system in the package (SiP)* in printed circuit board designs. Figure 2.4(b) shows a scheme of the DAVID approach for the C2W approach. Functional elements presented in figure 2.4(b) are discussed in [35].



(a) (b)

Figure 2.4: (a) Hybrid integration of MEMS and ASIC in a ceramic package. The interconnects are realized by wire bonds. (b)Vision of the DAVID project. A MEMS is directly bonded to an ASIC by using a C2W approach. TSV allow a signal routing directly to the ASIC back-side and solder ball processes can be performed.

Example B ISIT has developed a mass flow sensor for gaseous and liquid media. The sensor operates on the hot wire anemometer principle combined with calorimetric principles. The primary sensor of this mass flow sensor is a heated wire that is exposed in a media flow (either gas or fluid). A second sensor is used to measure the ambient (media) temperature. The heating sensor shows a low electrical resistance (50-90 Ω) and the reference sensor shows a high value (2 kΩ). As the flow passes over the hot wire, it carries away heat. The heat loss depends on the mass flow rate, the heat capacity of the media, and the temperature difference between the wire and the media. Since the heat capacity of the media is known and the temperatures are monitored in real-time, the mass flow rate can be determined from the heat loss (related to the electric resistance of the wire via Ohm's law) and the temperature coefficient α of the wire. The sensor principle is shown in detail by [36]. Figure 2.5(a) illustrates a sketch of the sensor and (b) shows a sensor setup used in field tests for water flow monitoring.



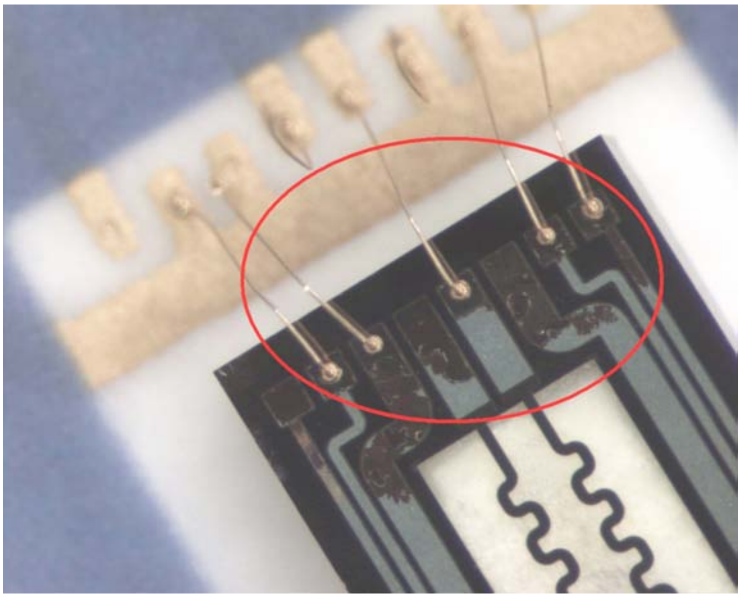
(a) (b)

Figure 2.5: (a) Sketch of an anemometric mass flow sensor developed at ISIT. (b) MAF measurement setup used for water flow monitoring.

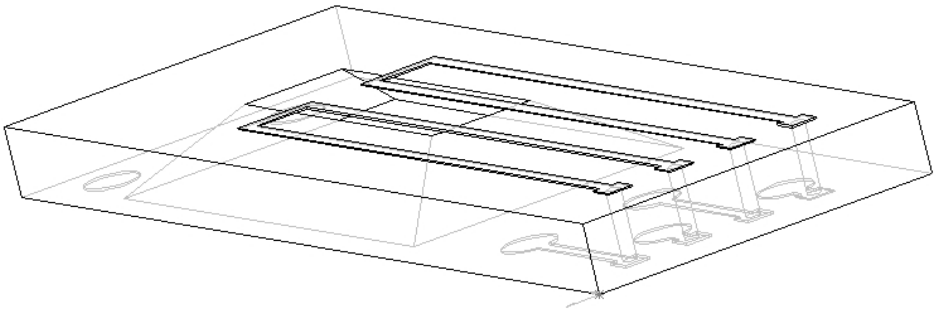
Field tests showed that corrosion of bond pads can occur after long measurement times even though organic protection layers (glob top) were applied on top of bond wires and pads like it is shown in figure 2.6(a). Water infiltration between the glob top interface area and the substrate was observed. A good example of a better performance of an TSV integration in MEMS is the mass flow sensor for two reasons

- to avoid the observed corrosion and
- to prevent micro-turbulences.

TSV fed the sensor signal to the wafer back-side. Redistribution layers on the wafer back-side allow an electrical contact between the mass flow sensor and a substrate by solder ball or bump technologies. Pads on the wafer front can be protected by inorganic films deposited by standard LP- or PE-CVD techniques. Films deposited by these techniques show a good chemical resistance against various media that were investigated. Therefore, mass flow sensors with integrated TSV allow measurements of gaseous and fluid media even in harsh environments [14]. In addition, the measurement performance of the sensor is improved by TSV implementation. The media investigated flows homogeneously over the sensor using TSV, because turbulences of flowing medias caused by the bulky glob top in the actual system integration approach can not occur by a TSV integration. The signal to noise ratio and the sensitivity is thus enhanced by TSV integration in mass flow sensors. Figure 2.6(b) illustrates a mass flow sensor with integrated TSV which prevents corrosion and micro-turbulences.



(a)



(b)

Figure 2.6: Conventional mass flow sensor package after field test and mass flow sensor with TSV. (a) Mass flow sensor after field test and glob top removal. Corroded bond pads were observed due to water infiltration at the glob top interface to the sensor. (b) TSV integration in mass flow sensors developed at the Fraunhofer Institute for Silicon Technology.

3 Specifications of TSV in MEMS-packages at Fraunhofer ISIT

3.1 TSV process sequences

TSV carry electric signals from the wafer front- to back-side. Thus, electric conducting films must connect electrical connection points (pads) of IC or MEMS front-sides with pads on wafer back-sides. A direct connection of front-side pads from the wafer back-side by using:

- a hole etched through the wafer,

and subsequently a deposition and structuring of,

- an electrical isolating material,
- an electrical conducting material and
- a protection material

is an appropriate TSV solution for MEMS packages. TSV etch processes required must stop underneath the first metallization layer of the front-side pad in order to realize a good electrical contact between deposited electrical conducting material and the front-side metallization. In addition, hermetic TSV require stable pad-cells after TSV processing. ASIC and MEMS pad-cell specifications have to be taken into account regarding these two aspects. Pad-cell structures are discussed in sections 3.2.1 and 3.2.2. Electrical potentials of metallization films deposited must be separated from the substrate by an electrical isolating material in order to avoid cross talking between TSV and other functional elements on the wafer. Thus, organic or inorganic films have to be deposited inside the holes etched and on wafer back-sides. A structural dense film composition is necessary in order to avoid leakage currents during the device lifetime. Isolating material deposited covers the TSV hole bottom and hole sidewalls simultaneously and an anisotropic etching only at the hole bottom opens again front-side pad structures. An appropriate electrical conducting film, in general a metal, is deposited inside TSV geometries and on wafer back-sides for

electrical conduction purposes. Conventional metal deposition techniques does not allow a void free filling of the TSV techniques. Electroplating is often used to fill holes completely with metals. However, a complete TSV filling inside the TSV holes with a depth of $>300\mu$m is economically and technologically not useful. First, Dixit et al have shown that a complete filling of 400μm deep holes takes 20 hours, which is economically unacceptable [37]. Second, c-Si and the metal used (often Cu) have a coefficient of thermal expansion of 4.2 ppm/K and 20 ppm/K, respectively. This mismatch introduces a large stress inside the TSV system under any thermal treatment during TSV processing and is larger for complete filled TSV structures. Thus, a ring metallization like shown in figure 3.1 step 4 should be targeted for a TSV implementation inside MEMS packages with wafer thicknesses $>300\mu$m. This deposited film is the base material for the back-side pad-cell. Thus, a structuring of the material deposited is necessary. Metallic films deposited inside the TSV can not be structured in order to minimize the electrical TSV resistance. This requirement creates a high challenge for the deposition of photoresists, because standard resist deposition processes are not developed for this high topography challenge. The deposition and partial opening of a passivation layer are final process steps of this TSV flow. Figure 3.1 shows schematically the described TSV fabrication flow.
This TSV solution requires direct access to front side pads from wafer back sides. This is sometimes, especially for ASIC pads, hard to achieve due to implemented electrical protection structures next or underneath the pad, see chapter 3.2.1. A redistribution of pads on wafer front sides overcomes this challenge. A second pad which is electrically connected to the original pad must be implemented which fulfills requirements of a TSV implementation inside CMOS or MEMS wafer.

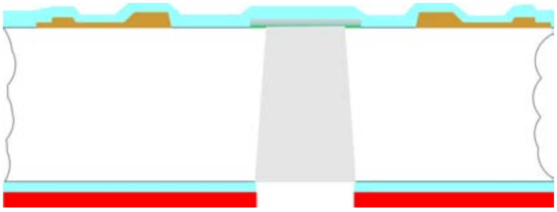
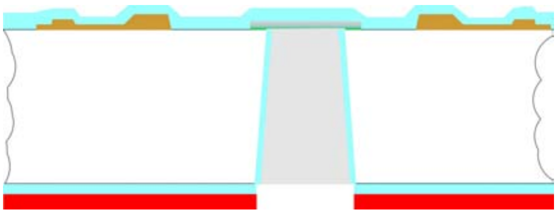
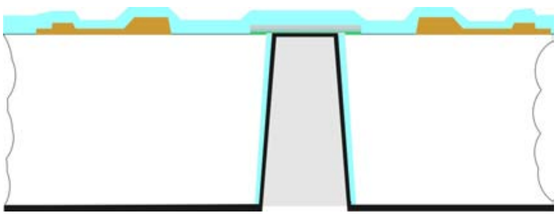
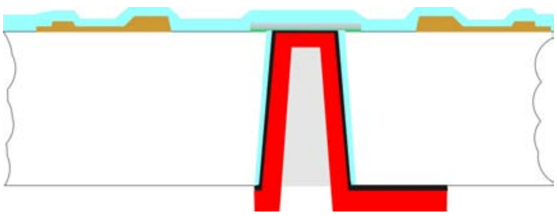
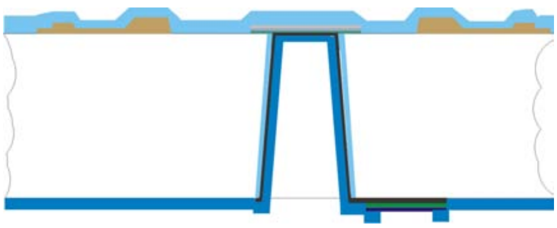
Step	Process sketch	Process description
1		CMOS or MEMS wafer with active structures (brown) and front side pad (gray-green)
2		Etched hole through the entire wafer defines the TSV geometry. The etch processes must stop underneath the first metallization level of the CMOS or MEMS wafer (red: photoresist).
3		Deposition of an insulating material (turquoise) inside the TSV geometry and the wafer back side. Material deposited on the hole bottom is removed afterwards.
4		Deposition of a conduction material (black) inside the TSV geometry.
5		Structured conducting material with photoresist (red) on top of this film.
6		Deposition and structuring of a passivation layer (blue).

Figure 3.1: Basic process flow of a post-CMOS compatible TSV.

3.2 Pad-cell requirements

3.2.1 CMOS pad-cell

CMOS pad-cell architectures are not standardized. Electrical device performance defines pad-cell layouts. For instance, pads in high frequency application devices require much thicker isolation layers between two metal layers in order to avoid cross talking compared to direct or low frequency signal devices. In addition, pad-cells used must withstand mechanical forces during subsequent processes like wire bonding or soldering. Broken pads reduce system yields and this results in higher production costs. Thus, all CMOS wafer vendors have developed their own pad-cell designs. Design rules used are confidential. However, all pad architectures are based on the same functional elements and fabrication technologies.
First, isolating materials are deposited onto wafers in order to isolate the silicon wafer electrically from pad structures or other functional elements. These layers or layer stacks are called pre-metal dielectric (PMD) and are based on silicon oxide or nitride variations like un-doped or doped silicate glasses. Metallic films are deposited on top of the PMD in order to connect functional elements on the wafer. These films must fulfill the following criteria due to reliability issues:

- Materials deposited must show good adhesion.
- Diffusion of any material inside other structures or functional elements must be avoided.
- The electrical conductivity must be minimized in order to reduce parasitic effects.

Thus, transition metals like Ti are deposited on top of the PMD and react with the surface. Ti does not diffuse through the PMD or other isolating materials. The electrical conductivity of Ti is not high enough for conduction purposes in CMOS devices. Therefore, high electrical conducting metals preferred Al, Cu or AlCu alloys, are integrated. The adhesion of these metals is good on Ti, but their diffusion inside oxides is not negligible. Diffusion barriers like TiN or TaN are deposited between adhesion promoters and metallization layers to avoid material transport. All three different films are sputtered. This film stack made out of an adhesions promoter, a diffusion barrier and a metallization is called 1^{st} level metallization. Pad-cell specifications defines the pattern of the metal deposited.
High transistor densities in modern CMOS devices need more than only one metallization level to make the system function. A passivation layer, also called inter metallic dielectric

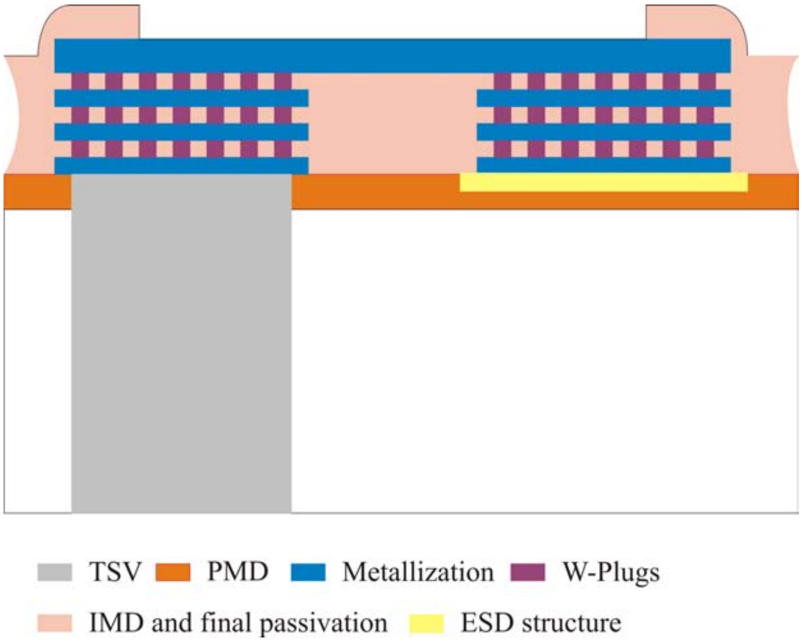
(IMD), is deposited on top of the 1^{st} level metallization. A planarization of this film is performed by chemical mechanical polishing in order to define a planar level for the next process. Via holes are etched inside the IMD and then filled with W completely. These W-plugs allow an electrical connection between the 1^{st} and 2^{nd} metallization level. The process sequence for the deposition of the 2^{nd} metallization level is the same as described above for the 1^{st} level metallization. These processes are repeated until the last metallization level is reached. Some CMOS devices need six to nine metallization levels.

TSV implemented in CMOS devices require a planar 1^{st} level metallization surface in order to achieve a defined etch stop at the adhesion promoter. A mosaic design, which is sometimes used in RF-applications, does not allow a defined etch stop, because oxides are deposited between metal structures. These oxides will be removed during the PMD etching. The metal remaining is possibly not mechanically stable after the oxides are removed.

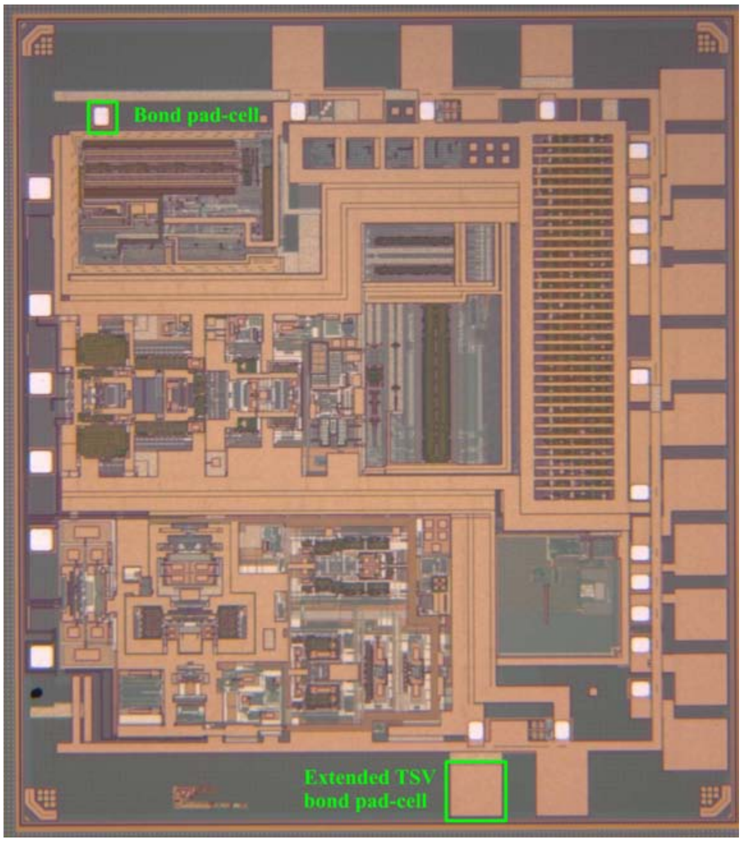
Several functional elements on wafers are electrostatic sensitive and require protection structures due to possible short electrical current pulses during testing or assembly. Thus, electrical protection structures are sometimes implemented underneath the 1^{st} metallization level. These structures must remain stable during TSV processing. A placing of these structures around pad cells allows a TSV process as described before. This is often not possible due to design aspects. A pad extension like the one shown in figure 3.2 is otherwise required for a TSV integration. A complete chip re-design is not necessary in this case. Figure 3.2 shows also a top view of an ASIC design with an extended TSV pad-cell.

TSV implementation in CMOS devices limits the processes that can be used. For instance, the thermal process budget is limited due to already implemented metallic films like Al. Higher temperatures cause a diffusion of Al into the Si substrate even if a diffusion barrier is present. This diffusion can cause non-functional electrical circuits.

Alkali ions contamination may occur during an exposure of the wafer with etchants such as KOH or photo-resist developers like NaOH. The main concern of alkali ion contamination is the probability of positive alkali ions to diffuse to functional elements and change physical parameters such as the threshold voltage of transistors. Suitable cleaning procedures are necessary in order to remove all ions after wet etching processes. In addition, Al is etched by some wet chemical processes. Process flows must be chosen in such a way that no contamination and destruction of pad-cells appear.



(a)



(b)

Figure 3.2: Pad-cell structure of CMOS devices. (a) Extended pad-cell allows an integration of TSV in standardized Pad cells without a re-design of ESD structures. (b) Topview of an ASIC by ST Microelectronics with conventional bond and extended TSV pads.

3.2.2 MEMS pad-cell

Different technologies and process flows were developed for MEMS fabrication. Thus, standard MEMS designs are not realized. Several projects tried to find a solution for this challenge, but each MEMS vendor is still using different machines or technologies to produce MEMS. These different technologies have influenced MEMS pad-cell designs. No standard pad-cell designs are available. However, a pad-cell design for a mass flow sensor from ISIT will be presented here. The entire process flow of this mass flow sensor has to be explained for this purpose. The major process steps can be summarized as follows:

1. The mass flow sensor is a membrane sensor and this membrane is based on a three layer stack composed of a silicon nitride, a silicon dioxide and an additional silicon nitride layer. This optimized stack shows a small tensile stress and does not show any buckling after release etch.

2. The sensing structures are made by a stack of TiN, Ti, TiN and Al. Al has to be deposited in order to form a pad on which a wire bond process can be applied. The TiN protects the reactive Ti during further process steps and during measurement cycles.

3. Silicon nitride deposited on these structures protects the Al against corrosion forced by the media investigated. The nitride is only opened at the pad-cell area.

4. A wafer processing from the back-side is followed, which is not important for the pad-cell design. A complete process description is given by Melani et al. [36]

Figure 3.3 shows a cross section of the realized sensor.

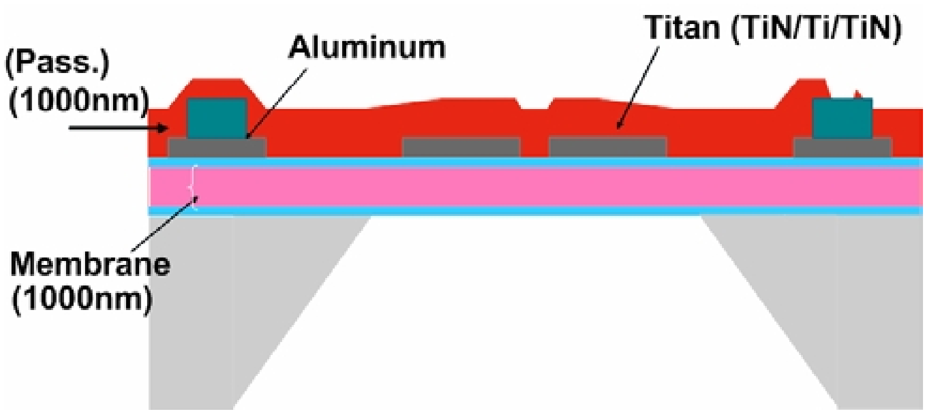


Figure 3.3: Cross section of the realized mass flow sensor at Fraunhofer ISIT.

3.3 TSV hole geometry

Pad-cell geometries and orientations on IC- or MEMS-wafer limit possible TSV hole geometries. Pad-cell geometries of 90μm x 90μm are common in actual IC layouts and are placed at chip corners. Common designs uses distances of 40μm between pads and chip edges. Pad-cells are placed often next to each other with an equidistant spacing (pitch) of 150μm. This geometrical view results in a maximum TSV hole geometry. Holes formed can not be larger than pad-cell geometries at the hole bottom (underneath the front-side pad). Larger hole diameters can destroy surrounding functional elements. This consideration is based on vertical etched holes. Formation of tapered holes is limited by the positions of placed pad-cells at chip corners. Large angles of tapered TSV holes will intersect dicing lines and TSV formed will be destroyed by the final dicing process. The TSV hole slope in respect to the planar wafer side is expressed by α.

$$\alpha_{Max} = \arctan\left(\frac{\text{Wafer thickness}}{\frac{\text{Pad size}}{2} + c - (a+b) - \frac{\text{d}}{2}}\right) \tag{3.1}$$

Factors used are indicated in figure 3.4. Large α should be targeted, because deposition processes are easier to perform for large α in deep holes. The maximum angle α_{max} for different wafer thicknesses is given by equation (3.1) and is summarized in table 3.2. Equation (3.1) takes only the distance between the bond pad and the chip corner into account due to the fact that this distance is much smaller compared to pitch sizes.

Wafer thickness / [μm]	50	100	300	508	675	760
TSV angle α / [°]	51	68	82	85	87	87

Table 3.2: Possible TSV profiles dependent on the wafer thickness

3.4 Mechanical Aspects

3.4.1 Wafer robustness

A conformal deposition of electrical isolating and conducting materials is challenging in TSV geometries with high aspect ratios. A detailed explanation of the deposition processes and their capabilities to deposit a conformal layer inside >300μm deep TSV is discussed in chapter 4.2. Wafers of 50μm thickness or less are used in several TSV approaches in order to simplify this deposition challenge. Wafer handling without carriers is not possible

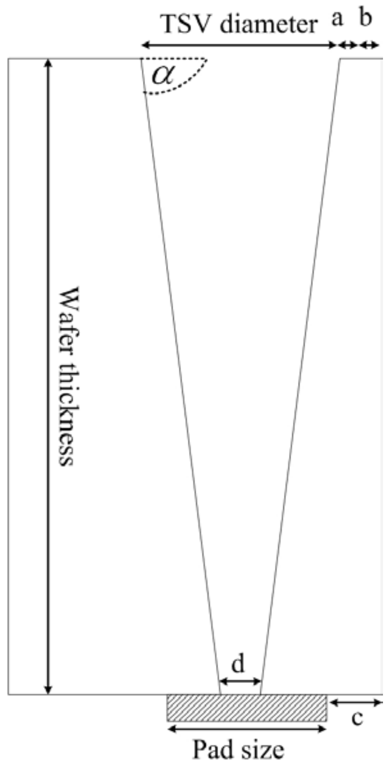


Figure 3.4: Possible TSV geometry at chip corners; a is a safety distance of 25μm; b is given by possible backside chipping (15μm), c is the distance between the outside of a pad and the dicing line (40μm), d is the contact window opening (here 10μm).

for these wafer thicknesses due to the resulting high fracture probability. Thus, carrier wafers fixed to thinned wafers are used during TSV fabrication. The processes needed to fix and release carrier wafers are expensive. In addition, a TSV implementation in MEMS wafer does not allow wafer thinning to thicknesses of 50μm due to their sensitive stress behavior. MEMS performances are changed or even destroyed by extreme wafer thinning (50μm). The possibility of operating MEMS with thinned wafers to thicknesses of 300μm to 400μm exists. Previous investigations have shown that a wafer processing with these thicknesses is possible without a significant yield loss [38]. This investigation was performed on planar wafers without TSV. Therefore, handling limits for silicon wafers of different thicknesses that contain TSV are discussed in the following mechanical simulations. The work is performed together with Prof. Fiedel of the University of Wroclaw and is partially presented in [39].

Model description

A wafer handling description in a complete process flow is difficult to perform. For instance, wafer holding systems (chucks) of processing machines are not standardized. A definition of one universal mechanical loading force is not possible. Therefore, a normal loading force applied at the wafer center is used as a mechanical loading force for all processes. In addition, the loading area is taken into account as a system parameter. Figure 3.5 shows the simulation model and the stress distribution inside the wafer while external load is applied. In brittle crystalline materials such as Si, fractures can occur by cleavage as a result of tensile stress acting normally to crystallographic planes with low bonding forces. These planes are also called cleavage planes. Values of compressive strength are much higher than the tensile strength in almost all materials. Therefore, crack initiation starts preferably at the point in which the maximal tensile stress occurs (indicated as A in figure 3.5).

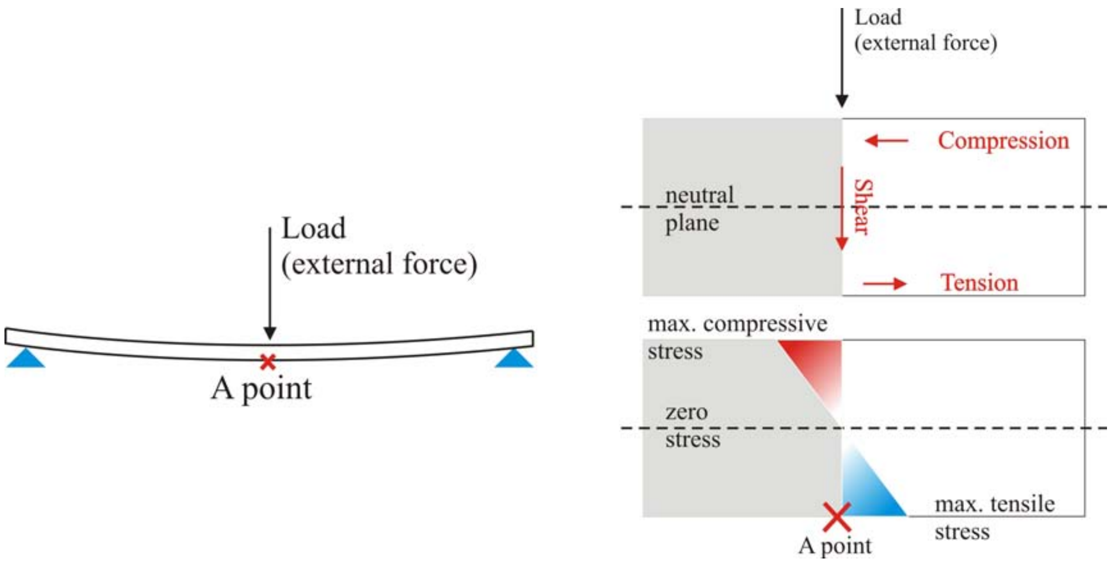


Figure 3.5: Simulation model for determination of wafer stability during processing and stress distribution inside the wafer while an external load is applied

The fracture criterion is defined as follows. The flexural strength which is also known as modulus of rupture, bend strength or fracture strength should be selected as the critical material strength parameter in case of beam bending. Pecht et al show that the flexural strength is usually less than 10% of the compressive strength [40]. The compressive strength of silicon is well defined with 6GPa, but literature shows a wide range of flexural strength values for silicon. Values between 60MPa and 2.4GPa are reported [40][41]. Here, a

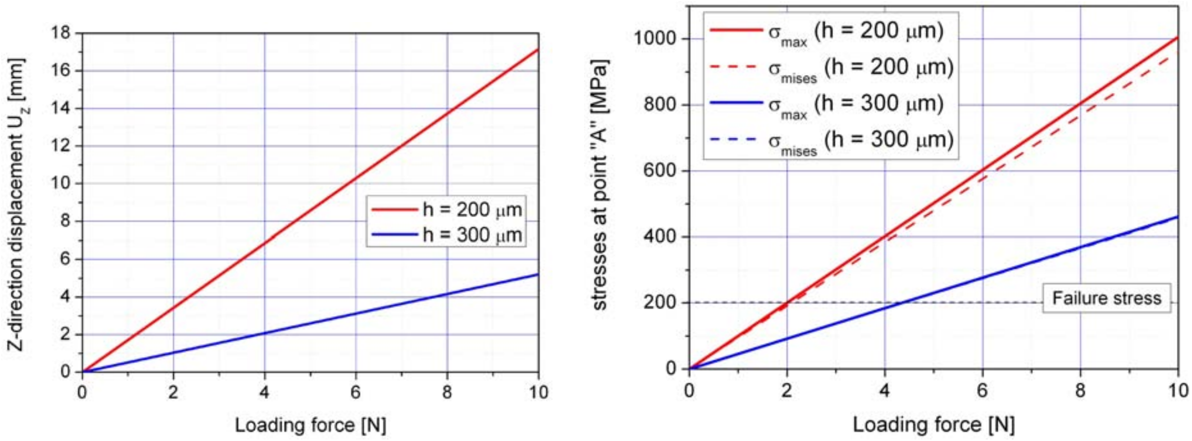
maximum flexural strength of 200MPa is taken as a fracture criterion.
8 inch (100) Si wafers with a thickness of 200μm and 300μm will be considered. Two different wafer types are considered for the calculation of the mechanical strength:

Test A Blanket Si wafer without TSV.

Test B Si wafer with TSV oriented in-one-line along the x- and y-axis and in a staggered orientation.

TSV hole diameters of 30μm and a 80μm pitch are defined in this model. These hole dimensions are four orders of magnitude smaller compared to the wafer size. In this case it is not possible to simulate the complete model (with all holes) with sufficient accuracy (coarse mesh) or in satisfactory time (to many elements). Thus, the problem is divided in two easier models. First, a coarse model uses only a few holes, but with a bigger diameter. The sum of surface areas created is the same in the coarse and the original fine models. This coarse model allows an interpretation of stability issues on wafer level. A sub-model is created in a second step at the wafer center, because the loading force is the highest at this point. Original TSV hole geometries are used in this model. In addition, wafer symmetry allows calculations on only a wafer quarter. Sub-modelling and the wafer size reduction reduces calculation times and show sufficient results.

Test A Kroenninger showed that chips with breaking strengths >20N allows a processing with a sufficient yield [16]. This investigation is performed on chip level and the values are obtained by three- and four-point bending tests. The maximum strength during wafer processing is assumed to be lower than these measured values. Therefore, an external load of 10N is assumed as a possible maximum force which will be applied to the wafer during processing. Figure 3.6 (a) shows the displacement in z direction at the point A dependent on the external load. Wafer bows of 17.17mm or 5.21mm are observed for 200μm and 300μm thick wafer, respectively. Figure 3.6 (b) shows the predicted stress in point A in dependent on the external load and indicates that an external load of approximately 2N and 4N can be applied to the 200μm and 300μm thick wafer, before the predicted stress is larger than the defined failure stress.
This investigation is based on a infinitely small (0mm) external applied load on point A, but mechanical handling tools have certain dimensions. Thus, the external load is also applied with a varying radii. A pressure is defined in such a way that the external load at the extended area is the same compared to the concentrated force of 4N. Table 3.3 summarizes the predicted stress values and the wafer displacement in z-direction at point



(a) (b)

Figure 3.6: Displacement and stress dependent on the external load.

A for a 200μm and 300μm thick wafer and a variation of extended areas. The principal stress at point A decreases about 24% and 27% for the 200μm and 300μm thick wafer, respectively. The displacement in z-direction is the same for all radii, because the applied pressure is kept constant. All values predicted that principal strengths for 200μm thick wafers are larger than the allowed 200MPa, whereas the values of principal strength for the 300μm thick wafer are below the failure criteria. This prediction is in a good agreement with previous investigations at the Fraunhofer ISiT [38]. It can be concluded that a wafer processing with 300μm thick wafer is possible without a significant yield lost and the assumed flexural strength value of 200MPa for Si seems to be in a good agreement with the experimental results at Fraunhofer ISiT.

Test B The following simulations show how the wafer strength changes with a TSV implementation. Two different TSV orientations are tested. Figure 3.8 indicates a TSV orientation in-one-line along the x- and y- axes and an alternative staggered orientation. The TSV dimensions are also indicated in this figure. In addition, the crystallographic orientation of the x- and y- axes of the in-one-line oriented TSV is varied.
The failure criteria and the simulation parameters are not changed for these geometries. Figure 3.8 shows predicted principal strength values for the in-one-line placed TSV and a wafer thickness of 200μm. The maximum principal stress is 396MPa at the TSV entrance on the wafer backside, whereas the TSV are placed in the <100> along x- and <010> along y-axes. The same investigation on TSV placed in the <110> along x- and y-axes shows a maximum stress of 397MPa. The crystallographic orientation of the TSV placement does

			Wafer thickness h = 200μm		**Wafer thickness h = 300μm**	
Radius	**Area**	**Pressure**	σ_{Max}	z-displacement	σ_{Max}	z-displacement
$[mm]$	$10^{-2}[mm]$	$[MPa]$	$[MPa]$	$[mm]$	$[MPa]$	$[mm]$
0	0	–	402.6	6.87	184.6	2.08
0.1	3.14	127.3	375.8	6.87	160.4	2.08
0.2	12.56	31.9	346.5	6.87	152.7	2.08
0.3	28.27	14.1	323.0	6.87	143.9	2.08
0.4	50.26	7.9	306.4	6.87	136.6	2.08

Table 3.3: Influence of area radius R on the maximal principal stress and z-displacement

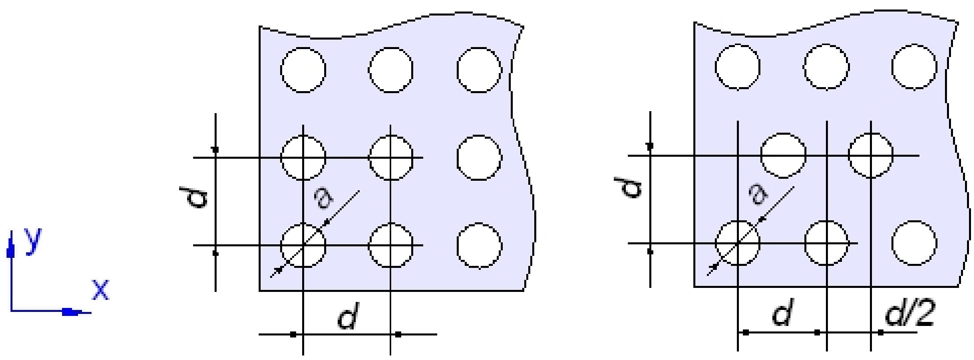
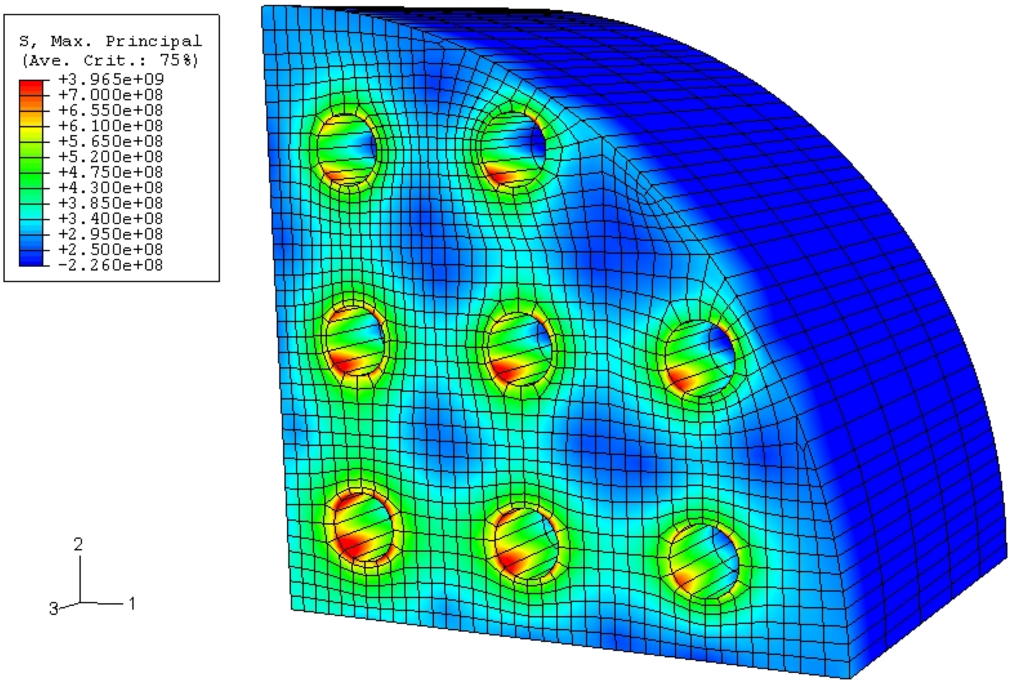


Figure 3.7: TSV orientations on a wafer. The left illustration shows a TSV orientation in one line and the right illustrations indicates a staggered orientation. a=30μm, d=80μm

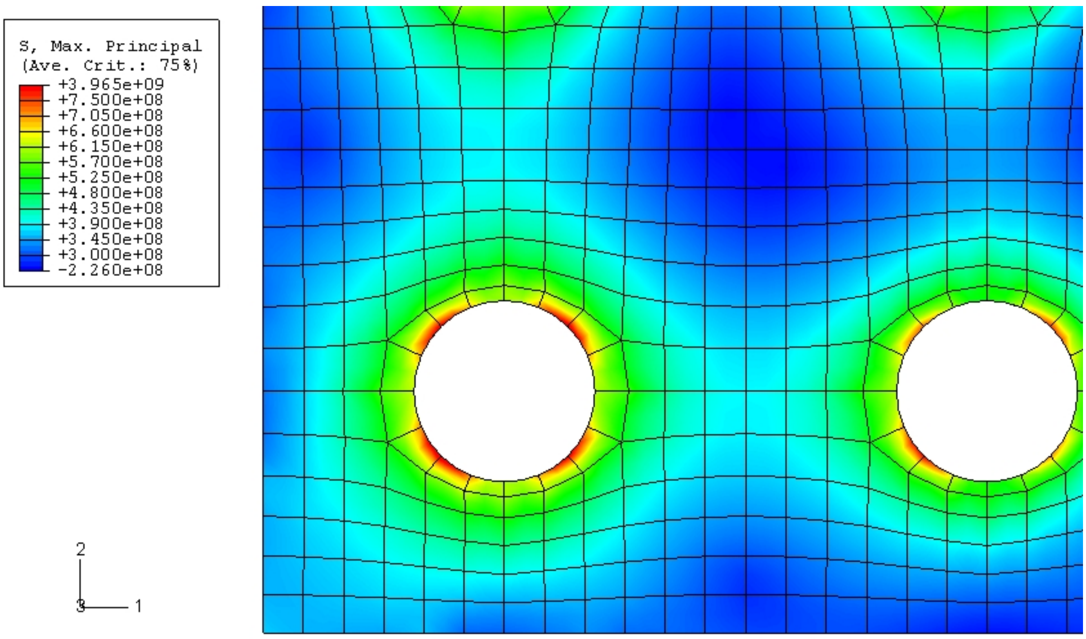
not influence the introduced stress.
In addition, the external load was varied as described above. Figure 3.9 shows the maximum stress dependent on the external load for both wafer thicknesses and TSV orientations. The stress predicted reaches the failure stress if an external load of 2N is applied to a 200μm thick wafer. This value of the maximum allowed load is similar compared to blanket Si wafer. A higher principal stress is predicted at the TSV sidewalls compared to point A even if the same external load is applied. A principal stress of 200MPa is reached on the TSV sidewalls if an external load of 1N is applied. Thus, the highest probability of a cleavage fracture is given at the TSV entrance when an external load is applied. The TSV were placed in one line in the previous investigations. A staggered arrangement like the one shown in figure 3.8 was also investigated. The principal stress values are similar for all investigated TSV arrangement. Table 3.4 summarizes the predicted principal stress values for 200μm and 300μm thick wafers and different TSV arrangements. It can be concluded that the wafer stability does not change significantly by a TSV implementation.

Wafer thickness &			**Principal Stress [MPa]**	
	TSV orientation	**Crystallographic orientation**	Point A	TSV hole entrance
200μm	**blanket Si wafer**	$--$	402.6	$--$
	in-line	$< 100 > x, < 010 > y$	390.6	799.3
		$< 110 > xy$	406.4	834.7
	staggered	$< 100 > x, < 010 > y$	386	788.9
		$< 110 > xy$	400.3	846
300μm	**blanket Si wafer**	$--$	186.6	$--$
	in-line	$< 100 > x, < 010 > y$	170.7	325.7
		$< 110 > xy$	176.2	350.1
	staggered	$< 100 > x, < 010 > y$	173.7	327.6
		$< 110 > xy$	180.9	354.6

Table 3.4: Predicted principal stresses at point A and on the TSV hole entrance under an external load of 4N. The TSV are placed on the given crystallographic orientations.



(a)



(b)

Figure 3.8: Predicted principal stresses of 200μm thick wafer under an external load of 4N and a TSV placement in <100> along x- and <010> along y-direction. (a) Principal stress values obtained by coarse modelling. (b) Principal stress values obtained by fine modelling.

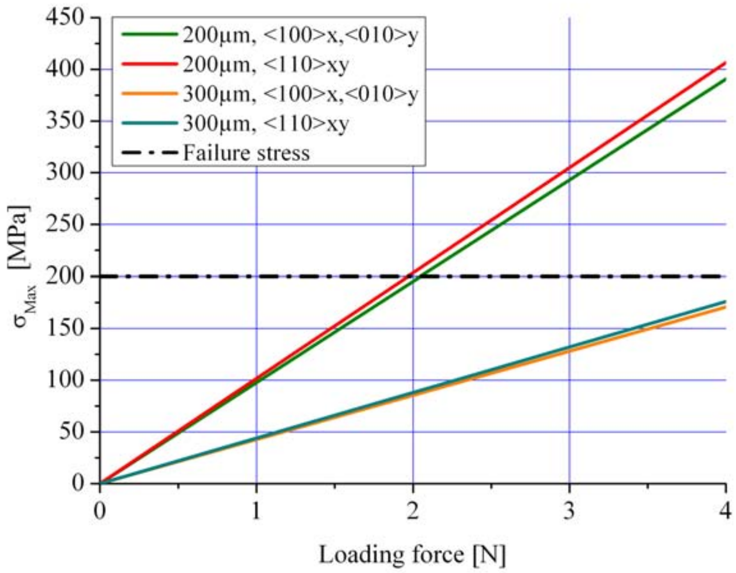


Figure 3.9: Predicted principal stress at point A for 200μm thick wafer dependent on an external load. The crystallographic orientation of the TSV is indicated.

3.4.2 TSV system

Thermo-mechanical predictions of MEMS packages with integrated TSV are investigated in the following chapter. Examples of MEMS package like shown in chapter 2.2.4 require different assembly technologies. The DAVID project targets a chip-scale package (CSP) [35] as a final demonstrator. The integration of MEMS and ASIC is suggested in a direct face-to-face bonding in a chip-to-wafer (C2W) approach like it is shown in figure 3.10. Vertical interconnects and a metallic interface between the MEMS and the ASIC lead to a wafer-level package that protects the device against particles, moisture and mechanical stress and can even maintain a vacuum around resonant sensors. A getter film is integrated on top of the ASIC in order to maintain the established vacuum during the device lifetime. The getter film used needs an activation at temperatures of 400°C [32]. A TSV technology is targeted to connect ASIC pad-cells with external substrates. Therefore, solder balls are placed on pad-cells formed on the ASIC back-side. Wafer molding of the ASIC - MEMS stack with integrated TSV allows a direct integration of this measurement unit on other substrates with a small foot print. A detailed description of the wafer molding process in the DAVID-project is described by Gal [34]. Getter film activation at 400°C and the moulding process apply the highest load to the package during the assembly. Thus, these two processes are investigated in the following.

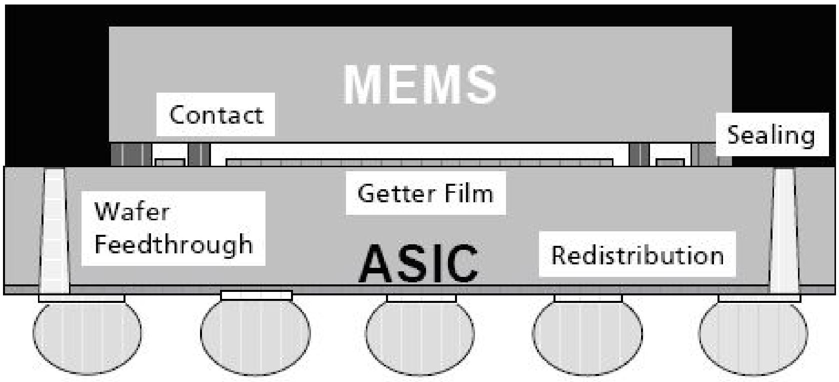
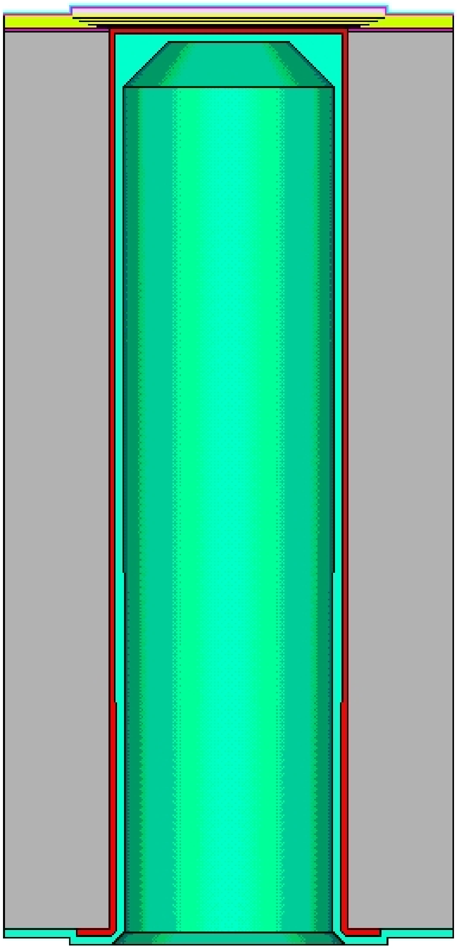
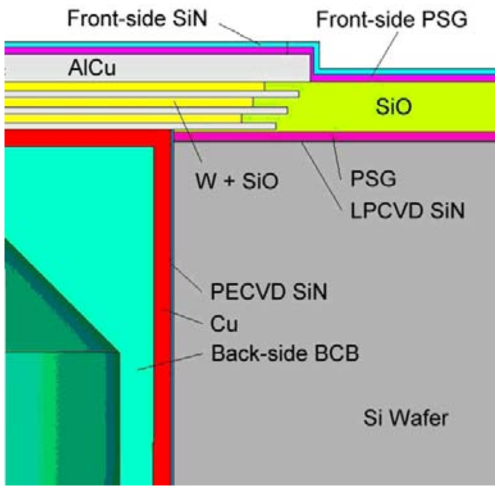


Figure 3.10: Cross section of the targeted CSP of the DAVID project. The functional elements are described in the text.

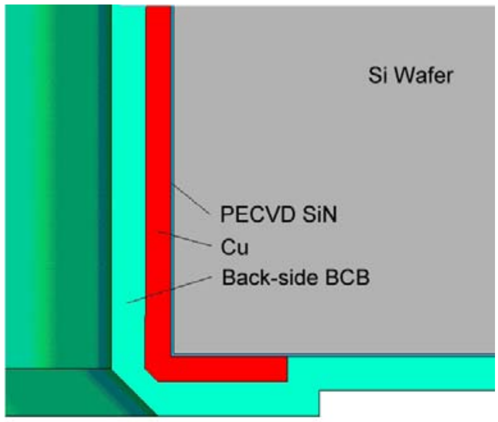
Model description

The TSV model used is similar to the TSV obtained by the process flow described in chapter 3.1. In addition, the DAVID project targets a TSV implementation inside ASICs. Thus, a CMOS pad design as described in 3.2.1 is used. Figure 3.11 shows the model used. The most material properties were treated as non-dependent on temperature. However, some known properties are regarded as linear functions of temperature except for the coefficient of thermal expansion (CTE) for Si, which is highly non-linear [42].
The W-plugs and the surrounding isolation material are replaced by a homogeneous anisotropic material. Appendix B summarizes material parameters used. For most metallic materials, also for Cu and AlCu, elastic deformation persists only to strains of about 0.5%. Therefore, in this work the Bilinear Kinematic Hardening (BKIN) model of Cu and AlCu is used. In this material model the tangent modulus was prescribed for the part of stress-strain curve above the yield strength. Tangent modulus is usually taken as the slope of the stress-strain curve at some specified level of stress. However, this portion of the stress-strain curve is not linear. Therefore, in these calculations, the secant modulus instead off the tangent modulus was used to describe the material behavior in plastic regions. The secant modulus represents the slope of the secant drawn from the yield strength point to some given point for large elongation, but before tensile strength point is expected.
The wafer equipped with TSV is subjected for bonding of MEMS to ASIC at temperatures of 400°C which is necessary for getter activation. In addition, the molding process is done





(b) TSV bottom



(a) TSV overview

(c) TSV entrance

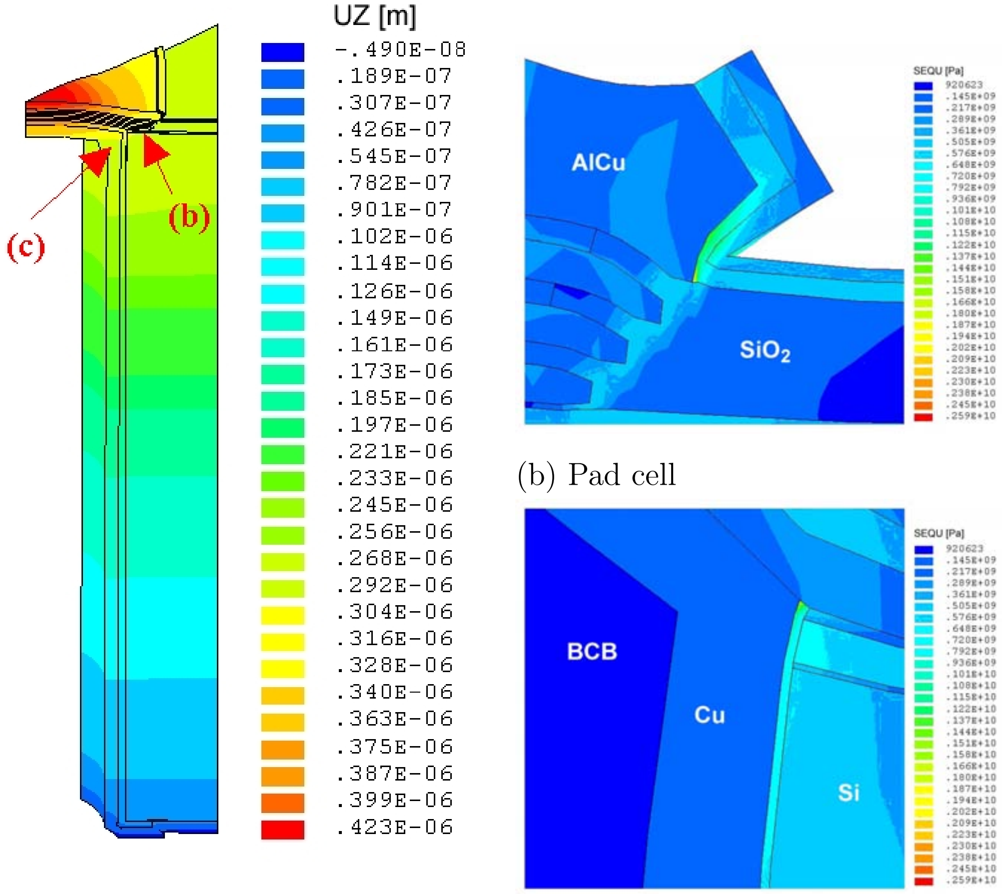
Figure 3.11: TSV model used for thermomechanical analysis. Figure (a) shows an overview of a TSV. Figure (b) shows the TSV bottom after complete TSV processing. A detailed description of geometries and film thicknesses used is shown in appendix C. Figure (c) shows the TSV entrance after complete TSV processing.

on the wafer level and the package is created afterwards by laser marking and scribing for singulation of the devices. A full encapsulation of the silicon is reached by a transfer molding process, which occurs usually at temperature of 175°C and at pressure of maximum 6MPa.
Stress distribution calculations within TSV structures were performed for two different conditions:

Test A Molding conditions in order to evaluate the TSV pad-cell toughness at temperatures of 175°C and simultaneously under high hydrostatic pressure (6MPa).

Test B Final bonding conditions when temperature reaches the highest value (400°C) during device assembly in order to evaluate critical spots of the TSV system.

Test A Molding processes uses pressures in the MPa regime. These pressures applied to MEMS packages like shown before are assumed to be critical for free standing pad-cells, which can be treated as a membrane. Electric contacts between front-side and back-side of TSV systems are made in this model a by Cu layer inside the TSV hole. This layer additionally strengthens the fragile stratified pad-cell against molding pressures. It is assumed that the Cu film thickness decreases about one third from 2.25μm at the TSV entrance at the wafer back-side to 1.5μm at the TSV bottom. Figure 3.12 (b) and (c) show the most endangered region during molding at temperature of 175°C and a pressure of 6MPa. The calculations predict the pad-cell structures used are strong enough to resist molding pressures. However, the thermal expansion of the Cu layer causes a convex shape of the pad-cell structure like it shown in figure 3.12 (b). A pad-cell displacement in z-direction of 8.5nm is predicted at the center of the pad geometry. This value is negligible for device reliability issues.
The large CTE mismatch between materials used cause large principal stresses especially in front-side passivation layers. The maximum stress is identified just in the corner of front-side passivation layers as shown in figure 3.12. Stresses inside films on the wafer back-side introduced by the given molding conditions are not higher than their fracture strength. It can be assumed, that the back-side films can withstand the external load. Figure 3.12 shows a maximum principal tensile stress of 1090MPa in the front-side SiN passivation layer. In addition, a stress of 811MPa is predicted inside the PMD. Both values estimated are higher than their fracture strength of 500MPa and are identified as weak point of this TSV approach.



(a) TSV overview

(b) Pad cell

(c) TSV bottom

Figure 3.12: Displacement and stress distribution of a TSV system during molding. Figure (a) shows the pad cell displacement in z-direction (displacement scale: 50x). Figure (b) shows the Mises stress distribution of the pad cell. Figure (c) shows the Mises stress distribution at the TSV hole bottom.

Test B Stress and strain in the TSV structure are even larger for temperature excursion from room temperature up to 400°C compared to values obtained by molding. Such a temperature excursion is necessary to activate the getter material [32]. The following calculations were performed only at this temperature excursion. The system was not loaded with pressure. A 200nm thick SiN layer was used for isolating purposes. This layer shows an unacceptable maximum principal stress value of 1.08GPa at the TSV sidewalls at 400°C. A film thickness enhancement up to 1000nm decreased the maximum principal stress to 541MPa, which is still above the critical fracture strength. However, the SiN layer should be as thick as possible since a 1000nm thick SiN layer does not cause a significant change of the maximum principal stresses in the front-side pad-cell layers.

The larger deformation of the pad-cell during temperature excursion can be assumed compared to values obtained from the molding calculations. A displacement in z-direction of about 350nm was estimated like it is shown in Figure 3.13. Thus, primarily the CTE mismatch causes the displacement or bending in z-direction. The pad-cell passivation on top of the last metallization layer is still the critical point of this TSV design. Maximum principal stresses over 1GPa were predicted for this point, which can cause yield losses. However, the operating temperature of MEMS devices is normally not 400°C. Further experiments must show how getter activation influences the MEMS functionality during the device life time. In addition, experiments must show how the pad-cell displacement in z-axis influences the hermetical behavior of the pad-cell structure.

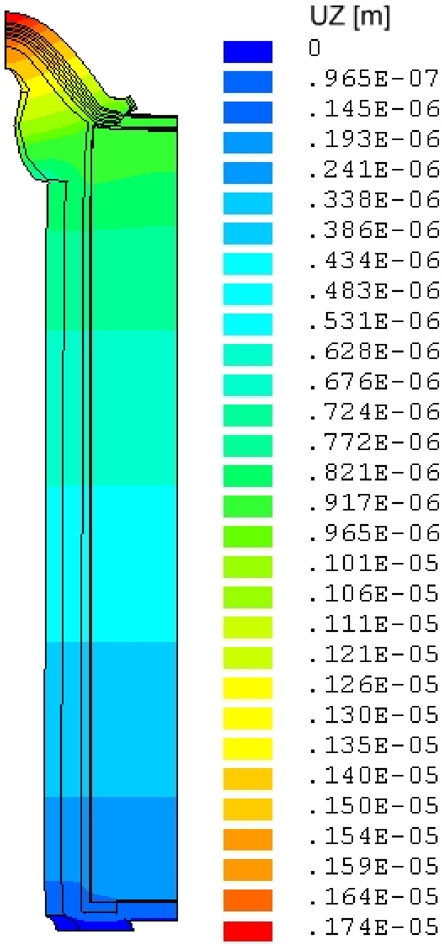


Figure 3.13: Pad-cell displacement due to temperature excursion from room temperature to 400°C (displacement scale:5X).

3.4.3 Hermetic criterion

Operation modes of several MEMS depend on vacuum levels established. For instance, vacuum levels of 0.1mbar are established for resonant operating MEMS at Fraunhofer ISiT. This vacuum level must be guaranteed for the complete device life time of 15 years. Possible in-coming gases are gettered by deposited materials. However, free standing pad-cells structures must be hermeticaly dense in order to allow a usage of MEMS packages with integrated TSV for a defined life-time of 15 years. Reinert showed that wafer-level based MEMS packages with a cavity of 1nl allow a leakage rate of $1.26 \cdot 10^{-16} mbar \cdot l/s$ [32] to full fill this requirement. Thus, this leakage rate has to be targeted for hermetic TSV in MEMS packages.

3.5 Electrical Specifications

TSV are an electrical conduction path in electronic devices. Films deposited induce electrical resistances and capacitances which contribute to parasitic effects of the complete system. The following considerations show estimations of electrical TSV elements. The last chapter showed that a wafer thickness of $>300\mu$m should be targeted in order to establish a robust process flow without a significant yield loss. In addition, the chosen TSV diameter is larger compared to the diameter used in the mechanical consideration. The processes described in chapter 4 are easier to develop for larger TSV diameters. Thus, a diameter of 80μm is considered in the following description.

3.5.1 Dielectric film

TSV metallization layers are isolated from the Si substrate by an isolating material. This layer structure gives a parasitic capacitance very similar to a capacitance of a metal oxide-semiconductor structure (MOS) as shown in figure 3.14. Thus, the parasitic TSV capacitance (C_{TSV}) is given by the series connection of the isolation capacitance ($C_{Isolation}$) and the semiconductor depletion-layer capacitance ($C_{Depletion}$) as indicated in figure 3.14:

$$C_{TSV} = \frac{C_{Isolation} \cdot C_{Depletion}}{C_{Isolation} + C_{Depletion}} \tag{3.2}$$

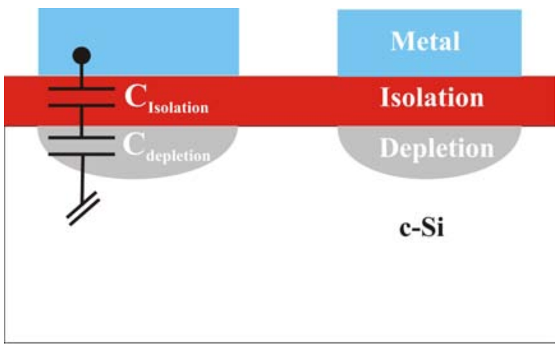


Figure 3.14: Schematic of the parasitic capacitance in an insulated metal strip.

$C_{Isolation}$ is given locally even for the given TSV ring symmetry by

$$C_{Isolation} = \epsilon \frac{t_{Isolation}}{A_{Isolation}} \tag{3.3}$$

where ϵ, $t_{Isolation}$ and $A_{Isolation}$ are the permittivity ($\epsilon = \epsilon_0 \cdot \epsilon_{Isolation}$), thickness and surface area of the isolating material inside the TSV, respectively. Dielectric constants of silicon oxides and nitrides vary between 4-6 and 6-9, respectively. An isolating material with a dielectric constant of 6 and a thickness of 1μm results in a capacitance per unit area of $5.3nF/cm^2$. The depletion-layer capacitance is given by [43]

$$C_{Depletion} = A_{TSV} \sqrt{\frac{q\epsilon_0\epsilon_{Si}N_B}{2\left(2\frac{kT}{q}\ln\frac{N_B}{n_i} - V\right)}} \tag{3.4}$$

Where ϵ_{Si} is the permittivity of silicon, N_B is the lightly doped bulk concentration, n_i is the intrinsic carrier concentration, k is the Boltzmann constant, T is the temperature and q is the elementary charge. For zero bias voltage the depletion capacitance per unit area can be calculated to 32.6 nF/cm^2 (for $N_B = 4 \cdot 10^{15}cm^{-3}$). Thus, depletion-layer capacitances are larger than isolation capacitances. It can be concluded that

$$C_{TSV} \approx C_{Isolation} \tag{3.5}$$

Isolating and electric conducting materials should be deposited only in ring symmetry due to fact that process times for a complete TSV hole filling are not acceptable. The capacitance of ideal ring symmetry is given by

$$C = \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\ln\frac{r_{out}}{r_{in}}} \tag{3.6}$$

where ϵ, L, r_{out} and r_{in} are the relative permittivity ($\epsilon_0 \cdot \epsilon_r$), the TSV depth, the outer TSV hole radius and TSV hole radius subtracted by the isolating film thickness, respectively. Figure 3.15 shows capacitance values of various isolating materials and a TSV geometry of 80μm in diameter and 400μm in depth. This graph shows, for instance, that SiO layers of 1μm deposited inside TSV with a diameter of 80μm have a parasitic capacitance of $8.7fF$ per μm hole depth. Table 3.5 summarizes electrical capacitance values per TSV length in dependent on isolating materials used at a film thickness of 1μm.
These calculations are performed for constant film thicknesses of isolating materials deposited. Literature shows that film thickness gradients occur especially for deep holes or when low temperature deposition processes are used [44][45]. Equation (3.6) changes to

$$C(x) = \int \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\ln\frac{r_{out}}{r(x)}} dx \tag{3.7}$$

where $r_{(x)}$ is now a function of the TSV hole depth. Equation (3.8) describes a possible **exponential profile** of the isolating material deposited on the TSV hole sidewalls.

$$r(x) = d_0 \cdot e^{-x/\tau} \tag{3.8}$$

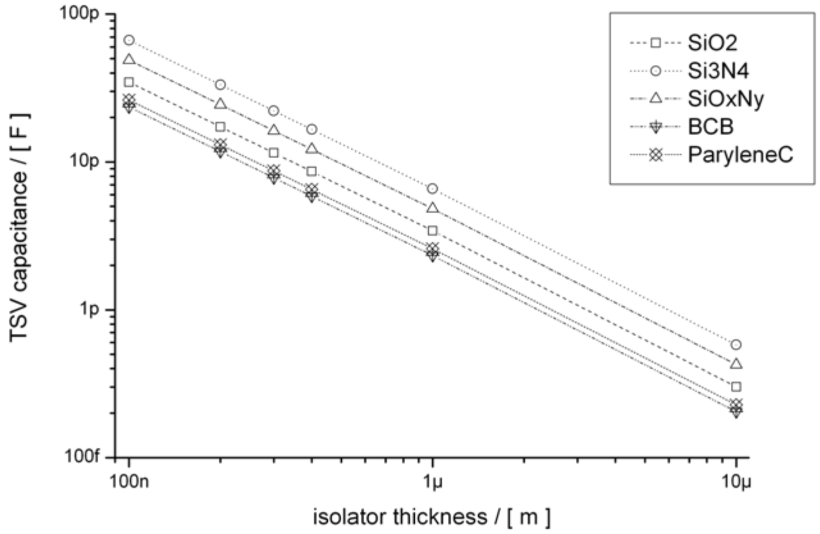


Figure 3.15: TSV capacitance dependent on film thickness and isolating material.

Material	**Dielectric constant**	**Relative capcitance** [fF / μm]
SiO	3.9	8.7
SiN	7.5	16.7
SiON	5.5	12.2
BCB	2.65	5.9
Parylene C	2.95	6.6

Table 3.5: Dielectric constant values of various isolating materials and calculated capacitance values per TSV length.

where d_0 and τ are the starting film thickness and the thickness when 63% of the decay is reached, respectively. Applying equation (3.8) to (3.7) and introducing $\lambda = \frac{1}{\tau}$ results to

$$
\begin{aligned}
C(x) &= \int \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\ln(r_{out}) - \ln(d_0) - \ln(e^{-\lambda \cdot x})} \, dx \\
\Leftrightarrow C(x) &= \int \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\ln(r_{out}) - \ln(d_0) + \lambda \cdot x} \, dx \\
\Leftrightarrow C(x) &= \int \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\lambda \cdot x + \ln(r_{out}) - \ln(d_0)} \, dx \\
\Leftrightarrow C(x) &= 2 \cdot \pi \cdot \epsilon \cdot L \cdot \frac{1}{\lambda} \ln|\lambda \cdot x + \ln(r_{out}) - \ln(d_0)|_{x=0}^{x=L} \qquad (3.9)
\end{aligned}
$$

Equation (3.9) changes to

$$
C(x) = \begin{cases} \frac{2}{\sqrt{\Theta}} \cdot \arctan\left(\frac{2 \cdot \gamma \cdot x + \nu - 2 \cdot \gamma}{\sqrt{\Theta}}\right)\Big|_{x=x_0}^{x=L} & \text{for } \Theta > 0 \\ \frac{1}{\sqrt{|\Theta|}} \ln\left|\frac{2 \cdot \gamma \cdot x + \nu - 2 \cdot \gamma - \sqrt{|\Theta|}}{2 \cdot \gamma \cdot x + \nu - 2 \cdot \gamma + \sqrt{|\Theta|}}\right|\Bigg|_{x=x_0}^{x=L} & \text{for } \Theta < 0 \end{cases} \qquad (3.10)
$$

if a **linear profile** is observed for the deposition process used. The derivation of equation (3.10) and the definition of Θ are given in appendix A. Knowledge of the deposition profile is necessary for the calculation of the 'real' capacitance value. Lower capacitance values can be assumed for any film thickness profile compared to the ideal case. Thus, non constant film thicknesses of the isolating materials results in a reduction of capacitive parasitic effects. However, films deposited must be structural dense for any deposition profile in order to separate electrical potentials between the electric conducting TSV material and the Si-substrate. The dielectric strength describes the quality of isolating materials. This parameter is defined by the maximum electrical field which can be applied to isolating materials before a structural breakdown occurs. Literature reports values between $4MV/cm$ and $12MV/cm$ for different isolators, respectively [46][47]. Isolating materials inside the TSV geometry must show similar values for the dielectric strength.

3.5.2 Metallic film

Electric conducting materials are deposited inside TSV geometries and the wafer back-side in order to carry electronic signals from pad-cells on the wafer front-side to new pads formed on the wafer back-side. Metals with low resistivity values are preferably used, because the TSV resistance formed influences electrical propagation times or sensor sensitivities. Some applications does not allow TSV resistance values of 1000Ω, which are reported for Poly-Si TSV like it is shown in chapter 2.2.2. Therefore, metals like Cu, Al, Ag, Au and W must be considered as conducting materials in TSV. Figure 3.16 shows values of electrical resistances for ring metallization (R_{Metal} in a 400μm deep and 80μm in diameter) in dependent on the film thickness deposited. Different materials are indicated.

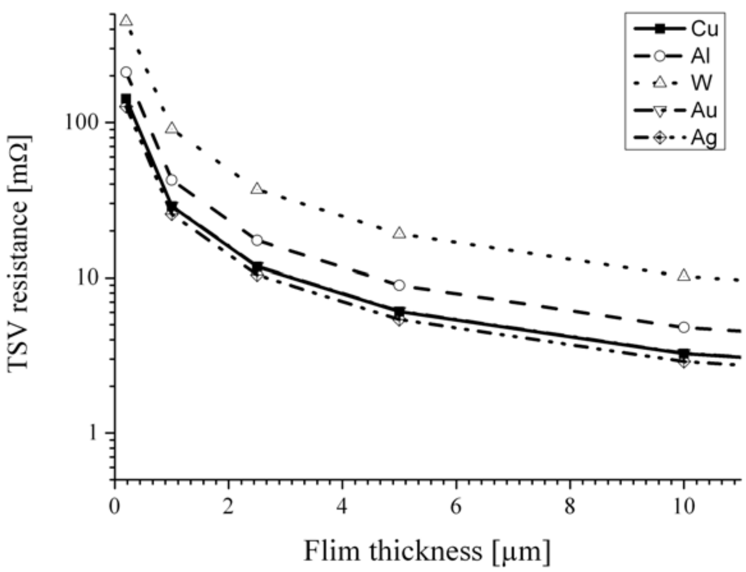


Figure 3.16: Electrical resistance values for a ring metallization in a a 400μm deep and 80μm in diameter TSV dependent on the film thickness deposited.

The calculations are based only on a deposition of materials indicated. Chapter 3.2.1 shows that diffusion barriers must also to be implemented in metallization schemes. The electrical resistance of this barrier $R_{Barrier}$ contributes also to the complete TSV resistance. Barrier resistance can be treated as a parallel resistance in an easy model and the TSV ring metallization resistance R_{ring} results to

$$R_{ring} = \frac{R_{Metal} \cdot R_{Barrier}}{R_{Metal} + R_{Barrier}} \tag{3.11}$$

Specific electrical resistances of barrier materials are commonly 100 times larger compared to metallic conduction film like Cu. Thus, barrier materials carry only a small portion of electrical signals and do not change significantly the value of the TSV ring metallization. However, barrier materials are also deposited on the TSV bottom. Electrical signals have to pass this layer. The electrical resistance of one complete TSV under the consideration of barrier resistances results to

$$R_{TSV} = R_{ring} + R_{bottom} \tag{3.12}$$

R_{bottom} is significant for TSV diameter in the range of 1μm or less, because the resulting resistance is in the order of several $m\Omega$. TSV geometries targeted here (TSV diameter >30μm) allow the assumption that

$$R_{TSV} \approx R_{ring} \tag{3.13}$$

Resistance values shown in figure 3.16 are based on a ring metallization with a constant film thickness. Plummer [45] or Baer et al [48] show that thickness gradients are observed for different metallization processes used. In this case, ring metallization resistances are given by:

$$R_{ring}(x) = \int_0^L \rho_{metal} \frac{L}{\pi} \frac{1}{(r_o^2 - r_i^2(x))} dx \tag{3.14}$$

where ρ_{metal}, L, r_o^2 and r_i^2 are the specific electrical resistance of the metal used, the TSV hole depth, the outer radii of the TSV hole and the TSV radii subtracted by the film thickness of the deposited metal, respectively. $r_i(x)$ is a function of the deposition profile. Ring metallization resistances result to

$$R_{ring}(x) = -\frac{\rho \cdot L}{\pi} \begin{cases} \frac{2}{\sqrt{\Theta}} \cdot \arctan\left(\frac{2 \cdot m \cdot x + 2 \cdot m \cdot b}{\sqrt{\Theta}}\right)\Big|_{x=x_0}^{x=L} & \text{for } \Theta > 0 \\ \frac{1}{\sqrt{|\Theta|}} \ln\left|\frac{2 \cdot m \cdot x + 2 \cdot m \cdot b - \sqrt{|\Theta|}}{2 \cdot m \cdot x + 2 \cdot m \cdot b + \sqrt{|\Theta|}}\right|\Bigg|_{x=x_0}^{x=L} & \text{for } \Theta < 0 \end{cases} \tag{3.15}$$

for a **linear decay** function of $r_i(x) = m \cdot x + b$ and the following substitution

$$\Theta = 4 \cdot m \cdot \left(b^2 - r_a^2\right) - (2 \cdot m \cdot b)^2 \tag{3.16}$$

Equation (3.15) changes to

$$R_{ring}(x) = \frac{\rho \cdot L}{\pi} \left[\frac{x}{r_a^2} + \frac{\tau}{2 \cdot r_a^2} \ln\left|r_a^2 + d_0^2 \cdot e^{\frac{-2 \cdot x}{\tau}}\right|\right|_{x=0}^{x=L} \tag{3.17}$$

for an **exponential decay** function of $r_i(x) = d_0 \cdot e^{-\frac{x}{\tau}}$.
Metal thickness gradients close to zero are preferred in TSV applications, because narrow profiles increase electrical resistance values.
Section 2.2.4 shows a mass flow sensor for liquid or gaseous media. The functional structures of this sensor are based on two resistive TiN,Ti,TiN lines with a resistance of 50Ω. The standard variation of the resistance difference between two lines on one sensor element is only 0.1%. This small variation allows precise flow measurements. Thus, TSV integrated inside this sensor must show electrical resistance values below 50mΩ in order to allow precise flow measurements. In addtion, it is important that electrical TSV resistances on one sensor elememt show also a small standard derivation. This electrical TSV specification is for the mass flow sensor essential in order to maintain the system functionalty. It is not useful to integrate TSV in this sensor if only the corrosion problem and micro-turbolences are neglected.

3.6 Test design

The following TSV test design is developed based on the considerations of the previous chapters. A pad-cell with only one metallization level is deposited on 6 inch (100) wafer. Figure 3.17 indicates the different layers deposited. The pad-cell structure basically is composed of isolation, metal and passivation layers. This film stack is in detail a Si_3N_4 from low pressure chemical vapor deposition (LP-CVD), a phosphorus silicate glass (PSG) deposited by plasma enhanced chemical vapor deposition (PE-CVD) and a low temperature oxide (LTO) from a low temperature LP-CVD for the isolation layer. A sputtered Ti, TiN and AlCu metallization film and a passivation layer of silicon nitride and silicon oxide deposited by PE-CVD completes the pad-cell structure. Layer film thicknesses are indicated in figure 3.17. This layer structure is similar to common pad-cell structures and materials of CMOS designs and also consists of materials which are used for MEMS. Daisy chain structures are formed on wafer front-sides in order to allow electrical measurements from the wafer back-side. Pad sizes are varied between 100μm, 150μm and 200μm. In addition, a staggered placement of 150μm pads is tested.
Mechanical considerations showed that wafer thicknesses >300μm should be targeted for robust wafer processing. Therefore, wafer with thicknesses of 300μm and 400μm are used. This wafer thickness allows only hole geometries with an 90° angle in respect to the wafer surface as shown in table 3.2. TSV hole diameters of 80μm are used. Amorphous SiN-films with incorporated hydrogen impurities (a-S$_x$iN$_y$:H) are used as isolation material due to the good diffusion barrier characteristics against metals. For instance, Cu was not diffusing

Figure 3.17: Film stack of a pad cell used in the test design (Film thicknesses: Si_3N_4 100nm, PSG 250nm; LTO 750nm, Ti 40nm, TiN 100nm, AlCu 1.4μm, SiN 500nm, SiO 500nm).

through a-Si_xN_y:H at the temperature range targeted during device operation. The PMD and the isolation layer underneath the front-side metallization are removed by dry- and wet-chemical etching processes. The metallization scheme consists out of an adhesion promoter (Ti), a diffusion barrier (TiN) and a highly electrical conducting film. Al and Cu are taken into consideration as conducting film. a-Si_xN_y:H is used again as passivation film, because silicon nitrides show good chemical resistance against water or moisture penetration inside the material. This passivation film avoids metal corrosion.
A redistribution layer is formed on the wafer back-side based on the metallization material deposited inside the TSV and the wafer back-side. Figure 3.18 show the Daisy chain structures realized on the wafer front-side and the designed wafer back-side redistribution layer.

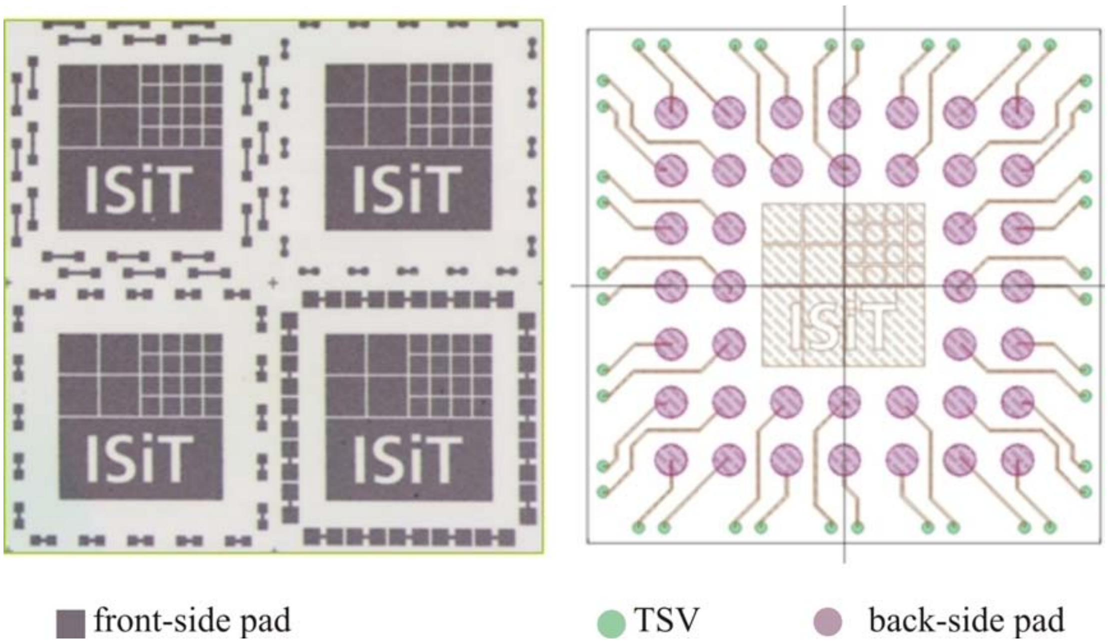


Figure 3.18: Test design on wafer front- (left) and back-side (right). Daisy chain structures on the wafer front-side allow an electrical characterization only from the back-side.

4 Key technologies

Chapter 3.1 showed a process flow for a TSV formation in >300μm thick wafer and consequences for wafer geometries, films depositions and TSV system parameters. Technological aspects based on these considerations are presented in this chapter. Processes needed can be divided in three major key technologies:

- Hole formation
- Film deposition
- Pattern transfer

4.1 Hole formation

TSV hole formation needs a removal of the wafer material (c-Si) down to the PMD. In addition, an electrical contact between the front-side pad metallization and the TSV metallization layer deposited is only possible if the PMD is removed completely. Figure 4.1(a) shows a TSV implementation in MEMS or IC devices with a vertical etched hole. Figure 4.1(b) indicates required TSV etch profiles underneath the front-side pad. First, c-Si is etched anisotropically. Second, an isotropic (red line) or anisotropic (red dotted line) etch process removes the PMD. The following overview shows common etching techniques and discusses the usefulness of these etch processes for TSV hole formation
There are mainly two methods used for the etching of silicon based materials or silicon itself. First, is wet etching a simple and cheap method. Wafers are immersed into basins filled with liquid etchants. Layers exposed are etched simultaneously even if several wafers are placed into the basin. Wet etching processes were developed for all steps during semiconductor device fabrication. For instance, hydrofluoric acid HF etches SiO_2 by a pure chemical process. The chemical overall reaction is

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{4.1}$$

Reaction 4.1 describes the typical reaction pathway of wet etching. Etchants (HF) react with films immersed (SiO_2) and form water-soluble byproducts (H_2SiF_6) or gases. Depletion of etchants eventually occurs by forming byproducts. Thus, buffering agents like

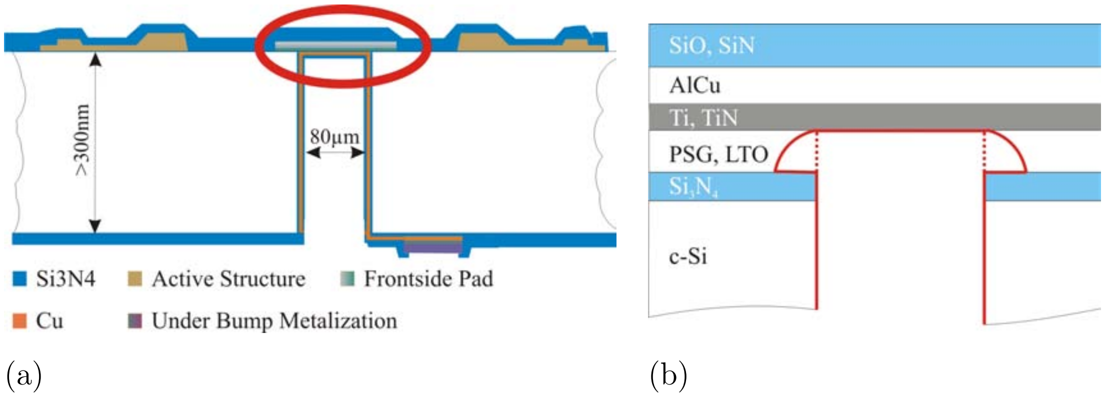


Figure 4.1: TSV etch profiles needed for the given specification. (a) shows a TSV implementation inside wafer with an vertical etch profile. The red marked area is magnified in (b). Isotropic (red line) and anisotropic (red dotted line) PMD etch profiles

ammonium flouride (NH_4F) are added to stabilize the HF over time. This mixture is called buffered oxide etch (BOE).
An indirect chemical pathway to etch c-Si is known. Chemicals like nitric acid (HNO_3) decompose in water to nitric dioxide (N_2O), which oxidizes Si surfaces. Adding HF dissolves the SiO_2 formed which is describe under equation (4.1). This isotropic c-Si etching process based on a HF and HNO_3 mixture is given by

$$Si + 2NO_2 + 2H_2O \rightarrow SiO_2 + H_2 + 2HNO_2 \tag{4.2}$$
$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{4.3}$$

TSV geometries targeted require an $>300\mu$m deep hole with an angle of 90° in respect to the wafer surface. This wet chemical c-Si etch process can not fulfill these requirements. First, etching rates of Si are in the order of 100nm min^{-1} to 200nm min^{-1} [49]. Thus, the etch time is too long to form the TSV hole if an economically TSV approach is considered. In addition, wet etching processes are predominantly pure isotropic and cause large undercut profiles underneath the hard mask or photoresist.
KOH etching is a second wet chemical way to remove c-Si. Etch rates are higher compared to the previous described method. In addition, the etch rates depend on the crystallographic orientation of the c-Si. Si in the [100] direction is etched much faster compared to the [111] direction, because the (111) planes are most closely packed and etch more slowly. Cavities with an angle of 54.7° in respect to the (100) plane are formed. Linder [11] and

Rassmussen [30] showed the capability of using KOH for TSV hole formation. The pad-cell pitch in CMOS devices (see chapter 3.3) does not allow the use of KOH for the TSV hole formation due to the etch profile obtained. TSV holes formed by KOH etching will interact with other TSV holes or dicing lines. A signal separation is not possible in this way.
Dry etching or plasma etching was developed in the 1970s to etch SiN passivation layer on top of SiO_2 and Al, because wet etching processes known for SiN were not selective enough to SiO_2 or caused large under-cut profiles [45]. CF_4 and O_2 gas mixtures in a plasma atmosphere allow an SiN etching with high anisotropies and good selectivity to SiO_2. Similar processes were developed for SiO_2, Si or even metals like TiN. The chemical or physical behavior of plasma etching characterize the etch process used. Reactive neutral chemical species, often free radicals, etch material in a pure chemical manner. Radicals are transfered from the process chamber to the substrate and adsorb at surface sites. Free radicals are neutral species which cause an isotropically arrival angle even under an applied electrical field. In addition, free radicals like F^* or CF_3^* show low sticking coefficients. Thus, the radicals tend to bounce around before surface reactions take place. Radical fluxes underneath mask result from this low sticking coefficient. Thus, plasma etching is not usable for the formation of the TSV holes. First, the under-cut is too large to etch c-Si 300μm deep hole. Second, plasma etching takes place in pressures regimes of 100mTorr and 1Torr. The mean free path is too low at these pressures in order to observe a direct movement of radicals to the TSV hole bottom. PMD are not attacked by plasma etching like it is shown in figure 4.2.

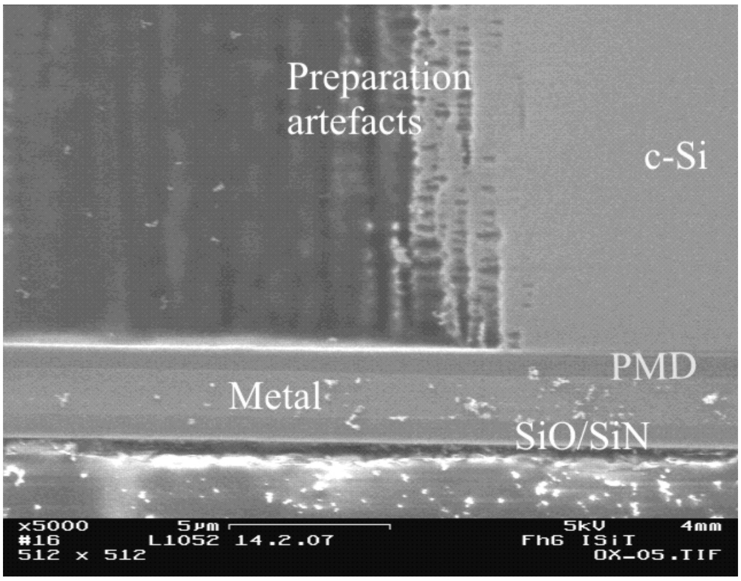
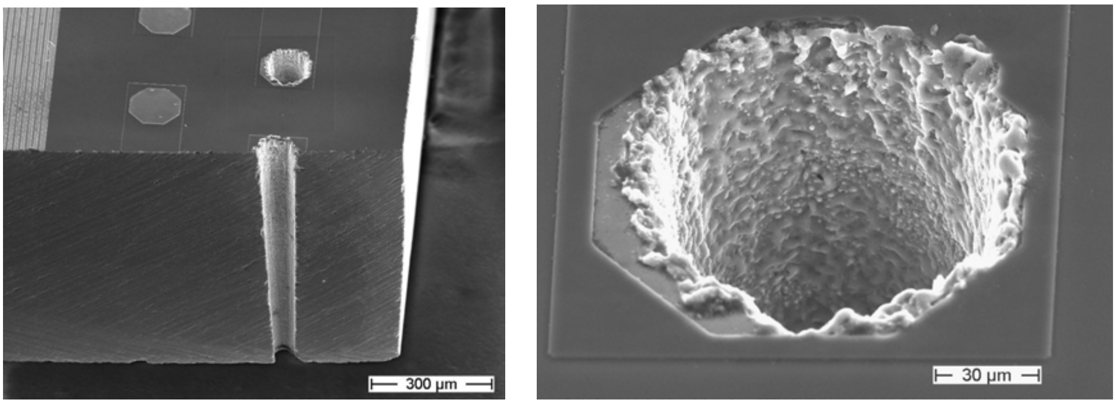


Figure 4.2: Cross section of a pad cell after a plasma etch process for SiO_x etching. The film is not eroded.

Ions can etch material in plasma systems by physical sputtering. Ions formed in the plasma are accelerated by an applied electrical field and hit surfaces under anisotropical arrival angles. Material is physically dislodged by incoming ions and pumped away. Anisotropic etch profiles characterize this etch technique. Sputter yields defines etch rates of this etch process. Coburn et al showed that etch rates increase if gases are also introduced to the chamber [50]. However, TSV hole formation by physical etching is not possible. Possible mask materials show a too low selectivity compared to c-Si to form a $>300\mu$m deep hole. PMD etching with an anisotropic etching process is preferred. Experiments showed that the available equipment does not allow PMD etching by physical etch processes.
High energy lasers allow a removing of all materials used in this TSV approach. Focused laser beams cause a sublimation of the material by an interaction with the material. The c-Si in the gas phase is pumped away and the hole formation stops when the final hole depth is obtained. The laser is moving to the next TSV position and forms the next hole. The major advantage of this sequential process is the possibility to change the TSV hole layout without immense costs. Thus, expensive photo lithography masks are not required. Figure 4.3 (a) shows a 675μm deep TSV hole formed by laser ablation. Figure 4.3 (b) indicates the entrance area of the laser. A defined etch stop is difficult to realize due to the non-selectivity of the laser process to certain materials. The probability that the front-side pad-cell is partially removed is high. Thus, a hermetic dense TSV can not be guaranteed

for the TSV hole formation by laser ablation.



(a) (b)

Figure 4.3: TSV hole formation by laser ablation. (a) 675μm deep TSV holes formed by laser ableation. (b) Close up of the TSV entrance area. A Si redeposition is observed.

The following sections show etch processes to form TSV holes for the given specifications under chapter 3.3.

4.1.1 Silicon and Silicon-nitride etching

Method

Laermer et al. have developed an anisotropic c-Si etch technique for high aspect ratio profiles and a good dimensional control [51]. This technique is called *Deep Reactive Ion Etching* (DRIE) and is based on an iterative deposition and etch cycle. An initial polymer etch inhibitor, commonly *octafluorocyclobutane* C_4F_8, is deposited on top of the wafer and inside the pattern as it is shown in Figure 4.4. This polymer is etched preferably anisotropically at the hole bottom during the etch cycle due to the accelerated SF_6^- ions. The c-Si underneath the polymer is etched isotropically after the polymer is removed in this region. The etch parameters must be chosen in such a way that the polymer film at the sidewalls is thick enough to protect the c-Si during the complete etch time. The deposition step is repeated before the polymer is completely removed from the sidewalls. This cycle continues until the desired etch depth is obtained. Cleaning processes like O_2 plasmas remove remaining polymer residuals after the last etch cycle is performed. The DRIE process chemistry used etches c-Si as well as SiN-layers [49]. Thus, the c-Si wafer and the Si_3N_4 of the PMD are etched by DRIE in one process step.

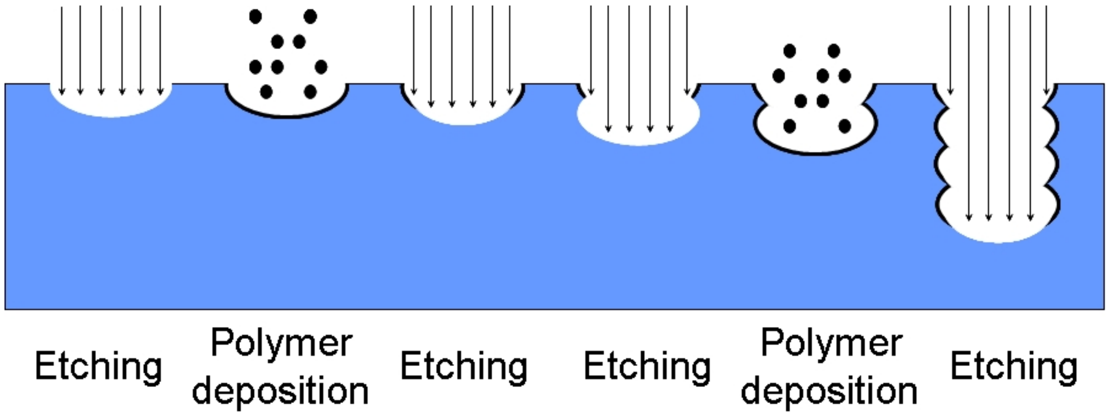


Figure 4.4: Etch cycles of deep reactive ion etching (DRIE).

Results and Discussion

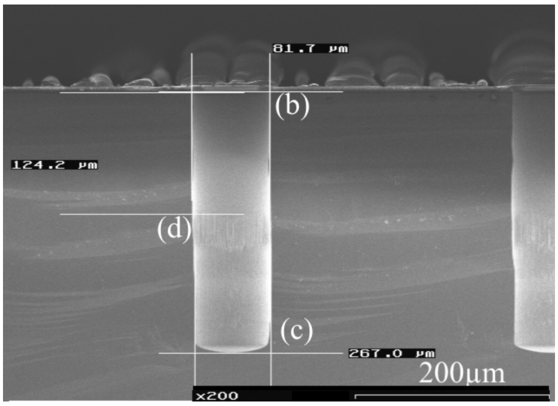
The experiments are divided in two parts

Experiment A Etching of >300μm deep holes in c-Si

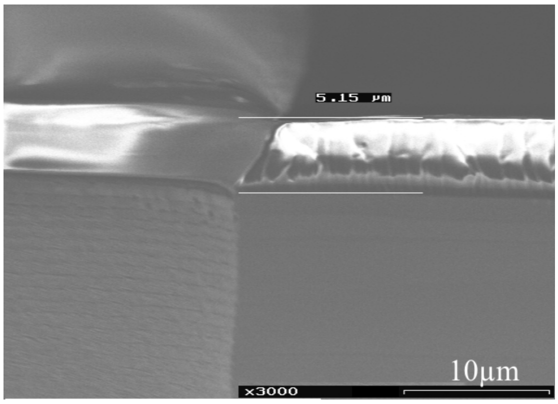
Experiment B Si_3N_4 etching at the hole bottom

Experiment A Pattern transfer inside c-Si needs masking materials on top of wafers. Materials used must show high etch selectivity against the etchant used. SiO_2 or photoresist are appropriate mask materials for etching processes based on SF_6^- ions. The etch selectivity between SiO_2 and c-Si is 1:100. This selectivity requires a >3μm thick SiO_2 layer to form >300μm deep structures. Common deposition machines used in semiconductor foundries are not designed for such thick films. For instance, the long process time can cause a material accumulation inside the exhaust pipes, which can result in plugged pipes. Thus, a thick photoresist layer (10 μm, AZ4562) was deposited on the wafer back-side for use as an etch mask during DRIE. Wafer surfaces were primed prior to resist coating in order to ensure proper photoresist adhesion. The wafers were exposed to *hexamethylsilizane* (HMDS) at 90°C in a gas phase to remove hydroxyl groups from wafer surfaces. A spin coating process deposited the 10μm thick photoresist on the wafer back-side. A so called soft bake at 90°C for 30min drove solvents out of the photoresist and enhanced also the film adhesion. Literature shows that thick photoresist require absorbed moisture to enhance the solubility of exposed parts during resist development [52]. The amount of absorbed moisture did not change the lithography quality, during the experiments performed in this work. The photoresist was exposed through a 7 inch wafer mask and afterwards developed

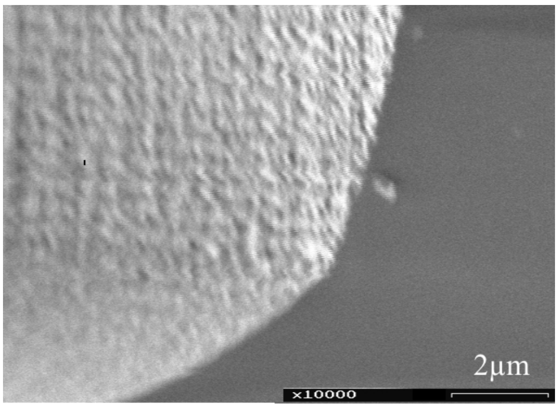
in a KOH based developer. A final photoresist bake in a convention oven at 80°C for 6h minimized the resist erosion during DRIE.
The c-Si is etched by using DRIE via a patterned photoresist on the Alcatel 601 etch tool. The process required to etch >300μm deep holes is not a standard etch process. The parameters are optimized in such a way that the etch rate is high as possible and the sidewall surface roughness is low as possible. Figure 4.5 shows the obtained vertical etch profile at different positions.



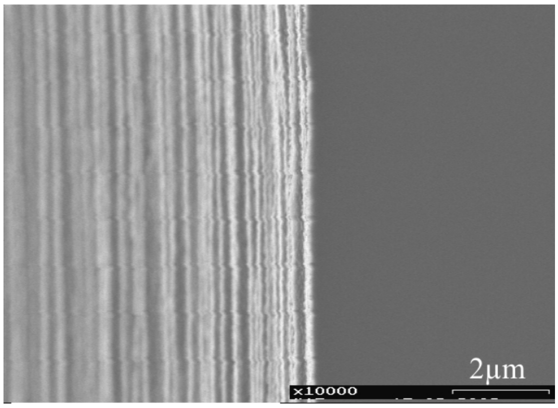
(a)Overview



(b) Hole entrance



(c) Hole bottom



(d) Hole center

Figure 4.5: TSV hole formed by DRIE. (a) TSV etch profile obtained by using DRIE (b) Cross section of the hole etched at the hole entrance (c) Cross section of the hole etched at the hole bottom (d) Cross section of the hole etched at the hole center.

Figure 4.5(b) indicates that 5μm photoresist were eroded for an etch time of 50 minutes. Longer etch times are possible without a critical ion interaction with the wafer surface.

It is possible to obtain a final TSV hole depth of >300μm with this resist. The TSV sidewalls showed the DRIE characteristic scallops at the hole entrance area. The sidewall topography changed at a hole depth of 120μm due to the SF_6^- ion flux. The ions arrived anisotropically at the wafer surface. However, there was a certain probability that ions arrive with an angle different than 90° in respect to the wafer surface. These ions caused an enhanced etching of the etch inhibitor on the sidewalls. Longer etch times did not change the locations of the observed grooves. This showed that the quality of the inhibitor was not time dependent. In addition, TSV holes etched with diameters of 50μm have not shown any grooves. Figure 4.6 indicates that the incoming ion flux, which arrives at the surface under the same angle α, hits sidewalls at higher hole positions for smaller hole diameters. Thus, it can be assumed that the adhesion between sidewalls and the inhibitor polymer varies with the hole depth.

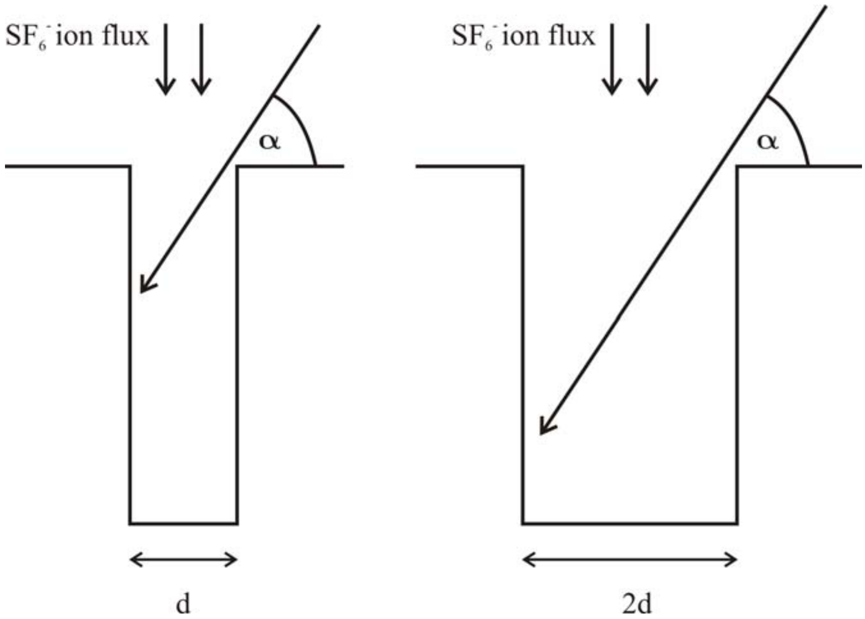


Figure 4.6: Maximum possible depth of incoming SF_6^- ions which arrive under an angle of α.

Previous investigations were performed on 675μm thick blanket c-Si wafer and the holes were not etched through the entire c-Si, which is required for the TSV system targeted. Thus, the DRIE process must stop on the PMD of the front-side pad. Isolating etch stop materials will most likely result in notching effects. Notching effects appear during overetching at the TSV hole bottom. The incoming ions charge the PMD electrically. This effect causes scattering of the incoming ions to the sidewalls and enhance the lateral etch rate at the c-Si – PMD interface. DRIE parameters used showed a maximum notching

between 3μm and 5μm.
Wafer used were thinned to 300μm or 400μm in order to reduce the challenge of the deposition processes. Wafer thinning was performed in different steps [16]. A coarse grinding removed most of the silicon, before a fine grinding defined the back side surface. A wet chemical stress release etch was required, because mechanical thinning introduced different zones of damages. Handling without this etching resulted in low wafer yield due to the introduced large wafer bow by the mechanical stress [16]. The wafers broke during the handling in different process steps. However, a TSV processing with a stress release etch after the fine grinding showed also a reliability risk. The DRIE etching behavior of these thinned wafers was different compared to blank substrates. A chipping was observed at the entrance of the TSV, like it is shown in Figure 4.7 (arrow (b)). The arrow (a) indicates the preferential grinding wheel direction. It can be assumed that the observed chipping results from the wheel direction. To give a detailed explanation of the interaction of the damage zones and the wheel direction is out of the scope of this thesis. It should be mentioned, that the observed cracks are not comparable with Mouse-bits [53] created during DRIE, because Mouse-bits are time related artifacts and the observed cracks are also observable after short etching times.

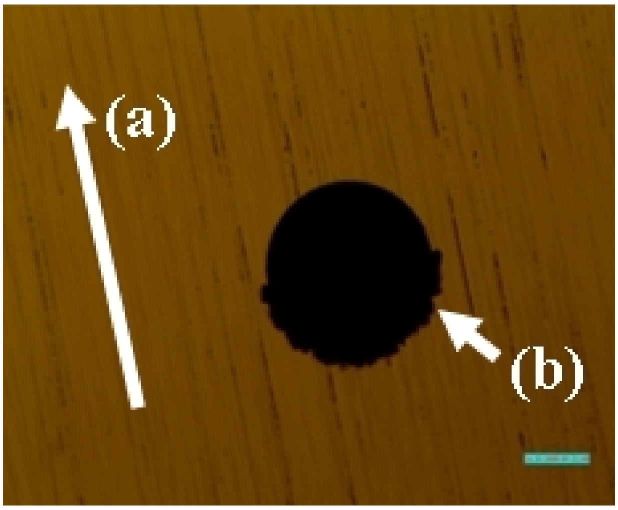


Figure 4.7: Etched hole from the wafer back-side.

Previous investigations at ISiT have shown that etch inhibitor residuals on etched structures remained even after an appropriate cleaning procedure. These residuals are Teflon^{TR} based compositions, which degrade the adhesion of materials deposited on these surface sites. TSV holes formed were cleaned by a combination of wet (RER and EKC) and dry (O_2 plasma at 250°C, 5min) processes. Outgasing measurements at 500°C showed no residuals after these cleaning procedures. Figure 4.8 shows this outgasing measurement of a sample with etched holes and without hole. The measured ion current is the same and it can be concluded that no polymer residuals are in the cavities.

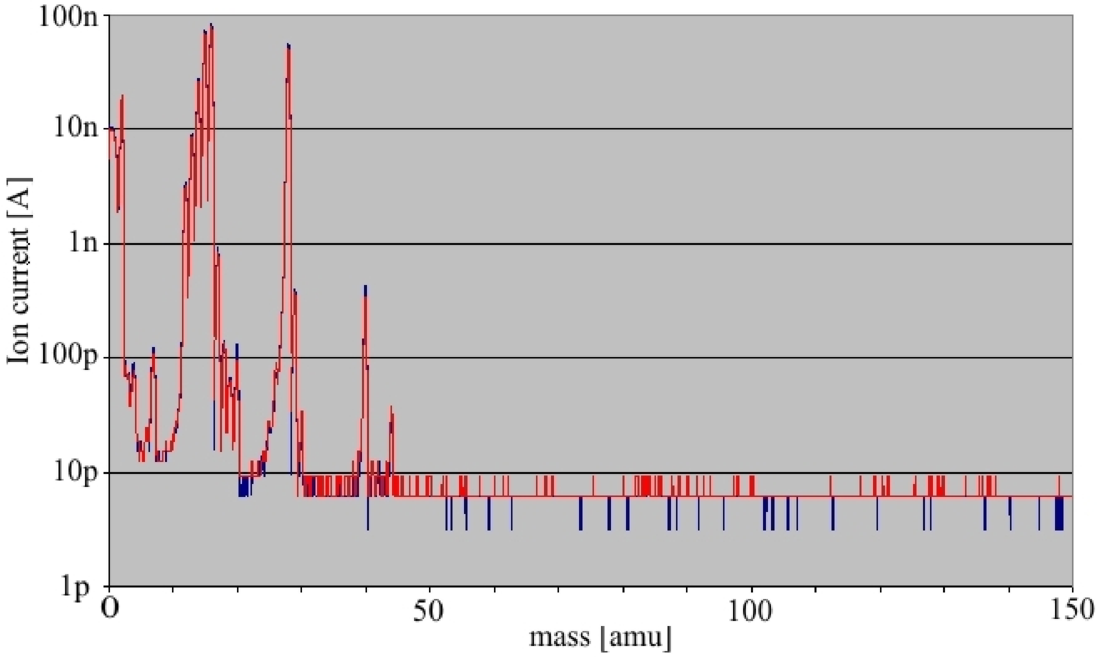
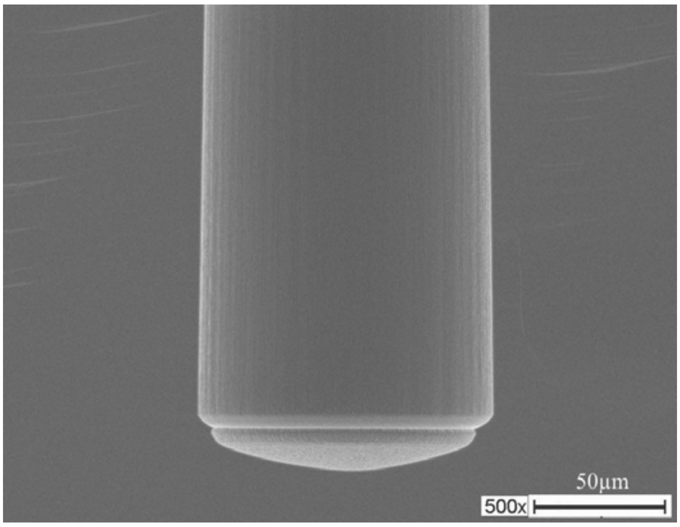


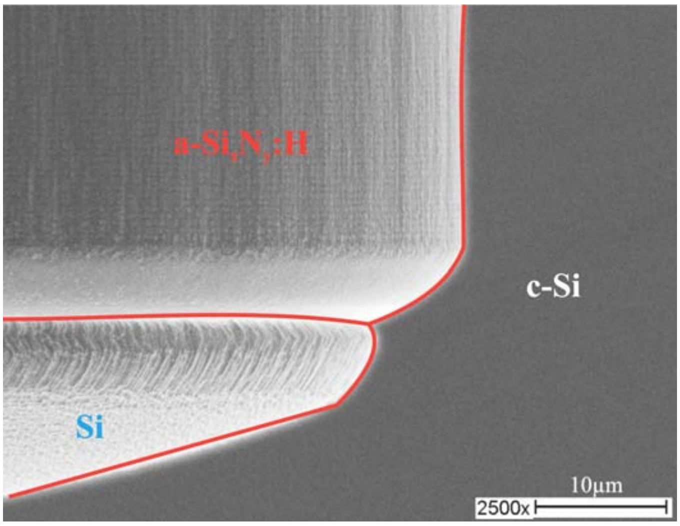
Figure 4.8: Outgasing measurement of a sample with etched (DRIE process) cavity (red curve) and without cavity (blue curve). The difference spectrum is zero and it can be concluded that no polymer residuals are present after the DRIE etch process.

Experiment B The TSV flow targeted requires two silicon nitride etching processes. The first PMD layer deposited (see chapter 3.6) is a 100nm thick Si_3N_4 layer and it has to be removed before the PMD oxides are accessible from the wafer back-side. In addition, the isolation layer deposited inside the hole (see chapter 4.2.1) is a-Si_xN_y:H, which has to be removed subsequently only at the hole bottom. The etch chemistry used of DRIE has a low selectivity to SiN films. However, an anisotropic etching of the SiN film at the hole bottom is not a common process and was developed the first time in this work at the Fraunhofer ISIT. The experiments were performed at the Alcatel 601. Figure 4.9 (a) indicates that the deposited a-Si_xN_y:H was removed only at the hole bottom and (b) shows a close up of the hole bottom. Different materials are indicated. The process developed to etch c-Si also removed Si_3N_4 at hole depth of 300μm. The available analytics do not allow a clear visual proof. However, electrical measurements in chapter 4.2.2 showed an electrical contact between the the front-side pad and the TSV metallization.

Pin-hole free isolation layers are essential to avoid electrical cross talking or leakage currents. Figure 4.9 does not show any changes of the surface morphology after this etch process visually. However, pin-holes are often not visible by microscopic investigations. Chemical perforation helps to indicate structural defects inside films deposited. Etchants like KOH show a high selectivity between silicon nitrides and c-Si. Thus, silicon nitride films immersed in KOH at 80°C were slowly etched, whereas c-Si was etched much faster. Pin-holes allowed KOH to penetrate through the silicon nitride and the c-Si was etched relatively fast. Figure 4.10 shows an a-Si_xN_y:H film deposited in 300μm deep cavities after a ten minute KOH immersion. Figure 4.10(a) shows a a:Si_xN_y:H with pin-holes and (b) shows a pin-hole free film. A etch time of 3min and 30sec shows a complete a-Si_xN_y:H etching at the hole bottom on the entire wafer.

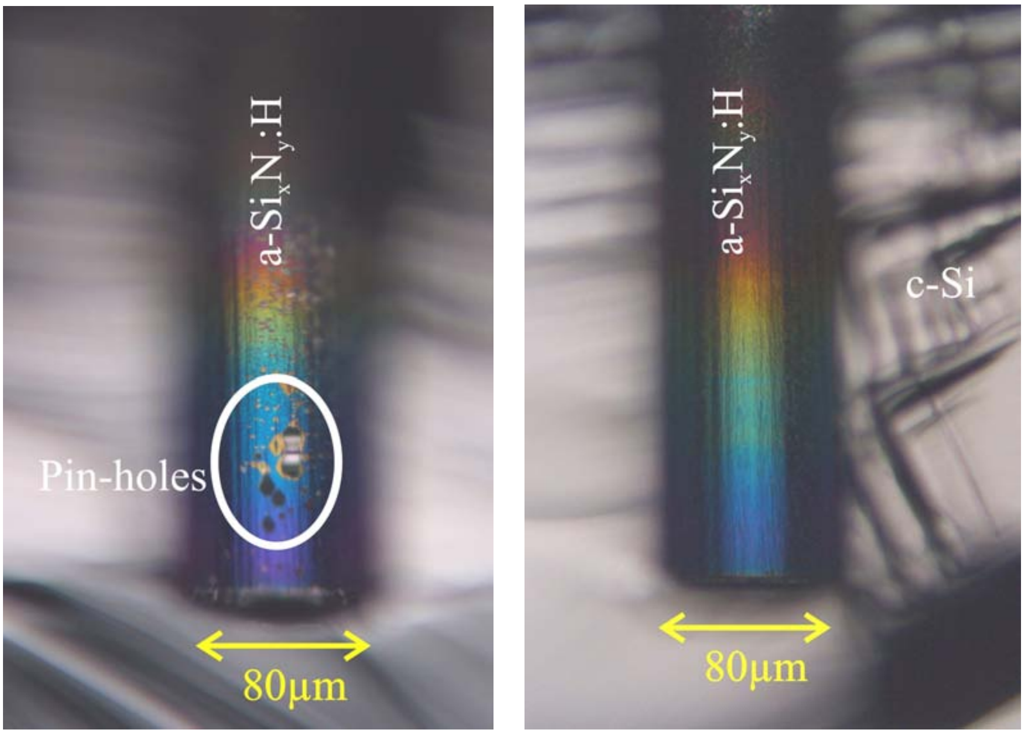


(a)



(b)

Figure 4.9: TSV holes after a-SiN:H deposition and spacer etch process. (a) Overview of a TSV hole formed. (b) TSV Hole bottom.



(a) (b)

Figure 4.10: TSV holes after a-SiN:H deposition and ten minute KOH immersion. (a) Non optimized spacer etch process. Pin-Holes are visible after KOH perforation (b) Optimized spacer etch process. No pin-holes are visible.

4.1.2 Silicon-dioxide

The PMD is mainly based on silicon dioxides as shown in chapter 3.6. Anisotropic etch processes are preferred to remove the PMD underneath the 1^{st} level metallization. Isolation layers deposited show a better reliability if no under-cut is formed during the PMD etching. Physical etch processes for silicon dioxides are available and often used in semiconductor device fabrications. Fraunhofer ISIT has different etching machines available, but their configuration does not allow an anisotropic silicon dioxide etching inside the given hole specifications anisotropically. The following experiments show etch technologies which allow a removal of the PMD.

Gas phase etching

Method

Holmes et al reported in 1966 a HF/H_2 vapor etching technology, also called gas phase etching (GPE), to etch silicon dioxides with high selectivities to c-Si, silicon nitrides or metals [54]. This process has been extensively utilized since that time and replaces wet etching processes often in modern MEMS fabrications. For instance, MEMS yields increase by vapor etching of sacrificial oxides compared to wet etch processes. This etching process defines freestanding MEMS structure elements, which are mechanically sensitive regarding cleaning processes needed after wet etching. Front-side pad structures are similar to thin membranes after PMD removal and are also mechanically fragile. GPE is therefore assumed as a more sensitive TSV process step compared to physical etch processes. However, GPE was not reported in the literature previously to etch the PMD from the wafer back-side through a $>300\mu$m deep hole. The etch model is given as follows [55].
It has been recognized that etching in a gas-phase regime takes place via a slow gas-solid reaction that is catalyzed by adsorbed moisture on the oxide surface. GPE uses H_2O(g) as etch inhibitor (catalyst) and HF(g) as etchant. Both gases adsorb physically on exposed surface

$$H_2O(g) \rightleftharpoons H_2O(ads) \tag{4.4}$$

$$HF(g) \rightleftharpoons HF(ads) \tag{4.5}$$

The adsorbed etchants react with each other to the point that HF_2^- is the most significant species to etch silicon dioxides.

$$2HF(ads) + H_2O(ads) \rightarrow HF_2^-(ads) + H_3O^+(ads) \tag{4.6}$$

It is assumed that a substitution of O in the silicon dioxide by F of the HF_2^- takes place and SiF_4 is formed. The overall reaction of etching silicon oxides by HF/H_2O gas phase etching is given by:

$$SiO_2(s) + 2HF_2^-(ads) + H_3O^+(ads) \rightarrow SiF_4(ads) + 4H_20(ads) \tag{4.7}$$

Both reaction products allow a desorption from the exposed surfaces

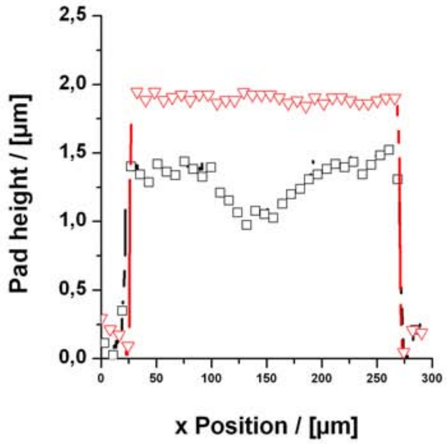
$$SiF_4(ads) \rightleftharpoons SiF_4(g) \tag{4.8}$$
$$H_2O(ads) \rightleftharpoons H_2O(g). \tag{4.9}$$

Several MEMS have shown sticking between functional elements after sacrificial oxide etching by using H_2O based GPE systems. Water free etch inhibitors were introduced to solve this problem. Different alcohols are used in MEMS foundries.

Results and Discussion

This gas phase etching technique was investigated in this work.

Experiment PMD was etched in a HF/Ethanol gas phase etching system after the c-Si and the Si_3N_4 was removed by DRIE from the wafer back-side. Therefore, wafers were placed in a Teflon™ container where only the wafer back-side was exposed to the gas mixture. The gases and the process chamber were heated to 33°C, which showed etch rates of 45nm/min for thermal silicon dioxides. However, various oxides show different etch rates. Sacrificial layers like phosphorus-doped silicon glasses (PSG) etch 19 times faster compared to a thermal oxide [54]. These etch behaviors resulted in a high vertical under-cut. A even higher under-cut was observed if PSG is deposited on top of a silicon nitride layer formed by LP-CVD. It can be assumed that a local stress between these two layers enhances the vertical PSG etch rate. An under-cut over a 100μm distance was observed at standard working conditions. A temperature increase during gas phase etching reduced the under-cut. However, this under-cut destabilizes pad-cells during further processing. Figure 4.11 shows a high pad buckling of different pad sizes. A thicker front-side passivation layer (500nm SiO_x) showed a stable pad-cell after GPE. This layer stack in combination with a pad-cell size of 200μm has not shown any film buckling.



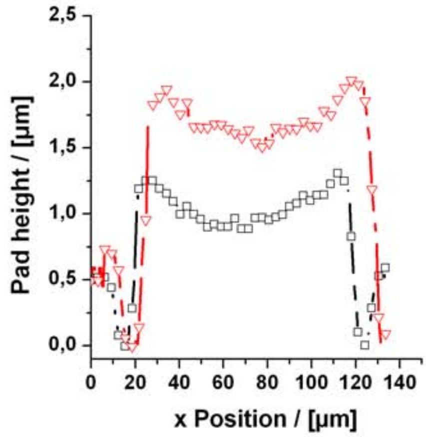


Figure 4.11: Pad buckling of a 200μm (left graph) and 100μm (right graph) wide pad. The red curves (∇) are with a SiO film on top of the pad structure.

Buffered oxide etching

Method

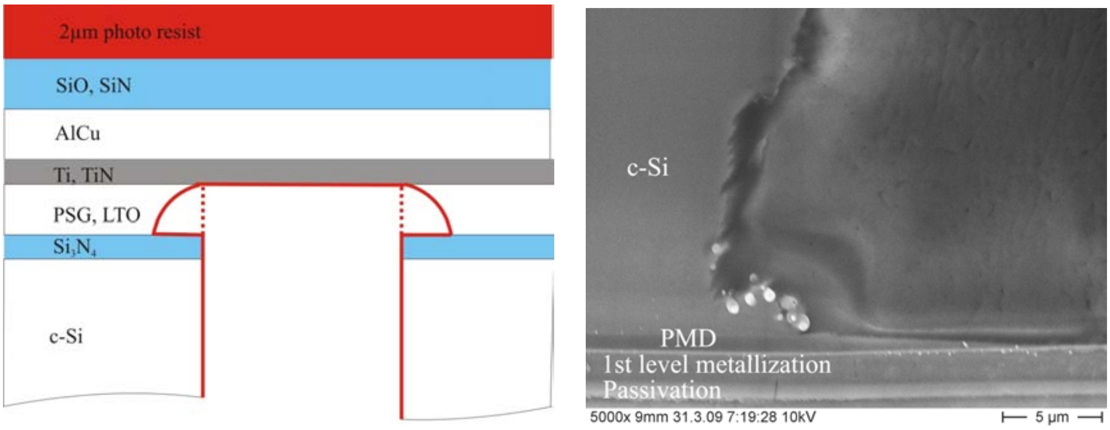
The method of etching silicon dioxides by liquid HF echants was already described in chapter 4.1.

Results and Discussion

This isotropic etch process was tested to remove the PMD underneath the 1^{st} level metallization of the front-side pad-cell

Experiment BOE (9:1) was used in this experiment. A etch rate of 63μm/min was measured for thermal silicon dioxides on a planar substrate. This etch process is a standard etch process at the Fraunhofer ISIT, but it was never used before to remove material in a >300mum deep cavity. An etch time of 15min was estimated in order to remove the 950nm thick PMD. The PMD was only 50% etched under these conditions. It can be assumed that the diffusion dynamics inside the TSV hole interferes with the reaction's mechanisms. A time of 30min. showed a complete removal of the PMD. The etch profile has not shown any under-cut even though BOE etching is an isotropic etch process. It is out of scope of this thesis to evaluate the etch mechanism of the PMD at the given TSV geometries.
BOE etching takes place in a basin. Thus, both wafer sides are immersed to the etchant at the same time. The last film deposited on the wafer front-side is a silicon oxide film as

indicated in figure 4.1 and is etched as well as the PMD by BOE. A photoresist was then coated on top of the front-side to protect the silicon oxide film. A 2μm thick photoresist (HIPR) allows a wafer immersion over one hour in BOE without an etching of the front-side passivation layer.



(a) (b)

Figure 4.12: PMD etching by using BOE. (a) photoresist protects front-side pad structures during PMD etching by using BOE. (b) BOE removed the PMD without an under-cut.

4.2 Deposition techniques

Different technologies were developed through the last decades to deposit electric isolating, semi-conducting or conducting thin films. Chemical vapor and physical vapor deposition techniques are predominantly used in CMOS and MEMS fabrication lines in order to deposit these films. All deposition techniques are based on the same two steps:

1. Material transport from given material sources to substrates,
2. Material deposition on the substrate.

These process steps affect the quality of the deposited films at given process parameters. Quality is defined in terms of composition, contamination levels, defect densities and mechanical and electrical properties. For instance, deposition temperatures used significantly influence electrical properties of isolating materials. High temperatures allow a deposition of stoichiometric Si_3N_4 with a low contamination level which corresponds to good electrical properties in terms of dielectric strength.
Uniform film parameters are an important issue regarding system specifications. Films deposited on wafers in CMOS or MEMS fabrication lines show the same film quality across the wafer, from wafer to wafer and from run to run. Low device standard derivations for MEMS and CMOS devices result from this deposition quality.
A special challenge arises for TSV deposition processes. Given geometries are indicated by a highly non planar substrate. Film parameters inside the TSV geometry must show similar properties compared to films deposited on planar substrates. Chapter 3.5 already indicated that step coverages <1 appear inside the TSV holes. TSV holes with $>300\mu$m depth and 80μm in diameter are not comparable with common topographies known in CMOS or MEMS fabrication. Thus, the following sections identify suitable deposition techniques for electric isolating and conducting thin films for the given TSV geometry. Figure 4.13 shows schematically a deposited film with a initial film thickness of d_0, hole depth of L and a hole diameter of d_{out}. The deposition profile $d_{in}(x)$ depends on the process used. Basic aspects which influence $d_{in}(x)$ are discussed in the following.

The arrival angle distribution of the direct incoming flux just above the substrate is defined in terms of the normal component of the incoming flux relative to a unit area on the wafer. Literature shows that the normal component of the flux $F_{direct}(\Theta)$ is proportional to the cosine of the vertical angle and is expressed by [45]

$$F_{direct}(\theta) = F^0 \cdot cos^n\theta \tag{4.10}$$

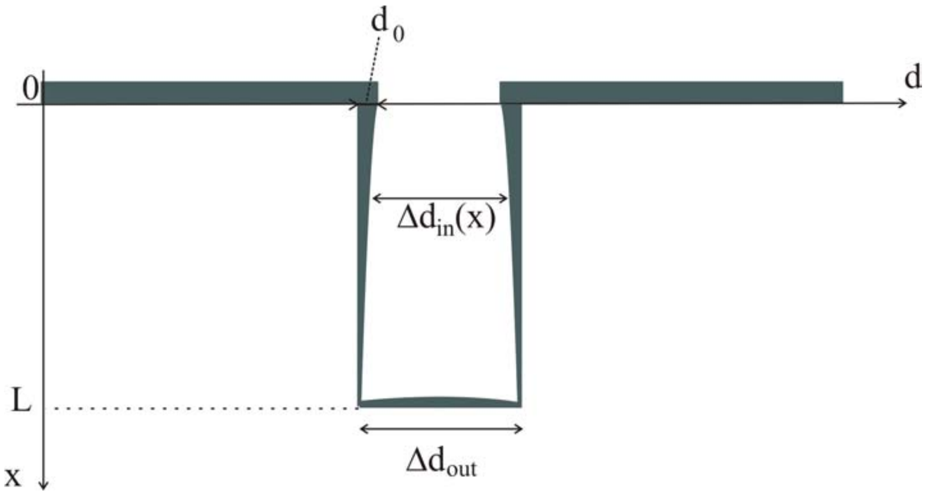


Figure 4.13: Geometry aspects of TSV deposition processes. L = TSV hole depth, d_{out} = TSV hole diameter, d_0 = film thickness at TSV hole entrance

where θ is the angle variation from the vertical direction and F^0 is the flux at $\theta = 0$. The factor n characterizes the isotropy of the incoming flux. Isotropic fluxes are obtained for n=1. Thus, particles arrive from all angles equally. High pressure deposition systems are an example for n values close to one, because more collisions of the particles in the gas phase and shorter mean free paths lead to an isotropic arrival distribution. In addition, large sources and small distances between sources and substrates also increase the isotropic behavior. Values of n<1 narrow the distribution angle and lead to a more anisotropic behavior of the incoming flux in respect to the vertical direction. Anisotropic distributions have longer mean free paths compared to isotropic distributions. Fewer particle collisions take place and particle transport inside deep holes or trenches is possible. Surface sides inside these geometries see fluxes arriving within a limited range due to geometrical considerations and shadowing [45] for collisionless systems (complete anisotropism) occur. This effect can lead to thicker films at hole orifices d_0 as indicated in figure 4.13.

Surface diffusion fluxes do not address atom diffusion during surface reaction processes, but concerns long range diffusion in order to reduce surface energies. This occurs by minimizing the curvature of surface features. A thermal treatment during or after deposition allows atoms to smooth surfaces. Mullins indicated that beside surface diffusion three other mechanisms reduce the total surface energy [56][57]:

- Surface diffusion: atoms diffuse along the surface to region of lower chemical potentials

- Volume diffusion: atoms diffuse through the volume of the material deposited
- Evaporation/condensation: atoms evaporate predominantly at surface with high energies and condense at low energy surfaces
- Viscous flow: Flow of atoms or molecules similar to motion in liquids

Thus, it can be assumed that a heat treatment during or after deposition improves the step coverage inside holes or trenches especially at temperatures close to the material melting point.

The emission flux takes into account that not all species of the incoming flux sticks immediately on surface sites where they arrived. The sticking coefficient S_C describes this process and is defined by the ratio of the flux which reacts and stays on surface sites F_{react} to the flux of the incoming deposition species $F_{incomming}$

$$S_C = \frac{F_{react}}{F_{incoming}} \tag{4.11}$$

S_C depends on the deposition system used, substrates used and on the material to be deposited itself.

The sputtered flux describes the removal of already deposited material by the incoming flux. This process arises predominantly when accelerated ions hit the surface. Ions with energies of several hundred eV are common for PVD processes like sputtering. A homogeneous film thickness contribution over the entire wafer is obtained by using this sputtering effect.

Materials deposited inside holes or trenches tend to form film gradients like shown in figure 4.13. The incoming high energy flux erodes more material at the hole orifice (x=0) compared to deeper hole position (x>0). A better step coverage of the deposited material is obtained by using this sputter effect.

4.2.1 Isolation-layer

Conventional technologies

Electric isolating materials are commonly deposited by chemical vapor deposition (CVD) processes [58]. The basic steps of film deposition, which are shown in the beginning of this chapter, characterize also CVD processes. Thus, some CVD reaction mechanisms are limited in terms of material transport to wafers [45]. Film thickness gradients are observed on wafers if the chamber configuration is not adapted to each deposition process. Only some wafers can be placed inside one chamber during film deposition. The introduction of reaction limited processes allowed a film deposition on several wafer at the same time, even if the wafers are placed vertical to the gas stream. The reaction velocity is the lower of these technologies compared to the transport limited processes. This results in a gas excess everywhere in the deposition chamber. High quality isolating films are deposited with these techniques. For instance, low pressure CVD (LP-CVD) is nowadays the common technique used to deposit PMD (silicon oxides and nitrides). In addition, isolating films deposited by LP-CVD show good step coverages even at high aspect ratios. This results from sticking coefficients in the range of 0.01 and an isotropic arrival distribution. However, LP-CVD uses commonly temperatures above 400°C and is therefore not post-CMOS compatible as required in this work.
Silicon dioxide deposition by using organic precursor instead of gases like N_2O and SiH_4 have been developed in the last decade. These techniques allow nowadays post-CMOS compatible silicon dioxide deposition with good step coverages in high aspect ratio geometries. An example of silicon dioxide deposition by using the organic precursor *Tetraethylorthosilicate* (TEOS) $C_8H_{20}O_4Si$ is shown in chapter 4.2.2. However, this technology is not considered as TSV isolation material due to the fact that silicon nitride was specified in the beginning of this work. The following two techniques allow a deposition of silicon nitride film under post-CMOS conditions.

Hot-wire chemical vapor deposition

Method

Wiesemann showed in 1979 an a-Si:H deposition by thermal decomposition of silane at 1600°C on tungsten or carbon foils [59]. This was one of the first investigation on the so called hot-wire chemical vapor deposition (HW-CVD). The groups of Matsumura [60], Gallagher [61] and Schropp [62] developed different processes for silicon-based films afterwards. All processes based on this technique use a thermal decomposition of silicon-containing

gases at a catalytic hot surface. This technique is also denoted as catalytic-CVD.
Hot surfaces, normally W or Ta wires, are placed in silicon-containing gas streams and the gases are decomposed and radicals are formed. The decomposition is a two step process [63]. For instance, silane and ammonium, which collide with the catalytic filament, react with the filament and silicides (W_xSi_y or Ta_xSi_y, etc.) are formed. The highly reactive hydrogen atoms subsequently evaporate from the filaments. Silicon can evaporate from the filaments if the filament temperature is high enough (>1600°C). Lower temperatures make the filament material brittle and wire breakage is often observed. The silane dissociation process at the hot filament is based on a hydrogen abstraction mechanism via [64]

$$SiH_4 \rightarrow SiH_3 + H \rightarrow SiH_2 + 2H \rightarrow SiH + 3H \rightarrow Si + 4H \tag{4.12}$$

Ammonium is not completely decomposed by the filament. Thus, NH_2 radicals and NH_3 molecules are both present in the gas phase. The created radicals react further in the gas phase, where growth precursors are formed. For instance, silicon nitride films are commonly deposited by a gas mixture of NH_3 and SiH_4. Si radicals, formed by SiH_4 decomposition, react predominantly with unreacted SiH_4 to SiH_3 radicals [65]. A formation of aminosilane is not observed [66]. Thus, the a-Si_xN_y:H formation must take place at the substrate surface like in PE-CVD processes.
Low temperature deposition of silicon-based films is possible by HW-CVD in spite of the high filament temperatures. Head radiation is inverse proportional to the fourth power of the temperature. a-Si_xN_y:H deposition processes were reported were substrate temperature around 250°C were obtained [67]. This low substrate temperature allows the deposition of silicon-based films on temperature sensitive substrates. In addition, the catalytic reaction on the heated filament does not form ions like in PE-CVD system. Thus, the deposition process is much gentler to the substrate.
In this thesis, amorphous SiN-films with incorporated hydrogen impurities (a-Si_xN_y:H) were deposited in a laboratory HW-CVD chamber in which 19 tungsten filaments were mounted parallel underneath the substrates. During deposition, the filaments were resistively heated. The substrate temperature was not controlled during deposition and a slight temperature change was observed due to radiative heating by the filaments. Deposition of SiN-layers was obtained from different NH_3-SiH_4 gas mixtures. Process pressures between 1-10 Pa and starting substrate temperatures below 200°C were used to form the SiN-films on top of the wafer.

Results and discussion

The presented HW-CVD technique is evaluated at the Fraunhofer Institute for Surface Engineering and Thin Films in order to realize the isolation film in the given TSV geometry. Two different experiments were performed:

Experiment A a-Si_xN_y:H deposition on different rough surfaces in order to evaluate material parameters on surface irregularities formed by DRIE.

Experiment B a-Si_xN_y:H deposition inside blind holes in order to evaluate the possibility to use HW-CVD in TSV applications.

The results were presented at the MRS Fall Meeting 2007 [68].

Experiment A The measurement of the dielectric strength of isolators with significant surface roughness in a TSV was difficult to perform. Therefore planar Metal-Insulator-Semiconductor (MIS) structures were used to measure the dielectric strength of the films. To investigate the effect of high surface roughness, the SiN-films were deposited on the non-polished side (side A) of a highly n-doped Si-wafer and compared to films deposited on the polished wafer side (side B). Both wafer types were coated with SiN using the same deposition cycle. Each deposition was repeated a second time. The wafers were cleaned in a standard RCA process before 1 μm thick Al electrodes were sputtered and structured over the SiN-films. For electrical breakdown measurements a voltage ramp of 0.1 V sec^-1 was applied with a limiting current of 3 mA. 90 different pad positions were measured on each wafer.
The electrical measurements were performed on different substrate conditions and various thicknesses and for two subsequent wafer lots (Batch 1 and 2). Table 4.1 summarizes the measured absolute breakdown voltages. The calculated dielectric strengths are significantly lower compared to reported ones [46]. They reveal values of about 3 MV/cm, nearly independently of the thickness of the layer and the underlying substrate. Also a large scatter around this value is observed. SiN layers deposited in LP- or PE-CVD processes show values in the range of 10 to 12 MV/cm. The deposition environment used and the substrate surface condition before the SiN deposition are viewed as the major cause for the lower values. The deposition equipment was not operating in a clean room and a surface cleaning either by oxygen plasmas or by wet cleaning directly before deposition was not performed. KOH pinhole-etching tests on the planar surface showed more pin-holes in the films used than in tested PE-CVD films, which indicates a particle contamination on the surface. This explains also the high standard deviation of the measured values, because

the early breakthrough events due to the pin-holes are still in this statistic. The medium and high breakdown events are assumed to be caused by pinhole like distortions in the bulk which form only breakdown channels after electrical stress. These macroscopic distortions are not observable in IR measurements which cover short and medium range order effects. Films inside the TSV showed a higher etch resistivity against KOH in contrast to the planar investigations, which means that only particles on top of the wafer were present, thus the real breakdown voltage can be higher.

Wafer side	**SiN thickness [nm]**	**Breakdown voltage [V]** Batch 1	**Breakdown voltage [V]** Batch 2
Side A	10	not measurable	not measurable
	50	13.8 ± 0.6	15.1 ± 0.4
	100	27.4 ± 12.1	27.4± 1.21
Side B	10	2.8 ± 1.0	2.9 ± 1.2
	50	14.5 ± 4.28	16.3 ± 0.4
	100	32.6 ± 1.13	28.1 ± 1.4

Table 4.1: Measured breakdown voltages vs. SiN film thickness and surface roughness obtained by MIS-structure measurements (Side A: non polished wafer side; Side B: polished wafer side: Replicate runs were performed: Batch 1 and Batch 2)

For the evaluation of the compositional properties of the HW-CVD film a comparison of films formed in different deposition processes was useful. The left graph of Figure 4.14 shows IR spectra of silicon nitride processed in LP-, PE- and HW-CVD. The LP-CVD film is taken as a reference system, since high stoichiometry and minor amount of impurities are well classified [69]. All films displayed a distinct main absorption band at about 830-840 cm^{-1}. The slight variation in position was interpreted as not significant enough to indicate morphological changes. The half width of the principal band appears essentially to be the same for all the films. That means the respective networks display very similar variations in the tetrahedral (N-Si-N) and dihedral (Si-N-Si) angles. A slight shoulder appears on the low frequency (1175cm^{-1}) side of this peak and is attributed to an N-H bending vibration. The oscillator strength (IR activity) of the 1175cm^{-1} mode is reported to be high, which can explain its appearance in all of the films. The distortion at about 1107 cm^{-1} was caused by an interstitial oxygen absorption mode. However, the appearance of this oxygen band was subjected to the calculation of the difference spectra that display different amounts of oxygen in the substrates and shall not be discussed here. However, there appear to be striking deviations in the amount and bonding structure of hydrogen in the different films. Besides the shoulder at 1175 cm^{-1} (N-H) some distinct hydrogen related absorption bands can be observed at 2300 cm^{-1} (Si-Hn stretching) and 3400 cm^{-1} (Si-NHn stretching). The oscillator strength of these modes is reported to have medium strength [70]. The appearance of the N-H stretching mode at 3400 cm^{-1} is correlated to the N-H absorption mode at 1175 cm^{-1}. Then also the Si-Si breathing mode at 460 cm^{-1} is more pronounced as shown in the right picture of Figure 4.14. If the NH stretching mode is very weak, then the Si-H stretching mode at 2400 cm^{-1} increases in absorption in conjunction with a weakening of the Si-Si mode. For the PE-CVD film these N-H vibrations are more pronounced and an additional Si-H vibration at 2300 cm^{-1} appears clearly. This indicates a high hydrogen content (up to 24 at %) [71]. For the HW-CVD films the appearance of the N-H and Si-H vibrations depend on the deposition conditions, whether the SiH4/NH3 ration is large or small and from the rf-power. A large absorption area of N-H bonds at 3400cm^{-1} corresponds to a small absorption area of S-H bonds of 2300 cm^{-1} and vice versa. In addition, the appearance of this NH mode correlates with a more distinct appearance of a so called Si-Si breathing mode at about 460 cm^{-1}, compared to the above mentioned films. Conversely, if the Si-H mode appears, the Si- Si breathing mode and the N-H modes disappear, except a remaining partition at 1175 cm^{-1}. It is beyond the scope of this work to give a detailed explanation to different binding sites for hydrogen for the same deposition process performed, however, under different conditions. The high structural order of the HW-CVD films is in agreement with their index of refraction values. The measured values were between 1.986 and 2 which is comparable with a value of 1.992 of the deposited PE-CVD film. This value indicates a stoichometric Si3N4 film.

Experiment B Holes of 100 μm diameters were etched by deep reactive ion etching (DRIE) inside 6 inch Si-wafers in order to determine the capability of the HW-CVD method as a deposition technique for the required isolation layer in TSV. SiN-films were deposited on the wafer and thus inside the holes by the described deposition arrangement. Cross sections of the samples were prepared with a wafer-dicing saw, where circle segments were varied in order to reduce measurement errors during the following electron probe micro-analysis (EPMA) measurements. The EPMA technique allows the indirect calculation of the SiN-film thickness by comparison with a standard. Only the nitrogen signal was used to determine the SiN-film thickness, because it is not possible to discern whether the measured X-Ray Si-wavelength came from the SiN-film or from the Si-substrate. Figure 4.15 shows

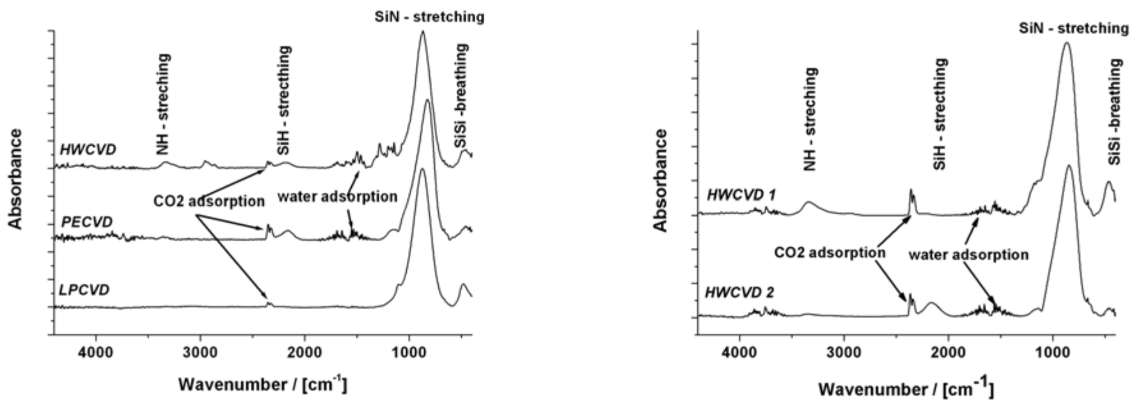


Figure 4.14: IR-Spectra of isolation layers deposited by HW-CVD, LP-CVD and PE-CVD. Left graph: IR-Spectra of SiN films deposited by LP-, PE- and a HW-CVD. Right graph: IR-Spectra of SiN films deposited by HWCVD under different deposition conditions. (HWCVD 1: q(NH3)= 15 sccm; q(SiH4)= 200 sccm; HWCVD 2: q(NH3)= 30 sccm;q(SiH4)= 1300 sccm)

the thickness of the material deposited versus the hole depth. It can be assumed that these measured values are lower than the real values, because the film thickness estimation was based on the theoretical film density of 3.4 g cm^{-2} and a stoichiometric Si_3N_4-film. The expected lower film density of the deposited films will increase proportionally the real film thickness, because the measured signal is proportional to the product of the film density and the film thickness at a constant stoichiometry. Figure 4.15 displays also a PE-CVD profile obtained.
Equation (3.9) shows the solution of the isolation capacitance if an exponential decay profile like (3.8) is assumed. Figure 4.15 shows the best fit through the obtained film thickness gradients by HW-CVD deposition. The deposition parameters are summarized in table 4.1. Equation (3.8) changes to

$$r(x) = 510nm \cdot e^{-x/125\mu\mathrm{m}} \tag{4.13}$$

by insertion of the fitted parameter values. The capacitance of the isolation material deposited is given by equation (3.9) and shows a capacitance value of 6.85pF for the given deposition profile. This results in a relative capacitance of 22.9fF/μm. This value is 2.6 larger compared to the theoretical value (8.7fF/μm) at ideal ring symmetry as shown in chapter 3.5.1.

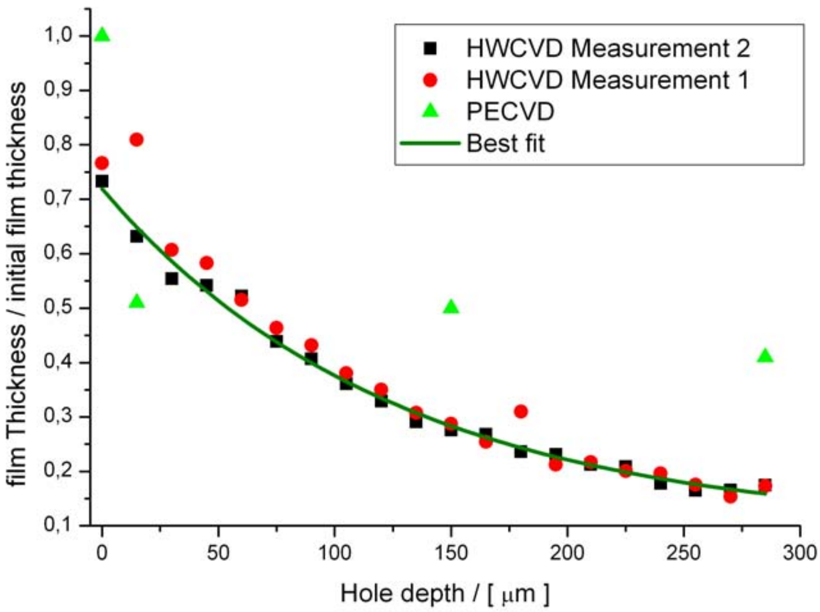


Figure 4.15: SiN-film thickness in respect to the initial film thickness on the planar subsrtrate deposited by HW-CVD and PE-CVD as a function of the hole depth. The best fit through the HW-CVD profiles is indicated. The initial film thickness was 710nm.

Plasma enhanced chemical vapor deposition

Method

Plasma-enhanced chemical vapor deposition (PE-CVD) is a widely used method to deposit silicon-based thin films. Gases are dissociated in a rf-plasma, typically at a frequency of 13.56MHz and radicals, electrons and ions are formed. The plasma supplies additional energy and reduces the temperature needed for this dissociation reaction. Common PE-CVD systems work with temperatures between 300°C and 400°C and allow an post-CMOS processing. For instance, silane and ammonium are decomposed into Si_xH_y, NH_x and H radicals at temperatures of 350°C in the case of silicon nitride deposition by using PE-CVD. Further gas phase reactions between species formed and other radicals, ions or gas molecules are possible. However, film growth is driven by diffused radicals to the wafer surface. Reaction mechanisms are difficult to predict due to non-equilibrium reactions in the plasma. Non-stoichiometric films are usually formed by PE-CVD processes. In addition, H incorporation in silicon nitride films is possible. Silicon nitride films formed by PE-CVD processes are often indicated with a-Si_xN_y:H.
Step coverage is a critical issue for using PE-CVD systems in TSV applications. The relatively low temperature used does not show a significant material diffusion compared to silicon nitride films obtained by LP-CVD systems at 800°C to 900°C. In addition, the sticking coefficient is also higher in PE-CVD systems compared to LP-CVD. However, films with sufficient step coverages are obtained by PE-CVD systems. This phenomena is explained by the accelerated ions which hit the surface and sputter away already deposited films. This effect improves as mentioned before the step coverage.

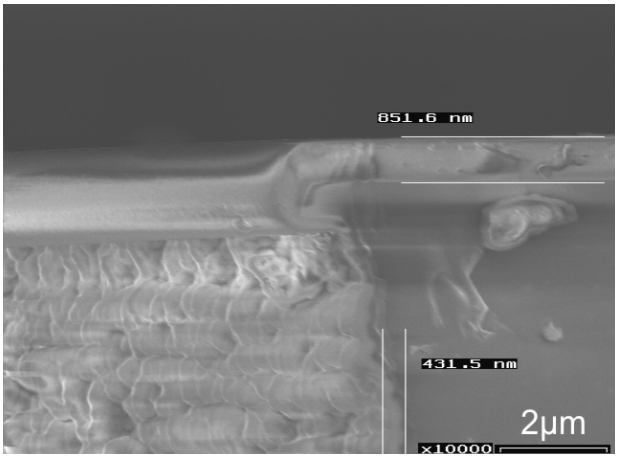
Results and discussion

A standard a-Si_xN_y:H deposition process (Delta Trikon 2001, 350°C, 1.1mbar) was evaluated in order to realize the isolation material in the given TSV geometry. Silane and amonium were used as source gases. The following experiments were performed:

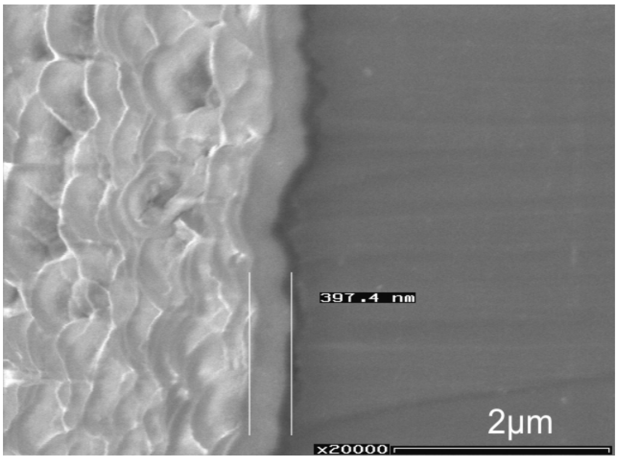
Experiment A a-Si_xN_y:H deposition inside blind holes in order to evaluate the possibility to use PE-CVD in TSV applications.

Experiment B a-Si_xN_y:H deposition on blanket substrates in order to evaluate material parameter.

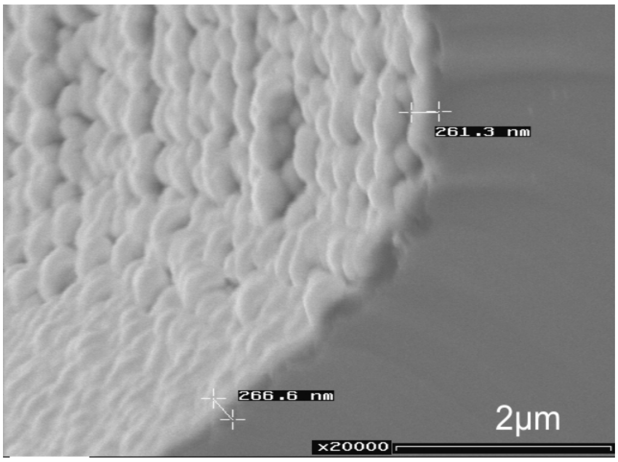
Experiment A The same geometries (100μm diameter and 300μm deep) were used in this investigation as in the HW-CVD experiments. Wafer were cleaned with a standard RCA procedure directly before a-Si_xN_y:H deposition was performed in order to obtain suitable film adhesion between the a-Si_xN_y:H and c-Si substrate. Figure 4.16 shows an example of a a-Si_xN_y:H film deposited inside TSV holes. In this case, an initial film thickness of 850nm was deposited. The film thickness on the sidewalls is already at the hole entrance only 50% of the initial film thickness. However, the film thickness remains constant up to a hole depth of approximately 100μm. The thickness decreases afterwards. Thus, it is assumed that the a-Si_xN_y:H deposition mechanism inside the TSV hole is reaction and diffusion limited. First, reaction limited deposition dominates from the TSV hole entrance down to approximatly 100μm TSV hole depth. Diffusion limited deposition dominates afterwards. Thus, a modeling of isolation film thickness profiles deposited by PE-CVD inside the given TSV geometry is hard to achieve. A calculation as shown before for the a-Si_xN_y:H deposited by HW-CVD will not be given here. In addition, a process parameter variation has not shown a significant change of the profile. Therefore, a well characterized a-Si_xN_y:H deposition process at Fraunhofer ISiT is used for the following investigations.



(a) hole entrance



(b) hole center



(c) hole bottom

Figure 4.16: a-Si_xN_y:H films in 300μm deep blind holes (100μm in diameter). Different hole positions are indicated. The film thicknesses obtained are: (a) entrance: 430μm, (b) center: 400μm, (c) bottom: 260μm, initial film thickness: 850μm.

Experiment B Different parameters like the index of refraction, the dielectric strength or the structural composition were determined for the deposition process developed in experiment A of this chapter. Most parameters were already compared to results obtained by using HW-CVD in the previous section. However, table 4.2 summarizes basic parameters of the a-Si_xN_y:H deposited.

Paramter	**[Unit]**	**Value**
dielectric strength	MV/cm	>10
hydrogen content	at%	>20
index of refraction	1	1.992
pin-hole density	%	no pin-holes observed after KOH treatment for 1h
IR spectrum		see figure 4.14

Table 4.2: Material parameters of a-Si_xN_y:H.

4.2.2 Metalization-layer

Conventional Technologies

Metallic films can be realized by physical vapor deposition (PVD), which implies sputtering and evaporation processes, and chemical vapor deposition (CVD). PVD works well for depositing films on planar substrates. A conformal deposition on rough surface or even a good step coverage inside the given TSV geometry are crucial issues for PVD technologies. The mean free path λ of these deposition techniques is too high in order to have enough particle interactions inside the geometry. In addition sticking coefficients of PVD systems are close to one. Thus, it can be assumed that standard PVD systems will not show a sufficient step coverage for the TSV metallization. The figures 4.17 (a) and (b) indicate that a metal film can be deposited down to TSV depth of 150μm by using a standard magnetron sputtering technique.
Evaporation systems normally rotate the wafers around the evaporation flux in order to achieve homogeneous film parameters on the entire wafer. A metal deposition by evaporation inside a 3D structure like TSV results in a columnar film growth. The TSV hole formation is often performed by a deep reactive ion etching (DRIE) process, see chapter 4.1, which produces a periodic surface pattern like is shown in figure 4.17 (c). Material will nucleate mainly on top of the hills of this periodic pattern due to the given geometry. The particles of the incoming flux nucleate at the hill and prevent further nucleation events on the valley surface, because the growing film shadows the valley. Typical deposition processes uses low temperatures which avoids surface diffusion. Therefore, columns are growing on top of the hills. The column orientation is given by the TSV profile and the angle of the incoming evaporation flux and can be described by the tangent rule [72]

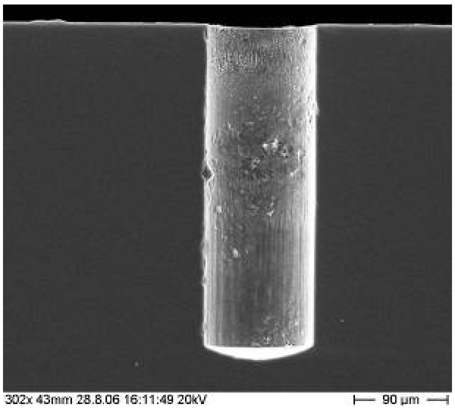
$$\tan(\alpha) = 2 \cdot \tan(\beta) \tag{4.14}$$

where α and β are the angle of the incoming evaporation flux and the angle of the growing film in respect to the surface normal, respectively. Figure 4.17 (d) shows an evaporated Ti film (adhesion promoter) inside a DRIE etched structure. Two different techniques were investigated in this work to deposit the metallization-layer.

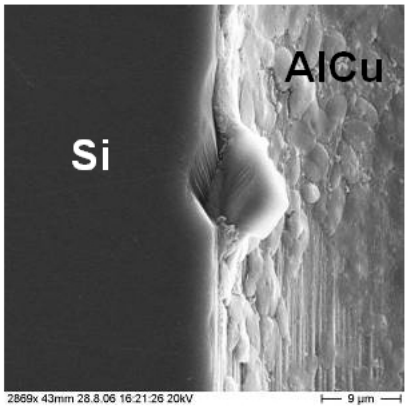
Gas flow sputtering (GFS)

Method

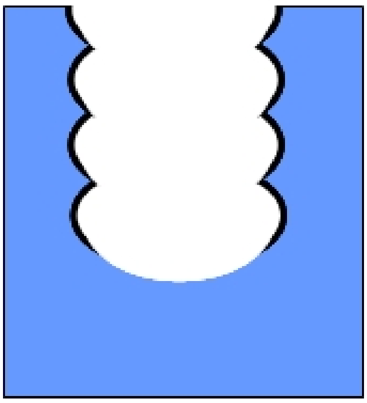
The GFS- technique is a special PVD technique, based on a hollow cathode glow discharge [73] and a gas flow driven material transport. In contrast to magnetron sputtering, the



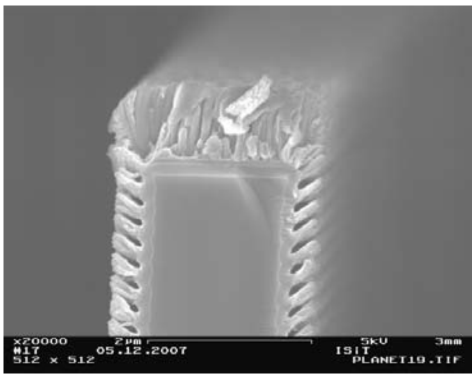
(a)



(b)



(c)



(d)

Figure 4.17: Metal deposited inside 300μm deep TSV holes. (a) Overview of a blind hole with deposited AlCu inside the hole by using magnetron sputtering. (b) Close up of (a) at a depth of 150μm. (c) Typical DRIE etch profile. (d) Evaporated Ti film on an oxidized side wall formed by DRIE.

target is hollow and arranged perpendicular to the substrate. The shape of this sputter source is either in the form of a tube or of two rectangular parallel plates facing each other. The discharge current increases up to 3 orders of magnitude, mainly due to the charge carrier confinement and merging of the negative glow from opposite cathode areas in an appropriate pressure range. This is the so called hollow cathode effect. In the GFS sources, cathode width and operating pressure usually are some centimeters and 0.1 to 1.0 mbar, respectively. A high power density can be realized due to the hollow cathode effect and the comparatively high operating pressure. This results in a high plasma density and an intense sputter erosion of the target. High ion densities are also obtained on the wafer surface by using this arrangement. Figure 4.18 shows a typical GFS setup. A detailed description of the deposition chamber used is given by Jacobsen [74].

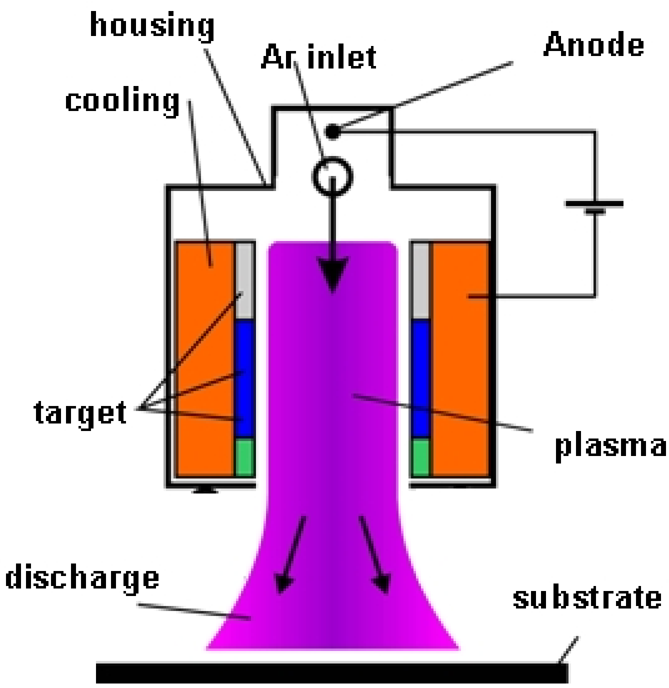


Figure 4.18: Gas Flow Sputtering arrangement.

Jung et al. investigated the GFS-technique for film deposition on three-dimensional structures [75]. They described that the film deposition is based on two different transport mechanisms. First, the intense gas flow indicates an anisotropic gas profile directly at the sputter source outlet. On the other hand, the gas flow is getting more and more isotropic on the way to the substrate surface due to the isotropic material out-diffusion from the gas flow. Thus, GFS is a combination of physical and chemical vapor deposition. In addition, high bias voltages and high temperatures can be applied to the wafer surface, which improves the step coverage. Thus, a partially isotropic emission flux, a high sputter flux and a possible large diffusion flux characterizes the GFS method and is therefore considered as a deposition technique to obtain the TSV metallization.

Results and discussion

Two different GFS-experiments were performed at the Fraunhofer Institute for Surface Engineering and Thin Films:

Experiment A Deposition of Ti, Cu inside given TSV geometries.

Experiment B Deposition of Al inside given TSV geometries.

Experiment A Plummer [45] shows that PVD techniques tend to form voids during filling of trenches due to the anisotropic emmision flux and sticking coefficients close to one. Applied bias voltages to substrates improve the deposition profile regarding a better step coverage. In addition, high pressures during deposition shorten the mean free path which is also preferable to obtain a constant film thickness inside the TSV geometries. Thus, the bias voltage and the operating pressure during Cu deposition were varied during the deposition of Cu inside TSV holes with diameters of 100μm and 300μm depth. Table 4.3 indicates the parameters used.

Process number	Pressure [mbar]	Bias voltage [V]	Initial film thickness [μm]
1	0.38	50	2.5
2	0.38	25	2.5
3	0.38	0	2.5
4	0.22	25	2.5
5	0.70	25	2.5
6	0.38	25	5.0
7	0.70	25	8.0
8	0.70	50	8.6
9	0.70	0	12.0
10	0.40	25	10.7

Table 4.3: GFS process parameter variation used during Cu deposition

All films obtained by processes 1 to 5 showed a non closed film at the lower part of the TSV hole. However, it was observed that more material is deposited for higher pressures used. In addition, all applied bias voltages do not show a significant difference in the film thickness profile.

An initial film thickness of 5μm, as deposited in process 6, showed a closed film even after an KOH etch test. KOH etches Si but does not attack Cu. Figure 4.20 (a) shows a cross section of the Cu film deposited by using process 6. The additional figures are close ups as indicated in (a).

However, the pressure was fixed to 0.7mbar and the bias voltage was varied during further experiments. The initial film thickness was increased to 10μm to 12μm. This thickness allowed a film thickness measurement with the available instruments. A maximum film thickness of 1.2μm at the hole bottom was obtained by using process 8 (50V, 0.7mbar) as expected from theoretical considerations discussed before. The film thicknesses at the hole bottom were only slightly thinner for the other process variations. The film thickness gradient of process 8 was parameterized by equation (3.8). The best fit results to

$$r(x) = 8.7\mu m \cdot e^{-x/64.6\mu m} \tag{4.15}$$

An electrical resistance of 320mΩ for the given TSV structure (100μm diameter, 300μm in depth) was obtained by placing (4.15) in (3.17). First electrical measurements indicated that the electrical resistance of one TSV is in the range of 100Ω. The morphology obtained explains this higher value compared to theoretical values. Figure 4.20 (c) shows a cauliflower film. Thus, a large Cu surface were formed and TSV geometry by using this technique. Ti was also deposited inside the TSV geometry for adhesion purposes. EDX measurements have not shown Ti on the sidewalls even at hole depth of 50μm. Thus, it can be concluded that the Ti film thickness gradient is large. A good adhesion of the deposited Cu inside the TSV structure can therefore not be guaranteed.

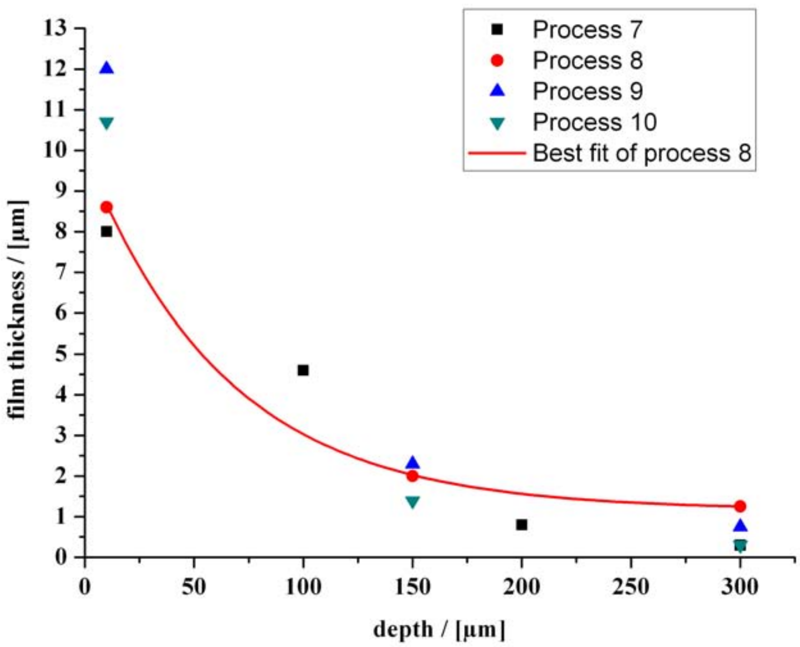
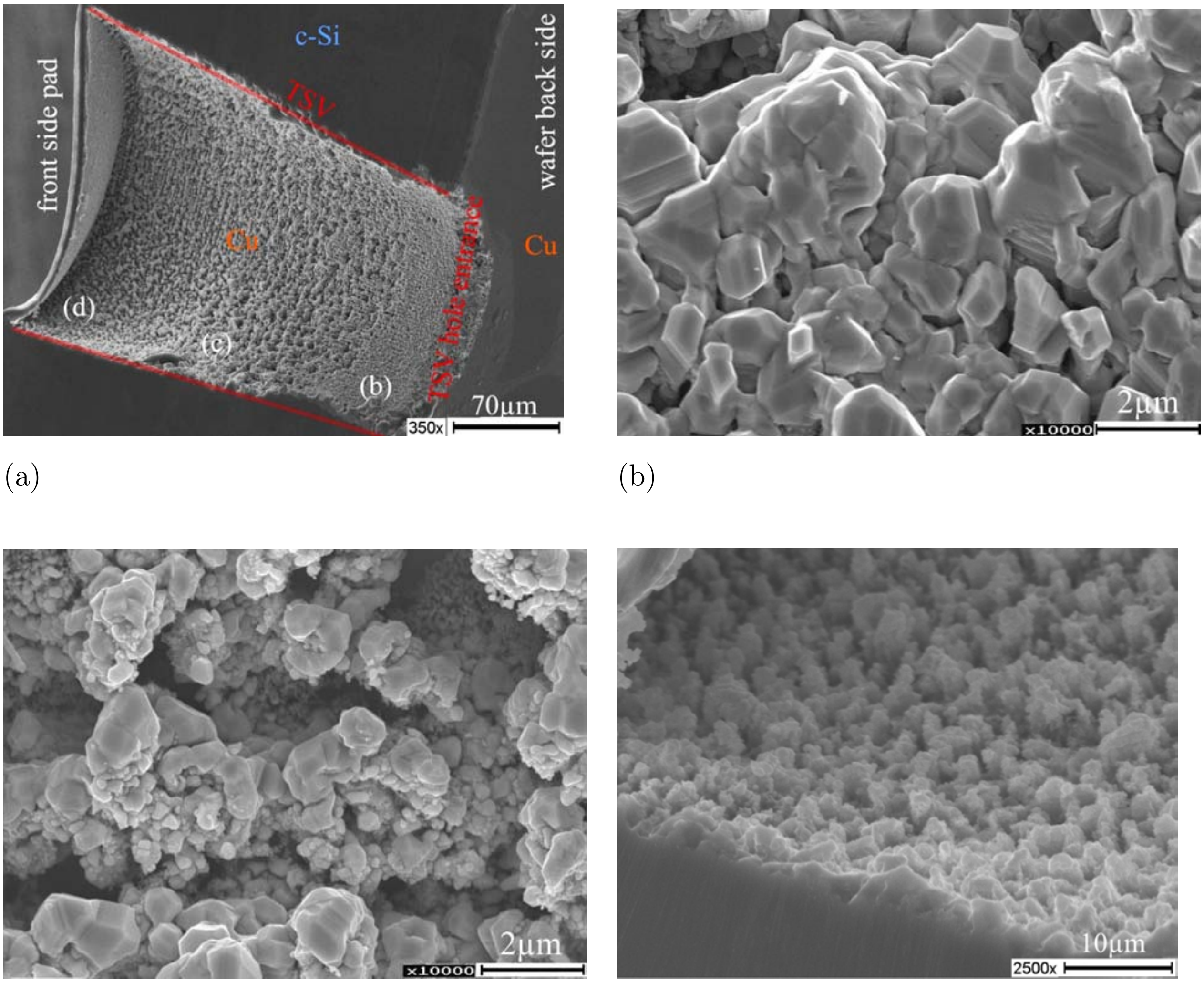


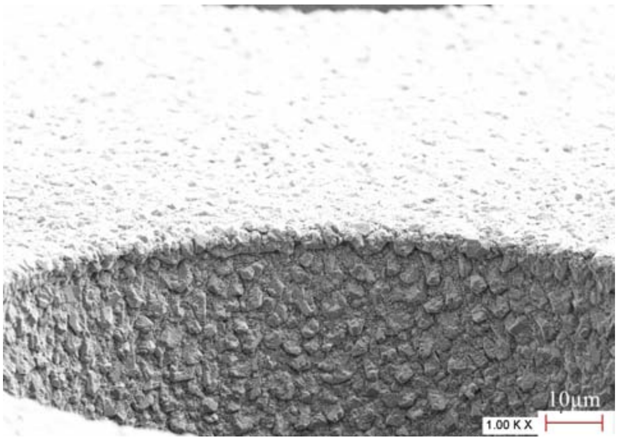
Figure 4.19: Film thickness gradient of Cu deposited inside 300μm deep TSV structures by gas flow sputtering. The different samples indicate deposition parameter variations (Process 7: 25V Bias Voltage; 0.7mbar pressure, Process 8: 50V Bias Voltage; 0.7mbar pressure, Process 9: 0V Bias Voltage; 0.7mbar pressure, Process 10: 0V Bias Voltage; 0.4mbar pressure)



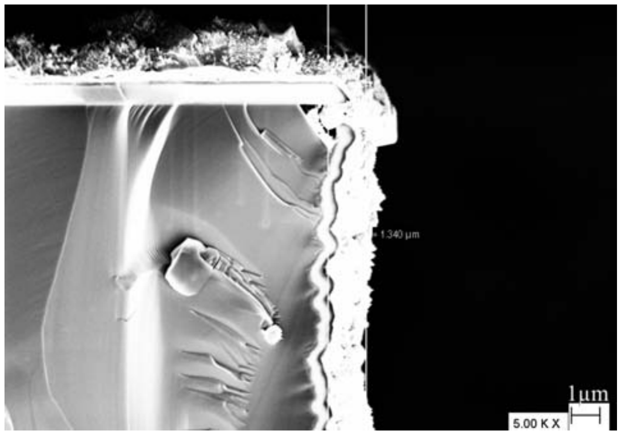
(a) (b) (c) (d)

Figure 4.20: Cross Section of a TSV after Cu deposition by using GFS (Process 8). Overview (a) and film morphologies at different hole positions are indicated ((b) hole entrance, (c) hole center, (d) hole bottom).

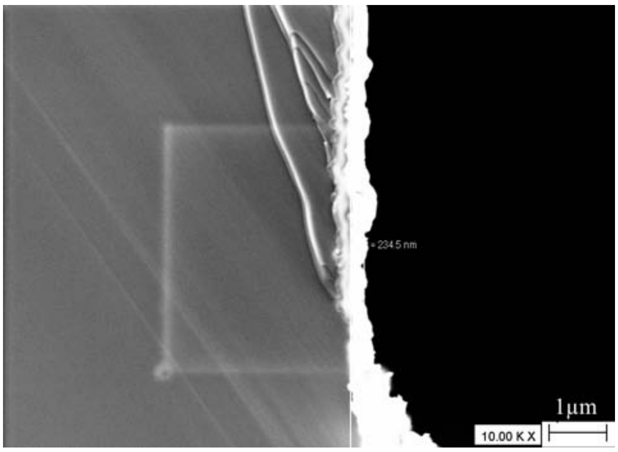
Experiment B The previous experiment has not considered diffusion fluxes for a better material sidewall coverage. Surface diffusion is a significant process during film formation for elevated deposition temperatures. Thornton defined qualitatively temperature regimes in which different film formation processes occur [76]. Four zones of growth were defined by the ratio of the substrate temperature T during deposition and the melting temperature T_M of the material deposited. Cu was deposited in experiment A under conditions which does not show surface diffusion $T/T_M < 0.3$ (Zone 1 and Zone T). Diffusion controlled growth processes can be observed for $T/T_M > 0.3$, whereas Zone 2 ($0.3 < T/T_M < 0.5$) and Zone 3 ($T/T_M > 0.3$) shows surface and bulk diffusion controlled growth, respectively. The melting temperature of Al ($T_M = 933$K) is lower compared to Cu ($T_M = 1357$K). Thus, Al was deposited in this experiment by GFS at a substrate temperature of 400°C - 450°C inside the given geometry in order to study the step coverage of the deposited Al if surface diffusion plays a significant rule during film growth. In addition, Al does not need an adhesion promoter on silicon nitrides.
Experiment A has shown that a pressure of 0.7mbar and a bias voltage of 50V are preferable for the deposition of the metallic layer inside the given TSV geometry. Thus, these parameters were used whereas the substrate temperatures were varied. Figure 4.21 shows an example of the optimized Al deposition process. The TSV hole entrance is indicated in figure 4.21 (a). A high surface roughness or even hillocks were observed, which was expected due to the Al stress relaxation during deposition. This relaxation occurs for $T/T_M > 0.4$ for soft metals like Al [77]. Figure 4.21 (b) and (c) show cross sections at the hole entrance and the hole bottom, respectively. Al film thicknesses of 52% at the hole entrance and 9.6%at the hole bottom compared to the initial film thickness of 2.5μm were measured. Figure 4.21 (d) shows also a porous film morphology. Electrical resistances of TSV formed were not measurable due to the porous film structure shown in figure 4.21 (d). Samples with thicker Al were broken during the following wafer processing.



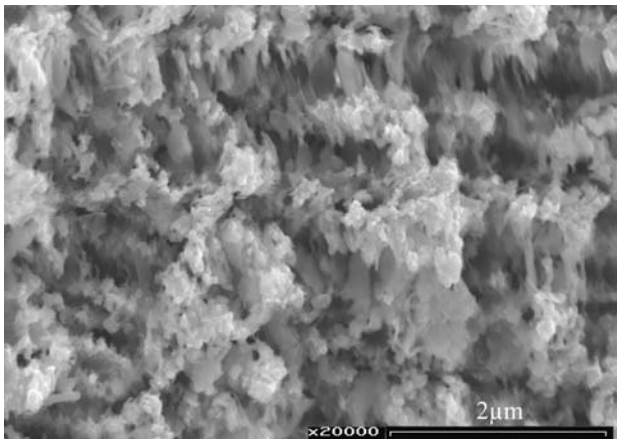
(a)



(b)



(c)



(d)

Figure 4.21: Al film deposition inside TSV geometry by gas flow sputtering.
Al film deposited inside TSV geometry by gas flow sputtering (Deposition temperature: 400°C - 450°C, Pressure: 0.7mbar, 50V). (a) Top view of TSV entrance (b) Cross section of a deposited Al film at the hole entrance; (c) Cross section of the deposited Al film at the hole bottom (d) Surface of the deposited Al inside the TSV geometry.

Metal organic chemical vapor deposition (MO-CVD)

Method

Chemical vapor deposition is well known for the deposition of dielectric layers in microelectronics. Tungsten and tungsten silicide CVD are so far the only metallic based systems which are commercially used. Tungsten is used in multi layer architectures to connect different metallic layers (tungsten plugs). Chapter 3.5 shows that copper based metallization systems are preferred in architectures with small feature sizes in order to reduce parasitic effects. Cu- and TiN-CVD are developed in the last decade and are commercially available now.
CVD processes require the material to be deposited in the gas phase. This so called precursor defines the film quality and the deposition parameters. Inorganic Cu halogenides can be reduced with hydrogen to Cu. A temperature of 1000°C is mandatory to achieve pure Cu films. This high temperature limits the process compatibility; post-CMOS processes are not possible. Cu precursors can also be established by organic Cu compounds. A thermal decomposition of bivalent Cu compounds require temperatures of 300°C to 400°C and the raw material is mostly available only as a solid material. The evaporation of the material from the solid phase to the gas phase and the gas transport to the reaction chamber is technically difficult to control. Such systems are not available on the market. Different variations of monovalent Cu precursors are developed, but *copper-hexafluoroacetylacetonate-thrimetylviniylsilane* ($C_{10}H_{13}CuF_6O_2Si$) is the most used precursor and is commercial available. The company Schumacher sells this precursor under the trade name CupraSelect. Figure 4.22 shows the chemical structure of CupraSelect.

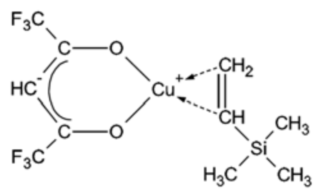


Figure 4.22: Chemical structure of CupraSelect ($C_{10}H_{13}CuF_6O_2Si$)

The literature shows also the name *(hfac)Cu(TMVS)* as a synonym of CupraSelect. This notation allows a better formulation of the disproportionation reaction, which is given by the simplified reactions:

$$2TMVS - Cu - hfac \rightarrow 2TMVS \uparrow +2Cu - hfac \tag{4.16}$$

$$2Cu - hfac \rightarrow Cu + hfac - Cu - hfac \uparrow \tag{4.17}$$

Equation (4.16) describes the splitting of the TMVS from the precursor. This reaction occurs at the surface or in the gas phase. Two of the resulting $Cu - hfac$ molecules undergo a disproportion reaction [72] as shown in equation (4.17). Two monovalent Cu atoms change their oxidation state and one bivalent and one neutral atom are formed by this reaction. The neutral Cu atom contributes to the film growth and the bivalent atom desorbs. Figure 4.23 shows the described mechanism.

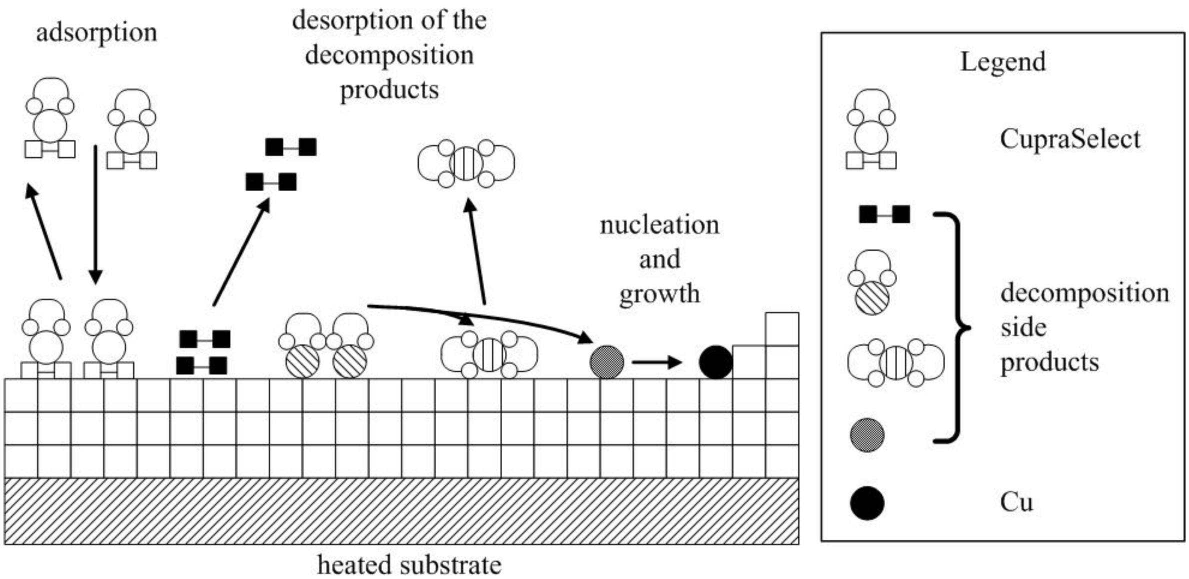


Figure 4.23: Reaction model of Cu MO-CVD on surface-sides (Redrawn from [78]).

Similar consideration must be taken into account for the TiN precursor selection. Liquid inorganic precursors like titanium chloride are available and often used in micro-electronics. Pure titanium or titanium nitride are obtained by this precursor. Temperatures above 600°C are necessary during the deposition in order to minimize the chlorine contamination inside the deposited films. Therefore, titanium chloride precursors are not practical for post-CMOS compatible TSV. Organic titanium nitride precursors are available which allow a deposition temperature below 400°C. *Tetrakisdimethylaminotitan* (TDMAT) is a commercially available precursor for the deposition of TiN. TDMAT undergoes a pyrolysis during the deposition process. The precursor is cracked and a film of Ti, N, C and a organic

rest is formed. The film properties are not sufficient for a diffusion barrier in microelectronics. Therefore, the TiN deposition is a time multiplexed process as shown in figure 4.24. First, a low quality TiN film of 5nm is deposited by the pyrolysis process. Hydrogen and nitrogen plasmas improve the film quality by removing almost all impurities. The film thickness after this treatment is roughly 2.5nm. These steps are repeated until the desired film thickness has been obtained. Some impurities still remain in the TiN film.
Chapter 3.2.1 shows that TiN is a diffusion barrier in Cu based metallization systems. An adhesion promoter is normally required, between Cu and TiN. Riedel has developed a treatment for the Cu, TiN stack, which shows good adhesion without an extra adhesion promoter [79]. The wafers were deposited with TiN and Cu without a break of the vacuum and afterwards directly tempered at 450°C in an argon atmosphere for several minutes. A new layer forms between the Cu and the TiN during this treatment. The impurities inside the TiN film are may be the reason for this film formation. An inter-diffusion between the Cu and the formed film is possible and a good adhesion is obtained. This film stack integrated in microelectronic systems is comparable with conventional sputtered Ti,TiN films.

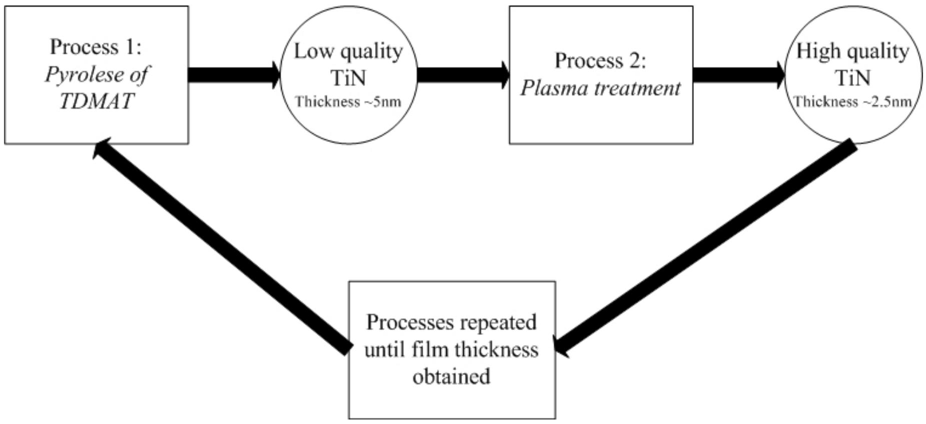


Figure 4.24: Process cycle of the TiN deposition by MO-CVD (Redrawn from [79]).

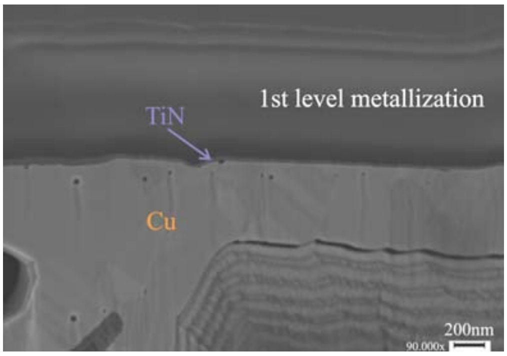
Results and discussion

The presented process flow is evaluated at the Fraunhofer Research Institution for Electronic Nano Systems in order to realize the metallization in the given TSV geometry. Two different experiments were performed:

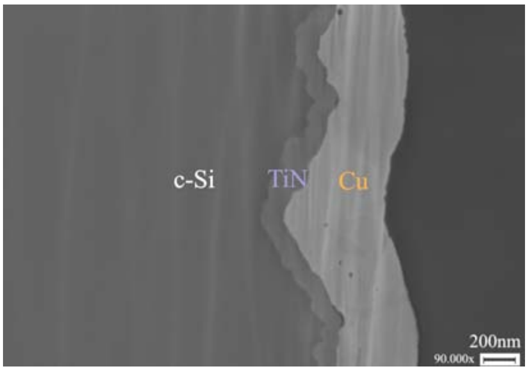
Experiment A Deposition into blind holes with different aspect ratios.

Experiment B Deposition on wafer with the test design and enhanced surface roughness.

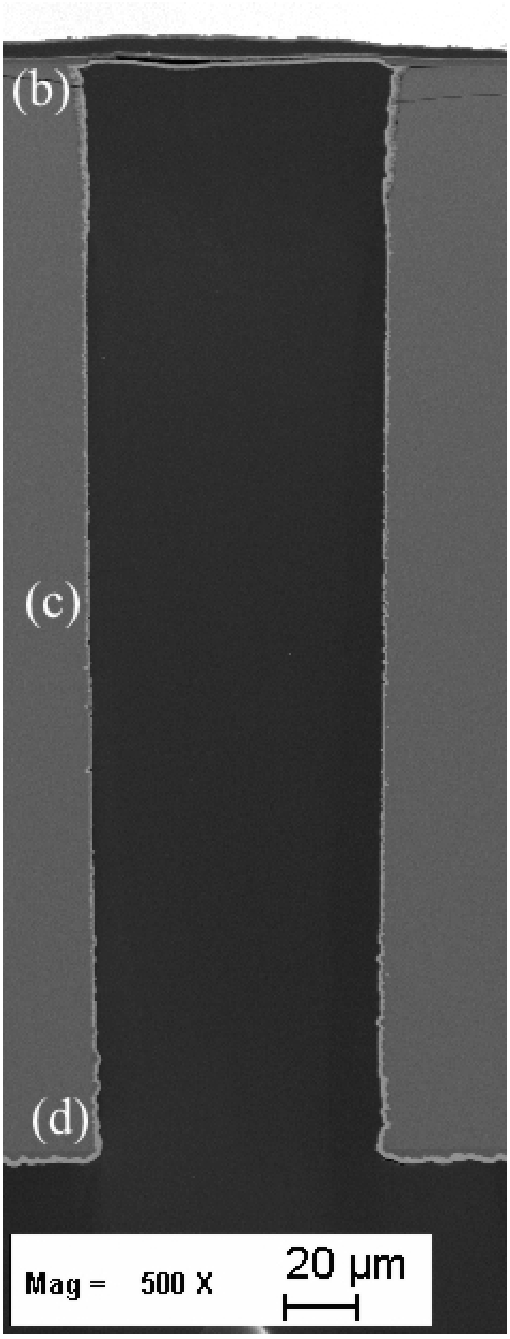
Experiment A TiN and Cu were deposited into 300μm deep blind holes with different aspect ratios (Applied Materials P5000, 150°C substrate temperature, 10Torr process pressure). A Cu step coverage close to one was observed for all aspect ratios. The pressure used was several orders of magnitudes higher compared to other CVD or PVD techniques. This results in a low mean free path of the molecules and several reflections of the molecules inside the TSV occur. A pressure gradient inside the TSV did not occur [80]. A constant reaction rate on the entire TSV sidewalls was taking place. A TiN film thickness decrease about 60% was observed. However, the TiN film deposited showed no pin holes even at the hole bottom and can be considered as a sufficient diffusion barrier for the TSV targeted.
Figure 4.25(a) shows an overview of a TSV with an aspect ratio of 3.75. The close ups of figure 4.25 show the deposited film at the TSV entrance (b), at 150μm depth (c) and at the TSV bottom (b).
The electrical resistivity of the deposited Cu on the TSV sidewalls was measured indirectly. A specific Cu resistivity of 3.1$\mu\Omega$cm $\pm$ 0.3$\mu\Omega$cm was determined on top of a grinded wafer surface (grid 2000). It can be assumed that the specific Cu resistivity inside the TSV is comparable to this measured value. Both surfaces, the grinded surface and the sidewalls inside the TSV, show a comparable roughness and the Cu grain structure was similar in the deposited films. First electrical measurements showed an electrical resistance of 32mΩ $\pm$ 8mΩ for a 1μm thick Cu layer deposited by MOCVD in a 300μm deep TSV with a diameter of 80μm. This value is slightly higher compared to the theoretical value of 22mΩ and can be explained by a non optimized electrical contact between the Cu deposited and the 1st level metallization.



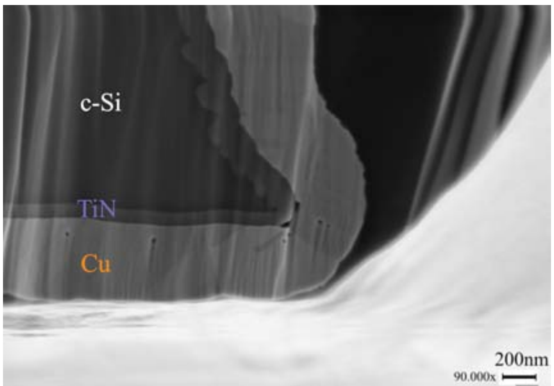
(b) TSV bottom



(c) TSV center



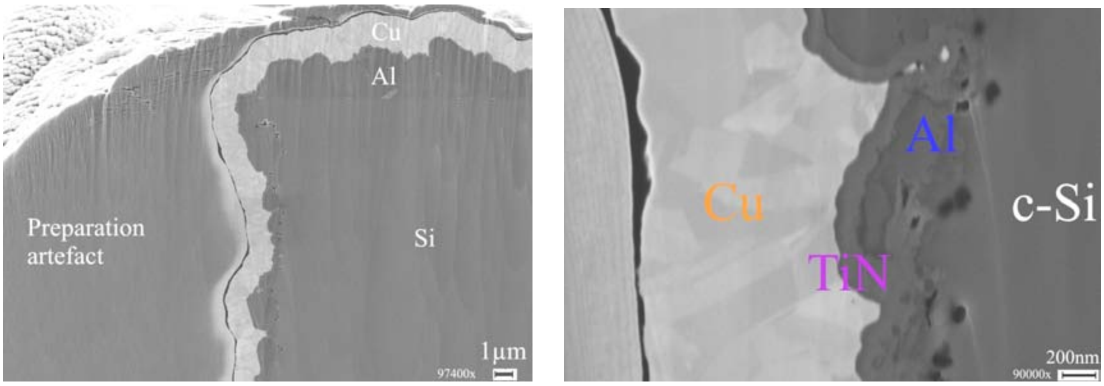
(a) TSV overview



(d) TSV entrance

Figure 4.25: Deposited Cu film inside the TSV obtained by MO-CVD.

Experiment B Al was deposited by hollow cathode sputtering on the test wafer design in order to increase the surface roughness of the substrate. Chapter 4.2.2 shows that the surface roughness is enhanced by increasing the substrate temperature. This rough surface simulates possible extreme surface irregularities from the deep reactive ion etching process like notching or so called mouse-bits. Figure 4.26(a) shows an overview of the TSV entrance. The deposited layers are indicated. The close up of figure 4.26(b) indicates that TiN and Cu smooths rough surfaces. This smoothing phenomenon is not common for other deposition techniques used in microelectronic device or MEMS fabrication. A phenomenological explanation based on the idea that the residence time and hence growth velocities are dependent on the curvature of surfaces is presented in the following.



(a) (b)

Figure 4.26: Cu deposition inside the TSV by using MO-CVD smooths surface irregularities. (a) Cross section after Al,TiN and Cu deposition. Al enhances the surface roughness. (b) Close up of (a).

The impinging Cupra Select flux adsorbs and desorbs at a certain surface site as shown in figure 4.23. Molecules remain a certain time at surfaces before they desorb. This residence time is expressed by:

$$\tau_s = \frac{1}{\nu} e^{\frac{E_{des}}{k_B T}} \tag{4.18}$$

where ν, E_{des}. k_B and T are the vibration frequency of an atom on the surface, the required energy to desorb back into the vapor, the Boltzmann constant and the system temperature, respectively. Molecules, which have not reacted to the surface, execute randomly. The residence time is higher inside valleys according to a larger interaction probability of desorbed molecules inside the valleys with other desorbed or new impinging molecules. The flux of

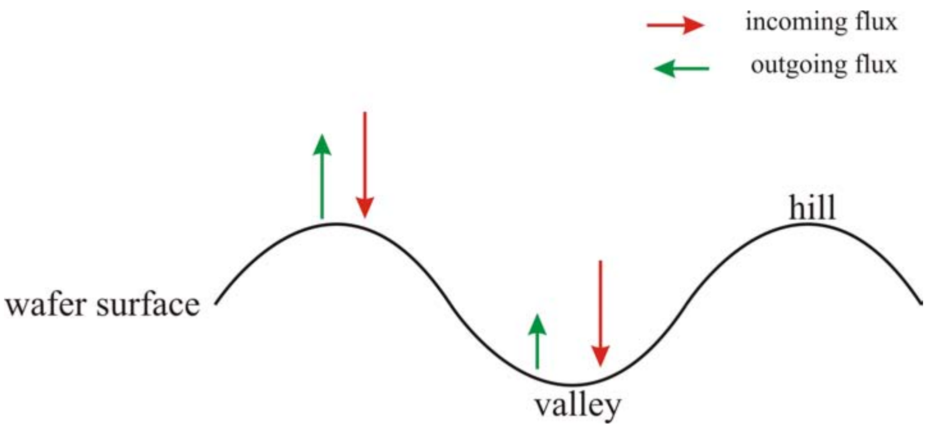


Figure 4.27: Flux rates dependent on the surface location.

the desorbed species out of valleys is therefore much smaller compared the same flux on the hills. This context is shown schematically in figure 4.27.

The Cu nucleation rate $\dot{N}$

$$\dot{N} = N^* \cdot A^* \cdot \omega \tag{4.19}$$

is consequently also higher inside the valleys. N^*, ω and A^* are the equilibrium concentration of stable nuclei and the neutral Cu atom impinge rate onto the nuclei critical area, respectively. N^* and A^* are assumed to be constant. ω is a function of the CupraSelect impinge rate r_m, the residence time τ_s and a surface diffusion related term D^* and can be expressed by

$$\omega = r_m \cdot \tau_s \cdot D^* \tag{4.20}$$

Thus, the nucleation rate is a function of the residence time and is therefore higher inside valleys. Figure 4.26 shows also that the formed Cu grains inside the valleys are much smaller compared to Cu grains in other positions, which correspond to the theoretical considerations. In addition, the higher nucleation rate and therefore the higher growth velocity inside the valley tend to smooth surface irregularities. This effect is not common for CVD processes. For instance, SiO_2 deposited with the precursor *tetraethylorthosilicate* (TEOS) $C_8H_{20}O_4Si$ deposited by low pressure CVD (LP-CVD) at 700°C covers rough surfaces conformally, but the topography of the substrate is reproduced during the SiO_2 film formation. The incoming and outgoing fluxes are balanced at the temperatures used. SiO_2 deposition with a TEOS precursor is also possible at lower temperatures, whereas an ozone activated plasma (PE-CVD process) is used during the deposition process [81]. This technique allows deposition at temperatures below 400°C. Figure 4.28 shows a comparison of a LP- and PE-CVD SiO_2 film by using the TEOS precursor. The low temperature process shows a smoothing, too. It can be concluded that a use of low temperature CVD deposition processes and using organic precursor result in a smoothing of surface irregularities.

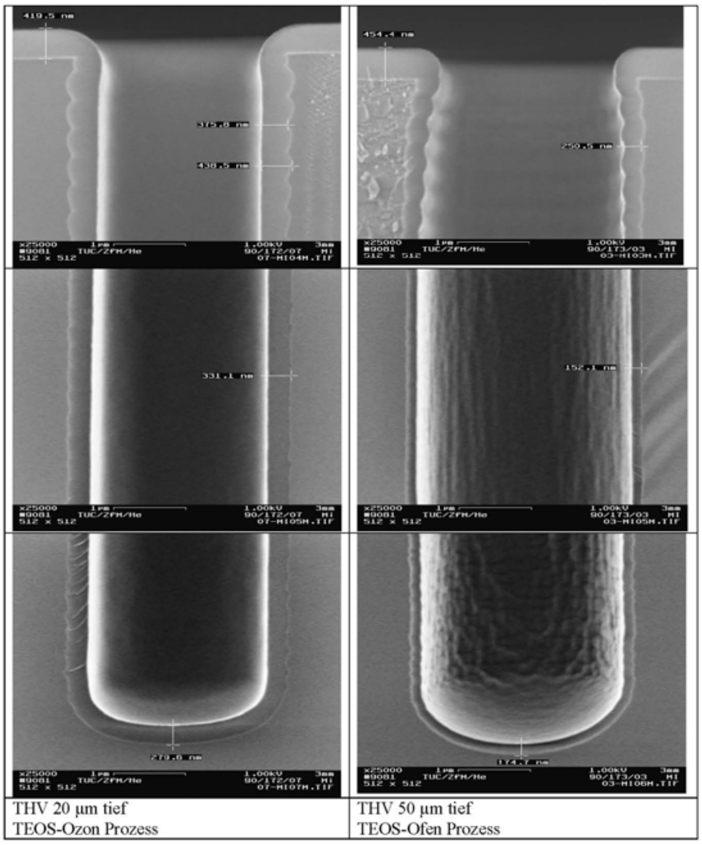


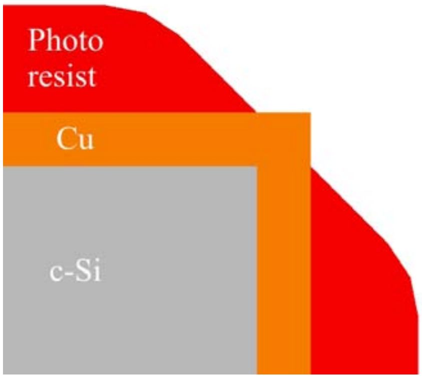
Figure 4.28: Deposited SiO_2 inside trenches whereas a TEOS precursor is used. The left picture shows a ozone activated plasma enhanced CVD process at a deposition below 400°C and the right picture illustrates SiO_2 deposited film by a low pressure TEOS CVD process. Results from the Fraunhofer ENAS.

4.3 Pattern transfer

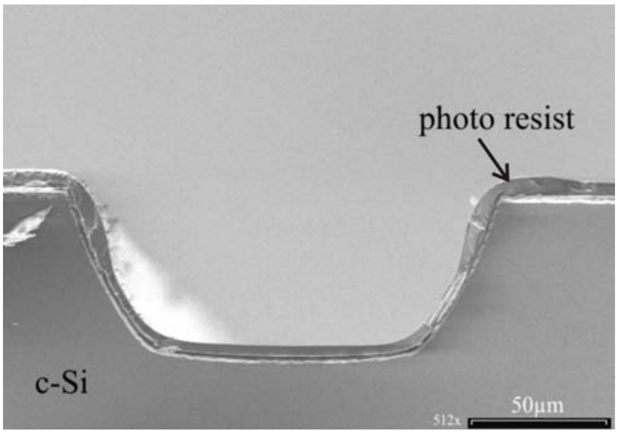
Conventional technologies

Pattern transfer inside deposited layers by using photo lithography and etching processes is a standard process sequence in all CMOS devices or MEMS. A photosensitive layer (photoresist) is thereby spincoated on top of the layer to be structured. The pattern inside the photoresist is realized by an exposure to light at a certain wavelength through a glass mask. Glass masks are fabricated in such a way that the light only interacts with the photoresist in defined positions. The light is adsorbed by a Cr-layer on the glass mask in the other regions. Two different tones of photoresists are developed. Photoresist remains on exposed areas after development by using so called positive photoresists, whereas the resist dissolves in this areas by using negative tones. The photo sensitive part of photoresist (initiator) changes their chemical stability against bases like NaOH during exposure. For instance, initiators change to acids (carbonic acid) by light exposure in positive photoresists. This acid reacts with the developer and forms a water soluble salt. Wafers are finally rinsed and dried to stop the chemical reaction. This structured photoresist is used to form the pattern in the underlying structure by etching processes.

Photoresist coating is the most crucial process for structures with a high aspect ratios. Spincoating processes, which are predominantly used, are based on rotating wafers on which liquid photoresists are dosed at the wafer center. A conformal resist thickness over the entire wafer is obtained by rotating the wafer. This spinning does not cover holes or even allow a conformal resist deposition on hole sidewalls. The resist does not cover the hole entrance edges like it is shown in figure 4.29 (a). Thus, spincoating is not a appropriate technique for the pattern transfer inside the deposited TSV materials. Cu deposited by MO-CVD or other techniques is etched at the hole entrance during the following wet chemical etching.
Therefore, spraycoating got a higher importance especially for MEMS, where high aspect ratios occur. Photoresists are sprayed through a nozzle on top of the wafer. The wafer is moving underneath the nozzle in x- and y-direction or vice versa until the wafer is conformally coated with photoresist. The process time needed for spraycoating is longer compared to spin coating. However, spraycoating allows a photoresist deposition in deep structures like it is shown in figure 4.29 (b). A 60μm deep cavity is formed by KOH etching and coated with a photoresist by using a spraycoating process. This performance makes spraycoating interesting for industrial production. EVG announced in 2007 that they



(a)



(b)

Figure 4.29: photoresist deposition by spin and spray coating. (a) Spin coated photoresist on wafers with high topography like TSV holes. (b) Spray coated photoresist inside a 60μm deep KOH etched cavity.

developed a spraycoating process for a 300μm deep blind holes with a diameter of 100μm. Photoresist drops are formed by an ultrasonic nozzle in this technique. This creates small drops and results in a fine photoresist mist. All surfaces exposed are covered by this mist. The available spraycoating tool at Fraunhofer ISiT forms photoresist drops by a nitrogen gas stream, which is blown inside a photoresist stream directly after the resist comes out of a nozzle. The nozzle shape, resist type and the gas flow defines the drop size. However, problems arise by using this drop generation technology in the TSV flow targeted. A nitrogen stream blows inside the TSV holes and a back pressure is formed, which avoids a conformal resist deposition at the hole sidewalls. A photoresist accumulation occurs at the hole bottom. A complete photoresist stripping is hard to achieve if these resist accumulations appear. Resist residuals can cause reliability problems of devices.
Electrophoretic photoresist deposition is reported in the literature as an alternative coating technique [82]. The coating process is similar to electro-plating. The wafer is connected to an electrode and placed into an electrolyte, which contains the photoresist. A voltage is applied between the electrode which is connected to the wafer and a second electrode inside the electrolyte. This allows a conformal deposition even if high aspect ratios are present on the wafer. However, the surface on top of the wafer must be electronically conductive. This technique allows a photoresist deposition on metals. The electrolyte condition changes with time and must be regulated during batch processing. Available bath control units are expensive. Thus, electrophoretic photoresist deposition is not used in CMOS or MEMS

fabrication.
The use of a photo sensitive foil is a other to way to protect 3D structures like TSV holes and will be presented later in detail.

Etching of metallic films like Cu or Al is often performed by wet chemical etching techniques by using PWS (80% phosphoric acid, 16% water, 4% nitric acid + tensid) and is a standard technique. The mutistep reaction meachanism occurs as follows [49]. Cu is first oxidized by the nitric acid. The phosporic acid and water etch the resulting CuO. The concentrations used allow an oxidizing and etching at roughly the same rate. The bath must not be controlled over time. Metal alloys like TiN can be etched by physical etch or wet chemical processes, whereas physical etch processes are commonly used in CMOS fabrication lines.

Dry resist photo lithography and Cu etching

Method

Photosensitive foils are commonly used in the fabrication of printed circuit boards (PCB) to protect vertical interconnects (vias) during Cu etching. The challenge of a 3D lithography in the TSV sequence targeted is therefore comparable to PCB applications. Spincoating processes as described before are not useful due to the rectangular PCB shape. Liquid resists will not cover corners sufficiently enough in order to protect deposited films in further etching processes. Thus, photosensitive foils are laminated on top of the PCB and trimmed to the PCB shape. The further processing is similar to photo lithography steps in semiconductor industry. First, the resist is exposed to light through a mask. An additional heating step is not required in order to remove organic solvents. Dry photoresist development can be accomplished using conventional spray developers with water based carbonate solutions. The foils can be removed (stripped) after etching processes are performed from the substrate by KOH- or NaOH based solutions.
Dry photoresist foils are delivered on a roll. Thus, protection foils are on top and below the photo sensitive film in order to separate the layers on the roll. Figure 4.30 (a) shows a typical three layer structure used of dry photoresist foils. Polyester films protect the photosensitive polymer film from particles or other contamination during handling. The composition of the photosensitive film is most likely confidential. However, they are based on acrylate polymers. The backside foil is based on polyethylene polymer foil.
The lamination principle of dry photo sensitive foils to substrates or wafers is shown in figure 4.30 (b). The resist roll is mounted on a rotating wheel and the foil end is placed

between two heated rolls made out of rubber. The rolls are heated resistively up to temperatures around 100°C . . . 120°C. The polyester film is separated from the photo sensitive foil in order to allow the contact between the substrate surface and the the photosensitive layer. The elevated temperature is required in order to improve the adhesion between the substrate and the photosensitive foil. Foils used are normally larger compared PCB or Si-wafers. In this case the photosensitive foil sticks to the lower roll and the roll must consequently cleaned after etch experiment. Thus, a protection foil is routed also between the rolls to protect the lower roll. Substrates are placed between these two foils and the rotating rolls and will be lead through the heated rolls automatically. Temperature, roll velocity, contact pressure between the two rolls and the substrate itself are the process parameters which determine the lamination quality.
The laminated photosensitive foil overlaps wafer corners. A radial cut around the wafer is therefore required before further wafer handling steps are possible. The polyethylene foils is still on top of the photosensitive foil, which allows a stacking of wafers on top of each other without changing properties of the photosensitive foil. This is not important for Si-wafers, because they are stored inside carriers in which wafers are not in contact. The further processing is similar to standard photolithography process step [52]. The following investigations show how dry photoresists can be integrated in the TSV process sequence targeted.

Results and Discussion

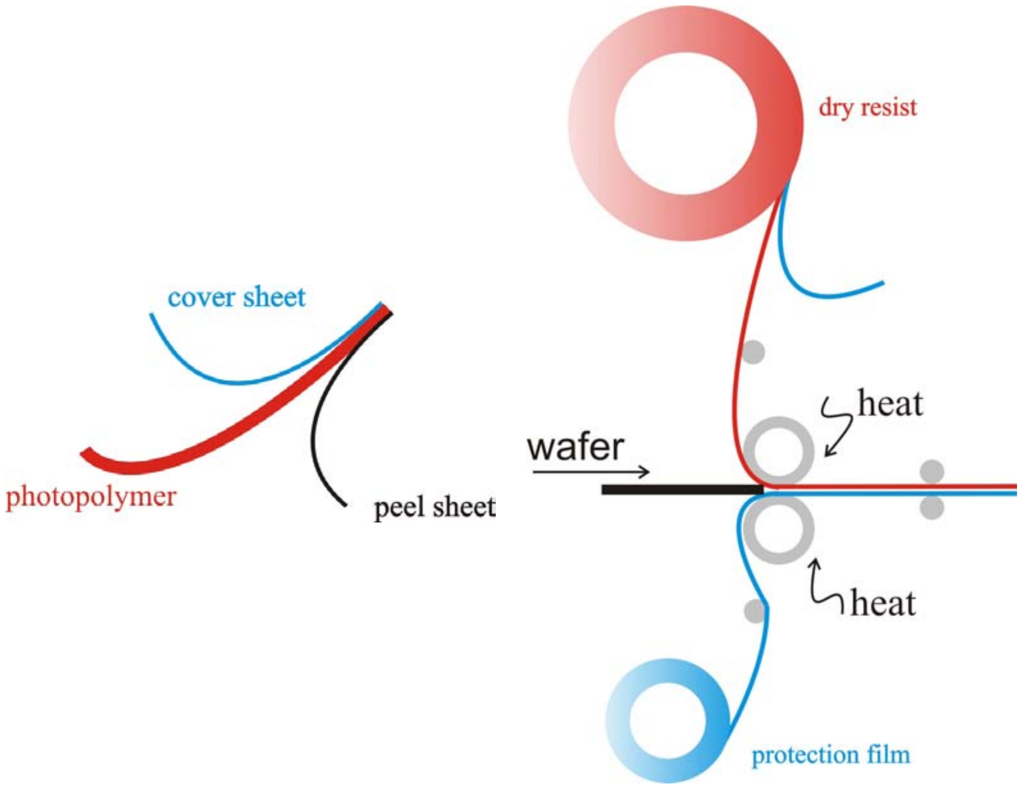
This dry resist lamination technique is evaluated for the use in TSV flows. The following experiments were performed:

Experiment A Dry resist lamination on wafer surface conditions.

Experiment B Evaluation of the maximum resolution.

Experiment C Protection of metallization inside TSV during metal etching.

Experiment A The dry resist KL1015 from the company Kolon was used during the experiments performed. Wafers were laminated by using different temperatures. The contact pressure was not varied, because the instrument used (Rollenlaminator DH 360 XL / A3) did not allow a reproducible adjustment of the rolls. A variation of the lamination speed has not shown a significant difference of the lamination quality. The adhesion of the laminated foils on top of polished Si - wafers and grinded wafers (grid 2000) were compared to the lamination on top of Cu films. The Cu films were deposited on top of polished c-Si



(a) (b)

Figure 4.30: Dry photoresist foil and lamination setup. (a) Dry photoresist foil composition. (b) Lamination setup.

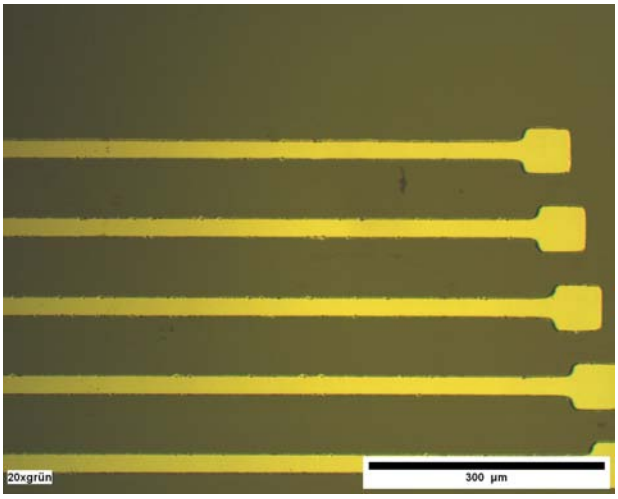
wafer by using magnetron sputtering and MO-CVD. Table 4.4 shows a adhesion quality rating of different experiments performed. The adhesion criteria was defined as followed: The photosensitive foils were removed by hand similar to the peel tape adhesion test [72]. Very good adhesion (++) was marked when the foil was not removable from the wafer. Good adhesion (+) was obtained when the foil was removed only at the wafer edges. Partial adhesion (-) was rated when not more than 20% of the foil was removed and poor adhesion (- -) was rated if more than 20% of the foil was removed.

Process temperature	**Si polished**	**Si grid 2000**	**Cu^a**	**Cu^b**	**Comment**
90°C	- -	+	+	+	
100°C	- -	++	+	+	
110°C	-	++	++	++	
110°C	-	++	++	++	
120°C	+	++	++	++	photo sensitive foil changed color

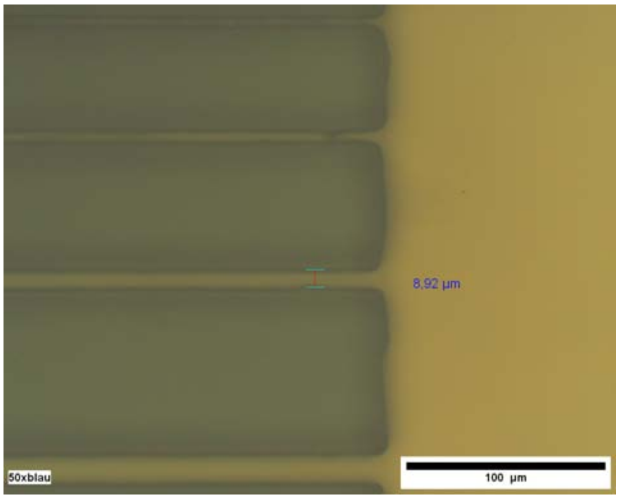
Table 4.4: Adhesion quality of a laminated photosensitive foil on different surfaces. Adhesion rating: ++ very good adhesion, + good adhesion, - partial adhesion, - - poor adhesion. The rating criteria is explained in the text. ^{a} deposited on a polished wafer by magnetron sputtering, ^{b} deposited on a polished wafer by MO-CVD

Table 4.4 shows that the foil adhesion is only not acceptable for polished Si. However, a good adhesion on the polished surface was obtained by using a temperature of 120°C. A color change of the photosensitive foil from light green-blue to dark blue was observed during the lamination at this temperature. This color change was also observed during the light exposure. Therefore, it can be concluded that the lamination temperature must be below 120°C. In addition, the dry resist foil adhesion on each Cu film was sufficient.

Experiment B The maximum resolution of the photolithography depends on the resist thickness and on exposure parameters [52]. Dry photoresist foil thickness are thicker compared to conventional liquid based photoresists. Foils thicknesses up to 120μm are common. The thinnest available foil (15μm) was used in this work. Figure 4.31 (a) shows Cu conduction path obtained after PWS etching, whereas a dry photoresist foil was used. The path width was 20μm. The path edges are not sharp. However, this is important for a reproducible redistribution layer on the wafer back-side. The path width must be therefore larger than 20μm. In addition, figure 4.31 (b) shows that the maximum resolution is around 9μm for the dry resist used. This resolution is sufficient for TSV applications.



(a)



(b)

Figure 4.31: Pattern transfer in Cu by using dry photoresist foils and PWS.(a) Cu Conduction paths formed. (b) Maximum resolution of dry photoresist foil.

Experiment C The protection of the deposited metal inside the TSV cavities is the major lithography challenge. This experiment showed how dry resist foils prevent a Cu-etching inside TSV cavities. First, 50μm deep holes were formed and a Cu seed layer was deposited inside these holes. The Cu thickness was enhanced to 2.2μm in order to investigate possible Cu etching by PWS inside the holes with a optical microscope. A dry photoresist foil was laminated on top of the of the wafer and further required lithography steps were applied before the Cu was etched by PWS. Figure 4.32 shows the structure described after Cu etching and resist removal. The Cu inside the hole was not attacked and it can be concluded that dry photoresist foils allow a protection of the metallization inside the TSV holes during back-side etching.

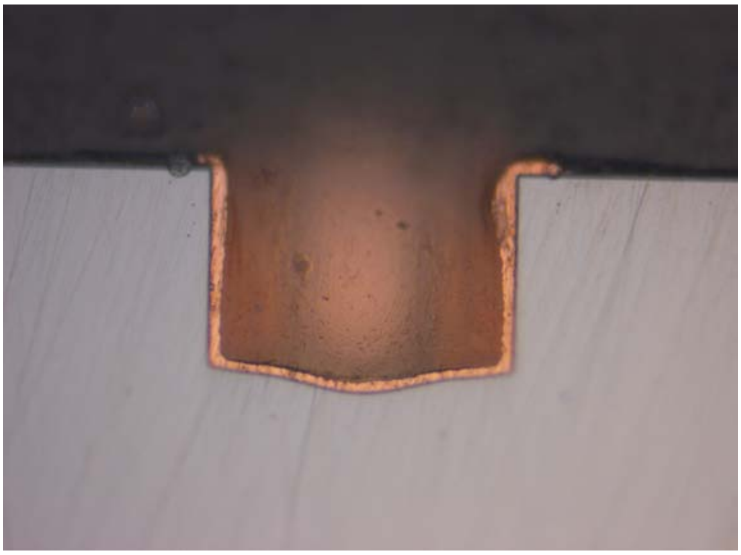


Figure 4.32: Cu film inside a 50μm deep hole after Cu etching and dry photoresist removing

PWS shows a high selectivity against TiN. This film was removed in a dip of HF based etchants after resist removal. Figure 4.33 shows a obtained Cu redistribution layer on the wafer back-side after the described treatment.

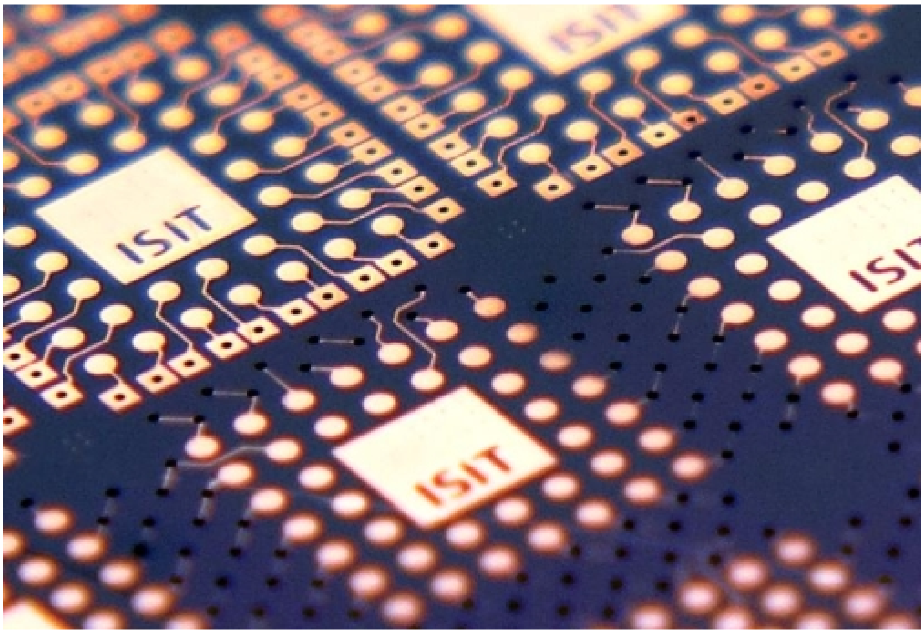


Figure 4.33: Wafer back-side after PWS etching.

4.4 Technology summary

The realization of TSV in wafer with thicknesses $>300\mu$m implicate a high challenge for several technologies required. Thus, the previous chapters investigated different technologies for their usability in the TSV flow targeted. This chapter summarizes the results.
A high anisotropic etch technique is required for the TSV hole/cavity formation. Laser ablation showed good anisotropy and high etch rates. However, a selective etch stop on the 1^{st} level metallization was hard to achieve. Only deep reactive ion etching allowed an anisotropic $>300\mu$m deep c-Si etching. The instrument used in this work showed an etch rate of approximately 5μm per minute. Etch times over one hour were required to form $>300\mu$m deep cavities. This results in an expensive process. However, new DRIE etch tools promise etch rates up to 20μm a minute for the given TSV structures. DRIE is therefore the best technique usable for TSV with a hole depth of $>300\mu$m.
A PMD etching requires a combination of etch processes for silicon nitrides and oxides. The first PMD layer is a silicon nitride layer which was removed in situ during the c-Si etching by DRIE. LTO and PSG are the next PMD layers. The RIE tool used have not shown any parameter combination to etch the 950nm thick layer stack. A buffered oxide etch (BOE) of these layers showed the possibility to remove these layer stack, whereas no under-cut was observed. The Ti diffusion barrier was removed to by using this technique, which reduces the contact resistance with the deposited metallization film. Chapter 3.2.1 showed an alternative approach to realize a proper electrical contact between the front-side pad-cell and the TSV metallization by arranging a second pad-cell next to the original pad-cell. This rearrangement was caused by existing ESD structures in the area of 1^{st} level metalizations. The PMD can be removed at the TSV hole positions from the wafer front-side during the formation of these new pad-cell structure. Processes required are standard and show a low reliability risk for the final device. Further processes to form the pad-cell are identical as described in chapter 3.2.1. The DRIE etch process for TSV hole formation will stop directly underneath the 1^{st} level metallization in this case. In addition, notching at the TSV hole bottom will be minimized, because Ti shows a better electrical conductivity compared to the PMD layers used in this work. Thus, PMD or other isolating layers underneath the front-side pad-cell should be etched from the wafer front-side during the TSV implementation in thick ($>300\mu$m) wafer.
The HW-CVD and PE-CVD techniques showed the possibility to deposit pin-hole free a:Si_xN_y:H isolation film inside TSV cavities. However, films deposited by PE-CVD showed a better step coverage compared to HW-CVD films. Thus, PE-CVD films are used in the following sequences.

Two different metallization techniques were evaluated in this work. Gas flow sputtering of Al or Cu showed the possibility to deposited material inside the given TSV geometry even on the sidewalls, whereas a poor step coverage was observed. The surface morphology showed a high porosity specially at the sidewalls near the hole bottom. The electrical resistance measured was too high for the TSV requirements in this work. The MO-CVD metallization process sequence developed by Riedel [79] allowed a deposition of TiN and Cu inside the TSV targeted. Both materials were deposited inside the TSV hole with a high step coverage, whereas a Cu step coverage close to one was observed. In addition, the resistivity of the deposited Cu and the realized film thickness of 1μm does not require a film thickness enhancement by electroplating. The electrical TSV resistance measured showed a sufficient value for several MEMS packages like describe in chapter 3.5. The MO-CVD deposition process showed a smoothing of surface irregularities, which were formed during the hole formation. Thus, MO-CVD is a deposition technique which allows the realization of a suitable TSV metallization in thick wafer.

The structuring of the metallization layers (TiN, Cu) on wafer back-sides is one of the last process steps in TSV process sequences. Cu deposited inside the the TSV holes must be protected during this etch process. Conventional photoresist deposition techniques (spincoating) does not allow a suitable coverage inside the holes. Spraycoating was was developed to cover structures with high aspect ratios with photoresist. However, the spraycoating tool used in this work has not shown a reasonable step coverage inside the TSV holes. A lamination of photosensitive dry resist foils on wafer back-sides showed a good protection of the deposited Cu films. This lamination technique is so far not a common technique in MEMS or CMOS fabrication lines and should be considered as a useful complementary technique. Photolithography processes were developed in this work based on dry photoresist foils. All processes developed showed a fully post-CMOS compatibility.

5 Process Flow Integration

A proposed process flow of a post-CMOS compatible TSV integration in MEMS packages is presented in this chapter. The flow chart developed is shown in figure 5.1 and is based on the results of chapter 4. In addition, the resist types used are indicated. Resist development, resist stripping and further cleaning procedures are not shown.

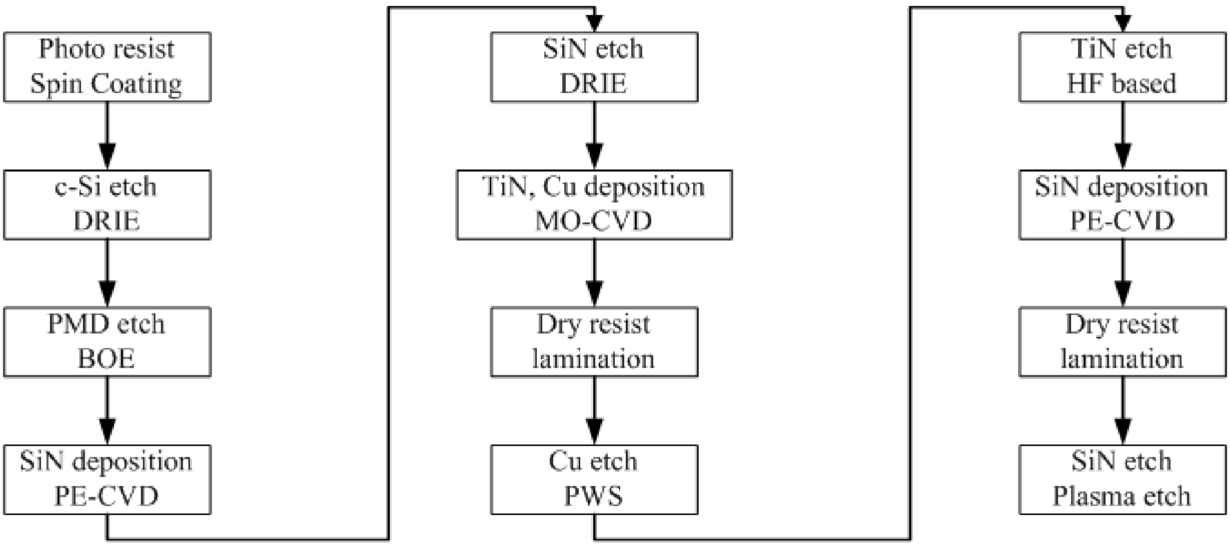


Figure 5.1: post-CMOS compatible TSV process sequence.

5.1 TSV in Test-Design

Initial wafer state

The test wafers were fabricated like described in section 3.6 and thinned to a final thickness between 300μm and 400μm. This state shall be deemed to be the initial wafer state for the following TSV sequence and is shown in figure 5.2.

Etching of c-Si and Si_3N_4

The first step of the hole formation was performed by deep reactive ion etching. Figure 5.3 shows this process step schematically and a graph of the obtained vertical etch profile.

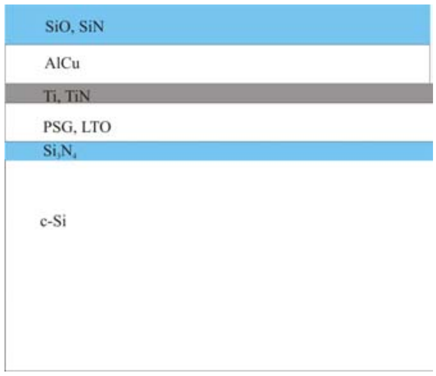
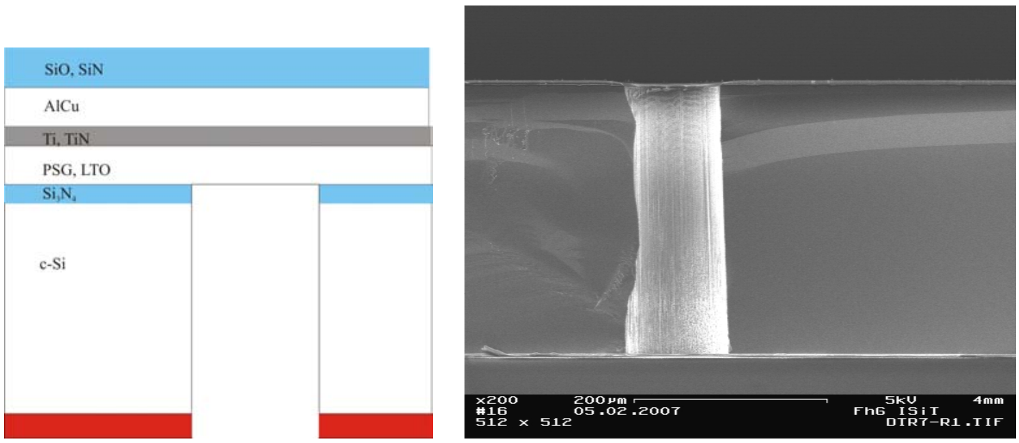


Figure 5.2: Initial wafer state of TSV process flow.

This process removed both materials (c-Si and Si_3N_4) inside the TSV hole. Etch residuals were not observed.

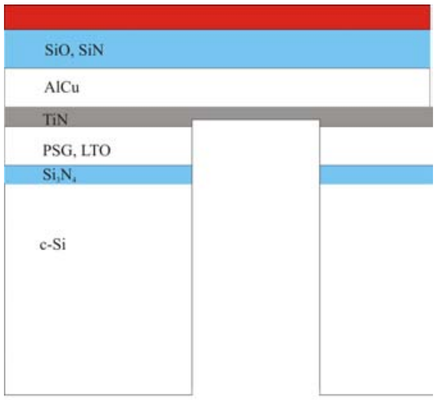


(a) (b)

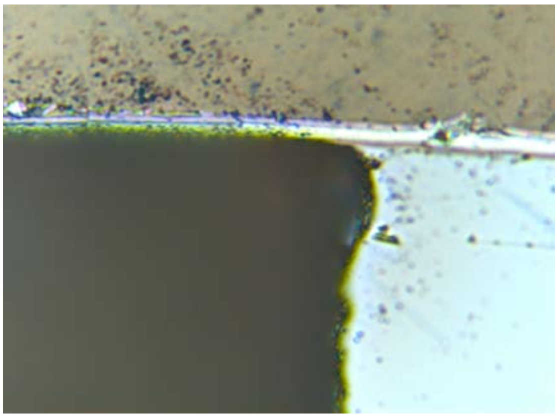
Figure 5.3: Hole formation by etching c-Si and Si_3N_4 by using DRIE. (a) Schemata of the etch profile. (b) Obtained etch profile in a 300μm deep TSV cavity.

Etching of the PMD

The PMD was etched by a BOE based etchant. This process removed the LTO and the PSG layer as well as the Ti adhesion promoter of the 1^{st} level metallization. Figure 5.4 shows this step schematically as well as the obtained etch result. This process step can be considered as critical. The wet chemical etching and the necessary cleaning can result in residuals inside the TSV cavity and a reliability risk arises during the device lifetime. A corrosion of the metallization is possible.



(a)



(b)

Figure 5.4: PMD etching by using BOE. (a) Schemata of the etch profile. (b) Obtained etch profile in a 300μm deep TSV cavity.

Isolation deposition

An a:Si$_x$N$_y$:H isolation layer was deposited by PE-CVD. Figure 5.5 shows this step schematically and a deposited a:Si$_x$N$_y$:H film at the TSV hole bottom is indicated. The film showed no pin-holes after a KOH-etch test which avoids cross talking between different TSV signals or other functional elements.

Selective isolation etching

The isolation layer deposited must be opened selectively only at the hole bottom. An etch process based on DRIE removed the a:Si$_x$N$_y$:H anisotropic as shown in figure 5.6. The remaining isolation layer on the sidewalls showed also no pin-holes.

Metallization deposition

The metallization layer was realized by a TiN,Cu layer stack by using MO-CVD. Figure 5.7 shows this process step schematically and a cross section of the test design is indicated. Both materials showed a good step coverage.

TiN,Cu pattern transfer on wafer-backside

The deposited metallization was structured by using a dry photoresist foil to protect the Cu inside the TSV holes during PWS etching. TiN was etched in a HF based etchant.

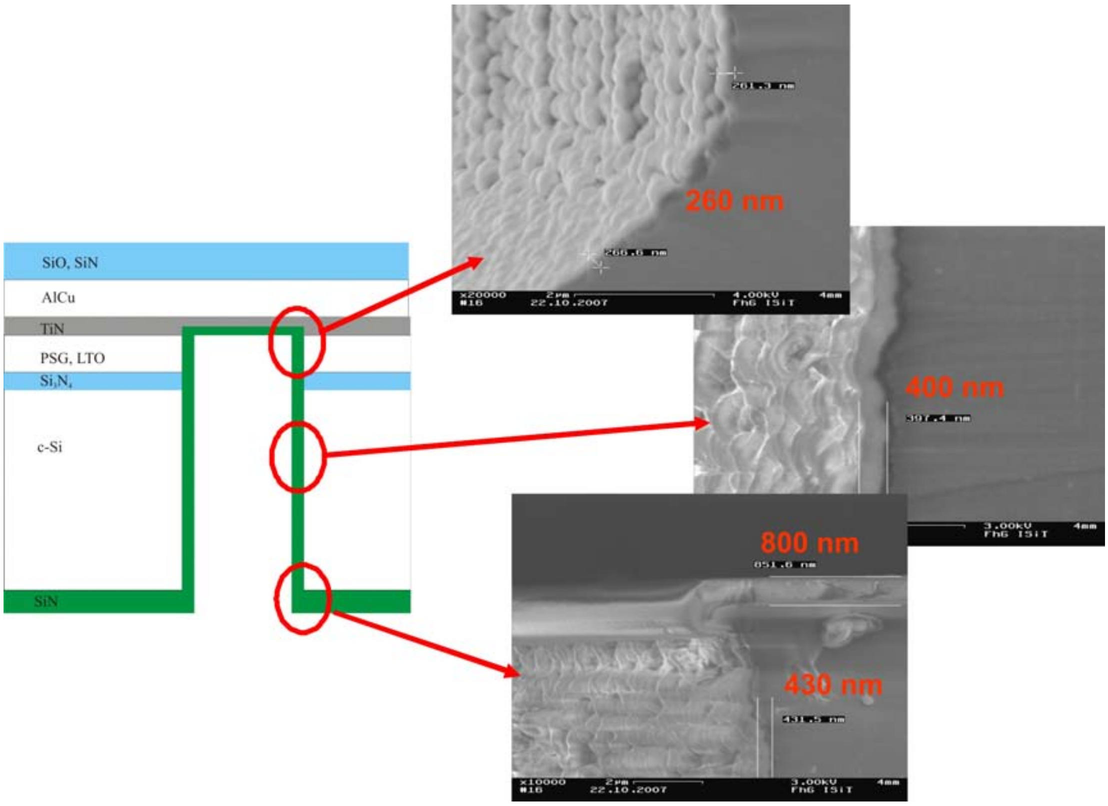


Figure 5.5: Isolation deposition (a:Si$_x$N$_y$:H) by PE-CVD. Schemata and obtained films are indicated. The pictures are rotated.

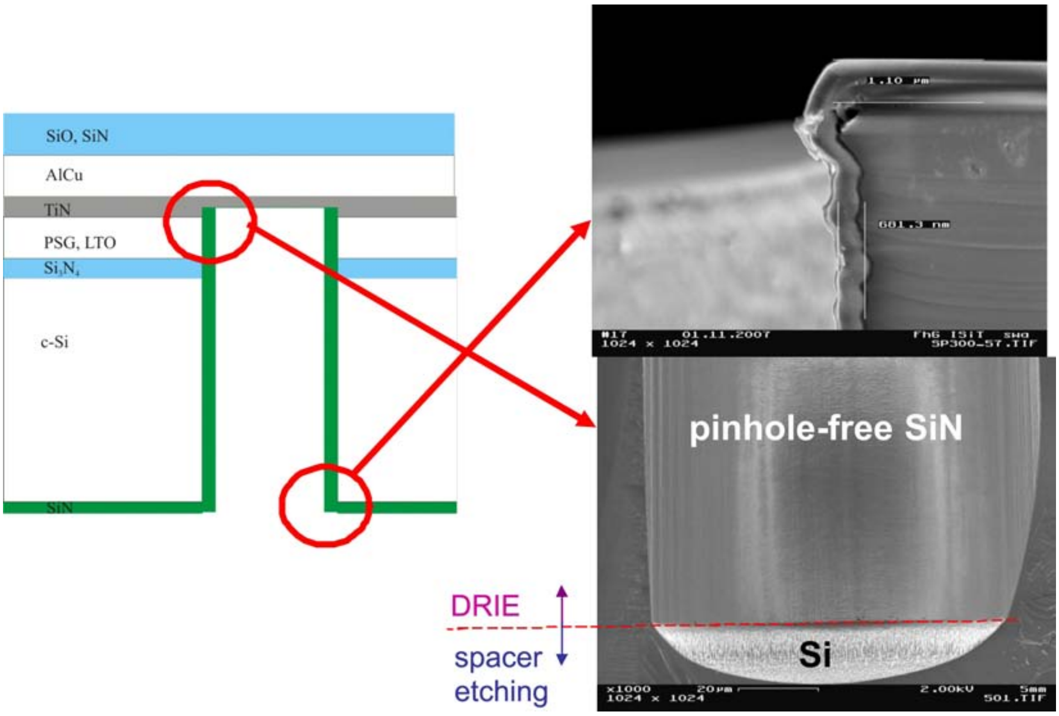
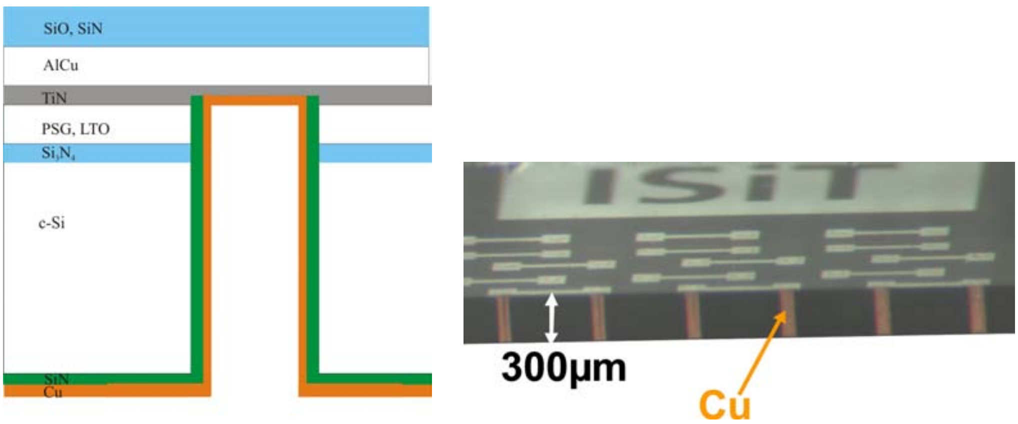


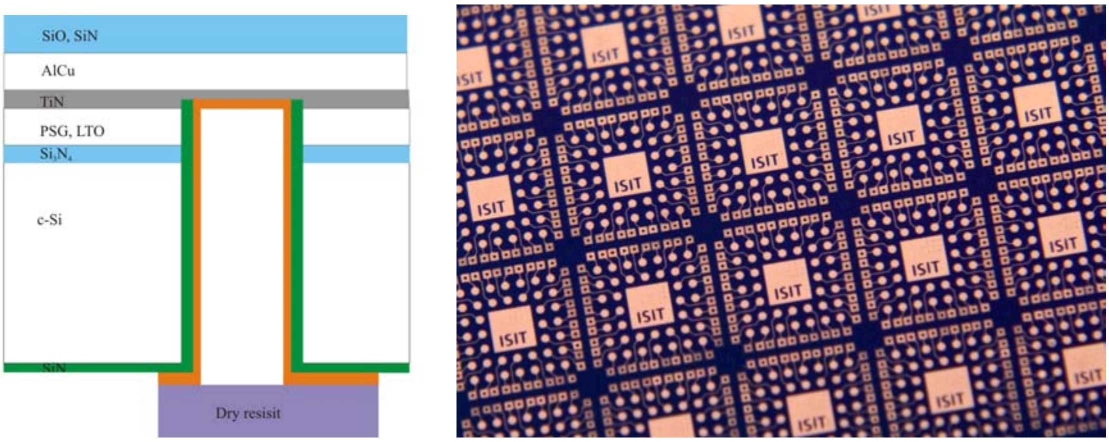
Figure 5.6: Etching of the isolation layer by DRIE.



(a) (b)

Figure 5.7: Metallization of TSV by using MO-CVD. (a) Schemata of the metallization step. (b) Cross section of the obtained deposition.

Figure 5.8 shows this process step schematically and a photo of the obtained back-side redistribution layer.



(a) (b)

Figure 5.8: Redistribution layer on wafer back-side. (a) Schemata of this pattern transfer step by using dry photoresist foils. (b) Photo of the realized wafer back-side.

Passivation layer deposition and pattern transfer

This process step is a combination of the deposition of an a:Si$_x$N$_y$:H film similar to the isolation layer and the pattern transfer by using a dry photoresist foil. This process step was not finally evaluated. A layer of a:Si$_x$N$_y$:H must be deposited by PE-CVD and a dry photoresist must be laminated on the wafer back-side. A standard plasma etch process for SiN can be used to define the pad-cell positions on the wafer back-side. Figure 5.9 shows this process schematically

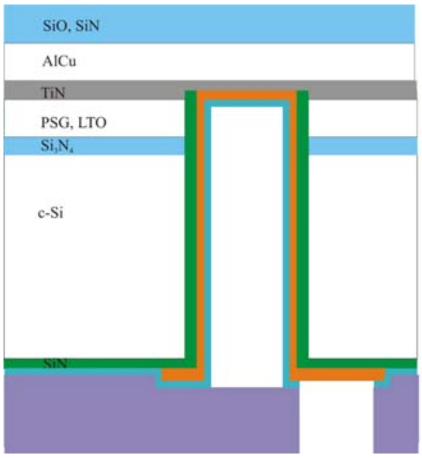


Figure 5.9: Anisotropic etching of the isolation layer by DRIE.

Front-side pad-cell stability

TSV for MEMS packages shows a hermetic front-side pad-cell structure as mentioned in chapter 2.2.4. Thus, the stability of the layer structure is important during the entire process sequence and during device lifetime. Chapter 4.1.2 showed that an implemented SiO layer on the wafer front-side stabilizes the front-side pad-cell during PMD etching. However, further processes treat this layer structure with heat excursions or pressure gradients. A pad-cell buckling of approximately 280nm was observed after the here described process flow. Wafer pieces were placed in a vacuum system in order to control the hermeticity of the realized TSV. The experimental setup and applied pressures on both sides are indicated in figure 5.10. A pressure increase on the vacuum side was not observed. It can be concluded that the fabricated TSV are hermetic. However, further gas leakage and water penetration tests must be performed in the future in order to guarantee the hermeticity of the TSV under several measurement conditions.

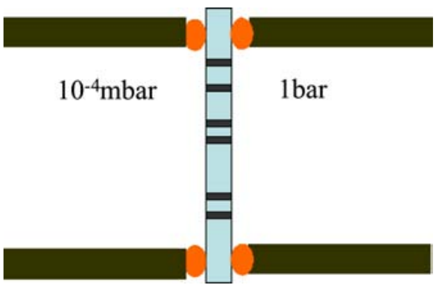


Figure 5.10: Experimental setup to control the hermeticity of TSV

5.2 TSV in the David-project

The technologies and process sequence described in the previous chapters allow an integration in ASIC wafer. The entire process sequence is post-CMOS compatible. Chapter 3.2.1 showed that a redistribution of the pad-cell is sometimes necessary due to an existing ESD-structure near the 1^{st} level metallization. The new pad-cell formed should be placed directly on top of the c-Si in this case in order increase the TSV process flow stability. Thus, the PMD must be removed in this area before the 1^{st} level metallization is deposited.
The DAVID approach (see chapter 2.2.4) requires a final molding step to form a CSP. Figure 5.11 shows the experimental setup, which was used for the molding at Fico B.V. in The Netherlands. A detailed process description is given in [34].

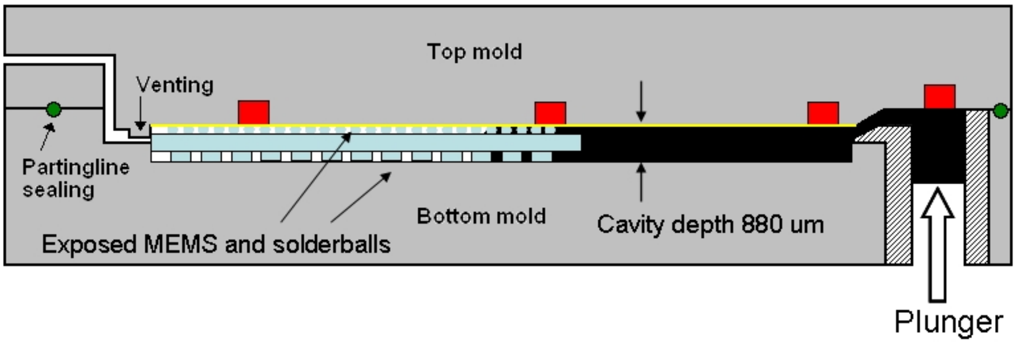


Figure 5.11: Experimental Setup for wafer molding

This process allows to fill TSV with mold compound. No voids were observed, whereas an evacuation of the mold cavity is not mandatory. Mechanical considerations have shown that the pad-cell cell is deformed marginal during this molding step, which is in agreement with the obtained results like shown in figure 5.12. Thus, the developed TSV flow can be integrated in thick ASIC wafer and they withstand additional loads applied by packaging processes like molding.

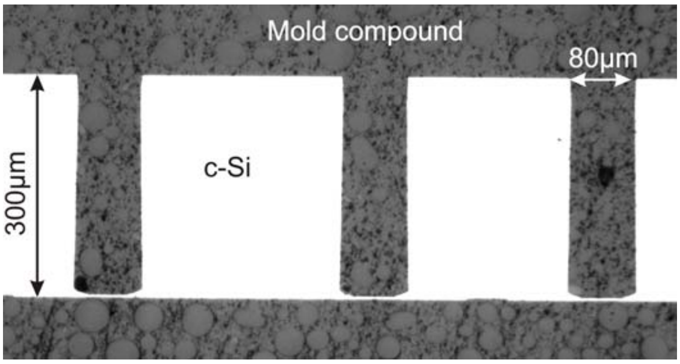


Figure 5.12: TSV filled with mold compound.

5.3 TSV in a mass flow sensor

An TSV integration inside a mass flow sensor from the Fraunhofer ISiT is also targeted in order to improve the system reliability. Chapter 3.2.2 shows the pad-cell used in this MEMS. A silicon dioxide layer is deposited underneath the metallization layers (TiN, Ti, TiN). This SiO layer must removed for a TSV integration in this device. The process required is the same compared to the previous described PMD etching 4.1.2 and was characterized as a critical process step due to reliability issues. Thus, a redistribution of the metallization like shown in figure 5.13 is preferred for a TSV implementation, because the the oxides are removed from the wafer front-side before the TSV are formed. The processes required for this etching are standard in all MEMS or CMOS fabrication facilities.

Figure 5.13: Redistribution of the metallization in a MEMS devices for TSV integration.

The further proposed process flow for a TSV integration inside a mass flow sensor is similar to the earlier presented flow inside the test design. KOH etching of the required membrane is an additional process step after TSV formation. Thus, the deposited materials must show a high selectivity to KOH. Figure 5.14 shows the schemata of the MAF with integrated

TSV. The next process step is the membrane formation by using KOH.

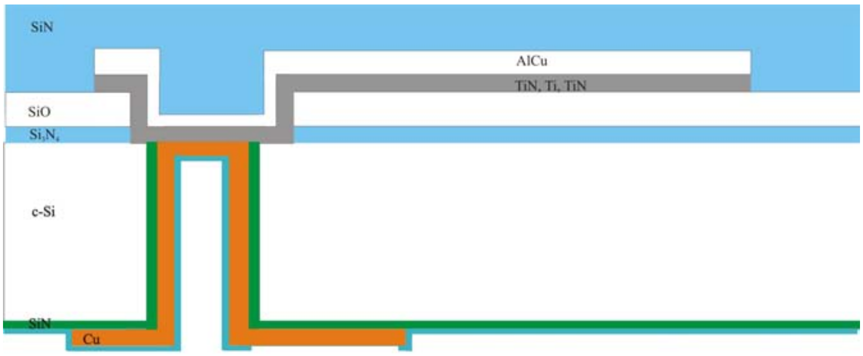


Figure 5.14: Mass flow sensor with integrated TSV before membrane formation by using KOH.

6 Summary and Outlook

Through Silicon Vias (TSV) are a key technology for the realization of miniaturized electronic devices in the near future. A signal redistribution from the wafer front-side pad to the wafer-backside is the basic idea of TSV. This allows a 3D stacking of electronic devices directly on top of each other. The electrical path between two devices is achieved by the TSV metallization, a back-side redistribution and an electric conductive bonding between these wafers. The foot print of this system configuration is much smaller compared to conventional packages based on the wire bond technology. Current TSV research or commercial activities a mainly driven by CMOS devices. Imaging sensors or memories with integrated TSV are prevalent on the market. MEMS packages can also benefit from implementing TSV. The functionality of the device will be improved. For instance, a separation of the measurement and connection area is possible by a TSV integration in mass flow sensors. This allows flow measurements in harsh environments. The challenges of a TSV integration in MEMS packages is not comparable to TSV in CMOS wafer. TSV for CMOS devices are integrated in 50μm to 100μm thick wafer which implies a wafer thinning during the TSV production. This wafer thinning is not possible for MEMS due to their stress sensitivity. Thus, the TSV fabrication technologies are different for MEMS and CMOS devices. The major challenge is the development of etching, deposition and pattern transfer processes in thick ($>$300μm) wafer.

This work has taken up these challenges and has shown technologies for TSV in wafer with thicknesses $>$300μm. First, FEM simulations have shown that an external load up to 4N can be applied to wafers with and without TSV before the flexural strength is achieved. A wafer handling with wafer thicknesses $>$300μm and integrated TSV is therefore possible without a significant yield loss. In addition, this stability allows a TSV fabrication without using carrier wafers which are mandatory and imply extra process steps in several other TSV approaches.

The front-side pad-cell passivation is a critical step regarding reliability issues during TSV processing. Critical stresses can arise in this passivation layer during temperature excursions up to 400°C or applied pressures up to 6MPa. However, calculation of the pad-cell displacement during TSV processing has not shown a significant risk to maintain hermetic TSV. This calculation is in a good agreement with the experiments.

The TSV hole formation is obtained by a deep reactive ion etching process. Vertical holes were formed with an etch rate of approximately 5μm per minute. The process was optimized in such a way that a notching of 3μm to 5μm occurred. Two different technologies were evaluated to remove pre-metal dielectrics (PMD) in a hole depth of $>$300μm. Gas phase etching (GPE) showed the possibility of etching these layers completely whenever a large under-cut was observed. PMD etching by using a buffered oxide etchant removed the PMD and the Ti underneath the 1^{st} level metallization. This isotropic etch process has not shown any under-cut. It can be concluded that the flow dynamics of etchants inside the TSV geometry influences the etch mechanism at the TSV bottom.
Isolation layers are required in all TSV in order to prevent crosstalking between two TSV or other functional elements of the device. The hot wire chemical vapor deposition (HW-CVD) and the plasma enhanced chemical vapor deposition (PE-CVD) techniques were evaluated to obtain a-Si_xN_y:H films. Getting a pin-hole free layer inside the TSV hole was possible by using both technologies. The dielectric strength of both films was measured on planar substrates whereas different surface roughness was used in order to simulate surface irregularities inside the TSV caused by the DRIE process. The a-Si_xN_y:H obtained by HW-CVD showed a value in the order of 3MV/cm. This lower value compared to results measured by PE-CVD films ($>$10MV/cm) can be explained by surface contaminations on the wafer surface during the deposition. The HW-CVD deposition chamber used is not located in a clean room. Higher dielectric strength values for a-Si_xN_y:H deposited by using HW-CVD can be predicted in a stringent deposition environment. The a-Si_xN_y:H film deposited by PE-CVD showed a better step coverage inside the TSV hole. However, a-Si_xN_y:H films obtained from both techniques allow their usage as isolation layers in TSV application with wafer thicknesses $>$300μm.
The a-Si_xN_y:H was also deposited on the TSV hole bottom. This film must be selectively removed at the hole bottom in order to allow an electrical connection between the TSV and the 1st level metallization. Isolation material deposited on the sidewalls must be stable in terms of a pin-hole free film after this etch process. A highly anisotropic etch process was developed in this work based on the DRIE technology. The a-Si_xN_y:H deposited film showed a KOH stability for over 1h after the a-Si_xN_y:H was etched at the TSV hole bottom. This KOH test implies that the films are pin-hole free.
Electrical signals must be transferred from the wafer front-side pad to the electrical back-side by metallic films. Two different techniques were evaluated. Ti, Al and Cu were deposited by the gas flow sputtering technique. It was possible to deposit material to the hole bottom, which is not common for physical vapor deposition techniques. However, films deposited by using this technique showed a high porosity and therefore a too high

electrical resistance. In addition, TiN and Cu were deposited by using the metal organic chemical vapor deposition (MO-CVD) technique. This layer stack (TiN, Cu) was previously evaluated as a possible metallization scheme which fulfills the required adhesion, diffusion and electrical conductivity properties in TSV. A step coverage close to one was obtained for both materials in the given TSV geometry. An electrical TSV resistance of $32\text{m}\Omega \pm 8\text{m}\Omega$ was measured for a 300μm thick wafer by using a 1μm thick Cu ring metallization. This value is sufficient for the targeted MEMS packages at the Fraunhofer ISIT. In addition, a smoothing of surface irregularities inside TSV hole was observed during Cu deposition by using the MO-CVD technique. This effect is explained by a higher nucleation rate inside the surface irregularities caused by longer residence time of the molecules at these surface sites.

A redistribution layer on the wafer back-side must be formed in order to allow a 3D stacking. A conformal photoresist deposition onto the TSV hole sidewalls is hard to achieve with common resist deposition techniques. A dry photoresist foil process was developed in this work. A photosensitive foil was laminated onto the wafer back-side and it protected successfully the TSV holes during the following Cu etching. In addition, photolithography processes required were developed and showed a full post-CMOS and MEMS compatibility. This lamination technique is so far not a common technique in MEMS or CMOS fabrication facilities and should be considered as a useful complementary technique.

The key technologies developed in this work allow a TSV integration in hermetic dense MEMS packages. A process flow was presented. It involved additional challenges for a TSV integration inside ASICs and MEMS with wafer thicknesses $>300\mu$m.

This thesis showed first steps for a realization of TSV in MEMS packages. The reliability of the TSV developed must be shown in further electrical measurements. The TSV reproducibility on the entire wafer, from wafer to wafer and from run to run has to be evaluated and optimized before a TSV integration inside commercial MEMS products can be targeted.

The isolation deposition processes showed sufficient step coverages for MEMS packages based on 6“ wafer. A critical film thickness of this layer can be predicted for a TSV integration inside a full thickness 8“ wafer in respect to the pin hole density and the film thickness gradient. A new technique must be found in order to fulfill the requirement to deposit an isolation layer inside the TSV structure by using low temperature ($<450°$C) process.

TSV are mandatory to satisfy the high request of an integration of more functionality in one device whereas the device size should remain constant or even decrease. A 3D stacking of MEMS and logic devices is possible with this technique and reduces the required foot print significantly. The development of TSV technologies in wafers with the uncommon thickness of $>300\mu$m is required for MEMS. This work produced a view of TSV requirements and possible process technologies in order to develop TSV for MEMS packages.

7 Appendices

A Capacitance as a function of the isolation thickness gradient (linear decay)

The capacitance of a ring geometry is given by Equation (3.6)

$$C(x) = \int \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\ln \frac{r_{out}}{r(x)}} dx$$

This equation changes

$$C(x) = \int \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\ln \frac{r_{out}}{\frac{\Delta d}{L} \cdot x + d_0}} dx$$

if a a linear film thickness gradient of the isolation material inside the TSV is assumed. Δd, d_0, L are the isolation film thickness gradient, the starting isolation film thickness at the TSV entrance at $x = 0$ and the TSV depth, respectively. An analytical solution of the given equation is not possible. The term

$$f(x) = \ln \left(\frac{\Delta d}{L} \cdot x + d_0 \right)$$

developed by a Taylor series of the second order at the position $x_0 = 0$ results to

$$f(x) = \ln (d_0) + \frac{\Delta d}{d_0 \cdot L} \cdot x + \left(\frac{\Delta d}{d_0 \cdot L} \right)^2 \cdot x^2 + R(x)$$

Putting the solution of the Taylor series in given capacitance function results to

$$C(x) = \int \frac{2 \cdot \pi \cdot \epsilon \cdot L}{\lambda + \nu \cdot x + \gamma \cdot x^2} dx$$

with

$$\begin{aligned} \lambda &= \ln \left(\frac{r_{out}}{d_0} \right) \\ \nu &= -\frac{\Delta d}{d_0 \cdot L} \\ \gamma &= \nu^2 \end{aligned}$$

The integral can be solved analytically [83] and results to

$$C(x) = \begin{cases} \frac{2}{\sqrt{\Theta}} \cdot \arctan\left(\frac{2\cdot\gamma\cdot x+\nu-2\cdot\gamma}{\sqrt{\Theta}}\right)\Bigg|_{x=x_0}^{x=L} & \text{for } \Theta > 0 \\ \frac{1}{\sqrt{|\Theta|}} \ln\left|\frac{2\cdot\gamma\cdot x+\nu-2\cdot\gamma-\sqrt{|\Theta|}}{2\cdot\gamma\cdot x+\nu-2\cdot\gamma+\sqrt{|\Theta|}}\right|\Bigg|_{x=x_0}^{x=L} & \text{for } \Theta < 0 \end{cases}$$

where Θ is defined as

$$\Theta = 4 \cdot \gamma \cdot \lambda - \nu^2$$

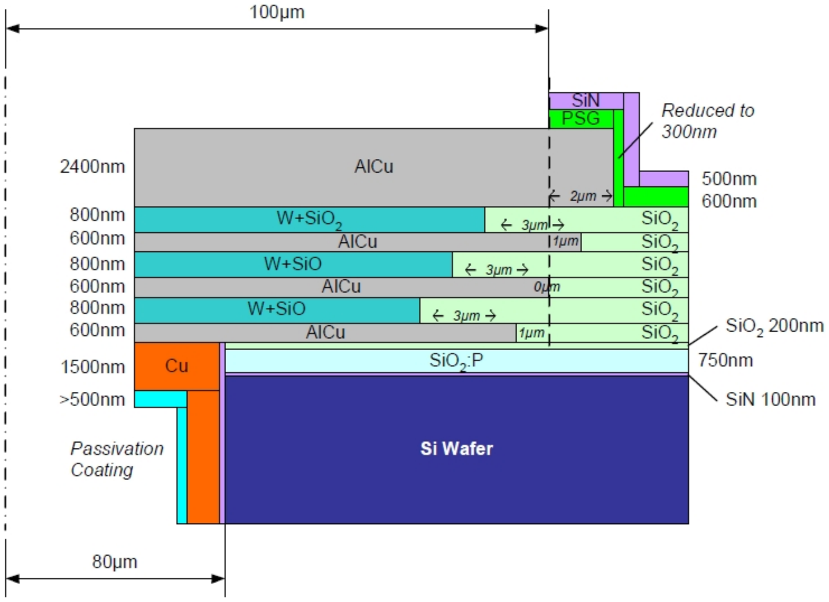
B Material Data

The following table shows material data used for thermomechanical calculations. The data is based on the personal data base of Friedel [42].

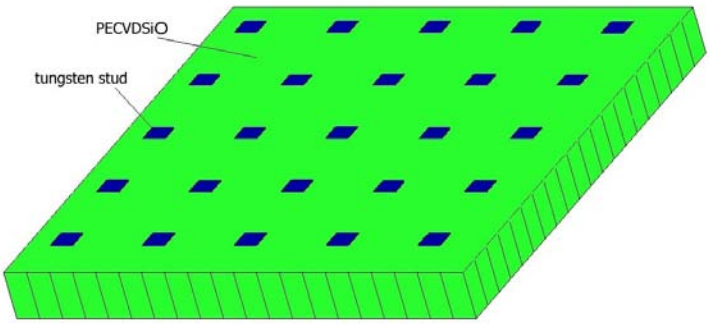
Material	Young modulus [GPa]	Poisson rate	CTE [ppm/K]	Thermal conductivity [W/mK]	Tensile (fracture) strength [MPa]	Fracture strain [MPa]
AlCu	90	0.33	24	130	340	0.6
PSG	150	0.21	5.0	1.6	(500)	0.07
LT SiO2	70	0.17	0.55	1.3	(500)	0.07
PECVD SiN	150	0.25	3.0	19	460	3.0
LPCVD SiN	100	0.27	3.0	30	(980)	3.0
Glass tungsten composite	148 (X, Y), 87 (Z)	0.18	1.57 (X, Y), 3.66 (Z)	1.50 (X, Y), 3.02 (Z)		
Si< 100 >	130	0.28	2.57 … 4.00	150…54	(200)	
Cu 99.9%	128	0.34	17	395…360	220	1.0
BCB	3	0.34	47	0.29	90	8.0

C Pad-cell model

Pad cell- and TSV geometries used during simulations. Film thickness values shown are taken as an example.



Model of an intermetallic dielectric layer. Tungsten plugs and isolation material are assumed as one composite. Material parameters of these composite are summarized in appendix B.



8 Published work

1. S.Warnat, N.Marenco, D.Kaehler, and W.Reinert. *Design rules for post-CMOS through silicon vias in an industrial environment.* 8th Electronic Packaging Technology Conference, pages 35–39, Singapore, |2006|. IEEE.

2. N.Marenco, S.Warnat, and W.Reinert. *Interconnect challenges in highly integrated MEMS.* ASIC subsystems, page 25, Stresa, |2007|. DTIP

3. S.Warnat, M.Hoefer, L.Schaefer, H.Foell, and P.Lange. *Low Temperature Silicon Nitride Films Deposited on 3D Topography by Hot Wire Chemical Vapor Deposition (HWCVD).* 2007 MRS Fall Meeting volume 1036, Boston, |2007|. Material Research Society.

4. N.Marenco, W.Reinert, and S.Warnat. *DAVID - a Strategic Research Project for Chip-Scale MEMS / ASIC Co-integration.*European Microelectronics and Packaging Conference & Exhibition , Oulu, |2007|. IMAPS.

5. T. Falat, K. Friedel, N. Marenco and S. Warnat. *TSV constraints related to temperature excursion, pressure during molding, materials used and handling loads.* Microsystem Technologies, |2008|.

6. T. Kraft, K. Reiter, S. Warnat. *Praeparation von beschichteten Durchkontaktierungen an Siliziumwafern.* 42. Metallographie-Tagung mit Ausstellung, Jena, |2008|.DGM.

7. S.Warnat, R.Ecke, S.Gruenzig, N.Marenco, W.Reinert, and P.Lange. *Through Silicon Vias in Micro-Electro Mechanical Systems.* 2008 MRS Fall Meeting, Boston, |2008|. Material Research Society.

References

[1] G. E. Moore. Cramming more components onto integrated circuits. *Electronics*, 38(8), |1965|.

[2] G. E. Moore. Progress in Digital Integrated Circuits. In *International Electron Devices Meeting*, pages 11–13. IEEE, |1975|.

[3] Intel Corporation. Intel Demonstrates Industry's First 32nm Chip and Next-Generation Nehalem Microprocessor Architecture, http://www.intel.com/pressroom, |last acess June 2009|.

[4] Scott E. Thompson and Srivatsan Parthasarathy. Moore's law: the future of Si microelectronics. *Materials Today*, 9(6):20–25, |2006|.

[5] G.E. Moore. No Exponential Is Forever: But Forever Can Be Delayed! In *IEEE Solid-State Circuits Society*, |2003|.

[6] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat. 3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. *Proceedings of the IEEE*, 89(5):602–633, |2001|.

[7] Infineion Technologies AG. Infineon leverages Multi-Gate Technology to achieve breakthrough results - New semiconductor structures significantly improve energy efficiency Three dimensions to success, |2006|.

[8] Samsung. Samsung Develops 3D Memory Package that Greatly Improves Performance Using Less Space, |2006|.

[9] N. Marenco, S. Warnat, and W. Reinert. Interconnect challenges in highly integrated MEMS. In *ASIC subsystems DTIP*, page 25, Stresa, |2007|.

[10] S. Warnat, N. Marenco, D. Kaehler, and W. Reinert. Design rules for post-CMOS through silicon vias in an industrial environment. In *8th Electronic Packaging Technology Conference*, volume One, pages 35–39, Singapore, |2006|. IEEE.

[11] Stefan Linder. *Chip Stacks for Memory Applications.* PhD thesis, ETH Zuerich, |1996|.

[12] P. Garrou, S. Vitkavage, and S. Arkalgud. Drivers for 3D Integration. In Garrou, P. and Bower, C. and Ramm, P., editor, *Handbook of 3D Integration*, pages 13–24. Wiley VCH, Weinheim, |2008|.

[13] Benedetto Vigna. More than Moore: micro-machined products enable new applications and open new markets. *ST Journal of Research*, 3(1), |2005|.

[14] S. Warnat, R. Ecke, S. Gruenzig, N. Marenco, W. Reinert, and P. Lange. Through Silicon Vias in Micro-Electro Mechanical Systems. In *MRS Fall 2008*, Boston, |2008|. MRS.

[15] P. Garrou and C. Bower. Overview of 3D Integration Process Technology. In Garrou, P. and Bower, C. and Ramm, P., editor, *Handbook of 3D Integration*, pages 25–44. Wiley VCH, Weinheim, |2008|.

[16] W. Kroeninger. Fabrication, Processing and Singulation of Thin Wafers. In Garrou, P. and Bower, C. and Ramm, P., editor, *Handbook of 3D Integration*, pages 175–208. Wiley VCH, Weinheim, |2008|.

[17] J.-P. Joly. Overview of Bonding Technologies for 3D Integration. In Garrou, P. and Bower, C. and Ramm, P., editor, *Handbook of 3D Integration*, pages 209–221. Wiley VCH, Weinheim, |2008|.

[18] P. Garrou. Commercial Activity. In Garrou, P. and Bower, C. and Ramm, P., editor, *Handbook of 3D Integration*, pages 271–287. Wiley VCH, Weinheim, |2008|.

[19] D. Shariff, N. Suthiwonsunthorn, and F. Bieck. Via interconnections for wafer level packaging: Impact of via shape on spray coating behavior. In *Electronics Packaging Technology Conference, 2006. EPTC '06. 8th*, pages 820–824, |2006|.

[20] http://www.tessera.com/technologies/imagingandoptics/imagesensorpackaging.aspx, |(last acess March 2008)|.

[21] C. Hammerschmidt. Stapelverfahren macht DRAM-Chips schneller und kleiner. http://www.eetimes.eu, |last acces June 2009|.

[22] P. Morrow, B. Black, M.J. Kobrinsky, S. Muthikumar, D. Nelson, C.-M. Park, and C. Webb. Design and Fabrication of 3D Microprocessors. In *2006 MRS Fall Meeting*, volume 970, Boston, |2006|. Material Research Society.

[23] J. Stockes. IBM goes vertical with chip interconnects. http://arstechnica.com, |last access June 2009|.

[24] P. Garrou. NXP Proposes Passive Integration in 3D IC Stacks, http://www.semiconductor.net, |last access June 2009|.

[25] M.M.V. Taklo, N. Lietaer, H.R. Tofteberg, T. Seppaenen, Prainsack J, J. Weber, and P. Ramm. 3D MEMS and IC integration. In *MRS Fall Meeting 2008*, volume 1112, Boston, |2008|. Material Research Society.

[26] M. Heschel, J. F. Kuhmann, S. Bouwstra, and I. Amskov. Stacking technology for a space constrained microsystem. In *The Eleventh Annual International Workshop on MEMS*, pages 312–317, |1998|.

[27] V. G. Kutchoukov, M. Shikida, J.R. Mollinger, and A. Bossche. Through-wafer interconnect technology for silicon. *Journal of Micromechanics and Microengineering*, 14:1029–1036, |2004|.

[28] Tomas Bauer. Standardized and Robust MEMS Foundry Processes Revolutionize Commercialization of MEMS. In *Semicon MEMS Forum*, Stuttgart, |2008|. Semi.

[29] Chiung-Wen Lin, Hsueh-An Yang, Wei Chung Wang, and Weileun Fang. Implementation of three-dimensional SOI-MEMS wafer-level packaging using through-wafer interconnections. *Journal of Micromechanics and Microengineering*, 17(6):1200–1205, |2007|.

[30] F. E. Rasmussen. *Electrical Interconnections Through CMOS Wafers*. PhD thesis, Technical University of Denmark, |2003|.

[31] P. Merz, W. Reinert, K. Reimer, and B. Wagner. PSM-X2: Polysilicon surface micromachining process platform for vacuum-packaged sensors. In *Mikrosystemtechnik Kongress*, Freiburg, |2005|. VDE Verlag.

[32] W. Reinert. *Neon Ultra-Feinlecktest zur Vorhersage der Vakuumerhaltung resonanter Mikrosensoren*. PhD thesis, Christian-Albrechts Universitaet zu Kiel, |2006|.

[33] N. Marenco. Downscaled Assembly Vertical Interconnect,www.david-project.eu, |last acces June 2009|.

[34] W. Gal, H. Fierkens, and H. Wensink. Wafer Level Packaging (WLP) by Transfer Molding . In *Smart System Integration*. VED-Verlag, |2009|.

[35] N. Marenco, W. Reinert, and S. Warnat. DAVID - a Strategic Research Project for Chip-Scale MEMS / ASIC Co-integration. In *European Microelectronics and Packaging Conference & Exhibition* , Oulu, |2007|. iMAPS.

[36] Massimiliano Melani, Lorenzo Bertini, Marco De Marinis, Peter Lange, Francesco D'Ascoli, and Luca Fanucci. Hot wire anemometric MEMS sensor for water flow monitoring, |2008|.

[37] P. Dixit, Xu Luhua, Miao Jianmin, John, H. L. Pang, D. Witarsa, P. Lim, P. Backus, and R. Preisser. Mechanical and microstructure characterization of high aspect ratio electroplated through-wafer copper interconnects. In *Electronics Packaging Technology Conference, 2006. EPTC '06. 8th*, pages 29–34, |2006|.

[38] K. Kohlmann von Platen. Fraunhofer ISIT Internal Report, |2006|.

[39] Tomasz Falat, Kazimierz Friedel, Norman Marenco, and Stephan Warnat. TSV constraints related to temperature excursion, pressure during molding, materials used and handling loads. *Microsystem Technologies*, |2008|.

[40] M. Pecht et al. *Electronic Packaging, Materials and Their Properties*. CRC Press, Washington D.C., |1999|.

[41] G. Coletti, C.J.J Tool, and L.J. Geerligs. Mechanical strength of silicon wafers and its modeling. In *15th Workshop of Crystalline Silicon Solar Cells and Modules*, Vail Colrado, |2005|.

[42] K. Friedel. Personal communication., |2007|.

[43] S.M Sze. *Semiconductor Devices Physics and Technology*. John Wiley & Sons, Inc., |1985|.

[44] Ui-Hui Kwon and Won-Jong Lee. Three-dimensional deposition topography simulation based on new combinations of flux distribution and surface representation algorithms. *Thin Solid Films*, 445(1):80–89, |2003|.

[45] J.D. Plummer, M.D. Deal, and P.B. Griffin. *Silicon VLSI Technology.* Prentice Hall, Inc, Upper Saddle River,, |2000|.

[46] Hideki Matsumura. Summary of research in NEDO Cat-CVD project in Japan. *Thin Solid Films*, 395(1-2):1–11, |2001|.

[47] A. G. Papathanasiou and A. G. Boudouvis. Manifestation of the connection between dielectric breakdown strength and contact angle saturation in electrowetting. *Applied Physics Letters*, 86(16):164102–3, |2005|.

[48] E. Bar, J. Lorenz, and H. Ryssel. 3D simulation of sputter deposition of titanium layers in contact holes with high aspect ratios. *Microelectronic Engineering*, 37-38:389–395, |1997|.

[49] Kirt R. Williams and Richard S Muller. Etch Rates for Micromachining Processing. *Journal of Microelectromechanical Systems*, 5(4):256–269, |1996|.

[50] J. W. Coburn and H. F. Winters. Plasma etching - a discussion of mechanisms. *Solid State and Materials Sciences*, 10(2):119–141, |1981|.

[51] F. Laermer and A. Schilp. Method Of Anisotropically Etching Silicon. US Patent 5,501,893:6, |1996|.

[52] M.J. Madou. *Fundamentals of Microfabrication.* CRC Press LLC, USA, |2002|.

[53] F. Roozeboom, M.A. Blauw, Y. Lamy, E. van Grunsven, W. Dekkers, J. F. Verhoeven, E. van den Heuvel, E. van der Drift, E. Kessels, and R. van de Sanden. Deep Reactive Ion Etching of Through Silicon Vias. In Garrou, P. and Bower, C. and Ramm, P., editor, *Handbook of 3D Integration*, pages 45–91. Wiley VCH, Weinheim, |2008|.

[54] A. Witvrouw, B. Du Bois, P. De Moor, A. Verbist, C. van Hoof, H. Bender, and K. Baert. A comparison between wet HF etching and vapor HF etching for sacrificial oxide removal, www.primaxxinc.com, |last acces June 2009|.

[55] Chun Su Lee, Jong Tae Baek, Hyung Joun Yoo, and Seong Ihl Woo. Modeling and Characterization of Gas-Phase Etching of Thermal Oxide and TEOS Oxide Using Anhydrous HF and CH_3OH. *Journal of the Electrochemical Society*, 143(3):1099–1103, |1996|.

[56] W. W. Mullins. Theory of Thermal Grooving. *Journal of Applied Physics*, 28(3):333–339, |1957|.

[57] William W. Mullins. Flattening of a Nearly Plane Solid Surface due to Capillarity. *Journal of Applied Physics*, 30(1):77–83, |1959|.

[58] Arthur Sherman. *Chemical vapor deposition for microelectronics*. Noyes Publications, New Jersey, |1987|.

[59] H. Wiesmann, A. K. Ghosh, T. McMahon, and Myron Strongin. a-Si : H produced by high-temperature thermal decomposition of silane. *Journal of Applied Physics*, 50(5):3752–3754, |1979|.

[60] Hideki Matsumura and Hiroyuki Tachibana. Amorphous silicon produced by a new thermal chemical vapor deposition method using intermediate species SiF[sub 2]. *Applied Physics Letters*, 47(8):833–835, |1985|.

[61] Alan Gallagher. Some physics and chemistry of hot-wire deposition. *Thin Solid Films*, 395(1-2):25–28, |2001|.

[62] H. D. Goldbach, C. H. M. van der Werf, J. Loffler, A. Scarfo, A. M. C. Kylner, B. Stannowski, W. M. ArnoldBik, A. Weeber, H. Rieffe, W. J. Soppe, J. K. Rath, and R. E. I. Schropp. Hot-wire chemical vapor deposition of silicon nitride for multicrystalline silicon solar cells. In *Photovoltaic Specialists Conference*, pages 1249–1252. IEEE, |2005|.

[63] J. Doyle, R. Robertson, G. H. Lin, M. Z. He, and A. Gallagher. Production of high-quality amorphous silicon films by evaporative silane surface decomposition. *Journal of Applied Physics*, 64(6):3215–3223, |1988|.

[64] Shinya Tange, Keisuke Inoue, Kenichi Tonokura, and Mitsuo Koshi. Catalytic decomposition of SiH4 on a hot filament. *Thin Solid Films*, 395(1-2):42–46, |2001|.

[65] V. Verlaan, Z. S. Houweling, K. van der Warf, H. D. Goldbach, and R. Schropp. Reaction Mechanism for Deposition of Silicon Nitride by Hot-Wire CVD with Ultra High Deposition Rate (<7nm/s). In *2006 MRS Spring Meeting*, volume 910, SanFrancisco, |2006|. Material Research Society.

[66] Hironobu Umemoto, Takashi Morimoto, Moroyuki Yamawaki, Yoshie Masuda, Atsushi Masuda, and Hideki Matsumura. Deposition chemistry in the Cat-CVD processes of the SiH4/NH3 system. *Thin Solid Films*, 430(1-2):24–27, |2003|.

[67] Samadhan B. Patil, Alka Kumbhar, Parag Waghmare, V. Ramgopal Rao, and R. O. Dusane. Low temperature silicon nitride deposited by Cat-CVD for deep sub-micron metal-oxide-semiconductor devices. *Thin Solid Films*, 395(1-2):270–274, |2001|.

[68] S. Warnat, M. Hoefer, L. Schaefer, H. Foell, and P. Lange. Low Temperature Silicon Nitride Films Deposited on 3D Topography by Hot Wire Chemical Vapor Deposition (HWCVD). In *MRS Fall Meeting 2007*, volume 1036, Boston, |2007|. MaterialResearch Society.

[69] P. Lange. Evidence for disorder-induced vibrational mode coupling in thin amorphous SiO2 films. *Journal of Applied Physics*, 66(1):201, |1989|.

[70] D. V. Tsu, G. Lucovsky, and M. J. Mantini. Local atomic structure in thin films of silicon nitride and silicon diimide produced by remote plasma-enhanced chemical-vapor deposition. *Physical Review B*, 33(10):7069, |1986|.

[71] C.M.M. Denisse, K.Z. Troost, F.M.P.M. Habraken, W.F. van der Weg, and M. Hendriks. Annealing of plasma silicon oxynitride films . *Journal of Applied Physics*, 60(7):2543, |1986|.

[72] M. Ohring. *Materials Science of Thin Films.* Academic Press, San Diego, 2 edition, |2002|.

[73] F. Paschen. Bohrs Heliumlinien. *Annalen der Physik*, 355(16):901–940, |1916|.

[74] H. Jacobsen. *Integration von piezoelektrischen Duennschichen in einen MEMS kompatiblen Prozessalauf auf Waferebene.* PhD thesis, Christian-Albrechts-Universitaet zu Kiel, |2007|.

[75] Th Jung, T. Kalber, and V. v d Heide. Gas flow sputtering of oxide coatings: practical aspects of the process. *Surface and Coatings Technology*, 86-87(Part 1):218–224, |1996|.

[76] J A Thornton. High Rate Thick Film Growth. *Annual Review of Materials Science*, 7(1):239–260, |1977|.

[77] D. L. Smith. *Thin-film Deposition: principal and practice.* McGraw-Hill, Boston, |1995|.

[78] Pascal Doppelt. Why is coordination chemistry stretching the limits of microelectronics technology? *Coordination Chemistry Reviews*, 178-180(Part 2):1785–1809, |1998|.

[79] S. Riedel. *Untersuchung zur Integration von MOCVD-Titannitridbarriere- und Kupferschichtern in Leitbahnsystemen der Mikroelektrinik*. PhD thesis, Technische Universitaet Chemnitz, |2003|.

[80] Stephen M. Gates. Surface Chemistry in the Chemical Vapor Deposition of Electronic Materials. *Chemical Reviews*, 96(4):1519–1532, |1996|.

[81] S. Nguyen, D. Dobuzinski, D. Harmon, R. Gleason, and S. Fridmann. Reaction Mechanisms of Plasma- and Thermal-Assisted Chemical Vapor Deposition of Tetraethylorthosilicate Oxide Films. *Journal of Electrochemical Society*, 137(7):2209–2215, |1990|.

[82] N.P. Pham, E. Boellard, P. M. Sarro, and J. N. Burghartz. Spin, Spray and Eloctroplating of Photoresist for MEMS Structures: A Comparison. In *SAFE* , pages 81–86, Veldhoven, |2002|.

[83] L. Papula. *Mathematische Formelsammlung*, volume 5. Auflage. Vieweg & Sohn Verlagsgesellschaft mbH, Braunschweig / Wiesbaden, |1998|.

Acknowledgment

I received assistance and advice from many friends and colleagues during work on this thesis. In particular I would like to acknowledge the following people.

I thank my „Doktorvater“ Prof. Dr. Helmut Föll for his lively interest in my work, even though I did my outside his group. He and his group gave me always the feeling that I was a part of this group - Thank you! It was good to get remarks regarding my work from scientists, who were not familiar with semiconductor technologies. In addition, I thank Prof. Dr. Föll also for his time to be the 1^{st} reviewer of this thesis. I thank Prof. Dr. Wagner in the same way. He showed a high interest of my results and asked the right questions. I thank him also for his acceptance to work as the 2^{nd} reviewer.

Most importantly, I thank my mentor Dr. Peter Lange for his guidance and many creative ideas. I also thank him for pushing me in my scientific work, which greatly improved the quality of the work in this thesis and made me a better scientist. I also enjoyed his knowledge of history and politics of the last century, especially during the MRS conference in Boston!

I was a member of the Module Integration Group at the Fraunhofer Institute for Silicon Technology during my thesis work. I thank the head of this group, Karin Pape, for her continuous support in all financial matters. In addition, her social competence helped me a lot during my familiar up and downs during the last four years. Norman Marenco helped me with administrative problems and I liked his critical questions. I also thank Dr. Wolfgang Reinert who had the idea for this thesis. I thank the entire ISIT team for their outstanding support.

I performed some work at other Fraunhofer Institutes. I thank Dr. Ramona Ecke, Dr. Lothar Schaefer, Dr. Thomas Jung, Dr. Markus Hoefer and Dr. Kai Ortner for the great collaborations and conversations during my experiments in their laboratories.