

# **Active Thermal Control of Power Electronic Modules in Smart Transformer Applications**

**Dissertation**

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# Erklärung

Ich erkläre an Eides statt, dass ich die Dissertation zum Thema:

*Active Thermal Control of Power Electronic Modules in Smart Transformer Applications*

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## Deutsch Kurzfassung der Arbeit

Durch den Ausbau der regenerativen Energien unterliegt das elektrische Netz einem Wandel von zentralisierten Kraftwerken hin zu vielen dezentralen Energieerzeugern. Im Rahmen dieser Transformation ist der Smart Transformer (ST) eine mögliche Lösung, um intelligente Knotenpunkte im Netz zu bilden, die für das Netzmanagement verwendet werden können und um die Netzintegration von mehr erneuerbaren Energieerzeugern zu ermöglichen.

Ein Problem für die Anwendung von STs ist die erwartete geringere Zuverlässigkeit im Vergleich zum traditionellen Transformator. Um dieses Problem zu bearbeiten, werden die Themen Energietechnik, Leistungselektronik und Zuverlässigkeit in dieser Arbeit kombiniert. Dem "Physics of Failure" Ansatz folgend, werden die am häufigsten ausfallenden Komponenten identifiziert, ihr Lastprofil im elektrischen Verteilnetz analysiert und schließlich Lösungen entwickelt, um die Zuverlässigkeit zu erhöhen.

Die Leistungshalbleiter werden als häufig ausfallende Komponente identifiziert und darauf basierend rezensiert diese Arbeit die Fehlermechanismen. Die meisten Fehlermechanismen basieren auf thermischen Zyklen, weshalb für ein typisches Lastprofil im elektrischen Netz der thermische Stress eines dreistufigen STs analysiert wird. Darauf basierend wird ein thermischer de-rating Algorithmus entwickelt mit dem Ziel die Leistungshalbleiter für die erwartete Lebensdauer minimal auszulegen.

Als Möglichkeit um die Zuverlässigkeit zu erhöhen, wird aktive thermische Regelung eingeführt, welche auf Basis von Software den thermischen Stress der Bauelemente im Betrieb reduziert. Die existierenden Ansätze für aktive thermische Regelung werden rezensiert und unterteilt in die Regelung der Leistungshalbleiterverluste, sowie die Regelung der Belastung. Für die kostengünstige Ermittlung der Temperatur wird ein Schätzer entworfen und validiert. Ein Algorithmus, der das Lastprofil zur Reduzierung der thermischen Belastung verändert, wird anhand eines Maximum Power Point Tracking Algorithmus für Photovoltaikanwendungen entwickelt und analysiert.

Für die Erhöhung der Zuverlässigkeit durch die Regelung der Verluste werden jeweils ein Algorithmus für hart schaltende Leistungshalbleiter und ein Algorithmus für resonant schaltende Leistungshalbleiter entwickelt und validiert. Beide Algorithmen basieren lediglich auf den elektrischen Messungen und benötigen keine Temperatursensoren. Der Algorithmus für hart schaltende Leistungshalbleiter verwendet die Schaltfrequenz, um die Chiptemperatur zu beeinflussen, während der zweite Algorithmus die Einschaltzeiten der Leistungshalbleiter derart manipuliert, dass die Verluste erhöht werden können.

Die Regelung der thermischen Belastung einzelner modularer Zellen in einem modularen Stromrichter wird eingeführt. Dabei wird die interne Steuerung des Energieflusses für seriell oder parallel verbundenen Zellen jeweils analytisch untersucht und mit Labormessungen demonstriert. Der Einfluss der thermischen Regelung auf die Belastung der einzelnen Zellen wird für parallel verbundene, seriell verbundene und über einen Mittelfrequenztransformator verbundene Zellen in einem modularen Stromrichter demonstriert.

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## English Summary

The increase of renewable energies affects a paradigm change in the electric grid from centralized power plants to many decentralized energy producers. Within this change, the Smart Transformer (ST) is a possible solution to obtain intelligent nodes in the electrical grid, which can be used for the grid management and increase the capacity for the integration of renewable energy sources.

A problem for the application of the ST in the distribution grid is the expected lower reliability in comparison with the traditional transformer. To address this problem, the knowledge of power system, power electronics and reliability is combined in this work. Following the "Physics of failure" approach, the most frequently failing components are identified, their load profile in the electrical distribution grid is analyzed and finally solutions are developed to improve the reliability.

The power semiconductors are found to be the most prone to fail components and most of their failure mechanisms are found to be affected by thermal cycling. For this reason, thermal stress analysis is performed for the three-stage ST. Based on this, a thermal de-rating strategy is proposed to minimize the size of the power semiconductors for a specific lifetime target.

As an opportunity to increase the reliability, active thermal control is introduced, which is a software based solution for the reduction of the thermal stress during operation. The existing approaches from literature are reviewed and categorized into control of the power converter losses and the control of the device loading. For a cost-effective mitigation of the junction temperature, an estimator is designed and validated. As an example for active thermal control by means of the device loading, a Maximum Power Point Tracking algorithm for photovoltaic applications is developed.

For increasing the reliability by control of the power converter losses, one algorithm is introduced and validated for hard switching power converters and one algorithm is introduced for soft switching power semiconductors. Both algorithms are only based on electrical measurements and do not require temperature sensors. The algorithm for hard switching power semiconductors changes the switching frequency for controlling the junction temperature fluctuations and thus the thermal stress. Instead, the algorithm for soft switching power semiconductors controls the duty cycles of the DC/DC converter for the control of the losses.

Controlling the thermal stress of modular building blocks in a modular power converter, referring to power routing, is proposed. The capability of the algorithm is investigated analytically for series connected and parallel connected modular building blocks. For the validation, the influence of the power routing on the loading of the single cell is demonstrated experimentally for series connected, parallel connected and medium frequency transformer coupled cells in modular power converters.

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## Used symbols and abbreviations

### General symbols

#### General symbols

$u(t), u$  Instantaneous value

#### Superscripts

\* Reference value  
*AC* Alternating current/voltage  
*DC* Direct current/voltage  
*LV* Low voltage  
*MV* Medium voltage

#### Subscripts

dc DC-link related  
 D Diode related  
 jc Junction to case  
 max Maximum value  
 min Minimum value  
 MPPT Maximum power point tracking related  
 off Turn off  
 on Turn on  
 T IGBT related  
 th thermal  
 i Index for representing the stress ranges  
 p Primary side related  
 s Secondary side related

### Special symbols

$A$  Consumed lifetime of a QAB  
 $a_1$  Constant of the lifetime model of an IGBT  
 $A_1$  Consumed lifetime of QAB 1  
 $a_3$  fitted parameter of the lifetime model of an IGBT

$a_4$	Fitted parameter in the lifetime model of an IGBT
$a_5$	Fitted parameter in the lifetime model of an IGBT
$a_6$	Fitted parameter in the lifetime model of an IGBT
$A_{a1}$	Consumed lifetime of port a of the QAB 1
$A_{b1}$	Consumed lifetime of port b of the QAB 1
$A_{c1}$	Consumed lifetime of port c of the QAB 1
$A_{d1}$	Consumed lifetime of port d of the QAB 1
$\beta$	Fitting parameter for the failure probability
$B_x$	Expected lifetime for the failure probability $x$
$\gamma$	Thermal design scaling factor
$c$	Accumulated damage of a power semiconductor
$C$	Capacitance
$C^{MV}$	Capacitance of the MV CHB-converter
$C^{LV}$	Capacitance of the LV CHB-converter
$c_a$	Exponent of the acceleration factor
$c_d$	Accumulated damage
$C_f$	Capacitance of the LCL filter
$C_r$	Resonant tank capacitor of the SRC
$C_r$	Resonant tank capacitor of the SRC
$C_r$	Secondary side capacitance of the DAB/QAB
$C_p$	Primary side capacitance of the DAB/QAB
$C_{th}$	Thermal capacitance
$C_{th,n}$	n-th chain of the thermal capacitance
$CSPI$	Cooling system performance index
$\Delta f_{max}$	Maximum switching frequency (for $f_{sw}$ control)
$\Delta P_{max}$	Losses for which the switching frequency is maximized (for $f_{sw}$ control)
$\Delta T$	Magnitude of a thermal cycle
$\delta T_{j,max}$	Maximum junction temperature gradient
$\Delta T_{Op}$	Thermal cycles in the operating conditions
$\Delta T_{test}$	Number of thermal cycles to failure in the stress range $i$
$d$	Duty cycle
$d_{MPPT}$	Duty cycle in the MPPT
$\eta$	Efficiency
$E_{off}$	Turn off energy
$E_{on}$	Turn on energy
$E_{total}$	Total harvested energy
$\varphi$	Phase displacement between voltage and current
$\varphi_u$	Grid angle
$\phi$	Phase shift of an isolated DC/DC converter
$\phi_0$	Duty cycle reduction an isolated DC/DC converter
$F$	Failure probability
$f_0$	Fundamental frequency
$f_a$	Accelerating factor for accelerated lifetime tests



$f_g$	Fundamental frequency of the grid
$f_{min}$	Minimum switching frequency (for $f_{sw}$ control)
$f_s$	Sampling frequency
$f_{s,cam}$	Sampling frequency of the IR camera
$f_{sw}$	Switching frequency
$f_{sw,av}$	Mean value of the switching frequency (for $f_{sw}$ control)
$G_{th,jc}$	Transfer function between junction temperature and losses
$G_{PI}$	Transfer function of the PI controller
$i, I$	Current
$i^{MV}$	MV side current
$i_a^{DC}$	QAB current of port a in the low frequency model
$i_a^{out}$	QAB current of port a
$I_A$	Output current of cell A
$i_b^{DC}$	QAB current of port b in the low frequency model
$i_b^{out}$	QAB current of port b
$I_B$	Output current of cell B
$i_c^{DC}$	QAB current of port c in the low frequency model
$i_c^{out}$	QAB current of port c
$I_C$	Output current of cell C
$i_d$	d-component of the current in the rotating reference frame
$i_d^{DC}$	QAB current of port d in the low frequency model
$i_d^{out}$	QAB current of port d
$i_{grid}$	Grid current
$I_k$	Current of the PV array at the time k
$i_{ll}$	Current of the DAB during duty cycle control
$i_{laod}^{pk}$	Peak current (for $f_{sw}$ control)
$i_{lv}$	Load current of the DAB
$I_{MPPT}$	Current the MPPT
$I_{out}$	Output voltage
$I_{out,max}$	Maximum output current of one cell
$i_q$	q-component of the current in the rotating reference frame
$I_{ref}$	Reference current from datasheet for derivation of the losses
$I_{sc}$	Short circuit current of the PV array
$K_{I,off}$	Exponent for the current dependency of the turn off losses
$K_{I,on}$	Exponent for the current dependency of the turn on losses
$k_p$	Proportional gain
$K_{V,off}$	Exponent for the voltage dependency of the turn on losses
$K_{V,on}$	Exponent for the voltage dependency of the turn on losses
$L$	Inductance
$L_0$	Neutral line inductance
$L_1$	Inductance of the boost converter
$L_a, L_b, L_c, L_d$	Leakage inductance of the QAB
$L_f$	Filter inductance

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$L_{fc}$	Converter side inductance of the LCL filter
$L_{fg}$	Grid side inductance of the LCL filter
$L_{MV}$	Line inductor in MV grid
$L_n$	Leakage inductance of the DAB
$L_r$	Resonant tank inductance of the SRC
$m$	Modulation index
$M_{12}$	Coupled inductance
$m_{max}$	Maximum modulation index
$n$	Fitted parameter in the lifetime model of an IGBT
$N$	Number of thermal cycles
$n_i$	Number of thermal cycles in the stress range $i$
$N_i$	Number of thermal cycles to failure in the stress range $i$
$N_f$	Number of thermal cycles to failure
$n_p$	Number of parallel connected SCs
$n_s$	Number of series connected SCs
$n_{un}$	Number SCs to be unloaded
$\Theta$	Fitting parameter for the failure probability
$P_0$	Power rating
$P_1$	Power transfer of QAB 1
$P_{1,max}$	Maximum output power of one cell
$P_A$	Output power of cell A
$P_{a1}$	Power transfer for path a of the QAB 1
$P_B$	Output power of cell B
$P_{b1}$	Power transfer for path b of the QAB 1
$P_C$	Output power of cell C
$P_{c1}$	Power transfer for path c of the QAB 1
$P_{con}$	Turn on losses
$P_{d1}$	Power transfer for path d of the QAB 1
$P_{in}$	Input power
$P_k$	Power of the PV array at the time $k$
$P_{loss}$	Power semiconductor losses
$P_{loss,max}$	Maximum power semiconductor losses of the design
$P_{PV}$	Power of the PV power plant
$P_{PV,rel}$	Relative PV array irradiance
$P_{ST}$	Active power of the ST
$P_{sw,off}$	Turn off losses
$P_{sw,on}$	Turn on losses
$P_{out}$	Output power
$Q$	Reactive power
$Q_a$	Reactive power of the QAB
$Q_{ST}$	Reactive power of the ST
$R$	Resistance
$R_0$	Gain for the virtual resistors

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$r_{ce}$	Turn on resistance of an IGBT
$R_l$	Load resistance of the QAB
$R_{th}$	Thermal resistance
$R_{th,n}$	n-th chain of the thermal resistance
$R_v$	Virtual resistance for a full QAB
$R_{va}$	Virtual resistance for path a in the QAB
$R_{va1}$	Virtual resistance for path a in the QAB 1
$R_{v,A}$	Virtual resistor for path A (parallel power routing)
$R_{vb}$	Virtual resistance for path b in the QAB
$R_{vb1}$	Virtual resistance for path b in the QAB 1
$R_{v,B}$	Virtual resistor for path B (parallel power routing)
$R_{vc}$	Virtual resistance for path c in the QAB
$R_{vc1}$	Virtual resistance for path c in the QAB 1
$R_{v,C}$	Virtual resistor for path C (parallel power routing)
$R_{vd}$	Virtual resistance for path d in the QAB
$R_{vd1}$	Virtual resistance for path d in the QAB 1
$s$	Frequency domain
$t$	Time
$T$	Time period
$T_a$	Ambient temperature
$T_c$	Case temperature
$T_I$	Integrator time constant
$T_j$	Junction temperature
$T_{j,av}$	Mean value of the junction temperature during a thermal cycle
$P_{c,max}$	Maximum designed case temperature
$T_{j,D1}$	Junction temperature of diode D1
$T_{j,D2}$	Junction temperature of diode D2
$T_{j,est}$	Estimated junction temperature
$T_{j,esti}$	Junction temperature estimated with the $i^{th}$ order estimator
$T_{j,D1,LV}$	Junction temperature of one diode in the QAB on the LV side
$T_{j,D1,HV}$	Junction temperature of one diode in the QAB on the MV side
$T_{j,lim}$	Junction temperature limit after which the software based limitation begins
$T_{j,meas}$	Measured junction temperature
$T_{j,max}$	Maximum junction temperature
$t_{on}$	Turn-on time of an IGBT in a lifetime model for IGBTs
$T_s$	Sampling period
$T_{j,T1}$	Junction temperature of IGBT T1
$T_{j,T2}$	Junction temperature of IGBT T2
$T_{j,T1,LV}$	Junction temperature of one IGBT in the QAB on the LV side
$T_{j,T1,HV}$	Junction temperature of one IGBT in the QAB on the MV side
$T_{MPPT}$	Sampling period of the MPPT
$\tau$	Time constant of the low pass filter (for $f_{sw}$ control)
$\tau_1$	Time constant of the low pass filter (for duty cycle control)

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$\tau_2$	Time constant of the low pass filter (for duty cycle control)
$\tau_{th,v}$	v-th time constant of the thermal impedance
$v$	Voltage
$\nu$	Index
$V$	PV-array voltage
$V_1$	DC voltage for emulation of an IGBT in an MMC
$V_{1,out,max}$	Maximum output voltage of one cell
$V_{1,out,min}$	Maximum output voltage of one cell
$V_1^{LV}$	LV side DC-link 1
$V_1^{MV}$	MV side DC-link 1
$V_2^{LV}$	LV side DC-link 1
$V_2^{MV}$	MV side DC-link 2
$V_3^{MV}$	MV side DC-link 3
$V_4^{MV}$	MV side DC-link 4
$V_5^{MV}$	MV side DC-link 5
$V_6^{MV}$	MV side DC-link 6
$V_{grid}$	Grid voltage
$v_a$	High frequency output voltage of port a
$V_a^{DC}$	DC-voltage of the QAB port a
$V_a$	Output voltage of cell A
$v_b$	High frequency output voltage of port b
$V_b^{DC}$	DC-voltage of the QAB port b
$V_b$	Output voltage of cell B
$v_c$	High frequency output voltage of port c
$V_c^{DC}$	DC-voltage of the QAB port c
$V_c$	Output voltage of cell C
$v_d$	High frequency output voltage of port d
$V_d^{DC}$	DC-voltage of the QAB port d
$v_{ce}$	Collector emitter voltage
$v_{ce,0}$	Constant voltage drop on IGBT
$V_{dc}$	DC-link voltage
$V_g$	Grid voltage
$V_{MPPT}$	Voltage in the MPPT
$V_{oc}$	Open circuit voltage of the PV array
$V_{out}$	Output voltage
$v_p$	Primary side voltage
$V_{ref}$	Reference voltage form dataheet for derivation of the losses
$v_s$	Secondary side voltage
$V_{src}$	DC power supply for the QAB
$VS$	Heat sink volume
$x$	Failure probability
$x_3$	Increased power routing capability of the third harmonic in series connected building block
$x_{CHB}$	Number of CHB cells

$Z_1$	Line impedance in a MV grid
$Z_2$	Line impedance in a MV grid
$Z_{th,ch}$	Thermal impedance between case and heat sink
$Z_{th,jc}$	Thermal impedance between junction and case
$Z_{th,ha}$	Thermal impedance between heat sink and ambient

## Abbreviations

AC	Alternating Current
BESS	Battery Energy Storage System
CHB	Cascaded H-Bridge Converter
DAB	Dual Active Bridge
DC	Direct Current
EMI	Electromagnetic Interference
EOL	End Of Life
ESR	Equivalent Series Resistance
FEA	Finite Element Analysis
IGBT	Insulated-Gate Bipolar Transistor
LV	Low Voltage
LVAC	Low Voltage Alternating Current
LVDC	Low Voltage Direct Current
LVRT	Low Voltage Ride Through
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
NPC	Neutral Point Clamped
P&O	Perturb & Observe
PWM	Pulse Width Modulation
QAB	Quadruple Active Bridge
SC	Single Cells
Si	Silicon
SiC	Silicon Carbide
SRC	Series Resonant Converter
SST	Solid State Transformer
ST	Smart Transformer
TSEP	Thermo-Sensitive Electrical Parameters

# 1 Introduction

This section motivates a modular Smart Transformer (ST) in the distribution grid and formulates the research proposal of the thesis. The structure of the thesis is explained and the publications related to the different sections are highlighted.

## 1.1 Motivation for the ST

In many countries, the electrical distribution grid is evolving from a structure based on centralized power plants to distributed generation, mostly based on renewable energy sources. A challenge of these renewable energy sources is the time varying generation affected by the weather conditions. Thereby, the inertia of the centralized power plants was supporting the frequency stability of the grid, whereas the renewable sources do not have such an inertia [1]. Moreover, the power generation of the renewable energy sources can fluctuate in periods of several seconds, which requires them to be compensated by other sources. Consequently, the potential for this compensation needs to be available in a sufficient reserve. Beside the fast varying power injection, the demand and the generation are not synchronized, which results in a high variability of the grid utilization. Therefore, the utilization of the current grid capacity is challenged and the curtailment of renewable power plants during high production and low consumption is a common practice [2].

In the year 2016, already 30 % of electrical energy in Germany was produced by renewable energy sources and the target of the Energiewende is to increase the renewable energy production up to 40 – 45 % by 2025 and more than 80% in 2050 [3]. To enable such a high integration of renewable energy, it is not only mandatory to compensate the fast power fluctuations, e.g. with conventional power plants, but also to balance the time varying generation and the demand in the grid with sufficient dynamics. Energy storage systems are a potential solution for the balancing of the generation and the load demand, but they are decentralized systems itself and the control of the grid remains an open issue.

Microgrids are a potential solution for a decentralized grid, which can form an energy balancing unit and comprise distributed generation, energy storage and flexible loads [4]. It can be connected to the main grid and act like a single controllable entity or operate autonomously [5]. However, in many cases, the generation of renewable energies and the consumption of the loads are geographically distributed and the power needs to be transferred over long distances [6]. This may require the microgrid to be kept connected to the main grid for most of the time. Apart from the increase of electrical energy generated by renewables, the targeted electrification of the transportation poses further challenges. Fast charging stations for the vehicles are absorbing high power from the grid in relatively short time instants. The requested energy needs to be either provided directly by the microgrid or stored before it is charged into the batteries of the vehicle. When the energy should be provided by renewable energy in the microgrid, the fast charge of the vehicle is even more challenging for the grid. After all, this makes the management of the future grid and the balancing of the demand more

difficult compared to the grid with centralized power plants and is potentially a challenge in the microgrid concept.

A possible solution to improve the grid management is the ST, which is a power electronics based transformer. It is proposed to be installed as a part of the grid infrastructure for the interconnection between the medium voltage grid and the low voltage grid, where it can constitute intelligent nodes in the electrical distribution grid [7]. In comparison with the Solid State Transformer (SST), the ST is a power electronics based transformer with advanced control and communication capability. It can provide services to the grid, support the controllability of the grid and enables management of loads and generators in the grid [8]. The SST instead is focused on hardware aspects. In the ST based microgrid concept, the ST relies on the already available main grid and facilitates direct control of the energy storage systems with its communication infrastructure.

## 1.2 Motivation for the modularity of the ST

Beside the advantages of the ST based grid, the ST itself is opposed by increased costs, lower efficiency, shorter lifetime and expected lower reliability in comparison to the traditional transformer. To cope with these challenges, the maximization of the efficiency and the reduction of the costs is proposed to be addressed in the hardware design. The reliability is particularly important, because the ST is a series connected device in the grid, which is extremely important for the quality of service. In order to ensure the acceptance of this device in the electrical distribution grid, the reliability needs to be maximized for providing high quality of service.

A modular ST design based on low voltage power semiconductors is proposed to take advantage of the commonly good characteristics of the low voltage power semiconductors. The modular power converter enables to reduce the switching frequency for the single modular block and to use smaller output filters of the converter compared to non-modular power converters, which enables to increase the efficiency [9]. In addition, modular power converters obtain advantages like scalability in voltage and scalability in power, which enables an adaptation of the ST design to different locations in the grid.

The reliability of a system needs to be investigated based on a physics of failure approach, which means that every failure is traced back to its physical root cause. For power electronic converters, power semiconductors have been found to be among the most sensitive devices [10, 11]. Several failure mechanisms are caused by thermal cycling, which is why this work conducts thermal stress analysis for the different stages of the ST [12]. From this thermal stress analysis, the lifetime prediction can be made.

An opportunity to increase the reliability without additional costs for the hardware is active thermal control. Active thermal control uses software for reducing the thermal stress of a system by modifying its control variables with the goal to achieve a lifetime extension without hardware or design modifications. The concept of active thermal control was first

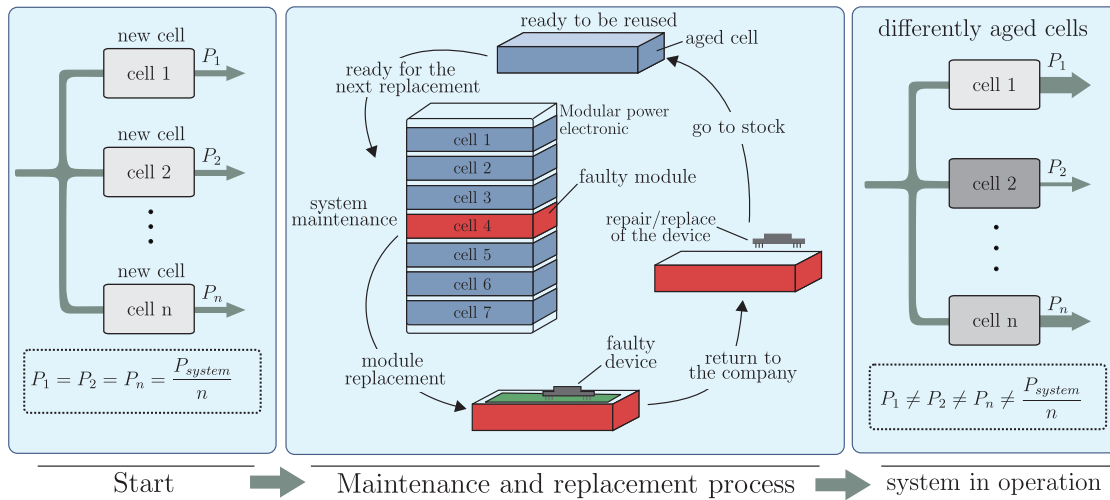


Figure 1.1: Concept of a modular repairable ST based on uneven cell loading and replacement of cells [15].

proposed from industry for electric drive motors during low speed and high torque, where the switching frequency was adapted to reduce the thermal stress in the fundamental period [13]. By using the proposed approach early failure were prevented, which was partially used for reducing the oversizing of the power semiconductors.

For the power electronics based ST in the distribution grid, the reliability of the system needs to be maximized to be competitive with the traditional transformer. This can be achieved by reducing the stress for sensitive components. An opportunity to reduce the stress for the power semiconductors is to apply active thermal control. Non-modular power converter can apply active thermal control only for the whole converter stage, whereas modular power converters make it possible to selectively control the stress for the different blocks, enabling to control their lifetime. Furthermore, the concept of fault tolerance can be applied on the cell level of the modular building blocks [14], whereas non-modular power converters need to apply it on the level of a full stage.

### 1.3 Motivation for power routing

A high reliability target for a long lifetime of a modular power converter requires an appropriate design of the whole system. However, even if the reliability of all components is maximized and the lifetime is controlled, it is expected, that there are components, which approach their end of life. In this case, the ST as a part of the infrastructure is not expected to be replaced by a new ST, but a repairable system based on the modular architecture is proposed as shown in Fig. 1.1. In this concept, the faulty cells need to be isolated and will be replaced without interrupting the operation of the system. The excluded cells will be maintained and can be used thereafter to replace other cells.

The concept of a repairable system impairs to schedule maintenance and to replace faulty components. In the grid with locally distributed STs, the maintenance is expected to be costly



and consequently, the time between the maintenance is targeted to be maximized. However, the failure of the components will occur in different instants and condition monitoring is proposed to obtain the information about the condition of the components in the different cells. This information can also be utilized to apply active thermal control for devices, whose time to the failure needs to be prolonged.

Modular power converters do not only enable to apply active thermal control to the single building block, but also to balance the loading among the building blocks. This can be achieved by applying active thermal control by uneven control of the cells, referring to as power routing [15]. It needs to be pointed out, that the described concept is applicable for modular power converters, whereas non-modular systems do not enable its application. Power routing is proposed to control the lifetime of the different cells in the overall system and therefore maximize the time to the next maintenance. This implies to unload devices, which are approaching their end of life and to load their power on devices with higher expected remaining lifetime.

## 1.4 Research proposal

The aim of this thesis is to investigate the reliability of an ST in the power system and to realize software based solutions for potential improvements. The reliability of the ST is analyzed based on the thermal stress for the power semiconductors in different conditions. Furthermore, as a solution for increasing the reliability, active thermal control algorithms are developed and implemented to reduce the thermal stress for the power semiconductors.

*Target I: Analysis of the thermal stress of the ST in the power system environment*

The first objective is to investigate the operation of the ST under consideration of the conditions in the power system in terms of thermal stress for the power semiconductors. This requires applying a physics of failure based approach, taking into account the typical operation conditions in the power system. The thermal stress at different power levels and different behavior of the loads and the electrical distribution grid is investigated and the conditions, which are influencing the lifetime of the power semiconductors, are investigated. It is targeted to find critical operation modes of the ST in the distribution system, which have an impact on the reliability. The investigation includes all stages of the three-stage ST.

*Target II: Active thermal control for increased lifetime of the ST*

The second research objective is to investigate the tradeoff between efficiency optimization and thermal stress for the power semiconductors. Active thermal control is targeted to be applied for increasing the lifetime in the detected critical operation conditions for overcoming the lifetime limiting conditions. To address this, the modular structure of the ST, consisting of parallel and series connected building blocks, should be exploited to route the power optimally with respect to efficiency and reliability in the system.

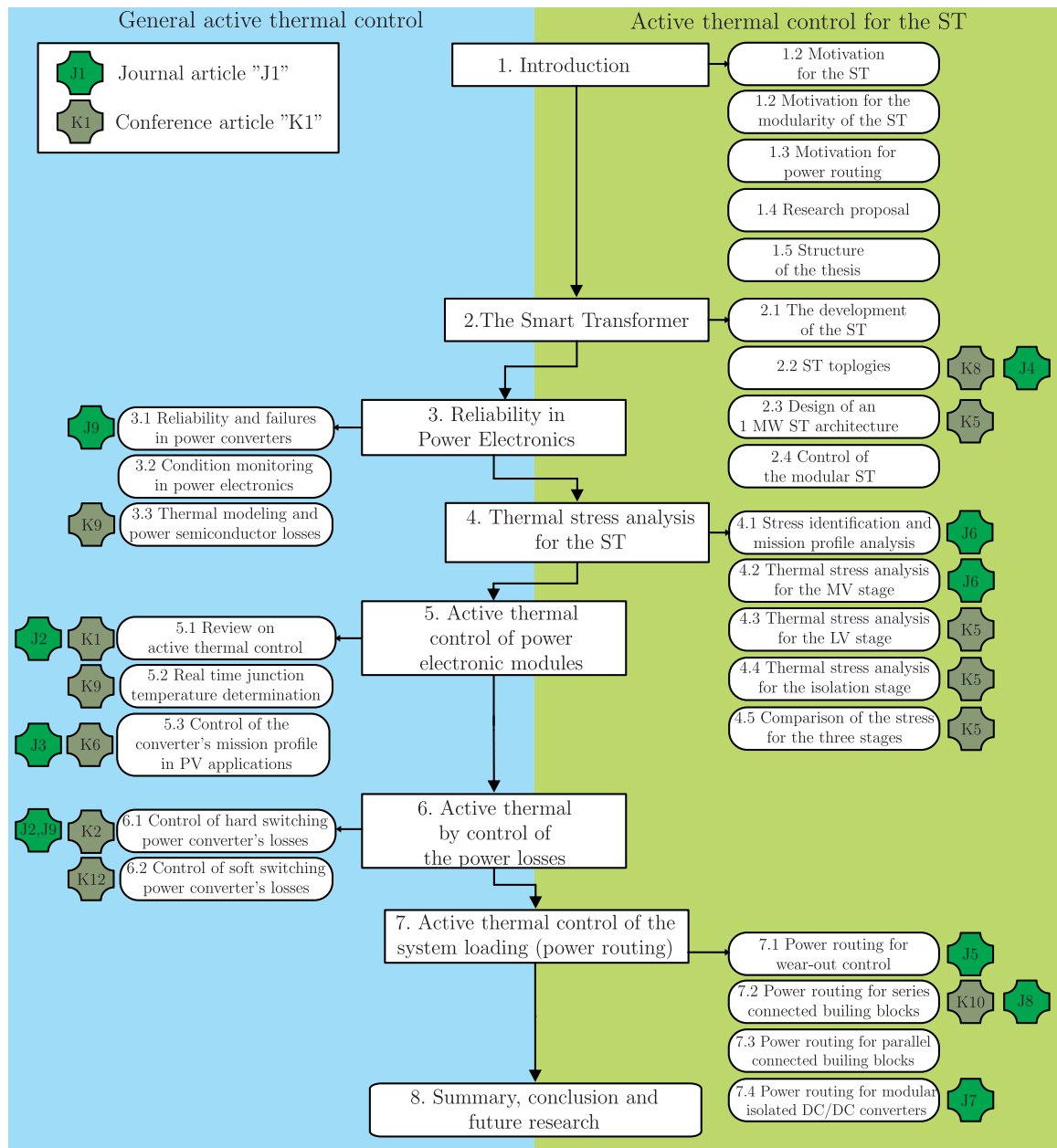


Figure 1.2: Structure of the thesis and the related publications.

## 1.5 Structure of the thesis

The structure of the thesis is shown in Fig. 1.2. The concept of the ST is introduced and motivated in section 2, where also different topologies are introduced for a three-stage ST architecture. Section 3 introduces the reliability concept and examines the failure mechanisms of power electronic modules, which are mostly dependent on the junction temperature. Condition monitoring in power electronics is reviewed and the approach for junction temperature modeling, which is applied in this work, is introduced. Based on this, thermal stress analysis is conducted for the three stages of an ST during power variations in the grid and a simulated grid fault in section 4. From this analysis, the expected lifetime under different probabilities is obtained and a thermal de-rating is proposed to design the system for predefined lifetimes.

In section 5, active thermal control is introduced and categorized. A review on the literature in the field is given and it is categorized in control of the power converter's losses and control of the power converter's system loading. For junction temperature estimation during power converter operation, an estimator is introduced and validated experimentally with a maximum junction temperature limitation. As an example for control of the power converter's system loading, a multi-objective Maximum Power Point Tracking (MPPT), which reduces the thermal cycling during fast changing irradiance, is presented. In section 6, two algorithms for the control of the power converter's losses are developed. One of them is applicable to hard switching power converters and one is applicable for isolated DC/DC converters. Active thermal control by means of power routing is addressed in section 7 and demonstrated for a modular system composed of series connected building blocks, parallel connected building blocks or coupled by isolated DC/DC converters. These categories represent all stages of the ST, whereby the application of power routing is not limited to STs. The power is routed in dependence of the condition of the building blocks to control the wear out and the aging of the cells.

In section 8, the results are summarized and concluded before an outlook on future work is given.

## 1.6 Assignment of publications to the sections of this thesis

The publications related to this thesis are assigned to the different sections in the following, which is additionally visualized in Fig. 1.2. A complete list of the publications related to this thesis is given in the attachment (section 10.1).

- Section 2 addresses the architectures considered in [K8] and [J4] and the design of the ST was proposed in [K5]
- Section 3 is based on the conference publications of [K9] with short parts of [J9]
- Section 4 contains parts of the conference article [K5] and the journal articles [J6] plus an additional analysis
- Section 5 is based on conference publications [K1], [K6], [K9] and the journal articles [J2] and [J3]
- Section 6 uses parts of the conference articles [K2], [K12] and the journal articles [J2] and [J9]
- Section 7 contains parts of the conference article [K10] and the journal articles [J5], [J7], [J8]

## 2 The Smart Transformer

This section reviews the origins of the ST and categorizes the different possible architectures by the number of DC-links and by its modularity. The three-stage ST is motivated and for each of the three stages possible power converter topologies are proposed and compared. A 1 MW ST is designed and its control is described.

### 2.1 The development of the Smart Transformer

#### 2.1.1 Introduction of the ST

The SST was patented by McMurray as a device based on solid state switches with high frequency link for AC/AC conversion or AC/DC conversion in 1968 [16]. This high frequency link is differentiating it from back to back converters already commonly applied in wind turbine systems [17]. In the 80s, Brook highlighted the output voltage magnitude and waveform conditioning capability in a patent about a high frequency (HF) AC/AC converter [18]. These two described inventions provide the basis for the SST, which was further defined to be connected to MV in [19] to delimit the SST from already established isolated power converters operating with LV [20].

At the time of the inventions, the limitation of the application of the SST was given in the cost, volume, efficiency and reliability. Advantages, which balance out these disadvantages, have not been found and the resulting concepts have not been transferred into products at that time. However, the development of fast switching power semiconductors, like Insulated-Gate Bipolar Transistor (IGBT) and the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), improves the potentially achievable efficiency and enables a reduction of the volume in comparison with the traditional transformer. The reduced weight and volume in comparison with the low frequency transformer has encouraged projects targeting the application of the SST in traction [21, 22]. A prototype was built and tested, but despite the additional advantage of higher efficiency than the 16.7 Hz transformer, it has not achieved market breakthrough. As a reason for this, the current standard is changing to 50 Hz transformers, which already enables a significant reduction of the volume.

The SST could have a second chance in the electrical distribution grid, where it can potentially increase the penetration of renewable energy and relieve the transmission costs. In the grid, the SST can provide ancillary services and the capability to link AC grids with DC grids, being an enabler for a smooth transition to DC in parts of the grid. Similar to the application in traction systems, the volume and weight are important in the grid, but even more important is the capability for communication and grid management, which makes the SST smart. This results in the name Smart Transformer.

The vision of the application of STs in the electrical grid differs, but follows the trend of installing more intelligent devices with communication and control capability in the grid [23]. The FREEDM center is advertising the Energy Internet [24], where an ST is connecting

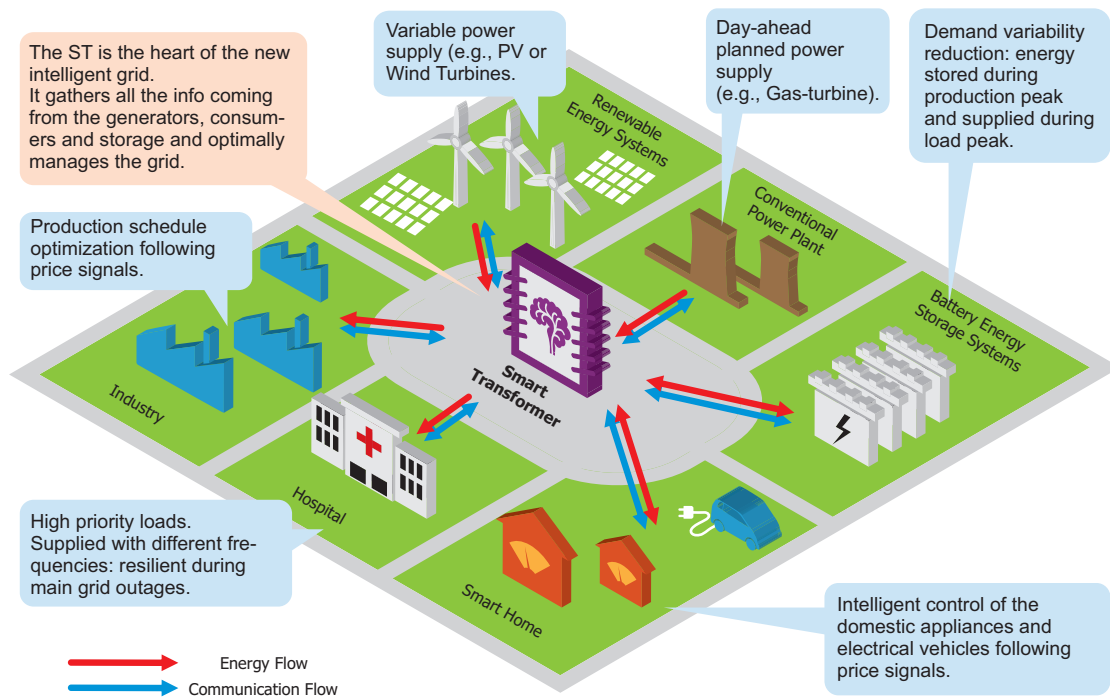


Figure 2.1: The ST in the distribution grid is managing power and information [7].

all loads and the energy is managed like the information in the internet. Other researchers see the potential waveform shaping capability for the electrical grid [25, 26], whereby one of the few prototypes tested in the real distribution grid with the validation of the services is demonstrated in [27]. However, most industrial SST prototypes, which were realized, e.g. by General Electric [28], Alstom [29] or ABB [30] were proposed for traction applications. For the application of an ST in the distribution grid, it is mandatory to combine knowledge from the fields of power electronics and power system, in which the ST needs to operate. This is done for the first time in the HEART project. A scenario, which is proposed by this project, is shown for one ST applying autonomous grid management, control of the grid connected loads and storage in Fig. 2.1.

In contrast to the traditional transformer, the ST can provide reactive power in the LV and the MV grid. Furthermore, it can communicate with the connected generators and loads in the grid, which enables to optimize the generation and the consumption in the node. As an opportunity, also the Battery Energy Storage System (BESS) can be managed by the ST. With the knowledge of all the generators and loads connected to the grid, it can also enable a grid optimization as shown for the connected electric vehicle charging stations. Thereby, the vehicles can be charged when the power is provided for a low price.

Beside the listed advantages of the ST, the main concerns against its application are still expected higher system costs, lower efficiency, higher complexity and lower reliability. In order to meet the concerns of high costs, ancillary services for the grid can be provided to pay back the investment costs. The efficiency can be addressed with modular power converters and/or wide bandgap devices, such as Silicon Carbide (SiC) with its superior behavior in comparison with Silicon (Si) based devices. The reliability of the ST is affecting the quality of service, which is important for the acceptance from the user's point of view. It is important

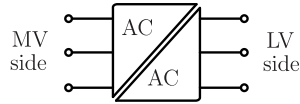


Figure 2.2: ST architecture without DC-link.

to highlight, that the ST as a series connected device in the grid potentially affects a blackout, if it is failing. Consequently, a failure needs to be prevented to avoid the related costs of a blackout and the repair under time pressure.

In order to optimize the system and to achieve the goals of the system design, an appropriate architecture with suitable topologies needs to be chosen and realized, because not every design may enable the desired features. For this reason, a categorization of possible ST designs is done in the following.

### 2.1.2 Categorization by the number of DC-links

Several SST and ST topologies have been proposed for different voltage ranges and different applications. In this work, the connection of two AC grids is considered and consequently, the following analysis is assuming only ST topologies for AC/AC conversion. Following the definition of the ST, the services are the key element of the ST in the distribution grid and motivate its application [7]. Therefore, a categorization should point out the different potential to provide services. This capability is closely related to the number of DC-links:

- No DC-link
- Single DC-link
- Two DC-links

The ST architecture without a DC-link is shown in Fig. 2.2. An opportunity to realize the single-stage ST are matrix converters. Their main advantage is the low component count due to the single power conversion stage, whereas its biggest disadvantage is to offer only limited grid services due to the coupling between the AC grids. Furthermore, the control effort and the complexity of the protection for these topologies is high [31]. Despite high research effort, the matrix converters have only been applied in niches applications. With respect to its application in STs, a Matrix converter based topology seems to be the least promising category, because of the limited capability to decouple the connected grids. Nevertheless, in SST applications, where services are less important, this evaluation might change.

Another opportunity to realize single-stage ST architectures is the use of current source topologies [32]. This holds the advantage of not requiring DC-link capacitors, whereby grid services can be provided [32]. As a problem, the topologies require power semiconductors, which can conduct and block the current in both directions, which requires the use of two power semiconductors per switch if Silicon components are used. Despite the advancement of new power semiconductor technologies, the efficiency of current source topologies is still a concern.

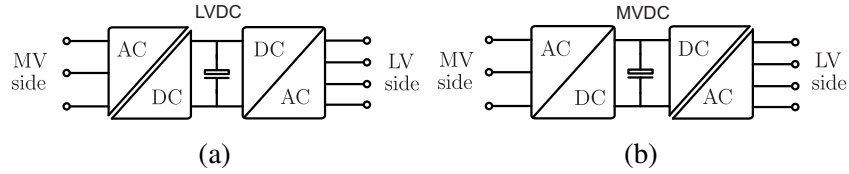


Figure 2.3: ST architecture with single DC-link based on two power conversion stages: (a) with LVDC link, (b) with MVDC link.

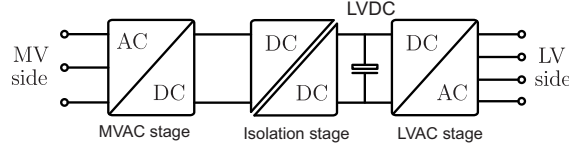


Figure 2.4: ST architecture with single DC-link based on three power conversion stages.

The ST with a single DC-link can be realized either with two or three power conversion stages. With two stages, it is based on an isolated AC/DC conversion and a non-isolated power converter. The isolated power converter can either be installed in the MV stage with access to the Low Voltage Direct Current (LVDC) link as shown in Fig. 2.3 (a) or it can be installed in the LV stage with access to the Medium Voltage Direct Current (MVDC) link as shown in Fig. 2.3 (b). Depending on the realization of the isolation, the rating of the power semiconductors needs to be set. For the case in which the isolation is provided in the Medium Voltage Alternating Current (MVAC) side, the whole ST can be realized with LV power semiconductors. If instead the isolation is installed in the Low Voltage Alternating Current (LVAC) side, the power converter requires to be rated for MV, which requires to cascade building blocks, cascade power semiconductors or even use SiC based power semiconductors. The differences between the two concepts are summarized in table 2.1.

The ST architecture with a single DC-link and three power conversion stages is shown in Fig. 2.4. It obtains a AC/DC conversion in the MV side and the LV side, whereas the LVDC link is interfaced with a medium frequency DC/DC converter to the MV side. The isolation stage operates with fixed input/output voltage ratio and can be realized with soft switching power converter topologies, which are operating with high switching frequency [33]. Thus, it is possible to reduce the space requirement of the transformers [34]. This makes this architecture a promising candidate for the ST.

As the third opportunity, the ST can be realized with two accessible DC-links in the MV and LV stage as shown in Fig. 2.5. Similar to the three-stage architecture with a single DC-link, it benefits from the reduced space requirement gained by the medium frequency DC/DC

Table 2.1: Comparison of the two-stage ST architectures with the isolation in the MV/LV side.

	Galvanic isolation on MV side	Galvanic isolation on LV side
Power converter	LV rating	MV rating
Available DC-link	LVDC	MVDC

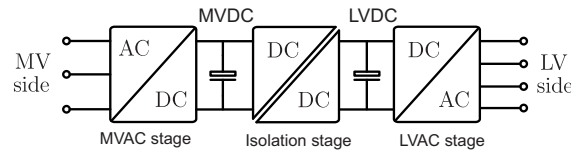


Figure 2.5: ST architecture with two DC-links based on three power conversion stages.

converter in the isolation stage. The biggest advantage of two DC-links is the capability for providing additional services to both connected AC grids. In addition, two DC-links obtain the capability to interface DC grids with MV and LV levels [35]. As a disadvantage for the topology, the three stages potentially reduce the efficiency of the system if no DC grids are fed. Instead, if DC grids are connected, the number of energy conversions can possibly be reduced [36].

In summary, a higher number of DC-links comes at the expense of more components, which can possibly fail. As a difference between the two-stage ST and the three-stage ST with one DC-link access, the decoupling of the grids from each other requires the third stage. In the two-stage ST, disturbances in one grid may be reflected in the DC-link and consequently in the other grid. As another disadvantage for the two-stage architecture, the isolated converter is driven as a matrix converter or current source converter with the afore mentioned disadvantages. A volume and weight-reduction as targeted for the ST in these topologies can only be achieved, if the converter of the isolation stage is switching with a high frequency. This is challenging the target for high system efficiency, since the devices are operating in hard switching in the converter, which is limiting the maximum switching frequency by the losses of the power semiconductors. Instead, from the perspective of the losses of the converter, the target is to minimize the switching frequency. As another important difference between the possible topologies, the DC-link is either available in the MV side or the LV side. The voltage level of MV might be beneficial in case of the connection of big generators or loads, e.g. renewable energy sources in DC. The LVDC access might be more suitable for the connection smaller generators or loads, such as households in DC.

Because of the services, which can be provided by the different architectures, the ST is most likely to be realized with two DC-links. If the MV side DC-link is not required, the realization based on a single DC-link in the three-stage architecture is also a promising architecture. This is in accordance with the result of the ST topology comparison made in [37], where a three-stages ST architecture concluded to be most promising architecture. In the following, practical examples of suitable topologies will be presented and the related challenges are discussed.

### 2.1.3 Three-stage ST categorization by modularity

The definition of the ST from subsection 2.1 requires the connection to the MV grid. A resulting problem is the definition of the voltage range, which is between 2.3 kV and 35 kV in different countries [33]. This brings the challenge to use suitable power semiconductors for this voltage range in a suitable topology. Additionally, the power rating has significant



influence on the performance of the devices and the topologies. One solution is to use the well-established topologies of the low voltage applications with power semiconductors rated for MV applications. This is the non-modular realization of the ST as it is found in [38]. For a realization of a 2.3 kV prototype, there are even Si components available, which can be used, whereas higher voltages require wide-bandgap devices or the series connection of multiple devices, if a two level converters is used. However, even today's SiC devices cannot be used for a grid voltage of 35 kV in a two level converter. To the current state, there are Si-components with a blocking voltage of 6.5 kV [39]. For SiC this voltage range has been extended up to 15 kV IGBTs and MOSFETs [40]. As an example in ST applications, the FREEDM center has applied the SiC devices with a blocking voltage of 10 kV in an ST prototype [41]. The advantage of this approach is the low number of drivers, sensors and the single transformer, whereas disadvantages are the required high converter output filter and the stress for the passive components. Particularly, the higher blocking voltages in combination with the higher switching frequencies and the higher commutation speed increase the stress for the insulation material [42]. However, these devices are only available for research purposes so far and there is no product in the market. Another possible solution to build MV converters is the use of multilevel converters, which can be realized in a modular architecture consisting of several cells [43]. The number of cells in the modular converter is another degree of freedom for the optimization. In general, devices rated for lower blocking voltage demonstrate better characteristics than devices for high blocking voltages of the same technology. Furthermore, there is the possible to combine the technology of wide bandgap power semiconductors with the modularity to design systems with even higher efficiency [44].

Modular converters are advantageous in terms of scalability in power, scalability in voltage, reduced  $dv/dt$  and reduced  $di/dt$  resulting in lower Electromagnetic Interference (EMI). In [9], it has been concluded that modular power converters are an opportunity to achieve higher efficiency with Si-based power semiconductors to make it competitive for the application in STs. Another central advantage is the opportunity to include fault tolerance on the cell level in the system design [14, 45].

As a conclusion, the optimum topology and its design is dependent on the required grid services, the AC grid voltage, the requirement for DC connectivity, the criteria for efficiency, the reliability requirements and others. As an example in the SST review [19] services are not in the focus, leading to a categorization, where the position of the transformer is dividing the topologies in matrix converters, isolated back end converters, isolated front end converters, isolated modular multilevel converters and the single-cell approach (corresponding to the Modular Multilevel Converter (MMC)). Furthermore, the technology of the power semiconductors changes the costs and the performance of the ST, whereby SiC is enabling to increase the blocking voltage and thereby reducing the complexity and the minimum number of levels in a converter as demonstrated in [41]. However, Si technology is currently attractive because of the lower costs in comparison to the SiC components and the higher power cycling capability. For this reason, this work relies on the current Si technology and requires designing modular power converters with a high number of cells.

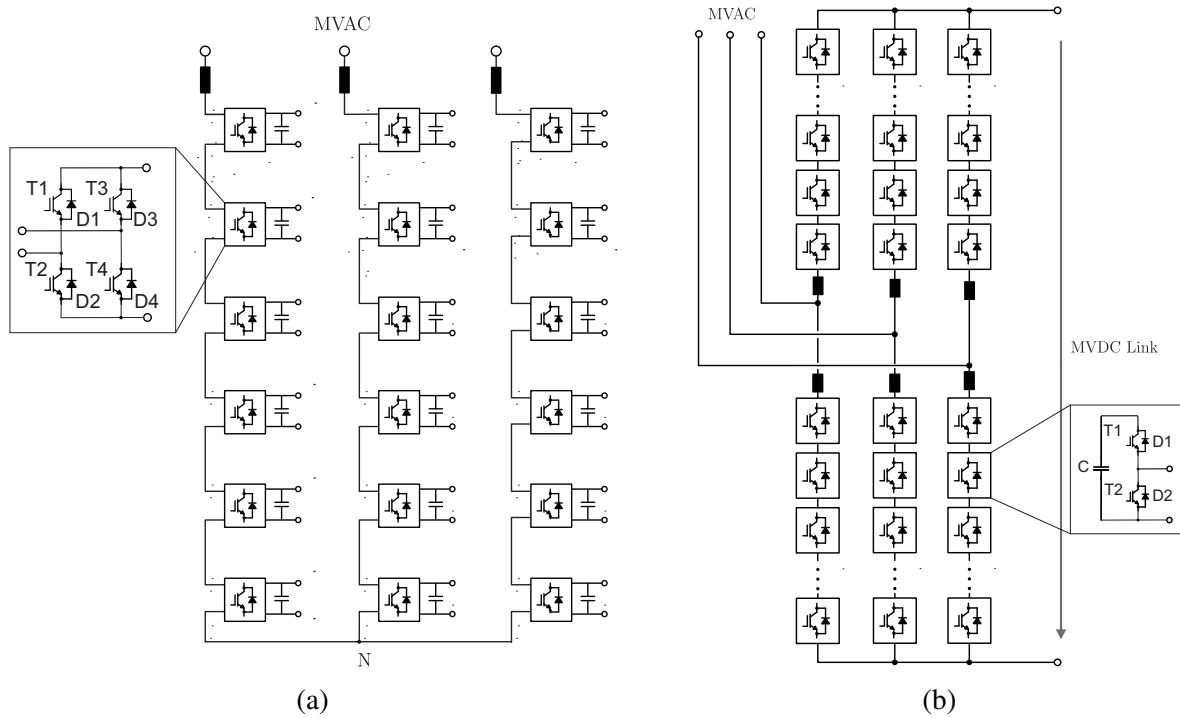


Figure 2.6: Possible topologies for the MV stage of the ST: (a) Cascaded H-bridge converter (CHB), (b) Modular Multilevel Converter (MMC).

## 2.2 Smart Transformer topologies

Motivated by the maximum flexibility and the maximum capability for services, a three-stage ST is chosen in the following. A modular ST architecture is designed and suitable modular topologies are introduced for the MV stage, the LV stage and the isolation stage.

### 2.2.1 MV stage topologies

Challenged by the voltage blocking capability in the MV side, modular power converters seem to be a suitable solution to achieve low switching frequencies for the power semiconductors and to obtain a smaller output filter compared to a non-modular power. Candidates reported in literature for the three-stage ST are the Cascaded H-Bridge Converter (CHB) as shown in Fig. 2.6 (a) and the MMC as shown in Fig. 2.6 (b) [46]. Both considered converter topologies are built by modular Single Cells (SC), which are connected in series. An important difference in the two converters is the DC-link access, whereas the MMC provides MV access and the CHB converter does not provide it. Another central difference is the number of cells required for the converters: The CHB is a star connected power converter and requires a lower cell number than the double star connected MMC [47]. In this work, the CHB is using full bridge cells and the MMC consists of half bridge cells. Both topologies can use other basic cells, which can even be Neutral Point Clamped (NPC) cells [48]. The difference in the rating of the components for a given grid voltage is presented in table 2.2 [47]. Assuming a similar voltage rating of the power semiconductors in the different topologies, the number of power semiconductors in the CHB converter are half the number of the

Table 2.2: Comparison of required cell number in the MV side converters for a predefined grid voltage and similar device voltage rating.

	<b>CHB</b>	<b>MMC</b>
MVDC link access	not available	available
Number of MV side cells	$x_{CHB}$	$4 \cdot x_{CHB}$
Number of power semiconductors	$4 \cdot x_{CHB}$	$8 \cdot x_{CHB}$ (for half-bridge cells)
Required number of isolation stage cells	$x_{CHB}$	flexible ( $4/3 x_{CHB}$ for voltage rating of CHB-cells)

Table 2.3: Comparison of the considered MV power converter topologies.

	<b>Advantages</b>	<b>Disadvantages</b>
MMC	<ul style="list-style-type: none"> <li>•MVDC-link access</li> <li>•Commercially available for HVDC</li> </ul>	<ul style="list-style-type: none"> <li>•No direct connection to the individual cell in the isolation stage required</li> <li>•High control complexity</li> <li>•Higher number of cells in the isolation stage needed</li> </ul>
CHB	<ul style="list-style-type: none"> <li>•Redundant power paths</li> <li>•Lower number of components and cells</li> <li>•Established in MV drives</li> </ul>	<ul style="list-style-type: none"> <li>•No MVDC link access</li> <li>•<math>2^{nd}</math> harmonic oscillation on the DC-link cell voltages</li> <li>•failure in one cell affects the correspondent DC/DC cell</li> </ul>

MMC. Instead, if a full bridge is used, the number of power semiconductors for the MMC is four times higher than in the CHB-converter, but the current rating of the MMC cells can be reduced. Because of the shared DC-link, the number of cells in the isolation stage of the MMC requires a higher number of cells in comparison to the CHB converter with similar component rating. The CHB converter requires for every MV side cell a connection to the isolation stage with similar voltage and power rating. Instead, the MMC enables to use a flexible voltage sizing of the cells in the isolation stage, but needs to block the whole MVDC link voltage. The advantages and disadvantages of the considered power converter topologies are shown in table 2.3.

### 2.2.2 LV stage topologies

The LV stage design of the ST can benefit from the knowledge and experience with power converters for the integration of renewable energy, e.g. wind turbines and photovoltaic power plants. As a difference to the application in PV converters, the ST requires four wires due to the possible connection of single-phase loads to the grid.

The LV stage of the ST faces the challenge of a high current rating compared to the other stages. Possible power converter topologies for this stage are the standard two level converter or three level converters, such as the NPC or the T-type. The requirement of the fourth wire of the converter is especially easy to access in the three level converters. In addition, the efficiency of the three level converters is expected to be higher than the efficiency of the other

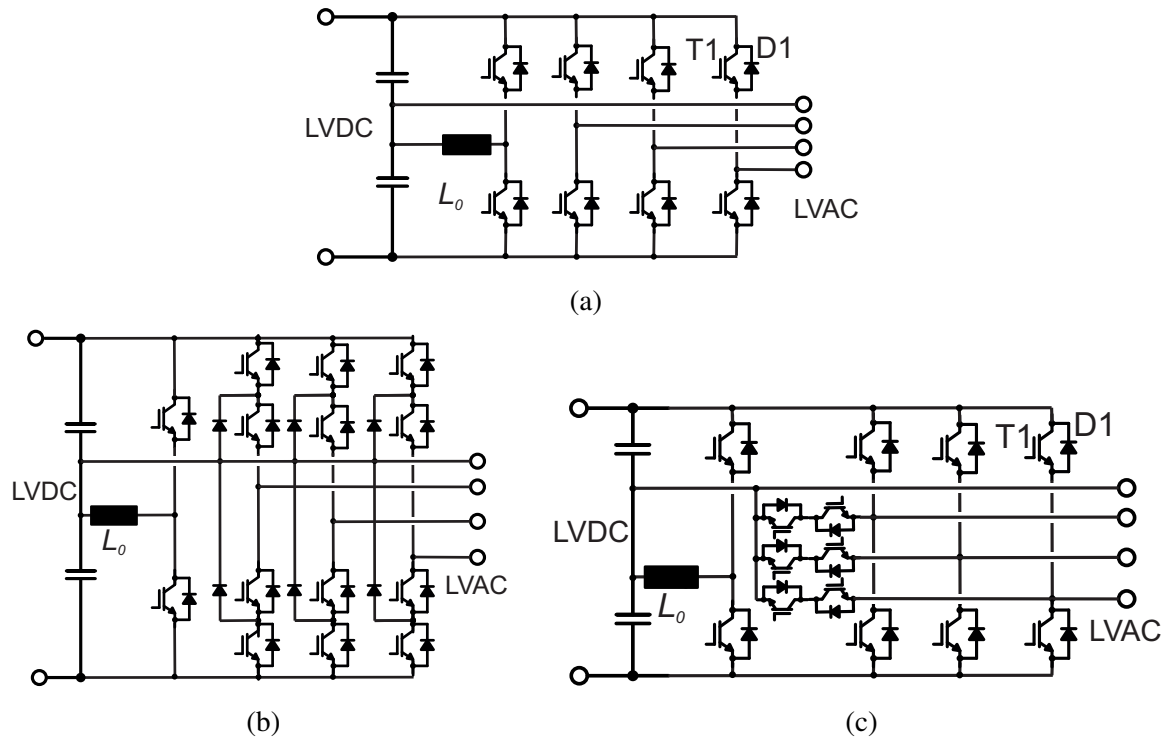


Figure 2.7: Possible topologies for the LV stage of the ST: (a) Two level Voltage Source Converter (VSC), (b) Three level Neutral Point Clamped (NPC), (c) T-type.

alternatives. However, the drawbacks of the three level converter topology is the higher component count and the uneven thermal stress distribution between the power semiconductors [49].

The two level VSC shown in Fig. 2.7 (b) is consolidated in the literature due to its common application in motor drives, which makes many optimized power semiconductors suitable for the voltage range. As pointed out before, the fourth wire requires the access of the midpoint potential of the DC link. To reduce the capacitance of the DC-link and to enable an active balancing, a fourth half bridge is added. However, the control is well known and a realization will benefit from low costs. The biggest disadvantage is the efficiency, which will be limited by the power semiconductors technology.

The NPC as shown in Fig. 2.7 (c) is a three level converter, which has been studied in comparison with the two level VSC in [50]. The main advantage of this topology is the higher number of levels in combination with a reduced blocking voltage for the power semiconductors. This results in a higher expected efficiency in comparison with the two level VSC, because power semiconductors rated for a lower voltage usually exhibit lower losses. Disadvantageous is the higher component count in combination with unequal stress for the power semiconductors, which can be solved by an active NPC [51]. Additionally, the balancing of the capacitor voltages is increasing the control complexity.

The T-type topology presented in 2.7 (d) has been proposed as an alternative to the NPC. The disadvantage compared to the NPC is the higher voltage rating for the power semiconductors [52], which needs to be similar to the two level converter. Furthermore, the connection of

Table 2.4: Comparison of the considered modular LV power converter topologies.

	<b>Advantages</b>	<b>Disadvantages</b>
Two level VSC	<ul style="list-style-type: none"> <li>•Widespread adoption in industry</li> <li>•Low component count</li> </ul>	<ul style="list-style-type: none"> <li>•Access of the neutral point requires additional components or capacitance in the DC link</li> </ul>
Three level NPC	<ul style="list-style-type: none"> <li>•Direct neutral line access</li> <li>•Power semiconductors rated for lower voltage</li> <li>•Higher efficiency</li> </ul>	<ul style="list-style-type: none"> <li>•Higher number of components</li> <li>•Uneven thermal stress</li> </ul>
Three level T-type	<ul style="list-style-type: none"> <li>•Direct neutral line access</li> <li>•Higher efficiency</li> </ul>	<ul style="list-style-type: none"> <li>•Higher number of components</li> <li>•Full voltage rating of the power semiconductors</li> </ul>

the phases to the fourth wire requires two IGBTs per phase with also two diodes if silicon components are used. Nevertheless, the component count is lower in comparison with the NPC, which requires six diodes more. Finally, the advantages and disadvantages of the considered power converter topologies are summarized in table 2.4.

### 2.2.3 Isolation stage topologies

The high blocking voltage in combination with low current on the MV side and the low voltage with high current in the LV side challenge the isolation stage. This can be addressed by series input and parallel output connected modular power converters. Nevertheless, as pointed out in the last subsection, the architecture of the isolation stage is dependent on the design of the MV converter stage. If the CHB converter is chosen in the MV stage, the cells in the isolation stage are sized for the similar voltage and power rating. Instead, the MMC enables to access the MVDC voltage and thus gives the freedom to arbitrary scale the voltage of the basic cells.

As possible cells for the isolation stage, soft switching power converters are favored because of the goal to maximize the efficiency. Candidates for this stage are the Dual Active Bridge (DAB) as shown in Fig. 2.8 (a), the Series Resonant Converter (SRC) as shown in Fig. 2.8 (b) and the Quadruple Active Bridge (QAB) as shown in Fig. 2.8 (c). For the SRC and the DAB only the single-phase topology are considered, because of the increased complexity for the three phase transformer design. Furthermore, the third phase of these DC/DC converters would not reduce the number of power semiconductors or the rating of the power semiconductor's blocking voltage in the MV side.

The DAB was proposed as a topology for DC/DC power conversion [53] and consists of two power converter cells coupled by a medium frequency transformer. In case of the single-phase DAB as shown in Fig. 2.8 (a), two full bridges are used. By applying the commonly used phase shift modulation, the full bridges switch with constant duty cycle of  $d = 0.5$  and the phase shift between primary and secondary side is defining the power transferred by the converter, enabling bidirectional power flow. Beside this basic operation with phase shift

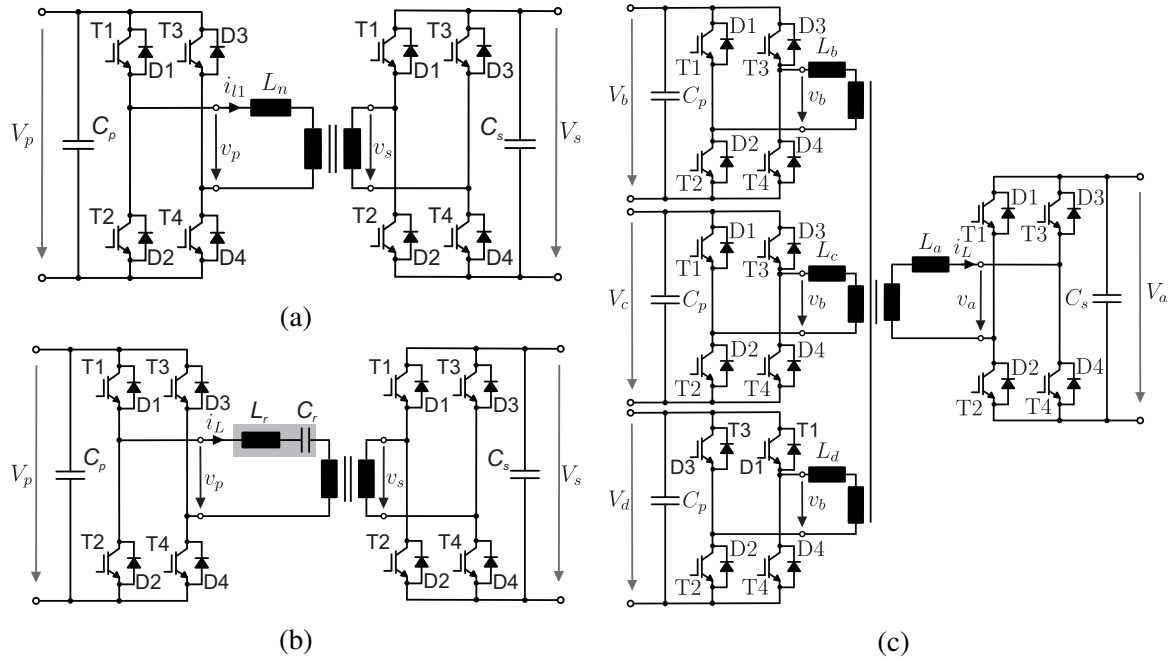


Figure 2.8: Possible topologies for the isolation stage of the ST: (a) Dual active bridge (DAB), (b) Series Resonant Converter (SRC), (c) Quadruple Active Bridge (QAB).

modulation, several strategies have been employed to optimize the operation of the DAB [54, 55].

The SRC was proposed in the prototype for traction applications from ABB [30]. The architecture of the SRC, shown in Fig. 2.8 (b), is comparable to the DAB, but has an additional capacitor in series to the transformer, forming a resonant tank. During operation, phase and frequency are modulated to transfer the power [56]. Its advantage is to exhibit good open loop voltage regulation and thus does not require a current sensor. This is a possible advantage for several applications, but in the electrical distribution grid, this is a disadvantage, because its behavior as a DC transformer directly couples the DC-links to each other. In this manner, the AC transformer would be replaced by a DC transformer without the desired decoupling of the two grids. In [57], the converter consisting of full bridges was even proposed to be reconfigurable from a full bridge SRC to a half bridge SRC after the failure of one power semiconductor. As an additional opportunity, the SRC can be designed with multiple ports [58]. However, since the disadvantage of the coupled DC-links remains, this topology is not considered.

The input voltage to output voltage ratio offers the opportunity to use a semi-modular architecture in the isolation stage, which is based on the QAB as shown in Fig. 2.8 (c) [59]. Semi-modular power converters utilize the multiple windings on a transformer to implement series connected cells on the MV side and parallel connected cells on the LV side. Concerning the cells of the QAB, it is also possible here to use different basic cells for the QAB [60]. The QAB has been proposed for ST applications as well as for a LV converter, which is connecting load, source, grid and storage [61]. For the application in LV drives, this approach

Table 2.5: Comparison of the considered modular power converter topologies for the isolation stage.

	<b>Advantages</b>	<b>Disadvantages</b>
SRC	<ul style="list-style-type: none"> <li>•Simplicity (fixed input/output voltage ratio)</li> <li>•Already adopted in SST prototype for traction system</li> <li>•No closed loop control mandatory</li> <li>•Low number of sensors required</li> </ul>	<ul style="list-style-type: none"> <li>•High number of cells required</li> <li>•Low flexibility</li> <li>•Behavior of a DC transformer</li> </ul>
DAB	<ul style="list-style-type: none"> <li>•Simplicity</li> <li>•Mature technology, already adopted</li> <li>•Partial decoupling of the grids connected to the DC-links is possible</li> </ul>	<ul style="list-style-type: none"> <li>•High number of cells required</li> <li>•Low flexibility</li> </ul>
QAB	<ul style="list-style-type: none"> <li>•Redundant power path possible</li> <li>•Lower number of high-frequency transformers compared to the DAB</li> <li>•Partial decoupling of the grids connected to the DC-links is possible</li> </ul>	<ul style="list-style-type: none"> <li>•Coupling of the MV side cells through the transformer</li> <li>•LV side full bridge with higher current rating</li> </ul>

has also been implemented for multiple active bridges connected to one single core [34]. An advantage of this topology is its potential reconfigurability and the DC-link balancing can be performed by transferring energy between the bridges through the magnetic core. As an advantage of the QAB, the windings can be connected to different cells, enabling to route the power in the system. However, this can also be a disadvantage in the case, that different power is transferred by the different ports, leading to increased reactive current and a reduction in the efficiency, which will be demonstrated later in this work. The advantages and disadvantages of the considered power converter topologies are summarized in table 2.5.

### 2.3 Design example of a 1 MW ST architecture

A three-stage ST with a power rating of 1 MVA is designed as the basis for the reliability analysis of the ST. In addition to the choice of the topology, the power semiconductors are chosen and the cooling system is designed. The ST is based on the MMC topology in combination with the QAB in the isolation stage as shown in Fig. 2.10. For the LV stage, four parallel two level VSC are designed. The proposed topology and the grid parameters are shown in Table 2.6. It is worth to mention that the optimal topology and the optimum modularity is difficult to define because each topology requires different voltage and current ratings of the power semiconductors, different filter sizes, different number of power semiconductors and different control methods. Furthermore, the number of modular components has strong impact on the device loading and needs to be defined carefully [62]. With the continuously ongoing improvements in the field of power semiconductors, this optimum might change rapidly. However, the methods for thermal stress and reliability analysis for the chosen modular system can be transferred easily to other solutions and designs. It is noted that the medium voltage DC-link and the low voltage DC-link are shown and they are possible to

be individually connected with additional DC grids, which can have an additional impact on the rating and the reliability of the ST.

Beside the choice of the modularity, suitable power semiconductors and the heat sinks are chosen. In order to ensure a certain reliability for each stage of the ST, a conservative design is considered.

### 2.3.1 Optimization of the cooling system

The cooling system for the power converter is of importance for the optimization of the system, because the design for the maximum junction temperature is affecting the reliability, which will be investigated in the following sections. Moreover, the maximum junction temperature is defining the required thermal resistance and therefore the required technology and size of the heat sink. Thereby, the thermal impedance is assumed to correlate with the size of the heat sink. Thus, it is affecting the power density of the system and furthermore, the size of the heat sink is assumed to correlate with its costs. After all, this design is an optimization between reliability on the one hand and volume and costs on the other hand.

To describe the influence of the cooling system on the power density, a cooling system performance index (CSPI) was introduced in [63]. This index was used to evaluate the effectiveness of different heat sinks in dependence of their thermal resistance  $R_{th,ca}$  and their size  $VS$ . This definition of the CSPI and is given in (2.1).

$$CSPI = \frac{1}{VS \cdot R_{th,ca}} \quad (2.1)$$

In the following, the CSIP is used to determine a connection between maximum junction temperature and required heat sink size. Since it is required to design a cooling system for the dissipation of the maximum losses  $P_{loss,max}$  without exceeding the designed maximum junction temperature  $T_{j,max}$ . In steady state conditions, the dependence of the junction temperature on the losses can be expressed in dependence of the thermal resistance between junction to case  $R_{th,jc}$  and the designed maximum case temperature  $T_{c,max}$ , as it is expressed in (2.2).

$$T_{j,max} = R_{th,jc} \cdot P_{loss,max} + T_{c,max} \quad (2.2)$$

In this equation, the maximum case temperature  $T_{c,max}$  can be expressed in dependence of  $R_{th,ca}$ , the maximum losses and the ambient temperature  $T_a$ , which is shown in (2.3).

$$T_{c,max} = R_{th,ca} \cdot P_{loss,max} + T_a \quad (2.3)$$

This equation is now inserted in (2.1) and results in (2.4).



Table 2.6: Studied grid and ST architecture.

Rated power	1 MW
MVAC line to line voltage	11 kV rms
MVDC link voltage	19 kV
LVDC link voltage	800 V
LVAC line to line voltage	380 V rms
MV side converter	MMC with 15 cells
Isolation converter topology	9 QABs
LV side converter	4 parallel VSC

$$VS = \frac{P_{loss,max}}{CSPI \cdot (T_{c,max} - T_a)} \quad (2.4)$$

This is resulting in a dependence of the heat sink volume on the maximum losses, the temperature drop on the heat sink and the CSPI. The CSPI is assumed to be constant and can be derived for any heat sink. However, it is suggested to use this equation to evaluate different designed maximum junction temperature to an already known design. Thereby the new maximum junction temperature  $T_{j,max,2}$  is the sum of the constant temperature drop  $T_{jc,max}$  (affected by the known maximum losses) and the resulting maximum case temperature  $T_{c,max,2}$ . This is expressed in (2.5), where  $VS_2$  is the volume for the new maximum junction temperature,  $T_{c,max,1}$  is the maximum case temperature of the existing reference design and  $VS_1$  the corresponding heat sink volume.

$$VS_2 = VS_1 \cdot \frac{T_{c,max,1} - T_a}{T_{c,max,2} - T_a} \quad (2.5)$$

The resulting equation shows a hyperbolic dependency of the heat sink volume to the design for a maximum junction temperature. It needs to be considered, that this result was obtained with the assumption of a similar CSPI, which may not be valid for changes in the cooling system technology (e.g. for water cooling). Nevertheless, this equation can be used to size a heat sink based on a new maximum junction temperature design.

Since the ST needs to operate during the whole year for a long lifetime, a conservative design is initially chosen. It is targeted to share the temperature drop between junction and case and between case and ambient equally. The heat sink is selected to maintain the case temperature at  $T_{c,max} = 60^\circ\text{C}$ , and the power semiconductors are selected to obtain a junction temperature around  $T_{j,max} = 80^\circ\text{C}$  under full rated power.

For the proposed thermal design, the dependence of the heat sink volume on the thermal design is shown in Fig. 2.9. For the proposed design, a revised maximum junction temperature of  $T_{j,max} = 100^\circ\text{C}$  doubles the temperature drop between case and heat sink and therefore enables to reduce the heat sink size by 50%.

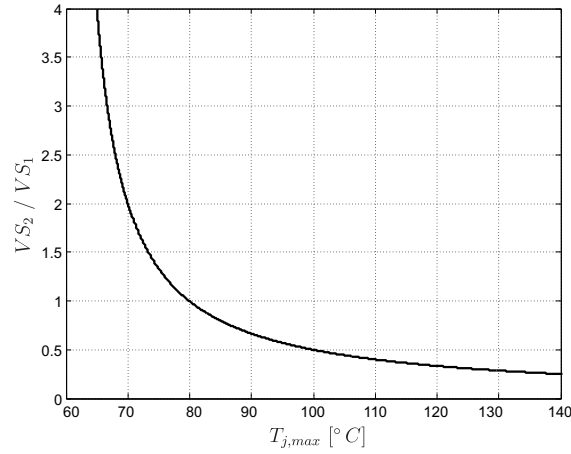


Figure 2.9: Example for the required heat sink volume on different maximum junction temperature based on the initial design for  $T_{j,max} = 80^{\circ}C$ .

Table 2.7: Parameters of the studied MMC converter in the MV stage used in this ST.

Rated power	1 MVA
Power factor	1.0
Rated MVDC voltage	19 kVrms
Rated load current $I_{load,HV}$	75 A
Cell number of each arm	15
Fundamental frequency	50 Hz
Switching frequency $f_{sw}$	2 kHz
Filter inductance $L_f$	57.8 mH (0.15 pu)

### 2.3.2 MV converter stage design

As pointed out before, the MMC topology is a promising solution because of its modularity, industry proofed technology and the described DC-link accessibility. In this study, an MMC based on half bridge cells is chosen because of the lower number of power semiconductors in comparison to the other cells. The number of cells per arm is compromising between a relatively low number of cells with high blocking voltage and a high number of cells with lower blocking voltage. Usually, higher blocking voltages come for the disadvantage of higher switching and conduction losses of the devices, whereby the lower rated devices and a higher number of modular components is advantageous with respect to the losses. An additional disadvantage for a high number of cells is the increased control complexity. However, a higher number of cells might be advantageous for the fault tolerance by means of a breakdown of one cell.

For using the well-established 1200 V power semiconductors, which are used in electric drives, 15 cells per MMC arm are considered. The parameters of the system are listed in table 2.7. The rated MVAC current amplitude is 74.2 A, which results from the design of a 1 MW prototype. The half-bridge IGBT modules SKM100GB176D (100A/1700V) are selected with a heatsink of P3/180 from Semikron for each MMC cell. A conservative

Table 2.8: Parameters of the studied VSC converter in the LV stage used in this ST.

Rated power	4 x 250 kVA
Power factor	0.9
Rated load current	537 A
Fundamental frequency $f_0$	50 Hz
Filter inductance $L_f$	0.37 mH

Table 2.9: Parameters of the studied QAB converter in the isolation stage used in this ST.

Rated power	9 x 111 kVA
MV DC bus	19 kV
Rated MV load current	63 A
Rated LV load current	192 A
Switching frequency $f_{sw}$	5 kHz
Leakage inductance $L_a = L_b = L_c = L_d$	57.8 mH (0.15 pu)

thermal design is made, such that for an ambient temperature of  $T_a = 40^\circ\text{C}$  the maximum junction temperature is  $T_{j,max} = 80^\circ\text{C}$ .

### 2.3.3 Low voltage stage design

Instead of a single converter in the low voltage stage, four parallel two level VSC with the parameters of table 2.8 are used. This enables to continue operation in case of a fault of a singular converter and to operate the converters in interleaved operation, which can improve the optimization of switching losses and filter size. Because of the reactive power consumption in the grid (e.g. caused by directly connected induction machines), the converter is designed for an inductive power factor of 0.9 and the rated load current is 537A. An Infineon half bridge IGBT module is selected (FF900R12IE4) and a sink from Semikron is used (P16/300). The thermal design is made to obtain  $T_{j,max} = 80^\circ\text{C}$  for  $T_a = 40^\circ\text{C}$  under the rated load.

### 2.3.4 Isolation stage design

The isolation stage of the ST is built by 9 QABs in series with a power rating of  $P_0 = 111\text{ kW}$ , each with the parameters listed in table 2.9. The ratio between the ports is chosen to be 1 : 1 : 1 : 1, which results in a similar voltage rating of the primary and the secondary side power semiconductors. The half-bridge IGBT modules FF300R12KT4 (300A/1200V) are selected for the LV side, and FF100R12RT4 (100A/1200V) is selected on the MV side, with a heatsink of P16/300 on both sides to dissipate the heat of an H-bridge cell. Similar to the other stages, for an ambient temperature  $T_a = 40^\circ\text{C}$  the maximum junction temperature is  $T_{j,max} = 80^\circ\text{C}$  under the rated load.

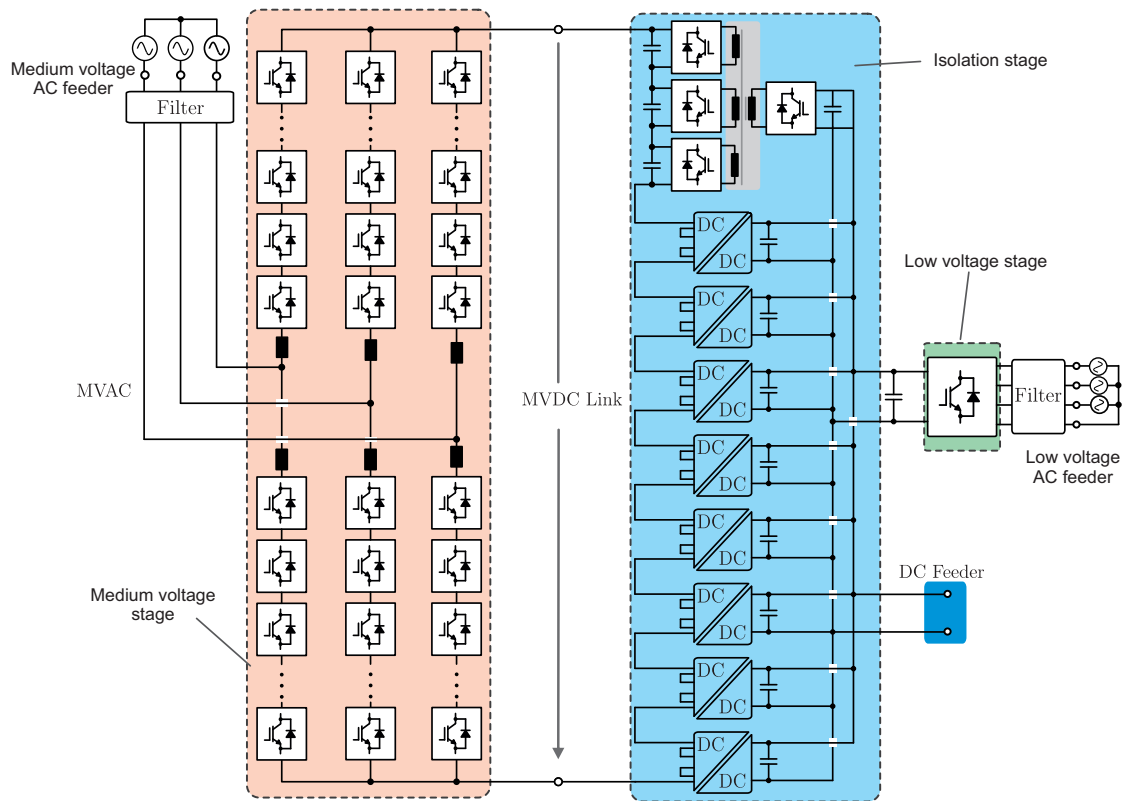


Figure 2.10: Full ST architectures with MVDC and LVDC access consisting of Modular Multilevel Converter (MMC, red), quadruple active bridges (QAB) and two level voltage source converter (VSC, green).

### 2.3.5 Examples of modular ST architectures

Based on the topologies introduced in the last subsection, two examples of three-stage ST architectures are presented in the following. The first architecture is chosen to obtain a DC-link in the MV side. The isolation stage is built by the QABs to enable the use of LV power semiconductors as shown in Fig. 2.10. The QABs are sharing the same DC-link, but can be scaled independently from the voltage rating of the SC in the MMC. In both converters, the number of modular cells is a compromise between lower losses of the power semiconductors due to their low voltage rating and high control complexity because of the higher number of cells. From this DC-link, the LV stage is feeding the LV grid. Storage systems and DC grids can be connected to the LVDC link as shown and the MVDC link is accessible for MVDC connectivity. In this example, the LV stage is not shown because there is no dependency in the interaction with the other converters.

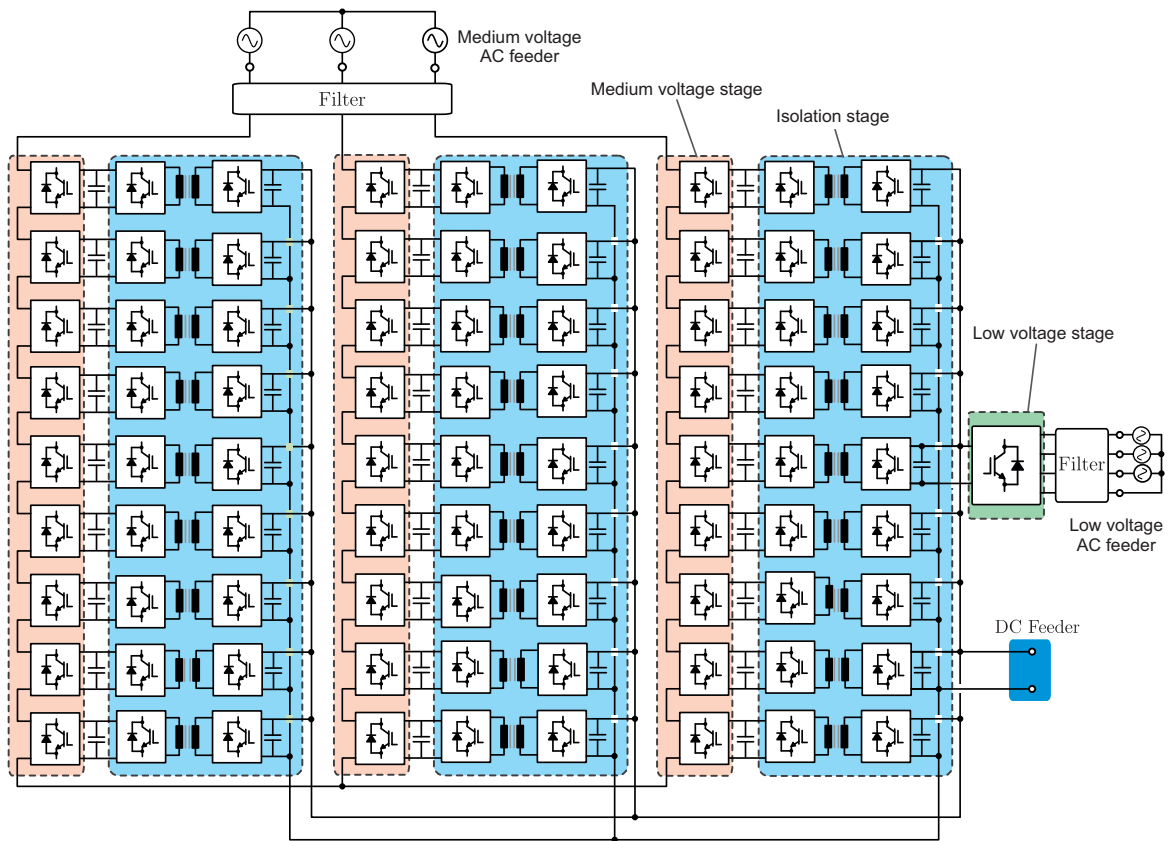


Figure 2.11: Full ST architectures with LVDC access consisting of Cascaded H-bridge converter (CHB, red), Dual Active Bridges (DAB, blue) and two level Voltage Source Converter (VSC, green).

As the second example, a CHB converter is chosen because of the reduced component count compared to the first architecture. The H-bridges are connected to DABs in the isolation stage as shown in Fig. 2.11. There is no MVDC link access in the architecture and the connection of DC grids can only be done in the LVDC link. Both topologies utilize the modularity in the medium voltage side and the isolation stage with series connected power converters. As a central difference to the first architecture, the power processed by a CHB cell needs to be processed by its corresponding cell in the isolation stage. Because of this, the cells in the isolation stage have to have the same voltage and current rating as in the MV side. Affected by the direct connection of the cells, the isolation stage can be unloaded by a suitable modulation of the CHB converter [64]. For the MMC based architecture, there is no comparable opportunity since the DC-link voltage needs to be shared by the converters in the isolation stage and consequently, they need to transfer the same current.

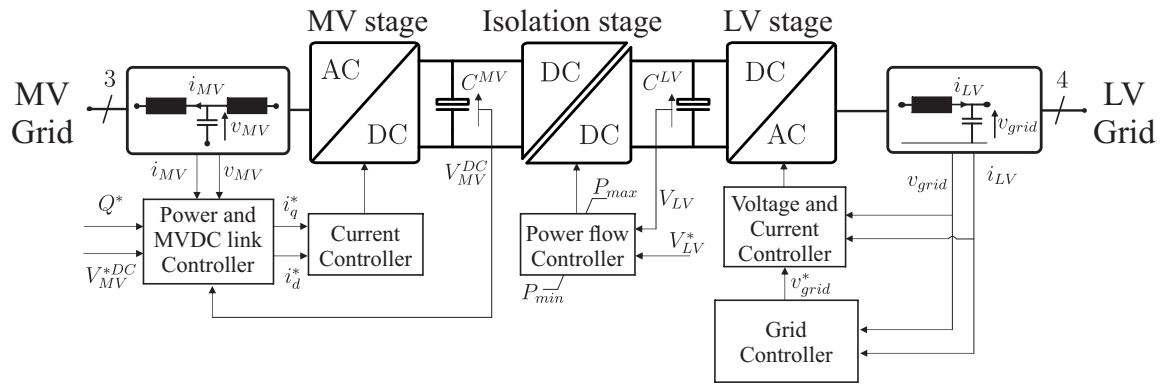


Figure 2.12: Three-stage ST and the proposed control scheme

## 2.4 Control of the modular ST

The control of the ST can be implemented almost independently from the chosen topology. The proposed controller diagram for the three-stage ST is shown in Fig. 2.12. The priority of the control is given to the LV stage of the ST, which generates the grid voltage in the LV grid in order to supply power to the loads. By generating this voltage, the ST enables to shape the amplitude and the frequency of the grid voltage. The reference values are generated by a grid-shaping controller and can be used in order to provide ancillary services to the LV grid. For instance, the frequency can be controlled to influence the droop control of the connected generators [8]. In the cited work, this has been used to prevent reverse power flow in a grid. This is beneficial in case that the voltage drop of the reverse power flow, which is also reversing, would violate the voltage limits defined in the grid codes. Remarkably, solely the load connected to the grid determines the amplitude and the shape of the current waveform.

The DC/DC converter in the isolation stage of the ST adapts the voltage level from MV to LV and controls the voltage of the LVDC link by exchanging the power that has been consumed by the loads or generated by the sources in the grid. Therefore, the MV stage of the ST needs to control the MVDC link voltage, which is done with a current controller. Similar to the LV stage, the MV stage can provide ancillary services to the MVAC grid, by providing voltage support by means of reactive current injection.

The controller design of the three-stage ST is challenging because of the communication for the mandatory synchronization between the different stages and cells. At the same time, high bandwidth is desired for the controller, which is a conflicting goal. For this reason, it needs to be defined, if a centralized controller or decentralized controller of the converter is designed. As a reported solution from literature, the SST in [65] has been designed with a DSP performing the overall control and FPGAs for cell level implementation. A big challenge for this system is the minimization of the communication infrastructure by also ensuring the reliability of the operation. As a solution applied in [66], the controller cells are combined with graph theory and a fault tolerant controller is designed with the capability to reconfigure itself.

## 3 Reliability in Power Electronics

There is no consensus about a universal definition of reliability. When referring to reliability, a future behavior and performance of a system is addressed, which holds uncertainty. However, in this work, the definition of [67] is used, which is defining reliability to be the ability of a product or a system to perform as intended for a specific time in its life cycle. This gives high flexibility for the definition of the functionality and the time in operation, but it requires knowledge about the related operation conditions. The reliability of a system is significantly dependent on its design, therefore the sizing, and the quality of the components. It is assumed, that good quality and bigger size are associated with higher costs, whereas a cost effective system design is another target. The resulting challenge is to find the compromise between these targets.

In the following section, the most recently failing devices in power electronic converters are identified and their potential failures are traced back to the reported failure mechanisms. The most frequently failing components are found to be the power semiconductors and thermal stress is identified to be the most relevant stressor. This is examined in the following along with the fundamentals to perform thermal stress analysis.

### 3.1 Reliability and failures in power converters

#### 3.1.1 Most frequently failing components in power converters

Power converters consist of several components, which can possibly fail. In order to identify the most frequently failing components, a survey was made in [11]. This survey identified the power semiconductors to be the component with the highest probability for a failure. Beside the power semiconductors, capacitors and gate drivers were listed among the three most fragile components. Others reported failing components in the survey are connectors, PCBs, inductors, resistors and fuses.

In order to understand and prevent failures, the physics of failure approach needs to be applied [68, 69]. This requires identifying for each component the physical mechanism and the stressor, which is leading to wear out. The real operating conditions need to be emulated by means of a mission profile to analyze the influence of this stressor. For power semiconductors, the most relevant failure mechanisms are related to power cycling and thermal cycling [12].

Capacitors are the second most fragile components, which also undergo thermal stress [70]. Because of a very large thermal capacitance of the hot spots in the capacitors, these thermal effects require relatively long time and can usually only be affected by permanent influences, e.g. harmonics in the grid. Consequently, the failure mechanism of the capacitors and the power semiconductors have different influencing factors and a separate analysis is required. Since power semiconductors have been found to be the most frequently failing components

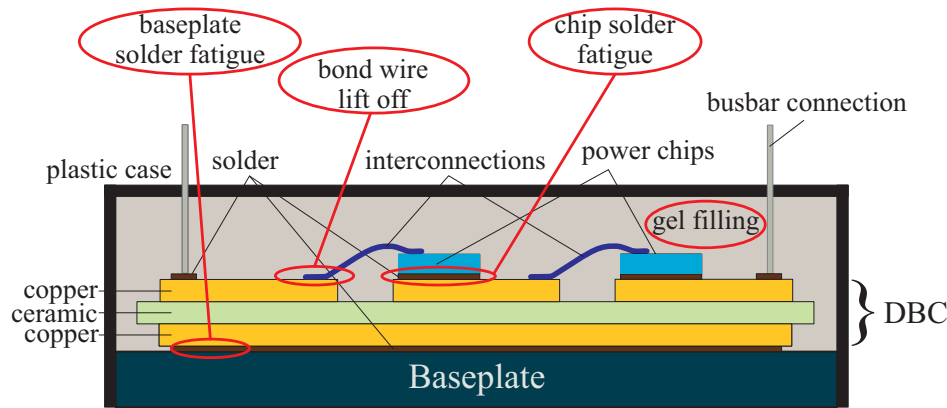


Figure 3.1: Structure of a power module and common failures.

and their sensitivity to fast varying conditions is much higher compared to the sensitivity of capacitors, this work focuses on power semiconductors.

### 3.1.2 Failure mechanisms in IGBT modules

Failures in power modules influence security in operation and cause downtime, giving extra cost for the operators of the system. To limit the increase in costs caused by bad quality, the root causes of the failures need to be understood. In the 1950s, the first relations between the plastic strain amplitude and the number of cycles to failure were established by Coffin and Manson in studies on fatigue in material science caused by cyclic plastic deformations [71]. Since all materials expand and shrink due to thermal cycles, nowadays modified relationships are also used to estimate the capability of power semiconductors to withstand thermal cycles. Because of the different coefficients of thermal expansion within the commonly used Direct Bonded Copper (DBC) structure of the power electronic modules, a variation of the temperature causes mechanical stress. Fig. 3.1 shows a schematic structure of a power electronic module, where the parts more susceptible to thermal cycling are highlighted in red. The common failures in power electronic modules are found at the bond wires and the interconnections within the modules, namely chip solder, base plate solder and bond wire liftoff. Since mechanisms, which cause the wear out are based on the temperature swing, the thermal swing needs to be separated from the temperature profile. A common way to do is to apply thermal cycle counting, such as Rainflow counting. From the counted cycles, there are models to derive the thermal stress and the accumulated damage. One of the models taking into account this failure mechanism is the LESIT lifetime model based on the accelerated tests of IGBT modules leading to solder fatigue [72]. The data is only available for limited thermal swings between  $\Delta T = 30\text{ K}$  and  $\Delta T = 80\text{ K}$ , but in this work the range is extrapolated to smaller magnitudes. Furthermore, the technology has proceeded and there are new IGBT technologies, which are having higher thermal cycling capability. Nevertheless, the failure mechanisms and the dependence on the temperature swing remains [12].

In order to increase lifetime and reliability of power electronic modules, improvements in the connection technology and assembly of the modules have been achieved. Sintering, also



low temperature joining, instead of soldering the chips is used to increase robustness of the connections and bonds are replaced by pressure contacts in high reliability product lines [73]. Delamination of the substrate can be reduced by avoiding 90° angles on the pattern [74] and other strategies try to optimize the cooling system [75]. Danfoss is using a cooling concept defined "ShowerPower" to homogeneously cool the base plate of power modules and thereby eliminate temperature gradients of the cooling medium. Therefore, the coolant's path along the module is designed to cool all chips to their specific needs.

Other failures can be affected by moisture [76], vibration [77] and cosmic rays [78, 79]. Their influence on the lifetime of the system can be dominant, but a combination of different failure mechanisms is out of the scope of this work. In the following, only failures affected by thermal cycling are addressed.

### 3.1.3 Lifetime modeling of power electronic modules

Manufacturers and operators of power electronic modules share the interest to estimate the impact of certain usage on the lifetime of the modules [11]. The lifetime of a system is an important parameter, as cost calculations for purchase, maintenance and replacement depend on it. The aim of a lifetime prediction is to investigate over which time interval a module can be used without expecting to see a failure for a particular application.

Based on this, a well-known approach to estimate the module's lifetime is the Coffin-Manson-Arrhenius model [10]: The number of cycles to failure  $N_f$  is described in dependency of the amplitude of thermal cycles  $\Delta T_j$  and the average temperature  $T_{j,av}$ . Other coefficients  $a_1$ ,  $n$  and  $a_3$  are extracted from a data set of multiple reliability experiments and they are adjusted for best match to the module [73]. Its analytical equation is:

$$N_f = a_1 (\Delta T)^n \cdot e^{\frac{a_3}{T_{j,av}}} \quad (3.1)$$

Other researchers have modified this relationship, recognizing for instance the frequency of thermal cycles, heating and cooling times as well as more electrical variables. An example for an empirically obtained model from accelerated lifetime tests of power modules with different current and voltage rating is the Bayerer model, which includes the turn on time of the IGBT  $t_{on}$  and the current rating  $I$  of the power semiconductors [80].

$$N_{f1} = a_1 (\Delta T)^n \cdot e^{\left(\frac{a_3}{T_{j,av}}\right)} \cdot t_{on}^{a_4} \cdot I^{a_5} \quad (3.2)$$

Manufacturers of semiconductors use the relationship of (3.1) to express the thermal cycling capability of their modules. Fig. 3.2 shows this for a Semikron module with coefficients matched to IGBT4 modules. It can be seen that compared to the thermal cycle amplitude the average temperature has only a slight impact on the lifetime. This approach gives an indication for the impact of different parameters on power electronic modules thermal cycling capability. These temperature cycles cause the strain, which is hard to measure during

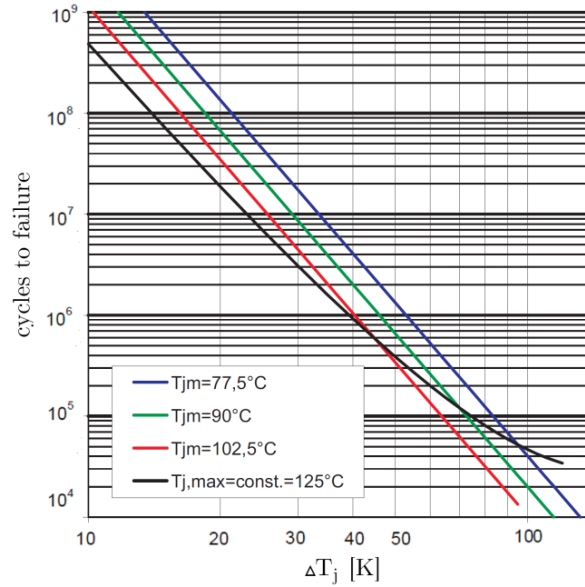


Figure 3.2: Power cycling capability for a Semikron IGBT module [73].

operation and cause the wear out [81]. However, the model is not sufficient to make a statement about the lifetime of a module in a specific application assigned to a specific mission profile [82]. To rate the impact of a certain mission profile on the module's lifetime, first a temperature profile is created from the power profile, calculating the losses of the semiconductors, thermal related characteristics and environmental influences. As it can be seen in the lifetime models of (3.1) and (3.2), the equations only indicate a singular magnitude of thermal cycles,  $\Delta T$ . In contrast to this, the power semiconductors in operation undergo thermal cycles, which are superimposing each other. The common approach is to apply linear damage accumulation with Miner's rule [83]. The Miner's rule is written as:

$$C = \sum_{i=0}^{\text{inf}} \frac{n_i}{N_i} \leq 1 \quad (3.3)$$

Here  $C$  is the cumulative damage of the device,  $n_i$  the number of detected cycles in the stress range  $i$  and  $N_i$  the number of cycles to failure in the  $i$ -th stress range. Thus, the cumulative damage will rise with the number of thermal cycles in the mission profile. If the cumulative damage reaches 1, the module has reached its failure criteria according to the model [84]. Other models for acceleration factors exist, regarding more parameters to the investigated failure mechanism and can be found in [74]. However, this will not be analyzed deeper, because it is not the focus of this work.

To obtain the thermal cycling characteristics, it is necessary to perform an End Of Life (EOL) test by experiment. This requires using high magnitude of thermal cycles to obtain results within a reasonable amount of time. If a period of 30s is assumed for a thermal cycle, a conventional test would take about ten years to fulfill  $10^7$  cycles, which may not even be enough to reach EOL for the module depending on the test parameters. Therefore, a time acceleration factor  $f_a$  is introduced, in order to carry out a test in shorter time, but

Table 3.1: Different  $B_x$  lifetimes normed on the  $B_{10}$  lifetime.

Failure probability $x$ [%]	1	5	10	25	50	75	90	95	99
Lifetime expectation $B_x$ normed on $B_{10}$	0.46	0.79	1	1.40	1.87	2.36	2.80	3.05	3.52

higher stress having the same impact to the modules lifetime [85]. All thermal cycles in a temperature profile  $\Delta T_{op}$  are converted to a corresponding amount of thermal cycles with an appropriate amplitude for the experiment  $\Delta T_{test}$ . The Coffin-Manson acceleration factor definition, where  $c_a$  the fatigue ductility, is given as [74]:

$$f_a = \left( \frac{\Delta T_{op}}{\Delta T_{test}} \right)^{c_a} \quad (3.4)$$

Despite the testing to the EOL most devices will not be destroyed, but reach a predefined failure criteria (e.g. a certain increase of  $V_{ce}$ ). Several devices need to be tested, because the lifetime of all components does have a standard deviation and even if components come from a similar batch and undergo similar stress, they are still expected to fail after different times in operation. A statistical method, which is considering this, is the Weibull distribution. It is commonly used, since most of the available lifetime models derive the lifetime with a 10 % failure probability, referring to the  $B_{10}$  lifetime. The Weibull probability density function is expressed in (3.5), where  $F(t)$  is the failure probability at the time  $t$  and the fitting parameters  $\Theta$  and  $\beta$ .

$$F(t) = 1 - e^{-\left(\frac{t}{\Theta}\right)^\beta} \quad (3.5)$$

Remarkably,  $\beta < 1$  models early failures, whereas for  $\beta = 0$  the function is modeling a constant failure rate, representing random failures. The wear out related failures are modeled with  $\beta > 1$  and since power electronics are undergoing aging before their failure,  $\beta = 3$  is set. Of course  $\beta$  is dependent on the design of the singular components as well as the whole system. Nevertheless, it is modeling the variance of the time to failure. Based on this function, the  $x^{th}$  quartile  $B_x$  can be derived, which corresponds to the expected lifetime under the failure probability of  $x$ .

$$B_x = \Theta \left( -\ln(1-x) \right)^{\frac{1}{\beta}} \quad (3.6)$$

To point out the effect of different failure probabilities as modeled with (3.6), the results of the lifetime expectation are normed on the  $B_{10}$  lifetime of the system and presented in table 3.1. Based on the parametrization of the Weibull distribution function, for a failure probability of 1%, the expected lifetime is  $B_1 = 0.46 \cdot B_{10}$ . In the opposite way, a higher failure probability increases the lifetime, e.g. the failure probability  $B_{99} = 3.52 \cdot B_{10}$ . Expressed in other words, the time until the converter has failed with a probability of 1 % is approximately less than half the time until the converter has a failure probability of 10 %.

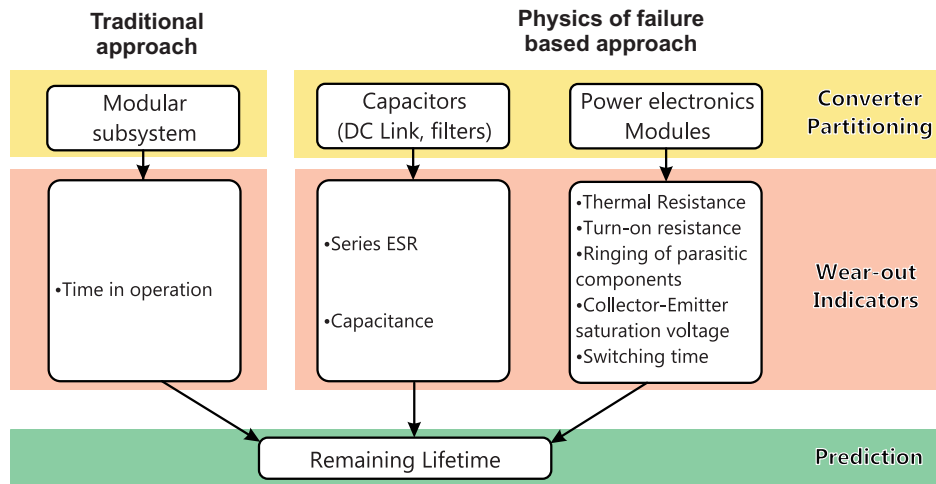


Figure 3.3: Condition monitoring for power electronic converters.

Instead of using a model-based approach, another possibility to detect the aging of a device during operation is the measurement of a physical parameter, which is correlating with aging. This is referred to as condition monitoring and is addressed in the next subsection.

### 3.2 Condition monitoring in power electronics

Condition monitoring is the process of monitoring parameters, which could allow observing the degradation of a system's components. In combination with health prognostics, this enables to schedule maintenance and replacements before a component fails and thus prevents down times of a system. In the field of power systems, condition monitoring is well known and used to monitor the health of transformers, induction machines and On Load Tap Changers [86]. The concept has further been applied for health monitoring in power electronic converters as shown in Fig. 3.3. Here, the system is systematically grouped into smaller parts to enable the desired model precision in the estimation of the remaining lifetime. The simplest form is to measure the time in operation with the assumption that the oldest subsystem fails first.

As pointed out before, critical components for power converters are capacitors and power semiconductors. Condition monitoring for electrolytic capacitors is possible by monitoring the Equivalent Series Resistance (ESR) and the capacitance, which can be implemented for real time application [87]. For power semiconductors, condition monitoring is challenging, because of the various possible failure mechanisms and the various possible parameters. One of the challenges is to separate the correlation of these parameters with other states, such as the current or the junction temperature.

In [88], it is suggested to monitor the junction temperature with Thermo-Sensitive Electrical Parameters (TSEP) (e.g. the collector emitter saturation voltage of an IGBT  $v_{ce}$ , the MOSFET's turn on resistance  $R_{ds,on}$ , the thermal resistance, gate signals and switching times). As an example, the collector-emitter voltage  $v_{ce}$  is observed for bond wire lift-off [89]. However,  $v_{ce}$  is also sensitive to the applied power level and changes of the temperature. A method

to detect degradation of the solder joints is given in [90]. The stressed material joints lose their capabilities in heat transfer, leading to non-uniformities in the heat distribution in the module. These can be detected by measurements at multiple positions on the substrate. The TSEP hold the advantage, that most wear out based failure mechanisms can be led back to the influence of the junction temperature.

Further investigated approaches observe the output harmonic identification for condition monitoring [91] or monitor the case temperature of different power semiconductors during accelerated lifetime tests [92]. Another interesting approach is to use the PWM pattern as excitation voltage to observe the health [93]. The work studies the ringing of the resonant circuit composed by the IGBT parasitic capacitors and the circuit inductance and allows detecting an increase of the damping factor with aging. In combination with a band-pass filter tuned at the ringing frequency, this can be used as a diagnostic signal to assess the power module's conditions. A comprehensive work including the condition monitoring and prognostics for the lifetime of power semiconductors has been made in [82]. The work demonstrates a lifetime estimation technique based on accelerated lifetime tests.

All approaches hold different advantages and disadvantages without an overall optimal choice [94]. To correlate the variation of the monitored parameter with the lifetime, a failure criterion needs to be set to define the EOL. This criterion will have a standard deviation for the different components and different technologies, challenging the precision of the prediction. In combination with the physics-of-failure approach, this problem has recently been reviewed for IGBTs by also highlighting the failure modes observed in literature for accelerated lifetime tests [95]. One of the requirements pointed out in the review is to perform the condition monitoring without impact on the normal operation.

### **3.3 Thermal modeling and power semiconductor losses**

Based on the operating conditions, design and control methods for each stage of the ST, the junction temperature of the power semiconductors can be simulated with proper loss and thermal models. In the following, thermal modeling and loss modeling in power electronics are introduced with the target to provide tools for the thermal stress analysis.

#### **3.3.1 Thermal modeling in power electronics**

As shown in the lifetime models for power semiconductors, the junction temperature is affecting the reliability of the system. Unfortunately, modeling the junction temperature variations in real time is challenging, because the physical behavior is based on the three dimensional heat transfer. This can be done with Finite Element Analysis (FEA) and requires knowledge about all materials in the module and their thickness. Regrettably, the manufacturer consider this information to be confidential and do not provide it, which increases the uncertainty of the thermal model. Furthermore, the model obtained from FEA is a high order

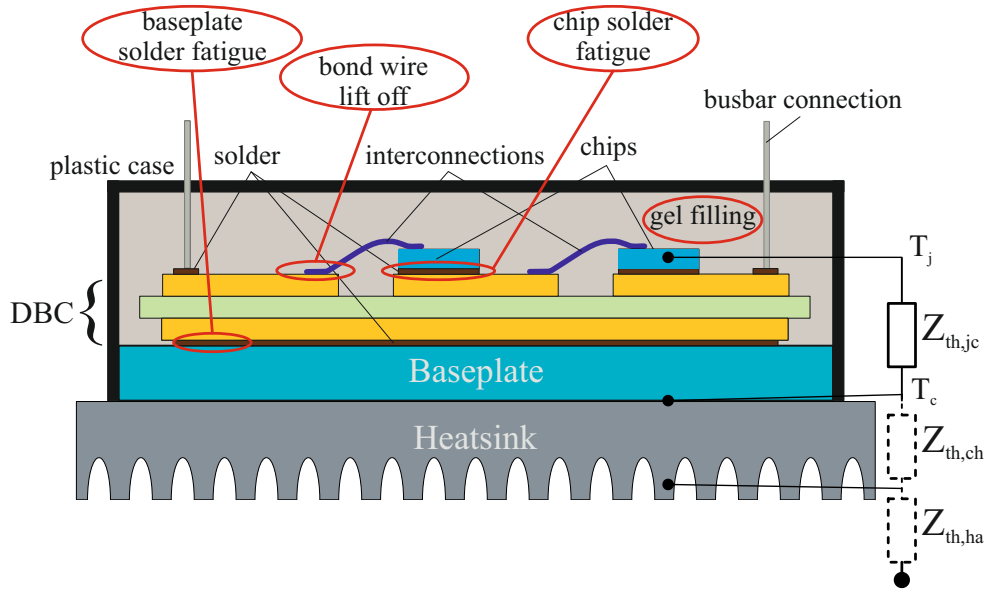


Figure 3.4: Failures of power electronic modules and schematic thermal impedance.

differential equation. The complexity of this equation can be reduced with approximations, but they are still impractical for the application in real time.

An opportunity to model the thermal behavior of the power semiconductors with reduced complexity is to model a reduced number of heat transfer paths inside the module. This is possible, because the dominant heat transfer goes from the chip to the baseplate of the module. The potential second heat transfer path takes into account the thermal conduction on the surface of the module, also including the cross coupling of the chips between each other's. FEA can also be applied to obtain the parameters of the model, but the parameter uncertainties remain. The single heat transfer paths brings the advantage of a much simpler model, while still modeling the dominant heat transfer path. As an alternative to FEA, the parametrization of this model can be done by measuring the heating up/cooling down curve. This overcomes the disadvantages of the model based on FEA, but compromises the potential accuracy of the model. The simple model based on the single heat transfer path is commonly used in the datasheet of the manufacturer. It is mathematically shown in (3.7), where the junction temperature  $T_j$  is derived as the sum of the case temperature  $T_c$  and the convolution of the thermal impedance between junction and case  $Z_{th,jc}$  and the losses  $P_{loss}$ .

$$T_j(t) = Z_{th,jc}(t) * P_{loss}(t) + T_c(t) \quad (3.7)$$

In Fig. 3.4, the scheme of a power electronic module is extended with the thermal impedance between junction to case,  $Z_{th,jc}$ , the thermal impedance case to heat sink  $Z_{th,ch}$  and the thermal impedance between heat sink and ambient  $Z_{th,ha}$ .

The thermal impedance  $Z_{th,jc}$  can be modeled with thermal resistors  $R_{th}$  and thermal capacitors  $C_{th}$ . In the model, the thermal resistance is commonly considered to be constant, even if it is slowly increasing over the lifetime of the power semiconductor and indicates the aging.

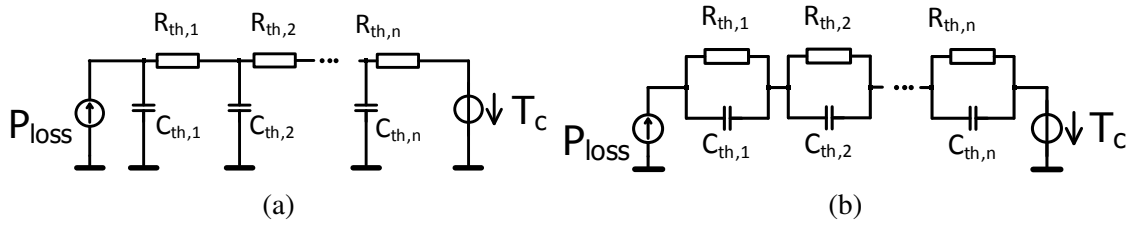


Figure 3.5: Equivalent electrical circuit representing the thermal impedance  $Z_{th,jc}$ : (a) Cauer circuit, (b) Foster circuit.

Thus, based on the models, the ambient temperature and the losses are the only parameters, which are varying and actively affect a thermal swing. The ambient temperature usually varies slowly while the losses vary in dependence of the mission profile.

In case that the impedance is obtained by FEM, the Cauer network shown in Fig. 3.5 (a) is usually used. Each chain link represents a layer of the module and is calculated based on the physical material properties. Therefore, the Cauer network has a physical background. However, beside the effort to be made for the modeling, the materials and the thickness of the layers are generally not provided by the manufacturer, which makes these models based on FEA not practical. As an alternative, the thermal impedances can be obtained from fitting the measured cooling down curves. This cooling curve is fit to the thermal impedance of a Foster network shown in Fig. 3.5 (b). The series connected RC chains are represented with (3.8).

$$Z_{th(jc)}(t) = \sum_{v=1}^n R_{thv} \cdot (1 - e^{-\frac{t}{\tau_{thv}}}) \quad (3.8)$$

There is the possibility to transform a Foster network into a Cauer network, but the transformation implies the deprivation of the physical background. In many cases, the Foster network parameters are actually provided by the manufacturer in the datasheet. For both, Cauer and Foster networks, the number of chain links is arbitrary. More chain links increase the precision of the model with the downside of higher complexity.

Unfortunately, the simple combination of impedances, e.g. the thermal impedances of the module and the heat sink, causes errors, even if both models are provided by the manufacturer. At least the thermal grease needs to be taken into account for obtaining the overall thermal resistance, whereas the dynamic behavior is generally difficult to model with datasheet information [96]. In addition, the influence of a potentially available fan is changing the thermal impedance, which is causing high errors in models, which assume the thermal impedance to be constant.

### 3.3.2 Modeling of power semiconductor losses in this thesis

The introduced thermal models all have in common to require the losses of the power semiconductors as an input parameter. For this purpose, the driving losses and the blocking losses

are commonly neglected and only the conduction and the switching losses are taken into account. The loss model are following the principle of [97], which is a commonly accepted method for the loss evaluation of power semiconductor devices. The switching losses can be divided in the turn on  $P_{sw,on}$  and the turn off losses  $P_{sw,off}$  as expressed with (3.9).

$$P_{loss}(t) = P_{con} + P_{sw,on} + P_{sw,off} \quad (3.9)$$

The losses are derived based on the electrical parameters like the collector current  $I$ , the blocking voltage  $V_{dc}$ , the modulation index  $m$  and the switching frequency  $f_{sw}$ . The turn on losses  $P_{sw,on}$  are approximated with (3.10) and the turn off losses  $P_{sw,off}$  are approximated with (3.11).

$$P_{sw,on} = f_{sw} \cdot E_{on} \cdot \left( \frac{I}{I_{ref}} \right)^{K_{I,on}} \cdot \left( \frac{V_{dc}}{V_{ref}} \right)^{K_{V,on}} \quad (3.10)$$

$$P_{sw,off} = f_{sw} \cdot E_{off} \cdot \left( \frac{I}{I_{ref}} \right)^{K_{I,off}} \cdot \left( \frac{V_{dc}}{V_{ref}} \right)^{K_{V,off}} \quad (3.11)$$

In the equations  $I_{ref}$  and  $V_{ref}$  are the values for which  $E_{on}$  and  $E_{off}$  are provided in the datasheet of the manufacturer.  $K_{I,on}$ ,  $K_{V,on}$ ,  $K_{I,off}$  and  $K_{V,off}$  are the exponents that allows scaling the losses to voltages or currents different than the reference ones. The conduction losses are linearized for IGBTs with the constant voltage drop  $v_{ce0}$  and the resistance  $r_{ce}$  (3.12).

$$P_{con} = v_{ce0} \cdot I + r_{ce} \cdot I^2 \quad (3.12)$$

Thus, the losses of the converter depend on the choice of the power semiconductors and their characteristics. Additionally, the loading and the control of the converter influence the losses, consequent the junction temperature. These equations can be used to derive the losses of various converter topologies, e.g. a two level converter [73].



## 4 Thermal stress analysis for the ST

During operation of the ST, the power semiconductors undergo thermal cycling with different magnitudes and average junction temperatures. The power cycling tests of the manufacturers instead only test single magnitudes of thermal cycles under specific average temperatures until their failure criteria is reached. With the target to obtain realistic lifetime expectations for the ST, this section develops a mission profile for the ST by superposing different conditions, which affect thermal stress for the power semiconductors. The developed mission profile is used to extrapolate the behavior during the full year and a comparison is made how the thermal stress is affecting the different stages of the ST. A thermal de-rating strategy is proposed with the target to obtain a design for the three stages, with has similar lifetime expectations.

### 4.1 Stress identification and mission profile analysis

#### 4.1.1 Possible stressors for the ST

The ST undergoes power flow variations, which are caused by the variation of the load and the power generation in the connected grid feeders. These power variations are affecting the junction temperature of the components and cause thermal stress for the power semiconductors. Beside the power cycling, variations in the grid voltage affect the operation of the ST and can even lead to a disconnection of the ST to prevent its damage. These grid voltage variations can occur in the medium voltage grid side or the low voltage grid side of the ST and affect only the stage of the ST, which is connected to this grid. Particularly, the increased penetration of renewables has led to an increment of disturbances in the grid in the last years. These are overvoltages, voltage variations due to faults or fast power variations (e.g., generator disconnection), harmonics, higher short circuit currents and flickers. The voltage variations are causing a variation in the current of the ST, because it is behaving like a constant power load by controlling the LVAC grid voltage. Thus, a voltage sag forces the ST to increase the output current to maintain constant power transfer with the LV grid. Of course, this effect is highly dependent on the depth of the voltage sag, possibly leading to the disconnection of the ST from the grid, which is why this point is discussed in the following.

The magnitude of a voltage variation is corresponding to the response of the grid to a grid fault. It is dependent on several influencing factors, such as the nature of the fault (number of phases, short circuit, ground fault), the grid composition and the location of the fault. Over-voltage or undervoltage conditions can be caused by the fault in each phase, depending on the grounding adopted in the grid [98]. A well-earthed neutral system leads to high short circuit currents, which is limiting the overvoltages, but it requires the installation of big short circuit breakers. This is usually adopted in High Voltage (HV) transmission grids. In ungrounded systems, a temporary overvoltage (until 2.5 – 3 pu) can occur during a single-phase fault contingency [99]. If the system is grounded by means of a Petersen coil or a suppression coil

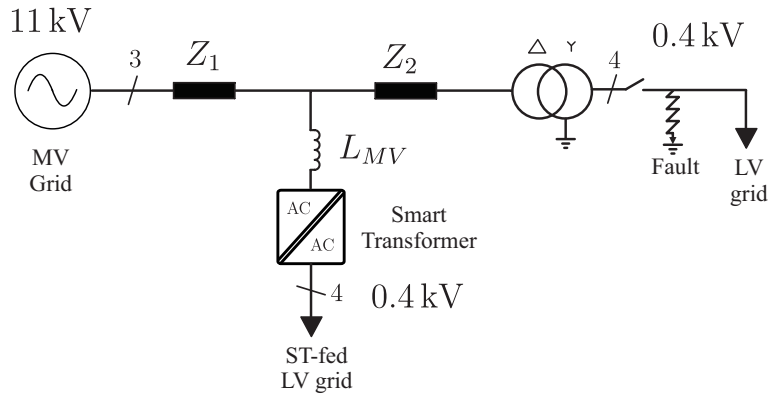


Figure 4.1: Investigated MV grid with an ST feeding a LV grid and a feeder connected by a traditional transformers

(e.g. in Germany), the overvoltage can be reduced to 1.8 pu. For the power semiconductors overvoltages need to be limited in magnitude, because exceeding the rated collector emitter voltage causes immediate destruction of the device. Undervoltages can also occur during a fault. As observed in [100], the junction temperature of power semiconductor components can increase significantly with the magnitude of the voltage dip. The temperature depends also on the type of fault (single-, two- or three-phase fault). Providing services, like the reactive power injection, for voltage support can affect the lifetime of the components. As shown in [101], the injection of reactive power increases the thermal cycling of each component, increasing the losses and influencing the lifetime of the devices.

#### 4.1.2 Description of the investigated grid

For simulating the thermal stress of an ST in the distribution grid, it is considered to link an AC microgrid with a MV grid as shown in Fig. 4.1. The power of the investigated feeder is 1 MVA, whereas the ST is sized as described in Table 2.7. The ST is located in a distance of 2 km to the feeder of the MV grid and another LV grid is connected to the same MV feeder by a conventional transformer in a distance of 1 km to the ST.

The LV grid, which is fed by the ST, is composed of connected photovoltaic power generation (PV), wind power generation and loads. It is assumed that the MV side converter does not generate reactive power for the MV grid and operates with  $\cos(\varphi) = 1$ , while the LV side converter of the ST is providing reactive power for the LV grid. In contrast to the traditional transformer, the reactive power in the LV is provided by the LV side of the ST without affecting the MV-side converter of the ST. Remarkably, the traditional transformer needs to absorb the reactive power from the MV line and thus reduces the power factor in the MV lines. The ST instead provides the reactive power locally and can absorb power with unity power factor from the MV grid.

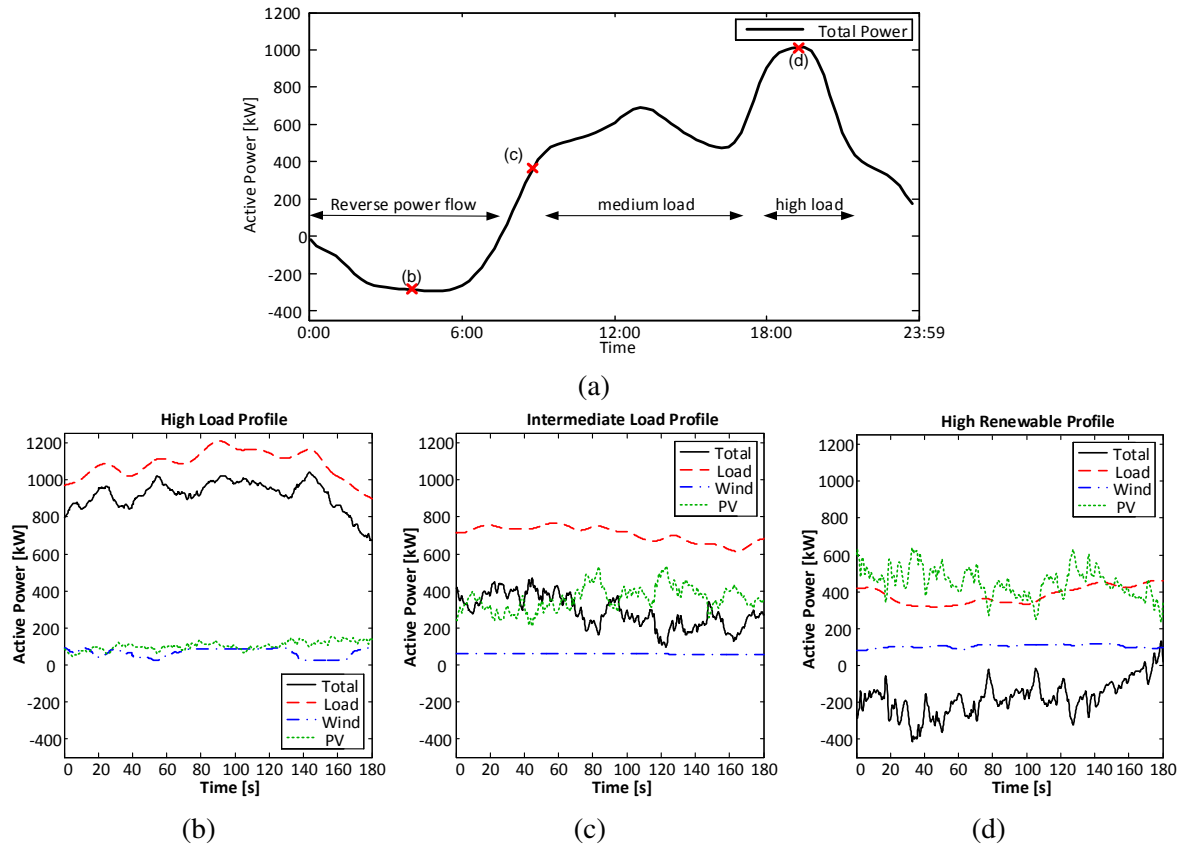


Figure 4.2: Load Profile for the study with active power in a grid: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

#### 4.1.3 Power variations in the mission profile

For the ST in the distribution system, it is expected, that there are recurring power cycles with different periodicity, such as daily, weekly or yearly. As a study case, a daily power profile is shown in Fig. 4.2 (a) for the ST fed microgrid in Fig. 4.1. Because of the power generation in the grid, the power flow can be bidirectional, which is changing the stress distribution between the power semiconductors. The first scenario shown in Fig. 4.2 (b) is characterized by high power consumption of the loads in the LV grid and low power production by the renewable power plants, which will result in high power flow from the MV grid into the LV grid. The second scenario in Fig. 4.2 (c) shows the medium power consumption by the loads and medium power generation in the LV grid. This is expected to be the loading condition of the ST for most of the time and it results in a medium power transfer from MV grid into the LV grid. The third scenario is characterized by high power production of the renewable sources in the LV side and low consumption by the connected loads of the LV grid. It results in bidirectional power flow and higher fluctuations of the power.

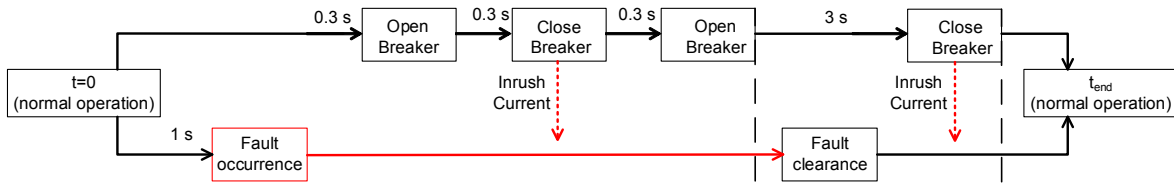


Figure 4.3: Grid reconnection procedure after a fault using the breaker in Fig. 4.1.

#### 4.1.4 Study case on a grid fault

Other stressing conditions for the power converter are the externally caused voltage variations, leading to thermal cycling. This is investigated in a study case for the power semiconductors in the MV stage of the ST during grid faults in LV feeders, which are fed by the traditional transformer. A fault in the LV grid can cause voltage sags in the MV grid, which is influencing all connected feeders. In particular, the ST is behaving like a constant power load, which increases the transferred current and thus increases the stress for the power semiconductors. In case of a deep voltage sag, the feeder needs to be disconnected to prevent the destruction of the ST. Additionally, the reconnection of the LV grid feeder after a tripped breaker causes inrush currents for the transformers. These inrush currents will stress the MV grid by injecting a zero sequence current with a magnitude, which can be several times higher than the nominal current [102]. Due to the limited overloading capability of power semiconductors, this case is studied for the three-phase short circuit in the LV grid fed by the traditional transformer. A three-phase short circuit in the LV grid does not have the highest probability, but the biggest impact on the grid in terms of voltage sags. For this reason, it is taken as the worst study case to demonstrate the influence of faults in feeders of the ST connected to the same grid. The position of the fault occurrence is shown in Fig. 4.1.

The disconnection and reconnection procedure of this transformer after a fault is visualized in Fig. 4.3. In this study, the fault occurs after  $1\text{ s}$  of the simulation and  $0.3\text{ s}$  later the breaker is activated. After additional  $0.3\text{ s}$ , the breaker is closed to test if the fault is cleared. This closing induces an inrush current in the transformer of the reconnected grid, because it is not magnetized. However, due to the uncleared fault, the breaker reopens after  $0.3\text{ s}$  and reopens again after  $3\text{ s}$  to test if the fault is cleared. In the meantime, the fault is cleared. Thus, the breaker is closed, which is causing another inrush current in the transformer and then the grid is back to normal operation.

The fault in the connected feeder influences the current and voltage profiles of the ST. During faults, the impedance of the transformer and the stiffness of the MV grid determine the short circuit current. This short circuit current is causing a voltage drop on the transformer and causes a voltage dip in the MV grid before the breaker opens. Since the ST is behaving like a constant power load, which is different with respect to the traditional transformer, the current on the MMC (as shown in Fig. 4.4) is increasing. The characteristic behavior of the grid voltage and current during the three-phase short circuit is presented in Fig. 4.5. In Fig. 4.5 (a) the MV side ST voltage and current during the investigated grid fault are shown. In this case, the ST is behaving like a constant power load, but does not actively

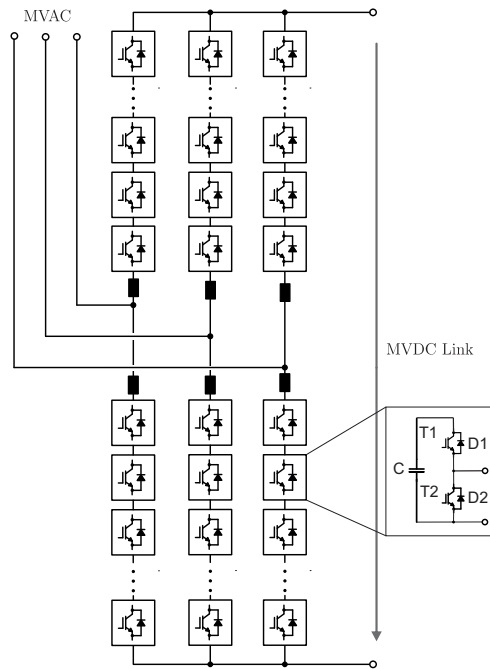


Figure 4.4: Modular Multilevel Converter (MMC) topology.

react on the fault. Instead, it is still feeding the LV grid feeder and the current is increased because of the drop in voltage. Instead, in Fig. 4.5 (b), the ST is injecting reactive current to support the grid voltage, which results in a higher output current of the ST. This higher output current is expected to cause higher losses and thus higher thermal stress for the power semiconductors.

## 4.2 Thermal stress analysis for the MV stage

In the following, the MMC is considered for the MV stage of the ST. The electrical and thermal design is similar to the MMC in section 2.3.2 and it is used to evaluate the thermal stress during the introduced mission profile and the grid fault. The conditions are extrapolated and superposed to obtain a yearly mission profile. With the resulting lifetime expectation, a method is introduced and applied for the optimization of the thermal design for a predefined lifetime.

### 4.2.1 Short term power variations

For the thermal stress analysis during short-term power variations, the three mission profiles shown in Fig. 4.2 are simulated with the thermal model from [103] to emulate the operating conditions. In Fig. 4.6 the junction temperature of all power semiconductors in one half bridge are shown. These temperature profiles are similar for the power semiconductors in the other half bridge cells in the MMC converter, because a PWM is used. The first profile leads to junction temperatures between 60 °C and 85 °C. The IGBT T1 and the diode D1 in the half bridge cell are the most stressed devices in this condition and the maximum junction

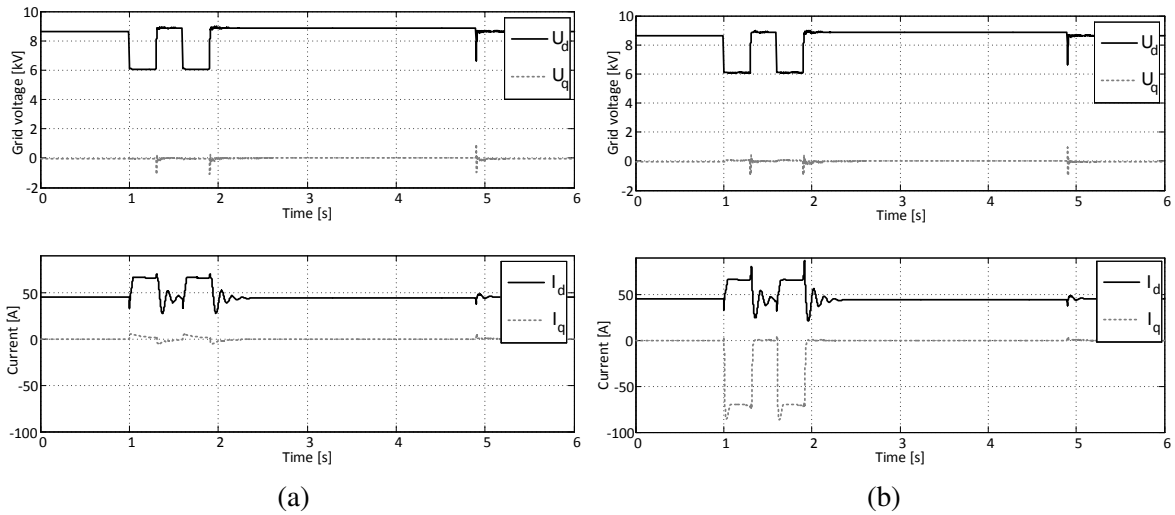


Figure 4.5: Current and voltage profile of the ST during a three-phase MV grid fault and reconnection procedure: (a) for normal ST operation, (b) for reactive current injection.

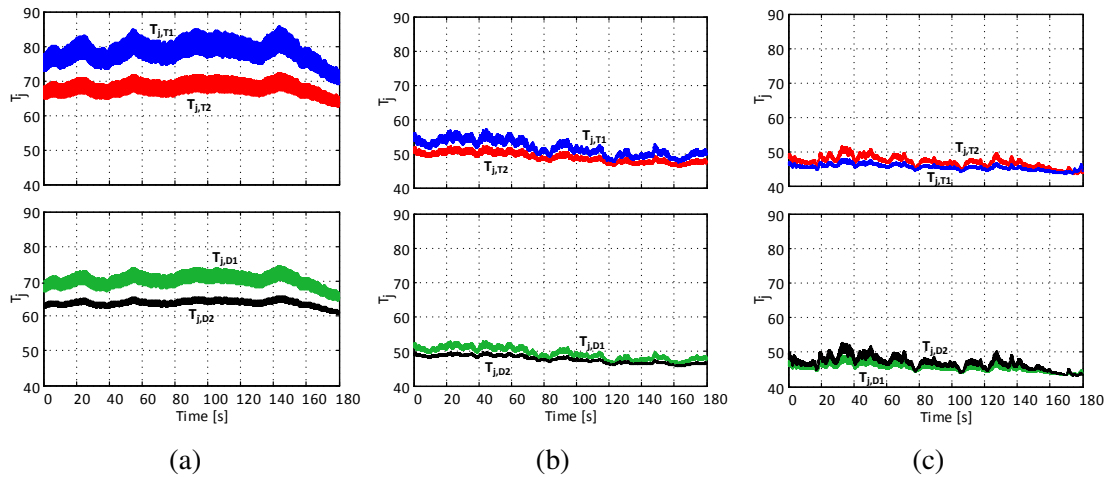


Figure 4.6: Thermal stress for the MMC during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

temperature is in accordance with the design. T1 shows a thermal swing of  $\Delta T \approx 4 K$  in the fundamental period, while T2 is stressed less with  $\Delta T \approx 3 K$ . The diodes obtain approximately the same temperature swing of  $\Delta T < 1 K$ . In the second profile (Fig. 4.2 (c)), the average temperature is remarkably reduced for all power semiconductors and the temperature swing is much lower than in the first profile. Especially the stress for the diodes D1, D2 and transistor T1 are significantly reduced. The third profile (Fig. 4.2 (d)) with reduced load and bidirectional power flow shows further reduction of the mean temperatures of T1, D1 and D2. The IGBT T2 is now more loaded than T1 and the diodes undergo higher thermal cycles than in the previous case. This is mainly caused by the high power generation of the renewable sources, which cause high power fluctuations.

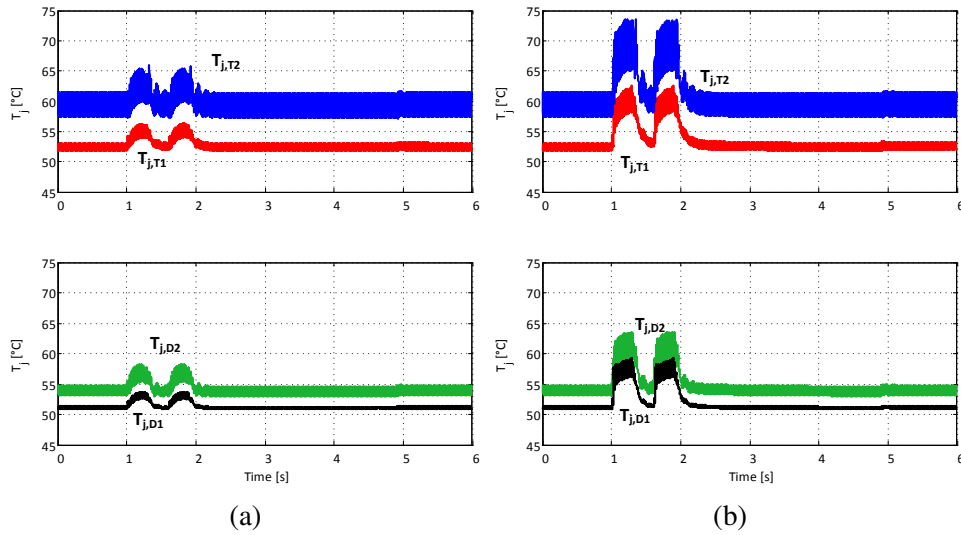


Figure 4.7: Junction temperatures of one cell during fault and reconnection procedure:(a) for normal ST operation, (b) for reactive current injection.

#### 4.2.2 Faults

The voltage and current profiles of the fault, which are shown in Fig. 4.5 are simulated to evaluate the thermal stress for the power semiconductors in this occurrence. This results in the junction temperature profiles as shown in Fig. 4.7 for the case without reactive power injection and for the case with reactive power injection. In both cases, the fault causes increased magnitude for the thermal cycles. This increased magnitude of the thermal cycles occurs during the fault and during the first closing of the breaker, when the fault is not cleared. The thermal swing is relatively low, because the time until the breaker opens is short, even in comparison to the time constants of the thermal impedance of power device and heat sink. Of course, there are situations in which the voltage in the grid is even lower than in the simulated case, but this is very rare in grids with high standards. Remarkably, the effect of the inrush currents on the ST is not even visible in the junction temperature profile of the ST.

#### 4.2.3 Damage accumulation of the short-term power variations and faults

The thermal profiles from section 4.1 are used to compute the consumed lifetime of the power semiconductors, which is also defining the lifetime of the power converter. The short-term power variations are analyzed in Fig. 4.8. Rainflow counting is applied for the IGBT T1, which is the most stressed power semiconductor in this topology. Most thermal cycles in all load conditions are generated by the fundamental frequency, which can be identified by the density of cycles with similar amplitudes. The other thermal cycles are generated by the load profile and some are visible as steps in the accumulated damage (Fig. 4.8 (b),(c)). The total consumed lifetime is the inverse of the damage correlated to the time in which this was affected. This lifetime consumption is maximum during the high load profile, whereby

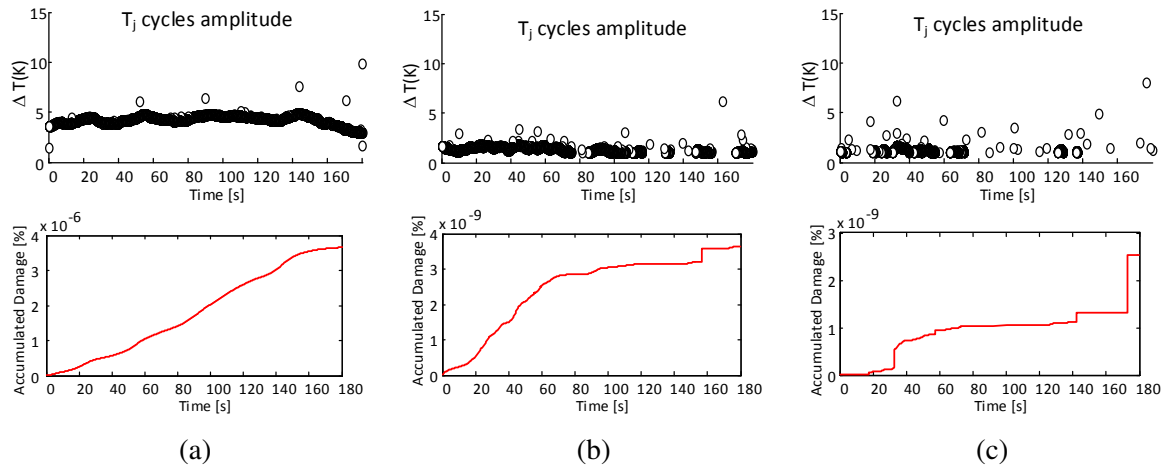


Figure 4.8: Rainflow cycle counting and accumulated damage of the bond wire for the junction temperature of T1 in the MMC during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

the others obtain almost similar consumed lifetime. Nevertheless, their consumed lifetime is much lower than the consumed lifetime of the high load profile.

The effect of the grid fault on the thermal stress for the power semiconductors is investigated in the following. To identify the magnitude of the thermal cycles during the fault, Rainflow counting is applied to the temperature profile of Fig. 4.7, which is shown in Fig. 4.9. The magnitude of the largest thermal cycles without reactive current injection is approximately  $6.5\text{ K}$ , whereby in the case with reactive current injection, the thermal swing is increased to  $8\text{ K}$ . This has limited influence on the lifetime of the ST, as it can be seen in the damage for both cases. Even if the damage for the injection of reactive current is ten times higher than in the first case, the overall damage is still low. Remarkably, the inrush currents of the reconnection procedure can neither be identified in the thermal profile of the power semiconductors nor in the Rainflow counted cycles or the damage accumulation. This leads to the conclusion, that the inrush current do not influence the lifetime of the ST in under the investigated conditions.

In the case of a blackout of the MV grid, the reconnection of the LV feeder is usually coordinated in time. Thus, it is prevented that the effects of the reconnection, such as inrush currents, are accumulating and result in high damage.

#### 4.2.4 Experimental validation of the thermal stress in the MV stage

To validate the thermal stress for the power semiconductors in an MMC cell, one MMC half bridge cell (as shown in Fig. 4.10) is used in an H-bridge setup for emulating the current profile of the power semiconductors in an MMC cell. For the evaluation, an open IGBT power module (Danfoss DP25H1200T101667-101667) is used in the setup, which requires operating the cells with reduced DC-link voltage due to the absence of the gel in the module. The junction temperature is measured with a high-speed infrared camera and the grid voltage



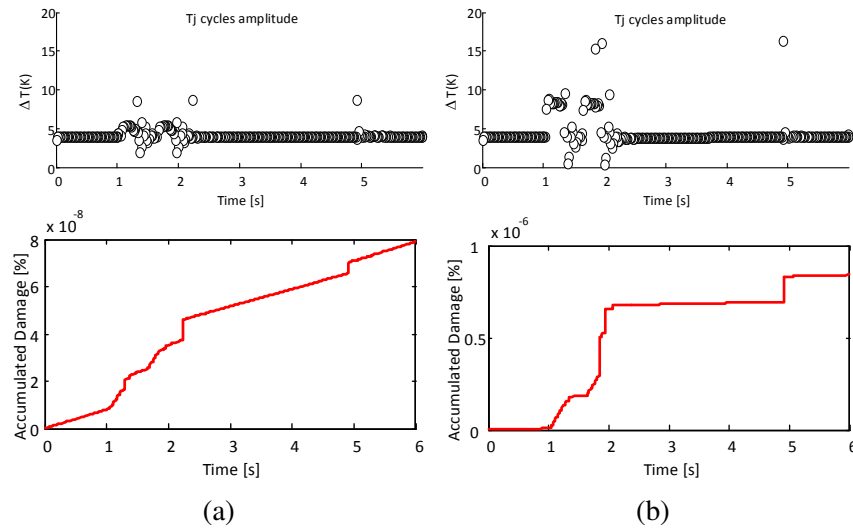


Figure 4.9: Rainflow cycle counted for junction temperature and accumulated damage of the bondwire for one IGBT in the MMC during the grid fault: (a) without reactive current injection, (b) with reactive current injection.

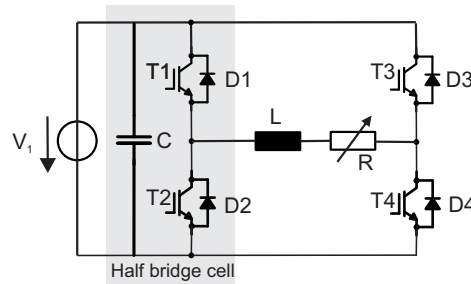


Figure 4.10: H-bridge converter for the emulation of the power semiconductor stress in one MMC cell.

drop is emulated with an electronic load by reducing its resistance. The half bridge, which emulates the MMC cell is driven with the same modulation signal as the MMC cell, while the second half bridge in the H-bridge is operating with a constant duty cycle of 0.75. This results in the same turn on times and the conduction times as for the power semiconductors in the MMC cell. The parameters of the H-bridge are shown in Table 4.1.

To demonstrate that the electrical characteristics of one MMC cell and the H-bridge are similar, Fig. 4.11 (a) shows the electrical characteristics of the MMC cell, whereas the corresponding measures of the H-bridge cell are presented in Fig. 4.11 (b). The DC-link of the MMC cell shows an oscillation, which is not reconstructed in the full bridge, but this oscillation is relatively low, which makes it negligible for the loading of the device. With the same modulation signal, the voltage and current of both cells show approximately similar AC and DC components.

The H-bridge is used to emulate the behavior of one MMC cell during operation and the described voltage sag. Thereby, the converter is driven in steady state to obtain a stationary temperature distribution on the surface of the power electronic module. To emulate the voltage sag, the resistance is changed stepwise from  $R = 7\ \Omega$  to  $R = 4\ \Omega$  for 0.5 s and the results

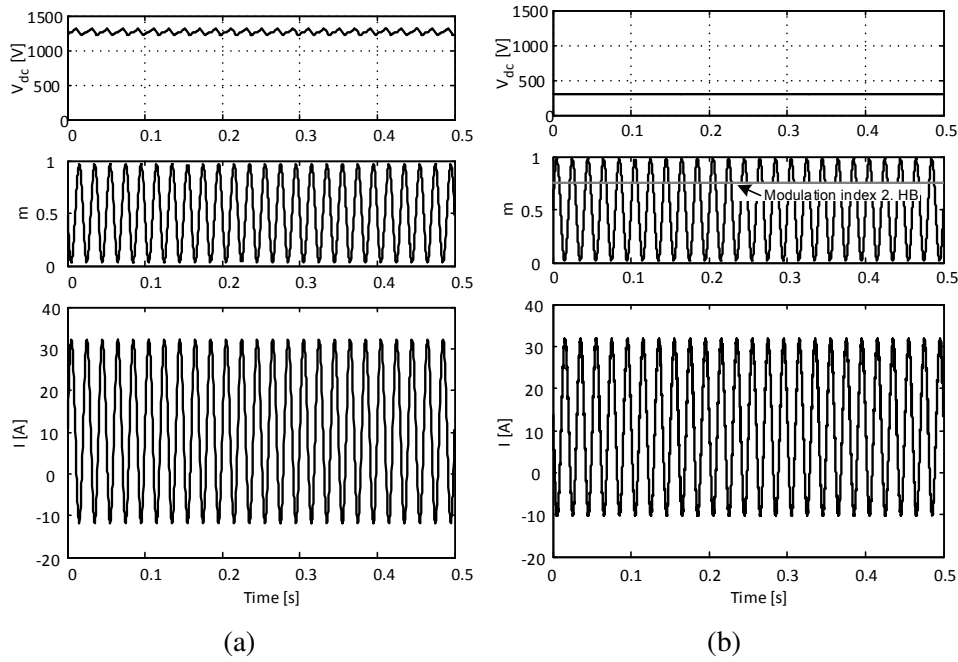


Figure 4.11: Comparison of electrical characteristics between (a) MMC cell voltage and current and (b) H-bridge voltage and current for reduced DC-link voltage and modified modulation.

Table 4.1: Parameters of the experimental setup for the MMC cell emulation.

Cell voltage $V_1$	300V
Switching frequency	20kHz
Rated rms cell current	25A
Load inductance	2mH
Load resistance	7 $\Omega$
Load resistance during voltage sag	4 $\Omega$

of the recorded thermal profile are shown in Fig. 4.12. The thermal cycles in the fundamental period have magnitude of  $\Delta T = 0.5 K$  and during the voltage sag the temperature is cycling with  $\Delta T = 6.5 K$ . It can clearly be seen that the power semiconductor is heated up during the power cycle. Both thermal swings are lower than in the simulations, but show the same characteristic behavior. A possible explanation is the use of passive heatsinks without fans in the setup, which results in a higher thermal resistance compared to actively cooled devices in the simulation.

These tests demonstrate an increase in the thermal stress for the power semiconductors, which was affected by a variation in the grid voltage. The drop of the grid voltage in combination with the constant power load behavior of the ST have affected thermal stress, which was reconstructed in the described experiment. Nevertheless, in the investigated loading conditions, this increase in thermal stress is not critical to affect immediate destruction of the devices.

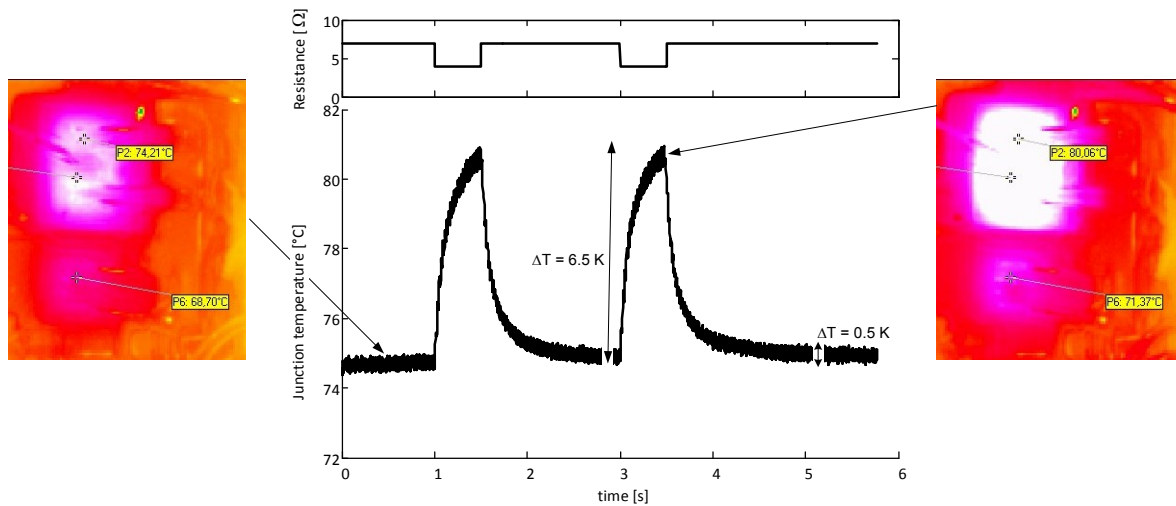


Figure 4.12: Laboratory measurement: Junction temperature measurement of one IGBT during the emulation of the investigated grid fault.

#### 4.2.5 Lifetime evaluation of the MV stage

The thermal stress, which was detected in the simulations of the last subsection needs to be translated into the lifetime of the MMC in the distribution grid. It needs to be pointed out, that this is highly dependent on the load profile and thus on the connected loads and generators. In this study, the profile of section 4.1 with high power, medium power and reverse power flow is assumed to repeat daily. Since the thermal simulations are made for short time periods of *3 min*, it needs to be extrapolated to cover the whole time in operation. Furthermore, periodic or statistic occurrences need to be estimated to identify factors affecting the lifetime of the system. Examples of stressing factors are thermal cycles caused by daily power variations (e.g. caused by consumer behavior, factories or generation), sun/wind variation affecting the renewables, ambient temperature variations affected by weather variations and faults. In table 4.2 the assumed parameters are shown. For only 10% of the time full load operation is assumed, whereas medium power is assumed for 65% of the time and reverse power flow for 25% of the time. For every working day per year, a thermal cycle of 45 K is assumed and for the weekend a thermal cycle with the magnitude of 30 K. Additional cycles are assumed to be affected by variation of the renewable generations, ambient temperature variations and grid faults. In case of grid faults, it is distinguished between the simulated case with reactive current injection and the case of feeder disconnection, which results in a total cooling down of the power semiconductors. The damage affected by these conditions is low and results in a lifetime expectation of more than 50 years. For such a long lifetime, other components in the system are expected to fail before. Consequently, the thermal stress investigation was made for a too conservative thermal design. Therefore, in the following subsection, the obtained results are used to optimize the thermal design based on the investigated mission profile.

#### 4.2.6 Thermal design for a specified maximum junction temperature or lifetime

Based on the oversized thermal system, the target is to use the mission profile analysis for a thermal design, which fulfills the reliability criteria, but minimizes the volume and the costs for the heat sink at the same time. For this purpose, first the maximum junction temperature is derived, which fulfills the lifetime criteria. In the second step, the heat sink is virtually reduced and the volume reduction can be quantified.

The relation between thermal cycles and the number of thermal cycles to failure (3.1) is used and the influence of the design for the maximum thermal swing and the average junction temperature is investigated. For this purpose, the accelerating factor introduced for the accelerated lifetime testing  $f_a$  from (3.4) is used, whereby  $\Delta T_{op}$  are the detected thermal swings of the actual design and  $\Delta T_{test}$  is the thermal swing of the revised thermal design. To simplify the mathematical expressions,  $\gamma = f_a^{-\frac{1}{ca}}$  is introduced. The connection is used, because the thermal de-rating leads to a proportional increase of all thermal cycles as expressed in (4.1). In this equation,  $\gamma$  is a scaling factor for the thermal design, defining for which thermal swing the lifetime expectation is fulfilled and  $x_{av}$  is the influence of the increase in the average junction temperature.

$$N_f = a_1 \cdot (\gamma \cdot \Delta T_j)^n \cdot x_{av} = \gamma^n \cdot a_1 \cdot (\Delta T_j)^n \cdot x_{av} \quad (4.1)$$

The influence of the average junction temperature is more difficult to be taken into consideration, because the thermal swings can be distributed in the power profile with different average temperatures, which do not just increase or decrease by a scaling factor. Consequently, an increase of the average junction temperature can have low influence for low average temperatures or it can have high influence for high average temperatures. This cannot be taken into account anymore if the damage is already accumulated. For this reason, the lifetime model is approximated in a different form, which considers the average junction temperature not in the denominator of the exponential function, but in the nominator as expressed in (4.2) with the new fitting parameter  $a_6$ .

$$N_f = a_1 (\Delta T)^n \cdot e^{a_6 \cdot T_{j,av}} \quad (4.2)$$

For the LESIT results, which were tested with  $\Delta T = \{30,40,50,60,70,80\}^\circ C$  and  $T_{j,av} = \{60,80,100\}^\circ C$ , this results in a good fit to the original test results [72]. The parameters, which are obtained for the influence of the average temperature are shown in (4.3). In this equation the increased average temperature is expressed in dependence of the old maximum temperature increase to ambient for which the system was designed  $T_{j,av,old}$  and the de-rating factor  $\gamma$ . As a limitation of this equation, the variations caused by the superposition of the ambient temperature cannot be separated.

$$x_{av} = e^{(\gamma-1) \cdot 0.0555 \cdot \Delta T_{j,max,old}} \quad (4.3)$$

Table 4.2: Parameters for the translation from thermal stress to lifetime of the MV stage.

Occurrence	Assumed frequency of occurrence
Short-term power variations: Under high load (as in Fig 4.2 (b)) Under medium load (as in Fig 4.2 (c)) With reverse power flow (as in Fig 4.2 (d))	10 % of time per day 65 % of time per day 25 % of time per day
Working day consumer behavior as shown in Fig. 4.2 (a)	5 cycles per week ( $\Delta T = 45 K$ )
Weekend consumer behavior	2 cycles per week ( $\Delta T = 30 K$ )
Weather and wind variations affecting the generation	12 cycles per week ( $\Delta T = 55 K$ )
Weather and wind variations affecting the ambient conditions	2 cycles per week ( $\Delta T = 65 K$ )
Ambient temperature variations	2 cycles per month ( $\Delta T = 70 K$ ) 2 cycles per year ( $\Delta T = 90 K$ )
Grid faults Without disconnection (as in 4.5 (b)) With disconnection of the grid	1 per week with damage from Fig 4.9 (b) 1 per month with $\Delta T = 50 K$

The equation indicates for an increase of the maximum junction temperature by  $10^\circ C$  a decrease of the lifetime to 57 % of its prior time. This is alignment with the common approximation, which assumes a decrease of the lifetime by 50 % for an increase in the maximum junction temperature by  $10^\circ C$ . For the linear damage accumulation, (4.3) is now used in the Palmgren Miner rule (3.3) with the number of cycles to failure in the stress range  $N_i$  and the number of detected cycles in the stress range  $n_i$ . This is applied to the mission profile in this work, leading to (4.4).

$$\sum_{i=0}^{\inf} \gamma^{-n} \cdot e^{(\gamma-1) \cdot 0.0555 \cdot \Delta T_{j,max,old}} \cdot \frac{n_i}{N_i} = \gamma^{-n} \cdot e^{(\gamma-1) \cdot 0.0555 \cdot \Delta T_{j,max,old}} \sum_{i=0}^{\inf} \frac{n_i}{N_i} \leq 1 \quad (4.4)$$

This de-rating equation is now a non-linear dependence and is used for two purposes: The first one investigates the expected lifetime based on the design for different junction temperatures and the second one investigates the optimal thermal design for a predefined lifetime target. For this purpose, it is distinguished between the thermal cycles, which are influenced by the design and those, which are caused by ambient conditions. This is shown in table 4.3.

Based on the mission profile expressed in table 4.2, the lifetime model is used to evaluate the design for different maximum junction temperatures. The results are shown in table 4.4 for thermal designs from  $80^\circ C$  to  $120^\circ C$ . Lifetimes, which indicate a high overdesign of the heat sink have been marked to be higher than 50 years. However, it can be seen, that the lifetime is sensitive to the design for a maximum junction temperature. The design for

Table 4.3: Dependence of the thermal stress on the design.

Occurrence	Influenced by the thermal design
Load variations	yes
Consumer behavior	yes
Renewable power fluctuations	yes
Ambient temperature variations	no
Grid faults	yes

Table 4.4: Lifetime expectations for different thermal designs of the mission profile. The assumed mission profile is shown in table 4.2.

Maximum junction temperature [ $^{\circ}C$ ]	80	90	100	110	120
Resulting $B_{10}$ lifetime [years]	>50	>50	50	17	5

$100^{\circ}C$  is an overdesign with a long lifetime, whereas only  $20^{\circ}C$  more result in only 5 years of expected lifetime.

To obtain the optimal thermal design for a given lifetime target, (4.4) cannot be solved analytically and requires a numeric solver. However, the  $B_{10}$  lifetime is used to determine the optimal thermal design, fitting the lifetime target of the system. The parameters for this optimization are the designed maximum thermal swing  $\Delta T_{j,max}$  and the maximum junction temperature  $T_{j,max}$ . The results of this comparison are shown for different lifetime targets of 40, 30, 20 and 10 years in Table 4.5. A lifetime target of 40 years is still an overdesign of the heat sink, but shows the high sensitivity of the thermal design. The thermal swing can be increased to  $63K$  for a lifetime of 40 years and for a lifetime target of 10 years even to  $74K$ .

It can be seen, that for all lifetime targets, the limitation of the maximum junction temperature is much colder than the typical physical limit of  $T_{j,max} < 175^{\circ}C$ . However, the different thermal designs are very sensitive to the maximum junction temperature. Between the design for 40 years and the design for 10 years, there is only a difference of  $11K$  in the thermal design. For this reason, the thermal design and the operating conditions need to be considered carefully in the design process.

Table 4.5: Resultant thermal swing and maximum junction temperature for the design target of a specified  $B_{10}$  lifetime for the MV stage of the ST. The assumed mission profile is shown in table 4.2.

Estimated $B_{10}$ Lifetime [years]	> 50	40	30	20	10
Thermal design scaling factor $\gamma$	1	1.59	1.64	1.72	1.85
Resulting design for the thermal swing $\Delta T_{j,max}$ [K]	40	63	66	69	74
Resulting maximum junction temperature design $T_{j,max}$ [ $^{\circ}C$ ]	80	103	106	109	114

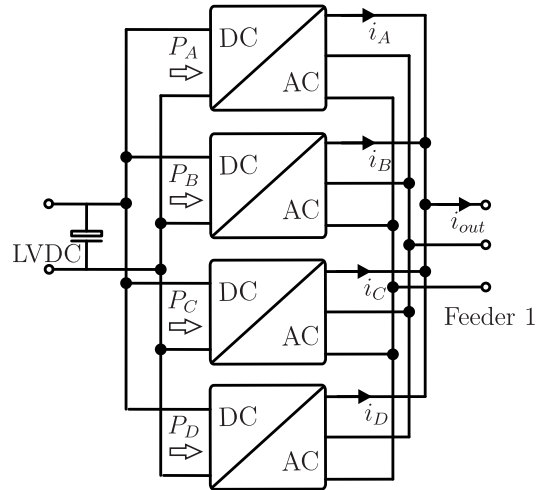


Figure 4.13: LV stage of the ST composed by four parallel converters connected to one grid feeder.

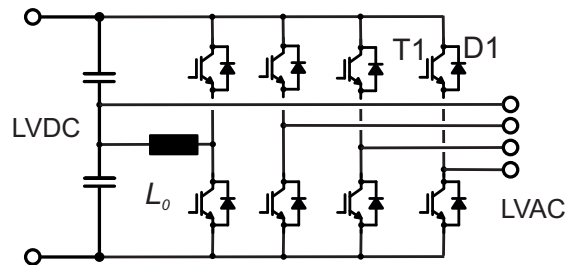


Figure 4.14: Topology of the two level VSC in the LV stage of the ST in Fig. 2.12.

### 4.3 Thermal stress analysis for the LV stage

This subsection investigates the thermal stress for the LV stage of the ST. In addition, the derating strategy of the thermal design, introduced in the last subsection, is applied to optimize the utilization of the devices.

#### 4.3.1 Short term power variations

The ST is considered to transfer the whole power from the MVAC grid to the LVAC grid, whereby the power among the parallel converters in the LV side is equally shared as shown in Fig. 4.13. Consequently, no DC grid is considered to be connected. The connection of all converters to a single feeder provides parallel redundancy and in the case of a fault in one of the converters, the others can continue to operate if the failure is isolated fast. Not having this redundancy makes the reliability for the converter indispensable. The four parallel two level VSCs are designed as proposed in the example in section 2.3.3. A single converter is shown in Fig. 4.14 and designed with the parameters of table 2.8. Because of the expected reactive power consumption in the grid, the converter is designed for an inductive power factor of  $\cos(\varphi) = 0.9$  and a rated load current of 537A. For the thermal stress analysis, only one out of the four converters is studied and the same mission profile like in the MV stage is applied. The temperature profiles of the power semiconductors under these mission profile

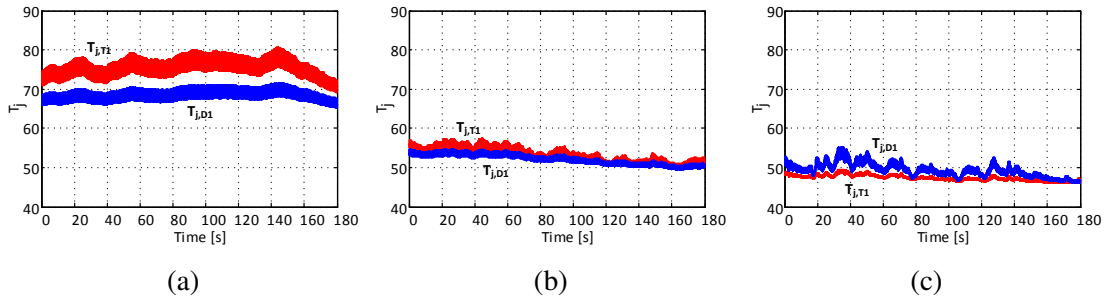


Figure 4.15: Thermal stress for the two level VSC (see Fig. 4.14) during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

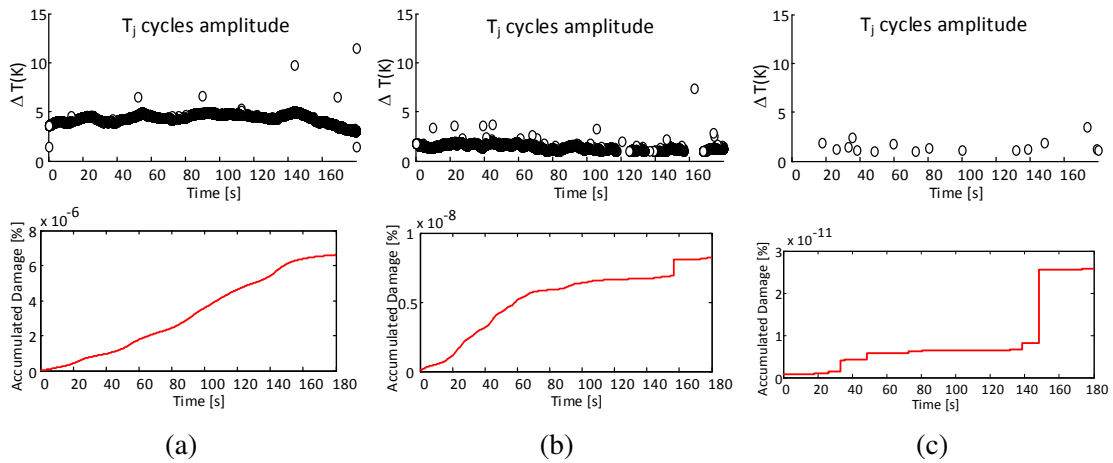


Figure 4.16: Rainflow cycle counted for junction temperature of T1 in one two level inverter during the different loading conditions (see Fig. 4.2): (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

are shown in Fig. 4.15 for the IGBT T1 and the diode D1. Despite considering four wires in the converter, the load is assumed to be balanced in the three grid feeders, which does not put loading on the neutral wire.

The thermal stress for the converter is evaluated by simulating the three profiles shown in Fig. 4.2. For the high load mission profile, the junction temperature of T1 is highest and between  $70^{\circ}\text{C}$  and  $81^{\circ}\text{C}$ , whereas the temperature of D1 is between  $65^{\circ}\text{C}$  and  $71^{\circ}\text{C}$ , which is in accordance with the power semiconductor choice as in the case before. The cycles in the fundamental period are approximately  $\Delta T \approx 5\text{ K}$  for T1 and  $\Delta T \approx 4\text{ K}$  for D1. The junction temperature profile for the medium load profile in Fig. 4.15 (b) shows reduced stress for the diode with lower average temperatures and lower thermal swing for both semiconductors. Similar to the stress for the power semiconductors in the MMC topology, the high renewable energy production in Fig. 4.2 shows a higher temperature fluctuation for the diode. Remarkably, in the reverse power flow the IGBT T1 has a much smaller thermal swing compared to the diode D1.

In Fig. 4.16 the thermal cycles are counted for the IGBT T1 in the VSC under the assumed load profile. The identified thermal cycles of the Rainflow counting obtain the same char-



Table 4.6: Parameters for the translation from thermal stress to lifetime of the LV stage.

Occurrence	Assumed frequency of occurrence
Short term power variations:	
Under high load (as in Fig 4.2 (b))	10 % of time per day
Under medium load (as in Fig 4.2 (c))	65 % of time per day
With reverse power flow (as in Fig 4.2 (d))	25 % of time per day
Working day consumer behavior as shown in Fig. 4.2 (a)	5 cycles per week ( $\Delta T = 45 K$ )
Weekend consumer behavior	2 cycles per week ( $\Delta T = 30 K$ )
Weather and wind variations affecting the generation	12 cycles per week ( $\Delta T = 55 K$ )
Weather and wind variations affecting the ambient conditions	2 cycles per week ( $\Delta T = 65 K$ )
Ambient temperature variations	2 cycles per month ( $\Delta T = 70 K$ ) 2 cycles per year ( $\Delta T = 90 K$ )
Grid faults	
With disconnection of the grid	1 per month with $\Delta T = 50 K$

Table 4.7: Lifetime expectations for different thermal designs of the LV stage. The assumed mission profile is shown in table 4.6.

Maximum junction temperature [ $^{\circ}C$ ]	80	90	100	110	120
Resulting $B_{10}$ lifetime [years]	>50	>50	34	9	3

acteristics to those ones of the semiconductors in the MMC. During reverse power flow, the affected damage is very low in T1, whereas for the other power semiconductors it is almost comparable to the profiles of the power semiconductors in the other topologies. It can be concluded, that most of the thermal stress is affected by the thermal cycles in the fundamental period, but this damage is still low and does not limit the lifetime of the system for the design in this work.

### 4.3.2 Lifetime and design evaluation of the LV stage

For a lifetime evaluation of the LV stage, a study based on a mission profile consisting of different operating conditions and influencing factors is made, which is similar to the analysis for the MV-stage. The profile is composed as shown in table 4.6, which is similar to the MV stage, but without the investigated grid fault.

Also in the LV stage, the conservative thermal design results in an expected lifetime, which is higher than 50 years. For this reason the lifetime expectation is derived for different thermal designs in table 4.7. A thermal design for  $100^{\circ}C$  results in a lifetime expectation of 34 years, whereas a design for  $T_{j,max} = 110^{\circ}C$  results in a lifetime expectation of only 9 years.

Table 4.8: Resultant thermal swing and maximum junction temperature for the design target of a specified  $B_{10}$  lifetime for the LV stage of the ST. The assumed mission profile is shown in table 4.6.

Estimated $B_{10}$ Lifetime [years]	> 50	40	30	20	10
Thermal design scaling factor $\gamma$	1	1.42	1.47	1.60	1.73
Resulting design for the thermal swing $\Delta T_{j,max}$ [K]	40	58	61	64	69
Resulting maximum junction temperature design $T_{j,max}$ [ $^{\circ}$ C]	80	98	101	104	109

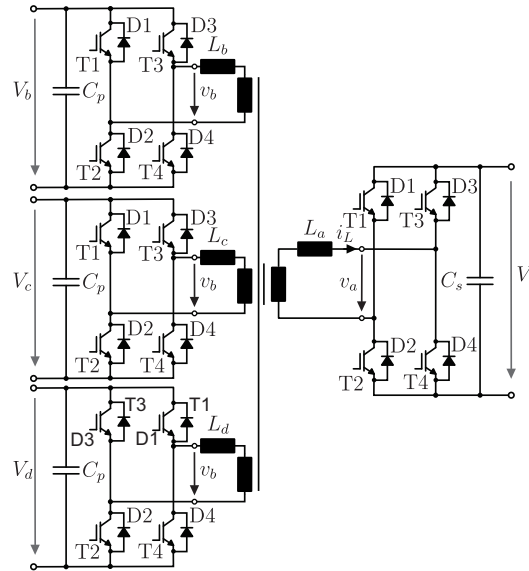


Figure 4.17: Quadruple Active Bridge (QAB).

Similar to the MV stage, the optimal thermal design for different lifetime targets is derived numerically with (4.4) and the results are presented in table 4.8. A lifetime target of 40 years results in a thermal design for a maximum junction temperature of  $98^{\circ}$ C and the lifetime target of 10 years in a design for a maximum junction temperature of  $109^{\circ}$ C. The difference for these designs is only 11 K, showing again the sensitivity of the design for a maximum junction temperature and the according thermal fluctuations.

#### 4.4 Thermal stress analysis for the isolation stage

This subsection evaluates the thermal stress for the isolation stage during fast power variations for a similar thermal design as for the LV stage and the MV stage to enable a comparison between the stages with the target to quantify in which stage the power semiconductors are most thermally stressed. In addition, the thermal de-rating strategy is applied to optimize the system design under the consideration of thermal stress, volume and costs.

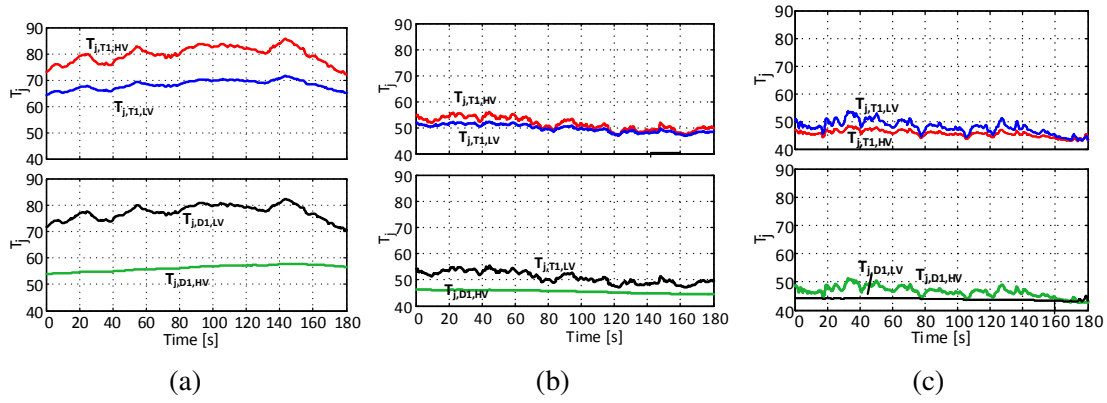


Figure 4.18: Thermal stress for the QAB (see Fig. 4.17) during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

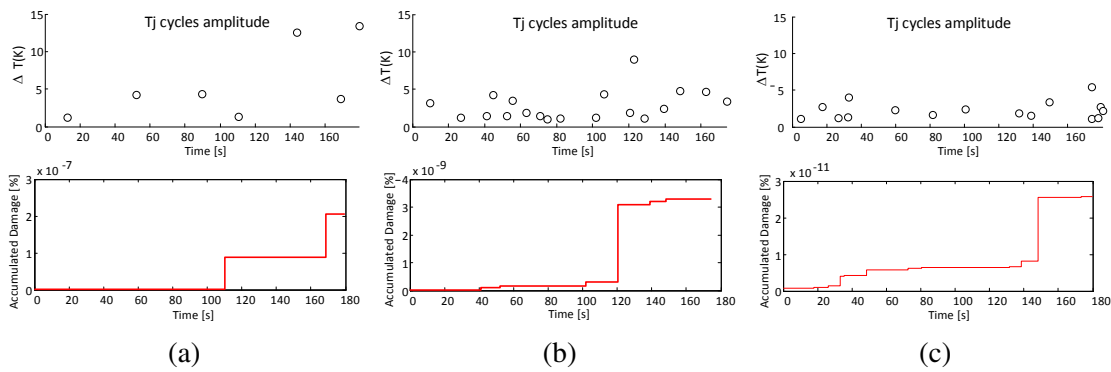


Figure 4.19: Rainflow cycle counted for junction temperature of  $T_{j,T1,LV}$  in the QAB during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

#### 4.4.1 Short term power variations

The isolation stage is interfacing the LV and the MV converter and consequently, it needs to exchange the active power between the MV stage and the LV stage. Thus, the QAB converters, which are designed as described in the architecture of section 2.3.4, undergo the same mission profile as the LV stage (see Fig. 4.2). The related thermal simulations are shown in Fig. 4.18 for the three load profiles. The temperature fluctuation under the high load mission profile is approximately proportional to the mission profile for the most stressed components  $T_{j,T1,HV}$  and  $T_{j,D1,LV}$ . Remarkably, one of the devices,  $T_{j,T1,HV}$ , is installed in the MV side and the other one,  $T_{j,D1,LV}$ , in the LV side. The diode  $T_{j,D1,HV}$  is almost not stressed for the conditions of the high and the medium load profile, whereas the maximum temperature of the highest loaded device is  $86^{\circ}\text{C}$ , which is in accordance with the system design. For the medium load profile, the thermal swing is very low and the average temperatures are low as well. The third profile with reverse power flow has also a relatively low average temperature, but the anti-parallel power semiconductor is stressed higher. Thus  $T_{j,T1,HV}$  and  $T_{j,D1,LV}$  are less stressed than  $T_{j,T1,LV}$  and  $T_{j,D1,HV}$ .

In Fig. 4.19 the thermal cycles are Rainflow counted and shown for IGBT T1 of the LV side

Table 4.9: Parameters for the translation from thermal stress to lifetime for the isolation stage.

Occurrence	Assumed frequency of occurrence
Short-term power variations: Under high load (as in Fig 4.2 (b)) Under medium load (as in Fig 4.2 (c)) With reverse power flow (as in Fig 4.2 (d))	10 % of time per day 65 % of time per day 25 % of time per day
Working day consumer behavior as shown in Fig. 4.2 (a)	5 cycles per week ( $\Delta T = 45 K$ )
Weekend consumer behavior	2 cycles per week ( $\Delta T = 30 K$ )
Weather and wind variations affecting the generation	12 cycles per week ( $\Delta T = 55 K$ )
Weather and wind variations affecting the ambient conditions	2 cycles per week ( $\Delta T = 65 K$ )
Ambient temperature variations	2 cycles per month ( $\Delta T = 70 K$ ) 2 cycles per year ( $\Delta T = 90 K$ )
Grid faults With disconnection of the grid	1 per month with $\Delta T = 50 K$

H-bridge (see Fig 4.17) undergoing the three load profiles. The LV side is chosen, because it is stressed most in this topology for high power flow from MV to LV grid. The DC/DC converter has much less thermal cycles than the other two stages under the same profile, because the cycles are only generated by the load profile.

Because of the lower number of thermal cycles in the profile, the damage is also low compared to the converters connected to the AC grids. The variations in the mission profile are clearly indicated as steps in the mission profile. It is concluded that the lifetime of the QAB is only marginally affected by the applied conservative thermal design. Moreover, the damage affected by the three profiles is even lower than for the two other stages.

#### 4.4.2 Lifetime and design evaluation of the isolation stage

Similar to the other two stages, the expected lifetime for the system is derived by assuming different thermal cycles and different operating periods, which are affecting thermal stress. The isolation stage is not affected by disturbances in the grid or reactive current injection. However, the disconnection of the connected feeders can still influence it. The assumed mission profile is similar to the mission profile of the LV stage and is shown in table 4.9. With the applied thermal design, the resulting lifetime is higher than 50 years, which is an overdesign of the heat sink, again.

The thermal design of the isolation stage is evaluated for different maximum junction temperature designs between  $80^{\circ}\text{C}$  and  $140^{\circ}\text{C}$  as shown in Fig. 4.10. In this case, a design for a maximum junction temperature of  $120^{\circ}\text{C}$  still results in a high lifetime expectation.

Table 4.10: Lifetime expectations for different thermal designs of the isolation stage. The assumed mission profile is shown in table 4.9.

<b>Maximum junction temperature [<math>^{\circ}C</math>]</b>	80	90	100	110	120	130	140
<b>Resulting <math>B_{10}</math> lifetime [years]</b>	>50	>50	>50	>50	>50	27	9

Table 4.11: Resultant thermal swing and maximum junction temperature for the design target of a specified  $B_{10}$  lifetime for the isolation stage of the ST. The assumed mission profile is shown in table 4.9.

<b>Estimated <math>B_{10}</math> Lifetime [years]</b>	> 50	40	30	20	10
Thermal design scaling factor $\gamma$	1	2.16	2.22	2.31	2.48
Resulting design for the thermal swing $\Delta T_{j,max}$ [K]	40	86	89	93	99
Resulting maximum junction temperature design $T_{j,max}$ [ $^{\circ}C$ ]	80	126	129	133	139

For an optimization of the design, the thermal design for a specific lifetime is evaluated and shown in table 4.11. Remarkably, the design for a lifetime of 40 years, the maximum junction temperature is  $126^{\circ}C$  and the design for 10 years leads to a maximum junction temperature of  $139^{\circ}C$ . These are very high temperatures and they need to be considered carefully, because of other failure mechanisms, which might be activated by the high junction temperatures. Furthermore, power fluctuations, which cause overload conditions cannot be accepted in this case, because the safety margin to the maximum junction temperature, which leads to a destruction of the device, is reduced.

## 4.5 Comparison of the stress for the three stages

The thermal stress analysis is completed with a comparison of the accumulated damage for the power semiconductors in the three stages of the ST with the applied thermal design. First, this comparison is done for the high load profile, because it is affecting most of the wear-out in operation. The normed damage for the most stressed power semiconductor in each of the three stages under the investigated conditions is chosen and compared in table 4.12. It can be seen that the lowest accumulated damage is derived for the QAB, whereas the MMC has still lower consumed lifetime than the two level VSC. The result comes despite the design for a similar maximum junction temperature of the power semiconductors. The accumulated damage of the IGBTs is higher than the accumulated damage of the diodes, which is affected by the power flow direction. The MMC has the most equal stress distribution for the diode and the IGBTs, whereas the QAB and the VSC obtain very unequal stress distribution among their anti-parallel power semiconductors.

In addition to the comparison of the damage for the single power semiconductors under a specified profile, the stress for the most stressed power semiconductor is extrapolated to longer lifetimes by considering thermal cycles affected in different periodicity and sources.

Table 4.12: Comparison of the damage of the power semiconductors undergoing the high load profile normalized on one IGBT in the LV stage.

Power semiconductor	Relative damage
T1 in the MMC	0.56
D1 in the MMC	0.24
T1 in the LV side of the QAB	0.03
D1 in the LV side of the QAB	0
T1 in the VSC	1
D1 in the VSC	0.1

Based on this long time mission profile, a lifetime of 20 years is targeted for the three stages and the maximum junction temperature, which would lead to this results is shown in table 4.13. As a result, the isolation stage can be designed for a much higher junction temperature of  $133^{\circ}\text{C}$  than the low voltage stage ( $104^{\circ}\text{C}$ ). For the utilization of this de-rating, the heat sink can be re-sized as explained in section 2.3.1. The new size under the assumption of a constant CSPI is estimated with (4.5).

$$VS_2 = VS_1 \cdot \frac{T_{c,max,1} - T_a}{T_{c,max,2} - T_a} \quad (4.5)$$

By applying the proposed de-rating, the volume of the heat sink can be reduced to 23 % of its prior volume in the MV stage and to 18 % in the isolation stage. This results in a significant reduction of the volume and a reduction of costs for the heat sink.

Instead of changing the cooling system design, it is also possible to feed higher power with the proposed system design to influence the thermal stress. For this purpose, the thermal scaling factor  $\gamma$  can be applied for the power semiconductor losses. As it is shown in table 4.13 for a lifetime expectation of 20 years, it is obtained, that the losses for the MV stage can be increased by 72 %, the losses of the isolation stage by 131 % and the losses of the LV stage by 60 %. These numbers can result in significant financial savings, but the stress for other components needs to be evaluated carefully to ensure not to overload any other components in the system. As an example, this stress can affect bond wires, which should not exceed the rated current limits or even other components like capacitors and inductors in the converter.

## 4.6 Short summary of the section

Thermal stress analysis has been made for the three-stage ST under consideration of realistic operation conditions in the power system. No lifetime limiting conditions have been found and based on the originally proposed design, thermal de-rating is proposed. This leads to different maximum junction temperature designs of the three stages for a lifetime target of 20 years. Thereby, the isolation stage was least thermally stressed and the LV side converter

Table 4.13: Comparison of the thermal design and the cooling system design for a lifetime target of 20 years.

	<b>Design for the maximum junction temperature</b> $T_{j,max}$	<b>Relative size of the de-rated cooling system</b>	<b>Potential increase of losses</b>
MV stage	109°C	23 %	72 %
Isolation stage	133°C	18 %	131 %
LV stage	104°C	19 %	60 %

was most thermally stressed. Based on this finding, the design was exploited to optimize the design by increasing the maximum junction temperature and minimize the system's volume and the costs for the cooling system. It is shown, that a tailored design needs to be made for each of the three stages. Based on the initial design, a significant reduction of the cooling system or an increase of the losses is possible for all three stages without compromising the reliability.

## 5 Active thermal control of power electronic modules

The reliability of the power semiconductors has been demonstrated to be influenced by the design for the maximum junction temperature. In addition, the maximum junction temperature influences the volume of the cooling system and the related costs, which results in conflicting goals. An opportunity to improve the reliability without increasing the costs of the hardware is active thermal control and will be introduced in the following. This section first provides a review of active thermal control in literature and then, to overcome the problem of junction temperature measurement for active thermal control, an estimator is designed and validated. To demonstrate the principle of active thermal control, an algorithm for controlling the thermal stress of PV converters during fast changing irradiance is presented.

### 5.1 Review on Active thermal control

#### 5.1.1 Introduction of active thermal control

The power variations and the ambient temperature variations in the mission profile will be directly reflected by the thermal loading of the power semiconductors, which was described in section 3. This results in thermal cycling, which affects the wear-out of the components. Additionally, the temperature gradients in the modules, affected by the heat transfer from junction to heat sink, are causing strain between the different layers in the power modules. The thermal stress of the power devices needs to be assessed and properly considered in the design process of a system [104]. To fulfill the reliability requirement of the application, the design is usually iterated until the reliability target is fulfilled without oversizing the components [105]. Well-known design parameters to improve the reliability are the design for a reduced maximum junction temperature or for higher current ratings.

As an alternative, active thermal control is the concept to regulate directly the junction temperature to control the thermal stress. The general principle is to vary one or more temperature related control variables of the system to influence its junction temperature in order to prevent damage. Active thermal control can be implemented with different algorithms controlling different variables, whereas all currently documented approaches can be grouped in two different basic ideas. The first approach relies on control of the heat dissipation, such as variable forced cooling [106, 107, 108, 109] and thermoelectric cooling [110]. In this case, the thermal impedance  $Z_{th}$  is influenced by the controller. The second approach targets to control electric parameters [111, 112, 113] and controls the losses of the system  $P_{loss}$ .

Controlling the fan of the cooling system to control the junction temperature fluctuations seems to be a promising approach, because the operation of the converter is not affected. However, the cooler control might not be able to reduce the stress affected by the junction temperature gradients in the modules. Even if perfect tracking of the junction temperature is achieved, the temperature gradients in the module are changing and result in strain variations, consequent to thermal stress. To reduce the stress affected by the junction temperature



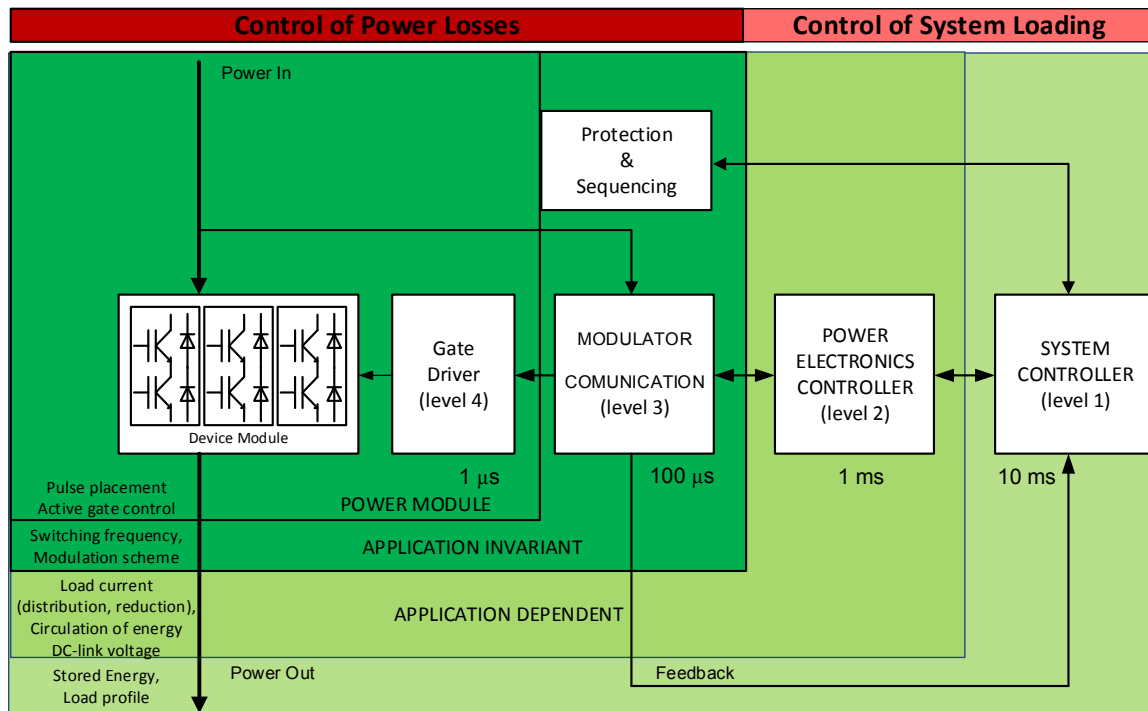


Figure 5.1: Active thermal controllers in different layers of a system.

gradients, the losses of the power semiconductors need to be kept constant despite variations in the mission profile. This keeps the temperature between junction and case constant as well as in the whole power electronic module. In contrast to the cooler control, the ambient temperature variations are still expected to cause thermal stress, because for constant losses, they would be reflected in the junction temperature.

In the following, the focus is put on the approach to control the power semiconductor losses, because the load profile has been shown to have much higher influence on the thermal stress than the assumed weather variations in the mission profile analysis of section 4.2.5. The approach can be further categorized into controlling directly the losses of the system and controlling the loading of the system. For both approaches, there are several possible algorithms on different layers of the overall control system, addressing different periods of thermal cycles, which is visualized in Fig. 5.1. Remarkably, the implementation and the benefits highly depend on the application, the system design and the mission profile. In order to maximize the effectiveness, the implementation of multiple thermal controllers is possible.

In the following, the control of the power losses and the control of the system loading are reviewed in literature with the target to identify suitable algorithms for the application in STs.

### 5.1.2 Junction temperature control by control of the power losses

Controlling the junction temperature by control of the power losses can be achieved by controlling one or more parameters, which is directly influencing the losses. In Fig. 5.1, this

is indicated to be application invariant with potential high dynamics. Application invariant describes, that no further conditions need to be fulfilled, whereas the impact on the system in the chosen application still needs to be studied. The smallest accessible time constants are accessed by gate driver control, which was applied in [114, 115, 116, 107], mainly to balance the stress between parallel semiconductors. The balancing between parallel chips brings the advantage that parameter differences like resistances in parallel chips can be compensated by the gate driver and do not result in imbalanced loading. Without this gate driver, the parallel chips need to be designed for a higher current to ensure, that no chip is overloaded. As a further development, an active gate driver was proposed to reduce the thermal cycling by controlling the turn on time and thereby controlling the turn on losses [117, 118].

The control of the power losses by controlling the switching frequency was first proposed by industry as a solution to reduce thermal cycling of power semiconductors in motor drives during low speed and high torque [119]. The initiative was motivated by the target to derate the power semiconductors in this application and thereby reducing the costs without impairing the reliability. As a solution, excessive junction temperatures were detected and the frequency of the Pulse Width Modulation (PWM) was reduced to reduce the switching losses and thereby the junction temperature [120, 121]. The same technique is adopted in [112], where the aim is reducing the thermal cycling during high torque and low speed, whereby a region-based control was implemented to ensure that the thermal control is only active for severe operating conditions. As another advancement to this approach, the thermal controller can also be implemented on a system level, whereby system constraints by means of an electrical machine are taken into account [122]. As a possible real time implementation, a virtual state machine has been proposed, which controls the load current and the switching frequency of a converter [123].

Similar to the control of the switching frequency, changing between continuous and discontinuous  $60^\circ$  PWM to reduce losses was applied in [124, 113]. Furthermore, for grid-connected applications, the modulation strategy was modified to address specific problems, like the Low Voltage Ride Through (LVRT) [125], which normally increases the stress of the anti-parallel diodes of the power modules. With the proposed modulation, the stress is reduced for the most stressed semiconductor by using other redundant space vectors.

Another approach is to manipulate the loss distribution between IGBTs and diodes, by adjustment of the modulation index. This has been proposed for controlling the DC-link voltage, which is directly coupled to the modulation index [126]. The approach can be used to relieve stress from specific semiconductors on the expense of additional losses in the inverter caused by a higher current magnitude. In the MMC operating with nearest level modulation, the cells can be stressed unequally in specific conditions, leading to higher thermal stress in some cells. This gets even more critical if there are redundant cells, which are not required to generate the output voltage. To overcome this problem, an algorithm, which is taking into account the junction temperature, is proposed in [127] for balancing the stress for the power semiconductors in the MMC cells. This algorithm is resulting in thermal balance for the power semiconductors without increasing the losses of the converter.

As a disadvantage of controlling the losses in the power converter, many algorithms affect the efficiency of the system and the current ripple. Since the efficiency directly influences the operation cost, an estimation of the reduced system efficiency is mandatory before the system is designed and a thermal controller is tuned.

### **5.1.3 Junction temperature control by control of system loading**

The potential for junction temperature control by control of the system loading is highly dependent on the application and the system design. Therefore, there are no variables, which are generally controllable in every system. As an example for a possible control variable, a dynamic limit of the inverter current under thermal constraints is proposed in [112]. This enables to continue operation of systems close to the thermal limits, while a further rise in temperature and thereby a complete shutdown or damage of the module due to over temperature is prevented. However, there are applications in which a limitation of the output current is not acceptable, because the safe operation can be impacted.

If the system is composed of multiple cells or multiple converters, additional thermal controllers can be implemented, which take advantage of the redundancy in the system. As an opportunity, the redundancy can be used to control the loading of different parts or to balance the loading among different paths. In [128], commutation counting was performed to select the cell to switch in a CHB structure. Intelligent management of the power sharing among parallel power converters has also been an object of interest in [129]. In the cited work, the parameter tolerances were investigated with the target of thermal load sharing. Another approach is to control the loading of the system. The thermal cycling with multiple grid-connected inverters in a wind farm was proposed in [101], where reactive power was circulated among parallel power converters in order to prevent excessive cooling down of the power modules during abrupt output power changes. For photovoltaic application, a MPPT algorithm has been proposed for shaping the mission profile. The MPPT algorithm does not only consider the harvested energy, but also considers the damage caused by thermal cycling during fast changing irradiation [130], [131].

As a conclusion, the control of the system loading requires redundancy to be exploited. This is not possible in every system, but in case it is possible, it offers a promising opportunity to utilize this for active thermal control.

## **5.2 Real time junction temperature determination**

### **5.2.1 Review of junction temperature determination**

A real-time information about the junction temperatures of a power module is of interest for active thermal control. The biggest challenge is to obtain a practical non-invasive and inexpensive method for achieving a bandwidth high enough to detect all junction temperature

variations. To the current state, this has not been found and a compromise needs to be made between by choosing one out of the three following approaches:

- Direct measurement
- Measurement with Thermo-Sensitive Electrical Parameters
- Model based approaches

As the most intuitive solution, direct measurements of the junction temperature is possible, but usually, this requires removing the gel filling in the module. In this case, optic fibers or infrared cameras can be used to measure the junction temperature. Both methods are expensive and can only be carried out in special laboratory setups with reduced operation voltage because of the missing gel filling. Consequently, this is only practical for research and development purpose. Other direct measurements, like thermocouples connected to the chips, are impractical, because they cannot reach the necessary bandwidth for active thermal control application.

For commercial product solutions, junction temperature measurements based on electrical measurements are more realistic [132, 133]. This is referred to as TSEP. Classical TSEPs are the collector-emitter voltage drop at low current, the threshold voltage and saturation current of metal-oxide semiconductor gated devices [133], the short circuit current [134] and others. TSEPs have been implemented in commercially available power semiconductor modules by integrating a small diode on the chips for the measurement of its forward voltage. This forward voltage correlates linearly with the junction temperature, but the disadvantage is a reduction of the useful chip area. As a general disadvantage, the measurements of TSEPs requires additional circuitry and thus causes additional costs.

An alternative to the direct measurement and TSEPs is to developed a junction temperature model. Based on this model, estimators and observers have been developed, whereby parameter variations, parameter uncertainties and sensor delays are a challenge [135, 136]. In order to overcome this problem, a model-based approaches has been combined with TSEPs to obtain fast bandwidth and to observe the aging of the system [137]. For the suppression of measurement noise of the  $V_{ce}$ -measurement, an observer has been proposed [138]. However, this requires additional circuitry and affects additional effort, which is impractical for a modular system consisting of several building blocks with many junction temperatures.

A cost effective approach for the modeling of the junction temperature relies on the junction temperature model, which is described in section 3.3.1. This enables to obtain an estimation of the junction temperature by only increasing the calculation effort without additional hardware costs. The disadvantage of the approach is, that the variations in the thermal resistance, which occur because of aging, cannot be modeled in the estimator and there might be a deviation between the real chip temperature and the estimated junction temperature. However, the application of active thermal control targets to reduce the thermal swing, which is still modeled in the estimator.

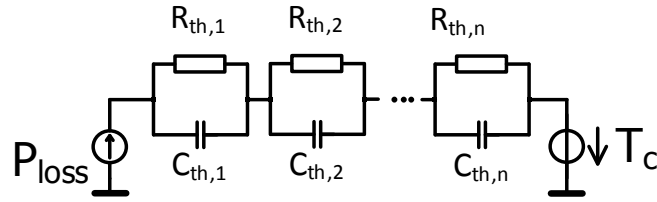


Figure 5.2: Model of the thermal impedance  $Z_{th,jc}$  with a Foster circuit.

A disadvantage of all model based approaches is the precision. This can be improved by feeding back one or more parameters. As an example, the thermal impedance between junction and ambient is highly influenced by the chosen heat sink and the ambient conditions. As a simple solution to overcome this issue, a narrow bandwidth case temperature measurement can be included. Since this is commonly included in many of today's power electronic modules, the increase of the complexity is relatively small. As a disadvantage of this approach, the problem of aging in the power electronic module is not solved. For detecting aging, additional information is required. In [139], a FPGA was used to measure the switching losses of the power converter during operation. With the measurement of the losses and the case temperature, a model is developed, which can identify the aging of the system. The disadvantages are increased costs for the equipment, which is required for the measurement of the losses.

### 5.2.2 Design of a Foster circuit based junction temperature estimator

To reduce the costs affected by additional measurement circuitry for junction temperature assess, a model-based approach is investigated. A junction temperature estimator is designed, which targets to be as simple as possible by still achieving high bandwidth. For this reason, the junction temperature model, which has been introduced in section 3.3.1 is used. The estimator relies on three parts: An electrical model for the losses characterization of the semiconductors, a thermal model to estimate the heat propagation in the module and a narrow bandwidth case temperature measurement.

The thermal Foster network (as shown in Fig. 5.2) is used to model the thermal behavior of the power semiconductors in the power electronic module. For the model parametrization, the thermal impedance needs to be known and the losses of the power semiconductors represent the input variable. The losses can be derived with the knowledge of the operation point, which is defined by the current, the voltage, the switching characteristics and the conduction characteristics of the power semiconductors.

In order to apply the junction temperature estimation of (3.7) in real time, it is transferred into a differential equation and discretized. For a single order estimator based on the Foster circuit, this is shown in (5.1). In this equation  $T_{jc}$  describes the junction to case temperature,  $T_s$  the sampling period,  $C_{th}$  the thermal capacitance and  $R_{th}$  the thermal resistance. The index of the thermal resistance and the thermal capacitance stand for the parameters of the according RC element.

Table 5.1: Source of parameters for the estimator. **green**: parameter is constant over time; **orange**: parameter might be affected by aging

Parameter	Source
$E_{on}, E_{off}$	<b>datasheet</b> or <b>electrical characterization</b>
$r_{ce}, v_{ce,0}$	<b>datasheet</b> or <b>electrical characterization</b>
$R_{th,i}$	<b>datasheet</b> or <b>thermal characterization</b>
$\tau_i$	<b>datasheet</b> or <b>thermal characterization</b>

$$T_{jc}(k+1) = e^{-\frac{T_s}{R_{th,1} \cdot C_{th,1}}} \cdot T_{jc}(k) + \frac{T_s}{C_{th}} \cdot P_{loss}(k) \quad (5.1)$$

The same procedure is used to develop the second order estimator in (5.2) for the demonstration of the increase in mathematical complexity by only increasing the order of the estimator by one.

$$\begin{aligned} T_{jc}(k) = & T_{jc}(k-1) \cdot (e^{-\frac{T_s}{R_{th,1} \cdot C_{th,1}}} + e^{-\frac{T_s}{R_{th,2} \cdot C_{th,2}}}) - T_{jc}(k-2) \cdot e^{-\frac{T_s}{R_{th,1} \cdot C_{th,1}} - \frac{T_s}{R_{th,1} \cdot C_{th,1}}} \\ & + P_{loss}(k) \cdot T_s \cdot \left( \frac{1}{C_{th,1}} + \frac{1}{C_{th,2}} \right) - P_{loss}(k-1) \cdot T_s \cdot \left( \frac{e^{-\frac{T_s}{R_{th,2} \cdot C_{th,2}}}}{C_{th,1}} + \frac{e^{-\frac{T_s}{R_{th,1} \cdot C_{th,1}}}}{C_{th,2}} \right) \end{aligned} \quad (5.2)$$

The electrical and thermal parameters, which are needed for the model are summarized in table 5.1 with their possible sources. All required parameters of the electrical and thermal characteristics can be found in the datasheet or can be obtained with individual measurements. The switching and conduction characteristics can be obtained from a double pulse test and the thermal characteristics by measurement and fitting of the cooling down curve.

The total losses are derived as described in section 3.3.2 and fed to the thermal model for the junction temperature estimation, which is mathematically described by a convolution of the losses with the thermal impedance (as shown in (3.7)). This model calculates  $T_j$  based on the narrow bandwidth measurement of  $T_c$ . Therefore, the thermal impedance of the thermal grease  $Z_{th,ch}$  or the heat sink  $Z_{th,ha}$  are not needed in this thermal model.

### 5.2.3 Characterization and estimator parametrization

The electrical characterization is done for the Danfoss (DP25H1200T101667-101667,  $V_{ce} = 1200 \text{ V}$ ,  $I_c = 25 \text{ A}$ ) module with a double pulse test setup. The obtained characteristics of the losses are fit to the mathematical representation of the turn on losses, the turn off losses and the switching losses (3.10)-(3.12) to derive the losses of the system online.

The thermal characterization of the module is done by measuring the cooling curve after heating up the chips with a DC-current and turning off the power. A high-speed infrared camera

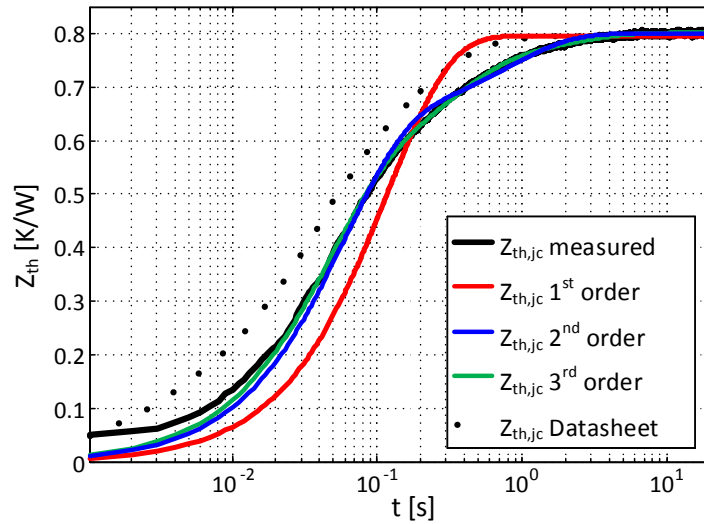


Figure 5.3: Thermal impedance measurement of IGBT 1 and fit to a different number of thermal chains with the parameters of table 5.2.

Table 5.2: Parameters of the thermal impedance obtained from the fitting curve in Fig. 5.3.

	$R_{th}$ [K/W]	$\tau$ [s]
<b>1 RC-Element</b>	0.7981	0.197
<b>2 RC-Elements</b>	[0.1532, 0.6521]	[2.4837, 0.0911]
<b>3 RC-Elements</b>	[0.5934, 0.1768, 0.042]	[0.0739, 1.0995, 11.7802]
<b>Manufacturer datasheet</b>	[0.09025, 0.3612, 0.2031, 0.1403]	[0.0023, 0.0282, 0.1128, 0.282]

is used to measure the IGBT junction temperature with high bandwidth and a curve fit with the Foster thermal network is done by using the least mean square algorithm. In the last step, the measured cooling curve is divided by the losses of the DC current to obtain the thermal impedance. The result for this thermal impedance is shown in Fig. 5.3 for different orders of RC-elements, achieving a different precision in the curve fit with the parameters in table 5.2. As it can be seen in the results, the second and third order thermal impedance obtain a good fit, whereas the first order estimator shows a deviation in the magnitude below periods of 1 s. In general, the higher order based estimators obtain the better fit with the measured thermal impedance. For a comparison with the parameters of a typical thermal impedance in a comparable module, the parameters of thermal resistors and time constants are shown in the table for the Infineon FP25R12KE3 module. In comparison with the other module, the thermal resistance is approximately equal, whereas the time constants are smaller.

In order to test the thermal model under realistic operating conditions, the estimator with the obtained parameters is tested with sinusoidal positive half wave excitation, which cor-

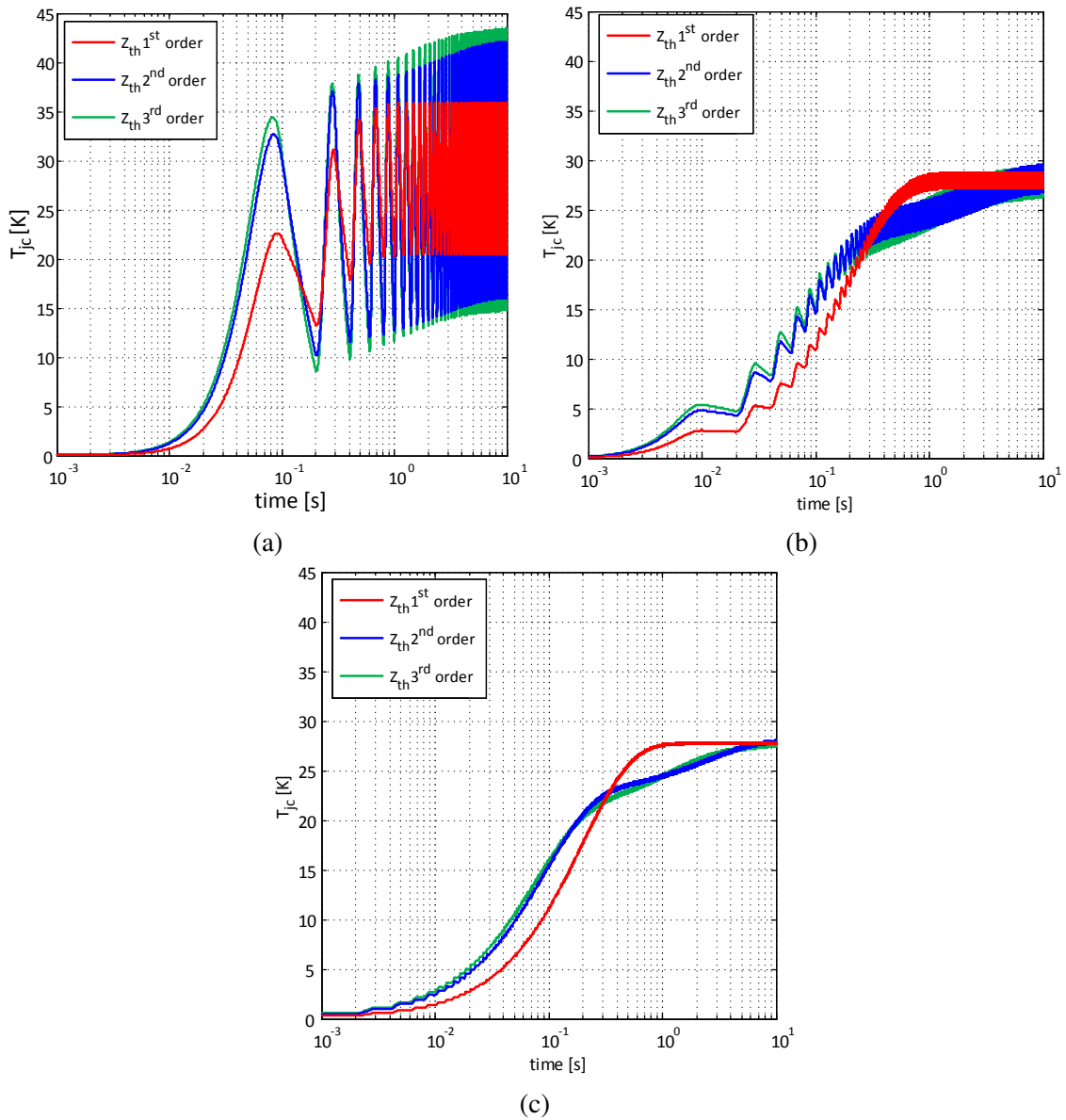


Figure 5.4: Simulation: Step response of the thermal impedances  $Z_{th,jc}(t)$  to sinusoidal power losses with different fundamental frequencies: (a)  $f_0 = 5$  Hz, (b)  $f_0 = 50$  Hz, (c)  $f_0 = 500$  Hz.

responds to the loading of power electronics in a converter with sinusoidal current. The response is shown in Fig. 5.4 for different fundamental frequencies of 5 Hz, 50 Hz and 500 Hz under equal average losses. Similar to the fit of the thermal impedance, the difference between the second order estimator and the third order estimator is low, whereas the first order estimator has a slower response than the others. For the fundamental frequency of  $f_0 = 5$  Hz, the thermal swing is high and it decreases for the case of  $f_0 = 50$  Hz and even more for 500 Hz. The magnitude of the thermal swing in the fundamental frequency is minimum for the first order estimator and maximum for the third order estimator. Remarkably, the steady state average temperature estimation is similar for the different estimator order in all cases.



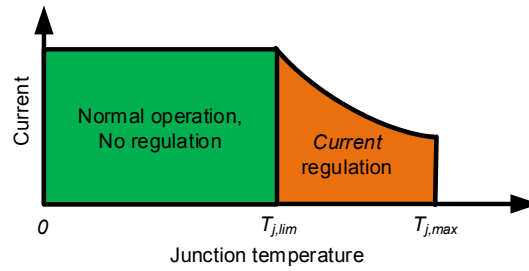
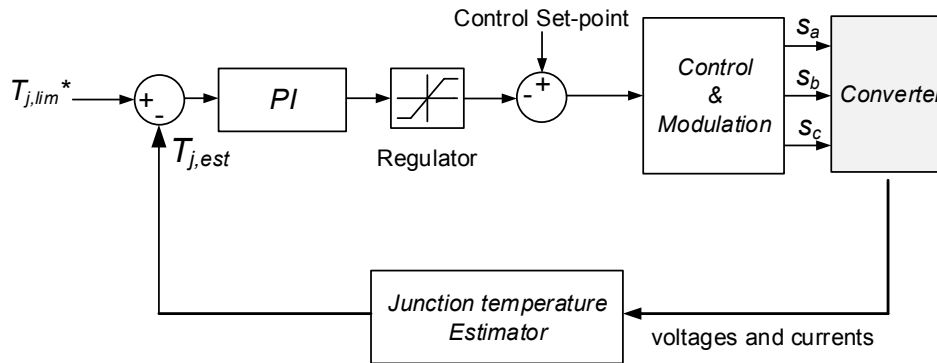


Figure 5.5: Region for the junction temperature regulation.

Figure 5.6: Control circuit of the PI control with temperature feedback for  $T_j$  regulation.

#### 5.2.4 Estimator based dynamic overtemperature protection

An excess of the maximum junction temperature  $T_{j,max}$  of an IGBT module causes destruction, e.g. by melting of the solder in the module. In order to prevent this, a dynamic junction temperature limitation is implemented, which is a simple active thermal control algorithm with protection capability. For not disturbing the normal operation, the limitation is only implemented for an excess of the chosen limited temperature  $T_{j,lim}$  as shown in Fig. 5.5 with different regions for the thermal controller. The advantage compared to an overall maximum current limitation is the capability to operate with an increased current until the thermal limitations of the system are reached. With respect to a maximum case temperature limitation, the dynamic response is much higher, which requires a smaller safety margin, consequently a better utilization of the power semiconductors. Furthermore, during high ambient temperatures, the junction temperature limitation is superior to a case temperature limitation, because a maximum case temperature limitation does not respect the power processed by the converter and thus does not model the temperature between junction and case. Therefore, it needs to be tuned for the worst-case conditions, whereby a junction temperature limitation can reduce the safety margin.

The limitation of the junction temperature is implemented with a PI-controller and tuned to regulate the temperature to a maximum by reducing the load current as shown in Fig. 5.6. It needs to be pointed out, that the thermal regulation has no impact when  $T_{j,est}$  does not exceed  $T_{j,lim}$ .

The control loop is modeled with the transfer function of the thermal impedance obtained from the cooling down curve in Fig. 5.3. After transforming them into the frequency domain,

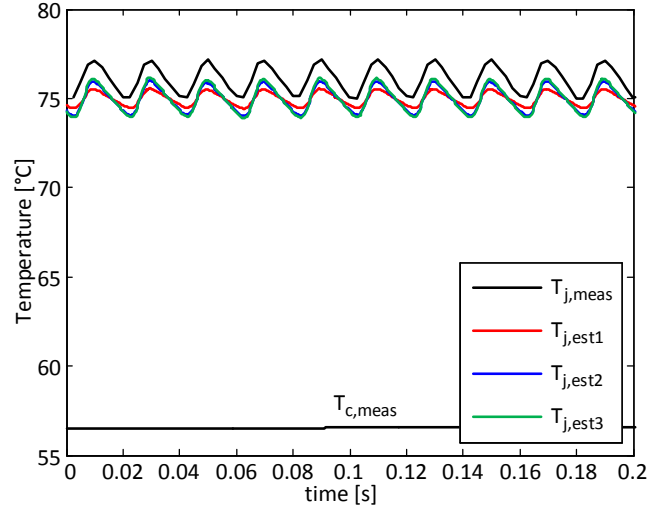


Figure 5.7: Measurement: Thermal cycling in the fundamental period (50 Hz) measured and modeled with different number of RC-elements.

the transfer function of (5.3) is obtained in dependence of the order of the approximation  $n$ .

$$G_{th,jc}(s) = \sum_{v=1}^n \frac{R_{thv}}{1 + s \cdot \tau_{thv}} \quad (5.3)$$

This results in a control loop only consisting of first order time delays, which can be controlled by a PI controller. The transfer function of this PI-controller is shown in (5.4).

$$G_{PI}(s) = k_p \cdot \left(1 + \frac{1}{s \cdot T_I}\right) \quad (5.4)$$

The tuning of the PI controller can be optimized in dependence of the requirement in terms of dynamic response and steady state behavior. Beside the requirement of fast dynamic response, another constraint can be the maximum allowable overshoot in the junction temperature. As a tuning algorithm for current controller, the technical optimum is well known for high dynamic response and is used to tune the controller in this work.

### 5.2.5 Validation of the junction temperature estimator

The estimator is implemented on a dSpace System driving a full bridge converter connected to a passive load with the parameters ( $R = 10 \Omega, L = 3.5 mH$ ). The DC-link voltage is set to  $V_{dc} = 400 V$ , the switching frequency to  $f_{sw} = 25 kHz$  and the fundamental frequency of the output voltage to  $f_0 = 50 Hz$ . For the validation of the estimator, the junction temperature is measured with an IR camera.

The estimators with first, second and third order are implemented and tuned with the parameters of table 5.2. All three estimators run in parallel for a comparison of the precision and potential delays in stationary conditions. The results are shown in Fig. 5.7, where  $T_{j,meas}$  is the measured junction temperature with a sampling frequency of  $f_{s,cam} = 400 Hz$

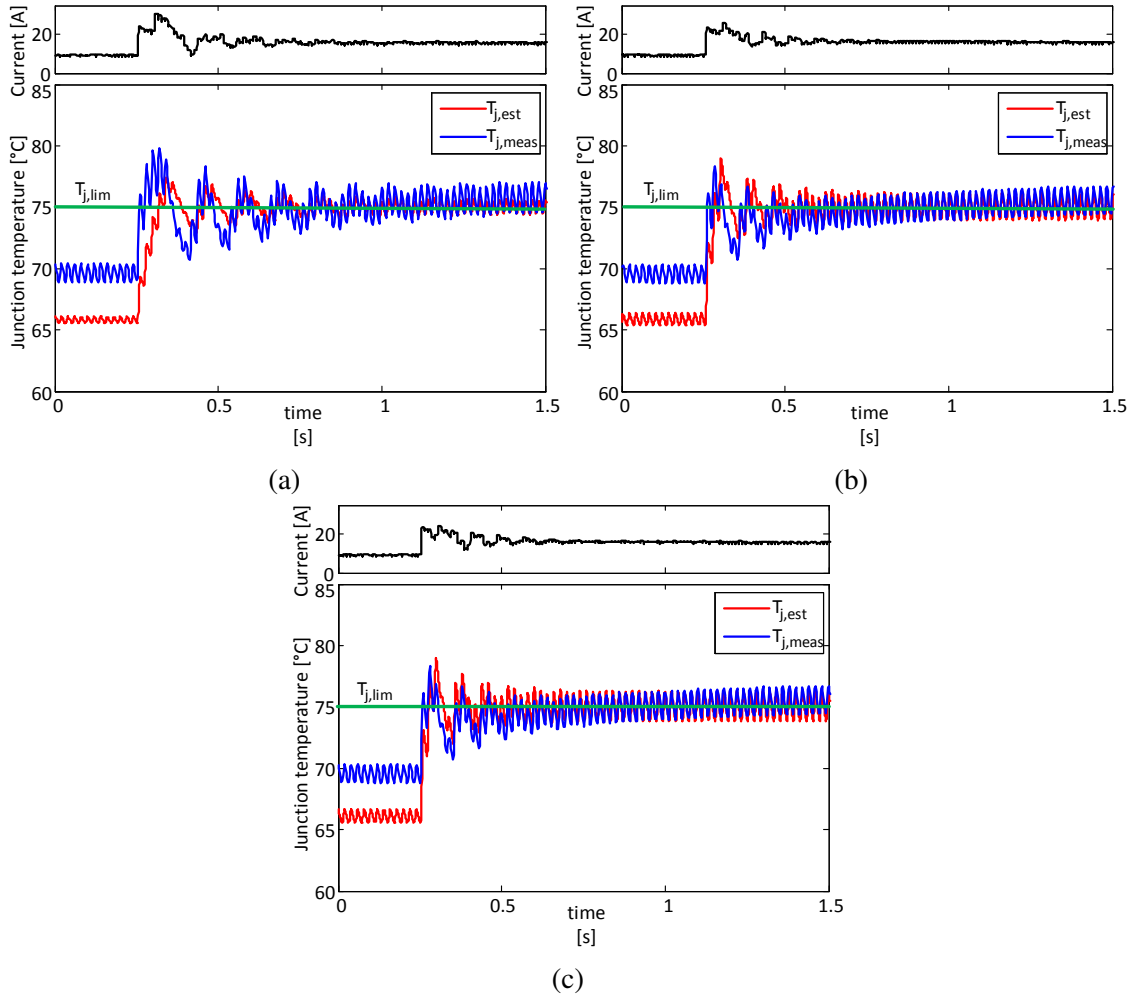


Figure 5.8: Measurement: Limitation of the junction temperature to  $T_{j,lim} = 75^{\circ}\text{C}$  by feedback of different order estimations: (a) Regulation with the first order estimation  $T_{j,est1}$ , (b) Regulation with the second order estimation  $T_{j,est2}$ , (c) Regulation with the third order estimation  $T_{j,est3}$ .

and  $T_{j,esti}$  is the temperature estimation with the estimator order  $i = \{1,2,3\}$ . The measured junction temperature has thermal cycles of  $\Delta T = 2\text{K}$  with an average junction temperature of  $T_{j,av} = 76^{\circ}\text{C}$ . Compared to the estimated junction temperature, the average temperature is  $1\text{K}$  higher than the average junction temperature  $T_{j,av} = 75^{\circ}\text{C}$ . Remarkably, the thermal swing in the fundamental period for the second and third order model is similar to the measured thermal swing. The thermal swing of the first order estimator is only  $\Delta T = 1\text{K}$ , which is lowest compared to the other models and fits worst whereas the results for the second and third order estimator are comparable.

The model is tested for the described dynamic limitation of the  $T_{j,lim} = 75^{\circ}\text{C}$  and the results for the control system modeled with the different order are shown in Fig. 5.8. During stationary conditions, a step variation in the output power occurs, which leads to higher losses and consequently an increase of the junction temperature. Without the limitation, the junction temperature would exceed  $T_{j,lim}$ , which affects the reliability. To prevent this, the limitation is tested by using the estimators of different orders.

For the junction temperature estimation of the first order estimator, shown in Fig. 5.8 (a), the response of the estimator is slower than the measured junction temperature. Due to the resultant delay, the regulation of the current is causing an oscillation in the output current and the junction temperature. This causes additional thermal stress. Instead, the junction temperature regulation with the estimators of second order, shown in Fig. 5.8 (b), and the third order estimation, demonstrated in Fig. 5.8 (c), show a faster response. The response of the second and third order estimator is very similar and the overshoot is smaller compared to the first order feedback. In all cases, the stationary junction temperature limitation holds with a deviation of maximum  $1 K$  to the mean value.

The first order estimator can be used for junction temperature estimations, but is problematic in active thermal control applications, where high dynamics are required. Instead, the second and third order estimator achieve a good fit with the measured thermal response. The second order estimator is considered to fit best, because its performance is comparable to the third order estimator, while the calculation effort is lower.

As a result, the dynamic behavior of the estimator has been demonstrated to fit the physical behavior. Nevertheless, in operation points, where other effects like thermal cross coupling with other power semiconductors are affecting the junction temperature, it is expected, that there are differences between the estimated and the measured junction temperature.

### 5.3 Control of the converter's loading in photovoltaic application

Similar to the thermal stress for the power semiconductors in the ST, the grid connected photovoltaic converters undergo thermal stress caused by the variation of the irradiance, whereby they need to operate reliably for a long lifetime. As a difference to the ST, the PV system is consisting of a lower number of power semiconductors and the mission profile is well known. For this reason, thermal stress is investigated for PV converters and active thermal control is applied to reduce the thermal stress. In PV-systems, the optimization of the energy harvesting during fast variable irradiance conditions has been an active area of research and of competition among the companies. However, the proposed fast MPPT algorithms can produce extremely variable loading of the power semiconductors resulting in a decrease of the system's lifetime, which in consequence can nullify the economic advantage of higher energy harvesting. This subsection analyzes the problem and proposes a multi-objective MPPT, which limits the positive temperature gradient and the maximum junction temperature of the power semiconductors. The algorithm is introduced and fully validated experimentally with a mission profile emulating variable irradiance conditions.

#### 5.3.1 Introduction to photovoltaic power converters

Photovoltaic power plants are built worldwide to increase the renewable energy production and power electronics are a key factor for their grid integration [140]. To amortize their high manufacturing costs, these systems need to harvest maximum power for lifetimes of 20 years. These goals, maximum energy and long life, which later will be demonstrated as conflicting, had push tremendously the research towards more performing MPPT algorithms [141, 142] and more efficient and robust power electronics solutions [143, 70]. The MPPT strategies offer different advantages with respect to tracking speed, complexity and performance under partial shading conditions, whereby the maximization of the energy harvesting is important to justify the cost of a PV system. However, the possible failure of the power converter is also influencing the cost of PV energy. In literature, an analysis is done for the reliability critical parts of the photovoltaic system [70]. The reliability of several components, different MPPT algorithms and anti-island schemes is evaluated, but no action is taken to improve the algorithms with respect to reliability. In the following, a "lifetime-optimized" MPPT to control the stress of the power electronics in the DC/DC converter is proposed. The thermal effects of traditional MPPT algorithms are analyzed and an algorithm is introduced, which reduces the thermal stress during fast changing irradiance and limits the maximum junction temperature.

#### 5.3.2 Mission profile and system description

The ambient temperature and the irradiance profile define the mission profile of the power semiconductors in PV application. To evaluate the relevance of the varying irradiance and its impact on semiconductor's lifetime, in Fig. 5.9 the irradiance is measured and displayed for

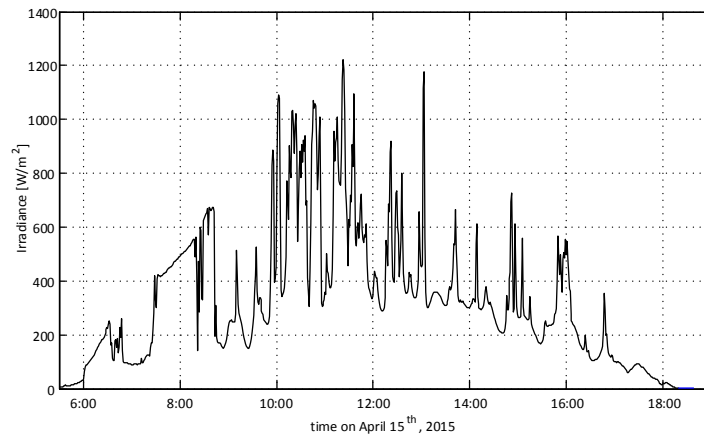


Figure 5.9: Time profile of changing irradiance [144].

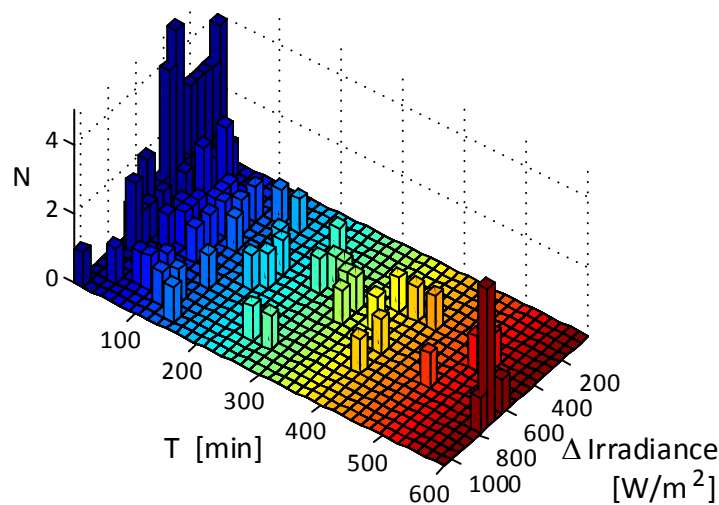


Figure 5.10: Rainflow counted cycles of changing irradiance in 5.9.

one day in 1 *min* average values. The sun is rising before 6 am and increases the irradiance until its maximum around 11:45 until it sunset at approximately 18:30. The irradiance is rapidly changing with various different magnitudes and periods during the whole day. To better identify the cycles in the profile, Rainflow counting is applied and presented in Fig. 5.10 in dependence of the irradiance cycles and the period of the cycles. In the profile, it can be seen that different magnitudes of irradiance are well distributed in the profile, whereby the relatively short periods with less than one hour are predominant. However, time periods of 1 *min* might not be sufficient to detect all fast changes in the irradiance and there might even be more cycles in the profile.

Photovoltaic power plants have challenged the engineers to reduce the ground leakage currents, achieve high-energy conversion efficiency and to comply with international regulations. [145]. For cost efficiency of a PV power plant, the maximum energy from the array needs to be harvested. To extend the operation range, often a boost converter is used to step-up the voltage to the level of the DC-link voltage. The structure of a single-phase one and double-stage PV system is shown in Fig. 5.11. The MPPT of the two-stage converter in this work is performed by control of the duty cycle  $d$ , which is expressed by the ratio of the turn

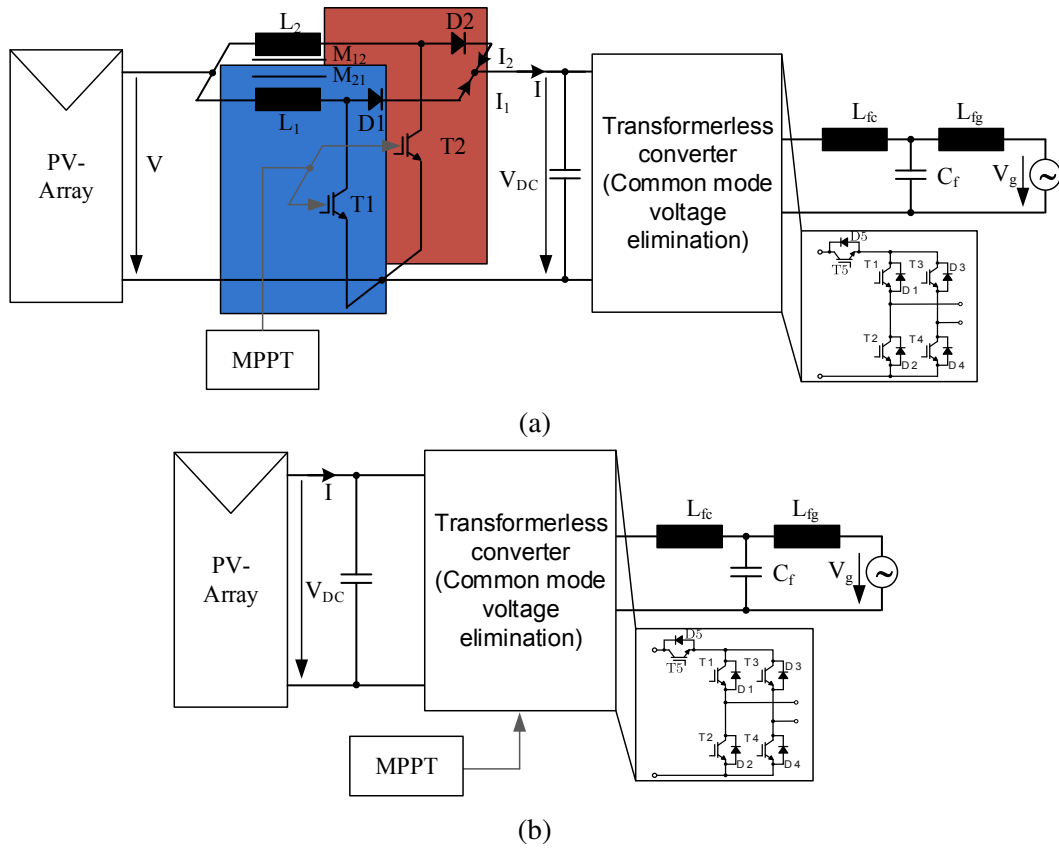


Figure 5.11: Single-phase grid connected PV converter: (a) with boost converter, (b) without boost converter.

on time of the IGBT  $t_{on}$  and the sampling time  $T_s$  or with the PV array voltage  $V$  and the DC-link voltage  $V_{dc}$  as shown in (5.5). Contrary, the MPPT of the single stage PV converter is performed by current control of the converter.

$$d = \frac{t_{on}}{T_s} = 1 - \frac{V}{V_{dc}} \quad (5.5)$$

To perform MPPT, the controller needs to have information about the current operation point of the PV array and at least the current and voltage measurements of one additional operation point. To obtain the voltage and current measurement of the second set point, the actual operation point needs to be changed, which changes the losses of the system and thus causes a thermal swing  $\Delta T$ . The thermal swing depends on the MPPT algorithm, which normally implies the control of the current or the voltage of the PV array. Thereby, the thermal swing caused by the perturb and observe algorithms are expected to be low, whereas the measurement of the short circuit current or the open circuit voltage are expected to cause severe thermal stress. The optimal point of operation is changing with the irradiance and thus over the time. On days with fast passing clouds, the irradiance is varying fast and thus the optimal set point for the MPPT changes, too [146]. The passing clouds cause power cycling for the power semiconductors and thus cause additional thermal cycles of the junction temperature, which reduces their lifetime. Independently from the chosen topology, the variation of the irradiance causes thermal cycles, which is shown in Fig 5.12 (a) for a two-stage PV

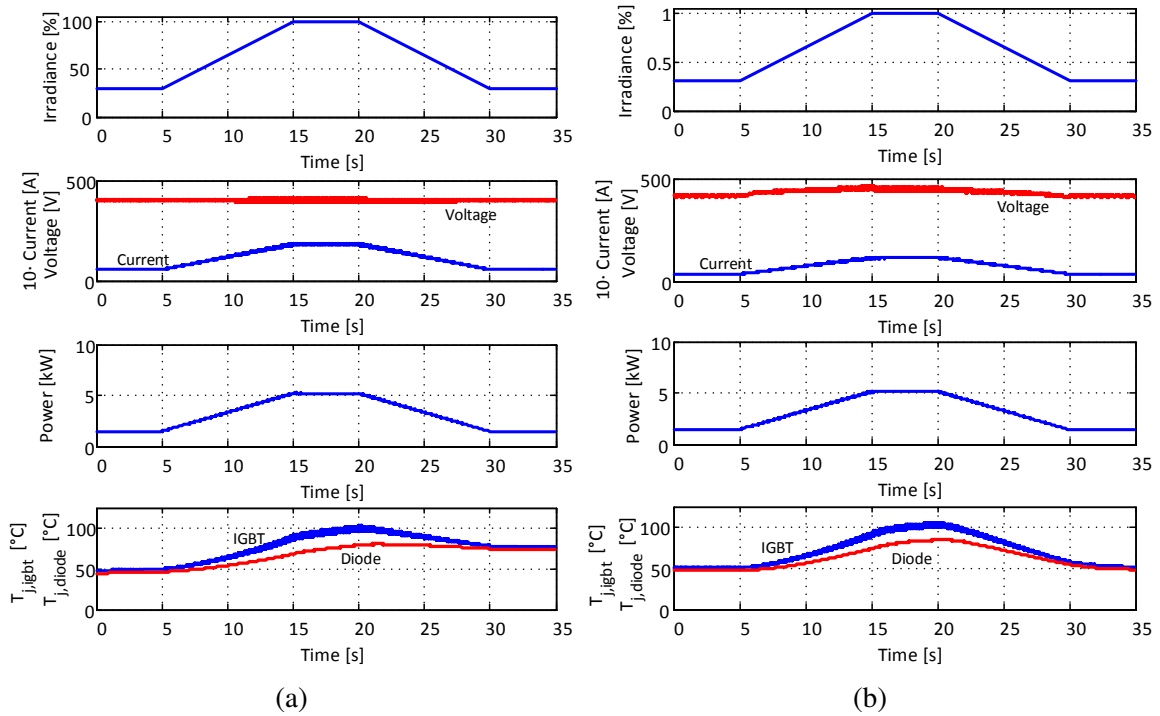


Figure 5.12: Simulation of thermal stress of a single-phase PV converter for a trapezoidal change of the irradiation: (a) two-stage converter, (b) single-stage converter.

power plant and in Fig. 5.12 (b) for a single-stage PV power plant as shown in Fig. 5.11 with the parameters of table 5.3. For the comparison, both plants are connected to the same PV power ( $P_{PV} = 5.2kW$ ), but in the double-stage plant, the number of parallel connected strings is higher to utilize the boost function of the converter. The irradiance is changed trapezoidal from 30 % to 100 % and back to 30 % as done in standard test conditions. Because of the variation of the DC-link voltage in the single-stage, the results can only partially be compared, but the affected thermal swing on the IGBTs is approximately  $\Delta T = 55K$  for the two-stage system and  $\Delta T = 60K$  for the single-stage system. Thus, the problem of thermal cycling is relevant for both topologies: the single-stage and double-stage suffer from the same problems regarding thermal stress. In the following, the analysis based on the two stages and the DC/DC control will be carried on. A similar analysis could be extended to the single-stage by modifying the grid current set point. However, the double-stage system is taken for the analysis due to its wide application in small PV power plants, which suffer most of the fast changing irradiance due to small area the PV arrays cover.

In literature many MPPT algorithms can be found, whereby most of them can be categorized in the following basic schemes [147]:

- Open voltage measurement or short circuit current measurement
- Temperature based
- Curve sweeping
- Perturb & Observe (P&O) or incremental conductance



Table 5.3: Simulation parameters for the thermal stress comparison of the PV converter topologies.

Variable	Value single stage PV power plant	Value two-stage PV power plant
Grid frequency $f_g$	50 Hz	
Grid voltage	230 V rms	
Filter capacitance $C_f$	2.2 $\mu F$	
Grid side inductance $L_{fg}$	1 mH	
Converter side inductance $L_{fc}$	6.9 mH	
Irradiance	1 kW/m <sup>2</sup>	
DC-link voltage $V_{dc}$	variable	400 V
Open circuit PV voltage $V_{oc}$	552 V	353 V
Short circuit PV current $I_{sc}$	12.75 A	20 A

These algorithms have advantages and disadvantages with respect to tracking speed, detection of partial shading conditions or thermal stress for the power semiconductors. Concerning the thermal stress, short circuit current measurement is known to be problematic for the lifetime of the system. To overcome a disadvantage of one scheme, algorithms can be combined e.g. [142]. However, not only the advantages sum up: also the disadvantages, such as thermal stress of short circuit current needs to be considered. The thermal stress of the four above mentioned MPPT algorithms can be analyzed theoretically. The measurement of the open circuit voltage ( $d = 0$ ) or the short circuit current ( $d = 1$ ), causes a variation of thermal stress and thus thermal cycling. Worst from the point of thermal stress is curve sweeping, because the whole curve from  $d = 0 \dots 1$  is passed through for the MPPT and thus minimum load and maximum load is applied every time the algorithm is run, leading to significant stress. Instead, when the P&O algorithm is operating in the MPP, only low thermal stress is expected during constant irradiance. As it will be demonstrated later in this work, the MPPT with a temperature measurement may not detect the maximum power point, which reduces the harvested energy. Thus among the considered MPPT strategies, the P&O is expected to be the best from the point of thermal stress. Other algorithms behave in a similar way and avoid large power swings.

### 5.3.3 Lifetime corrected MPPT

In the following, the P&O algorithm will be used as a base for the thermal stress control due to its wide use in PV converters. The topology and the implementation of the active thermal control algorithm with its control variable are shown in Fig. 5.13 (a). Furthermore, in Fig. 5.13 (b) the conditions are shown, in which the thermal stress reduction is applied. During fast changing radiation a positive temperature gradient limitation  $\Delta T_{j,max}$  is applied and for high load operation a maximum junction temperature limitation  $T_{j,max}$  is implemented. These targets can be set at the same time without conflicting with each other. The first goal to reduce thermal cycling during fast changing irradiance is implemented by limiting the

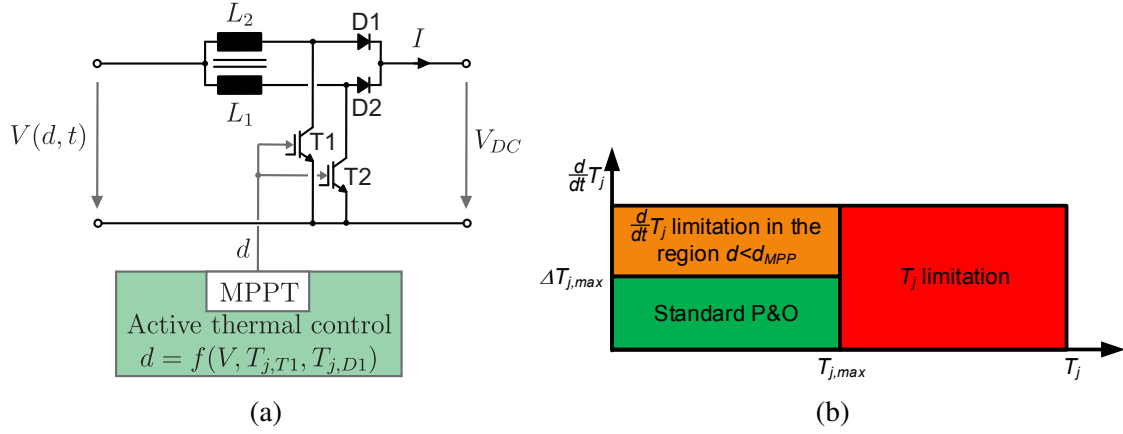


Figure 5.13: Implementation of the proposed active thermal control algorithm: (a) Considered topology and implementation of the algorithm, (b) Regions for application thermal stress reduction.

positive temperature gradient at the price of a slower and less energy efficient MPPT. The gradient is chosen because of the unpredictable behavior of passing clouds, which reduce the irradiance in fast changing weather conditions. In case of a shaded PV array and dispersing clouds, it is not certain how long it takes until the next cloud shadows the array. The temperature gradient limitation shows the advantage not to influence the operation on a sunny day for an adequate temperature gradient  $\Delta T_{j,max}$ , but prevents excessive thermal swings during fast changing irradiance.

Furthermore, in contrast to the power gradient, the junction temperature gradient addresses the cause of the failure mechanism and is not influenced by the nonlinear PV characteristics in the current source or voltage source region. This is also important for thermal cycling during varying irradiance, because the junction temperature can still cool down while the power is already increasing again. The second control target, the limitation of the maximum junction temperature  $T_{j,max}$ , is used to achieve maximum utilization of the power semiconductors, by guaranteeing not to exceed the maximum junction temperature. This mechanism enables de-rating of the components, which reduces system costs. A flow chart shows the realization of the overall MPPT based on the P&O algorithm in Fig. 5.14. At the beginning of the algorithm, the electrical ( $V_{dc}$ ,  $I_k$  and  $P_k$ ) and thermal ( $T_{j,T}$  and  $T_{j,D}$ ) properties are sampled and updated. From the duty cycle and the DC-link voltage, the PV- array voltage can be derived as shown in (5.5).

The positive temperature gradient limitation is applied in the region  $d < d_{MPP}$  by means of a tolerance band in which the temperature can vary before the controller limits the energy harvesting. An advantage of this scheme is low influence of the noise related to the temperature measurement during normal operation. The first condition of the MPPT algorithm is to check the temperature limitations. In case of a violation of the maximum temperature gradient or the maximum temperature,  $d$  is increased to reduce the output power. A high increase is made in the case of power point tracking in the current source region ( $d > d_{MPP}$ ) because of the reduced thermal stress in this region. If no temperature violation is detected, the normal P&O algorithm is carried out with the comparison of the power variation and the

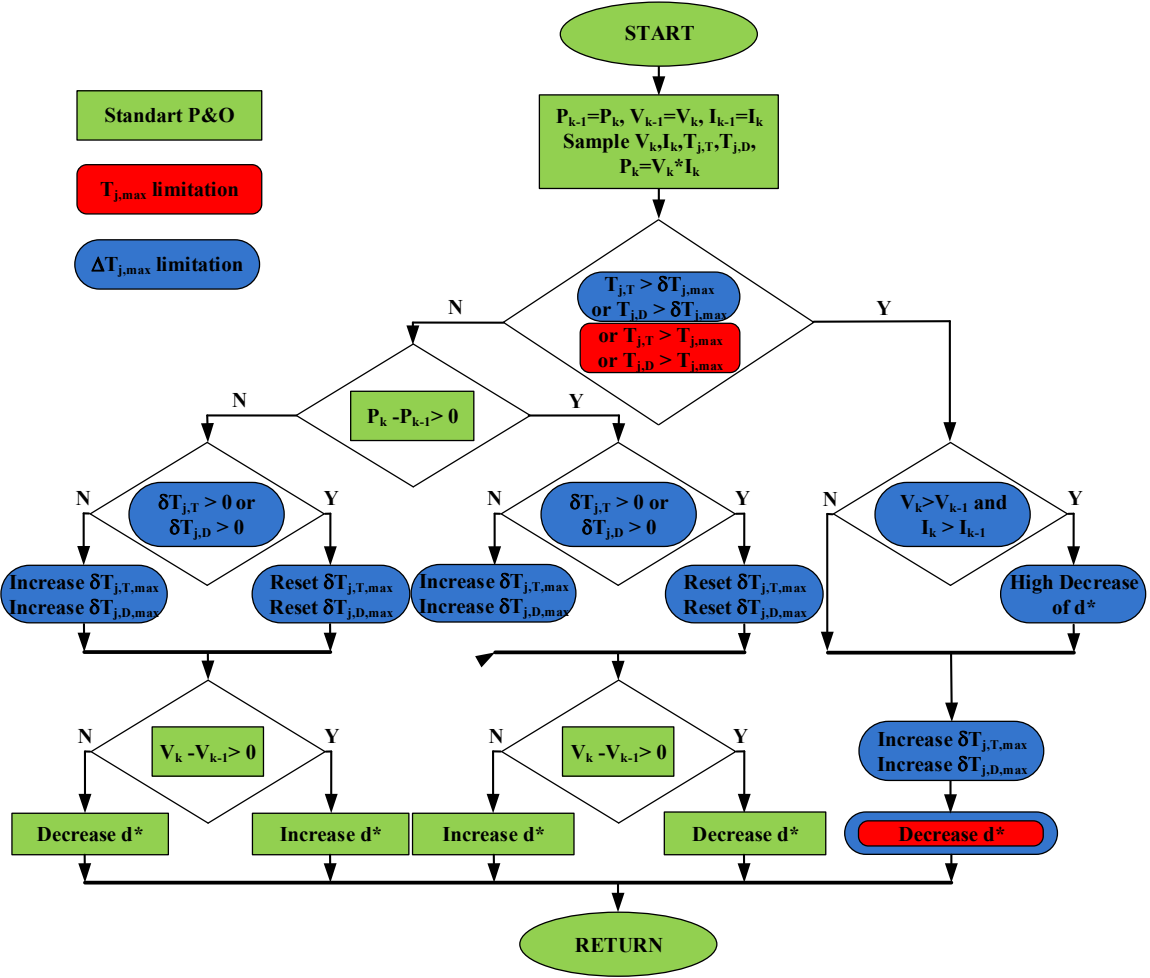


Figure 5.14: Flow chart of the thermal stress reduced and maximum junction temperature limiting maximum power point tracking algorithm.

voltage variation. Additionally, the new thermal limitation for the next maximum temperature gradient limitation needs to be set. This part is independent from the power variation, but in the case of a temperature decrease, the new maximum temperature of the next step is set to the temperature given by the gradient limitation. Otherwise, for increasing temperatures, the new maximum temperature is the sum of the old maximum temperature and the applied gradient. In (5.6) the mathematical expression is shown.

$$\delta T_{j,max} = \begin{cases} T_{j,max} + \Delta T_{j,max} \cdot T_{mppt} & \frac{d}{dt} T_j(t) > 0 \\ T_j + \Delta T_{j,max} \cdot T_{mppt} & \frac{d}{dt} T_j(t) < 0 \end{cases} \quad (5.6)$$

### 5.3.4 Tuning of the proposed algorithm

The irradiation on the PV panels defines the mission profile of the PV converter and thus the thermal stress for the power semiconductors. These irradiation characteristics are influenced by the unpredictable passing clouds. Despite the uniqueness of each measured irradiance profile, the general characteristics are similar. An example of an irradiance measurement

Table 5.4: Time constants of the PV system.

Property	Time constant
$T_{mppt}$	50ms
Slowest time constant of the thermal impedance of power semiconductors	282ms
Variations in the irradiance	$> 1 s$
Time to MPP (of the applied algorithm)	$\approx 5 s$
Expected cloud speed	$> 8 m/s$

Table 5.5: Potential estimation for the thermal stress reduced MPPT in case of fast varying conditions (13% of time in a year).

Proposed temperature gradient limitation [K/s]	Yearly reduction of energy harvesting using the modified MPPT [%]	Stress reduction under varying irradiance [%]
0.5	[0.8, 1.1]	[0, 41]
0.33	[1.6, 2.8]	[33, 83]

with high sampling time is presented in [20]. The irradiance in Tallinn is measured with a sampling rate of 1 s for 2.8 h. This study illustrates the frequency distribution of 150 illumination windows in cloudy conditions, whereby 2/3 are in the high irradiance region. Furthermore, out of all windows, 2/3 were shorter than 65 s and 1/3 were even shorter than 23 s. These fast varying irradiance conditions are addressed in few publications, which optimize the maximum power point tracking without taking into account the damage caused on the system. Considering this damage and cloud speeds higher than 8 m/s, even large PV power plants suffer from high thermal stress under fast changing irradiance. In table 5.4 the time constants, which are influencing the process are shown as well as expected cloud speed to highlight the relevance of the thermal stress during fast changing irradiance. The important time constants are the maximum power point tracking speed, the varying irradiance and typical large time constants of thermal impedance (junction to case) in power electronic modules. The smallest time constant is the MPPT period, whereby also the thermal impedance has a relatively small time constant. However, it should be considered, that passing cloud fronts, which are shading the PV panels smooth the variation in irradiance.

To evaluate the potential of thermal stress reduction by MPPT, the described weather conditions of [148] are used to estimate how much the thermal stress can be reduced for which cost of energy. The fast changing clouds were measured in 13% of the time, which corresponds to the potential, when the MPPT algorithm can reduce the thermal stress. For the potential estimation, two different positive junction temperature gradients are considered for the algorithm and shown in table 5.5. The gradients are assumed to require 23 s and 65 s respectively to the MPP. This enables to analyze best case and worst-case scenarios for the reduced energy harvesting and lifetime extension during this profile. This leads to a reduction of 0.8 – 1.1% of the harvested energy for the higher maximum junction temperature gradient and 1.6 – 2.8% for the smaller maximum gradient. For a rough estimation about

Table 5.6: System parameters of the laboratory setup.

Variable	Value
Switching frequency $f_{sw}$	15 kHz
Irradiance	1 kW/m <sup>2</sup>
DC-link voltage $V_{dc}$	380 V
$L_1 = L_2 = M_{12} = M_{21}$	3 mH
Open circuit voltage $V_{oc}$	180 V
Short circuit current $I_{sc}$	10 A

the reduced thermal stress, the linear damage accumulation (5.7)-(5.8) is used with the irradiance instead of the temperature and the possible reduction in the cycles. Furthermore, the described severe thermal cycles, which can be manipulated by the MPPT, are assumed to obtain similar magnitude and their periods are equally distributed. This results in a stress reduction of up to 41.2% for the higher maximum junction temperature gradient and up to 82.8% for the smaller gradient.

$$N_f = a_1 (\Delta T)^n \cdot e^{\frac{a_3}{T_{j,av}}} \quad (5.7)$$

$$C = \sum_{i=0}^{\inf} \frac{n_i}{N_i} \leq 1 \quad (5.8)$$

To demonstrate the effectiveness of the proposed MPPT algorithm, the behavior is tested in three different conditions:

- Steady-state operation
- A step-variation in the overall maximum junction temperature
- The temperature gradient limitation for a high increase in the irradiance.

The influence of the MPPT on the thermal stress is tested on a PV system with a boost inverter in continuous current conduction mode. A PV emulator is used to emulate the PV array and the boost converter is operated in interleaved mode. The system parameters are shown in Table 5.6, whereby the maximum power point is set to  $V_{MPP} = 160$  V and  $I_{MPP} = 9.5$  A. In the boost converter, a Danfoss (DP25H1200T101667-101667) open IGBT module is used and the junction temperature measurement is done with a high bandwidth optic fiber measurement system, which is directly fed back into the used dSpace 1006 system. The DC-link is controlled by an electronic load. For thermal stress analysis, the junction temperature of the IGBT T1, the Diode D1 and one spot on the passive heat sink are measured and displayed in Fig. 5.15 with the parameters of table 5.6 for a variation of the duty cycle  $d$ . The system is driven with each  $d$  until it reaches approximately steady-state conditions. This requires a substantial long time, because the heat sink needs a long time to reach thermal steady-state. Remarkably, the Maximum Power Point (MPP) with the duty cycle  $d_{MPP}$  is not the point with the maximum temperature for the power semiconductors. The thermal

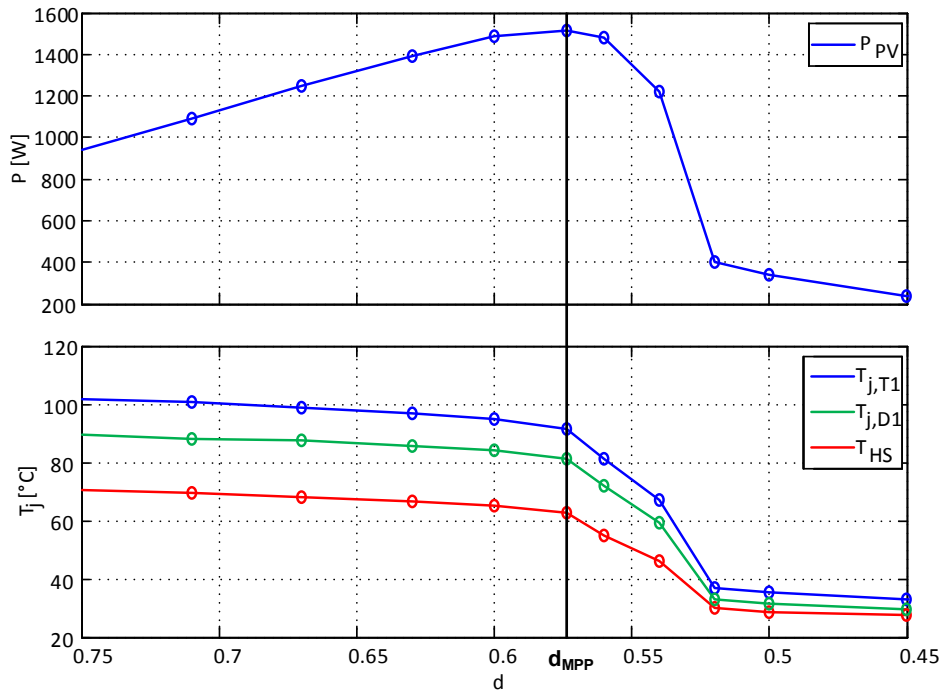


Figure 5.15: Measured PV output power and junction temperature of the power semiconductors of the boost converter for varying duty cycles and constant irradiance.

stress increases with an increase of the duty cycle, which can be explained with an increase of the current ripple and a decrease in the DC part, which leads to a lower root mean square value of the current. Thus, the current ripple needs to be minimized in operation, which is achieved in the MPP. In general, the diode is colder than the IGBT and the temperature difference between the power semiconductors and the heat sink temperature increases with the temperature of the power semiconductors. Furthermore, the operation points with equal power transfer for  $d > d_{MPP}$  are more stressing than for  $d < d_{MPP}$ . The heat sink temperature even reaches  $70\text{ }^{\circ}\text{C}$  compared to  $62\text{ }^{\circ}\text{C}$  in the MPP.

For demonstrating the effectiveness of the maximum temperature limitation, the system is operated without thermal limitations until it reaches thermal steady-state conditions for an MPPT period  $T_{MPPT} = 50\text{ ms}$ . This is shown in Fig. 5.16, where at  $t = 2\text{ s}$  the temperature limitation is changed from  $T_{j,max} = 110\text{ }^{\circ}\text{C}$  to  $T_{j,max} = 85\text{ }^{\circ}\text{C}$ . Displayed are the junction temperatures of one IGBT and one Diode, the heatsink temperature, the array current and the duty cycle. The maximum temperature reference step forces the MPPT to decrease the duty cycle, which at the same time reduces the PV current and thus the temperature. The cooling down can be seen from  $2\text{ s}$  until  $t = 8\text{ s}$ . Afterwards the duty cycle is increased again until the temperature limitation is violated. In steady state this leads to an oscillation of the output power and a consequent oscillation of the junction temperatures, which can be seen in the profile of the currents  $I$ . This oscillation can be reduced by either reducing the step size of the MPPT or the execution period  $T_{mppt}$ . The disadvantage is a slower tracking of the MPP, which is undesired. The diode has a lower temperature than the IGBT in the whole experiment and the temperature of the heat sink changes only marginally.

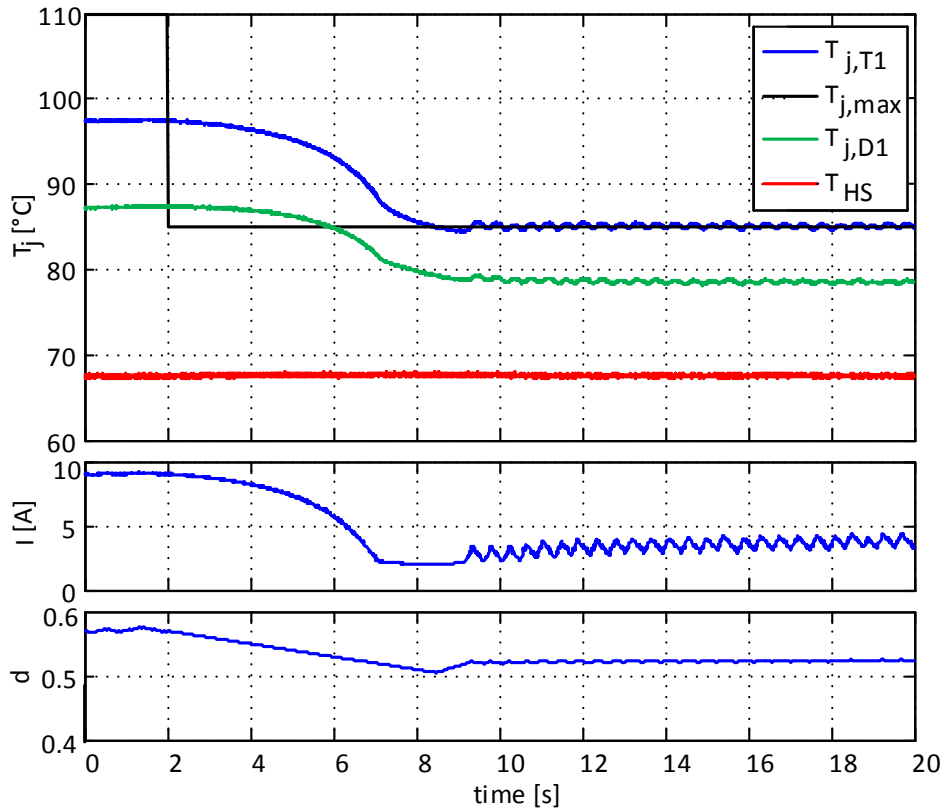


Figure 5.16: Behavior of the MPPT for a step in the maximum junction temperature  $T_{j,max} = 110^{\circ}\text{C} \rightarrow T_{j,max} = 85^{\circ}\text{C}$  and  $T_{mppt} = 50\text{ms}$ .

Next, the junction temperature gradient limitation is tested. To achieve a sufficient increase in the temperature, the irradiance is set to  $P_{PV,rel} = 10\%$  and increased in a step to  $P_{PV,rel} = 100\%$ . This experiment is done for standard MPPT and for  $\delta T_{j,max} = \{1, 0.5, 0.33\} \text{K/s}$ . In the following  $\delta T_{j,max} = 1 \text{K/s}$  corresponds to Modified MPPT 1,  $\delta T_{j,max} = 0.5 \text{K/s}$  corresponds to Modified MPPT 2 and  $\delta T_{j,max} = 0.33 \text{K/s}$  corresponds to Modified MPPT 3. The results are shown in Fig. 5.17 for the junction temperature of the IGBT, which was discovered to reach the highest temperature in the boost converter. Without the gradient limitation, the MPPT directly detects the new maximum power point after 5 s, while the temperature of the IGBT rises quickly. The maximum temperature gradient limitation holds in all cases and the maximum power point is reached after 13 s, respectively 28 s and 58 s. Even if the most stringent temperature gradient limitation of  $\delta T_{j,max} = 0.33 \text{K/s}$  holds, the instantaneous increase of the temperature for an increase of the duty cycle is challenging the algorithm. This sets the limit for the smallest junction temperature gradient in this system, whereas for different parameter tuning and measurement equipment the result will vary.

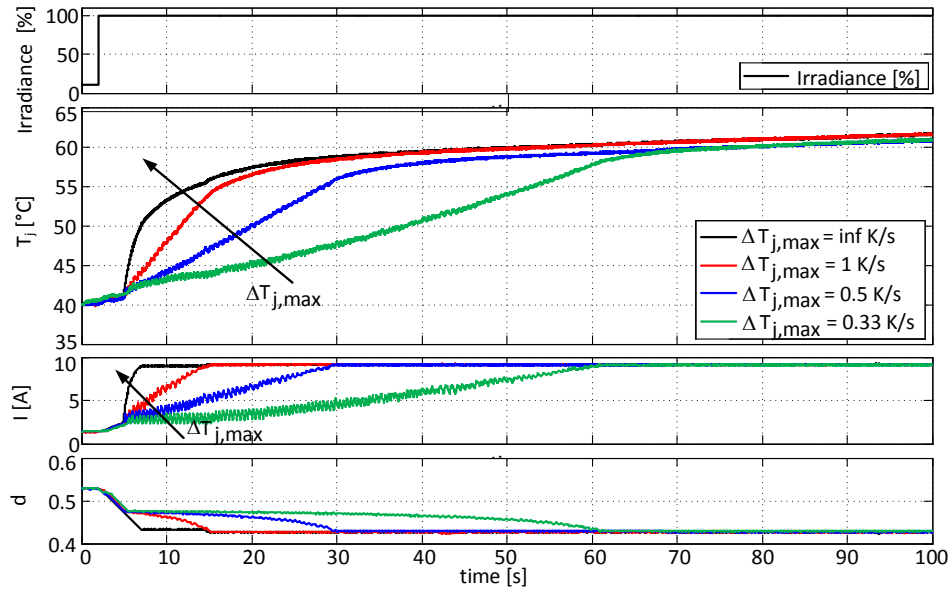


Figure 5.17: Behavior of the MPPT for a step in the irradiance  $P_{PV,rel} = 10\% \rightarrow P_{PV,rel} = 100\%$  for different temperature gradients and normalized starting temperature in one IGBT.

### 5.3.5 Lifetime evaluation of the proposed algorithm

To evaluate the behavior of the controller during unpredictable changes in the irradiance, a 620s mission profile as shown in Fig. 5.18 is created and the thermal controller is tuned with the similar temperature gradients as in the previous experiment to investigate the tradeoff between reduced thermal stress and maximum power harvesting. Compared to the standard for MPPT profile testing [149], the irradiance profile is changed to have short ramp up/down times and different magnitudes and periods to see the behavior under different conditions.

Standard trapezoidal MPPT testing profiles were not used because they would lead to a repetition of the temperature profiles, whereas the used profile shows the response to different variations in frequency and irradiation cycles. Thereby, the driving cycles for electric vehicles with their different conditions seem to be a suitable analogy. The profile is characterized by irradiance cycles with periods of 4s and 50s, which is within the time affected by the thermal controller as shown in Fig. 5.18 and similar junction temperature gradient limitations  $\delta T_{j,max} = \{1, 0.5, 0.33\} K/s$ . To evaluate the achieved benefits and the costs for the MPPT algorithm, an estimation of the lifetime consumption needs to be made. The mathematical model of the LESIT results is used in combination with linear damage accumulation as described in (3.1)-(3.3). The Rainflow counting algorithm is applied to extract the thermal cycles from the mission profile. The histograms with 20 boxes with a width of 1K for the thermal swings of all tunings are shown in Fig. 5.19.

The higher the magnitude of a cycle, the higher is its impact on the lifetime consumption. Without the temperature gradient limitation, the histogram shows one cycle for the magnitudes  $\Delta T = \{18, 16\} K$  and 2.5 cycles with a magnitude of  $\Delta T = \{12, 13\} K$ . Furthermore, there is one cycle at  $\Delta T = 10K$  and 5 cycles with a magnitude  $\Delta T < 5K$ . For the tempera-



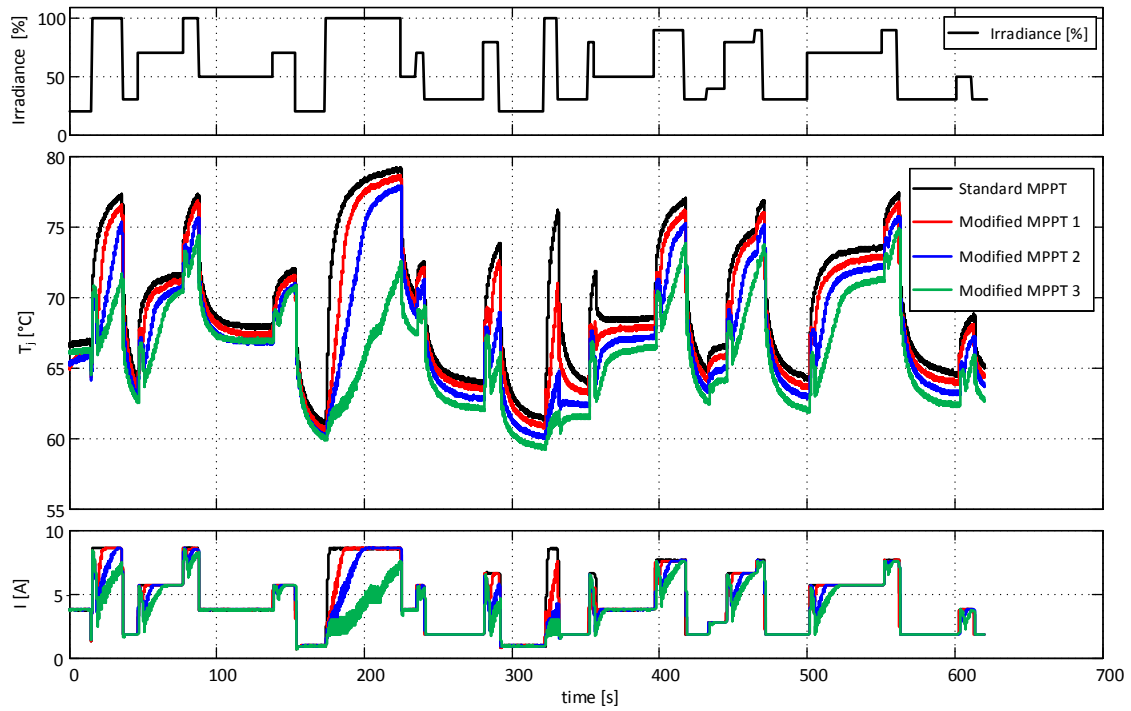


Figure 5.18: Comparison of the MPPT for different temperature gradients during a 620s mission profile with the parameters of Table 5.6.

ture gradient limitation with the modified MPPT 1, the high magnitudes are remaining, but one cycle with a magnitude of  $\Delta T = 13 K$  is reduced and a new cycle at  $\Delta T = 8 K$  is new in the histogram. Caused by the implementation of the temperature gradient limitation in this work, there are 10 cycles with a magnitude of  $\Delta T < 5 K$ , which means there are five new thermal cycles with low magnitude. This is caused by the step in the irradiance, which brings the operation point of the former MPP in the current source region. From here, the MPPT algorithm is driven into the voltage source region, because of the demonstrated higher stress before the new MPP is tracked again. For the more stringent temperature gradient limitation, a better reduction of the thermal cycles with high magnitude is achieved. Especially in the case of the modified MPPT 3, a considerable shift from high magnitude thermal cycles

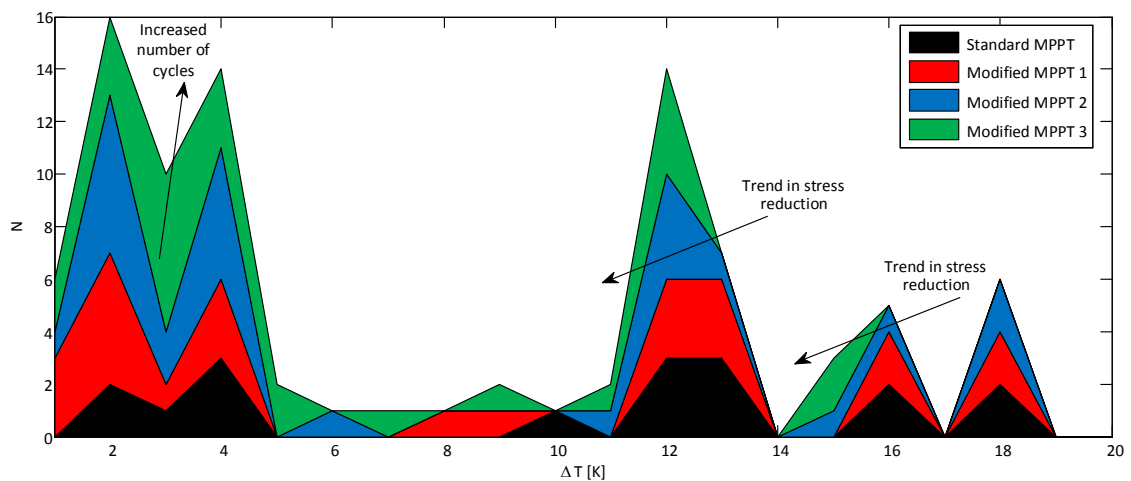


Figure 5.19: Rainflow histogram of the thermal cycles for a 10 min mission profile.

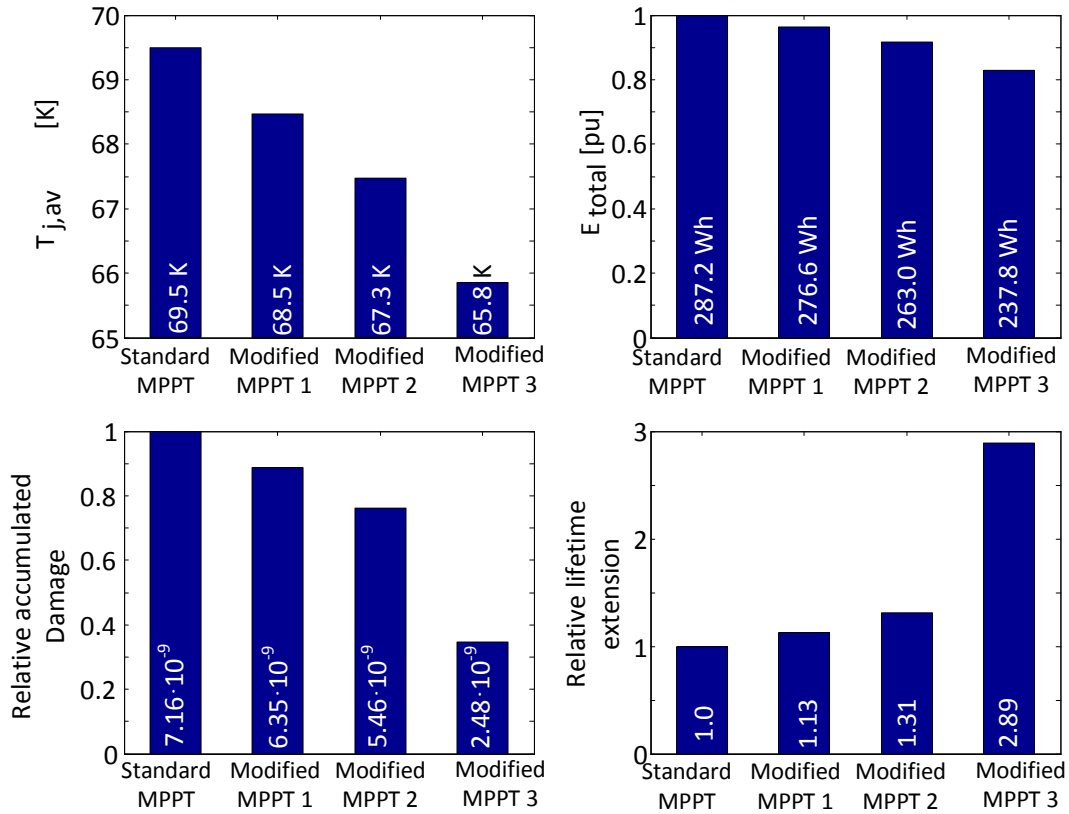


Figure 5.20: Analysis of the mission profile tests with different positive temperature gradients.

to lower cycles is achieved. These results are basis for the derivation of the lifetime consumption of the different profiles, which are collected in Fig. 5.20, together with the derived average temperature of the different profiles and the energy harvested from the PV array. The harvested energy is derived with the measurement data of the dSpace system, which implies a certain inaccuracy of the relatively slow sampling rate compared to the dynamic of the currents. Similar, the thermal steady state before the experiment is started might not be equal, leading to an imprecision of the average temperature. However, a limitation with the modified MPPT 1 leads to a reduced average temperature by 1 K and only reduced energy production of 3.7%, whereby the accumulated damage is only 89% of the case without temperature gradient limitation. Thus under the tested mission profile, the lifetime of the system would increase by 13% compared to the system without temperature gradient limitation. For the more stringent limitations, this trend is amplified, showing the tradeoff between maximum energy harvesting and increased lifetime. In the case of the highest temperature gradient limitation of the modified MPPT 3, the average temperature is decreased by 4.7 K and the energy production is reduced to 82.8% of its possible value, whereas the lifetime is increased to 289%. Despite the reduction of the harvested energy, it must be considered that the majority of the energy harvested by a PV system comes from sunny days, whereas the temperature gradient limitation affects the operation only during fast-changing irradiance conditions. In fact, while the total accumulated damage is greatly reduced, the loss in harvested power may not be so relevant, if the total useful life of the system is considered.

## 5.4 Short summary of the section

This section has reviewed active thermal control algorithms for power electronic modules and categorized them in control of the power converter's losses and the control of the power converter's loading. A junction temperature estimator based on a low bandwidth case temperature measurement is designed and validated for different order of the estimator. A dynamic limitation of the maximum junction temperature is demonstrated with the estimator and the second order estimator has been shown to fit well for the tested power module, whereby low computational burden is caused. As an example for controlling the converter's loading in a less complex system than the ST, a thermal stress reduced MPPT algorithm has been proposed. The perturb and observe algorithm has been further improved with a limitation of the junction temperature gradient of the power semiconductors to reduce the thermal stress during fast changing irradiance. For a mission profile subjected to fast changing irradiance the tradeoff between energy harvesting and lifetime consumption is experimentally demonstrated. Reduced thermal stress and thus improved reliability of the power electronic components is achieved at the expense of reduced energy harvesting. Under tested conditions, a reduction of 3.7% of the energy harvested has increased the lifetime for the investigated mission profile by 13%.

## 6 Active thermal control by control of the power losses

The approach to control directly the losses for controlling the junction temperature has been introduced in the literature review. However, it was mostly applied for power converters feeding electric drives because of the varying fundamental frequency, which can impose severe thermal cycles. In this section, one algorithm is introduced, which is applicable to hard switching inverters and one algorithm, which is applicable to soft switching converters. Both algorithms enable to reduce the junction temperature fluctuations by controlling the losses of the power converter without the need for an additional junction temperature measurement. For the hard switching power converter's active thermal algorithm, the junction temperature is measured and the impact on the efficiency is demonstrated. Furthermore, an estimation is given how much impact the algorithm can have on the lifetime or the de-rating of the components. The active thermal control algorithm for soft switching power converters is introduced and validated experimentally.

### 6.1 Control of hard switching power converter's losses

#### 6.1.1 Motivation for the proposed algorithm

As it has been shown in section 4.2.5, the high load operation of the ST was more stressful than the daily power and weather variations. In the investigated profile, there are thermal cycles with short time periods and relatively high magnitude, which have been shown in the according Rainflow diagrams. For reducing the damage caused by these thermal cycles, a fast response of the thermal control is required, which can be achieved by controlling the losses of the power converter. The reduction of the thermal cycle's magnitude of the power semiconductors in the ST is reducing the stress and thereby decreases the damage for the devices.

The approach to control the junction temperature by controlling the switching frequency of the converter has been addressed in the literature review of active thermal control. This algorithm was mostly used to reduce the overall losses of the power converter, which may not be possible in grid-connected applications, because the overall losses of the converter are minimized by still complying with the grid codes. This is usually done in the system design, which does not leave an additional margin to reduce the losses of the converter during operation without changing the operation setpoint. Consequently, a reduction of the switching frequency is assumed to be impossible without violating the grid codes.

As an alternative to a switching frequency reduction, it is possible to increase the switching frequency and thereby increase the losses of the power converter during operation. This enables to reduce thermal cycling during fast changing loads and thus reduces the stress for the power converter, while the average junction temperature is increasing. A challenge for the application of this algorithm is to detect, if a reduction in power is leading to a short thermal cycle, which needs to be compensated, or if a reduction in power will be kept for a

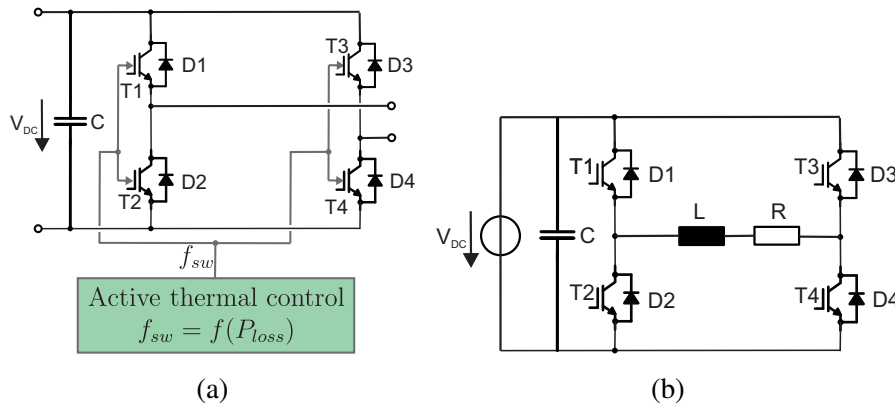


Figure 6.1: (a) Scheme of the H-bridge and the control algorithm, (b) H-bridge converter connected to a passive load.

long time. Thus, a prediction would be required, but unfortunately, the mission profile of the ST is not known a priori. Without a prediction of the future output power of the converter, there is a risk to only increase the losses by affecting higher costs for the reduced efficiency without a reduction of the stress.

Several publications have investigated the lifetime of the system based on the mission profile and the system parameters for an appropriate system design [84, 100, 150, 151, 152, 153]. This procedure is well known and several simulations have been presented, which analyze different applications. In the cited studies critical ambient and operating conditions have been found, which limit the lifetime of the power semiconductors, e.g. grid faults [100]. Based on the different identified stressing conditions, it can be investigated, which active thermal control variable can be used and how significant the impact of this control variable is on the performance of the system. Moreover, the cited studies can be extended to the application of active thermal control and the optimized tuning of the thermal controller.

This section proposes to control the switching frequency of a hard switching power converter for reducing short thermal cycles. An algorithm is introduced, which does not require a junction temperature measurement, but only the electrical measurements. Furthermore, it is targeted to investigate the tradeoff between the costs for a reduction of the thermal cycles in magnitude by means of higher losses and the benefit gained in terms of reduced damage for the power converter. A study on a laboratory setup validates the effectiveness of this approach.

### 6.1.2 System description and controller design

In hard switching power converters, a variation of the switching frequency enables to vary the losses and thus the junction temperature as shown in (3.7) and (3.9). This potential is dependent on the chosen power semiconductor and the design of the converter, but mainly the ratio between conduction and switching losses. The idea proposed in this loss control is to exploit the switching losses for a reduction of the thermal cycling. As a building block for several ST topologies, the H-bridge shown in Fig. 6.1 (a) is considered in this study. In

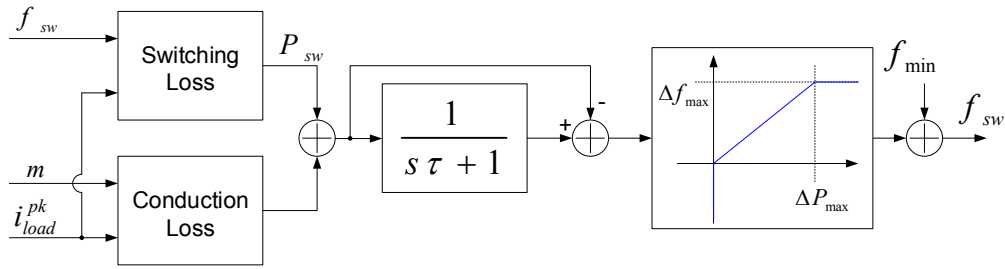


Figure 6.2: Controller diagram of the proposed thermal controller.

the same figure, also the switching frequency is highlighted to be the variable, which is set in dependence of the converter losses. The proposed algorithm could be applied for a CHB converter or even for a LV side converter consisting of a standard two level VSC. In Fig. 6.1 (b) the configuration of the H-bridge converter with an inductive-resistive load is shown to be fed by a DC source. This configuration is used in the following.

For addressing the identified problem, that the mission profile is not known and the junction temperature is hard to obtain, an algorithm is developed, which does not require a junction temperature measurement. Only variations of the power semiconductor losses are detected to perform active thermal control actions, which can be done based on the electrical parameters, which are already sensed for the control of the system. This has the advantage to be easily implementable in a controller of a power converter without additional hardware costs or the challenge for a wide bandwidth junction temperature measurement. The proposed controller is shown in Fig. 6.2, where the losses are derived based on the electrical parameter and filtered by a low pass filter to detect power variations. Appropriate tuning of this controller is essential to compensate the most severe thermal cycles in the profile without deteriorating the efficiency of the converter system. A lookup table links the power difference to the frequency increase, so that a higher switching frequency is selected when the output power is reducing (with the gain  $\Delta f_{max}/\Delta P_{max}$ ). Instead, when the output power is increasing, the switching frequency is locked to the minimum. This non-linear control aims at preventing the cooling of the power module when the output power is reduced, but does not work when the module is heating up. This behavior actually limits the increase of the switching frequency, consequently reduces additional losses introduced by the active thermal controller. The tuning parameters of the control are represented by the gain  $\Delta f_{max}/\Delta P_{max}$ , that should be tuned to have the maximum allowed frequency in the case of the maximum power difference, and the time constant  $\tau$ , that selects the speed of the control.

For the tuning of the time constant  $\tau$  no standard tuning procedure can be adopted, because the effectiveness of the thermal controller is highly dependent on the mission profile. Thus the thermal cycles, which are targeted to be compensated, need to be identified first. For demonstration, a 10min mission profile with highly fluctuation power is generated and shown in Fig. 6.3 along with the constant switching frequency of  $f_{sw} = 10kHz$  and measurement of the junction temperature. The junction temperature is measured for two IGBTs and two diodes in the H-bridge converter with an optic fiber measurement system from Opsens. Additionally, the case temperature is measured with the already integrated sensor in the mod-

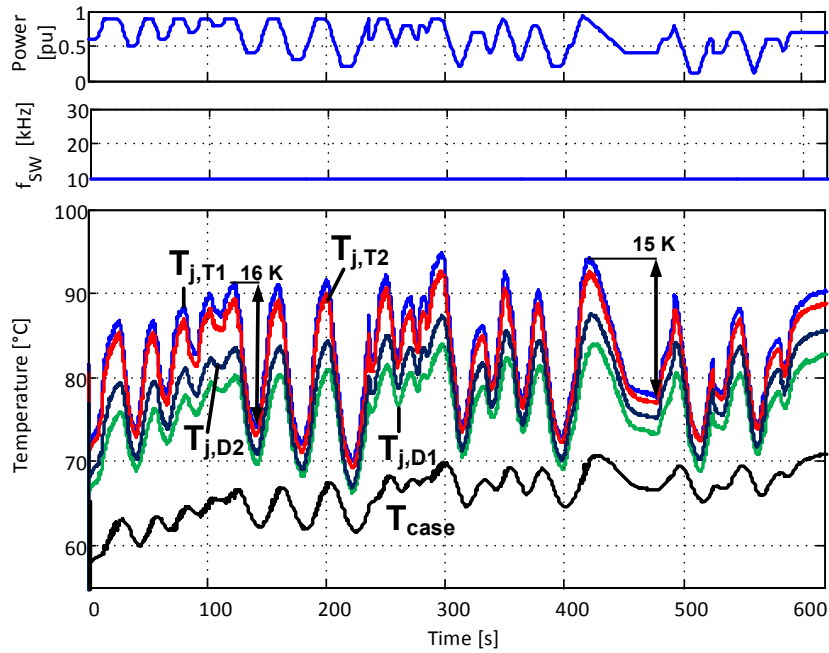


Figure 6.3: Junction temperature measurement for  $V_{dc} = 350V$  and a variation of the modulation index without active thermal control.

ule (Danfoss DP25H1200T101667-101667). As it can be seen, every power variation in the mission profile is reflected in the junction temperatures of the power semiconductors, leading to thermal cycles up to  $\Delta T = 16K$  in relatively short periods. Even in the case temperature, many of the power variations can be seen, whereby their magnitude is much smaller.

The thermal cycles in the profile obtain periods between several seconds and one minute. For the compensation of thermal swings with a length of several minutes, the affected losses would be relatively high, which does not seem to be acceptable. Instead, it appears to be more promising only to target the compensation of the fast thermal cycles, which is implemented and tested in the following.

As an initial test for the tuning, the time constant of the thermal controller is set to  $\tau = 1s$  and the same mission profile is run as shown in Fig. 6.4 under the same conditions. It can be seen, that the switching frequency is increasing for decreasing power in the profile, which is behaving as targeted by the controller. In the junction temperature measurement, it can be seen, that the fast thermal swings with periods of few seconds are well compensated and even thermal swings with longer periods are reduced in their magnitude. For example the thermal swing at  $t = 480s$  is reduced from  $\Delta T = 15K$  to  $\Delta T = 8K$  by the proposed thermal controller.

Based on this initial tuning, a compensation of thermal cycles with shorter periods and with longer time periods are tested. The time constant is set to  $\tau = 0.1s$  and  $\tau = 10s$  to enable a cost benefit comparison. For a comparison of the effect, Rainflow counting is applied as shown in Fig. 6.5. In this diagram,  $N$  represents the number of thermal cycles with the magnitude  $\Delta T$  and the mean junction temperature  $T_{j,av}$ . As it can be seen in the figure, an increased  $\tau$  leads to a stronger shift of the thermal cycles to lower magnitudes. At the same

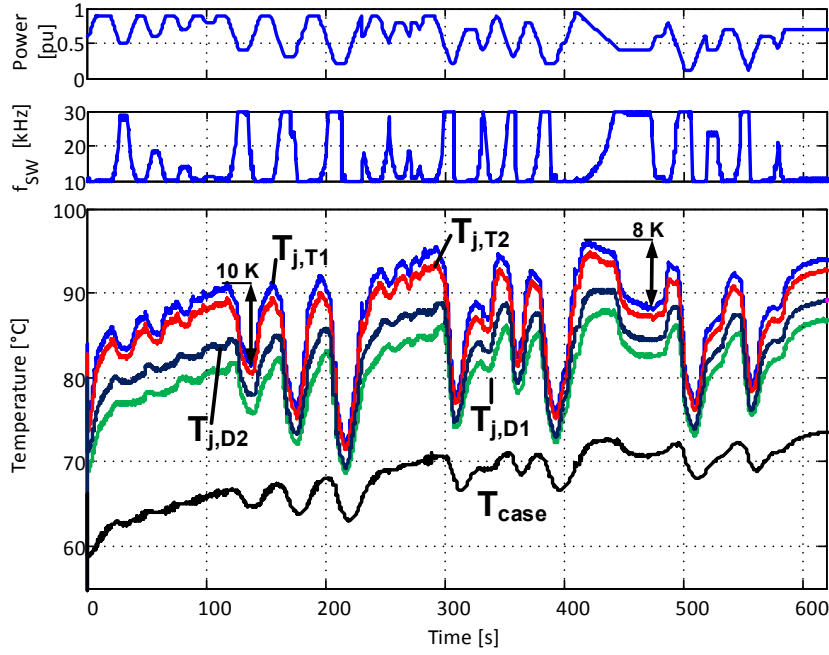


Figure 6.4: Junction temperature measurement for  $V_{dc} = 350V$  and a variation of the modulation index with active thermal control.

Table 6.1: Comparison of the thermal stress in IGBT 1 without active thermal control and with active thermal control for different controller tuning.

	Without thermal control	With thermal control $\tau = 0.1 s$	With thermal control $\tau = 1 s$	With thermal control $\tau = 10 s$
$T_{j,av} [^{\circ}C]$	82.5	89.2	87.8	87.9
$\Sigma\Delta T [K]$	265.3	179	177	182
$f_{sw,av} [kHz]$	10	14.6	15.0	14.9

time, the average temperature is increasing as expected. Particularly the thermal cycles with the large magnitude are severe for the power semiconductor, which makes their reduction beneficial.

The results are compared in Table 6.1, where the average junction temperature  $T_{j,av}$ , the sum of all detected thermal cycles  $\Sigma\Delta T$  with a magnitude  $\Delta T > 1 K$  and the average switching frequency  $f_{sw,av}$  are compared. As expected, the activation of the thermal controller increases the average junction temperature, reduces the thermal swing and increases the average switching frequency. For the three different controller tunings, the tuning for  $\tau = 1 s$  obtains the highest average switching frequency, whereby the average junction temperature and the sum of the thermal swings is lower than for the other tunings. Since the average junction temperature correlates with the losses, it is concluded, that the increase of the switching frequency is done for lower power. Thus  $\tau = 1 s$  is the best tuning out of these three time constants for the given junction temperature profile.

In the following subsection, the tradeoff between thermal swing reduction and the associated higher costs for higher losses will be analyzed deeper with an estimation how much the stress is reduced or how much de-rating of the power semiconductors is possible for the



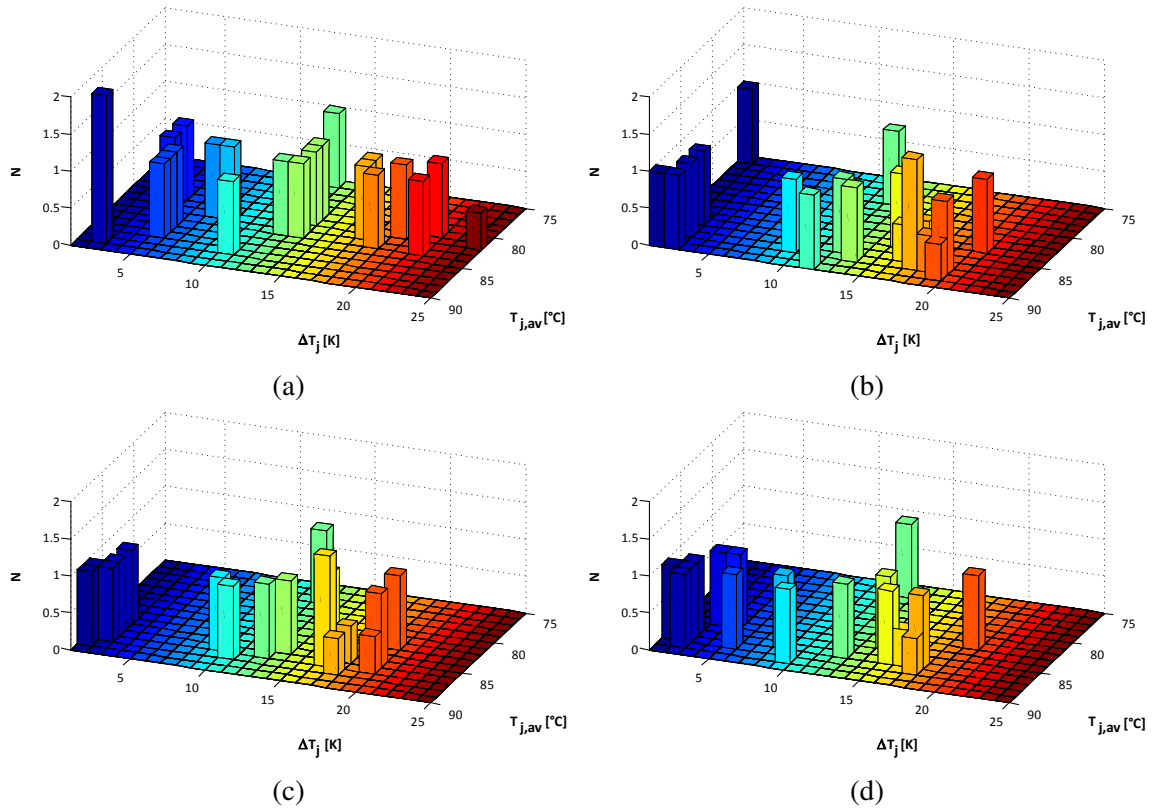


Figure 6.5: Measurement results after Rainflow counting for IGBT T1: (a) without active thermal control, (b) with active thermal control  $\tau = 0.1 s$ , (c) with active thermal control  $\tau = 1 s$  and (b) with active thermal control  $\tau = 10 s$ .

investigated mission profile with similar lifetime expectation.

### 6.1.3 Cost and benefit analysis for active thermal control

In the last subsection, it has been shown that a lifetime extension of a power module with active thermal control by means of switching frequency control can be achieved with associated higher costs in terms of additional losses. Remarkably, the potential and the cost-benefit tradeoff of active thermal control varies with the mission profile and the thermal characteristics of the power converter system. The determination of the related optimum is a difficult topic, especially if no known periodic power cycle is applied. To overcome the complex interaction between mission profile and thermal behavior, it is suggested to start the analysis with a given junction temperature profile as shown in Fig. 6.6. This profile corresponds to the junction temperature measurement during the same mission profile as shown in Fig. 6.3, but with a high-speed infrared camera instead of the Opsens system. An indication of the lifetime estimation for power semiconductors is expressed with (3.2), where the number of cycles to failure for a specific IGBT generation is affected by various influencing factors, such as the thermal cycles magnitude  $\Delta T$ , the average junction temperature  $T_{j,av}$ , the power on-time  $t_{on}$  and the current per bond wire  $I$  [80]. With respect to the cited work, the diameter of the bond wires and the voltage rating of the power semiconductors have been omitted,

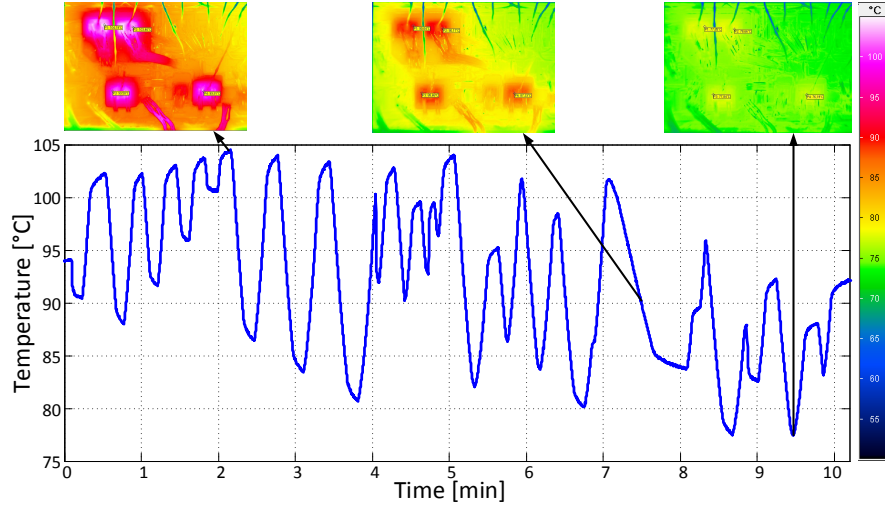


Figure 6.6: Junction temperature profile and infrared camera images for different conditions in a full bridge converter.

because the voltage rating is usually given by the application requirement and the diameter of the bond wire is designed by the manufacturer. As a design parameter of the power converter, the current rating can be used, because it correlates with the number of cycles to failure, consequent the lifetime.

Following the correlation of the lifetime to the current rating, an alternative goal to the lifetime extension with active thermal control can be defined. This goal is the de-rating of the current rating per bond wire  $I'$  with application of active thermal control under the constraint of equal lifetime expectation. To quantify the potential de-rating, the lifetime estimation is done for the junction temperature profile without active thermal control ( $N_{f1}$ ) and the junction temperature profile with active thermal control ( $N'_{f1}$ ). This is done by deriving the number of cycles to failure as shown in (3.2). The ratio between this number of cycles to failure can be used to derive the reduced required current rating for a similar number of bond wires as expressed with (6.1). The connection of current rating per bond wire and the lifetime enhancement/reduction based on the empiric lifetime model is visualized in Fig. 6.7 with the additional indication of a higher or lower number of bond wires [80].

$$\frac{N'_{f1}}{N_{f1}} = \left(\frac{I'}{I}\right)^{-0.717} \quad (6.1)$$

Apart from the lifetime enhancement of active thermal control, the reduced efficiency has to be considered. An accurate derivation requires taking the dynamic behavior of the thermal impedance into account. In (6.2) the derivation is shown for the junction temperature  $T_j(t)$  in dependence of the starting temperature  $T_{j,0}$  added to the convolution integral of the losses  $P(t)$  and the derivative of the thermal impedance  $Z_{th}(t)$  [154].

$$T_j(t) = T_{j,0}(t) + \int_0^t P_{loss}(\tau) \dot{Z}_{th}(t - \tau) d\tau \quad (6.2)$$

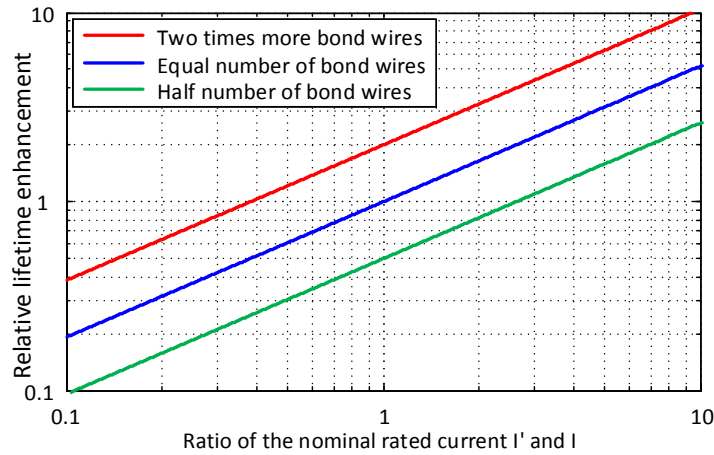


Figure 6.7: Power module lifetime dependence on current rating and number of bond wires.

The active thermal controller is affecting an increase in the junction temperature by increasing the losses. Since deriving the losses with this equation based on the temperature profile is too complex to analyze, this work proposes only to give a qualitative estimation based on the distribution of thermal cycles. An effective way to analyze the potential of an application based on a thermal profile is to identify the thermal cycles, which are most responsible for the degradation. This is done by applying thermal cycle counting, which leads to a histogram with the thermal swing  $\Delta T_j$ , the period of the cycle  $T$ , the mean temperature of the thermal swing  $T_{j,av}$  and the number of cycles in a defined interval of these variables. Even if there are several ways to count thermal cycles, in reliability literature Rainflow counting [155] has been preferred and it is applied in this case study. The  $10min$  temperature profile of a power semiconductor during operation in Fig. 6.6 is used to present the proposed method. The Rainflow histograms for the aforementioned temperature profile are derived and shown in Fig. 6.8 (a). Here, thermal cycles with a magnitude lower than  $\Delta T_j < 1 K$  are neglected. The x-axis displays the cycles period  $T$ , the y-axis the thermal swing  $\Delta T_j$  and the z-axis the number of thermal cycles  $N$ . The most severe cycles have high thermal swings, which make their reduction most important [12]. However, beside the magnitude, the period is important, because a long period affects high additional losses for the compensation of the cycle and thus a high drop in efficiency. As a result, high potential for a cost effective thermal controller design is existing for profiles with high thermal swings, which occur in short periods. In the second step Rainflow counting is repeated based on  $T_{j,av}$  instead of the period. This identifies the temperature distribution of the cycles in the profile. In Fig. 6.8 (b), this Rainflow histogram is shown. It can be used to estimate the lifetime of the power semiconductors with the lifetime model of (3.1), which does not respect the ratings (e.g. current rating or bond wire diameter) of the power semiconductors. Since this equation is only valid for a specific  $\Delta T$ , the Palmgren Miner rule is commonly applied as described in (3.3). This is applicable with the power cycling data commonly published by the module manufacturers, which makes it a practical solution in combination with the Rainflow histograms.

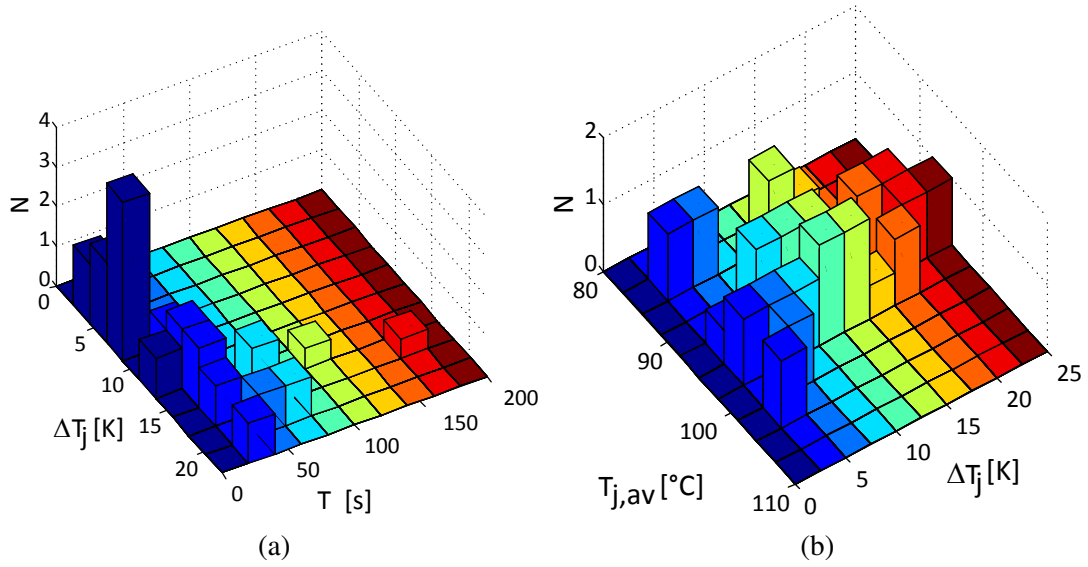


Figure 6.8: Rainflow counting of the thermal cycles: a) in dependence of the cycles period and magnitude, b) in dependence of the cycles mean temperature and magnitude.

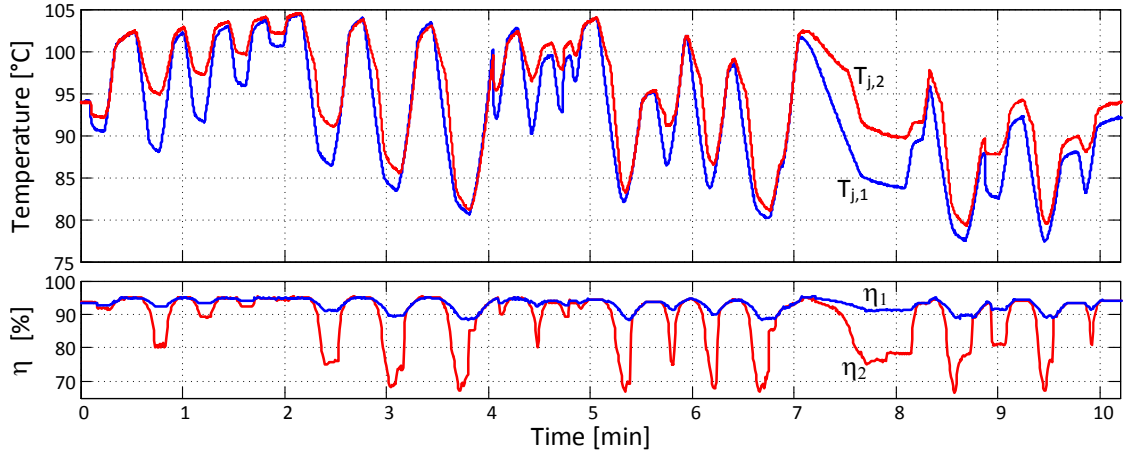


Figure 6.9: Measured temperature and efficiency profiles:  $T_{j,1}$  without thermal control and  $T_{j,2}$  with active thermal control.

### 6.1.4 Potential estimation with the proposed active thermal controller

For demonstration of the concept in a study case, the same mission profile composed of active and reactive power profile, already presented in Fig. 6.4, is considered and run with constant switching frequency  $f_{sw} = 10 \text{ kHz}$ , constant voltage  $V_{dc} = 300 \text{ V}$  and constant output frequency  $f = 50 \text{ Hz}$  on a full bridge converter, resulting in the temperature profile of Fig. 6.6. To reduce the temperature fluctuations, a thermal controller is designed as shown in Fig. 6.2 to vary the switching frequency between  $10 \text{ kHz} < f_{sw} < 30 \text{ kHz}$ .

The same mission profile of the previous case is now applied to test the thermal controller, which results in the temperature profiles of Fig. 6.9, where also the measured efficiency is shown for both cases.  $T_{j,1}$  is the recorded temperature measurement without thermal control and  $T_{j,2}$  is the temperature measurement with active thermal control. It can be seen that several thermal cycles are significantly reduced in magnitude, while others are affected less.

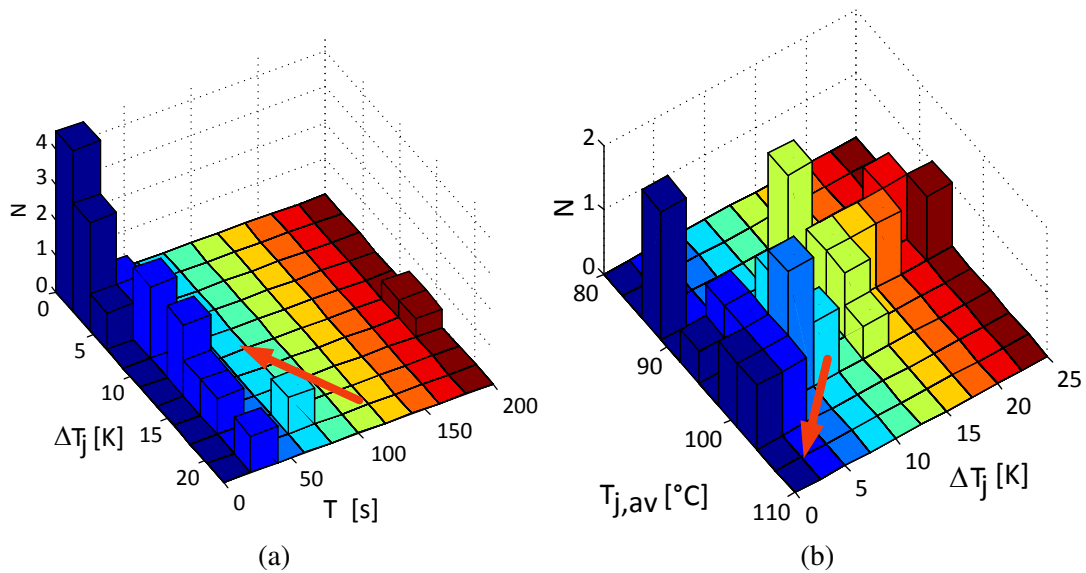


Figure 6.10: Rainflow counting of the thermal cycles after applying active thermal control: a) in dependence of the cycle's period and magnitude, b) in dependence of the cycles mean temperature and magnitude.

Table 6.2: Comparison of the profile with thermal control and without thermal control.

	<b>With thermal control</b>
Efficiency	-1.1 %
Lifetime enhancement	39 %
Current rating for similar lifetime	-22 %

The efficiency without thermal control is between 88.5 % and 95 %. For the active thermal control instead, it is varying between 67 % at decreasing low power and 95 % for full power. For a deeper analysis of the thermal cycles and thus the reliability, the Rainflow histograms are shown in Fig. 6.10. In Fig. 6.10 (a) the thermal cycles are reduced in magnitude compared to the histogram without thermal control, whereas the periods of the cycles show only few changes. In Fig. 6.10 (b), it can be seen that also the average temperature of the cycles has increased. In total, fewer cycles are counted than in the previous temperature profile. For the comparison between the cases with thermal control and without thermal control, the lifetime consumption of the profiles is derived.

The data of this experiment is furthermore used to apply the proposed method for the de-rating of the current carrying capability of section 6.1.3 and the results are shown in table 6.2. The overall efficiency of the profile is reduced by 1.1 % for the activation of the thermal controller. This can either be used to achieve a lifetime enhancement of 39 % or to apply it for de-rating as shown in Fig. 6.7. The de-rating leads to power semiconductors with 22 % lower current rating compared to no thermal control under equal expected lifetime.

## 6.2 Control of soft switching power converter's losses

Several active thermal control algorithms have been proposed for hard switching power converters and many of these algorithms are based on a regulation of the switching frequency. However, this is not applicable for the soft switching isolated DC/DC converters without also affecting the magnetizing losses of the medium frequency transformer. This subsection proposes an algorithm, which regulates the duty cycle of the DC/DC converter to control the semiconductor losses, aiming at influencing the consequent thermal stress. The proposed algorithm is analytically analyzed and the effectiveness is demonstrated on a laboratory prototype with junction temperature measurement. In continuation of the algorithm for hard switching DC/DC converters, the algorithm is implemented without measurement of the junction temperature and only detects the variations of the output current to control the losses.

### 6.2.1 Motivation for the proposed algorithm

For a reduction of the thermal stress, several existing algorithms apply a variation of the switching frequency. This idea has been proposed to control the switching frequency for regulating the thermal fluctuations of hard switching power converters in the last subsection. Further active thermal controllers have been proposed based on circulating the reactive power [101] or rerouting the power in redundant paths [49]. However, none of these thermal controllers is applicable to the emerging high power DC/DC converters. The commonly used DAB or even multi pole DC/DC converters, such as the QAB operate under soft switching conditions and interact with a medium frequency transformer. A reduction of the switching frequency increases the flux in the transformer, possibly leading to a saturation of the flux. An increase of the switching frequency instead reduces the power and thus the losses of the power semiconductors, while the magnetizing losses of the transformer are increased. Consequently, considering a switching frequency variation in the system design requires overdesigning the transformer. This increases the system size and costs, which is not acceptable and calls for a specifically tailored algorithm for the application of isolated DC/DC converters.

This subsection proposes to control the duty cycle of the isolated high DC/DC converter, which is operating with phase shift modulation for regulating the junction temperature of the power semiconductors during operation. When the DC current decreases, the duty cycle is reduced, which increases the peak current. In the opposite way, for increasing power and during constant operation conditions, the converter is operated with minimal losses. Therefore, the approach does not require knowledge of the profile, but compensates thermal cycles shorter than the time periods it is tuned for. The strategy to reduce thermal cycling in operation is demonstrated in simulations and validated on a DAB converter prototype with an open IGBT module and junction temperature measurement to reduce the thermal swing during operation.

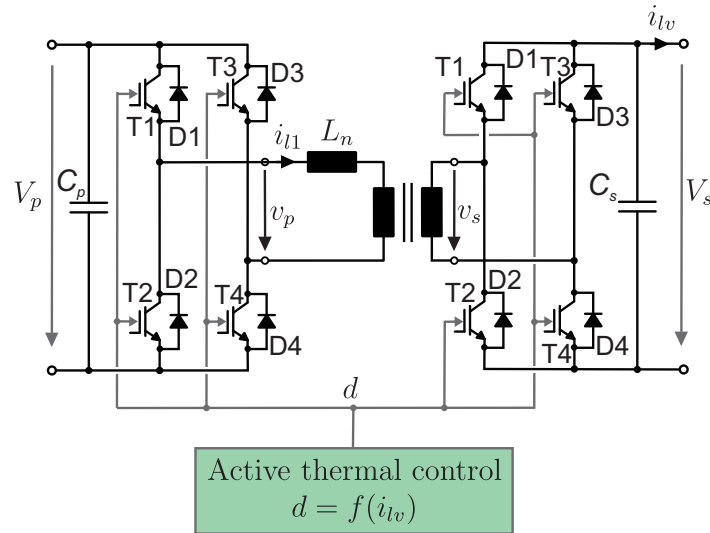


Figure 6.11: Dual Active Bridge (DAB) with the proposed active thermal controller .

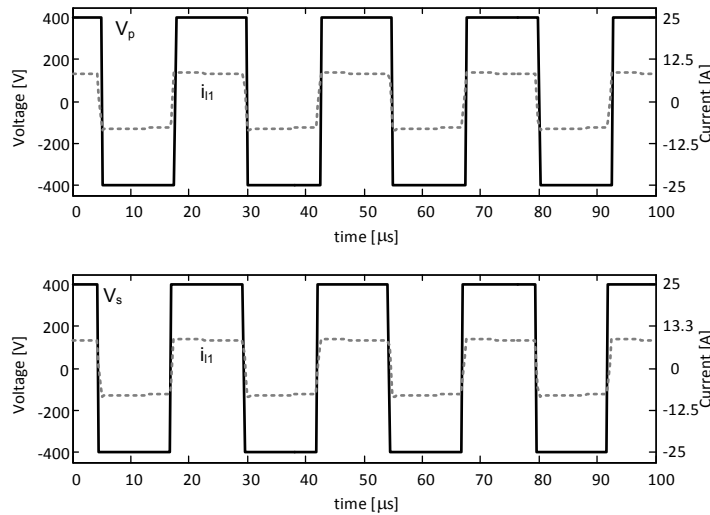


Figure 6.12: Operation of the DAB with phase shift modulation.

## 6.2.2 System description and controller design

The DAB has been proposed as an isolated DC/DC converter with high input-/output ratio and bidirectional power flow capability. The equivalent circuit of the DAB, consisting of the medium frequency transformer and two full bridge converters, is shown in Fig. 6.11. In addition to the topology, the active thermal control scheme is shown, which changes the duty cycle in dependence of the DC current.

The current and voltage waveforms of the DAB converters with the commonly applied phase shift modulation are shown in Fig. 6.12. Primary and secondary full bridge switch with a constant duty cycle of 0.5, whereby the phase shift determines the direction and the quantity of the transferred power. The power transfer from primary side to secondary side can be described with (6.3) in dependence of the primary side voltage  $V_P$ , the secondary side voltage  $V_S$ , the switching frequency  $f_{sw}$ , the leakage inductance of the transformer  $L_n$ , the transformer ratio  $n$  and the phase shift  $\phi$  between primary and secondary side.



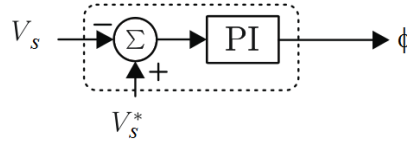
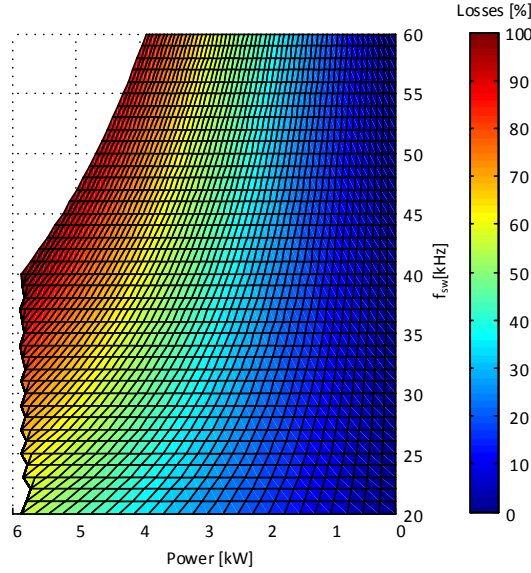


Figure 6.13: Phase shift control of the DAB converter.

Figure 6.14: Demonstration of the power semiconductor losses of the DAB for bidirectional power flow with the parameters of table 6.3 for the control of the switching frequency  $f_{sw} = [20,60] kHz$ .

$$P = \frac{V_P V_S}{2\pi f_{sw} L_n} \phi \left(1 - \frac{\phi}{\pi}\right) \quad (6.3)$$

In the extension to multiple active bridges, every phase shift between the full bridges affects a current, which increases the reactive power in the system. This affects additional losses and thus deteriorates the efficiency. However, if the converter is used for voltage adaptation with different DC-link voltages on the MV side, the different bridges are expected to transfer the same power and thus operate with similar phase shift. The voltage control of the DAB is done with a PI controller, which is setting the phase shift for the applied phase shift modulation as shown in Fig. 6.13. In case of multiple bridges, the balancing of the secondary cells needs to be performed, which can be done by control of the phase shift between the different secondary bridges.

With respect to the described lifetime models in (3.1)-(3.3), a reduction of the thermal swing can increase the lifetime of power semiconductors. If no snubbers are used, the DAB converter's transistors operate in zero voltage switching turn-on and hard turn-off. This causes switching losses, which are dependent on the switched current, the voltage, the switching frequency and the power semiconductor characteristics. However, the control of the switching frequency is not a solution for the application in isolated DC/DC converters, which is demonstrated in Fig. 6.14. The losses for the control of the switching frequency are shown



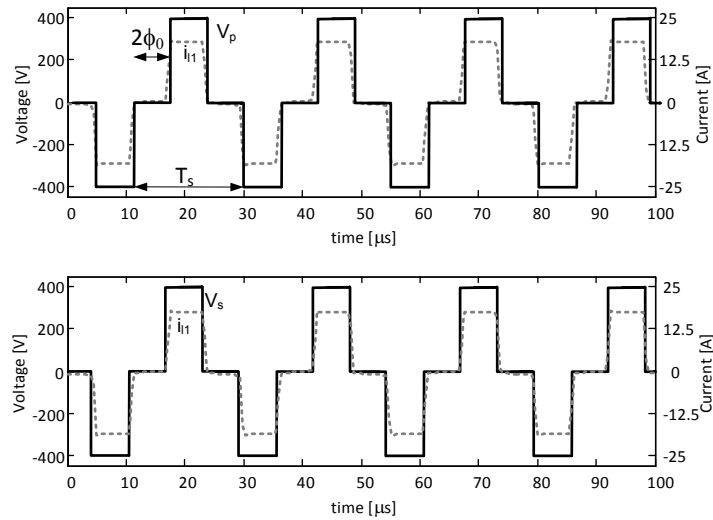


Figure 6.15: Voltage and current waveforms for the proposed duty cycle control.

in dependence of the power, whereby similar colors indicate similar losses. It can clearly be seen that the losses are highly correlated to the power and an increase of the switching frequency reduces the transferred power and changes the losses. As a limitation, the decrease of the switching frequency is limited by the current rating of the power semiconductors and the rated transformer flux. Consequently, for a reduced switching frequency, the maximum phase shift between primary and secondary side cannot be reached without exceeding the stress of the components under the rated power. Thus, the system needed to be highly over-rated to apply this algorithm.

As a more suitable control variable for the manipulation of the losses, it is proposed to control the duty cycle of the converter. The duty cycle is a degree of freedom in the operation of a DAB, which is normally kept constant for phase shift modulation. It has been chosen because of the possible fast reaction time and the discussed disadvantages of the switching frequency control for isolated DC/DC converters. The current and voltage waveforms for the modification of the duty cycles are demonstrated in Fig. 6.15 and described in the following. The reduction of the duty cycle requires a higher current for transferring the same power and causes higher switching losses for the power semiconductors. In Fig. 6.16 the dependence of the power semiconductor losses is shown for different power and duty cycles with the parameters of table 6.3, showing how the losses can be controlled in all operation points. The losses can be controlled for a wide range, making this a promising solution. The only limitation is the maximum current, which can flow in the transformer windings and the consequent transformer flux. For a limitation of the reactive power, the maximum phase shift is set to  $\phi \leq 0.3\pi$ . In efficiency optimized systems, the phase shift is usually limited to  $\phi_{max} \leq 0.18 \cdot 2\pi$ .

With the proposed duty cycle control, the peak current in the transformer can be increased, which affects higher switching losses. The active power remains constant, whereas the reactive power is increasing and hence the power factor is reduced. Remarkably, the power exchange with the MV side converter and the LV side converter is not affected by the algorithm. In operation with phase shift modulation, the current magnitude and the consequent varia-

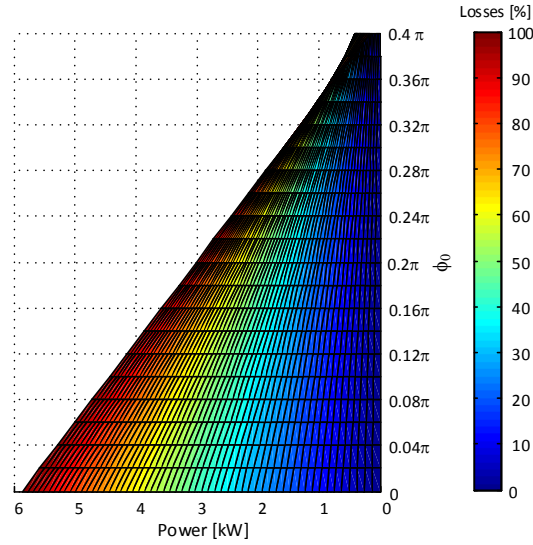


Figure 6.16: Demonstration of the power semiconductor losses of the DAB for bidirectional power flow with the parameters of table 6.3 for the proposed thermal controller with  $\phi_0 = [0; 0.2 \cdot \pi]$ .

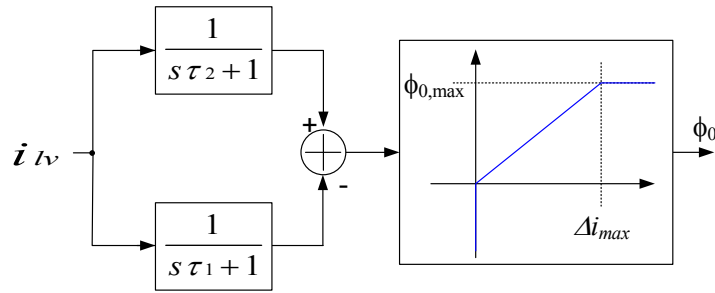


Figure 6.17: Control diagram of the QAB converter.

tions of the phase shift are the only quantities, which are varying. Thus, they are the only influencing factor on the power semiconductor losses. A reduction of a potential junction temperature swing, occurring during power variations, requires controlling the peak current. As an example, during decreasing power the peak current can be increased to compensate thermal swings. For simplicity and the target of not requiring direct junction temperature measurement, the magnitude of the current exchanged with the LVDC link  $i_{lv}$  is used as shown in Fig. 6.17. The current is low pass filtered to detect power variations, whereby the controller has to be tuned for two different goals:

- Compensation of thermal cycles imposed from the mission profile
- Reversal to normal operation with minimal losses in long-term steady state operation.

Similar to the tuning for the hard switching power converters, it is not possible to derive a generally optimal controller tuning. The tuning of the controller depends on the mission profile and the desired compensation of thermal cycles. The first low pass filter with the time constant  $\tau_1$  detects the power variations as explained and enables to revert to normal operation after the reduction of power is permanent. This is important because the system should operate with maximum efficiency, when a reduction of thermal stress is dispro-

Table 6.3: Simulation parameters of the QAB

Parameter	Value
Rated Output Power	$P = 6kW$
LVDC link voltage	$V_p = 400V$
MVDC link voltage	$V_s = 400V$
Switching frequency	$f_{sw} = 20kHz$
Leakage inductance	$L_n = 22.5\mu H$
Transformer turn ratio	$n = 1 : 1$
IGBTs	<i>Infineonfs50r12kt4_b11</i>

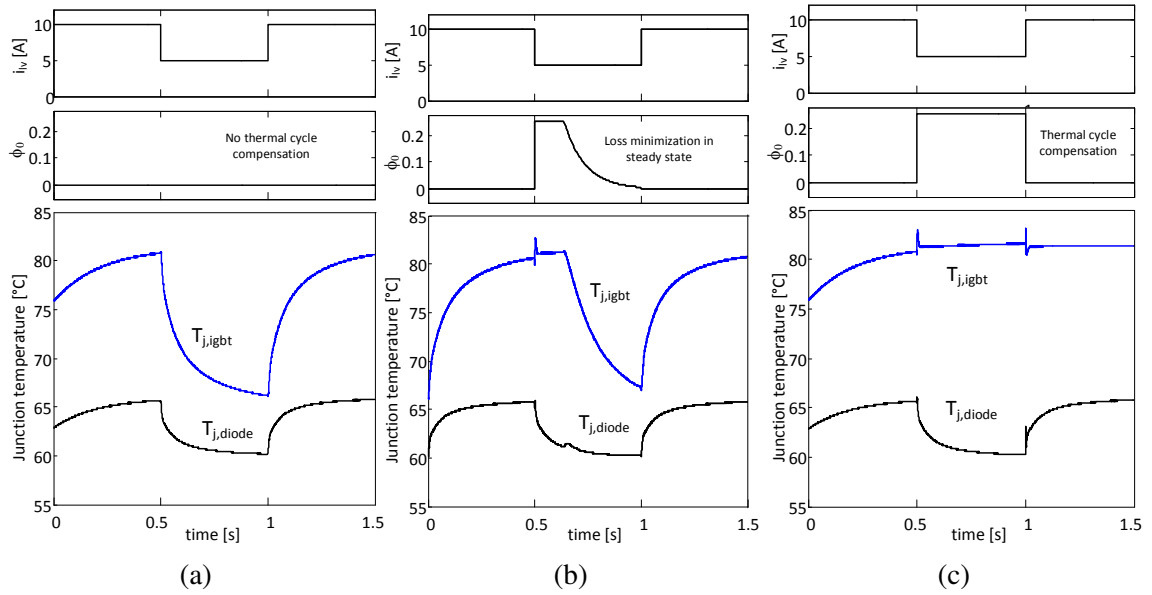


Figure 6.18: Simulation results: Power cycle of one power semiconductor in an QAB: (a) Without thermal control, (b) With thermal control and full cycle compensation, (c) With thermal and demonstration of loss minimization in steady state conditions.

tionate with respect to additional losses for the compensation of a thermal cycle. For an appropriate tuning of  $\tau_1$ , the mission profile should be known and evaluated. The second low pass filter needs to be tuned to delay the controller response to a variation in the current. Otherwise, a fast controller response can cause an increase of the junction temperature and thus counteract the target of a thermal swing reduction. For the tuning of this parameter  $\tau_2$ , it is suggested to tune it with the most relevant time constants of the cooling path. This represents the time constant, which is most relevant for the variation of the junction temperature during the cooling down process.

### 6.2.3 Validation of the thermal control algorithm

To demonstrate the capability of the proposed controller, a system with the parameters of table 6.3 is simulated. The low pass filter is tuned with  $\tau_1 = 0.1s$  and  $\tau_2 = 0.002s$  to com-

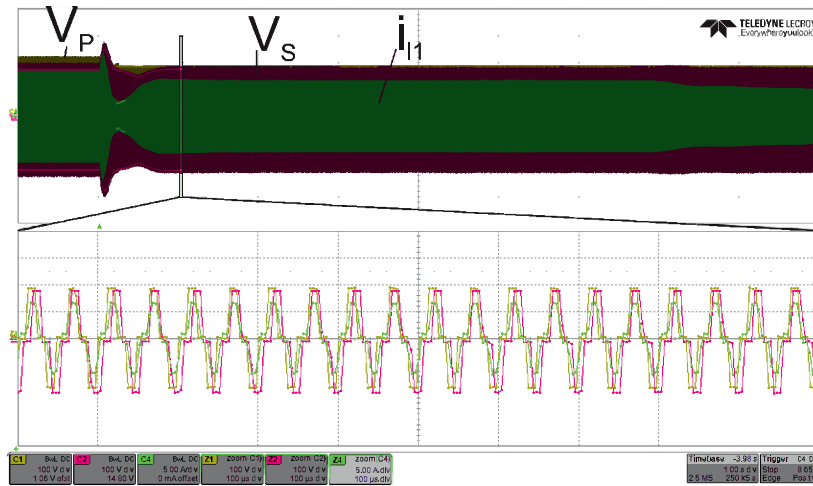


Figure 6.19: Laboratory measurement of a step in the output power.

compensate thermal cycles with periods smaller than  $100\text{ms}$ . Simulations are run for  $1.5\text{s}$  with a power cycle for  $0.5\text{s}$  during which the power is decreased. First, this is run without the thermal controller to demonstrate the resulting thermal swing, and the results are shown in Fig. 6.18 (a). The step in the current causes the cooling down of the IGBT and the diode. In Fig. 6.18 (b) the thermal control is activated, but the period of the thermal cycle is too long to be compensated with the controller tuning. However, the cooling down is delayed and the cooling is slower than in the case without thermal control. Hence, the thermal controller is reducing the efficiency without reducing the thermal stress. This demonstrates the steady state efficiency optimization of the controller.

In the third case, shown in Fig. 6.18 (c), the thermal controller is tuned with  $\tau_1 \rightarrow \infty$  to fully compensate the thermal cycle. As expected, the thermal swing during the power cycle for the IGBT is compensated. However, the junction temperature of the diode is not affected by the thermal control. The diode is cooling down, because the losses are only caused by the conduction losses, which are reduced for the smaller duty cycle. Consequently, the thermal swing of the diode is not reduced. As explained, the losses should only be increased temporarily to compensate thermal cycles below certain periods. Nevertheless, the cross coupling within the module will also prevent the cooling down of the case temperature and thus indirectly reduce the thermal swing for the diodes in the module.

A DAB prototype has been built to validate the proposed algorithm with junction temperature measurement on an open IGBT module. The junction temperature is measured with an optic fiber measurement system, whose sensors have a response time of  $7\text{ms}$ . The parameters of the setup are similar to the parameters of the simulation system in table 6.3. A mission profile with varying power is realized by using an electronic load (Chroma 63800), which is operating with varying resistances to emulate the variation of the load. The controller is tuned with  $\tau_1 = 10\text{s}$  and  $\tau_2 = 0.1\text{s}$ .

The dynamic performance of the controller is demonstrated with a variation of the power, which is shown in Fig. 6.19, where the primary side voltage, the secondary side voltage and the current are recorded. The variation of the power is done by a step in the resistance, which

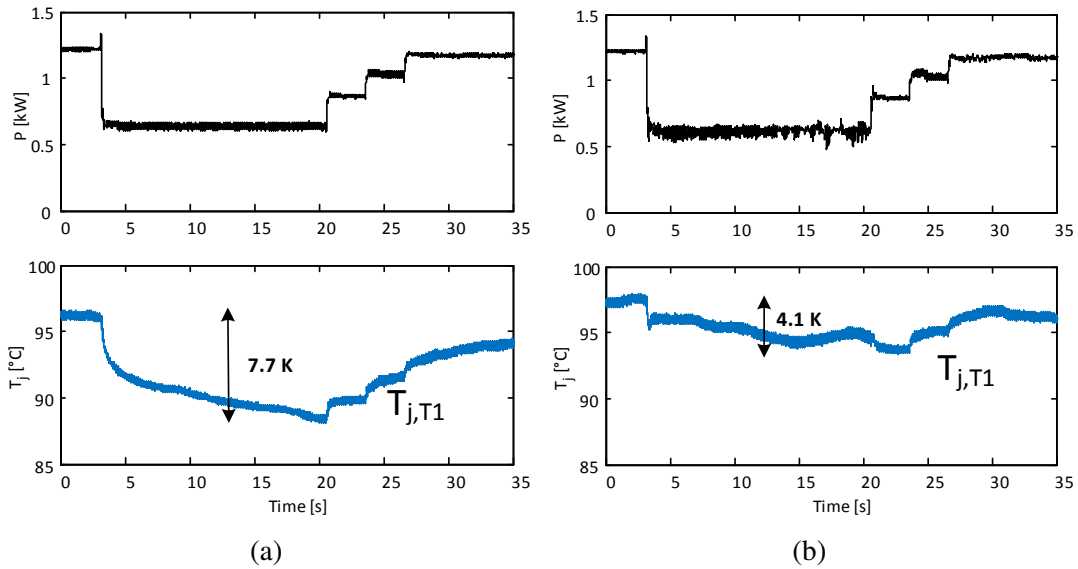


Figure 6.20: Laboratory measurements for a variation in the output power and measurement of the power and the junction temperature of one IGBT: (a) with standard phase shift modulation , (b) with the proposed active thermal control algorithm.

is emulated by the electronic load. Caused by the voltage-balancing controller, the power is increasing first, and reduced quickly. Then, the thermal controller is reducing the duty cycle and the peak current is increasing. Over time, the duty cycle is increased again, because the power is kept constant and the operating point is shifted back to normal operation. This behavior is operating as expected.

For validating the thermal behavior of the algorithm, the optic fiber temperature measurement system is used and a temperature sensor is attached on the surface of one IGBT in the open module. Additionally, the power consumption of the electronic load is measured and the results of a power reduction from  $P = 1.2\text{ kW}$  to  $P = 600\text{ W}$  is shown. In Fig. 6.20 (a) no thermal control is applied and in Fig 6.20 (b) the thermal controller is activated. Without the controller, the thermal swing in the profile has a magnitude of  $\Delta T = 7.7\text{ K}$ , which is reduced by almost 50% to  $\Delta T = 4.1\text{ K}$ . Here, the tuning of the controller can be modified to optimize the tradeoff between a higher reduction for the cost of higher power semiconductor losses or a lower thermal swing reduction for lower increase of the losses. Beside the reduction of the thermal swing, the average temperature  $T_{j,av}$  is increased. However, as shown in (2), this reduction of the thermal swing has a bigger impact on the lifetime than the increase of  $T_{j,av}$ .

### 6.3 Short summary of the section

An active thermal control algorithm for hard switching power semiconductors has been introduced, which enables to reduce the thermal cycling by controlling the switching frequency of the power converter. The algorithm relies only on the electrical measures of the converter and reduces the thermal swing of thermal cycles with short time periods. Different tunings

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have been compared in a study case and the algorithm has been shown to reduce the damage by 28 % at the expense of 9.7 % higher losses. Consequently, for an expected efficiency reduction of 1.1 %, the lifetime of the system is increased by 39 %. Alternatively, to a damage reduction, a method by means of Rainflow counting has been demonstrated to estimate the possible de-rating gained through the application of active thermal control. In the study case, the current rating was found to be reducible to 78 % of its prior value under the same lifetime conditions.

A second active thermal control algorithm has been proposed for reducing the thermal stress of power semiconductors in isolated DC/DC converters. Thermal cycling is reduced by the control of the power semiconductor losses to reduce thermal swing caused by power variations without prior knowledge of the profile. The proposed strategy to control the duty cycle of isolated soft DC/DC converters is introduced and investigated analytically. The results are validated on a laboratory setup with high-speed junction temperature measurement and the capability to reduce the thermal swing with the proposed controller is demonstrated.

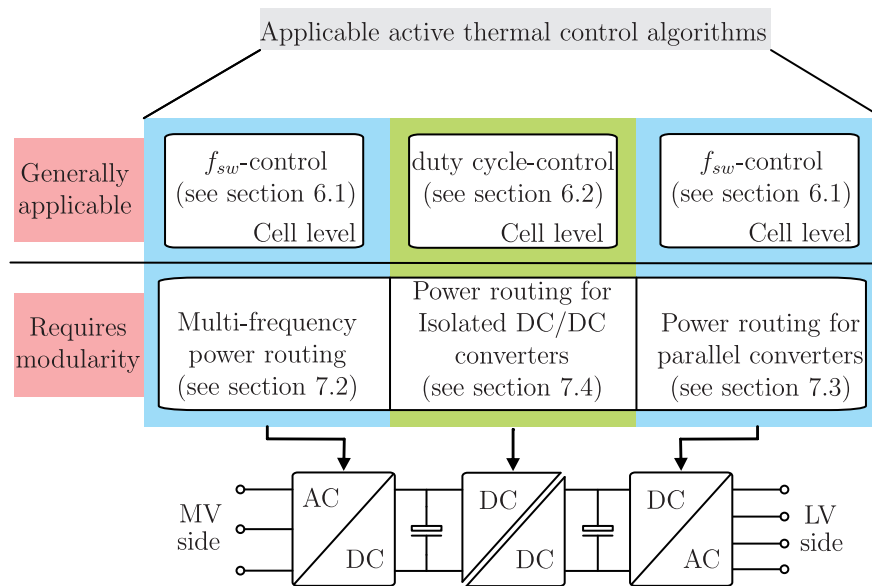


Figure 7.1: Active thermal control algorithms addressed in this work with their applicability to modular and non-modular power converters.

## 7 Active thermal control by control of the system loading (power routing)

This section proposes to apply active thermal control for the architecture of a modular power converter by taking advantage of the modularity. It is proposed to equalize the lifetime consumption of the single cells in a modular power converter to enable prognostic maintenance and thereby reduce the total operating costs. To highlight the applicability of all introduced active thermal control algorithms for the different stages, they are shown in Fig. 7.1. It is distinguished between generally applicable algorithms and algorithms, which require modularity to be applicable. For the hard switching power converters the switching frequency control algorithm introduced in section 6.1 can be applied, while for the isolated DC/DC converter the duty cycle control introduced in section 6.2 can be applied. These algorithms can also be implemented in a modular converter, but their discussed disadvantages by means of increased losses remain. As an innovation of the power routing algorithm, the distinction is not anymore between hard- and soft switching power converters, but between series and parallel connected building blocks. First, this section introduces and explains the concept of power routing, which is then demonstrated in study cases for series connected cells, parallel connected cells and a mixture of both, interfaced with a high frequency transformer.

### 7.1 Power routing for wear-out control

#### 7.1.1 Introduction of the concept

The two active thermal control algorithms, which were introduced in the last section, target to reduce the thermal stress for increasing the lifetime. This delays the time to the next

failure, but cannot totally prevent the failure of a device. Consequently, for ensuring a high quality of service with short down times, these algorithms are not suitable. A concept to improve the reliability is to integrate a redundant cell, which was also implemented in one of the SST-prototypes for traction applications [30]. As a result, the prototype was able to continue operation with one faulty cell.

After the failure, maintenance needs to be scheduled to replace the faulty device before the next component fails. This is particularly problematic for power converters, which are locally distributed, e.g. in rural areas or even offshore. If frequent unscheduled maintenance is required to replace components, the costs will be high. Enabling long periods between the maintenance can be realized with a high number of redundant cells, but this deteriorates the efficiency for series connected cells and increases the costs for the system in general, which is not desired. To prolong the time to the next maintenance, it is proposed to install a condition monitoring system for scheduling prognostic maintenance as described in section 3.2. However, also the condition monitoring based maintenance can be problematic for the optimization of the scheduled maintenance, because components may need to be replaced, which have a significant remaining useful lifetime shorter than the time to the next maintenance. To overcome this problem and to use this as a potential, in the following it is proposed to take advantage of the modularity of the architecture.

Modular power converters are composed of building blocks, which are scalable in voltage and current. Usually, the building blocks consist of devices rated for the same voltage and current, which are loaded equally. However, there are examples in literature, where the optimization of the system requires uneven loading of the devices during operation. As an example, for the maximization of the energy harvesting in PV applications, CHB converters were proposed to have independent MPP trackers in the singular cells [156]. Caused by shadowing or different power connected to the cells, this can lead to uneven loading of the cells. Another example can be found in the optimization of the efficiency for multiphase DC/DC converters, where it was proposed to activate/deactivate power converters [157, 158]. In the cited work, the efficiency during partial load operation was increased with the deactivation of cells. Beside the drawback of influencing the power quality in terms of current and voltage ripple, this activation/deactivation also has an impact on the reliability of the devices.

Based on the most frequently failing parts in power converters and their described failure mechanisms (as examined in section 3.1), several failures of power semiconductors are caused by the thermal swing, which itself is dependent on the loading. It is concluded, that the loading is affecting the stress of the devices, particularly the wear out of the power semiconductors. In case of the deactivation of phases for the DC/DC converters, the components in the deactivated phases do not undergo the stress caused by the active power cycling, while the activated phases need to take over the power, stressing higher their components. Consequently, the stress for the components is unequally distributed and leads to different remaining useful lifetimes. In addition to this unequal remaining lifetime potentially caused by the operation of the system, the lifetime of components is naturally expected to be different. This can be also observed in the accelerated lifetime tests of power semiconductors,



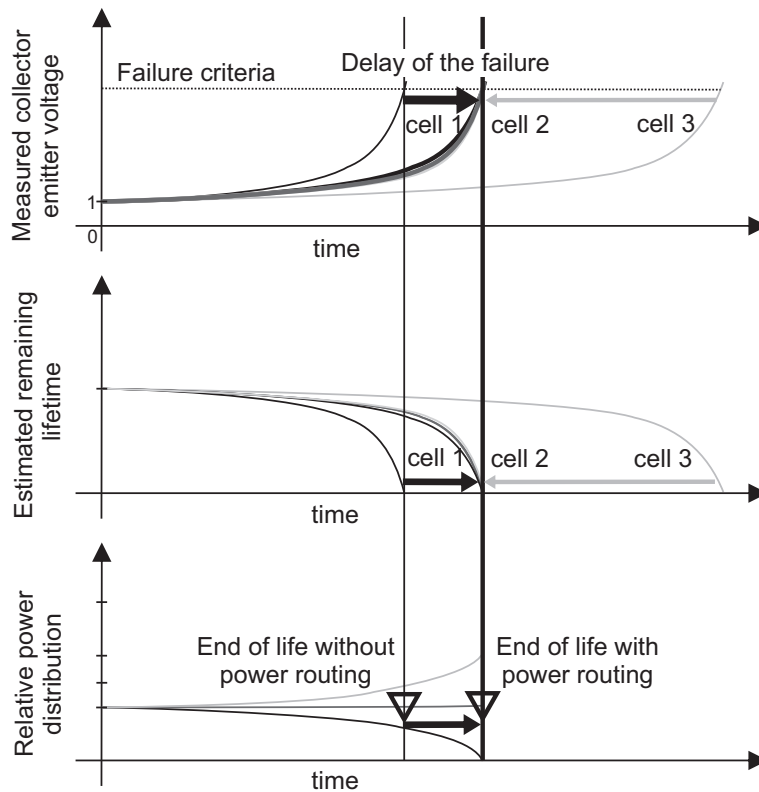


Figure 7.2: Demonstration of the power routing concept for three redundant power paths with different lifetimes with power routing for extending the time to the next failure.

where the end of life criteria is reached after different testing periods [159].

With the high reliability requirements over a long lifetime of a power converter, it is proposed to optimize the system under consideration of the component's condition in the modular building blocks. Based on the redundant power paths of a modular power converter, a repairable system is proposed, where the building blocks are exchangeable cells. At the commissioning of the system, the components have the same aging indication, which is changing during operation. Based on the Weibull failure probability function in (3.5), the failure probability is low at the commissioning and will accumulate after a certain time, leading to regular failures and maintenance to replace faulty components. This results in high costs for the frequent replacement during that phase. To cope with the maintenance and to be able to schedule maintenance in dependence of the condition of the system, it is proposed to route the power in the system in such a manner, that the failures are delayed and the time to the next maintenance is maximized.

Routing the power changes the thermal stress during normal converter operation for specific parts of the system. This can follow the target of stress reduction for a specific part of the power converters, e.g. when the components in one building block are suffering from wear out and have a low remaining lifetime with respect to the components in others. For an optimization, the information obtained from a condition monitoring system is used and applied to control the lifetime of all parts in the system. This is demonstrated in Fig. 7.2 for controlling the lifetime of the power semiconductors. The normalized collector emitter voltage  $V_{ce}$  is used as the parameter for the condition monitoring for the three converters. To define the

EOL, a failure criteria needs to be set, e.g. a 5 % increase of  $V_{ce}$ . In each converter cell, the component, which is expected to fail first, corresponding to the power semiconductor with the highest relative increase of the collector emitter voltage in the cell, needs to be chosen for representing the condition of the cell. At the commissioning, this parameter is similar for all devices in the SCs, but over time, the aging leads to different estimated remaining lifetimes. The aging of the cells is demonstrated for equal power distribution in the system with thin lines and the EOL happens when the first converter is failing. The concept of the power routing is demonstrated with bold lines, while the difference is highlighted with the arrows. The different lifetimes of the cells are used to route the power in such a way, that the converter, which would naturally fail first, is unloaded, while the other converters with longer expected lifetimes are loaded higher. This is highlighted in the relative power distribution shown in the third diagram. Therefore, the failure can be delayed and during the next maintenance, one or more parts can be substituted. In the following, the limits of the power routing capability are investigated.

### 7.1.2 Power routing capability of the different architectures

The application of power routing requires the availability of redundant power paths and is highly dependent on the system architecture. Potential redundant power paths for the different topologies are discussed in this section and it is targeted to quantify their power routing potential and to highlight the influencing variables. In the following, it is distinguished between series and parallel connected building blocks.

Power routing can be implemented by either changing the voltage, the current or both for the different building blocks in a modular power converter. A requirement for the application is the capability of the modular cells to have a sufficient margin, which enables to imbalance the loading by increasing the power for the cells by the value for which it was reduced on other cells. This needs to be done without exceeding the rated voltage/current limits or affecting excessive stress for other components. In the design of the system, this can potentially be addressed by overrating the cells, but this increases the system costs, what is not desired. To overcome this problem, while maintaining a cost-effective system, it is proposed to apply the power routing only in partial load operation. As pointed out before, many applications are operating in partial load operation for most of the time and consequently, the control of the loading can be applied in most of the time.

In the following, the power routing capability will be discussed for the considered topologies of the three-stage ST architecture, which are also found in many other applications of power electronics and do to limit the applicability to STs.

The considered modular MV converters, namely the CHB (as shown in Fig. 7.3 (a)) and the MMC (as shown in Fig. 7.3 (b)), consist of series connected SCs. The cells are splitting the overall output voltage  $V_{out}$  equally among each other's as shown schematically for a system consisting of three cells in Fig. 7.4 (a). In this configuration, the same current needs to be conducted by all cells to keep the DC-link voltages constant and to prevent charging

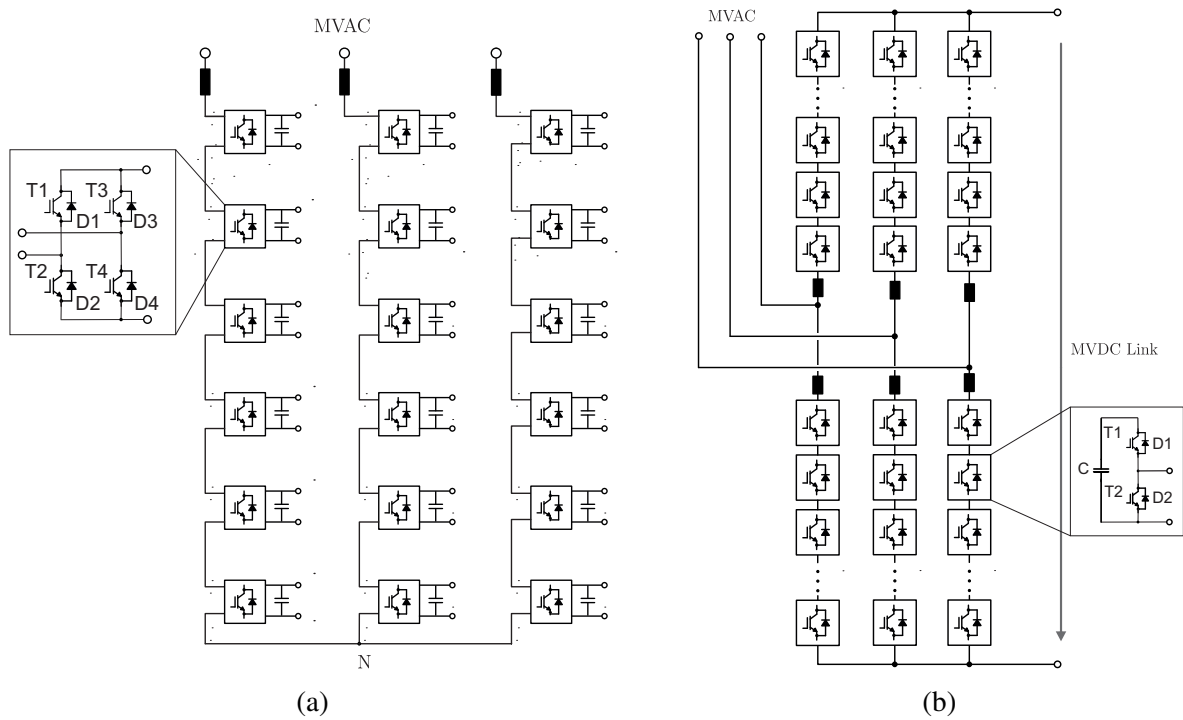


Figure 7.3: (a) Cascaded H-bridge converter (CHB), (b) Modular Multilevel Converter (MMC).

or discharging the capacitors in the SCs. Concerning the power routing capability with respect to a voltage imbalance as shown in Fig. 7.4 (b), it needs to be remarked, that the maximum blocking voltage of a semiconductor is closely related to the conduction losses. Overrating a system for a higher blocking voltage and adding reserve cells is reducing the efficiency, which is not desired. For this reason, the DC-link voltage references of all cells are considered to be equal. With this premise, the MMC has no power routing capability. The power can only be routed, if the SCs of the MMC are directly connected to the converters in the isolation stage. However, this seems to be impractical, because four times more cells are required in the isolation stage compared to the architecture based on the MMC and the QAB in Fig. 2.10 [47]. For this reason, a reliability enhancement for the MMC is concluded to

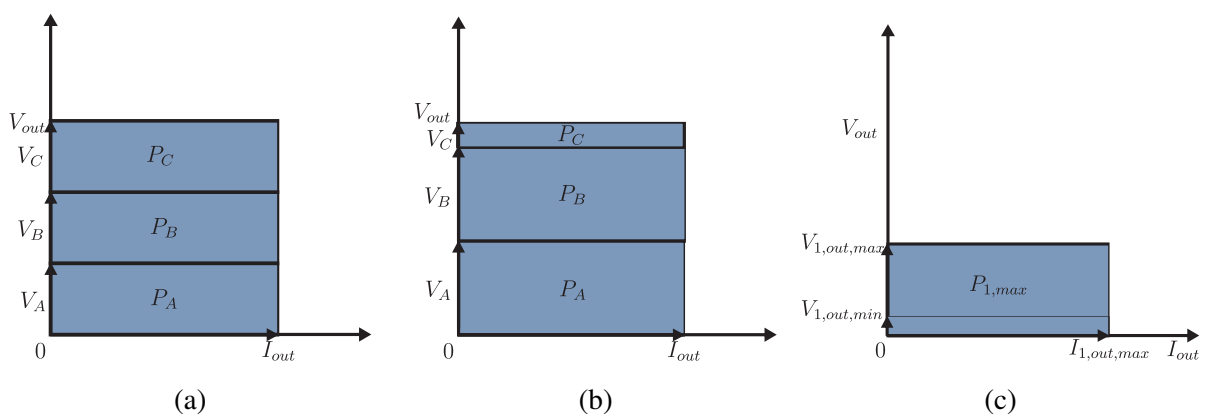


Figure 7.4: Power routing capability of series connected cells (a) balanced loading, (b) unloading cell A, and (c) maximum loading of one cell.

be most practical with reserve cells, as it is already commonly done in HVDC applications, where a faulty SC is bypassed and the system continues to operate [160].

In the CHB converter, the SCs are directly connected to the converters in the isolation stage. These converters are galvanically separated from the others and they can directly exchange power with the SC in the isolation stage. Therefore, it is possible to apply a suitable modulation strategy to imbalance the power transfer among the bridges as shown in Fig. 7.4 (b). Remarkably, the SCs in the CHB still transfer the same current, but the power, which they exchange with the cells in the isolation stage, is different. The maximum achievable unbalance is schematically shown in Fig. 7.4 (c), where the maximum loading is limited to the voltage  $V_{1,out,max}$ . This voltage is maximum for a modulation index  $m = 1$  and results in  $V_{1,out,max} = V_{DC}$ . For the capability to unload a device, the minimum voltage is of interest, which is dependent on the system design, in particular the ratio between grid voltage and DC-link voltage  $V_{grid}/V_{DC}$  and the number of SCs in the converter  $n_s$ . The mathematical expression for the minimum voltage for one cell in the converter  $V_{1,out,min}$  is given in (7.1).

$$V_{1,out,min} = \begin{cases} 0 & \text{if } 1 - (1 - \frac{V_{grid}}{V_{DC}}) \cdot n_s \leq 0 \\ (1 - (1 - \frac{V_{grid}}{V_{DC}}) \cdot n_s) \cdot V_{DC}, & \text{otherwise} \end{cases} \quad (7.1)$$

As an example, one cell in a converter consisting of three SCs with  $V_{grid}/V_{DC} = 0.8$  can be unloaded to  $V_{1,out,min} = 0.4 \cdot V_{DC}$ . This can be extended to the case, that an arbitrary number of cells  $n_{un}$  is unloaded and results in the mathematical representation of (7.2).

$$V_{x_{un},out,min} = \begin{cases} 0 & \text{if } 1 - (1 - \frac{V_{grid}}{V_{DC}}) \cdot \frac{n_s}{n_{un}} \leq 0 \\ (1 - (1 - \frac{V_{grid}}{V_{DC}}) \cdot \frac{n_s}{n_{un}}) \cdot V_{DC}, & \text{otherwise} \end{cases} \quad (7.2)$$

If two out of three cells with the similar ratio between grid voltage and DC-link voltage  $V_{grid}/V_{DC} = 0.8$  are intended to be unloaded, it is found, that the minimum voltage is  $V_{2,out,min} = 0.7 \cdot V_{DC}$ . This is also visualized in Fig. 7.5 for up to 20 series connected cells and the target to unload 1-9 cells.

In the parallel converters, as it can be realized in the LV stage of an ST or in power stacks for wind turbines, the current can be unequally distributed among the power converters. The schematic case of parallel connected converters with equal loading is shown in Fig. 7.6 (a), where the three cells share the current equally. This is independent from the chosen converter topology possible. For the lifetime control, it is proposed to imbalance the power transfer, which is schematically shown in Fig. 7.6 (b). The power converters share the same output voltage, but the current can be shared unequally among the cells. The maximum current  $I_{1,out,max}$ , which one cell can transfer is limited by its rated current. For unloading one cell, the minimum current is dependent on the number of parallel SCs  $n_p$  and the overall output current  $I_{out}$ . This is expressed in (7.3).

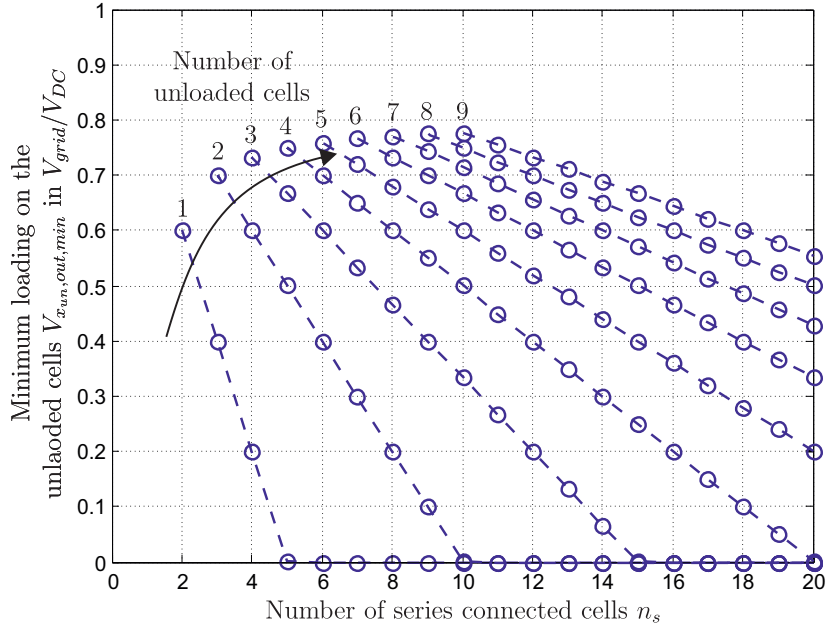


Figure 7.5: Capability for unloading series connected cells in a modular power converter with  $V_{grid}/V_{DC} = 0.8$ .

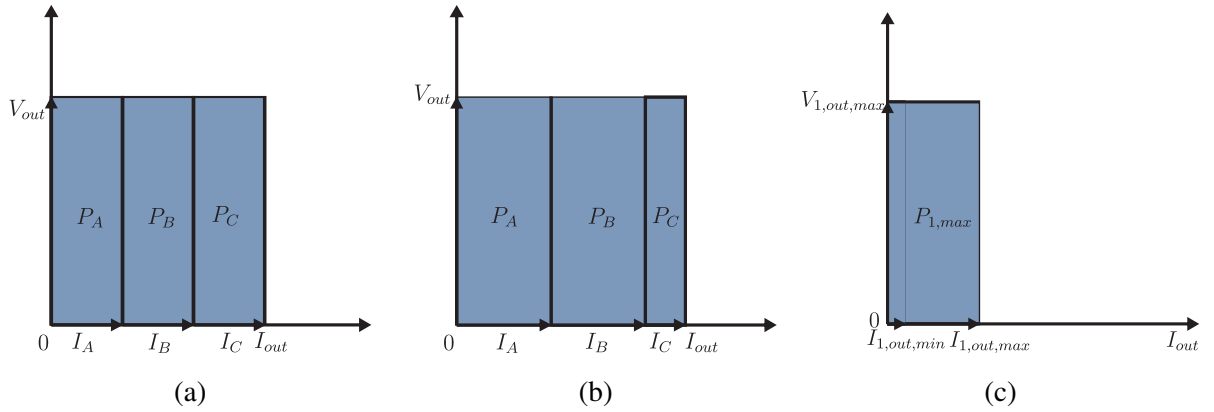


Figure 7.6: Power routing capability of parallel connected cells (a) balanced loading, (b) unloading cell A, and (c) maximum loading of one cell.

$$I_{1,out,min} = \begin{cases} 0 & \text{if } (n_p - 1) \cdot I < I_{out} \\ I_{out} - (n_p - 1) \cdot I, & \text{otherwise} \end{cases} \quad (7.3)$$

With this equation, it can be shown, that in a converter with three cells  $n_p = 3$ , one cell can be completely unloaded for up to 66.7 % of the rated current. The more general form in dependence of an arbitrary number of unloaded cells is expressed in (7.4).

$$I_{n_{un},out,min} = \begin{cases} 0 & \text{if } (n_p - n_{un}) \cdot I < I_{out} \\ \frac{I_{out} - (n_p - n_{un}) \cdot I}{n_{un}}, & \text{otherwise} \end{cases} \quad (7.4)$$

Based on this equation, it can be shown, that two SCs can be completely unloaded up to

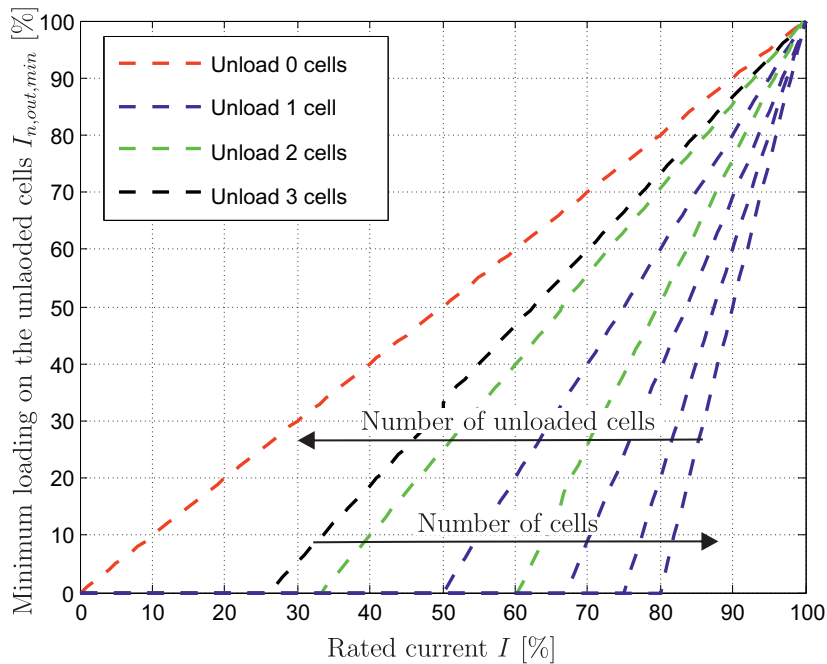


Figure 7.7: Capability for unloading parallel connected cells in a modular power converter.

0.33  $I_{out}$ . The power routing capability of parallel connected cells is visualized in Fig. 7.7 for up to four parallel cells and the case of unloading 1-3 of the cells. Despite the dependence of the power routing potential on the system design, it is concluded, that the restriction in the parallel systems are much less stringent compared to the series case and less building blocks per cell to be unloaded are required.

In isolated DC/DC converters, as they can be found in the isolation stage of the ST, the power routing capability of the DAB and the SRC is limited to the interaction with the MV stage. The QAB has the capability to imbalance the power transfer, but this requires additional parallel or series redundancy. This is investigated in section 7.4.

## 7.2 Power routing for series connected building blocks

In this subsection, the power routing for series connected building blocks, namely the CHB converter, is proposed. The regulation of the power transfer between the DC-links of the CHB converter and the components connected to these DC-link is addressed. It is proposed to use this concept to control the thermal stress for the components connected to the DC-links. The concept of using multiple frequencies for increasing the power routing capability is introduced and analyzed. Experimental results are presented to demonstrate the claim to control the power in the different cells. Finally, the effect of the power routing on the stress is analyzed.

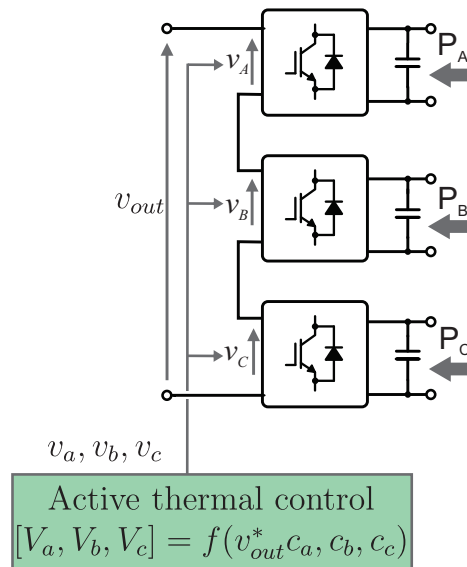


Figure 7.8: Single-phase seven level CHB converter with the proposed active thermal control scheme.

### 7.2.1 Introduction of multi-frequency power routing

To the current state, several techniques have been proposed for balancing the power in the cells of modular power converters in order to share the stress identically [161]. These algorithms rely on the sharing of the fundamental voltage among multiple CHB cells (see Fig. 7.3 (a)) or employ advanced balancing schemes embedded in the modulator without an external control loop [161]. In a similar way to the power balancing method, the fundamental voltage among multiple CHB cells can achieve the designated imbalance power routing, but offers a limited capability. This capability is dependent on the number of SCs and the ratio between DC-link voltage and converter output voltage. In addition, due to efficiency reasons, the DC-link voltage margins should be designed as low as possible. Therefore, in order to overcome the limitation of the conventional fundamental voltage method, the multi-frequency power routing, using the third-harmonic voltage, is proposed.

First, the fundamentals for applying the third harmonic based power routing are described and the concept is explained. In a seven level CHB converter as shown in Fig. 7.8, the power routing is demonstrated to control the loading of the three power path  $P_A$ ,  $P_B$  and  $P_C$ . Thereby the DC-link voltages of the cells are kept constant, while the converter output voltage is controlling the output current in each cell.

The concept of multi-frequency power routing can be applied to prevent or delay the failure of specific components. It holds the advantage not to influence the operation with the fundamental frequency, while the stress for the isolation stage is redistributed. As an example, a seven level CHB converter as shown in Fig. 7.9 has three cells with three power paths ( $P_A$ ,  $P_B$  and  $P_C$ ) and the components in one of them, e.g. in the DAB cells, show far higher degradation than the others. Since the converter is dependent on the operation of all cells, a failure of one cell or power path is the end of life. Instead of loading the cells equally (as shown in Fig. 7.9 (a)), unloading the power path with the highest degradation postpones

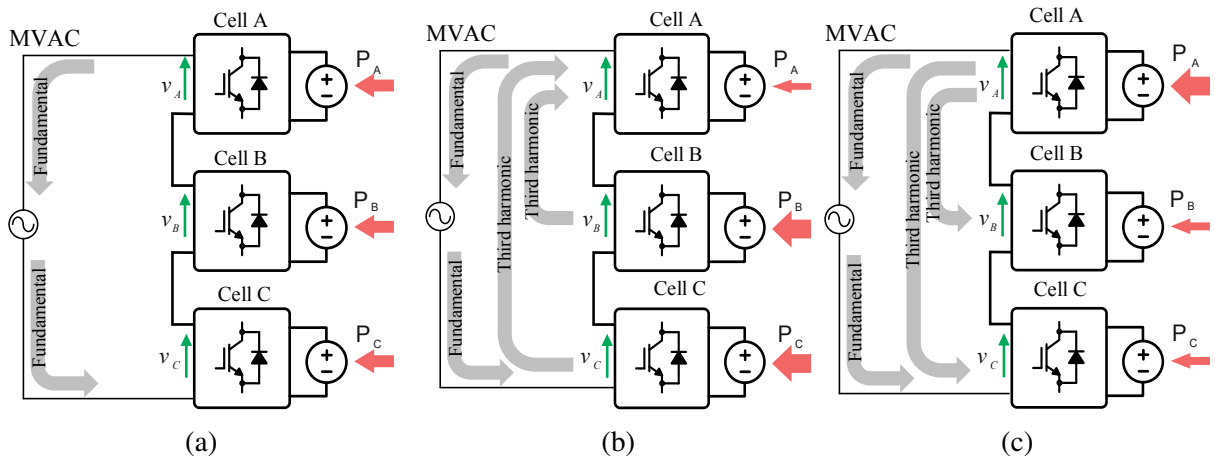


Figure 7.9: Power flow between CHB cells by multi-frequency method in case of (a) balanced loading C, (b) unloading cell A, and (c) overloading cell A.

the time to the failure, which is demonstrated in Fig. 7.9 (b) for unloading path A. As the opposite concept, it is possible to load one path higher and to bring it close to its wear out. This might be a solution, if the next maintenance is scheduled and the cell is planned to be replaced, while the remaining ones will not be replaced. This case is visualized in Fig. 7.9 (c). In contrast to bypassing the cell, which is commonly done after a failure in a modular converter, it holds the advantage to keep the cell in operation and still contribute to the output voltage reserve.

It is important to note that the basic principle can be extended to a greater number of cells and harmonics, always improving the DC-link voltage utilization for power imbalance among the cells. In order to maximize the DC-link voltage utilization, the derivation of the optimal magnitude of the third harmonic holds high similarity to the mathematical derivation of the third harmonic in the PWM modulation as presented in [162]. The modulation function with additional third harmonic in dependence of the angle  $\varphi_u$  and the modulation index  $M$  is expressed in (7.5).

$$m = M \cdot \cos(\varphi_u) + M \cdot k_3 \cdot \cos(3 \cdot \varphi_u) \tag{7.5}$$

Similar to the third harmonic injection, the minimum magnitude is obtained for  $k_3 = -1/6$ , leading to the maximum of the modulation function  $m_{max} = \sqrt{3}/2$ . This enables to utilize the linear range of the converter cells up to the inverse of  $m_{max}$ , which is  $M = 1.155$ . Of course, the power reduced with the third harmonic of one cell, needs to be provided by the other cells, which requires them to add the opposite harmonic sequence to their modulation function.

For the demonstration of the concept, Fig. 7.10 shows the unbalanced power sharing among three cells by means of the multi-frequency power routing method, where from the first to the third row are the duty cycle of three cells, A, B, and C, respectively. The last row shows the output power with respect to each cell. Since the duty cycle is typically normalized by the DC-link voltage, it is used instead of the actual voltage in the figure. In the first column,



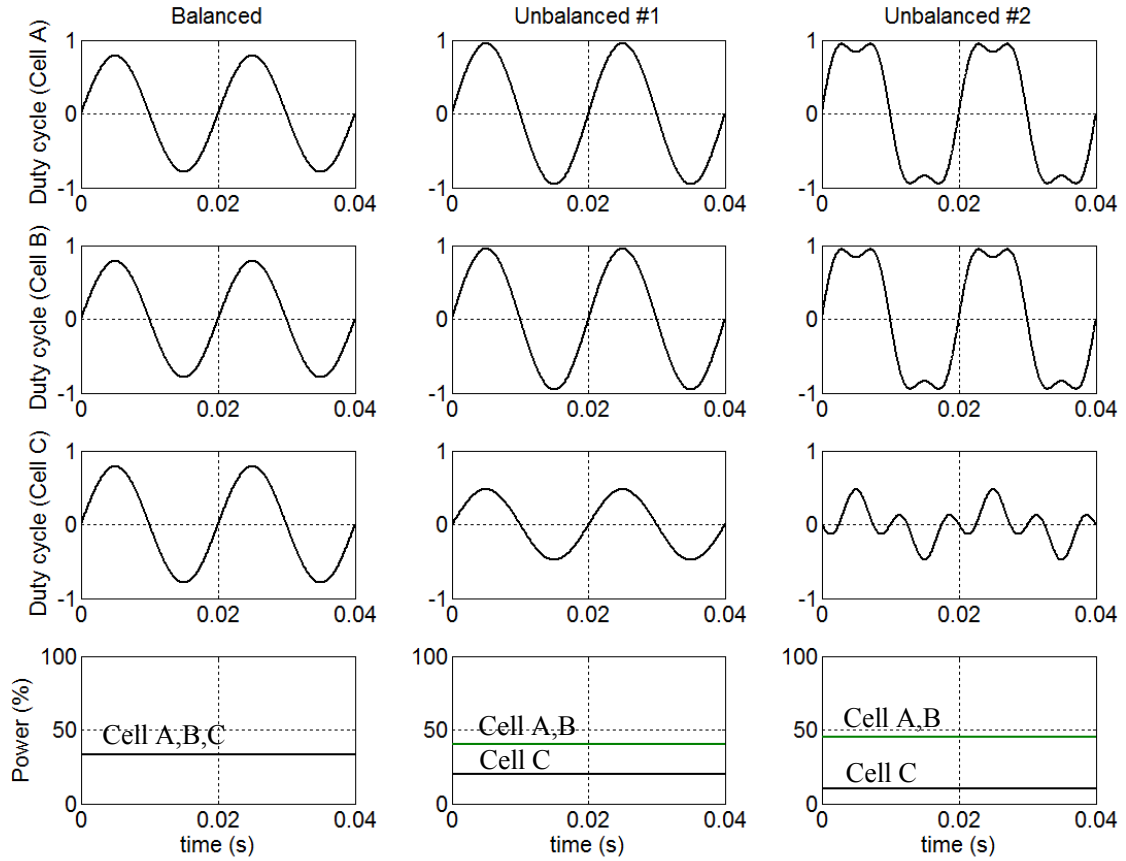


Figure 7.10: Principle of imbalance power routing by multi-frequency method: Balanced is equal loading of all devices, Unbalanced #1 is unloading cell C with the fundamental frequency and Unbalanced #2 is unloading cell C with multi-frequency power transfer.

the three cells share equal power, e.g. balanced power routing, with the same duty cycles. For the unbalanced power routing, the duty cycle of the overloaded cells increases, while that of the unloaded cell decreases.

As depicted in the second column, the unbalanced power routing by the fundamental voltage is restricted when two of the three duty cycles reach the maximum duty cycle. In order to achieve an even higher power imbalance, the third harmonic is utilized, which is in phase with the fundamental voltage as shown in the third column. For the overloaded cells, the third harmonic voltage is added to the fundamental voltage so that the fundamental voltage utilizes the maximum linear range of  $M = 1.155$ . The fundamental voltage of the unloaded cell is reduced and it is absorbing the third harmonic voltage from the overloaded cells.

To point out the additional power routing capability (7.6) is used to express the limits of the minimum voltage  $V_{num,out,min,mf}$  for unloading SCs. Thereby  $x_3$  has been introduced to express the improved power routing capability with the third harmonic.

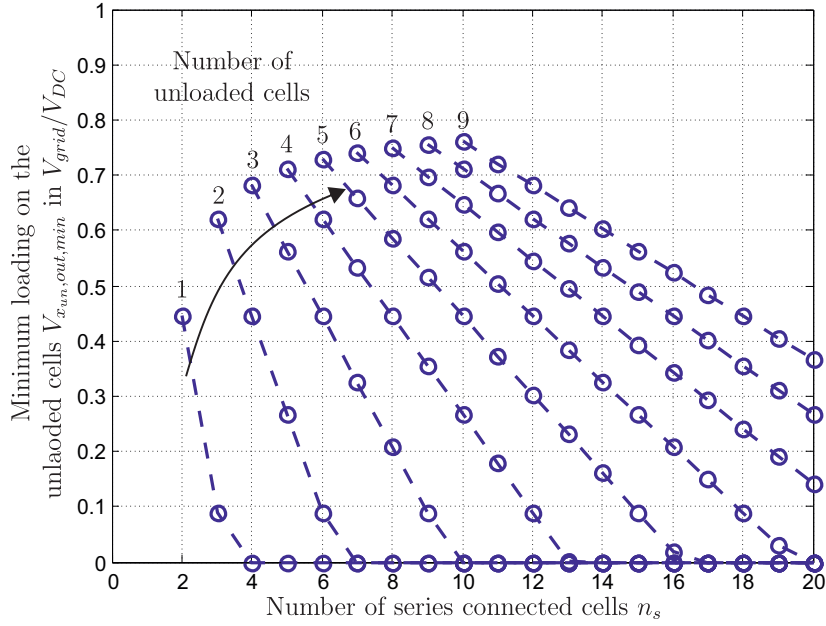


Figure 7.11: Capability for unloading the fundamental voltage of series connected cells in a modular power converter with  $V_{grid}/V_{DC} = 0.8$ .

$$V_{n_{un},out,min,mf} = \begin{cases} V_{grid} & \text{for } n_s = n_{un} \\ 0 & \text{if } 1 - (1 - \frac{V_{grid}}{V_{DC}} + x_3) \cdot \frac{n_s}{n_{un}} \leq 0 \\ (1 - (1 - \frac{V_{grid}}{V_{DC}} + x_3) \cdot \frac{n_s}{n_{un}}) \cdot V_{DC}, & \text{otherwise} \end{cases} \quad (7.6)$$

The increased power routing capability is expressed in (7.7).

$$x_3 = 0.155(1 - \frac{n_{un}}{n_s}) \quad (7.7)$$

It can be seen that the increased power routing capability is particularly improved for a high number of series connected cells, when only a small number should be unloaded. If instead a high number of cells needs to be unloaded,  $x_3$  converges to zero. This is caused by the fact, that the higher loaded cells need a sufficient number of cells, which can take over the inverse third harmonic component. The overall power routing capability with the third harmonic is visualized in Fig. 7.11.

Compared to the power routing capability only with the fundamental frequency, the potential power imbalance can be increased by 15.5 % per higher loaded cell. While in the former example, the power routing potential to unload two cells for  $V_{grid}/V_{dc} = 0.8$  was limited to 70 %, it can now be even reduced to 55 %. Nevertheless, it needs to be pointed out, that the cost is an increased third harmonic component on the unloaded cell.

Based on the seven level CHB converter, the power transfer in the different power paths can be controlled. The implementation of the power routing is achieved with an additional

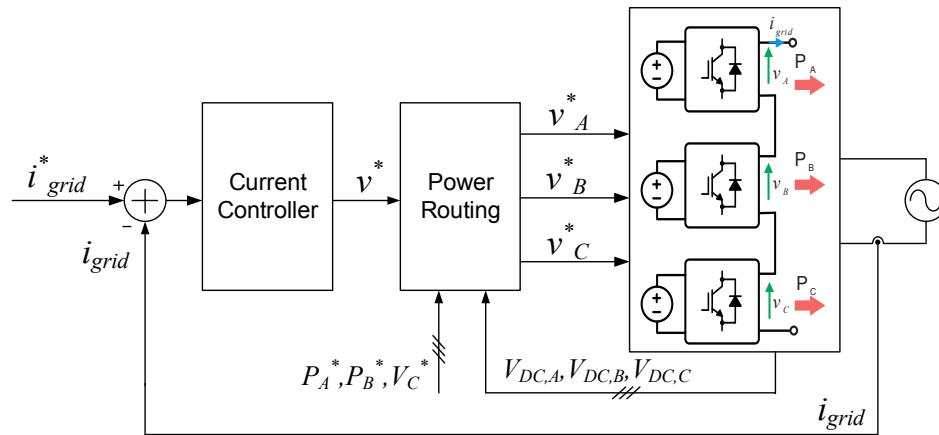


Figure 7.12: Current control scheme of a grid connected seven level CHB applying multi-frequency power routing.

open loop control nested in the standard current controller, as shown in Fig. 7.12. The fundamental components are determined depending on the power reference, and the second constraint is the cancellation of the third harmonic for the multi-frequency method. When the reference power of each cell is different, the unbalanced power routing is activated and it is determined whether the multi-frequency method should be applied or not, depending on the power reference ( $P_A$ ,  $P_B$  and  $P_C$ ). The multi-frequency method is applied when one of the fundamental references exceeds the maximum modulation index. In this situation, proper third harmonics are determined until the maximum  $k_3 = 1/6$  is reached.

### 7.2.2 Experimental validation of the algorithm

The power routing is tested on a seven level CHB converter implemented on a microcontroller and the CHB converter is connected to a passive load. For the demonstration, it is operated in open loop for a ratio between grid voltage and DC-link voltage of  $V_{grid}/V_{dc} = 0.7$ . This is shown for the balanced case in Fig. 7.13 (a), the power routing with the fundamental frequency in (b) and with the multi-frequency power routing in (c). The algorithm operates as expected and with only the fundamental frequency, cell C still needs to contribute with  $MI_1 = 0.1$  to the output power. The multi-frequency method enables to remove the fundamental frequency from cell C, but requires an increased third harmonic for the cell. This also has an effect on the current ripple in the output current of the CHB converter, which is analyzed in detail in [163].

To validate the power routing, a power analyzer (Yokogawa WT1800) measures the power of the cells for the cases of Fig. 7.13, which is shown in Fig. 7.14. Similar to the waveforms shown before, the power is processed with equal loading, with the fundamental voltage method and with the multi-frequency method. In accordance to the prior obtained results, the fundamental voltage enables to unload one device, while the capability is remarkably increased with the multi-frequency method. The power exchanged with the DC-link of cell C is almost zero. However, cell C is still required to contribute to the reactive power exchange with its third harmonic.

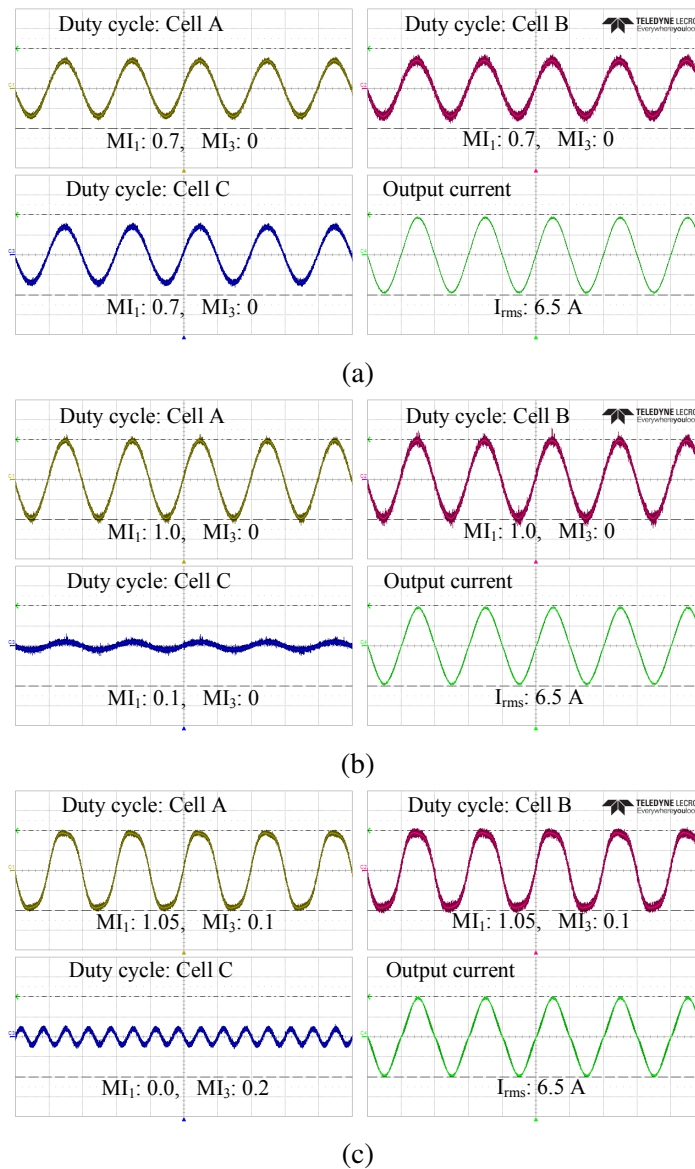


Figure 7.13: Measurement of duty cycles of each cell and output current under  $V_{grid}/V_{dc} = 0.7$ ,  $V_{dc} = 155 \text{ V}$ ,  $R = 35.4 \Omega$  and  $L = 1.3 \text{ mH}$ : (a) balanced, (b) unbalanced by fundamental component, (c) unbalanced by multi-frequency.

### 7.2.3 Mission profile based evaluation of the algorithm

It needs to be pointed out, that the capability of controlling the stress depends highly on the system design and the mission profile. With only small variations in the power, the thermal fluctuations can be eliminated from cells, while high power fluctuations affect all SCs.

In the architecture based on the CHB and the DABs in Fig. 2.11, the CHB cells exchange power with the DABs in the isolation stage. Consequently, the CHB cells can control the power flowing in the DABs by still transferring similar overall power to the LVDC link. As pointed out before, this can be utilized in order to unload the power paths with higher degradation for preserving its current health status and to stress the components as low as possible. Here, the power cycling is assumed to be the main failure mechanism, which leads

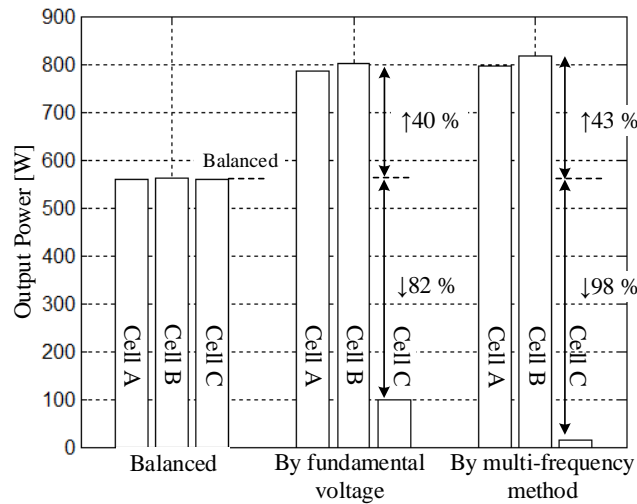


Figure 7.14: Power measurement of each cell under balanced and unbalanced conditions for  $V_{grid}/V_{dc} = 0.7$ . Power routing is applied with the fundamental frequency and the multi-frequency algorithm.

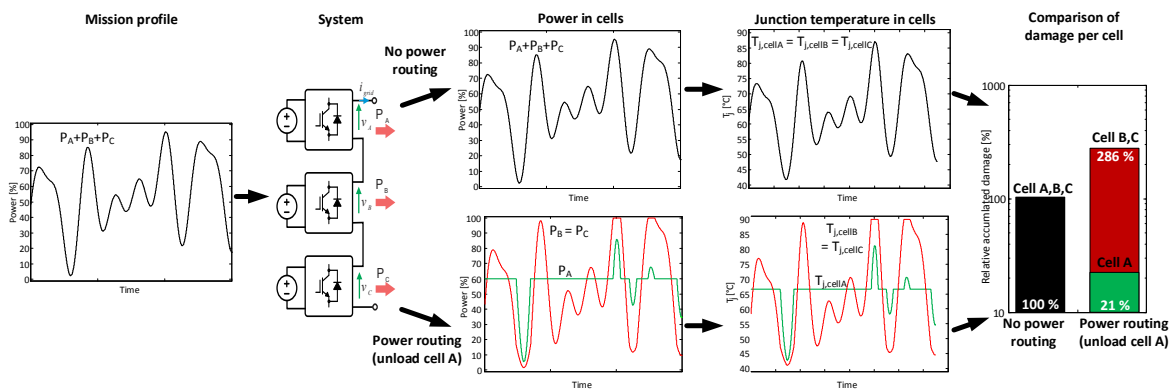


Figure 7.15: Effect of power routing in the CHB on the thermal loading and the normed damage caused in the power semiconductors in the DAB with  $v_{grid}/V_{dc} = 0.8$ .

to the requirement to prevent power variations for unloading the components. It is important to point out, that this failure mechanism is less influenced by the constant power operation.

In Fig. 7.15, the application of the algorithm is presented in a case study under consideration of the power routing limitations of the CHB converter. A mission profile with fluctuating power is presented and the multi frequency power routing is applied to control the loading, particularly preventing power fluctuations in path A. The converter operation is simulated analytically under consideration of the power routing capability and the efficiency of the cells. The cooling system is assumed to be designed for an ambient temperature  $T_a = 40\text{ }^\circ\text{C}$  and the maximum junction temperature  $T_{j,max} = 90\text{ }^\circ\text{C}$  under full load. The power fluctuations result in thermal fluctuation on the power semiconductors, which usually would be shared equally by the cells. However, in this case the path with the power  $P_A$  should be unloaded and targets to operate with constant power whenever it is possible. Consequently, the fluctuations in the other paths are increased. In this study, the power variations are assumed to be slower

than the dynamics of the heatsink, which results in a negligible influence of the thermal capacitors. The damage caused by the thermal cycling is reduced to  $1/5^{th}$  for the unloaded path, while the higher loaded paths increase to approximately 3 times more damage.

### 7.3 Power routing for parallel connected building blocks

This subsection proposes to route the power in the parallel converters in dependence of the wear out of their components. The equalization of the lifetime consumption of the single converters is targeted to schedule prognostic maintenance and thereby reducing the total operating costs. The strategy is introduced and implemented with virtual resistors. The effectiveness of the approach is experimentally demonstrated with fast junction temperature measurement for three parallel VSCs.

#### 7.3.1 System description

To overcome the problem of different remaining lifetimes of the power electronic modules, this work proposes to take advantage of the modularity of the system. The proposed approach is not to shut down modules, as it is done for the optimization of the efficiency in multi-phase DC/DC converters, but to route the power along different paths in partial load operation [15]. This enables to control the lifetime of the system and to extend the operation time for modules with high accumulated damage, which can be estimated with condition monitoring techniques. The goal is to let the weaker modules survive until the next maintenance is made, stressing them less compared to the stronger ones. Given these premises, the power is shared among the modules depending on the consumed lifetime. Moreover, the estimation of the consumed lifetime can be used to schedule prognostic maintenance.

In the following, the power routing concept is presented with the application of virtual resistors in the parallel power converters. The virtual resistors need to be tuned for achieving the maximization of the time to the next failure. For this tuning of the algorithm, it is important to define which failure mechanisms is dominant to ensure that the goal is achieved.

Several applications are challenged by a relatively low voltage and a high current rating, as it can be found in the LV stage of the ST. A possible solution are multiple parallel power converters, as it is already commonly done in parallel power stacks in wind turbines. In this work, three parallel power converters are considered as shown in Fig. 7.16 (a). In addition, the active thermal control scheme is shown in Fig. 7.16 (b) with the current to be the control variable. Each of the single converters consists of a two level VSC as shown in Fig. 7.17. The advantage of the parallel power converters is redundancy in case of a failure and the possible interleaved operation of the converters, enabling a reduction of either the switching frequency or the filter size in comparison with a single power converter.

Despite the advantages of parallel converters, there are issues, such as circulating currents if a shared DC-link is used for the three converters [164]. However, this is not the scope of this

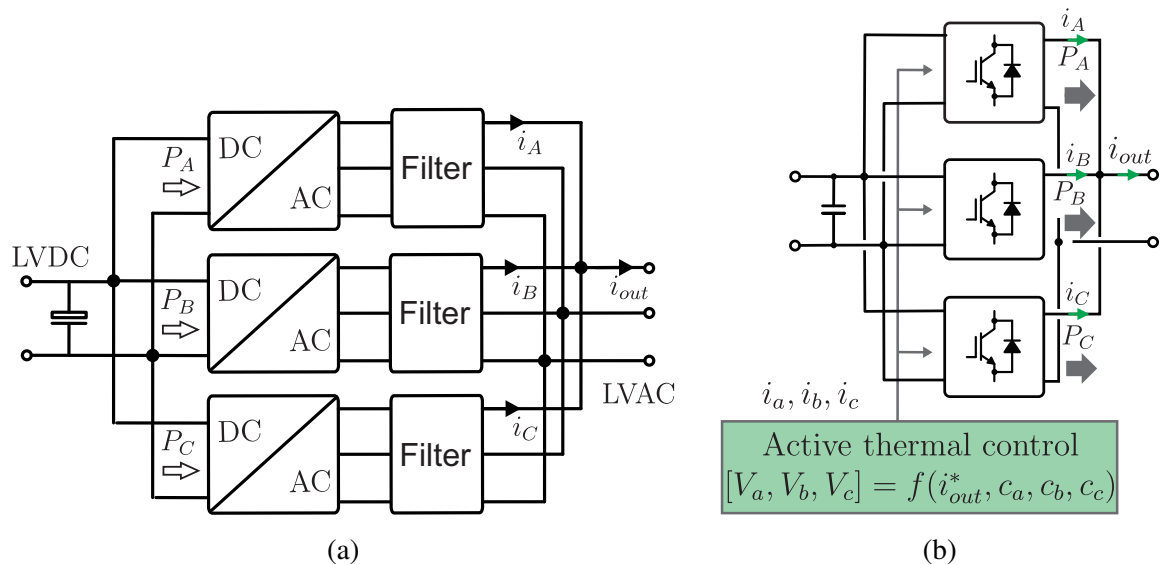


Figure 7.16: Power routing in the LV stage: (a) System of three power converters for the LV stage, (b) Architecture with the proposed control variables.

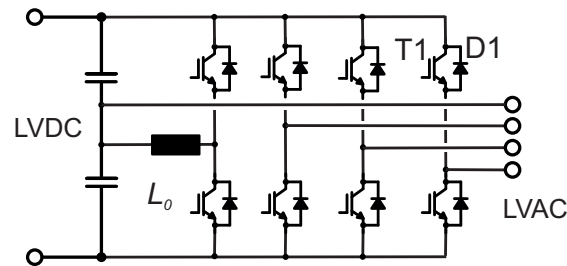


Figure 7.17: Two level Voltage Source Converter (VSC).

work and the known solution to use single-phase inductors for each converter is applied to overcome this problem.

### 7.3.2 Lifetime based control of the converter

Power converters are commonly controlled in the flux/field oriented control in the application of electric machines or the voltage oriented control in grid connected converters. As a similarity of these applications, the outer control loop is generating a current reference for the inner control loop. For the application of the power routing, only the inner current control is of interest and investigated in this work. The reference current is divided into the different reference values for the cells. This implementation in the current controller is shown in Fig. 7.18. The control of the power sharing is done with virtual resistors, which are used to route the power similar to current divider in the basics of electronics. These virtual resistors reflect the condition of the different cells ( $A \in (0,1)$ ), whereby  $A = 0$ , describes unstressed power semiconductors and  $A = 1$  determines the end of life for the power semiconductors. A possible model to determine  $A$  is the linear Palmgreen Miners rule, which is based on Rain-flow counting of the power semiconductors junction temperature and damage accumulation [165]. Consequently, the most aged power cells will be stressed least in the system. For

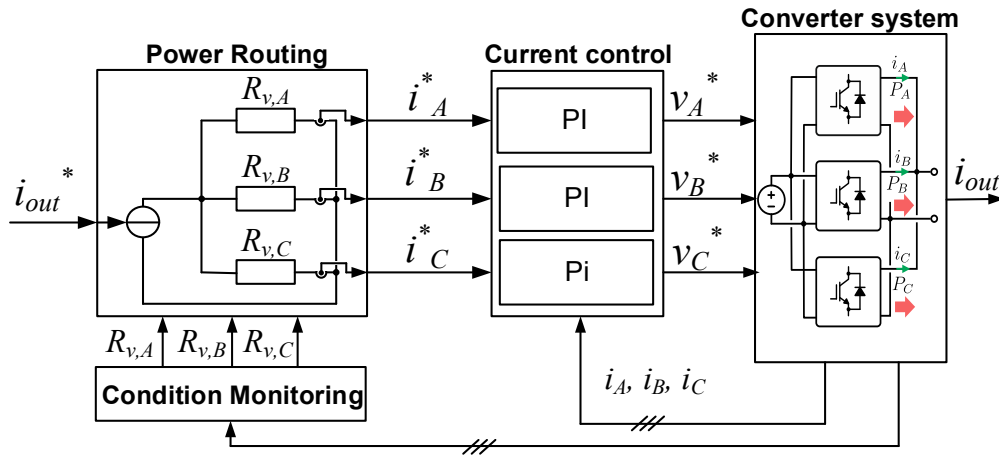


Figure 7.18: Control diagram of the power routing algorithm based on condition monitoring.

similar conditions of the converter, the power needs to be distributed equally and all virtual resistors need to have the same resistance. As an example for the current transferred in converter A,  $i_A^*$ , is dependent on the overall reference current generated by the voltage controller  $i_{out}^*$  and all virtual resistors in the parallel paths. This is mathematically expressed in (7.8).

$$i_A^* = i_{out}^* \cdot \frac{R_{v,A}R_{v,C}}{R_{v,B}R_{v,C} + R_{v,A}R_{v,B} + R_{v,A}R_{v,C}} \quad (7.8)$$

The power routing for all three reference currents is shown in a matrix representation in (7.9).

$$\begin{bmatrix} i_A^* \\ i_B^* \\ i_C^* \end{bmatrix} = \frac{i_{out}^*}{R_{v,B}R_{v,C} + R_{v,A}R_{v,B} + R_{v,A}R_{v,C}} \begin{bmatrix} R_{v2}R_{v3} \\ R_{v1}R_{v3} \\ R_{v1}R_{v2} \end{bmatrix} \quad (7.9)$$

It needs to be pointed out, that the power routing does not require an oversizing of the converter system. In case that a converter receives a higher current reference than the maximum current, the power exceeding the limit is redistributed for the other converters. Consequently, under full load every single converter is processing the rated power, independently from the tuning. As a potential challenge, circulating currents among the converters need to be suppressed. To overcome this problem, a closed loop control is implemented to prevent power circulation among different converters.

### 7.3.3 Reliability impact of power routing

In this subsection, the effect of unequal loading on the junction temperature of the converter is experimentally evaluated. The junction temperature of the power semiconductors in the three parallel power converters is measured with the optical fiber instrument and this enables to measure the junction temperature in the open modules. The three parallel converters with open IGBT modules share the same DC-link and have single-phase inductors at the output of



Table 7.1: Parameters of the laboratory setup.

Rated current per converter	25 A
DC link voltage	200 V
Filter size	1.8 mH
Load R	3.5 $\Omega$
Fundamental frequency	50 Hz
Switching frequency	20 kHz
Power Semiconductor module	Danfoss DP25H1200T101667

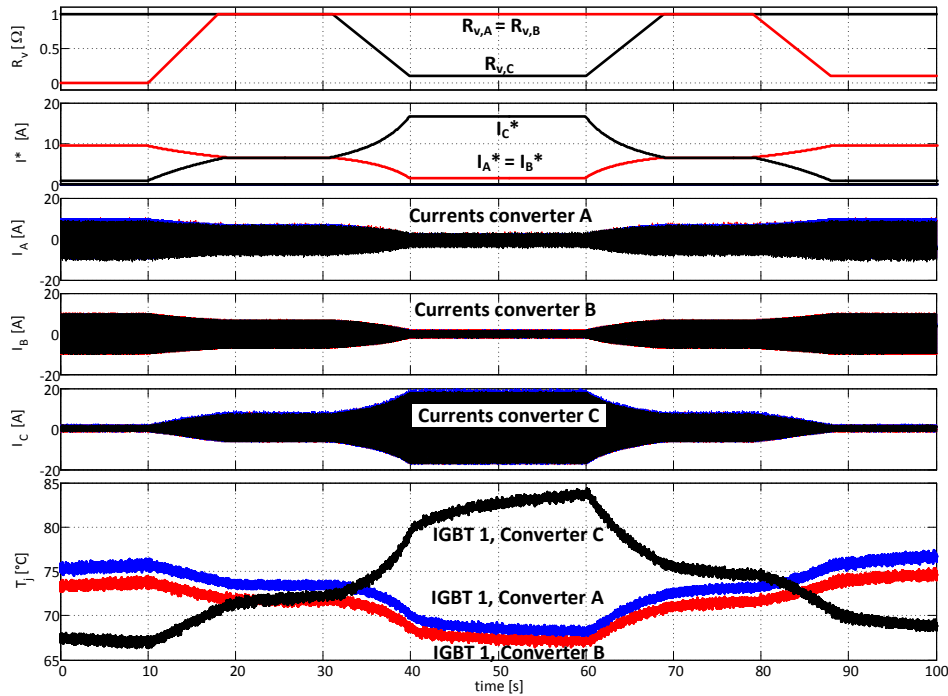


Figure 7.19: Measurement: Power routing in three parallel converters by means of virtual resistors for constant output power and a variation of the virtual resistors.

each phase. The IGBT modules are not filled with gel for direct measurement of the junction temperature, which is reducing the blocking voltage capability of the power module. The converters feed a three-phase resistive load and the parameters of the setup are shown in table 7.1. The capability of unloading parts of the system is demonstrated with high-speed junction temperature measurement. This junction temperature measurement is carried out by fiber optic temperature sensors directly attached on the chip.

The infrared camera is used to detect the hottest spots in the power electronic module. This hotspot is affected by singular spots on the chip as well as by the thermal cross coupling of the power semiconductors. The highest temperature is measured in IGBT 1 and for this reason the junction temperature of the IGBT T1 is measured in each of the converters.

First, the three converters are feeding constant current and the current distribution is varied slowly for demonstrating the capability of the controller to unequally load the devices in Fig. 7.19. Initially, converter C is unloaded and by a variation of the virtual resistor, all

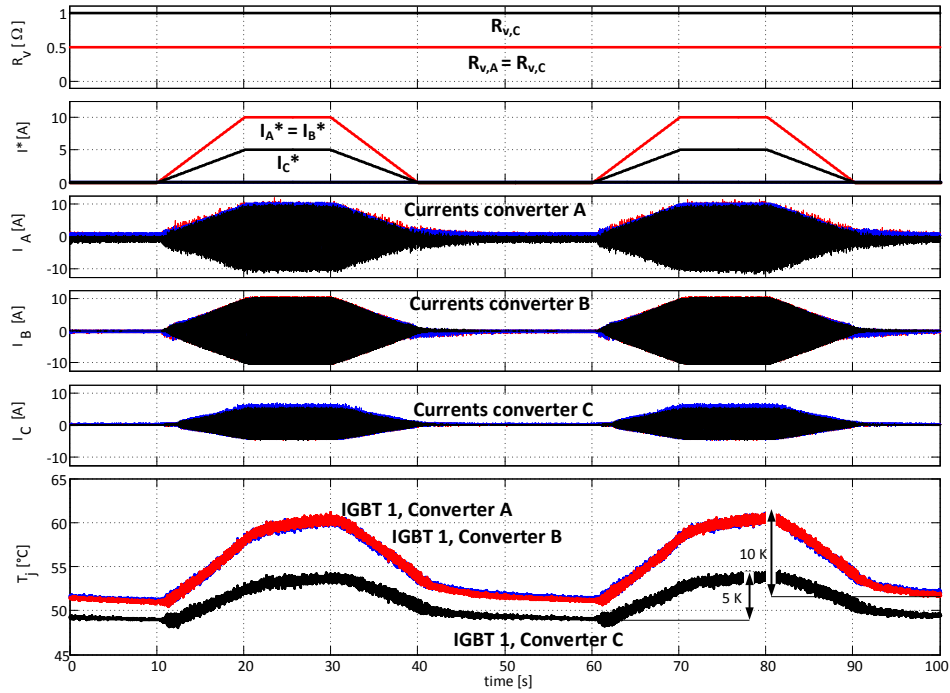


Figure 7.20: Measurement: Power routing in three parallel converters by means of virtual resistors for power cycle.

converters are loaded equally. Afterwards, the converter C is loaded higher, while the other two converters are unloaded. Finally, the virtual resistors are varied again to achieve equal power transfer and then back to the initial status. From the reference current, it can be seen, that the power is routed according to the virtual resistors as desired. The measured currents are in accordance with the reference value. However, even more important is the visible effect on the junction temperature. During equal loading of the converters, the junction temperature is approximately equal, but unloading a part leads to a reduction in the junction temperature. Similar to the single converter, the higher loaded converters exhibit an increased junction temperature. Thus, the capability to route the power among the different converters is demonstrated.

In the next step, the effect of the power routing on the thermal stress and consequently on the reliability is demonstrated. For this purpose, the reference current  $i_{out}^*$  is varied for different virtual resistors and the resultant power distribution is shown in (7.10).

$$\begin{bmatrix} R_{v,A} \\ R_{v,B} \\ R_{v,C} \end{bmatrix} = \begin{bmatrix} 0.5 \\ 0.5 \\ 1 \end{bmatrix} \rightarrow \begin{bmatrix} P_A \\ P_B \\ P_C \end{bmatrix} = \begin{bmatrix} 40 \% \\ 40 \% \\ 20 \% \end{bmatrix} \quad (7.10)$$

In this case, only the current is varied, while all other parameters are kept constant. The power cycle can be seen in the reference value of Fig. 7.20 as well as in the current distribution among the converters. Again, the measured currents have the same magnitude as the reference current, which demonstrates the functionality of the power routing. The power cycle is affecting a thermal cycle in the junction temperature measurements as expected. This

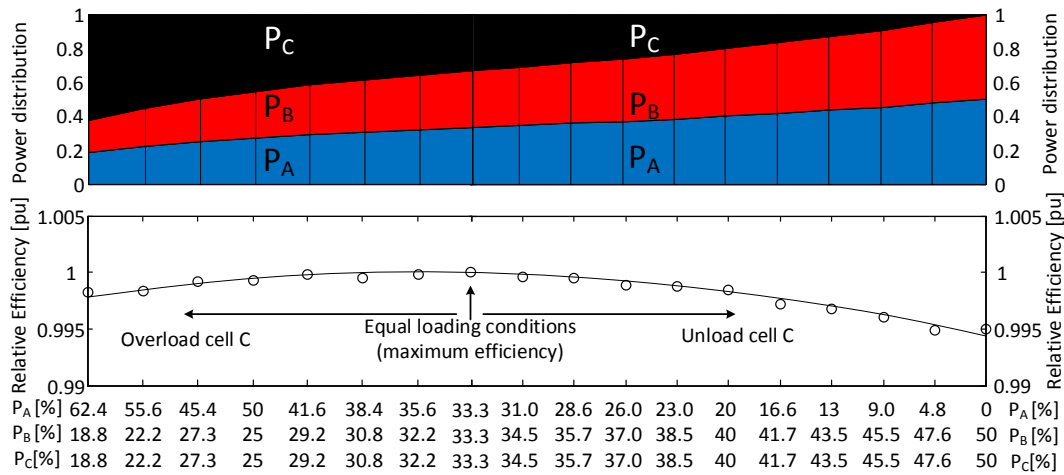


Figure 7.21: Measurement: Effect of Power routing on the efficiency of the converter system for unloading one converter and for overloading one converter.

temperature cycle shows a proportional behavior to the power distribution, which results in  $\Delta T = 10K$  for converter A and converter B, while the thermal cycle in converter C is only  $\Delta T = 5K$ . Also the average temperature of converter C is reduced, which is also affecting the stress.

As a consequence, the lifetime of the power semiconductors is consumed unequally. Following the simple lifetime model expressed in (3.1), the thermal swing  $\Delta T$  influences the lifetime consumption exponentially, leading to 32 times higher damage for the power semiconductors in converter A and B in comparison to those in converter C. This is even amplified with the difference in the average junction temperature, which is also higher for the two higher loaded converters. Consequently, the equalization of the wear out during a relatively high remaining lifetime requires only a very small imbalance of the power in the converters. A small remaining lifetime instead results in a high power imbalance, but has high potential to unload the thermal stress from the device for extending its lifetime. Beside the potential, it needs to be pointed out, that unequal loading of the devices consumes more lifetime of the system if all damages are summed up.

### 7.3.4 Efficiency impact of power routing

The impact of the power routing on the efficiency of the system is evaluated experimentally in this subsection. For the efficiency measurement, a Yokogawa WT1800 power analyzer is used. The efficiency is measured for the case that two of the converters process the same power, while the power of a single converter is either reduced or increased. The results for the different power distribution and the related efficiency measurement are shown in Fig. 7.21, when a single converter is unloaded and when a single converter is overloaded. Due to the open modules, the maximum blocking voltage is limited and thus neither the converter nor the operation point is optimized. For this reason, the efficiency is normalized on the maximum efficiency of the converters found during equal power sharing. The power

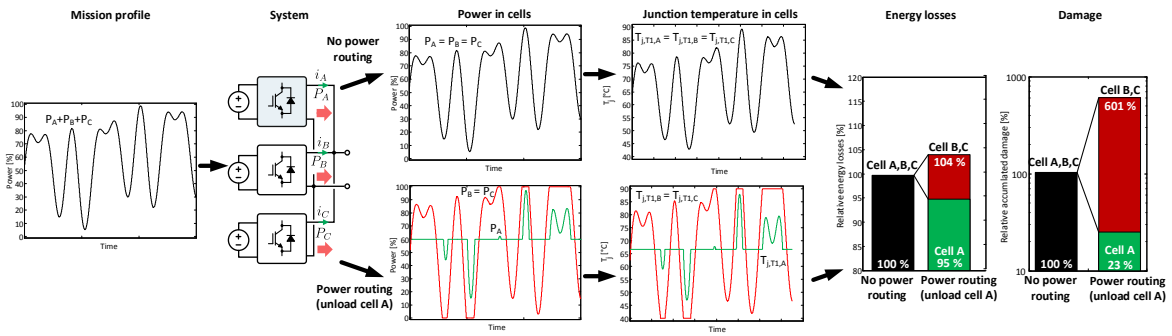


Figure 7.22: Schematic effect of power routing in three parallel power converters on the thermal loading and the normed damage caused in the power semiconductors.

distribution between the converters is visualized in the upper plot and quantified at the x label of the lower plot.

The measurements are obtained for approximately similar junction temperatures of  $T_{j1} = T_{j2} = T_{j3} = 60^\circ\text{C}$ . It can be seen, that unloading a power converter reduces the efficiency of the converter, which can also be observed for overloading one converter. Nevertheless, the maximum reduction in efficiency is only 0.5 % in the most extreme operating conditions. It needs to be pointed out, that this is the operation point with the highest unbalance, while smaller variations in the loading of the converters have a lower reduction of the efficiency. Overloading one converter results in a similar behavior, whereas it needs to be mentioned, that not all operation points could be measured because of the high current in the single converter. Nevertheless, the trend in the reduction of the efficiency is similar to the case of unloading one converter.

### 7.3.5 Mission profile based evaluation of the algorithm

In addition to the experimental demonstration of power routing, a mission profile based thermal stress evaluation is performed. Similar to the series connected power routing, the influence of power routing in the parallel cells is investigated analytically under consideration of the limitations of the power routing capability. A mission profile is developed and is simulated for the three parallel power converters, which are assumed to have a similar thermal design as the series connected building blocks in the mission profile analysis. This is shown in Fig. 7.22. Again, a mission profile with highly fluctuation power is analyzed and shared unequally by the different cells. Based on the thermal profile, Rainflow counting is applied and the data is used to calculate the damage for the power semiconductors. As it can be seen, the damage for the unloaded cell is reduced to approximately 23 % of its prior value, while the stress for the overloaded cells is increased by the factor six. Additionally to the damage, the loss energy is reduced for the unloaded cells to 95 % and increased for the overloaded cells to 104 %. However, it needs to be remarked, that the power variations in the profile are extreme, whereas many applications are expected to undergo power variations with lower magnitude. After all, it can be concluded, that routing the power can reduce the

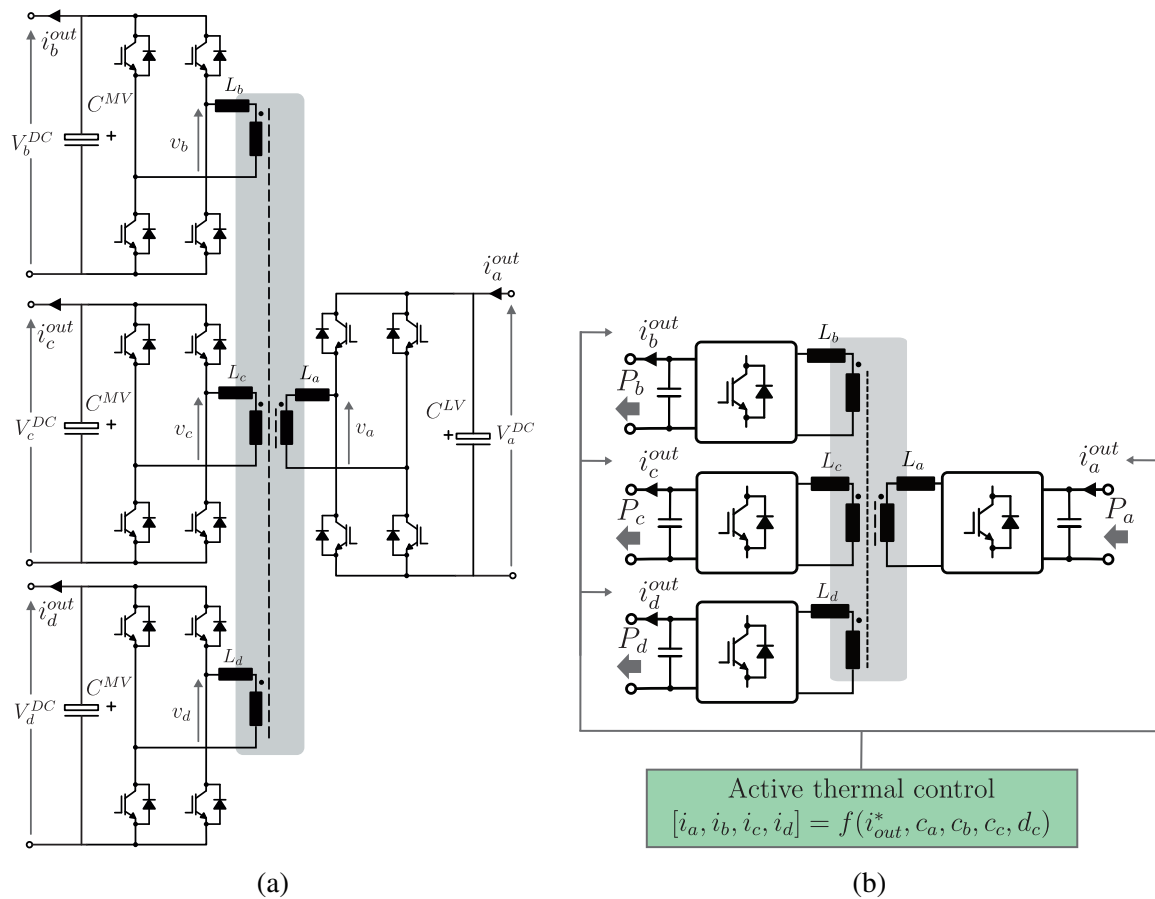


Figure 7.23: Power routing in the isolation stage: (a) Quadruple Active Bridge (QAB) converter, (b) Scheme of the active thermal control algorithm.

thermal stress and therefore increase the lifetime of the unloaded cells in a modular system for the costs of increased power losses.

## 7.4 Power routing for modular isolated DC/DC converters

This subsection proposes a modular isolated DC/DC converter with multiple QABs as building blocks. The design, in combination with a virtual resistor based control, weights the paths depending on the components wear out and can balance the stress of the semiconductors in the attempt of extending the overall system's lifetime. The effectiveness of the approach is demonstrated in simulations and supported with measurements on a small-scale demonstrator with open modules, built in order to verify in real time the capability to control the thermal stress of the semiconductors.

### 7.4.1 System description

A modular DC/DC converter based on multi-port cells that are connected in series and in parallel is introduced, in order to have multiple paths through which the power can be routed. A power sharing technique between the cells is then proposed, with the aim of relieving the

stress from the most deteriorated cells. In fact, whereas modular structures can be made fault tolerant either at system or at cell level [166], the novelty of this approach is that the control tries to delay the time of the failure by shifting the thermal stress to the healthier part of the converter. A simulation showing the long-term effects on a single building block is carried out, and an experimental setup is built to confirm the latter result. The proposed multi-port structure is described, analyzed and simulated at system level, where the interaction between multiple building blocks is shown.

This subsection is focused on a specific modular architecture of a DC/DC converter based on multiple QAB converters (see Fig. 7.23 (a)). Nevertheless, the concept can be extended to an arbitrary number of ports [167]. In addition to the topology, Fig. 7.23 (b) shows the thermal control scheme with the current being the control variable. The indicated four currents of the QAB converter are making the system overdetermined, which is done on purpose to better demonstrate the sharing algorithm in a system of multiple QABs in the following. The DC/DC converter is composed of multiple QABs connected to a LVDC link and to a MVDC link or a CHB converter in the MV side. As an example, the interconnections between the QABs and the CHB is reported in Fig. 7.24. Four QABs are connected with their twelve MV-side ports to a single-phase CHB converter based on six cells. The QABs are connected in such a way, that every converter has a redundant power path in the MV side and one shared MVDC link with one of the other QABs. In the LV side, the four DC-links are connected to obtain two DC-links. The two LVDC-links can be separated or constitute a single DC-link. In the figure, different colors describe different connections to the LVDC links, highlighting the specific connections between the MV and LVDC links. A change in  $V_2^{MV}$  can directly affect  $V_1^{LV}$  (direct connection), whereas a change in  $V_1^{MV}$  will affect both  $V_1^{LV}$  and  $V_2^{LV}$ . This basically means that the power from  $V_2^{MV}$  can be directly routed only to  $V_1^{LV}$ ; in the case power from  $V_2^{MV}$  needs to be routed to  $V_1^{LV}$ , an intermediate step is needed, where the MV ports of the QAB exchange power among themselves. Many degrees of freedom for the connections are present, depending on physical constraints (insulation voltage of the secondary windings) or the degree of imbalance that is expected from the LVDC links, to optimize a specific operating point.

The phase-shift modulation represents the simplest choice and a good solution if wide voltage variations do not happen in normal operating condition. One of the issues of the phase-shift modulation is the reactive power that each port is processing. Therefore, the reactive power can be defined as  $Q = f_{sw} V_a^{DC} \int_{t_1}^{t_2} i_a(t) dt$ , where  $t_1$  is the zero crossing instant of the current at port  $a$ ,  $t_2$  is the switching time of port  $a$  and  $f_{sw}$  is the switching frequency. As it will be shown in the following, this fact is limiting the operation to small phase-shifts, in order to limit the losses. The choice of the modulation and its thorough optimization are, however, not the core of this work and has been investigated in [168, 169].

The QAB schematic is shown in Fig. 7.23. In this figure, the condition  $V_b^{DC} = V_c^{DC} = V_d^{DC}$  is assumed and consequently, for the same phase shifts of  $\phi_{ba} = \phi_{ca} = \phi_{da}$  the QAB behaves similar to a DAB. If the parameters of the cells are similar, there is no power transfer between the MV-side ports. However, by routing the power in the system, the power transfer is not

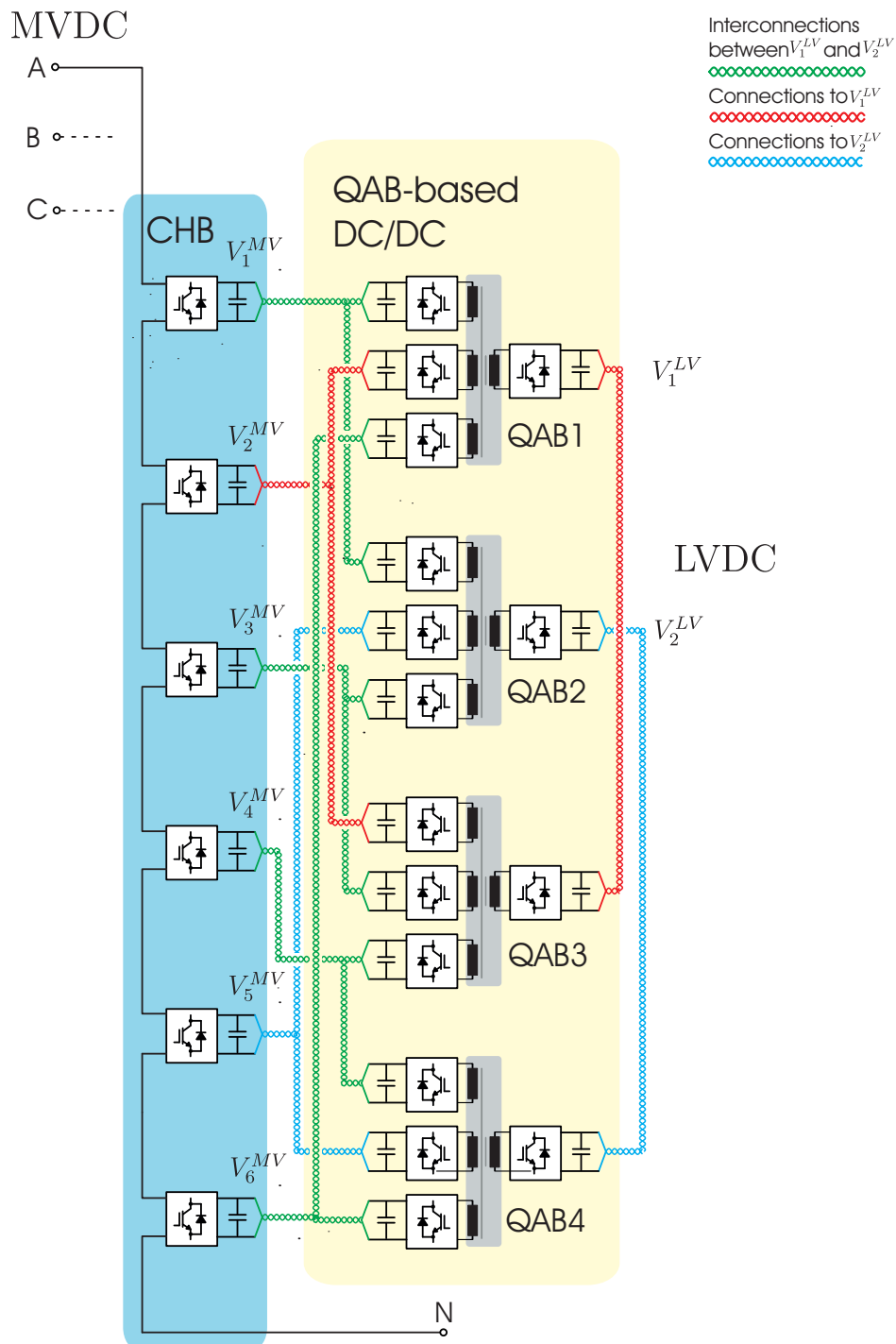


Figure 7.24: Example for an architecture based on the multi-port QAB-based DC/DC converter. The power paths in the DC/DC converter are highlighted depending on the target LVDC link.

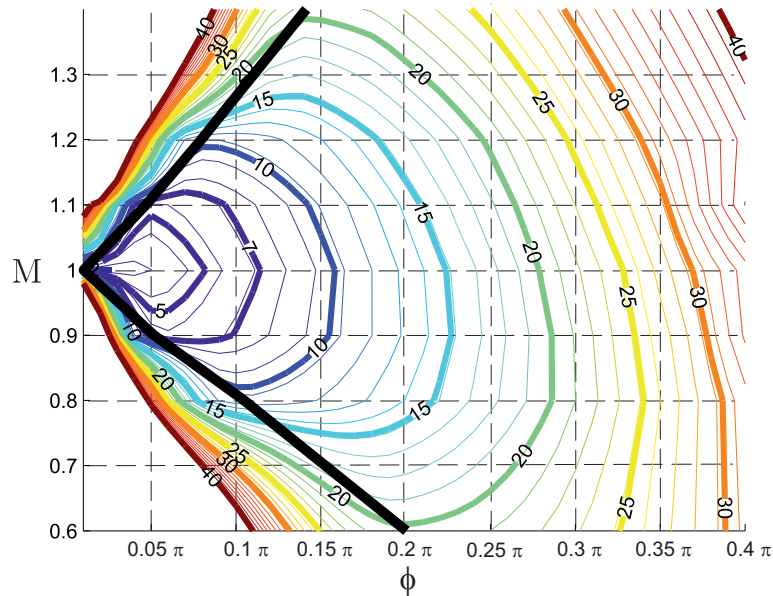


Figure 7.25: ZVS at turn-on range of the QAB for symmetrical power transfer operation. The black line shows the ZVS border and the numbers on the contour lines depict the reactive current in percent of the load current [170].

balanced anymore and the behavior changes. The influence of the unbalanced loading on the soft switching boundaries and the reactive power is demonstrated in the following.

#### 7.4.2 Analysis of the single QAB operation

The ZVS of the DAB is of major importance for the operation with high frequencies for minimizing the losses. In order to achieve ZVS turn-on of the devices, at the switching instant the current must flow in the anti-parallel diode. The soft switching of the QAB can be calculated in a similar fashion to the DAB [168], extending the condition to all bridges. Due to the complexity of the interaction among the different bridges, this was simulated in [170]. Fig. 7.25 depicts the simulation results for the ZVS range of the QAB, for symmetrical power transfer.  $M = V^{MV}/V^{LV}$  is the voltage transfer ratio and  $\phi$  is the phase shift. The contour lines depict the reactive current at port  $a$ , defined above, in percent of the average load current and the thick black line depicts the ZVS border. When the QAB is operated in the area left of the black line, ZVS is lost. As a result, these bridges are hard switched at turn-on. In addition, the reactive current is increasing rapidly when operating in these regions as is can be seen in Fig. 7.25.

Similar to the DAB, ZVS at turn-on is achieved for the full power range of the QAB, if the voltages on the primary side and on the secondary side are equal ( $M = 1$ ). For  $M \neq 1$ , ZVS at turn-on ZVS is lost for light loads (small phase shifts). As a conclusion, the ZVS at turn-on range of the QAB is decreasing with increasing voltage imbalance.

The core proposal is that an unbalanced power transfer can be realized to improve the lifetime of the converter. However, the cost of this procedure in terms of efficiency reduction should be evaluated in order to find the optimal tradeoff between thermal control and efficiency. Fig.



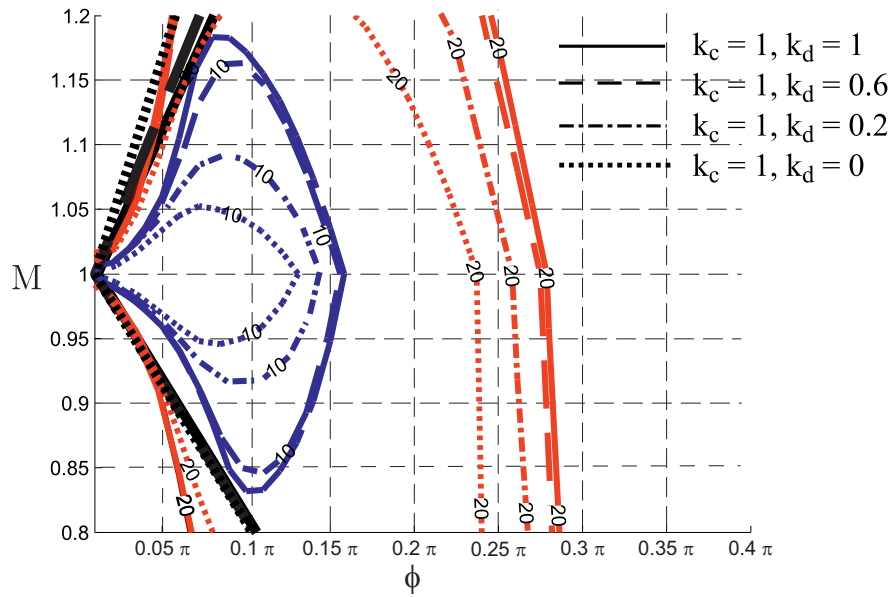


Figure 7.26: Contour plot for different power imbalance conditions introduced to one port. The black lines show the ZVS border and the numbers on the contour lines depict the reactive current in percent of the load current [170].

7.26 depicts how the reactive current and the ZVS border are changing with different power imbalances, defined as  $k_c = P_c/P_b$  and  $k_d = P_d/P_b$ . The power distribution of the secondary side ports is being changed, so that one of the input ports is transferring power while the overall power transfer remains constant. Four power transfer situations are depicted in Fig. 7.26:

- Symmetrical power transfer operation ( $k_c = 1, k_d = 1$ ): Secondary side ports power distribution 33.3% : 33.3% : 33.3%.
- Asymmetrical power transfer operation ( $k_c = 1, k_d = 0.6$ ): Secondary side ports power distribution 38.5% : 38.5% : 23%.
- Asymmetrical power transfer operation ( $k_c = 1, k_d = 0.2$ ): Secondary side ports power distribution 45% : 45% : 10%.
- Asymmetrical power transfer operation ( $k_c = 1, k_d = 0$ ): Secondary side ports power distribution 50% : 50% : 0%.

It can be observed that with increasing power imbalance the contour lines (constant reactive power) are moving to lower phase shifts. Consequently, the reactive power is increased for the unbalanced loading, whereby an increased unbalance increases the reactive currents.

### 7.4.3 Lifetime based control of the converter

In order to enable the power sharing, a droop control based on virtual resistors is implemented [171]. The concept is based on the fact, that the parallel connection of ideal voltage sources is not possible, whereas if they were coupled through an impedance, the modulus

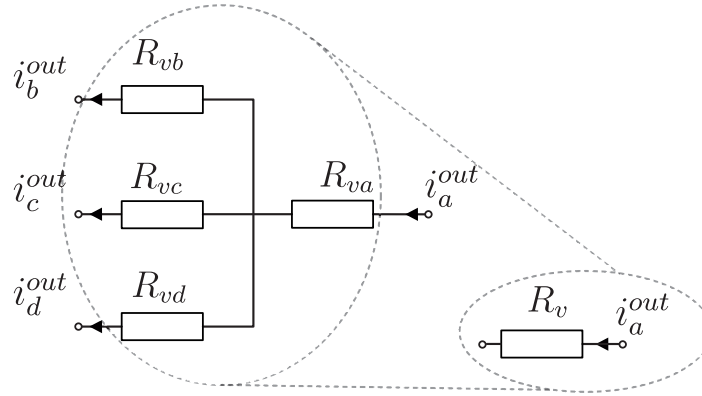


Figure 7.27: Equivalent virtual resistor schematic of the QAB.

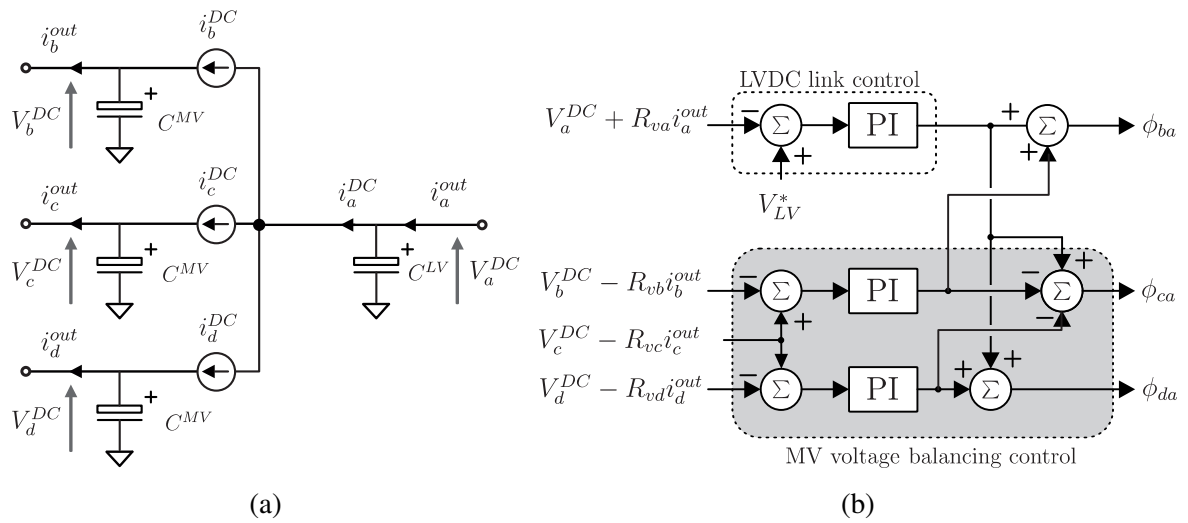


Figure 7.28: QAB Control: (a) Low-frequency model of the QAB, (b) control structure with regulators and virtual resistors.

of this impedance could be used for the power sharing (with the source having the higher output impedance giving less power). Since a physical impedance would add components and unacceptable losses, a resistance is mathematically emulated in the controller, in order to have the same behavior of a resistor connected in series to a voltage source. Consequently, when the current provided by the source increases, the voltage decreases.

The QABs are connected to the LV and MV side, in order to obtain the desired medium voltage level and ensure redundancy. The MV side controls the sum of the MVDC link voltages, while the DC/DC ensures the balance between the CHB DC-links and regulates the LVDC link voltage. Virtual resistors are used in LV and MV sides of the DC/DC converter, as depicted in Fig. 7.27. A low-frequency equivalent circuit of the QAB is reported in Fig. 7.28 (a). Controlled current sources represent the power transfer due to the phase-shift modulation. The virtual resistors  $R_{va}$ ,  $R_{vb}$ ,  $R_{vc}$  and  $R_{vd}$  are introduced only in the control and do not correspond to any physical component in Fig. 7.28 (b). In this work, it is assumed that each cell of the CHB processes the same amount of power (as the most usual application case). By changing the value of the virtual resistors, the power routing will take place, as it was introduced for the parallel converters. For the QABs, each full bridge has a consumed

lifetime  $A \in (0,1)$ .

In the configuration chosen for this work (see Fig. 7.24), two LVDC links are considered and six MVDC links. The repetition of three of these structures allows a complete three-phase MVAC to LVDC converters to be built. In the following, the notation is divided so that the letters  $a, b, c, d$  denote the single QAB ports, with port  $a$  being the LV one (Fig. 7.27), whereas the numbers 1, 2, 3, 4 refer to the QAB.

The total age of QAB1 is represented with (7.11), that can be conceptually described as the series connection between the "age" of the LV port ( $A_{a1}$ ) and the equivalent parallel of the three MV ports ( $A_{b1}, A_{c1}, A_{d1}$ ). It is important to note that  $A_1$  now represents an aggregate lifetime, so a direct relation to the Palmgren-Miner rule is not possible anymore. In fact, the total age is used only for the virtual resistance calculation and not for the lifetime estimation, so its physical meaning is not given anymore.

$$A_1 = \frac{A_{a1}}{2} + \frac{3A_{b1} \cdot A_{c1} \cdot A_{d1}}{2(A_{b1} \cdot A_{c1} + A_{b1} \cdot A_{d1} + A_{c1} \cdot A_{d1})} \quad (7.11)$$

Since in this example QAB1 and QAB3 (as defined in Fig. 7.24) are connected to LVDC1, the power request by this DC-link is shared in an inversely proportional way, see (7.12) and the resulting virtual resistor for QAB1 is expressed in (7.13). The term  $R_0$  constitutes the proportionality between the age and the resistance, and represents a degree of freedom. Thereby, a higher virtual resistance implies a higher steady-state error in the voltage control. The QAB can therefore be represented as an equivalent virtual resistor  $R_v$  (see Fig. 7.27) that is related to the total lifetime of the converter. In fact, if the LV side is aged or the three MV ports are aged, the concept is to increase  $R_v$  for reducing the power transferred by this QAB.

$$\frac{P_1}{P_3} = \frac{A_3}{A_1} \quad (7.12)$$

$$R_{v1} = R_0 \frac{A_1}{A_1 + A_3} \quad (7.13)$$

This first control allows selecting how much power is processed by each QAB through its LV side, whereby a bigger resistance would cause the current to be diverted to other QABs. The virtual resistance of the MV ports of the QAB are proportional to their single lifetime (7.14), this allows re-routing the power in the MV side in the case of a healthy LV module and a deterioration of a single MV cell. The coefficient  $\frac{9}{2}R_{v1}$  is added so that when all the H-bridges of the complete structure have the same age, the QAB presents a resistance  $\frac{R_{v1}}{2}$  in the LV side and three parallel resistances of value  $\frac{3R_{v1}}{2}$  in the MV side. Overall, the total virtual resistance of a QAB seen from the three MV ports in parallel and the LV side resistor is equal to  $R_{v1}$  (as it was shown in Fig. 7.27).

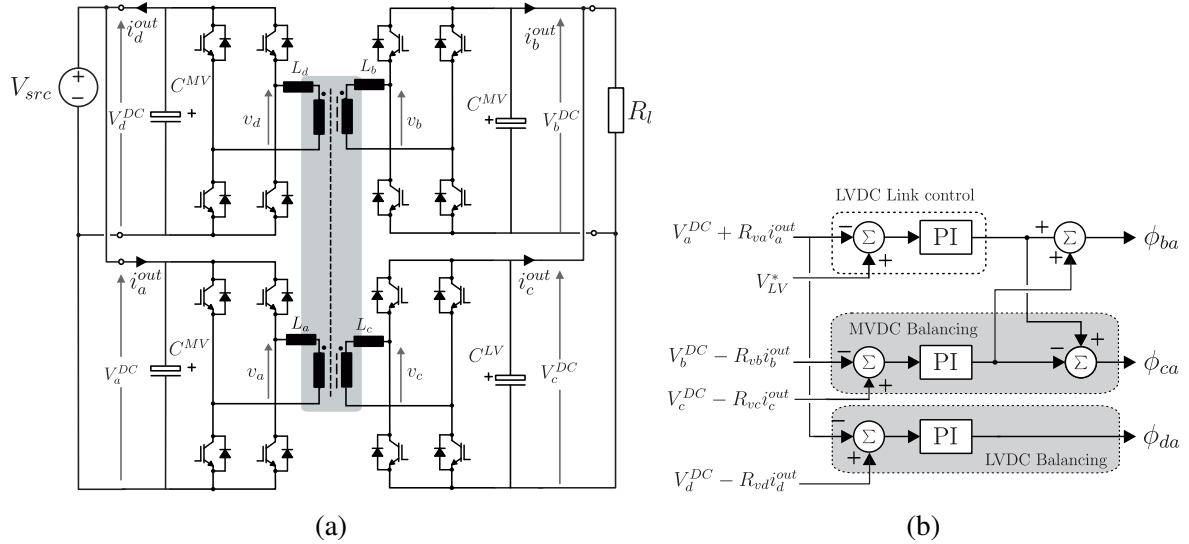


Figure 7.29: Quadruple Active Bridge configuration for the virtual resistance test: (a) circuit connection (b) control.

$$R_{va1} = \frac{R_{v1}}{2}$$

$$R_{vb1} = \frac{9}{2}R_{v1} \frac{A_{b1}}{A_{b1} + A_{c1} + A_{d1}} \quad (7.14)$$

It is worth noting that the imbalance happens only in the DC/DC converter system, and the power processed by the cells of the output ports is equally shared. If the AC cells were to process different powers, since they are series connected, different output voltages would result for each cell. However, the possibility to increase the output voltage is limited by the DC-link voltage. For this reason, in order not to modify the principle of operation of the CHB converter, it is assumed that all output ports, and the MVDC link therefore, process the same amount of power. It is true that the maximum power limits of a DC path could be reached, preventing this condition to be fulfilled. In this case, the power routing control would limit the power of every paths to its nominal power, because higher priority is given to supplying the load. The unrestricted power routing is to be applied only in partial load condition.

#### 7.4.4 Demonstration of the lifetime based power routing

To demonstrate the effect of the power routing on the lifetime, a system consisting of a single QAB is chosen as shown in Fig. 7.29 (a) with the QAB parameters as in table 7.2. This system is simulated in the following with MATLAB/Simulink and the PLECS toolbox. The values of the virtual resistors are variable, because they are used to route the power in the system. As a difference to the case studied before, this QAB has two parallel connected ports on the primary and two parallel ports on the secondary side. This requires changing the

Table 7.2: Simulation parameters.

$f_{sw}$	40 kHz	$R$	$6.6 \Omega$
$T_s$	$1e-4$ s	$L_{lk}$	0.035 mH
$C^{LV}$	0.33 mF	$C^{MV}$	0.33 mF
$K_I^{LV}$	0.2029	$K_P^{LV}$	0.0014
$K_I^{MV}$	0.2029	$K_P^{MV}$	0.0014
$K_I^{CHB}$	673	$K_P^{CHB}$	1.19
$V_x^*$	400 V	$V_{avg}^{MV*}$	2400 V

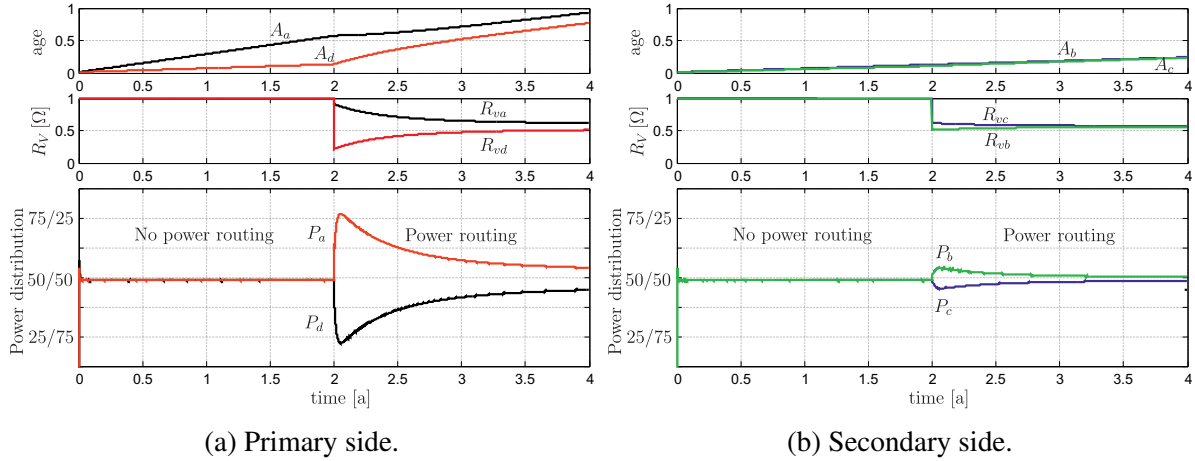


Figure 7.30: Simulation: Power routing in one QAB with 2 primary and 2 secondary ports.

control diagram of the QAB as presented in Fig. 7.29 (b). A regulator outputs the phase shift between the primary and the secondary sides, whereas the virtual resistors allow controlling the power distribution of the overall power in the parallel ports. The resulting power flow paths are two redundant paths on the primary and two redundant paths on the secondary side.

For this system, the long time effect of the power routing is demonstrated. As pointed out before, different lifetime consumption is assumed for the different power converter cells. Moreover, in this case the long time increase of the age in all cells is assumed to be different, whereby the aging of cell a is happening faster than that of cell d. On the secondary side, the aging of the cell c is slower than the aging of cell b. For demonstration, the lifetime is modeled by setting the age  $A_a$ ,  $A_b$ ,  $A_c$ , and  $A_d$  proportional to the integral of the losses of the power semiconductors. From this age the virtual resistors are derived, whereby the cells on the primary and secondary side are modeled as parallel resistors as exemplary shown in (7.15) for the virtual resistance of cell a.

$$R_{va} = \frac{A_a}{A_a + A_d} \quad (7.15)$$

The power routing for the primary side is shown in Fig. 7.30 (a) and the aging of the secondary side in Fig. 7.30 (b). For the first two years, this is presented without the power

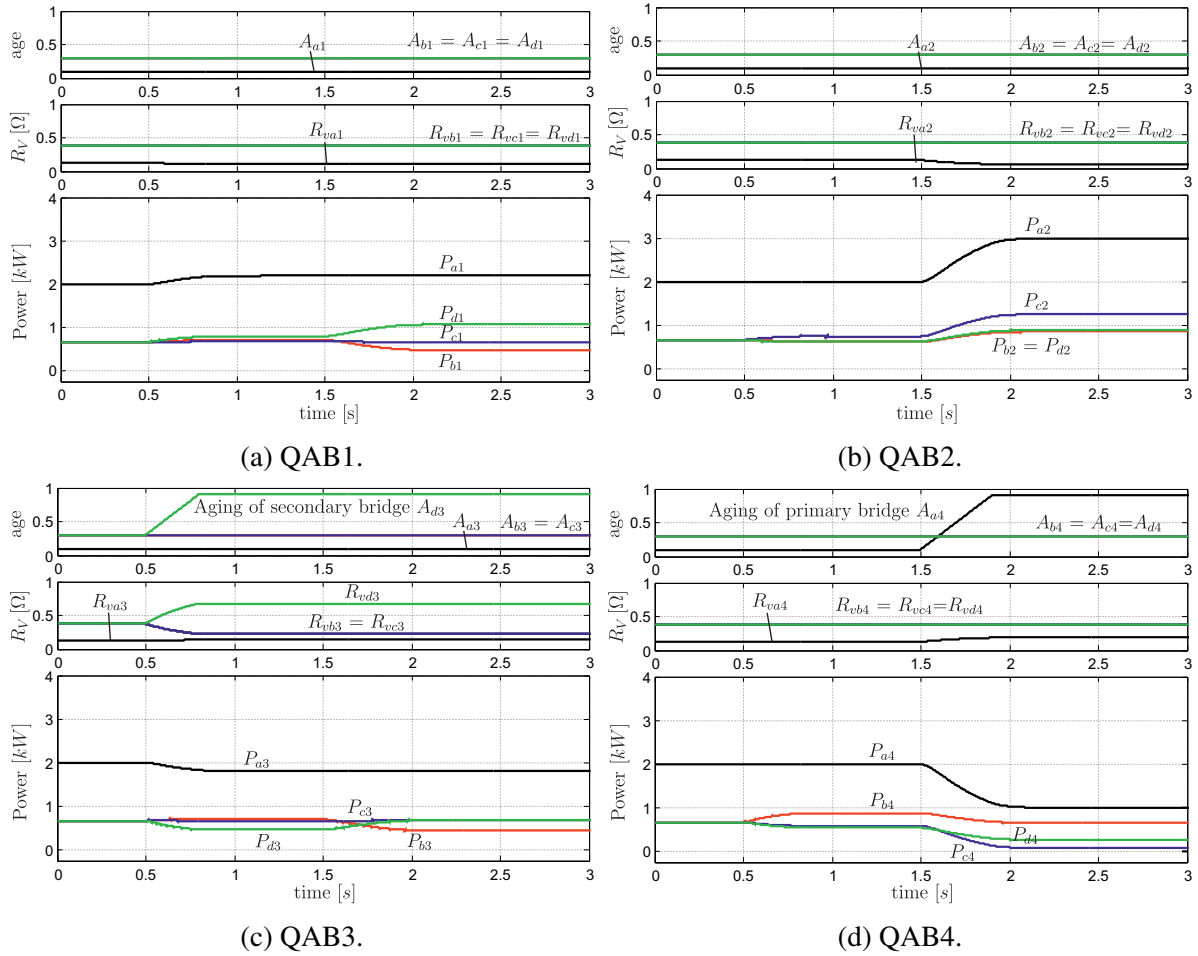


Figure 7.31: Simulation: Power routing by the converter assuming change of the component’s lifetime. Constant power case.

routing, showing that on both sides one cell is going faster towards its end of life than the other one. By activating the power routing, the aging of the cell with higher wear out is slowing down, while the aging of the other cell is accelerating. Affected by the activation of the power routing, the virtual resistors change and then converge to each other as expected for decreasing difference in the age. The power of the most aged cell is reduced as intended.

In the following, the power routing is extended for a multiple QAB structure as shown in Fig. 7.24. Each DC-link reference voltage in the system is set to 400V, the switching frequency is 40kHz with phase-shift modulation and the DC capacitors are 330μF. The transformers have unity turn ratio. The age of the modules is assumed to be different in the modular structure for different possible reasons, like thermal imbalances, parameter tolerances, or because of the choice of a repairable system, where all cells have different age, like explained in section 7.1.

First, a variation in the aging indicator of a secondary side bridge ( $A_{d3}$ ) and the primary bridge  $A_{a4}$  is demonstrated in Fig. 7.31. In particular, for each QAB the lifetime parameters (age and virtual resistance) are reported as well as the power processed by each QAB port. Initially, all primary and secondary bridges have the same aging indicator, and constant power of 2kW is processed by each QAB. All bridges are processing the same power, until

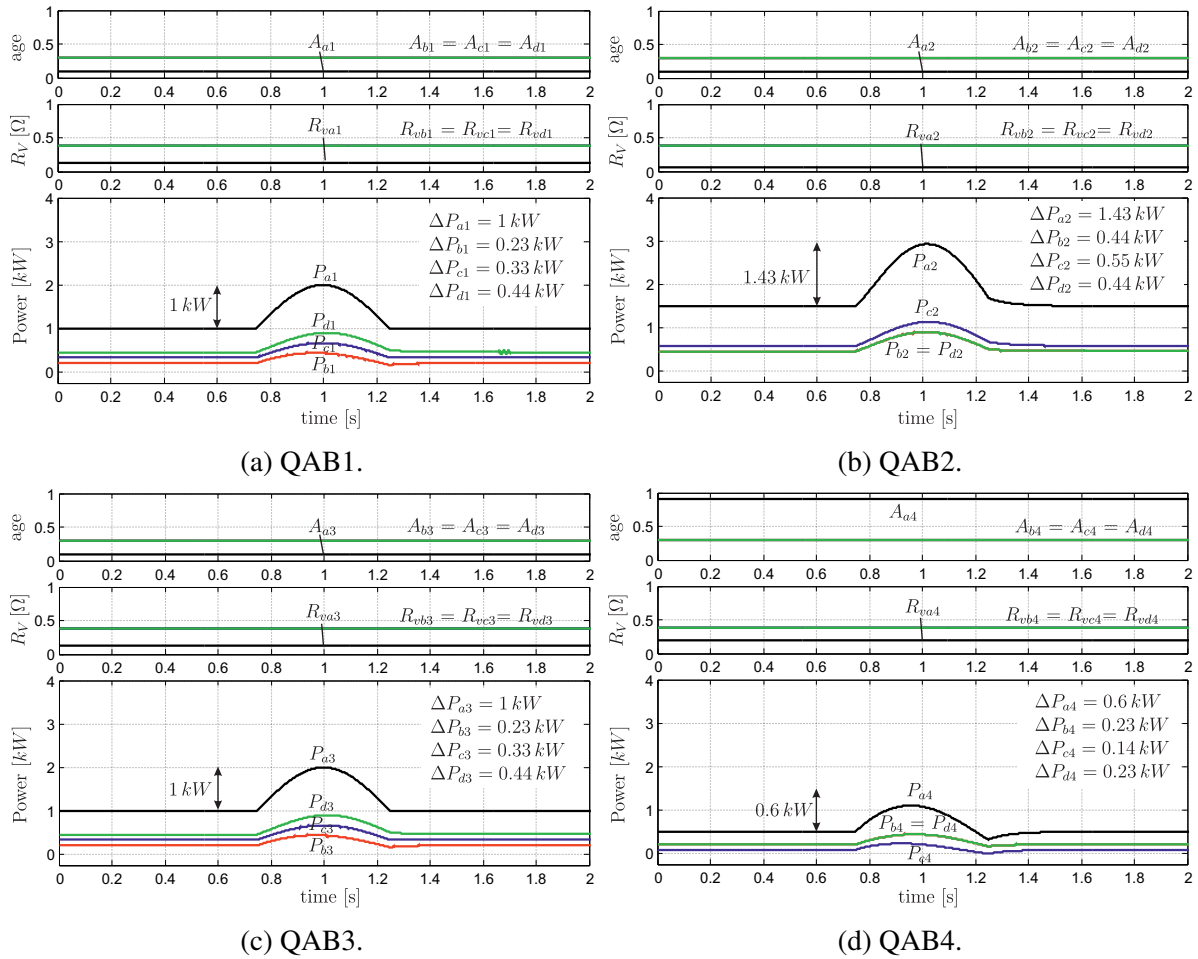


Figure 7.32: Simulation: Power routing by the converter assuming change of the component lifetime. Power cycle case.

at  $t = 0.5 s$  the aging indicator of one secondary bridge in QAB 3 is increased. This results in an increase of the virtual resistor and the power for the according cell is reduced. Due to the modular interconnection of the cells, the power  $P_{b4}$  in QAB 4 is increased. At  $t = 1.5 s$ , the primary aging indicator  $A_{a4}$  of QAB 4 is increasing and further unbalances the power transfer. As a result, the power in all bridges of QAB 4 is decreased, while the parallel structure of QAB 2 has to process higher power.

The second simulation in Fig. 7.32 is showing the influence of the virtual resistances on a power cycle. It is assumed, that all secondary bridges have equal aging indicator. Instead, on the primary side the aging indicator of QAB1, QAB2 and QAB3 is assumed to be equal  $A_1 = A_2 = A_3$ , whereas QAB 4 shows a higher aging indicator  $A_4 > A_1$ . The power is already unequally shared during constant power operation and a sinusoidal half wave shaped power cycle of  $\Delta P = 4 kW$  is applied to show the power sharing among the QABs. Similar to the constant power operation, the power cycle is unequally shared, resulting in different magnitudes of the power cycle for the QABs, which are quantified in Fig. 7.32. Particularly, the load in all bridges of QAB4 is significantly reduced, while the power cycle in QAB 2 is increased in all bridges. The power cycle in the primary bridge of QAB2 is approximately 2.4 times higher than the power cycle in the primary bridge of QAB 4. The power in the

LV-side ports of QAB 1 and QAB 3 remains unaffected because of their connection to the different DC-links. However, in both QABs the port  $d$  is loaded higher because of their interconnection with ports from QAB 2 and QAB 4.

The aim of these simulations is to prove that the power can be routed depending on an indicator of the consumed lifetime of the basic cells, leading to different power cycles within the system. Similar to the reduction of power cycles, the cycles of the power semiconductor's junction temperatures, which are causing wear out, can be controlled. If the age increases, the control reduces the stress on those semiconductors, and the distributed droop control keeps the correct DC-link voltages across the whole converter to delay the time of the next maintenance.

#### 7.4.5 Experimental validation of the algorithm

A prototype of the QAB for reliability investigation was built based on a 25A IGBT open module. This kind of module is not typically used for DC/DC converters. However, it was provided by the manufacturer without gel, which allows tracking directly the temperature variations. Due to the absence of the gel, the prototype has to be operated at lower voltage due to insulation issues. The goal of the test bed is to prove, in simplified conditions, that a control based on variable virtual resistance can affect the thermal distribution inside the power module. Figure 7.29 (a) shows the configuration of the experimental setup, where port  $a$  and  $d$  are connected in parallel to a power supply at  $V_{src} = 200V$  and port  $b$  and  $c$  to a load resistor of  $R_l = 25\Omega$ . The other parameters are the same as in the simulations.

To prove the thermal stress variation, the low load condition is emulated by increasing the virtual resistance of the module under test to twice its value (initially  $10\Omega$ ) and the high load condition is emulated by increasing the virtual resistance of the other module in parallel.

An IR camera was used to monitor the chip temperature of the open module (that implements an H-bridge cell) used for the tests, and the temperature was measured in steady state after 5 minutes. Fig. 7.34 (a) shows the measured temperature and Fig. 7.33 (a) shows the actual waveform of the converter. In the same fashion, equal load and high load are shown in Fig. 7.34 (b), 7.33 (b) and Fig. 7.34 (c), 7.33 (c).

This virtual resistance variation can be performed dynamically, as shown in Fig. 7.33 (d), where the resistance of module  $c$  performs a square wave between  $10\Omega$  and  $20\Omega$  with a period of 1 s. The output current is shared proportionally. Such fast variations of the virtual resistors only represent a proof-of-concept of the proposed method, whereas it is expected that the variations are much slower in operating conditions due to their correlation with the aging.



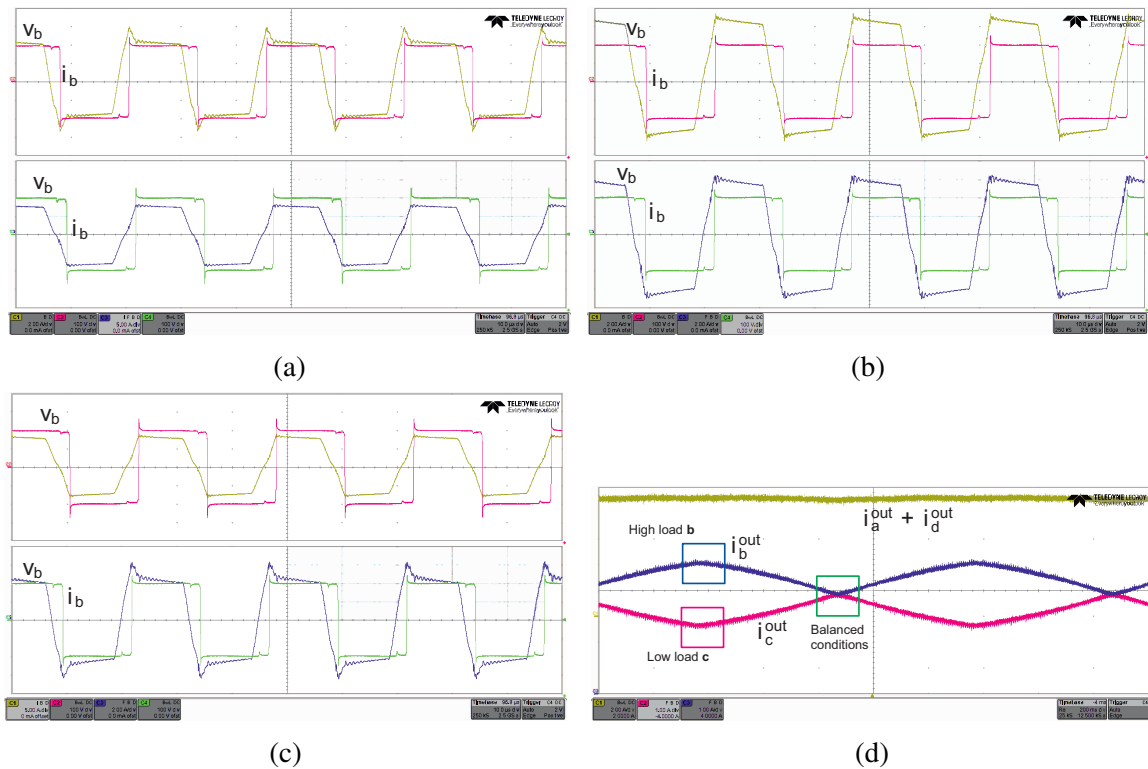
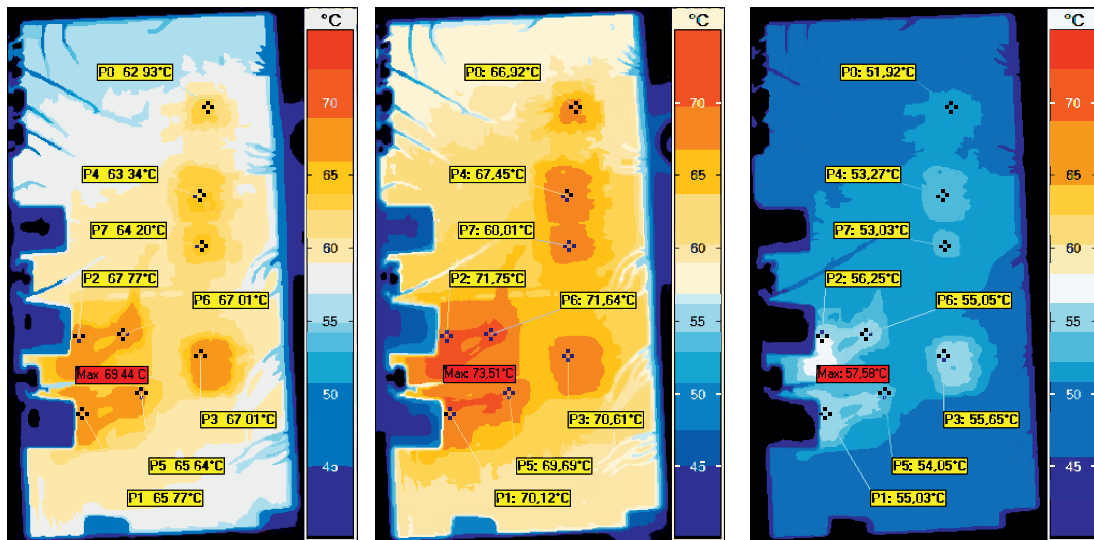


Figure 7.33: Measurement: Power routing by the converter assuming different component lifetime. (a) reduced load for recorded full bridge, (b) equal load sharing for the full bridges, (c) increased load for the recorded full bridge and (d) Variation of the virtual resistors for a variation in the power routing.

## 7.5 Short summary of the section

This section has introduced the concept of power routing for modular power converters consisting of series, parallel and multi-winding transformer coupled building blocks. The concept was introduced along with its limitations in the power routing capability. Furthermore, the capability of different converters is investigated before three case studies were carried out for each of the mentioned power routing concepts. The series connected power routing was demonstrated for a CHB-converter as shown in Fig. 7.35 (a). The loading of the converter cells is controlled to alter the power processed in the different paths and the multi-frequency power routing using third harmonic has been proposed to improve the unbalanced power sharing between the cells by up to 15.5% per higher loaded cell in comparison to the conventional method. The power routing for parallel building blocks has been demonstrated for the three parallel converters as shown in Fig. 7.35 (b). It is experimentally proven, that the stress distribution between the parallel parts can be controlled, consequent the wear out of the components. As a price to pay for this increased reliability, the efficiency is slightly reduced for unequally loaded converters. These findings are fully validated with a special set-up, which allows directly assessing the power semiconductor's junction temperature. A modular DC/DC converter for medium voltage application based on QABs as building blocks have been introduced for the power routing. The algorithm is based on a virtual resistor voltage control, where the virtual resistor is related to the accumulated damage of the power con-



(a) Reduced load for the recorded full bridge. (b) Equal load sharing for the full bridges. (c) Increased load for the recorded full bridge.

Figure 7.34: Power routing for assuming different component lifetimes: Thermal images of the used open IGBT module under load sharing.

verter cells. The obtained capability to re-route the power internally is proposed to be used to balance the consumed lifetimes of the different basic cells. A QAB prototype as shown in Fig. 7.36 was built to allow monitoring the junction temperature with a IR camera, proving that the virtual resistor voltage control can dynamically affect the thermal stress of the power modules.

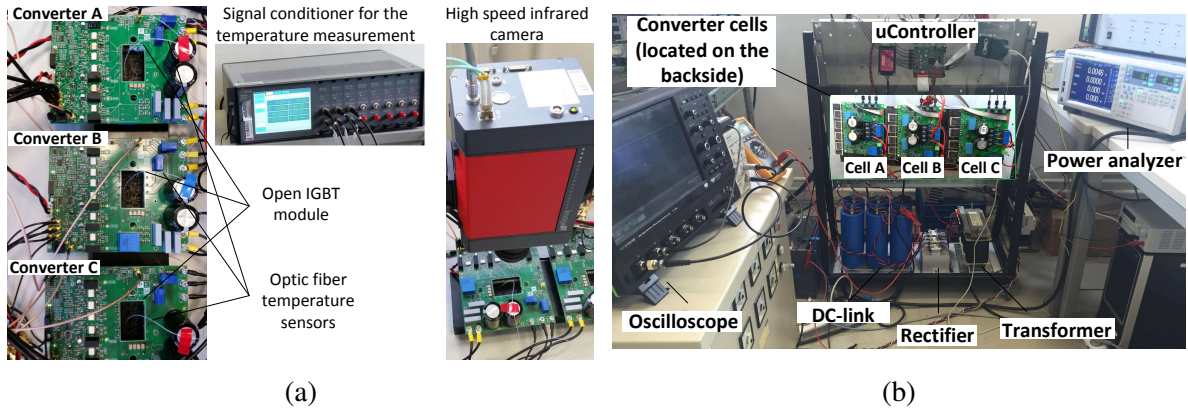


Figure 7.35: (a) Picture of the laboratory setup showing the seven-level CHB converter, (b) Picture of the setup showing the three parallel converters assembled on one heat sink, a signal conditioner for the fiber optic temperature sensors and high speed infrared camera for junction temperature measurement of a full power electronic module.

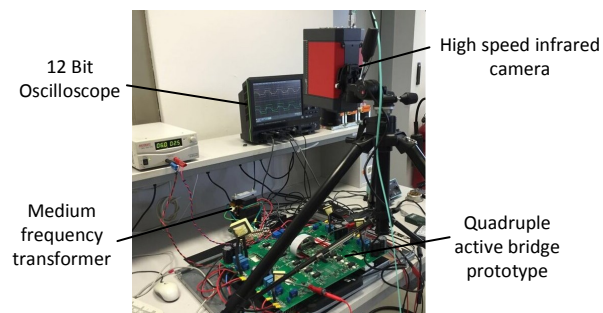


Figure 7.36: Picture of the laboratory setup with a QAB prototype and a high-speed infrared camera for junction temperature measurement in one open IGBT module.

## 8 Summary, conclusion and future research

### 8.1 Summary and conclusion

The ST has been proposed to solve problems of highly dynamic varying power injection from renewable energy sources, such as wind and photovoltaic power plants [33]. With its control and communication capability, it can provide new grid services, which the traditional transformer cannot provide. However, one of the challenges for the application of the ST is its expected lower reliability in comparison with the traditional transformer. This work combines the knowledge about the power system, power electronics and reliability in power electronics for an investigation about the thermal stress of power semiconductors. Furthermore, algorithms are developed to increase the reliability of the ST by means of active thermal control.

This thesis has reviewed possible ST architectures and a three-stage architecture with either one or two DC-links has been found to be most suitable. The advantage of these topologies is their capability to interface AC and DC grids and decouple the MV and LV grids to a certain extent. It is proposed to design a modular ST and for each stage potential power converter topologies have been reviewed and evaluated for their advantages and disadvantages. A three-stage ST consisting of the MMC in the MV stage, QABs in the isolation stage and two level VSC in the LV stage has been designed with a power rating of 1 MW. For the design of the maximum junction temperature, the tradeoff between reliability on the one side and volume and costs for the cooling system on the other side has been addressed and a hyperbolic dependence is demonstrated.

To cope with the expected lower reliability of the ST in comparison with the traditional transformer, the physics of failure approach has been motivated [68]. The most frequently failing components have been reviewed in section 3 and the power semiconductors have been found to be the most fragile ones in the system. Based on the physics of failure principle, the failure mechanism and lifetime models for power semiconductors have been described.

In order to enable the use of the power cycling data from manufacturers for the thermal stress evaluation of power semiconductors in the operating conditions of the ST, a mission profile is developed in section 4. Based on this mission profile, thermal stress analysis is made for all three stages of the ST. This analysis combines the thermal stress, which was affected in different periodicity to form realistic operation conditions. In addition to the occurring power variations, a grid fault has been taken into account. In the medium voltage stage, the thermal stress was analyzed for an MMC converter, in the low voltage stage for a two level VSC and in the isolation stage for a QAB converter. It has been demonstrated, that the thermal stress is least for the isolation stage, whereby most of the damage for the power converters is affected during the high load phase. To optimize the thermal design, a de-rating algorithm has been proposed for the optimization of the thermal design based on the mission profile and an acceleration factor, commonly used in accelerated lifetime tests. For the investigated failure mechanism, it is possible to de-rate the junction temperature design under the investigated

conditions and a lifetime target of 20 years to  $109^{\circ}\text{C}$  in the MMC,  $133^{\circ}\text{C}$  for the QAB and  $104^{\circ}\text{C}$  for the two level VSC. The potential increase of the junction temperature enables a reduction of the heat sink volume to less than 23% of its prior size, which also corresponds to reduced costs.

In section 5, active thermal control was introduced to improve the reliability of the power semiconductors [112]. The existing algorithms from literature were systematically categorized in control of the losses and control of the system loading. To obtain a junction temperature estimation, a computational light estimator is designed and it is demonstrated, that a second order approximation of the thermal impedance between junction to case and a case temperature measurement is sufficient to model the junction temperature fluctuations for the tested devices.

As a test case to demonstrate the potential of active thermal control by control of the system loading, a thermal stress reduced maximum power point tracking algorithm was developed and validated to reduce the thermal stress during fast changing irradiance in section 5.3. With a limitation of the junction temperature gradient, the thermal stress was reduced under an investigated profile for the cost of reduced energy harvested from the PV panels. As an example, the lifetime was increased by 31% of its prior value for a reduction in harvested energy by 8%.

For the application in the ST, two algorithms, which are controlling the power semiconductor's losses were developed in section 6, whereby one is applicable for hard switching power converters and the other one is applicable for soft switching power converters. These algorithms were proposed to maximize the lifetime and the reliability of the ST. The first algorithm controls the switching frequency and thus is applicable for the AC stages of the ST. The second algorithm is proposed for the application in isolated soft switching power converters and changes the duty cycle during the commonly used phase shift modulation. Both described algorithms do not require a junction temperature measurement and rely on the detection of power variations. The effectiveness of these two algorithms has been validated experimentally. For the switching frequency control, the algorithm was demonstrated to increase the lifetime by 39% for a reduction of the efficiency by 1.1%

After a certain time in operation, it is expected, that some components in a modular power converter approach the end of their life, while others still have a long remaining useful lifetime. To overcome the problem of potentially unpredicted failures a repairable system has been proposed. Furthermore, it has been proposed in section 7 to utilize the age of all components by controlling the lifetime of the components in different building blocks in modular power converters. This algorithm is referred to as power routing and the concept was introduced for series and parallel connected building blocks along with an investigation about the limitation. Power routing was demonstrated in case studies for one topology in series connected and parallel connected building blocks. In the MV stage, power routing was demonstrated for the CHB converter and multiple frequencies were proposed to increase the maximum power routing capability by up to 15% of the fundamental frequency per higher loaded cell. In the LV stage, a control strategy based on virtual resistors is introduced and

demonstrated experimentally for three parallel power converters by demonstrating, that the thermal stress can be controlled. For both algorithms, case studies demonstrate the capability to unload parts of the system for the expense of loading other parts higher. In addition, an algorithm for isolated DC/DC converters is demonstrated to have the capability to route the power and thereby control the thermal stress.

## 8.2 Research contribution

### Contribution for the reliability analysis of the ST

- A mission profile for the ST in the distribution system was developed, where thermal stress from different periodicity was superposed to obtain realistic operating conditions
- Thermal stress analysis was made for all three stages of the ST under the proposed mission profile
- An algorithm was proposed for the thermal de-rating to achieve a maximum utilization of the power semiconductors for a mission profile and a specified lifetime target

### Contributions in the field of active thermal control

- A comprehensive review about active thermal control with categorization in control of the power losses and control of the system loading was made
- A junction temperature estimator was designed and experimentally validated to achieve good precision and to obtain fast dynamic response

### Contributions in the field of active thermal control by control of the power losses

- For hard switching power semiconductors, an active thermal control algorithm using the switching frequency as control variable without junction temperature measurement was developed and validated
- For soft switching power semiconductors, an active thermal control algorithm controlling the duty cycle of the phase shift modulation without junction temperature measurement was developed and validated
- The tradeoff between efficiency and reduction of thermal stress was analyzed

### Contributions in the field of active thermal control by control of the system loading

- A thermal stress reduced MPPT algorithm was developed for PV applications
- Tools and methodologies for reliability research were demonstrated for the thermal stress reduced MPPT algorithm
- The tradeoff between efficiency and reduced thermal stress was analyzed for the proposed algorithm
- Active thermal control by means of power routing has been introduced for modular power converters for controlling the stress of different building blocks in the system

- The power routing capability of different series- and parallel connected building blocks has been investigated
- A power routing algorithm using multiple frequencies (fundamental and third harmonic) has been introduced and validated for a CHB converter
- A power routing algorithm based on virtual resistors has been introduced and validated for parallel power converters
- A power routing algorithm based on virtual resistors for a modular isolated multi-pole DC/DC converter has been introduced and validated

### 8.3 Future research

For ensuring a high quality of service, the availability of the system is of major importance. This also applies for the ST after applying the thermal design optimization, which has been introduced based on a mission profile. Consequently, the validation of the reliability for this design optimization is mandatory and needs to be tested in a real converter system. Furthermore, it needs to be evaluated how the system performs in overload conditions, which can occur and which may even be required by the regulations of the grid operator.

The validation of the claimed lifetime extension by the proposed active thermal control algorithms is another possible future research topic. Even if the first algorithms were proposed almost 20 years ago, an experimental proof has not been published yet. For this purpose, it is suggested to implement and test the proposed algorithms on a full-scale prototype and to apply accelerated lifetime tests for multiple converter systems with and without active thermal control. In addition to the validation, the results improve the knowledge about the metrics between costs, power density (volume) and reliability in the context of active thermal control. This knowledge provides insights about the potential of active thermal control in other applications.

The tuning of active thermal control algorithms is another potential research topic. Particularly, the nature of unknown mission profiles in many applications is challenging the performance of the algorithms, potentially excessively increasing the losses. In the application of the ST, a forecast of the loads and the generation can be used to tune the algorithms. Other possibilities are the tuning based on measured data in an existing application or self-tuning algorithms based on the detected thermal cycles in the the past.

As pointed out, to the current state, there is no inexpensive junction temperature sensing, which provides the junction temperature in high bandwidth and without sensitivity to parameter variations in the thermal system. The information about the junction temperature is required for active thermal control and should not increase the hardware costs significantly to ensure that cost savings gained by the application of active thermal control are not compensated. In this field, the development of new temperature sensing methods are a possible open research field.

For active thermal control by means of power routing, several future research opportunities exist. One is to evaluate the potential lifetime extension by taking into account not only the power dependent failure mechanisms, but also the other failures, e.g. affected by cosmic rays. A quantification of power dependent failures and failure mechanisms, which are not affected by the power transfer, can be carried out for this purpose. Based on this study, it is possible to derive failure probabilities for different lifetimes, like it is done for the  $B_x$  lifetime. In addition, suitable tuning procedures for controlling the lifetime of the power semiconductors by power routing can be optimized for the different topologies and the overall system.

This work has introduced control algorithms for controlling the lifetime of the power semiconductors. However, there are other components in the converter, which can fail. These components include capacitors, fuses, PCBs, sensors and inductors. To ensure, that the



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lifetime of the system is increased, it needs to be ensured, that not only the power semiconductors are kept operational, but also all other components. This can be addressed with the development of proper lifetime models for all components, which need to be included in a comprehensive approach.

Condition monitoring for power semiconductors and also for the other components offers further potential for improvements. Despite several parameters, which have been proposed to be monitored for power semiconductors, the time of the actual failure occurs with a high standard deviation. In addition to this, a better understanding of the failure mechanisms should be used to further develop and improve the lifetime models of power semiconductors. This can be utilized to improve the prediction of the time to the next failure and to route the power in the system accordingly.

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## 10 Attachment

### 10.1 Publications related to this thesis

- J1 M. Andresen, M. Liserre. "Impact of active thermal management on power electronics design." *Microelectronics Reliability* 54.9 (2014): 1935-1939.
- J2 M. Andresen, G. Buticchi, and M. Liserre. "Study of reliability-efficiency tradeoff of active thermal control for power electronic systems." *Microelectronics Reliability* 58 (2016): 119-125.
- J3 M. Andresen, G. Buticchi and M. Liserre, "Thermal Stress Analysis and MPPT Optimization of Photovoltaic Systems," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4889-4898, Aug. 2016.
- J4 M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa and Z. X. Zou, "The Smart Transformer: Impact on the Electric Grid and Technology Challenges," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46-58, Summer 2016.
- J5 M. Liserre, M. Andresen, L.F. Costa, G. Buticchi "Power Routing in Modular Smart Transformers: Active Thermal Control Through Uneven Loading of Cells," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43-53, Autumn 2016.
- J6 M. Andresen, K. Ma, G. De Carne, G. Buticchi, F. Blaabjerg, and M. Liserre, "Thermal Stress Analysis of Medium Voltage Converters for Smart Transformers," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4753-4765, June 2017.
- J7 G. Buticchi, M. Andresen, M. Wutti, M. Liserre, "Lifetime Based Power Routing of a Quadruple Active Bridge DC/DC Converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8892-8903, March 2017.
- J8 Y. Ko, M. Andresen, G. Buticchi, M. Liserre, "Power Routing for Cascaded H-Bridge Converters," *IEEE Transactions on Power Electronics*, in press.
- J9 M. Andresen, K. Ma, J. Falck, G. Buticchi, F. Blaabjerg, M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Transactions on Power Electronics*, in press.
- J10 F. Hahn, M. Andresen, G. Buticchi and Marco Liserre, "Thermal Analysis and Balancing for Modular Multilevel Converters in HVDC Applications," *IEEE Transactions on Power Electronics*, in press.
- K1 M. Andresen, M. Liserre and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," *Power Electronics and Applications (EPE'14-ECCE Europe)*, 2014 16th European Conference on, Lappeenranta, 2014, pp. 1-10.

- K2 M. Andresen, G. Buticchi, J. Falck, M. Liserre and O. Muehlfeld, "Active thermal management for a single-phase H-Bridge inverter employing switching frequency control," PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of, Nuremberg, Germany, 2015, pp. 1-8.
- K3 G. Buticchi, M. Andresen, L. Costa and M. Liserre, "Modular DC/DC converter structure with multiple power flow paths for smart transformer applications," Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on, Geneva, 2015, pp. 1-9.
- K4 K. Ma, N. He, F. Blaabjerg, M. Andresen and M. Liserre, "Frequency-domain thermal modelling of power semiconductor devices," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 2124-2131.
- K5 M. Andresen, K. Ma, M. Liserre and F. Blaabjerg, "Thermal stress comparison in modular power converter topologies for smart transformers in the electrical distribution system," Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on, Geneva, 2015, pp. 1-10.
- K6 M. Andresen, G. Buticchi and M. Liserre, "Thermal stress reduced maximum power point tracking for two stages photovoltaic converters," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 2116-2123.
- K7 J. Falck, M. Andresen and M. Liserre, "Active thermal control of IGBT power electronic converters," Industrial Electronics Society, IECON 2015 - 41st Annual Conference of the IEEE, Yokohama, 2015, pp. 1-6.
- K8 M. Andresen, L. F. Costa, G. Buticchi and M. Liserre, "Smart Transformer reliability and efficiency through modularity," 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, 2016, pp. 3241-3248.
- K9 M. Andresen, M. Schloh, G. Buticchi, and M. Liserre, "Computational light junction temperature for active thermal control," 2015 IEEE Energy Conversion Congress and Exposition (ECCE) Milwaukee, 2016.
- K10 Y. Ko, M. Andresen, G. Buticchi, L. Concari, and M. Liserre, "Multi-frequency power routing for cascaded H-Bridge Inverters in Smart Transformer Application," 2015 IEEE Energy Conversion Congress and Exposition (ECCE) Milwaukee, 2016.
- K11 J. Falck, M. Andresen, and M. Liserre, "Thermal-based Finite Control Set Model Predictive Control for IGBT Power Electronic Converters," 2015 IEEE Energy Conversion Congress and Exposition (ECCE) Milwaukee, 2016.
- K12 M. Andresen, G. Buticchi, and M. Liserre, "Active thermal control for isolated DC/DC converter," Industrial Electronics Society, IECON 2016-42st Annual Conference of the IEEE. IEEE, 2016.

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- K13 Y. Ko, M. Andresen, G. Buticchi, J.S. Lee, M. Liserre, "Modulation Strategy for Highly Reliable Cascade H-Bridge Inverter Based on Discontinuous PWM," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017.

## 10.2 Curriculum Vitae

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Abitur, Friedrich Paulsen Schule, Niebüll, 2007

Course of study:

2007 - 2011: Industrial Engineering at the Christian-Albrechts-Universität zu Kiel (Bachelor of Science)

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