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On the development of memristive devices for electroforming-free and analog memristive crossbar arrays

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Eidesstattliche Erklärung

Hiermit erkläre ich:

Diese Dissertation mit dem Titel "**On the development of memristive devices for electroforming-free and analog crossbar arrays**" habe ich noch nie, weder ganz noch teilweise im Rahmen eines anderen Promotionsverfahrens vorgelegt oder veröffentlicht. Ich habe mich bislang noch keiner mündlichen Prüfung im Rahmen eines Promotionsverfahrens unterzogen. Die vorliegende Arbeit habe ich ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt; die aus fremden Quellen direkt oder indirekt übernommenen Gedanken sind als solche kenntlich gemacht. Die Arbeit ist unter Einhaltung der Regeln guter wissenschaftlicher Praxis der Deutschen Forschungsgemeinschaft entstanden. Bei der Auswahl und Auswertung des Materials sowie bei der Herstellung des Manuskripts habe ich nur Unterstützungsleistungen meines Betreuers erhalten. Weitere Personen waren an der geistigen Herstellung der vorliegenden Arbeit nicht beteiligt. Insbesondere habe ich nicht die Hilfe eines Promotionsberaters in Anspruch genommen. Dritte haben von mir weder unmittelbar noch mittelbar geldwerte Leistungen für Arbeiten erhalten, die im Zusammenhang mit dem Inhalt der vorgelegten Dissertation stehen.

Parts of this here presented work were previously published in the following journals. A complete list can be found in the CV in the back-matter of this thesis.

List of Publications

1. M. Ziegler, K. Ochs, M. Hansen, and H. Kohlsted, "An electronic implementation of amoeba anticipation", in *Applied Physics A* (2014).
2. M. Ziegler, M. Hansen, M. Ignatov, and H. Kohlstedt, "Building memristive neurons and synapses", in *Circuits and Systems, IEEE International Symposium* (2014).
3. M. Ziegler, C. Riggert, M. Hansen, T. Bartsch, and H. Kohlstedt, "Memristive hebbian plasticity model: device requirements for the emulation of hebbian plasticity based on memristive devices", in *IEEE transactions on biomedical circuits and systems* (2015).
4. F. Zahari, M. Hansen, T. Mussenbrock, M. Ziegler, and H. Kohlstedt, "Pattern recognition with TiOx-based memristive devices", in *AIMS Mater. Sci.* (2015).
5. S. Dirkmann, M. Ziegler, M. Hansen, H. Kohlstedt, J. Trieschmann, and T. Mussenbrock, "Kinetic simulation of filament growth dynamics in memristive electrochemical metallization devices", in *Journal of Applied Physics.* (2015).
6. M. Ignatov, M. Ziegler, M. Hansen, A. Petraru, and H. Kohlstedt, "A memristive spiking neuron with firing rate coding", *Frontiers in Neuroscience* (2015).
7. M. Hansen, M. Ziegler, L. Kolberg, R. Soni, S. Dirkmann, T. Mussenbrock, and H. Kohlstedt, "A double barrier memristive device", in *Scientific reports* (2015).
8. M. Ignatov, M. Hansen, M. Ziegler, and H. Kohlstedt, "Synchronization of two memristively coupled van der Pol oscillators", in *Applied Physics Letters* (2016).

9. S. Dirkmann, M. Hansen, M. Ziegler, H. Kohlstedt, and T. Mussenbrock, "The role of ion transport phenomena in memristive double barrier devices", in *Scientific reports* (2016).

10. M. Hansen, M. Ziegler, and H. Kohlstedt, "Double barrier memristive devices for neuromorphic computing", in *IEEE International Conference on Rebooting Computing (ICRC)* (2016).

11. E. Solan, S. Dirkmann, M. Hansen, D. Schroeder, H. Kohlstedt, M. Ziegler, T. Mussenbrock, and K. Ochs, "An enhanced lumped element electrical model of a double barrier memristive device", in *Journal of Physics D: Applied Physics* (2017).

12. J. Strobel, M. Hansen, S. Dirkmann, K.K. Neelisetty, M. Ziegler, G. Haberfehlner, R. Popescu, G. Kothleitner, V.S.K. Chakravadhanula, C. Kübel, H. Kohlstedt, T. Mussenbrock, and L. Kienle, "In depth nano-spectroscopic analysis on homogeneously switching double barrier memristive devices", in *Journal of Applied Physics* (2017).

13. M. Hansen, F. Zahari, M. Ziegler, and H. Kohlstedt,"Double-barrier memristive devices for unsupervised learning and pattern recognition", in *Frontiers in Neuroscience* (2017).

14. M. Ignatov, M. Hansen, M. Ziegler, and H. Kohlstedt, "Memristive stochastic plasticity enables to mimic neural synchrony: Memristive circuit emulates the elephant illusion", in *Science Advances* (2017).

15. K. Ochs, M. Ziegler, E. Hernandez-Guevara, E. Solan, M. Ignatov, M. Hansen, M.S. Gill, H. Kohlstedt., " Anticipation of digital patterns", in *Journal of Circuit Theory & Applications* (2018).

16. R. Ranjan, M. Hansen, P. M. Ponce, L. A. Saleh, D. Schroeder, M. Ziegler, H. Kohlstedt and W. H. Krautschneider, "Integration of Double Barrier Memristor Die with Neuron ASIC for Neuromorphic Hardware Learning", in *Journal of Circuit Theory & Applications* (2018).

17. M. Hansen, F. Zahari, M. Ziegler, and H. Kohlstedt, "Unsupervised Hebbian learning experimentally realized with analogue memristive crossbar arrays", in *Scientific reports* (2018).

Mirko Hansen

Kurzzusammenfassung

Memristive Bauelemente sind Metall-Isolator-Metall Dünnschicht-Systeme, die ihren Widerstand durch das Anlegen einer elektrischen Spannung reversibel ändern. Durch diese Eigenschaft haben sie das Potential als zentrale Komponente in neuromorphen Schaltungen ähnliche Aufgaben wie Synapsen im menschlichen Gehirn zu übernehmen. Der Vorteil daran ist, dass sie im Gegensatz zu klassischen neuromorphen Schaltkreisen eine direkte zustandsbasierte und nicht-flüchtige Gewichtung zwischen zwei Neuronen in einem einzelnen Bauteil erlauben. Dies kommt dem natürlichen Vorbild des menschlichen Gehirns sehr nah, wo die Speicherung und Verarbeitung von Informationen in einer Komponente erfolgt.

Das Ziel dieser Doktorarbeit war die Entwicklung neuartiger memristiver Bauelemente für den Einsatz in neuromorphen Schaltungen. Eine wesentliche Anforderung war eine analoge Widerstandsänderung, die – ähnlich zu Synapsen im menschlichen Gehirn – kontinuierliche Änderungen im Widerstand erlaubt. Es hat sich herausgestellt, dass sich dafür Bauteile mit einer Kombination aus Tunnel- und Schottky-Barriere am Besten eignen. Diese Doppelbarrieren-Bauteile zeigen eine analoge und flächige Widerstandsänderung. Als Referenzsystem wurden zudem filamentbasierte memristive Bauelemente entwickelt, die ihren Widerstand durch die Migration von Silber verändern. Durch die geradezu zufällige Entstehung der Filamente, weisen sie jedoch eine wesentlich höhere Bauteilstreuung und nur wenige Zwischenzustände zwischen hoch- und niederohmigen Zustand auf.

Nur die hohe Qualität des Doppelbarrieren-Bauteils erlaubte die Schaltungsintegration, ohne für jedes Bauteil individuell Schaltungsparameter anpassen zu müssen. Aufgrund der nicht-linearen Schalteigenschaften und der vorteilhaften I-V-Kennlinien konnten die Bauelemente auch in einer

platzsparenden Crossbar-Architektur realisiert werden, wodurch die Packungsdichte verzehnfacht wurde (> 70 memristive Bauelemente / mm^2). Durch die gleichzeitig vereinfachte elektrische Ankontaktierung war es möglich, eine Schaltung zur Musterklassifikation mit 180 memristiven Bauelementen zu realisieren. Diese Crossbar-Arrays gehören weltweit zu den ersten, die einen formierungsfreien Betrieb und ein analoges Schaltverhalten ermöglichen.

Der Aufbau eines automatisierten Messplatzes ermöglichte die Charakterisierung einer hohen Anzahl von Bauelementen. Die Entwicklung datenbankgestützter Mess- und Auswerteprogramme erleichterte die Analyse der Bauteil- und Schalteigenschaften.

Abstract

Memristive devices can reversibly change their resistance by applying an electrical voltage or current. These thin-film devices have the potential to serve as central components in novel neuromorphic circuits, similar to synapses in the human brain. Unlike traditional neuromorphic systems, they enable a state-based and non-volatile weight between two neurons. This comes very close to the natural model of the human brain, where information is stored and processed together.

The aim of this thesis was the development of novel memristive devices and the integration into crossbar arrays. An essential requirement was an analogous resistance change, which - similar to synapses in the human brain - allows continuous changes in resistance. It was found, that devices with a combination of tunnel and Schottky barriers are best suited for this purpose. These double barrier devices show an analogous and homogeneous resistance change. As a reference system, filament-based memristive devices have been developed that alter their resistance due the migration of silver. Since the formation of filaments is almost random, they have a significantly higher device variability and very few states between the off- and on-state.

Only the high quality of the double barrier component allowed the circuit integration without the need to individually adjust circuit parameters for each memristive device. Due to the non-linear switching characteristics and the advantageous I-V characteristics, the devices were integrated into a space-saving crossbar architecture, which increased the packing density tenfold (> 70 memristive devices / mm^2). Due to the simultaneously simplified electrical connection, it was possible to realize a circuit for pattern classification with 180 memristive devices. These crossbar arrays are among the first in the world with an electroforming-free operation and analog switching behavior.

The construction of an automated measuring system enabled the characterization of a large number of devices. The development of database-supported measurement and evaluation programs facilitated the analysis of the device and switching properties.

Contents

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Chapter 1

Introduction

Current computing platforms commonly use the von Neumann architecture, suggested by John von Neumann in 1945 [Neu45]. The primary characteristic is the separation between data storage and computation. This was a feasible option back then, but today's processor power requires intensified efforts to avoid problems during the data transport through the so-called von Neumann-bottleneck [BSS+17].

The human brain, on the other hand, processes information completely different, because storage and computation occurs in the same place. Innovative computing architectures inspired by the human brain might be an interesting alternative, because the von Neumann-bottleneck is avoided [YSS13a]. This, however, has totally different requirements towards hardware than current systems.

The combination of storage and computation would require generalized components, which cannot be emulated efficiently on highly specialized storage or computing units. Figure 1.1 shows a simplified comparison between a modern CPU and the human brain. Clearly visible is the separation between computation and storage in the modern CPU, while the highly interconnected neurons in the brain allow highly parallel data processing. The average human brain has about 10^{11} neurons [ACG+09, CIG98] and roughly 10^{14} synapses (connections to other neurons) [She98, Koc04]. This leads to a high degree of inter-connectivity which helps to solve complex problems like pattern or image recognition efficiently [Mat14].

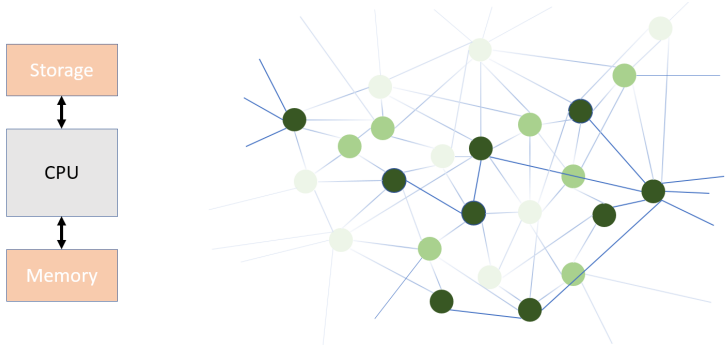

Figure 1.1: Figurative comparison between a modern computer and the human brain. The computer is limited due to the limited bandwidth of a connection between the CPU and the memory. The human brain, on the other hand, is highly interconnected and storage and processing occurs in the same place.

Even with the most advanced fabrication methods, it is virtually impossible to achieve a similar number of interconnections between electronic components like transistors. Although computers are typically superior at arithmetical problems, it took years to built a computer which could beat the chess world champion Kasparov. At the same time, the necessary computing power consumed significantly more power than a human brain [Mor98].

The first large-scale experiments to emulate synaptic behavior were conducted in the 1980s using using common CMOS technology[Mea89, SPP+17]. One alternative to the complex emulation of synaptic properties are memristive devices. These thin-film devices have the ability to reversibly change their resistance in dependence of the applied current or voltage. Initially only intended for innovative data storage systems, their unique properties are increasingly used in recent years to emulate synaptic-like behavior [SPP+17]. These devices are considered interesting candidates to mimic synaptic behavior, because their resistance depends on the history of applied voltage or

current – not unlike synapses in the human brain, where synaptic connections are strengthened or weakened depending on their activity.

Lots of effort went into the development of these devices, but most of the time without being directly optimized for neuromorphic applications. Since most of these devices had binary switching properties (distinct on- and off-states for memory and storage), their use in neuromorphic applications is sometimes limited [YSS13a]. The aim of this thesis is the development of memristive devices based on interface effects, with a gradual change in resistance and no distinct on- and off-states to get closer to the biological role model. It is, however, not sufficient to have single, individual memristive devices. Especially large-scale-implementations would require hundred or thousands of memristive devices to operate in a meaningful way. This is typically achieved using crossbar arrays, where common top- and bottom electrodes significantly increase the number of addressable devices. Although this was done for several types of memristive devices [PMBH$^+$15, AHP$^+$17, LHJ$^+$17], they show either binary switching, or require an electroforming procedure which increases the device variability during switching. Consequently, another important aim of this thesis is the development of truly analog, electroforming-free crossbar arrays.

Since the development of neuromorphic circuits is in an early stage, it is not clear which concept is the most promising and which memristive properties are required. To accommodate the requirements of a broad range of neuromorphic applications, memristive devices with digital switching will be explored as well.

The following chapter describes the theoretical background of memristive devices and the most common switching effects. The third chapter explains the individual fabrication steps of memristive devices. Chapter four deals with the characterization of the material and electrical properties. The hard-

and software, which was developed to measure, characterize and analyze memristive devices on wafer scale is described in chapter five. Chapter six deals with the fabrication of filament-based memristive devices. Chapter seven describes the development of interface-based memristive devices with various metal oxide materials. The last chapter features the successful integration of interface and filament-based memristive devices in two neuromorphic applications.

Chapter 2

Theory

This chapter deals with the physical background of common memristive devices. The aim of this chapter is to understand, which components and materials are necessary for various memristive devices. In addition, it illustrates how the different, individual layers can possibly interact with each other leading to interfacial properties like tunneling or Schottky-barriers. These effects are known to be (partially) responsible for the resistive switching of these devices.

2.1 Memristive Devices and Resistive Switching

The resistive switching phenomenon was first observed in aluminum oxide between two metallic films in 1962 by Hickmott. Since then, this electrically induced change in resistance was observed in various material systems with different switching mechanisms. Some examples will be given below. In 2008, this topic gained momentum when a paper from Dmitri Strukov and Stanley Williams compared resistive switching devices with memristors [SSSW08]. The memristor was proposed in 1971 by Leon Chua, and is supposed to be the fourth circuit element next to resistor, inductor and capacitor [Chu71]. In general, a memristor can be described as a resistor, where the resistance depends on the history of applied voltage or current. Depending on the choice of materials for the insulator or electrodes, different switching mechanisms

can be induced. Due to the large variety of different concepts, only the most common principles will be discussed.

2.1.1 Materials

In general, memristive devices consist of an insulating material between two electrodes. Depending on the choice of materials, a broad range of devices and switching mechanisms can be built. Therefore, it is reasonable to categorize the materials seperately into electrodes and insulators.

2.1.1.1 Electrodes

Electrodes used for memristive devices can be separated into three categories: inert, reactive and electrochemically active. For inert materials, it is typically assumed that the electrode (e.g. Pt, Au) does not react with the insulating layer (i.e. no oxygen uptake) [WDSS09a]. For example, an insulator between two inert gold electrodes may undergo an electrical breakdown during switching (described in section 2.1.2.2 in more detail).

Metals with a high mobility like Ag and Cu are typically used in electrochemical migration devices. These materials are responsible for the switching mechanism by migration through the insulation layer under applied voltage (see section 2.1.2.1). This mechanism is nearly independent of the insulator, because the resistance of the bulk insulator is typically unchanged.

In memristive devices with reactive electrodes, the electrode material plays an active role in the memristive switching. Apart from the previously mentioned electrode materials, most other metals react with the insulating material to some extent under bias application. For example, typical metals

like Al, Ti or Ni are used in these devices. The isolating material, commonly a metal oxide, reacts during switching via oxygen diffusion or redox-reaction with the electrode. [WDSS09a]

2.1.1.2 Insulators

Many metal oxide have been used in memristive devices [Iel16, IW15]. Among these metal oxides, however, the focus lies on transition metal oxides with various possible oxidation states. If a material has many oxidation states, the energy to trigger this oxidation is much less compared to a material with only a few states. For example, the reduction of the metal oxide leads to a lower oxidation state, which typically decreases the resistance [Bac09].

The resistance of a memristive device cannot be compared with the bulk resistance of the insulator. Most of the time, additional barriers have a significant influence on the resistance. Furthermore, the insulator thickness can determine the possible switching mechanism. In thick insulators (e.g. 100 nm), the field strength may not be sufficient to induce the motion of oxygen ions before the breakdown voltage is reached [Lom50]. For smaller thicknesses, the field strength can be significantly larger, enabling resistive switching effects unseen in thicker layers.

2.1.2 Switching Mechanisms

Most concepts are based on a metal-insulator-metal junction. Typically, the insulator is initially in the high resistance state. By applying a set-current or voltage, it is possible to change the resistance of the insulting material or

its interfaces from the initial high resistance[1] state to a low resistance state. The device can be switched back to the high resistance state by applying a suitable reset-current or voltage. The magnitude of this resistive switching and the necessary amplitudes and polarities strongly depend on the kind of switching mechanism.

The three most common switching principles are a) electrochemical metallization, b) valence change mechanism and c) interface switching. These three switching mechanisms will be explained in more detail in the next paragraphs, starting with an overview in Figure 2.1.

2.1.2.1 Electrochemical Metallization

This type of device typically consists of an inert electrode like gold, an ionic conductor and a material like copper or silver. These metals are known for their high ionic mobility under small electric fields. If a negative voltage is applied at the inert electrode, Ag+ ions are formed and migrate towards the inert electrode and accumulate, leading to a filament that grows in the directions of the silver electrode. In this state, the highly resistive ionic conductor is shorted by the silver filament leading to a very low resistance. In the beginning of the reset process, the filament is destroyed at a thin spot due to the high current density and temperature at this point. If the polarity is reversed, the filament dissolves and the silver ions move back towards the silver electrode. [DZH+15, KPM05]

This mechanism typically allows significant changes in resistance (several orders of magnitudes), but only allows binary on- or off-states.

[1] Nearly all memristive device initially have a high resistance. Ge_xSe_{1-x} in combination with Ag or Cu is one of the few devices that regularly show an initial low resistance state, which is explained by diffusion during the deposition. [SMR+09, SVW09]

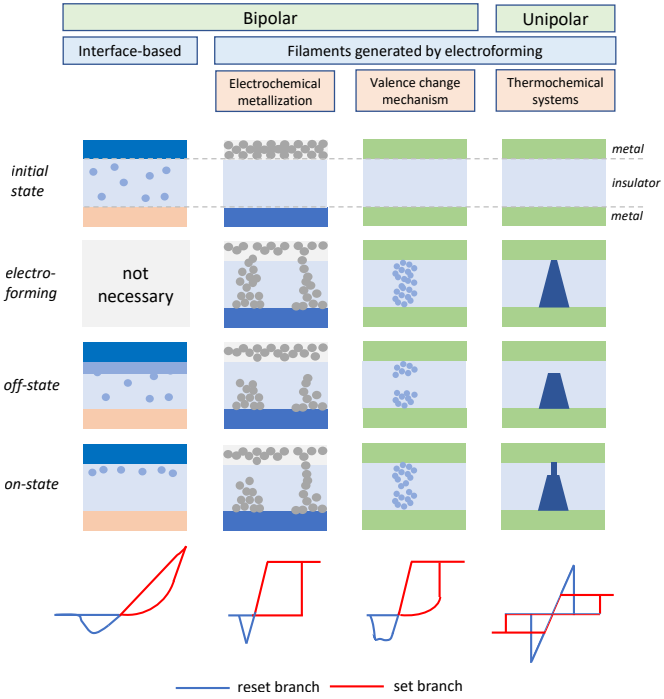

Figure 2.1: Overview over the most common resistive switching mechanisms. Schematically shown are intermediate stages of the switching process. The I-V-curves are simplified examples to show the different characteristic properties.

2.1.2.2 Thermochemical Systems

This switching mechanism typically consists of a rather thick dielectric layer between two metal electrodes. To induce resistive switching in this type of device, an electroforming step is necessary [Hic62, JSBW08, MMD+09]. This electroforming step leads a dielectric breakdown by applying a large voltage (and a suitable current compliance) to the device. This breakdown creates one or more highly conductive filaments between the electrodes, which is

often identical to the low resistance state of the device. Unlike the filaments created in ECM-cells (which mainly contain the electrode material), these filaments are highly conductive paths in the actual insulator. Afterwards, the subsequent application of smaller voltages (*without* current compliance) leads to large current densities, which is sufficient to destroy the filament at the weakest / thinnest spot and increases the resistance (the high resistance state). In subsequent set and reset cycles, this small part of the filament will be re-established and destroyed. Due to the thermochemical effect, this type of device is unipolar, i.e. can be set and reset with positive or negative voltage. Figure 2.1 shows an exemplary I-V-curve for this type of device. [ZLL+12]

2.1.2.3 Interface Mechanisms

In this type of device the change in resistance typically does not happen in the bulk insulator. Here, the dominating effect stems from changes of the electrical properties at the involved interfaces. Most of these devices utilize a Schottky-barrier, where slight changes at the corresponding interface leads to a significant change in resistance. One scenario could be that the distribution of oxygen ions in the insulator changes due to the applied electric field [MSB+08, BL10].

Chapter 7 describes the requirements for the fabrication of memristive devices using interface effects.

2.2 Current Transport through Energy-Barriers

2.2.1 Semiconductor-Metal Interface

Semiconductor-metal interfaces can form either rectifying or non-rectifying contacts. The non-rectifying, *ohmic* contact, is often wanted and needed to improve the electrical contact and to reduce unnecessary losses in semiconductor devices. For a series of memristive devices, however, rectifying contacts have essential properties that make the use of this *Schottky barrier* interesting and necessary. The electronic properties of metal-semiconductor-contacts will be described using the band diagrams shown in Fig. 2.2. Figure 2.2a shows the band diagram for a metal-semiconductor interface. The work-function $q\Phi_m$ of a metal is responsible for the type of contact formed when in contact with a semiconductor. This energy is necessary for an electron to leave a metal and enter the vacuum. Figure 2.2b shows the corresponding band diagram for the semiconductor-vacuum case.

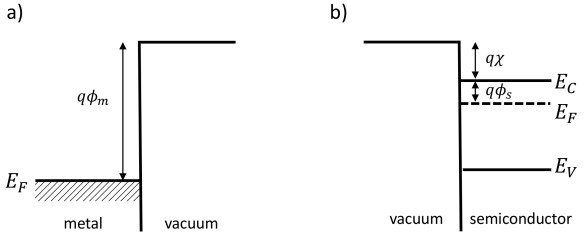

Figure 2.2: Band diagrams of metal-vacuum **a** and metal-semiconductor **b** interfaces.

When the metal and the semiconductor are brought in contact, the levels of the individual Fermi energies (E_F) will be the same. As a result, the valence (E_V) and conduction (E_C) bands will *bend* accordingly. The band diagram in thermal equilibrium is shown in Fig. 2.3a. The barrier height

for the metal decreased from $q\Phi_m$ by ($q\chi$) due to the electron affinity of the semiconductor ($q\chi$). For voltages below the built-in potential (V_{bi}), no current flows. If a large positive voltage is applied to the semiconductor (Fig. 2.3b), the band bending increases and the current in reverse direction decreases due to a larger barrier height.

In forward direction (Fig. 2.3c), on the other hand, the semiconductor potential increases with rising forward voltage and leads to a smaller energy barrier. The current in this direction increases exponentially with increasing forward voltage.

Beth [BL42] described the rectifying metal-semiconductor interface with a thermionic emission theory. This theory was developed with the following boundary conditions: The barrier height $q\Phi_{Bn}$ has to be significantly larger than kT, collisions within the depletion region and the effect of image forces are not taken into account.

The current in forward direction can be thus described by:

$$J_n = A^* T^2 \cdot \exp\left(-\frac{q\Phi_{Bn}}{kT}\right) \cdot \left(\exp\left(\frac{qV}{kT}\right) - 1\right) \tag{2.1}$$

2.2.2 Tunneling Effects

Figure 2.4 shows a metal-insulator-metal junction in equilibrium (a) and biased in reverse direction (b). For very thin insulator layers (few nanometers), electrons may *tunnel* through the insulator irrespective of the barrier height. [Sze81]

Simmons [Sim63] derived a set of equations to describe the tunneling phenomenon through thin insulating layers. For voltages $V < \Phi_0/e$, and if

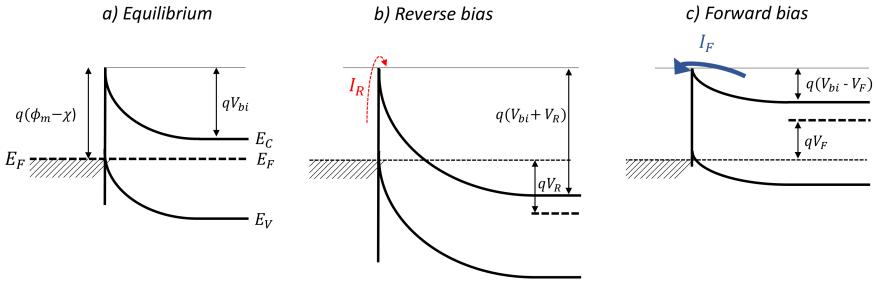

Figure 2.3: Metal-semiconductor Schottky-barrier in **a** equilibrium, **b** reverse bias and **c** forward bias

the mean barrier height of a tunnel barrier is known, the current through the barrier can be described by the following equation:

$$I = I_0 \left[(\phi - eV/2) \exp\left(-A\sqrt{\phi - eV/2}\right) - (\phi + eV/2) \exp\left(-A\sqrt{\phi + eV/2}\right) \right] \tag{2.2}$$

with

$$J_0 = \frac{e}{2\pi h \beta^2(\Delta) s^2} \quad \text{and} \quad A = \frac{4\pi\beta(\Delta)s}{h}\sqrt{2m} \tag{2.3}$$

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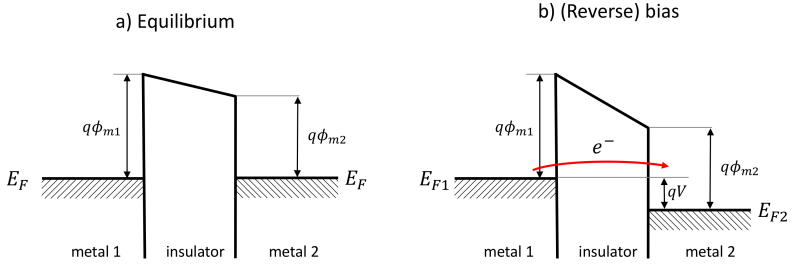


Figure 2.4: Band diagram of a tunnel barrier in **a** equilibrium and **b** (reverse) bias

2.2.2.1 Use in Memristive Devices

The use of the tunneling [BL10, MSB+08] and the Schottky effect has been used before to explain the resistive switching principle observed in memristive devices. In both cases, the general switching mechanisms can be explained by a decrease of the individual barrier height for the set process and a reversal or increase for the reset process. In most cases, the switching is assumed to occur either in the bulk material or at one interface.

2.3 Neuromorphic Computing

The concept of neuromorphic computing is attributed to Carver Mead, who proposed to use very-large-scale integrated (VLSI) transistor circuits to mimic or emulate neurological functions of animal or human brains [Mea89]. Although simulations of neuronal functions were already done on conventional computers back then [Ale89], the sheer complexity of the human brain with 10^{15} synapses and approximately 10^{16} synapse operations per second renders even the simulation of small parts of the brain impossible. It is thus assumed, that the only way to reach a similar computational power is through the adaption of brain-like behavior in highly integrated analog circuits [Mea90].

Almost all concepts for the emulation or simulation of neurological functionality implement synapses and neurons as the most fundamental building blocks of the nervous system in animals and humans. There are several types of neurons, but most are electrically excitable cells that transmit and process input by electro-chemical signals. Neurons are typically interconnected with hundreds or thousands other neurons. Each neuron in this network regularly receives electrical stimuli by incoming *action potentials*. Figure 2.5 shows a schematic connection between some neurons. Depending on the number and

frequency of action potentials generated by the pre-neuron, and the connection strength between the neurons, at some point the stimulation is sufficient to reach a certain threshold potential, and the receiving post-neuron fires. This induced action potential than triggers further connected neurons.

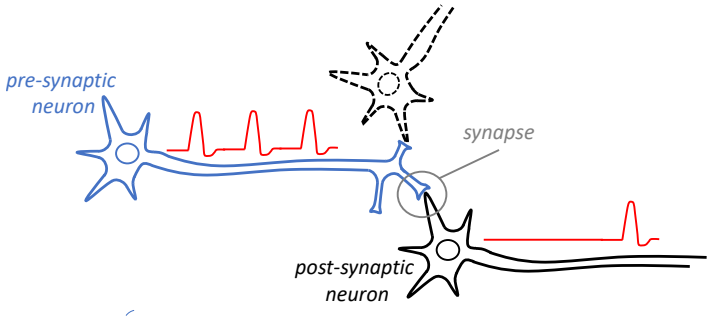


Figure 2.5: Interaction between neurons via electrical signals (action potentials) passed through synapses

The connection strength between neurons is not constant and changes over time. In general, it can be said that the connection strength between frequently stimulated neurons increases, while the connection strength of rarely used neurons decreases. The exact nature of this change in connection strength depends on many variables, but a very simple (and famous) *learning rule* [Heb49], coined by Donald Hebb, states in its simplified form: *"what fires together, wires together"*. This first description of synaptic plasticity states that the connection strength between neurons increases, if the pre-neuron is repeatedly involved in exciting the post-neuron.

The implementation of this synaptic plasticity (or the ability to change the connection strength between neurons), is one of the core components in neuromorphic computing [GLS+15, QMC+15]. A very simple potential implementation is the leaky-integrate-and-fire neuron shown in figure 2.6. The input current (equivalent to incoming action potentials at a post-neuron)

charges the "membrane potential" across capacitor. Similar to the *weight* of a synapse, the memristive device at the input modulates the input with its variable resistance. The leakage of ions into or out from a neuron through leak channels is realized by the parallel resistor, which permanently decreases the "membrane potential" of the capacitor. If the incoming electrical stimuli exceeds the leakage current, the membrane potential increases up to the threshold voltage defined by the comparator. At that point, the output of the comparator excites a spike (comparable to the post-neuron in figure 2.5). At the same time, the switch is closed and the capacitor is instantaneously discharged. The voltage across the capacitor remains suppressed for a refractory period τ, to prevent further increases in the membrane potential comparable to a biological neuron. [GHS02]

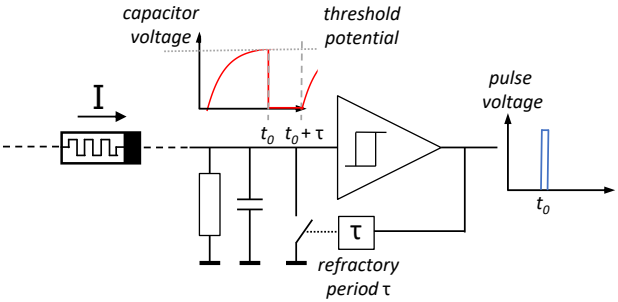


Figure 2.6: Schematic circuit to describe the realization of an leaky-integrate-and-fire neuron, which similarly to a neuron in the brain integrates incoming signals and spikes when a given threshold is reached.

2.3.1 Memristive Devices

A challenging problem in the field of neuromorphic computing is the significant number of connections between several neurons. This problem is further aggravated by the fact that each of these connections requires an adjustable weight to mimic the synaptic plasticity between neurons. If this is supposed to

be done in an efficient manner, the classical von Neumann architecture [Neu45] used on most computer systems has to be replaced with a system that does not separate the processing and storage of information. The emulation of synaptic plasticity would thus profit from electrical devices which combine the connection and weight between neurons without a significant circuit overhead. Memristive devices feature some intrinsic properties, which might allow to implement several of these key aspects. First of all, they can store the weight of a synaptic connection (in terms of resistance or conductivity). Furthermore, the change in weight due to neuronal network activity is the second property which is intrinsically available, because the resistive switching properties of memristive devices is exactly that.

Accordingly, it is no surprise that a multitude of emulations of neuronal phenomena using memristive devices, among them Hebbian learning [ZSP+12], spike-timing-dependent plasticity (STDP) [JCE+10, LBSGCM+11], long term potentiation or depression (LTP / LTD) [OHT+11] appeared in recent years. In most cases, however, these experiments where conducted only on one or few devices.

2.3.2 Requirements for Memristive Devices

Figure 2.7 shows a spidermap illustrating the importance of various device properties for different applications of memristive devices [YSS13a]. It is obvious that the requirements strongly depend on the intended use. For example, the switching speed and the retention are two drastically different parameters. While neuromorphic applications can be satisfied with short retention and slow switching speed, the opposite is true for storage applications, because the stored data has to be readable for at least 10 years and the switching speed needs to be compatible with current memory techniques. Memristive devices for neuromorphic applications are commonly

used as synapse emulators and the resistance change is often required to be continuous. This indicates that they need a large number of states, unlike memristive devices for storage applications, where only a small number of states needs to be read out quickly. The energy dissipation is a crucial factor

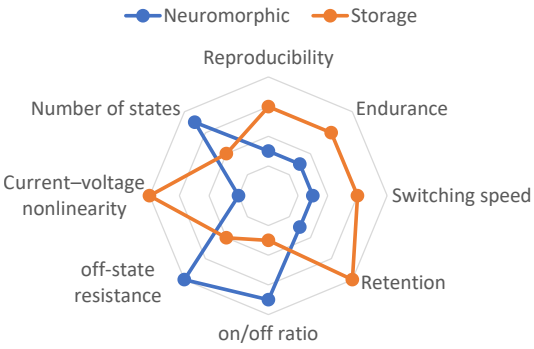


Figure 2.7: Spidermap illustrating the importance of several device parameters for neuromorphic and storage applications (adapted from [YSS13a])

for neuromorphic applications so that the current in the off state should be as small as possible. In order to make the design of neuromorphic circuits more simple, it is often helpful to have a huge margin between the on and the off state. A large current-voltage nonlinearity is important for storage applications because this would allow to build large arrays with densely packed memristive devices without the need for additional space requiring selector devices.

Chapter 3

Fabrication of Memristive Devices

Figure 3.1 shows a typical cross section of the memristive devices fabricated during this thesis. The most important layers are the aluminum oxide tunnel barrier, a thin reactively sputtered metal-oxide and the Schottky-contact (oxide-gold interface). This chapter describes the fabrication process of these devices from blank silicon wafer to finished devices. Since most techniques described here are standard technologies, a detailed description of the used techniques can be found in the literature [Was08, Mad11].

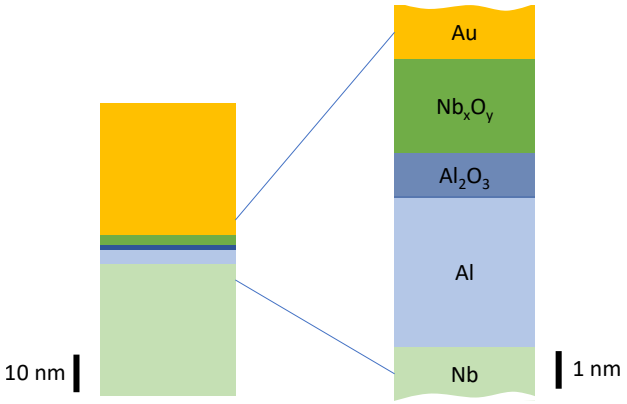


Figure 3.1: Layer sequence of a typical memristive device fabricated in this thesis. On the left, the complete stack with top and bottom electrode is shown. The zoomed-in part on the right highlights the functional layers necessary for these memristive devices. The aluminum oxide tunnel barrier, a thin reactively sputtered oxide and the Schottky-contact (oxide-gold interface).

The complete process is shown in Figure 3.2 and can be divided into four major steps: a) deposition of the memristive multilayer stack (Figure 3.2a), b) etching of unnecessary parts to define the contact area (Figure 3.2b), deposition of an insulating layer (Figure 3.2c), and the final metallization layer (Figure 3.2d).

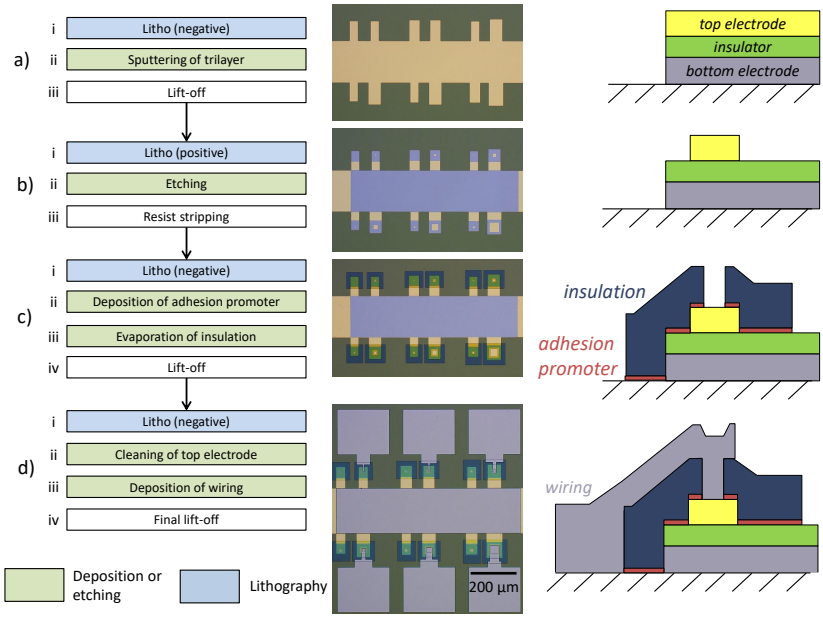


Figure 3.2: Generalized overview of the fabrication steps to fabricate memristive devices, showing microscope images from top and schematic cross-sections.

3.1 Mask Layout

Two typical sets of mask layouts used for two different processes used in this thesis are shown in Figure 3.3). The set of masks in Figure 3.3a was

used to fabricate memristive devices in the developing stage to determine the materials and parameters to yield memristive devices. It has independent contacts, ensuring that the measurements are only conducted on one device individually, with no influence of neighboring cells. One wafer contains 32.016 devices (or $\approx$ 5336 devices of one contact size). After the developing stage, the masks shown in Figure 3.3b were developed to integrate a large number of devices in neuromorphic circuits. A crossbar structure was used to limit the overhead to connect several devices individually, because now only 32 wires are necessary to address 256 devices. Due to the decreased overhead for contact pads etc., one wafer now contains 304.128 devices of one size. It is necessary to point out that not always all devices on the 4 inch wafers were usable, because only devices in the center of the wafer have the necessary deposition parameters and film quality. This limitation stems from the 4 inch targets in the sputtering system, which make a homogeneous deposition on 4 inch wafers difficult.

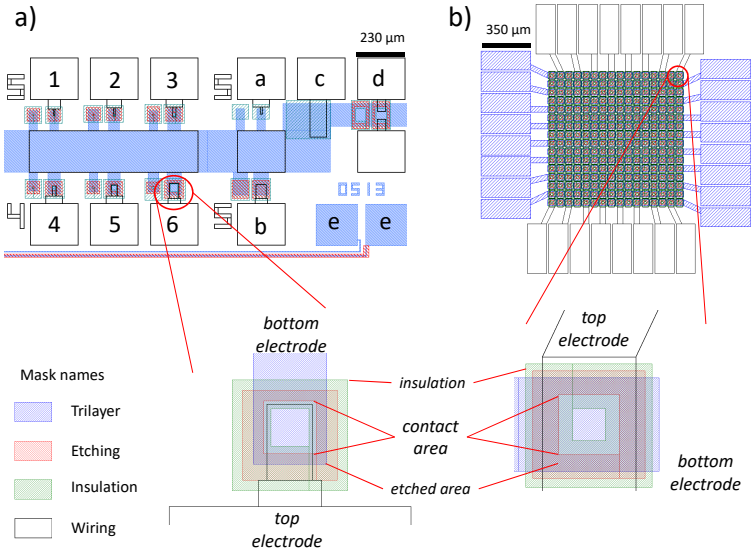


Figure 3.3: Subcells of the mask layout of the most commonly used masks: **a** Wafer layout used for initial characterization of new material systems, each contact has an independent top contact. The numbers 1-6 indicate the contact pads for contact areas ranging from 100 μm^2 to 2500 μm^2. The letters a-e indicate test-contacts to check a-c: insulation resistance of the evaporated SiO layer for 3 different areas; d: conductivity of the top electrode (after etching step in sputter system, before deposition of wiring); e: conductivity of the top and bottom electrode **b** 16 $\times$ 16 memristive devices arranged in a crossbar structure, with common top and bottom electrodes

3.2 Lithography

Silicon wafers are used as the substrate for the fabricated memristive devices. The wafers used here were single-side polished 4 inch / p-type wafers with (100)-orientation. The conductivity was 5-25 Ωcm. Additionally, 400 nm of

thermal oxide guarantee the electrical insulation between the structures on the wafer.

In the first preparation step (Figure 3.2 a-i), the wafer will be patterned using standard UV-lithography to define regions where the metal-insulator-metal stack will be deposited. In order to achieve this, a micrometer thick photoresist is spin-coated onto the wafer. Afterwards, the wafer will be placed on a hotplate to remove solvents from the polymer. This photoresist contains polymers, which — depending on positive or negative tone – make the resist either more soluble or less soluble in a developing agent than the unexposed areas. In combination with a chrome covered glass mask, these properties can be used to selectively cover certain parts of the wafer with resist, which will protect the underlying part of the wafer in the subsequent fabrication step.

For all samples fabricated in this thesis, the resist AZ5214E is used with the developer AZ726. AZ5214E is an image reversal resist, and can be used either as a positive or negative resist. The image reversal is induced by heating up the sample after the image-exposure using the aforementioned chrome mask to 120 °C and afterwards exposing the whole wafer to UV-light. This procedure yields a negative tone process, leading to resist structures with a pronounced undercut. This makes the removal (or lift-off) of the resist after a deposition step significantly easier, because the negative wall-profile always leaves the sidewalls of the resist uncoated. After the developing process, the wafer is removed from the clean room and brought to the sputter system described in the next section.

3.3 Sputtering

The metallic and insulating layers for the memristive devices in this work were magnetron sputtered using a Univex 450b system from Leybold (Figure 3.4). The samples are loaded using the load lock (EK). An automated transfer system transports the samples to the individual chambers, e.g. the main chamber (HK), where most materials were deposited using one of eight 4 inch sputter guns. The two remaining chambers (oxidation chamber – OK and separate chamber – SK) were used to oxidize samples at high pressures (max. 100 mbar) or deposit another material using a six-inch sputter source.

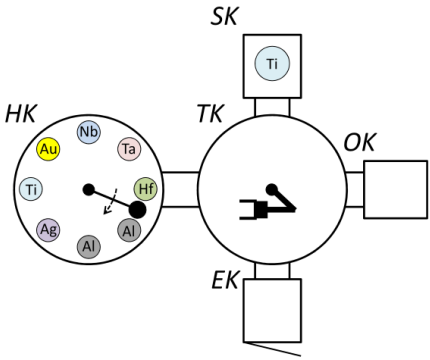


Figure 3.4: Schematic of the Oerlikon Leybold 450b sputter system and the different chambers; HK main chamber where most layers are deposited using 4 inch targets; SK separate chamber with 6 inch target; OK oxidation chamber for the oxidation of samples with pressures up to 100 mbar; EK load lock for sample loading; TK transfer chamber, computer-controlled transfer of samples between chambers.

Sputtering is a deposition process in a vacuum system, where the background pressure is typically very low (in the system used here, it is typically around 3-4·10^{-7} mbar). The sputter gun consists of a plate (target) of the material to be coated and is water-cooled from behind to remove excessive

heat during the sputtering process. The target is positioned downwards, facing the substrate. Between substrate and target is a shutter, which is closed during the initial pre-sputtering process to clean the target and achieve steady-state conditions for the actual sputtering process.

When the process gas (typically an inert gas like argon) is let in (to about 10^{-3} - 10^{-2} mbar) and a voltage is applied to the target, the gas ionizes and cations accelerate towards the target, ballistically removing atoms from the target surface, which subsequently coat the wafer below. For all deposited layers, the DC power source was set-up to maintain a constant power during sputtering.

For each sample, this sputtering procedure was repeated several times with different materials to deposit a multilayer stack. The procedure was similar for most samples: First (Figure 3.2 a-ii), the wafer is placed onto a copper sample holder and loaded into the sputter system using the load lock (Figure 3.4, EK). A load lock in a vacuum system allows loading samples without breaking the vacuum in the deposition chamber, avoiding time consuming pumping to a reasonable pressure. The sample is then transferred from the load lock to the main chamber (Figure 3.4, HK), where niobium is sputtered, followed by a thin layer of aluminum (while rotating the sample in the chamber, to get a thin and uniform layer). The Nb/Al material system was chosen because the deposited layers have a very small surface roughness (Al wets Nb, leading to closed Al films on Nb and furthermore smoothes the roughness introduced by the Nb). It is important to let the sample cool down before the deposition of the aluminum layer, because the quality of the aluminum layer decreases with an increase in substrate temperature. [Him15] After the deposition of the aluminum layer, the sample is transferred to the oxidation chamber (Figure 3.4, OK). Only this chamber allows the oxidation of samples with pressures up to 100 mbar, because the vacuum system was designed accordingly (e.g. closing the valve leading to the turbomolecular

pump for harmful pressures). The aluminum oxide tunnel barriers in this thesis were typically oxidized with pressures of 100 mbar for 20-30 minutes, resulting in approximately 1-2 nm thick tunnel barriers[RKGG00].

For the deposition of the remaining layers, the sample is transferred back into the main chamber where typically a reactively sputtered oxide followed by the top electrode is deposited.

Two methods are typically used to sputter memristive oxides. A common method is to use a stoichiometric metal oxide target. This, however, requires an RF-sputter source, because these targets are typically insulating and are thus not suitable for DC sputtering. Another approach is reactive sputtering using a conductive metal target in an Ar/O_2 atmosphere, which was commonly used for most memristive devices in this thesis. This allows the use of conventional metal targets and a DC power source, significantly easing the problems typically encountered with RF sputtering (e.g. plasma ignition, deposition rate). However, the degrees of freedom in terms of deposition parameters and film properties are reduced significantly, because stable operation is only feasible in the so-called "poisoned target" mode, where the first nanometers of the target surface are completely oxidized [SBS84]. This was observed even for minute amounts of oxygen, leading to layer properties that are mostly independent from Ar/O_2-ratio.

After sputtering, the samples are placed in acetone to remove the resist and the unwanted deposited materials (lift-off) (Figure 3.2 a-iii).

3.4 Etching

In the next step, the contact area of the memristive device is defined using the aforementioned resist AZ5214E without the image reversal step, yielding a

positive tone process (Figure 3.2 b-i). Due to the insulator / metal structure, it was sufficient to remove the top electrode to define the contact area (Figure 3.2b-ii). For the fabrication of memristive devices, the following etching techniques were used:

- wet etching – *for Au*
- reactive ion etching (RIE) – *for Nb, Ti*
- ion beam etching (IBE) – *for all other materials*

Initially, the ion beam etching system (Oxford Ionfab 300+) was the preferred etching tool, because the physical etching principle allowed etching of any top electrode material without difficulties. Furthermore, the integrated secondary ion mass spectrometer allowed a supervised etching process and made it possible to stop the etching when the relevant layers were completely etched.

However, during the fabrication of the first memristive devices, it was observed that the current through the device was not strictly depending on the contact area, but on the device circumference. This indicated problems during the etching process, because this is the only process related to the circumference (or sidewalls) of the device. Since etching defects like re-deposition of materials are a well known problem of ion beam etching, the following experiment was conducted to analyze the influence of the ion beam etching: A sample with the layer sequence Nb/Al/TiO_x (50 nm)/Nb (120 nm)/Au (37 nm) was sputtered and subsequently etched in several steps using different etching techniques.

Afterwards, the resulting devices were electrically measured. The results are shown in Figure 3.5. In the first scenario, the Au / Nb electrode was etched using ion beam etching. The resulting I-V-curve is shown in Figure 3.5 (red curve). Assuming a re-deposition of the surrounding metals, the

sample was afterwards etched using a pure SF_6-plasma with the intention to remove re-deposited Niobium from the sidewalls. Although the resistance of the device shows a significant increase (orange curve), significant features (around 2 V) remained. Another possible etching defect is damage induced by the highly energetic ion beam, possibly leading to oxygen vacancies and an increased conductance. To test this hypothesis, the sample was annealed in an oxygen plasma to decrease the influence / amount of oxygen vacancies (blue curve). Finally, a sample from the same deposition batch was wet chemically etched using potassium iodide (KI) solution to remove the Gold layer and reactively etched with SF_6 to the Niobium layer (black curve). This procedure can be considered to be significantly less harmful in terms of etching defects and leads to a significantly larger resistance compared to the other etching procedure. Even considering all the post-etching annealing steps, the ion beam sample never gets close to the reference sample, indicating that etching artifacts make a physically sound investigation of resistive switching effects difficult.

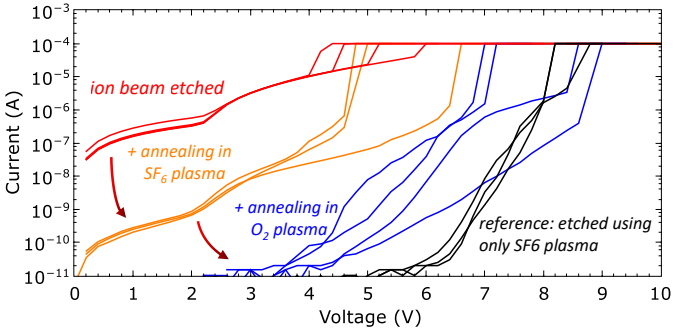


Figure 3.5: Electrical I-V-measurement on highly resistive Nb/Al/TiO_x/Nb/Au samples showing the influence of various etching and annealing steps on the resistance of the device.

3.5 Insulation

After the contact has been defined, an additional insulation layer surrounding the contact is necessary to separate the bottom electrode from the later sputtered wiring electrode (Figure 3.2 c-i). There are two requirements for the insulation resistance: The insulation resistance should be significantly higher than the resistance of the memristive layer in the device to guarantee that no parasitic effects influence the measurements. The material needs to have a reasonable deposition rate to allow a thickness of several hundred nanometers (typically 600 – 800 nm), to cover the topography or remainders of previous deposition steps (e.g. resist fences).

The method of choice is thermal evaporation of silicon monoxide (SiO) (Figure 3.2 c-iii), because it allows a high deposition rate without significantly increasing the substrate temperature, which would make the resist removal difficult. Furthermore, it has an un-measureable insulation resistance ($I = < 1 \cdot 10^{-12}$ A at 40 V) for the thickness used here. Due to the bad adhesion of evaporated films (compared to sputtered layers), it was necessary to sputter an adhesion-promoting layer of insulating aluminum nitride before evaporation[2] (Figure 3.2 c-ii). Due to the large film thickness, the lift-off after this step has to be done carefully and is best done overnight.

3.6 Metallization

In this last fabrication step, the top electrode is electrically connected to large pads (200 μm $\times$ 200 μm) close to the contact (Figure 3.2 d-i). This step (and the insulation step earlier) is often avoided in the fabrication of simple

[2] This step was necessary due to switching from ion beam etching to reactive ion etching / wet etching, because the adhesion on the partially etched layers decreased significantly.

memristive devices to reduce the time spent on fabrication. In this case, the top electrode is typically contacted directly through micrometer-sized probe tips. Although this works in principle (and was conducted here as well from time to time), there are significant uncertainties involved (e.g. pinching through the top electrode or compressing the layers; insufficient electrical contact) and was thus avoided to yield highly reproducible measurements.

For the metallization step, a metallic layer (typically niobium or titanium) is placed across the contact and the insulation to a pad next to the insulation. To improve adhesion, and to remove oxidized parts of non-gold top electrodes, an RF-plasma (typically 30-200 W, 5-40 seconds) in the sputtering system is used to etch the first nanometers of the top electrode (Figure 3.2 d-ii). The deposited wiring typically has a thickness of 300-500 nm, to cover the topography of the evaporated insulation (Figure 3.2 d-iv).

Chapter 4

Characterization

This chapter is divided into the (pure) material characterization as well as the electrical characterization of the complete memristive device. The in-situ as well as ex-situ characterization methods should reveal first of all the material quality after deposition. More importantly, it is used to identify and improve process as well as device parameters in order to fabricate different types of memristive devices. For that purpose, individual material components of the memristive layers are characterized using anodization spectroscopy and a low temperature measurement. Both of these measurements are necessary to investigate the interface effects leading to efficient tunneling behavior.

4.1 Material Characterization

4.1.1 Atomic Force Microscopy

Atomic force microscopy (AFM) is a scanning probe microscopy method, where a nanometer-sized tip attached to a micrometer-sized cantilever is used to analyze the surface of a sample. [BQG86] [EW10]. In the AFM operation mode used in this thesis(tapping mode), the AFM tip is brought close to the sample surface and the cantilever oscillates with a resonance frequency of $\approx$ 250 kHz. The repulsive and attractive forces between the sample and the tip change the deflection of the cantilever. This deflection is

detected using the reflection of a laser beam aimed towards the upside of the cantilever (Fig. 4.1**a**). This information is used to calculate the height of the sample topography, and was used to measure the roughness and thickness of deposited films. Figure 4.1**b** and **c** show the thickness measurement of a deposited metal film after the previously coated resist was removed with acetone.

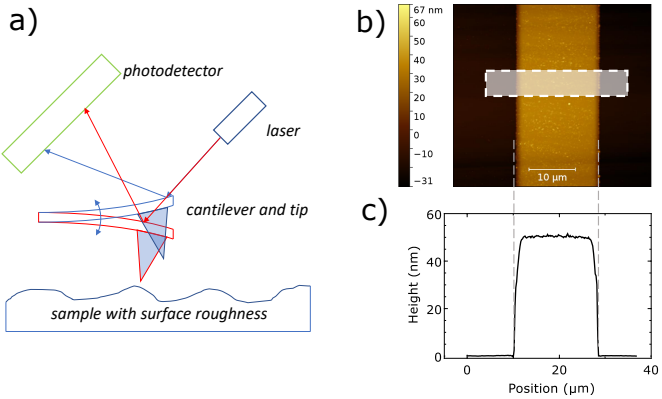


Figure 4.1: Description of atomic force microscopy measurement. **a** Basic description of an AFM measurement. **b** Exemplary measurement to determine the sputter rate of a new material. The white rectangle indicates the area used for the generation of the profile. **c** Background-removed cross-section of the structure.

4.1.2 Anodization Spectroscopy

Anodization spectroscopy has been applied successfully to optimize the fabrication of high-quality low-temperature niobium Josephson tunnel junctions [IH89] . If the sample is placed in an electrolyte with a gold counter electrode and a constant current is applied, the sample will start to oxidize. This oxidation front propagates from the top of the sample down to the

substrate. If the voltage during this anodization is measured simultaneously, the derivative dV/dt can be calculated and interesting features of the individual layers can be extracted from the resulting spectrum [JNR67]. This method allows to measure the thickness and interface roughness with characteristic anodization spectra of bulk materials and interfaces. Figure4.2 shows qualitatively how the thickness of a layer and the interface roughness affects the anodization spectrum. The thickness is calculated by measuring the voltage between the start of a layer and the end of a layer. Due to the roundish features of a curve, the full width at half maximum (FWHM) value is typically used. Using literature values (or otherwise calibrated values) the thickness can be calculated because every material has a specific anodization rate (voltage per nm). The interface quality can be qualitatively analyzed by comparing the transition region in the anodization spectrum. A sharper transition indicates a lower interface roughness, while a broader transition indicates a larger surface roughness. The width of the transition region depends on the surface roughness because in this region both materials are still present.

This anodization spectroscopy was applied to the characterization of Josephson junctions in section 7.1.2.

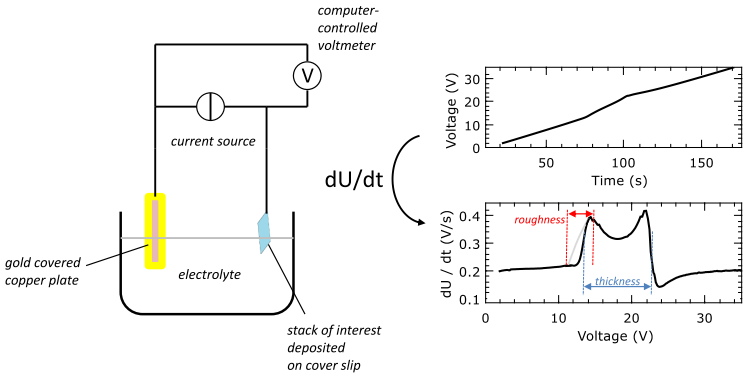


Figure 4.2: Basic setup to analyze metallic thin-films in an electrolyte with gold counter-electrode through anodization spectroscopy. The voltage is measured, and its time derivative is plotted against the voltage. The anodization spectrum shows an Nb/Al-Al_2O_3/Nb Josephson junction.

4.2 Electrical Characterization

4.2.1 Current-Voltage-Measurements

Two types of voltage/current measurements can be distinguished: Current-driven measurements where the resulting voltage is measured or voltage-driven measurements where the resulting current is measured.

To investigate the electric properties of memristive devices, a voltage is typically applied at the top electrode and the bottom electrode is grounded. For memristive devices, this voltage is changed over time (see Fig. 4.3 (**a**)) and the current is recorded simultaneously. The parameters of this sweep, e.g. the maximum positive/negative voltage, the sweep rate and the direction of the sweep depend on the memristive device and its switching mechanism. Due to the high resistance of the memristive devices, current-driven sweeps were not used to characterize memristive devices. While many

available instruments are able to measure currents down to the pico-amp range, *sourcing* currents over several orders of magnitudes (10^{-12}-10^{-3} A) is significantly more difficult, and is typically not used to characterize high-resistance memristive devices.

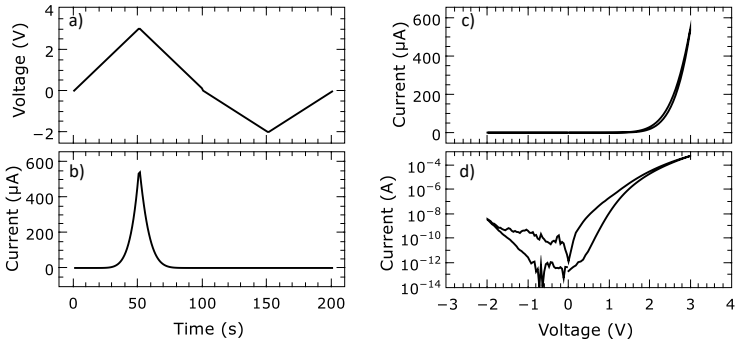


Figure 4.3: Current-voltage measurements. **a** Applied voltage over time and the simultaneously measured current **b**. **c** and **d** show the typically used current vs. voltage plot to highlight the memristive hysteresis. Due to the many orders in current magnitude, **d** is shown with a logarithmic current axis.

4.2.2 Low Temperature Measurements

In this thesis, low temperature measurements at 4 K were conducted to analyze the tunneling properties of aluminum oxide Josephson junctions. For this purpose, Josephson junctions with the layer sequence Nb/Al-Al_2O_3/Nb were fabricated [GWH83]. To investigate the quality of the tunneling barrier, the superconducting regime has to be reached for the Niobium electrodes, i.e. these devices have to be cooled down below the critical temperature of Niobium ($T_c \approx 9.2$ K). This is achieved using the setup shown in Figure 4.4**a**. After wirebonding, the sample is inserted in a height-adjustable dip

stick, and the sample is slowly submerged in liquid helium (T ≈ 4.2 K). The 8 x 2 wires in the stick allow a Kelvin connection (to account for the low resistance at low temperatures) to 4 junctions on the sample. If the sample is fully submerged, a current is applied to the device and the voltage is measured simultaneously. The resulting I-V-curve is shown in Figure 4.4**b**. The measurement starts at zero current and zero voltage. The current is increased and the voltage remains at zero up to the *critical current*. A more detailed description of the I-V-curve is given in section 7.1.2. The measurement setup used for this experiment is explained in more detail in the PhD thesis of Nico Himmel [Him15].

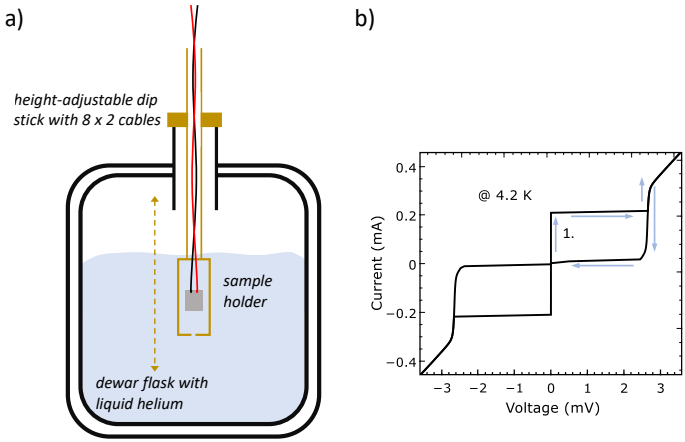


Figure 4.4: Low temperature setup and measurement result. **a** shows a schematic of the measurement setup used for measurements at 4 K **b** exemplary I-V-curve of an Nb/Al-Al_2O_3/Nb Josephson junction.

Chapter 5

Soft- and Hardware Development

This chapter describes the most important software and hardware developments to investigate different types of memristive devices for their future application in neuromorphic circuits.

> *The development of these tools was a major part of this thesis. Due to the length of the source code (10.000 lines of code), it is not included, but available on request.*

5.1 Electrical Measurements on Wafer-scale

Memristive devices are typically characterized with current-voltage measurements (see chapter 4.2). If the physics of the resistive switching of the devices is in focus, it is sufficient to analyze a few dozen devices. In order to implement the developed devices in neuromorphic applications, all the measurements are performed on wafer-scale on a large number of devices.

The general setup is shown in figure 5.1. The devices were contacted using probe heads (SUSS PH120) with electrically connected probe tips made out of tungsten. Several probe heads were mounted on a probe stage, contacting the wafer beneath them. The wafer is placed on a thermochuck (Temptronic TP03215A), which allowed temperature dependent measurements of the

devices under testing. This chuck is part of a semi-automatic probe station (SUSS PA150-II) with the ability to move the chuck in X, Y and Θ-direction.

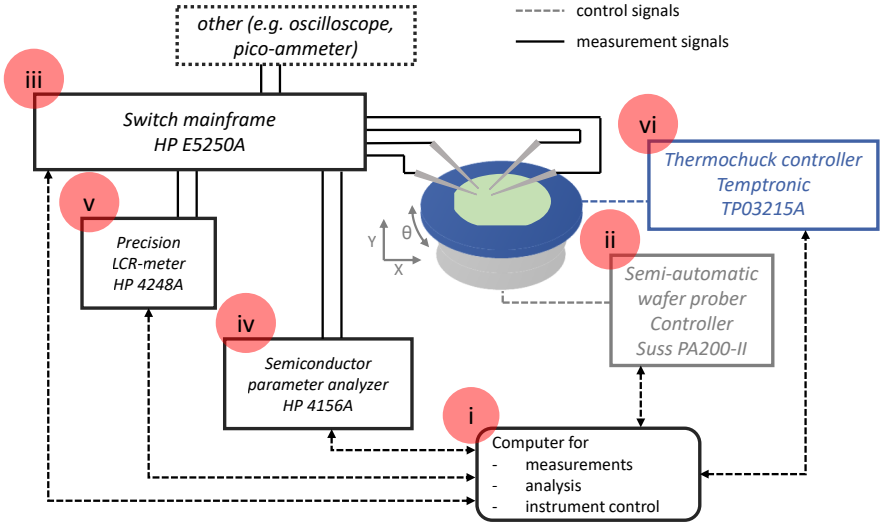


Figure 5.1: Schematic of the measurement setup established in this thesis. **i)** computer for instrument control and measurements; **ii)** semi-automatic wafer-prober from Suss, able to move wafer in X,Y and Θ direction; **iii)** switch mainframe from HP, connects different measurement instruments to the probe-heads; **iv)** parameter analyzer HP4156A, used for all I-V-measurements in this thesis; **v)** precision LCR-meter (HP4248A); **vi)** thermochuck from Temptronic, allows temperature dependent measurements ranging from room temperature to 200 degrees Celsius; Dashed lines show control lines for communication, solid black lines indicate electrical signals for measurements.

The probe heads are connected to a switch mainframe (HP E5250A), where input signals from various instruments could be connected to the device under testing.

Although all these devices were already available, they were not used to conduct automatic measurements. In fact, no measurement programs at all

existed for most devices. Due to huge number of similar measurements for every new wafer, it seemed reasonable to develop a measurement program that can address all these devices. With the help of this program, the measurement on wafer-scale was automated to a great extent, which reduced the time spent on repetitive tasks and to get statistically sound data.

For measurements and analysis, two programs were developed:

The first program is used to conduct several typical measurements on memristive devices, e.g. I(V), I(t), retention, or capacity measurements. It controls all connected devices using the well-established GPIB (General Purpose Information Bus) protocol. Figure 5.4 shows the possible procedures for the characterization of a wafer. A typical set of measurement tasks for the initial characterization of a new wafer included the following steps (see also Figure 5.2):

1. Measure the insulation resistance of the SiO passivation layer across the wafer (Figure 5.2a).
2. Measure the resistance of the memristive devices across the wafer (Figure 5.2b).
3. Conduct parameterized I-V-measurements with varying voltages for the set and reset polarity to find a suitable set of working parameters (Figure 5.2c).

These parameterized measurements turned out to be very helpful, because they enable an extensive and time-saving characterization. A typical set of measurements had the following properties: Besides the variation in set and reset voltage (Σ 23 measurements) the same parameters were sometimes applied to all 6 contact areas (Σ 138 measurements) at several (e.g. four) positions on the wafer (Σ 552 measurements). This task would have been a

matter of days when done manually - and is meaningful for *most* working wafers.

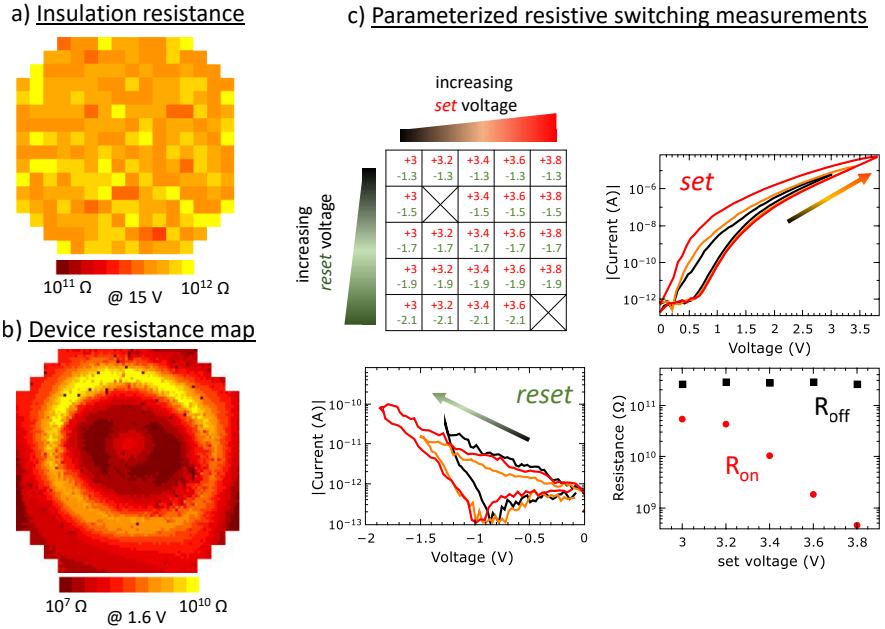


Figure 5.2: Typical automated measurements conducted on wafer-scale. **a** Measurement of the insulation resistance. **b** High resolution resistance map with color scale for the resistance. **c** Typical parametric resistive switching measurement to analyze the necessary voltages for set and reset.

Figure 5.3 describes in detail the program which was developed for the measurement of memristive devices.

i. Sample specific parameters, e.g. sample name, path for data storage and the currently selected device on the wafer.

ii. Selection of measurement (U-sweep, I-sweep, constant voltage, pulses, temperature, capacitance).

iii. General settings, e.g. current compliance, sweep rate.

iv. For batch measurements, this list contains the measurements to be conducted on wafer or cell level.

v. Each entry from iv. loads another list in this panel, which defines which actual measurements have to be conducted on the memristive devices. This includes most of the measurements described in ii.

vi. In the case of array or cell measurements, the applied voltages can vary for each device. These matrices define for every device the positive and negative voltage which is applied. This feature makes it possible to scan a broad parameter range on newly developed devices to automatically find the best parameters for resistive switching.

vii. Last measurements in linear scale.

viii. Last measurement in a logarithmic scale to show features in the low current range which are not visible in the linear scale.

ix. Logging output, which shows for example the current position on the wafer (in micrometers) or the success and failure of intermediate steps.

The batch procedure can be described with the flowchart in Figure 5.4. The upper level describes the list in Figure 5.3iv. Each line can define the type of the next measurement (wafer, cell) or adjust the temperature for subsequent measurements. The next step moves the wafer to the next position. The contact pads for top and bottom electrode are always connected using two micromanipulators each. This was deemed to be important in order to ensure a proper electrical contact. In order to properly create the contact, the switch matrix connected to the source measurement unit applies a voltage (10 V with a current compliance of 10 mA) across the tungsten needles first on the top electrode and afterwards on the bottom electrode. This creates a low-resistance connection to the top- and bottom electrode of the memristive device and was necessary because the electrical connection between needle and electrode is sometimes affected by the native oxide on the electrodes. Otherwise, the large series resistance leads to a major voltage drop and

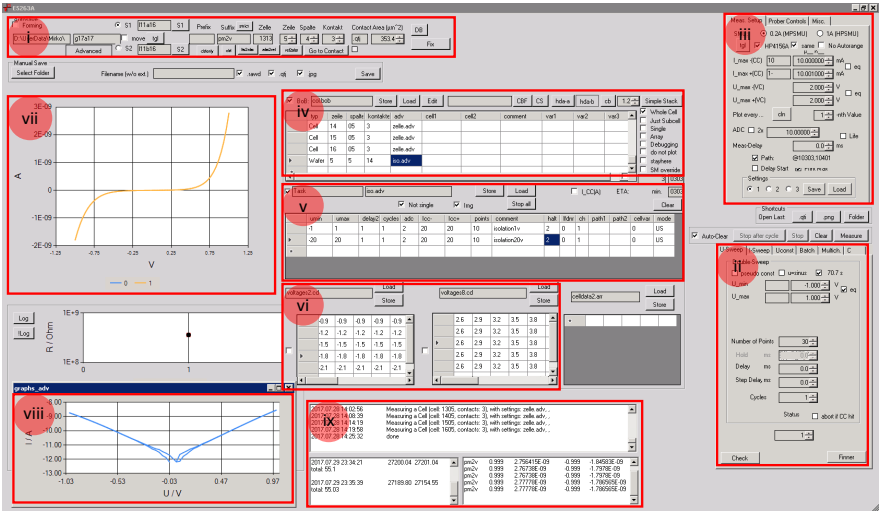


Figure 5.3: Program developed for the characterization of memristive devices. For a detailed description, see page 42.

consequently a smaller voltage across the device. Finally, the switch matrix connects the source measurement unit with the memristive device's top and bottom electrode. Afterwards, the individual measurement (see panel v. in Figure 5.3), is performed. Besides saving a) the data, b) the settings of the program and c) a picture of the measurement as separate files to the hard drive, the results are stored in a database for easier data management. If the measurements on the current device are completed, the next device on the wafer is selected and the procedure above is repeated. If the current task is completed (i.e. no more devices left to measure), the next task in the batch job is selected.

Occasionally, wafers with only minor differences (e.g. layer thickness, sputter power) were fabricated and a direct comparison (without unloading and changing the wafer) facilitated the analysis. In order to achieve this, the program was enhanced by the possibility to place two wafers on the

wafer prober and switch between wafers (a feature, which was actually not supported by the wafer prober itself).

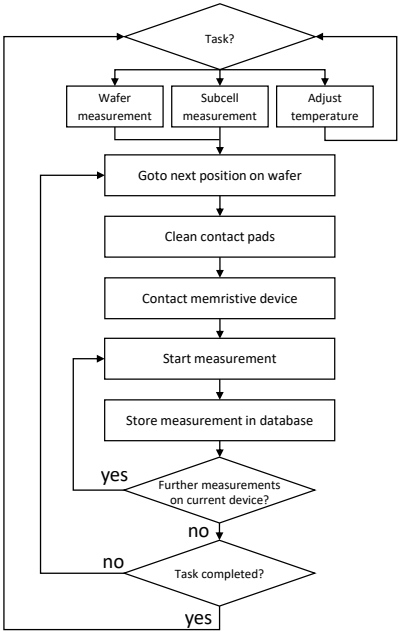


Figure 5.4: Program flow of a typical batch measurement, where several pre-programmed tasks are processed without further user input.

5.2 Graphical Analysis of Wafer Measurements

The analysis of individual measurements is typically performed using commonplace data analysis software (e.g. Origin, Qtiplot). This becomes difficult when measurements on full or parts of a wafer have to be analyzed, compared or post-processed because the amount of data and additional parameters like

the position on the wafer are not easily handled using these tools. It was thus necessary to develop a tool, which facilitates this specialized analysis. The second program uses the data which is stored in the database. With this program (*wafermap*, see Figure 5.5), all measurements in the database can be accessed and filtered (e.g. by sample name, type of measurement, additional comments etc.). Once a measurement is selected and loaded, a color representation of the resistance of each cell is drawn on a grid, representing the actual position of the wafer. Figure 5.5 shows a typical analysis conducted on a wafer with electrochemical metallization devices. The analysis starts with the selection of the measurement of interest (Figure 5.5 i). The example here shows five sets of measurements on wafer scale, which were conducted with different set and reset voltages on different contact sizes. The measurements opened for the individual contact sizes will be loaded from the database into the memory and stored in the working set of maps for comparison (ii). The corresponding map is shown in the center (iii). The color bar in this example was chosen appropriately to distinguish devices which successfully switched to the low resistance on-state (brown) and devices that remained in the high resistance off state. The parameters for the map visualization can be adjusted individually (iv) by changing the minimum and maximum resistance for the color bar. The upper plotting window (v) is used to compare a large number of devices (e.g. a column, row, or an arbitrary selection of devices) and compare the resistance at specific voltages. This example shows the on- and off-resistance of devices highlighted in blue on the map.

A direct comparison is possible with the lower plotting window, where I-V curves of the map are shown (by right-clicking on a device in the map). Important features can be highlighted using several useful charting options (e.g. linear scale, logarithmic scale). All curves can be easily copied for further post-processing in different applications. An important feature is that every copied curve is equipped with a unique identifier to trace the data back to the original measurement and measurement parameters. Different tools

were implemented to facilitate the analysis and comparison of individual or a complete set of devices, e.g. charting the resistance of cells row- and column-wise, visualize the change in on- and off-resistance across devices with different sweep parameters and plotting the I-V-curves for individual devices.

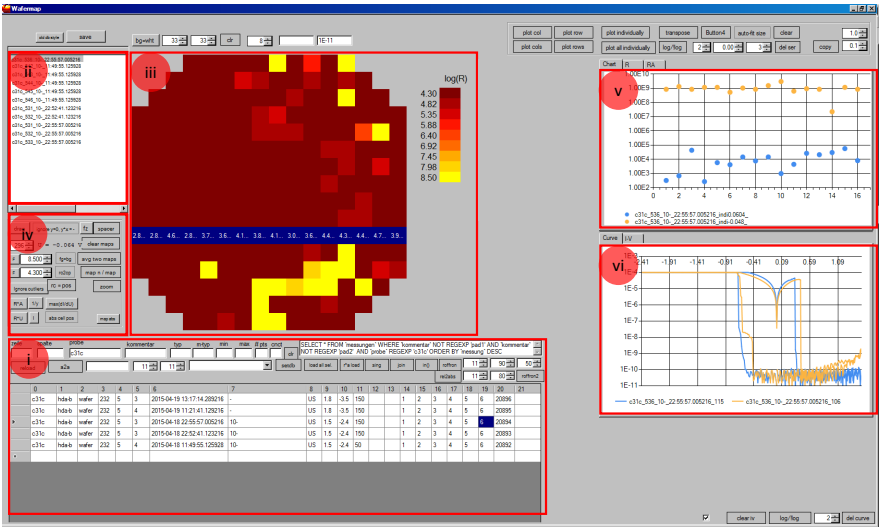


Figure 5.5: Wafer mapping software to analyze the wafer-level measurements; **i)** search panel for measurement selection, **ii)** list of currently loaded maps, **iii)** color representation of the active map, **iv)** parameters for map visualization , **v)** resistance of cells highlighted on the map, **vi)** I-V-measurements corresponding to devices on the map.

5.3 Multiplexing Circuit for Crossbar-Arrays

The development of more complex neuromorphic circuits requires a significantly larger number of memristive devices. If single devices would be used for this purpose, the number of connections increases linearly with the number of

devices – at least n+1 connections are required for n devices if one common connection for top or bottom electrode is used. For more than three devices, the wafer prober and the micromanipulators become unfeasible. Wirebonding (i.e. the semi-automatic creation of aluminum bond wires between sample and sample holder), on the other hand, allows to connect a significantly larger number of devices, although the number of connections is limited due to geometrical constraints between diced wafer and sample holder. For a reasonable number of devices, crossbar arrays have to be used (see Figure 3.3 on page 24). Due to the use of common top and bottom electrodes, n^2 devices can be connected using only 2n bond wires. For example, the 16×16 arrays consisting of 256 devices fabricated in this thesis thus only needed 32 connections, which is still feasible.

Another advantage lies in the connection between a neuromorphic circuit and the memristive devices. Although not suitable for all circuits, the individual selection of devices allows to design electronic circuits where different devices are connected to the same circuit (where the memristive devices serve as *memory*). An example for this kind of measurement is described in section 8.2.

Figure 5.6 shows the schematic setup for the characterization of crossbar arrays and the sample holder used to connect the crossbar array using a custom-made printed circuit board.

The control unit (Figure 5.6i) is a microcontoller connected to the measurement computer. The microcontroller receives commands from the computer, and is responsible to connect individual devices out of the 16×16 crossbar array. For each row and column, the specific electrode is electrically connected using low-resistance analog switches (Figure 5.6ii.). After the connection is established, a different set of analog switches (Figure 5.6iii.) selects the device needed to characterize the device (e.g. external source

measurement unit, on-board pulse generator and current measurement). The on-board pulse generator is able to generate time-variable pulses down to a few microseconds in length with different amplitudes. The operational amplifier (TL074A) serves two purposes: First of all, it serves as a buffer, which allows to source currents of several milliamps without distorting the pulse quality. Furthermore, the amplification of the applied voltage is controlled by the control unit. Using this configuration, it is possible to adjust the pulse amplitude for every applied pulse individually. The current is measured using an operational amplifier (LF356N) (Figure 5.6vi.) in transimpedance mode. In this configuration, the input of the opamp serves as a virtual ground and the output voltage is proportional to the input current, following the equation $U_{output} = R_{feedback} \times I_{input}$. Depending on the necessary current resolution, the voltage was either measured using an analog-to-digital converter IC with a 16 bit resolution or a bench-top multimeter (Agilent 34401A). With proper shielding, current measurements down to 50 pA were possible within some milliseconds. Figure 5.6vii shows the custom sample holders with a wirebonded crossbar array (Figure 5.6viii.).

This measurement setup was used during the characterization of crossbar arrays (see section 8 and during the development of the pattern recognition system in section 8.2.

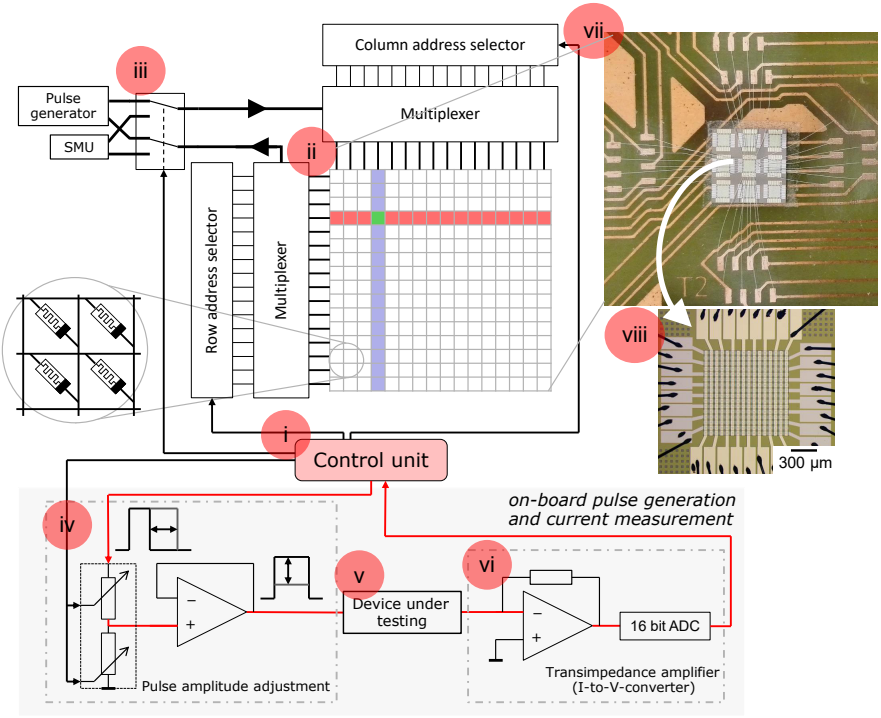
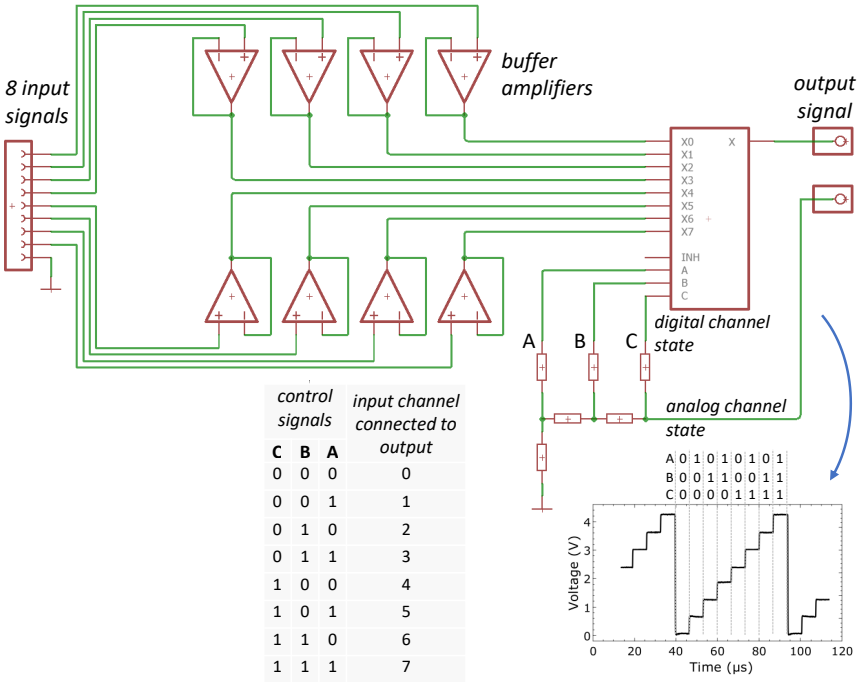


Figure 5.6: Setup for the characterization of crossbar arrays. **i)** Computer controlled microcontroller responsible for address selection and measurements, **ii)** multiplexers to create the connection to bottom / top electrode of the selected memristive device, **iii)** measurement device selection: externally connected source measurement unit or on-board pulse generation, **iv)** circuit for the creation of voltage pulses to read or set the device state (variable in time and amplitude, **v)** device under testing (i.e. the previously selected device in the crossbar array above), **iv)** current measurement using an I-to-V converter and subsequent voltage measurement, **vii)** custom made printed circuit board to connect one out of nine crossbar arrays on a 6.6 mm × 6.6 mm chip (taken from a 4 inch wafer), **viii)** wirebonded crossbar array.

5.4 Multi-channel Oscilloscope

The development of complex neuromorphic circuits is often accompanied with the need to acquire a large number of signals simultaneously in order to record the state of the network. If the signals would be only binary values, this could be achieved with logic analyzers. Since most of the signals of interest will have analog character, this would not be possible without a significant loss of information. Another problem was the limited record length of most multi-channel data acquisition systems. After careful consideration of commercially available (and financially feasible) devices, it was necessary to develop a new system, with a recording time from seconds to hours for many channels (e.g. 24). The biggest concern for high speed measurements is still the time necessary to transfer the data from the measurement device to a computer with a significantly larger memory. The initial trials (using a microcontroller with 80 Megasamples/second) were soon abandoned because timing issues with the USB protocol made reliable and continuous measurements impossible. The best alternative was a commercially available oscilloscope, which could be used with a custom software for data post-processing. For this purpose, a Picoscope 3403D was used because the software development kit from the manufacturer allowed to implement a streaming mode, which allowed the recording and simultaneous transfer to a computer. Oscilloscopes like that are typically only available up to eight channels. Therefore, it was necessary to develop a circuit, which would multiplex a number of channels using one channel from the oscilloscope. Afterwards, in software, the continuous stream of data would be de-multiplexed in order to regain the data for each input channel. Figure 5.7 shows the circuit necessary to record eight different signals using only one oscilloscope channel. On the left, the input signals are fed through operation amplifiers used as buffer amplifiers, to decouple the highly sensitive input signal from the noisy multiplexer stage.



control signals			input channel connected to output
C	B	A	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 5.7: Eight-to-one multiplexing circuit. The input signal is buffered by operational amplifiers to avoid distortions in the input signals. Depending on the digital input states (A,B,C) different input signals are fed through to the output. The selected channel is coded by the analog step-wave form and recorded for later channel de-coding.

The buffered signals are then connected to an 8-to-1 multiplexer. This multiplexer is controlled by three digital signals, where the binary numbers from "000" to "111" select which signal is routed to the output of the multiplexer. A microcontroller was used in order to apply these signals and thus iterate over all eight input channels. Although it might be possible to decode the channels using timing information of the microcontroller, this approach was abandoned to increase the robustness of the data acquisition. One possible alternative was to record the state of the digital signals which control the

multiplexer simultaneously. This was achieved using the resistor network shown in Figure 5.8. This resistor network (often called "resistor ladder") is a 3-bit DAC (digital-to-analog converter). The binary signals from "000" to "111" lead to the analog signal shown below the resistors. Each step represents the value of the digital signals. This makes it very simple to decode and split the continuous stream of signals into the individual channels.

This de-coding procedure is illustrated in Figure 5.8 in more detail. Figure 5.8a,b show the recorded oscilloscope data, which contains eight different input signals and the state of the digital control signals. The data from channel "1" and "4" are exemplarily decoded using the following procedure. The computer program separates the recorded data and collects all data points which belong to one step in the control signal waveform. The collected data is grouped into eight sub waveforms. These groups are identified by the voltage in the respective position in the control signal waveform. Each of these eight groups corresponds to one of the input signals in this time step. In this example, the signal recorded on channel 1 is the sine curve shown in Figure 5.8c.

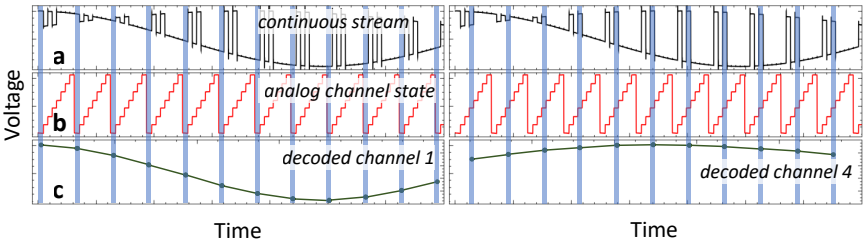


Figure 5.8: Exemplary decoding of two channels from the continuous stream of input signals. **a** Input stream containing the data of eight channels. **b** Step waveform necessary for the assignment of individual channels. **c** Exemplary decoding for channel 1 and channel 4. The corresponding section of the respective channel in the input data stream is highlighted by blue rectangles. The sampled values are indicated as green dots. These dots represent the decoded channel data.

Figure 5.9 shows how the input data is post-processed to minimize noise and artifacts induced by the multiplexing. It can be seen that transitions from large to small voltages (e.g. channel 1 is grounded and channel 2 has maximum voltage) induces large glitches (or ringing, highlighted by the blue circle) during the switching between the input channels. Without further post-processing, these distortions could render the output wave forms unusable.

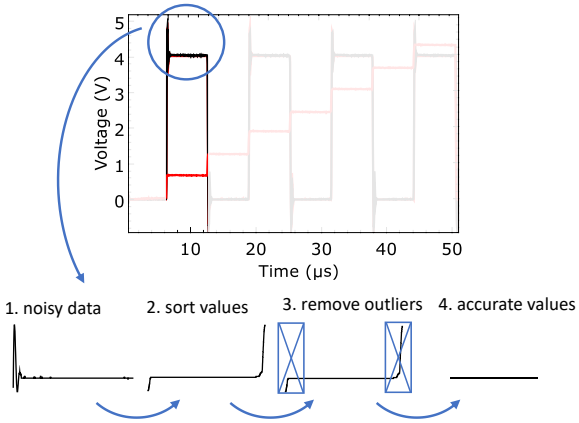


Figure 5.9: Signal disturbances induced by high voltage swings make a post-processing of the acquired data necessary. Highlighted in blue are glitches to be filtered.

In order to increase the signal quality, the first measurement after the channel was changed is always discarded. The remaining data is then sorted and afterwards (depending on the selected resolution of the measurement) the largest and smallest values are discarded as well. This procedure yielded a typical resolution of $\approx$ 10 bit.

The following two charts in Figure 5.10 show the possibilities of the developed measured setup. On the left hand side, a sine wave and a 25 microsecond

pulse were applied to the 24 channels of the setup. It can be seen that with a properly adjusted control signal waveform, rectangular pulses with 25 microsecond width can be recorded. Despite the large voltage swing (V_{pp} = 8 V), no distortions on other channels are visible. It should be emphasized that such short signals cannot be measured accurately, and only their existence is recorded. It is obvious that the sampling frequency needs to be larger than the signal frequency to accurately represent the input signal (Nyquist-Shannon sampling theorem).

An important requirement for this system is the long-term precision. To test the accuracy of the system, a 100 microsecond pulse was applied every 20 ms. In total, 4×10^9 byte ($\approx$ 37 GByte) were recorded with 4 million values per second and 24 input channels using a 4 channel oscilloscope. The timing difference shown in Figure 5.10b shows only deviations within the sampling window. If timing differences significantly longer or shorter than 20 ms would be observed, this would be an indicator for gaps in the data transmission. Since all values are within the sampling window, this setup is capable for long-term measurements, only limited by the computers hard drive space.

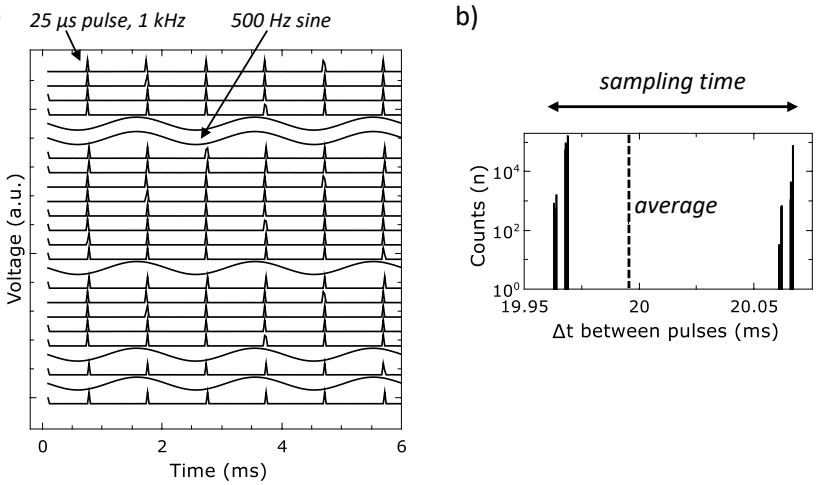


Figure 5.10: a) Exemplary measurement to show the highest resolution possible with this system. Using an arbitrary waveform generator, two signals were applied to various channels. The first signal is a 25 microsecond pulse with a frequency of 1 kHz and the second wave form is a sine wave with a frequency of 500 Hz (both amplitudes were $V_{pp} = 8$ V). Every pulse could be recorded and despite the large voltage swing the sine wave on neighboring signals was not distorted. **b**) Reliability measurement over 10000 seconds showed no missed signals.

Chapter 6

Filament-based Electrochemical Migration Cells

Complex neuromorphic circuits were first implemented by Carver Mead around 1990 to emulate neuro-biological processes using CMOS technology [Mea90, Mea89]. In recent years, the increased development of memristive devices for storage and memory applications has lead to an intensified interest to use these devices for neuromorphic circuits. The initial contributions were still focused on the development of devices with attractive properties. This included research on the materials which exhibit memristive properties and an increasing insight on the physical processes involved in the resistive switching. In recent years, the focus shifted towards first demonstrations of the emulation of neuro-biological properties [JKK+16]. These involved typically only few devices, but the trend grew towards circuits with a growing number of devices and an increasing complexity.

The aim of this thesis was the development of memristive devices with *analog* resistive switching. Nevertheless, it is reasonable to have a *toolbox* of devices to cover the broad range of neuromorphic applications with different requirements. Filament-based memristive devices using the migration of silver (electrochemical migration cells) were developed and characterized, because they offer properties which are nearly complementary to analog resistive switching. Among them, the resistance change over several orders of magnitude on a sub-millisecond timescale is probably the most important difference.

6.1 Resistive Switching Characterization

Memristive devices based on the migration of electrochemically active materials (e.g. silver or copper) are among the most studied devices [VWJK11]. As described in section 2.1.2.1, the switching mechanism in these devices is based on the high mobility of certain metal ions in an insulating matrix. Under an applied voltage, these ions drift through the insulator towards the adjacent counter electrode until a metallic filament is created between the electrodes. Since the main component is the mobility of metal ions, the requirements for the counter electrode and the insulating matrix are typically less demanding compared to other switching mechanisms. Dozens of material combinations show this behavior [LJKW12]. In the devices build in this thesis, the electrochemically active metal is silver; the insulator is Ti_xO_y and the counter electrode is aluminum. The material stack of the device is shown in Figure 6.1. Details on the fabrication are given in chapter 3. Aluminum as counter electrode is actually rather uncommon because typically inert materials like gold or platinum are preferred. When these devices were first fabricated, Gold was unavailable in the sputter system and had to be evaporated. Since the adhesion of evaporated Gold was insufficient, a different material was preferred. Nevertheless, no disadvantages were observed for aluminum during resistive switching.

Figure 6.2 shows a typical I-V curve for this type of device, in accordance to the literature [LJKW12, Sch09]. The voltage is decreased to -2.5 V; afterwards increased to 1.5 V and swept back to 0 V. The transition from the high resistance state to the low resistance state can be clearly observed around -0.6 V. At this point, the current increases rapidly to the previously programmed current compliance. This current limitation is necessary to avoid an uncontrolled increase in current, which could lead to a irreversible destruction of the device and to avoid a massive transport of silver into the insulator.

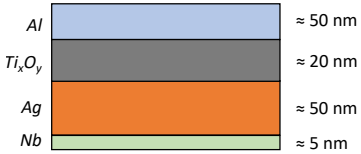


Figure 6.1: Schematic cross-section of the device material stack and approximate film thicknesses.

If the voltage is further increased, the ohmic conduction mechanism is still visible up to the point where the silver filament dissolves. This dissolution often occurs at a similar speed as the filament formation during the set process (i.e. within very few mV). After the filament is dissolved, the current is comparable to the initial current.

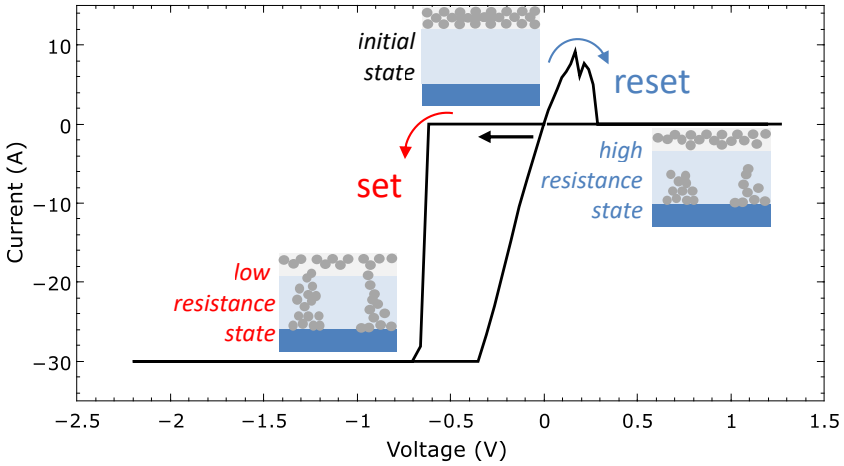


Figure 6.2: I-V curve measured on silver devices. The insets schematically show the filament growth during set (LRS) and reset (HRS). During the set process, the filament reaches the counter electrode and increases the current conduction. During reset, the filament is dissolved again.

6.1.1 Necessity of Electroforming

Figure 6.3 shows exemplary I-V-curves from two devices from the same wafer. The I-V curves on the left (6.3a) are from the initial cycle. The I-V-curves on the right (6.3b) show the second cycle. Interestingly, the first and second cycle for the first device look nearly identical. Device 2 shows significantly different behavior. Although the first increase in resistance occurs at a similar voltage ($\approx$ 0.9 V) as in device 1, the complete filament is only developed after $\approx$ -2 V. Similarly, the reset process requires multiple steps to reach the low resistance state. The second cycle on the other hand is comparable to device 1.

This observation indicates that this type of devices always needs an initialization step called electroforming before the final resistive switching properties are achieved. Although this procedure is necessary for most memristive devices [JSBW08, SWKW08, SMK$^+$09], it often leads to an unwanted parameter spread which might be problematic for a large-scale use [YMP$^+$09].

The difference in switching results from different properties of the sputtered layers. It was observed that the roughness of the deposited silver film varied in different parts of the wafer. AFM measurements of the silver bottom electrode revealed a rather high roughness ($R_{RMS} \approx$ 3-6 nm). This is large compared to other electrodes used in this thesis (Nb and Al: $R_{RMS} \approx 0.5$ nm). Figure 6.4a shows schematically the influence of an increased electrode roughness. The scale bars indicate the vertical ("thickness") and horizontal ("width") dimensions. It is obvious that this roughness decreases the effective insulator thickness, and the field strength is not homogeneous across the junction. During bias application, the electric field in the insulator will be maximized at these silver spikes. The field induced drift is most likely to start at these points of increased field strength. The different voltages observed

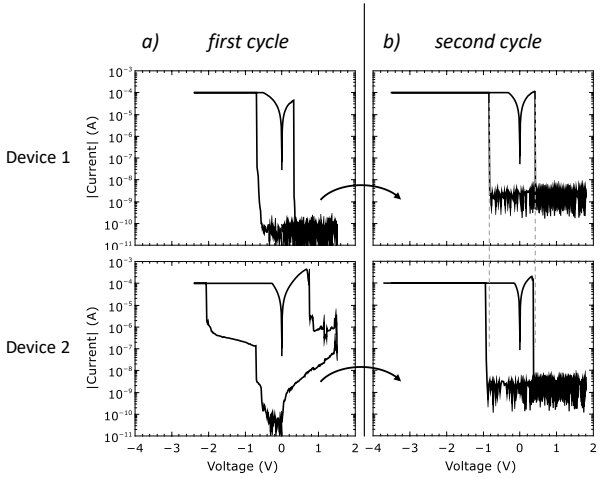


Figure 6.3: Necessity of electroforming. **a** Two initial I-V curves from different parts of the wafer differ significantly in set and reset behavior. **b** The following cycles show nearly identical characteristics. This emphasizes the necessity of an electroforming step.

for the on-set of switching can be easily explained by even minor variations in surface properties of the silver electrode (e.g. maximum deviation from the mean thickness, densities of spike or roughness in general).

Another observation points towards the silver roughness being the decisive parameter for the resistive switching. In order to test this hypothesis, the stack was inverted and aluminum was used as the bottom electrode and silver was used as the top electrode. Figure 6.4 b shows the schematic stack and the resulting roughness. Due to the lower surface roughness, the field strength in the insulator is smaller. Compared to the silver bottom electrode, the missing nucleation sites decrease the propability of filament generation. Indeed these devices did not show the characteristic switching behavior for filament growth. This theory is supported by a recent paper from You et

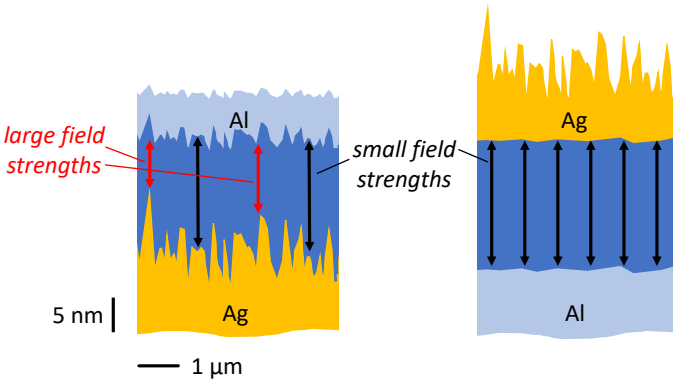


Figure 6.4: Schematic cross-section of two material stacks with silver electrodes. **a** The roughness of the bottom silver electrode decreases the effective insulator thickness. The decreased insulator thickness creates places with an increased field strength, where silver migration is likely to occur first. The roughness is adapted from an AFM measurement of sputtered silver thin films. **b** For silver top electrodes, on the other hand, the silver roughness does not influence the resistive switching because the important interfaces are smooth.

al. [YKJ+16], where the insulator was deliberately patterned. The aim was a decrease in the effective insulator thickness which create predefined nucleation sites for the subsequent deposition of silver. This significantly reduced the variation in on- and off-resistance and operating voltage.

6.1.2 Endurance

The use of memristive devices in any application requires a certain switching endurance. Memristive devices for memory applications are often required to switch 10^9 times [WDSS09b]. The requirements for a neuromorphic application are typically assumed to be less demanding which means that fewer cycles are sufficient. In order to get an idea of the endurance of this

device, 1000 I-V-sweeps were continuously measured. Figure 6.5a shows the on- and off current for each cycle. Despite some minor variations in the off-current (around cycle 100), the device was always able to switch into the high and low resistance state. The quality of the device is emphasized by Figure 6.5b, which shows the distribution of set voltages for all cycles. This shows that the set process occurred at nearly the same voltage of ≈ 0.6-0.7 V.

Since these devices can severely degrade with prolonged use, it is not sufficient to quantitatively analyze the on- and off-state and the set voltage. Figure 6.5c shows the first, 500th and 1000th I-V curve. This can be considered another hint for a high quality device because it did not suffer from switching induced fatigue.

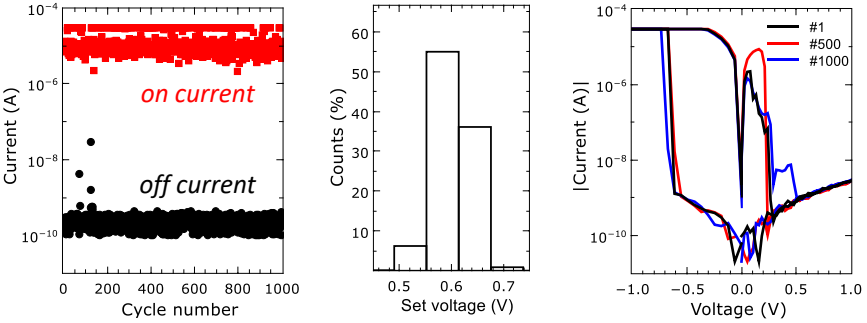


Figure 6.5: Performance of a silver device over 1000 cycles. **a** On- and off current in dependence of cycle number. Besides some minor variations in off state current, every cycle was successfully set and reset. **b** Histogram of the set voltages showing the very low variance and high reproducibility (sweep rates: 1.8 V/s (negative voltages) and 0.9 V/s (positive voltages)) **c** First, 500th and 1000th cycle show that the switching behavior did not undergo significant changes (no fatigue).

6.1.3 Multilevel Ability

The results up till now indicate that these devices would only show binary switching between two states. This would extremely limit their usability in neuromorphic circuits. Although it is not possible to achieve a truly analog resistive switching, it is possible to operate electrochemical migration devices with different on-resistances [Sch09]. Figure 6.6 shows how the on-resistance can be modulated by choosing different values for the current compliance. This chart shows the strong dependence between the on-resistance and the current compliance leading to a straight line in the double logarithmic plot. This happens in accordance to the previously mentioned need for the current compliance itself (i.e. current compliance necessary to limit the amount of silver introduced into the insulator). This variability in on-resistance can be explained by either the number of created filaments or by the strength (width) of the filaments.

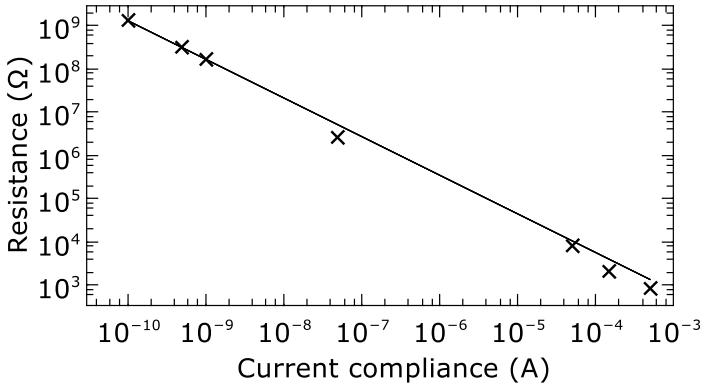


Figure 6.6: Even if a switching process shows binary characteristics, multilevel on-states can be generated by using different current compliances during set.

6.1.4 Switching Capability on Wafer Level

An essential requirement for the large-scale integration of memristive devices is the yield, i.e. the percentage of devices that actually work. This requires a successful fabrication on wafer-level, which is difficult with most unoptimized deposition systems. To investigate the switching capability on wafer level, one device of every 5 mm×5 mm cell was measured (in total 232 devices). This is schematically shown in the upper right part of Figure 6.7.

For each device, the voltage was swept between -2.5 V and 1.5 V. The maps in Figure 6.7 illustrates the high quality of the fabricated devices, and show the resistance in the initial state (map A), after the set process (map B) and after the reset process (map C). The color bar indicates the resistance of each cell and is the same for all three maps. Bright colors represent large resistances, whereas darker colors indicate small resistances.

The homogeneity of the first map is an indicator for the fabrication quality because 96 % of all devices have a high resistance in the beginning. The large initial resistance is a result of the thick titanium oxide insulator separating the top and bottom electrode. The most trivial reason, problems with the SiO insulator, can be ruled out because all defective devices showed at least some kind of resistive switching under applied voltage. More probable is a deviation in the actual film properties, either by migration of silver during the fabrication or due to small particles on the wafer prior to the deposition of the multilayer.

The second map shows the resistance of the devices at -2.4 V. Due to the use of a current compliance, every device should have the same current. This is not the case, and only $\approx$ 91 % of the devices reached the current compliance. This might be avoided by choosing a larger set voltage, even

though the current voltage was sufficient for most devices independent of the position on the wafer.

The last map shows the resistance after the reset procedure. In the best case, every device would exhibit again a large resistance (bright color). Some devices ($\approx$ 20 %) were not properly reset and remained in a low resistance state. This could have been avoided by a larger reset voltage for these devices, which, however, may have destroyed other – properly working – devices on the wafer.

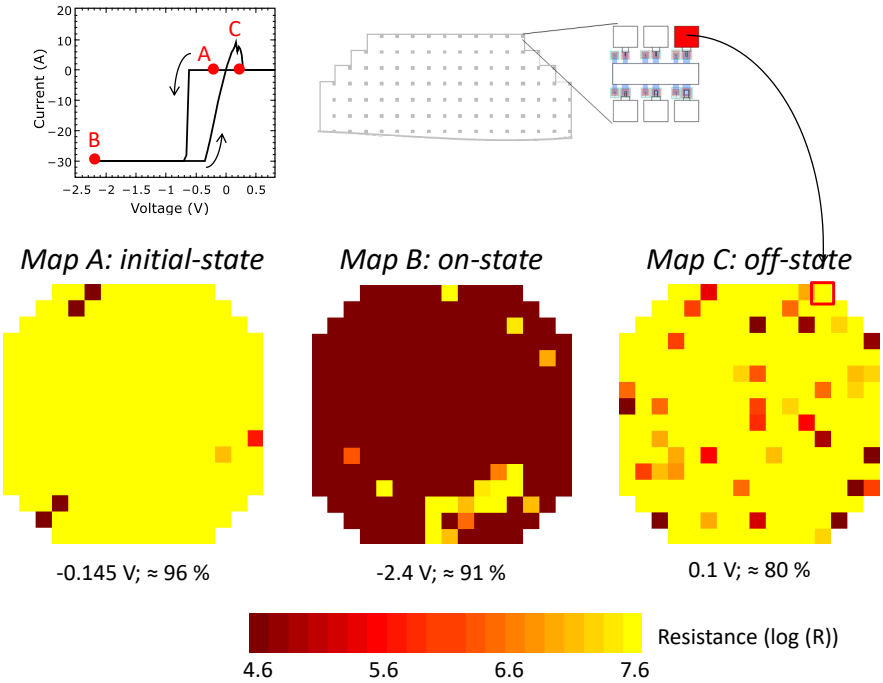


Figure 6.7: Set and reset applied to 232 devices across the wafer. Map A: Initial resistance at -0.145 V. Dark points indicate small problems during the fabrication process. Map B: Resistance measured at -2.4 V in the on-state. Devices with bright colors failed to reach the current compliance and were thus unable to switch to the low resistance state. Map C: Off-resistance measured at 0.1 V after reset. Devices that failed to change from dark color in the previous map to a bright color in this map were unable to switch back to the off-state.

6.1.5 Switching Speed

Although the switching speed of memristive devices is typically not considered to be very important for neuromorphic applications, it is interesting to characterize and compare it with similar ECM devices. It is very difficult

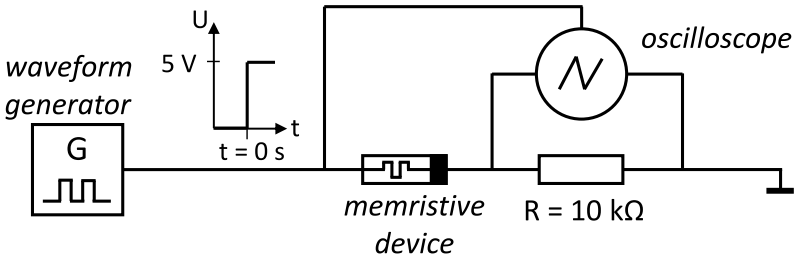


Figure 6.8: Setup for the measurement of the switching speed. The waveform generator outputs a 5 V pulse and most of the voltage initially drops across the memristive device. After switching, most of the voltage drops across the resistor and allows the use of an oscilloscope to record the onset of the switching.

to measure the switching speed using I-V curves, because the measurement speed for low currents typically takes at least several milliseconds. Thus, a different setup had to be designed in order to achieve a highly accurate time measurement. Since the absolute value of the current is not of interest, the voltage divider in Figure 6.8 can be used to measure the change of the on- and off-state. The voltage across the resistor is nearly zero for the high resistance state of the memristor and nearly the applied voltage when the device is in the low resistance state. This can be easily explained by the large change in resistance. In the off-state, the resistance of the memristive device is $\approx 10^5$ times larger than the resistor while it is ≈ 100 times smaller in the on-state. The voltage across the resistor is measured using an oscilloscope (Picoscope 3403D) with nanosecond resolution. Nevertheless, the measurements only indicate the maximum time because the set-up was not optimized for high-speed (e.g. no active probes).

Figure 6.9 shows voltage-time measurements for two devices with slightly different behavior: The upper curves show the initial transition from the off to the on-state. The lower curves show the recorded voltage when the devices are already in the on-state. In both cases, the applied voltage (black) and the

voltage across the resistor (red), are in the beginning ≈ 0 V. After the voltage is applied to the circuit, a delay of up to ≈ 3 microseconds was observed until the voltage across the resistor increased sharply, indicating that the device changed from the off- to the on-state. This shows that the total time for the formation of a filament has to be in the order of ≈ 3 microseconds. Of all devices measured, about half of them was able to turn on within (225 +/- 20) ns, while the other half needed about (3000 +/- 280) ns. All devices were in close vicinity on the wafer, and no device was switched previously. The huge discrepancy in the switching time probably further motivates the necessity of electroforming, similarly to Figure 6.3. The inset shows the device current before and after switching. This indicates that the filament formation is able to decrease the device resistance within 3 microseconds by ≈ 8 orders of magnitude. Considering the limitations of the measurement setup, the values are comparable to similar electrochemical metallization devices, where switching times in the order of ≈ 100 ns were observed [KPM05, Sch09].

The lower curves show the voltage development across the resistor for a device that was previously formed. Interestingly, the on-state measurements do not differ significantly neither in absolute resistance (i.e. measured voltage across the resistor) nor in shape.

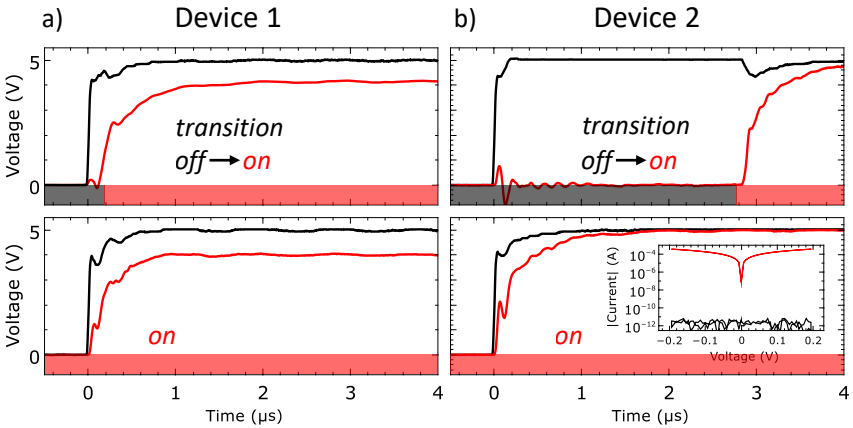


Figure 6.9: Two exemplary measurements of the onset of switching with different timings. **a** The upper images show the different times necessary for two devices. The gray and red bars above the time scale indicate the individual state. These curves show typical switching times and nearly all devices were able to switch within few microseconds. **b** Although the switching time was different, the device response is nearly identical when in the on-state.

6.2 Application: Electronic Implementation of Anticipation

Silver migration cells are important devices for neuromorphic applications that require a huge change in resistance. An important part of these applications include the electrical *emulation* of bio-inspired examples. An interesting candidate is the anticipation behavior observed in unicellular amoeba, which will be electrically emulated in this section.

Amoeba are single cellular organisms. Due to their simplicity, they attracted the attention for neuromorphic applications, because even though they have no nervous system, they show basic "intelligent" behavior. It can search for food if the ambient conditions are favorable (i.e. warm and humid), but if the conditions change from a warm and humid to a cold and dry environment, their movement stops.

6.2.1 Biologic Experiment

Saigusa et al. investigated the behavior of ameobas under alternating favorable and unfavorable conditions [STNK08]. In their experiment, the conditions are initially favorable and the amoeba has a constant speed. After the speed stabilized, short periods of unfavorable and favorable conditions were alternated, and the amoeba stopped and continued its movement accordingly (see Figure 6.10, feature #1). Interestingly, the movement of the amoeba slowed down when a change in conditions was supposed to happen, but did not occur (feature #2). Even after a prolonged time with constant ambient conditions, a single change in conditions (feature #3) was sufficient to induce once more the periodic response of the amoeba (feature #4). This

indicates, according to Saigusa et al., that the amoeba is able to learn and *anticipate* the periodic changes.

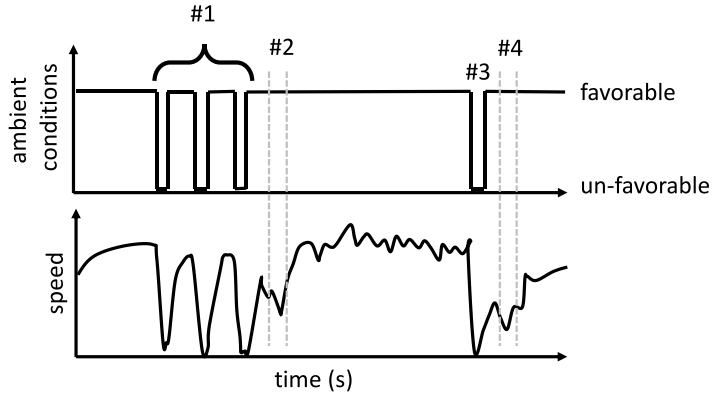


Figure 6.10: Adaptation of the biological experiment to analyze the speed of amoeba depending on ambient conditions. Drastic changes in the ambient conditions lead to a decrease of the amoeba's speed. Interestingly, the periodic changes in conditions later on were anticipated by the amoeba and it slowed down even when no change in conditions occurred. [STNK08]

6.2.2 Electronic Circuit

Pershin and Di Ventra proposed an electronic circuit with a memristive device, which emulates the amoeba's behavior under alternating conditions. The circuit shown in Figure 6.11 is similar to the proposed circuit, except for some adjustments which were necessary to realize the experiment using filament-based memristive devices [PLFDV09]. Besides adjustments to the capacitor and inductor values, a resistor was placed in series to the memristive device in order to act as a current compliance and to facilitate the measurement. With this additional resistor, it was possible to record the set process of the memristive device using only an oscilloscope.

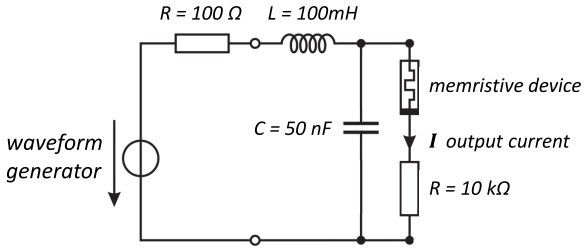


Figure 6.11: Experimental adaption of the proposed circuit to mimic amoeba anticipation using memristive devices [PLFDV09]. Initially, the memristive device is in the high resistance state and the circuit operates like an almost ideal RLC resonance circuit. If the circuit is excited in resonance, the induced voltage leads to a set of the memristive device and to a shift in the resonance frequency.

6.2.3 Electronic Experiment

Figures 6.12 and 6.13 show the experimental results of the electronic emulation of amoeba anticipation, which were conducted in accordance to the biological and the simulated amoeba response. It can be seen that the characteristic features are similar to the above description.

Figure 6.12 shows the excitation in resonance, and it can be clearly seen that the voltage in the circuit increases with each applied voltage pulse. The memristive device is initially in the high resistance state, and the circuit behaves like a lossy resonance circuit. During the application of the third pulse, the voltage increased sufficiently to set the memristive device. This change in resistance changes the impedance of the capacitor branch, which leads to a changed resonance frequency of the system. This explains why the single pulse later-on leads to "anticipated" events, i.e. a current through the memristive device.

For comparison, Figure 6.13 shows the out-of-phase scenario. Due to the out-of-phase excitation, the voltage in the resonance circuit does not increase sufficiently to decrease the resistance of the memristive device. It can be seen, that the following single subsequent pulse does not lead to the "anticipation" of further changes.

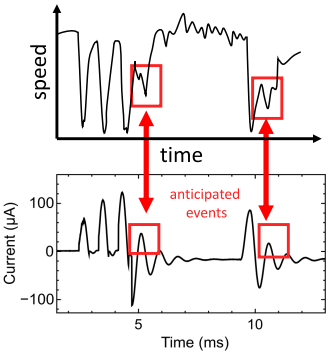


Figure 6.12: Periodic input signal and amoeba response. If a periodic input signal is applied to the circuit, the voltage increases with every pulse and is thus sufficient to set the device. The anticipated events, highlighted by red rectangles, are currents without corresponding input signal (i.e. a response of the resonance circuit).

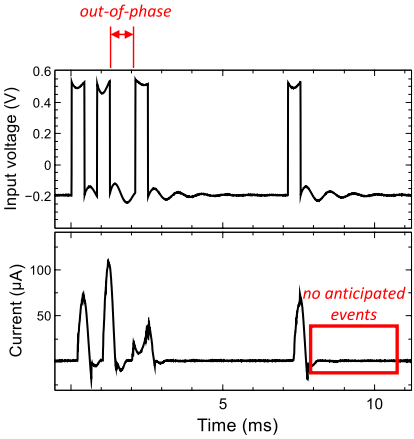


Figure 6.13: Aperiodic input signal and the system response. Unlike the periodic excitation, the missing increase in voltage does not set the memristive device and thus no events are "anticipated".

Chapter 7

Interface-based Memristive Devices

Section 6 dealt with a filament-based memristive device with pronounced on and off states. The aim of this section is to develop a memristive device with completely different resistive switching characteristics, e.g. analog vs. digital switching. This section will discuss the relevant components and requirements to yield memristive devices with an interface-based switching mechanism.

The beginning of this section describes the requirements, which have to be fulfilled in order to achieve interface-based switching. This includes, for example, specific film properties like the interface roughness or layer thickness. The transition from the first (barely working) devices towards high quality devices and the underlying implications will be discussed. Afterwards, these working devices are characterized extensively.

7.1 Towards Electroforming-Free Memristive Devices

7.1.1 Requirements

This chapter describes the development of memristive devices for neuromorphic applications. According to the requirements for this application discussed in section 2.3.2, the following properties are of interest:

(i) analog, multi-level switching
(ii) no electroforming necessary
(iii) high resistance

As shown in section 6, requirements (i) and (ii) are difficult to fulfill with filament-based devices. Although it was possible to operate electrochemical metallization cells with a variable on-resistance (see Figure 6.6 in chapter 6.1.3), this was only possible due to an externally controlled current compliance, which is difficult to realize in a neuromorphic circuit without significant overhead. Even if this could be done using additional circuitry, the rapid change in resistance makes it very hard to achieve real analog switching, where the resistance increases or decreases with every reset or set pulse.

Interface-based memristive devices are considered to be more suitable for this purpose, because the number of *states* the devices have (e.g. the different resistances that can be obtained between a minimum and maximum resistance) is very large. [Saw08, WDSS09a] The choice of switching mechanism was thus narrowed down to interface-based devices. Figure 7.1 shows the minimal configuration of such a memristive device, consisting of the bottom electrode, a highly resistive semiconductor/insulator and the top electrode.

Without further requirements or properties, these layers can consist of nearly any material.

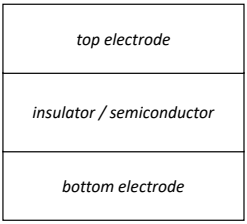


Figure 7.1: Schematic stack with the minimum number of required material layers.

High electrical field strengths are necessary to move, for example, oxygen ions and consequently, the memristive layers have to be thin, because the breakdown field strengths decreases for thicker layers [Lom50]. This requires a bottom electrode with a very small surface roughness to reduce the variation in electric field across the device (the impact of a large interface roughness has been discussed in section 6.1.1 in more detail). Figure 7.2 shows the enhanced schematic stack, where the thin insulator and the low interface roughness of the bottom electrode are highlighted.

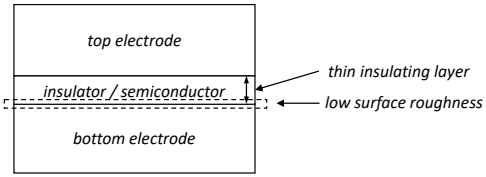


Figure 7.2: Enhanced schematic stack indicating important layer properties. For thin oxides a low interface roughness is essential in order to avoid unwanted, in-homogeneous, effects.

The interface roughness of most materials can be changed by adjusting sputter deposition parameters [JSLJ03, HDL99, LGMT03]. This time con-

suming step was avoided by choosing a multilayer of two materials, which intrinsically has a low interface roughness [RGG81, GWH83]: The deposition of a thin layer of aluminum on top of niobium leads to a) a complete wetting of niobium by aluminum, and b) a smaller surface roughness by smoothing the rough surface of the niobium [IH91]. Another beneficial property is adapted from the fabrication of Josephson junctions, where multilayer $Nb/Al/Al_2O_3$ stacks are used to deposit niobium-rich bottom electrodes (e.g. total Nb thickness of 200 nm) with a low interface roughness. Although the aluminum smoothes the niobium roughness, the columnar growth of the niobium still could propagate from bottom to top [IH91]. This is avoided by slightly oxidizing the aluminum, leading to an amorphous inter-layer which prevents the propagation of the previous crystal growth orientation.

The use of a tunneling barrier in a memristive devices is furthermore motivated in section 2.2.1.

The choice of the top electrode was more difficult. Resistive switching with a broad range of different physical mechanisms can be observed with reactive and inert metals [WDSS09a]. Initial trials with aluminum, titanium and niobium led to problems induced by artifacts generated during etching (e.g. etching induced parasitic conduction paths, see section 3.4 for a detailed description of the observed artifacts). A top electrode was thus wanted, which could be easily etched without the need for hazardous chemicals. Gold was an optimal choice, because it can be etched reproducible with a reasonable etching rate using, for example, potassium iodide. The corresponding schematic material stack is illustrated in Figure 7.3.

The last remaining requirement is the analog, or multilevel switching ability. This requires an insulating material that allows changes in its electrical properties with low effort (i.e. energy). Good candidates are transition metal oxides, which are extensively used in memristive devices due to their huge

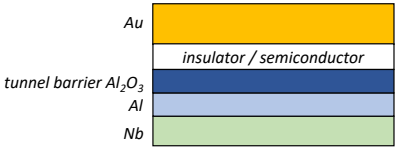


Figure 7.3: Schematic stack of the memristive device to be fabricated with all requirements up to now. The only material missing is the oxide.

bandwidth of suboxides [YSS13b]. Several (transition) metal oxides were studied, which will be discussed extensively in sections 7.1.3 and 7.2. Before, the properties of the individual components of the memristive device will be discussed in the next sections in detail.

7.1.2 Tunnel Barrier Characterization

An important step before the fabrication of memristive devices was to ensure the functionality of the tunneling barrier. Figure 7.4a shows schematically the tunnel junctions used here. In order to get the typical Nb/Al-Al_2O_3/Nb superconductor - insulator - superconductor (SIS) Josephson junction [LGGB91, RGG81, GWH83], no metal oxide is deposited and niobium was used as the top electrode. Apart from these differences, all other parameters (e.g. mask layout, fabrication steps etc.) are identical.

In the devices fabricated here, several aspects are different compared to highly optimized Josephson junctions. First of all, the thickness of the bottom electrode is significantly smaller ($\approx$ 40 nm) compared to typical niobium SIS junctions (160 nm [RSM$^+$15] - 200 nm [MSS$^+$85]). These thick niobium electrodes are necessary for the superconducting properties of the junction, and are not of importance for the memristive devices. The thickness of the bottom electrode was chosen as small as possible to reduce the probability of

insulation problems of the evaporated SiO layer, which separates top and bottom electrode.

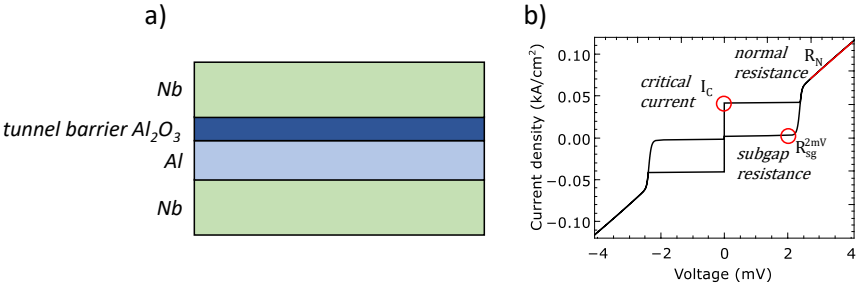


Figure 7.4: Characterization of aluminumoxide Josephson junctions. **a** Schematic of a superconducting Josephson junction. **b** I-V-measurement conducted while the sample is immersed in liquid helium (at T = 4.2 K). The highlighted parts indicate important parameters typically used to quantitatively compare Josephson junctions (normal resistance, critical current and sub-gap resistance).

Furthermore, the tunneling barrier used here was not optimized for large critical currents. This is typically achieved by using thinner barriers, which are, however, prone to pinholes (short-circuits in the tunnel barrier) [Him15] and not necessary for the resistive switching.

In order to analyze the quality of the Josephson junction, I-V-measurements were conducted at a temperature of 4 K (Figure 7.4b). Despite the not optimized parameters, the resulting junctions show the expected behavior. Two common figures of merit, like the V_m (subgap resistance – critical current product) and $I_C R_N$ (critical current – normal resistance product), indicate that the devices are high quality tunneling junctions. Similar values were

found during previous investigations [GWH83]. The individual values were taken from the curve in Fig. 7.4b at the respective positions.

$$V_m = I_C \cdot R^{2mV} = 27.6mV \quad \text{and} \quad I_C \cdot R_N \approx 1.5mV \tag{7.1}$$

Another possibility to analyze the tunnel junction is anodization spectroscopy (explained in more details in section 4.1.2). It has been used extensively to characterize superconducting tunnel junctions, because important properties of these junctions can be analyzed with a simplified sample preparation at room temperature. This avoids the time consuming fabrication of electrical junctions and the cumbersome analysis at low temperatures.

Figure 7.5 shows an anodization spectrum of a Josephson junction. Since the anodization front propagates from top to bottom, the spectrum starts with the niobium top electrode. The spectrum indicates schematically the corresponding layers with their individual thickness. Three distinct features are indicative for the quality of the junction and will be later of interest for comparison with anodization spectra of devices with memristive oxide layer. The anodization starts at the Nb top electrode and reaches at $\approx$ 12 V the Al_2O_3-layer (feature #1). The anodization rate increases sharply, because the anodization front passes a layer that is already oxidized. The decrease in anodization rate stems from the transition from the Al_2O_3 to the Al-layer and reaches the rate for bulk aluminum. The following second peak (at U $\approx$ 22 V, feature #2) and the immediate dip below the anodization rate of bulk niobium (feature #3) indicates the transition from the aluminum to the niobium layer. [IH89, RGG81]

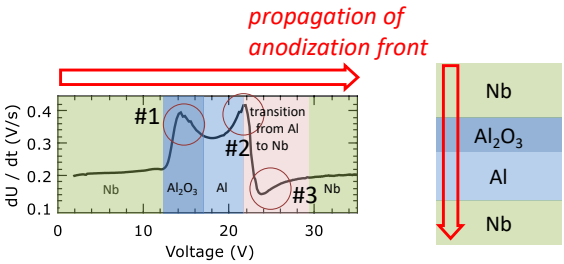


Figure 7.5: Anodization spectrum showing the stack used for the here fabricated Josephson junctions. The anodization front propagates from top to bottom through the layers.

7.1.3 Titanium-oxide Based Memristive Devices

As discussed in section 2.2.1, moving ions in a bulk material or at an interface can be used to change energy barriers. The resulting change in resistance offers interesting possibilities for memristive devices. Figure 7.6a shows the stack of a device, consisting of a tunneling barrier and a semiconducting titanium oxide layer as memristive layers. Titanium oxide was used because it is among the most common materials used in memristive devices, and was thus considered to be a good candidate for the first devices. [JLRC10, JKLC11, ZLG+11]

Figure 7.6b shows a resistance map of the wafer, which was recorded similarly to Figure 6.7 in section 6.1.4. The devices show a drastic variation in resistance across the wafer with a radial symmetry, which indicates that the deposition of the Ti_xO_y by reactive sputtering does not lead to devices with a homogeneous resistance. Considering that the film thickness is largest in the center of a wafer (at least for the sputter guns used here), it is surprising that the resistance is lowest in the center, while the resistance is largest at the border of the wafer. The exact reason remains currently unclear because most studies on memristive devices and reactively sputtered oxides typically do not show such detailed characteristics across a complete wafer.

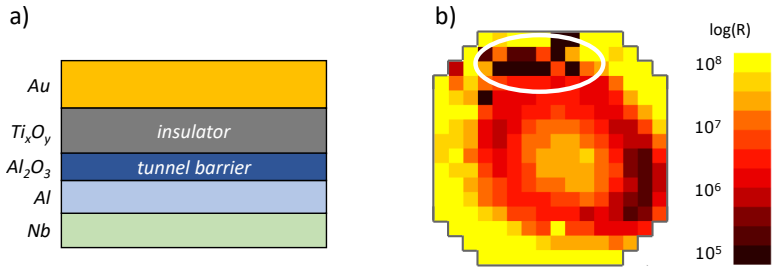


Figure 7.6: Properties of the $Al_2O_3/Ti_xO_y/Au$ device. **a** Schematic device cross-section **b** Resistance map showing the variation across the wafer. The colors indicate the resistance of the devices. Encircled in white are defective devices (low resistance), which indicates a problem during fabrication.

After the general resistance distribution was investigated, the resistive switching properties of these devices were investigated. Exemplary I-V curves of this type of device are shown in Figure 7.7. The voltage applied to the device starts at 0 V and is decreased to ≈ -2 V. Afterwards, the voltage is increased again up to 1.8 V and back to 0 V. The set process happens in the negative branch, visible in the increased current on the way back to 0 V. Accordingly, the reset process is supposed to happen in the positive branch. Since no decrease in current can be observed for positive voltages, the device is not able to revert the resistance back to its initial state.

These curves show a change in resistance of about a factor of ten. Interestingly, the resistive switching showed the same *irreversible* change in resistance across all contact sizes for a given set voltage (-2 V). This can be visualized by plotting the resistance × area product (Figure 7.7). In most devices, this leads to a horizontal line at least for the initial, as-deposited, state. After switching to the on-state, however, it becomes a line with a slope > 0 because one or more filaments are generated and the on-resistance is nearly the same for all contact areas. [VWJK11, XLS+08]

For this device, the resistance × area product also shows a straight horizontal line in *the on-state*. This leads to the conclusion, that not a single filament was generated (which is still, although not undisputed [DZH+15], assumed to be the most probable scenario for filament-based devices [WDSS09a]). Since a single filament can be ruled out, two possibilities remain: There might be either a certain distribution of filaments across the device (e.g. a constant filament density expressed in filaments per square-micrometer) or the change in resistance occurs homogeneously across the device.

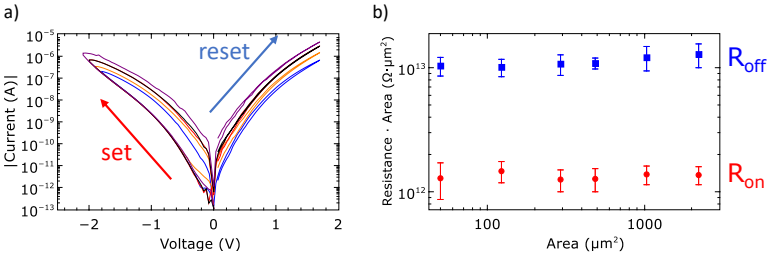


Figure 7.7: a I-V-curves to investigate the voltage-dependent memristive properties. The resistance decreases for negative voltages, but no resistance increase is observed for positive voltages. **b** The resistance × area product indicates that the observed change in resistance occurred homogeneously. The blue squares represent the initial state, whereas the red squares represent the irreversible on state.

Summarizing the results of this type of device, it was possible to change the resistance of the device under applied bias as intended. Furthermore, the resistance × area plot indicates that probably no filaments are involved. Nevertheless, it was impossible to reset these devices.

The question arose which internal properties of the device had to be changed in order to develop fully functional resistive switching devices. It can be imagined that the integration of highly mobile materials into the titanium oxide could lead to a resistive switching with reversible characteristic, because the necessary voltage to induce a drift of these ions would be significantly

lower than the voltage needed here to change the titanium oxide. The comparatively low voltages necessary to move ions in insulating materials was described in section 6. Considering the electrochemical metallization devices described in chapter 6, the material of choice is silver.

For the purpose of this new device, the possibility of filament formation has to be ruled out, without complicated modifications of the silver properties itself. The silver ions used to generate the filament in ECM cells are removed from the silver electrode, which is normally larger than the insulating oxide and thus acts as a sufficiently large reservoir. Consequently, a simple method to avoid the filament formation is to reduce the available amount of silver down to an amount which is insufficient to create a filament.

It is well-known that the wettability of silver is highly dependent on the used substrate and often does not lead to a layer-by-layer growth during deposition [BNLL11, PFA+00]. Therefore, the growth behavior was evaluated beforehand in a small set of samples. Figure 7.8 shows scanning electron microscopy (SEM) images of deposited silver films of 1.5 and 4.5 nm and a reference without silver. It can be seen that silver follows a Volmer-Weber type of growth, which is in good agreement with the literature [BNLL11, PFA+00].

In general, several places are possible for the placement of the silver. It could be deposited on top of the bottom electrode, inside the titanium oxide, or on top of the oxide (Figure 7.9). The island growth of the silver and the small oxide thickness makes it unreasonable to deposit the silver below or inside the titanium oxide layer. The increase in roughness would decrease the effective insulator thickness. Accordingly, the silver was sputtered after the titanium oxide deposition and before the deposition of the top electrode.

If the mobility of silver ions would be comparable to the resistive switching devices in section 6, the silver ions should migrate towards the lower electrode

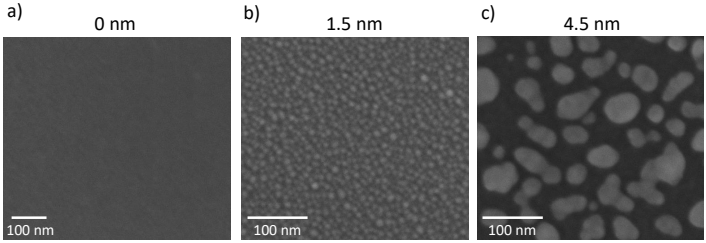


Figure 7.8: SEM images of silver films deposited with different deposition times. **a** Reference with no silver deposition. **b** Silver deposited with a nominal thickness of 1.5 nm leads to finely distributed islands. **c** Silver deposited with a nominal thickness of 4.5 nm does not show anymore homogeneously distributed silver islands, but instead leads to highly-localized agglomeration.

under positive bias. This was, however, not observed. A typical I-V-curve is shown in Figure 7.9. For positive bias voltages, no change in resistance occurs up to the point where the electrical field strength is too high and leads to a permanent breakdown of the device. For low negative voltages, a resistance is measured which is significantly larger compared to the previous device. If the voltage is further decreased, a hysteresis with a higher change in resistance (R_{init}/R_{on} = 5000 at -0.5 V) can be observed. The resistance decrease for negative voltages would imply that the reset should occur for positive voltages. Nevertheless, no sufficient reset was observed and the low resistive state (LRS) remained nearly unchanged.

The new Ti_xO_y/ Ag / Au device showed no improvement in terms of a reversible resistance change. Furthermore, considering the polarities for the set and reset branch, it has to be assumed that silver does not play an important role as an electrochemically active material, because the migration would have been expected for positive voltages, which did not occur. The main difference is the larger hysteresis in the "on"-state.

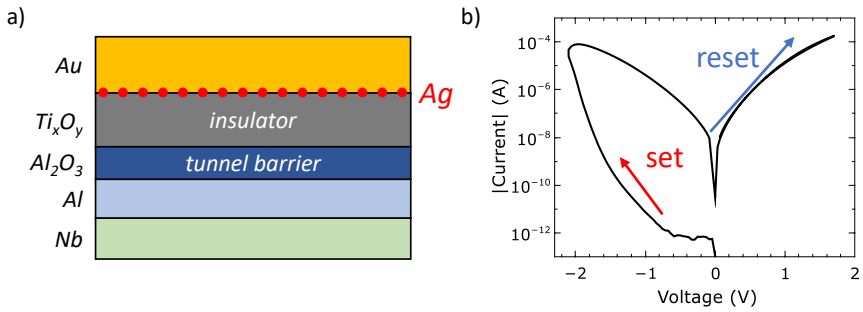


Figure 7.9: Enhanced titanium oxide device with silver. **a** Schematic cross section of the modified stack with the silver between the Ti_xO_y and the Au electrode. **b** Characteristic I-V-curve for this memristive device.

Titanium oxide has an electron affinity of ≈ 4.8-5.1 eV [SDB+13] (depending on crystal structure), while gold has a work function of ≈ 4.8 eV - ≈ 5.3 eV [Tra72, Riv66]. Considering this large range of energies, and the unknown parameters of the layers deposited in this thesis, it is not clear whether a Schottky-contact would form or not. The I-V curves shown in Figure 7.7 indicate that no Schottky-contact is formed (due to the large current at low negative voltages).

The silver/gold top contact would be expected to not form a Schottky contact, because the work function of silver is lower (4.3 eV - 4.6 eV [MM51, CM82]) than the work function of gold. The resulting work function would be thus expected to be in-between [FM74], and thus no Schottky-contact would be expected either.

The previously studied titanium oxide devices (Ti_xO_y/Au and Ti_xO_y/Ag/Au), even if they don't show reversible resistive switching, are perfect examples to highlight the importance of interfacial energy barrier properties. Although the reason for the formation of the highly-resistive rectifying contact for the Ti_xO_y/Ag/Au device remains unclear, its influence and importance is empha-

sized in Figure 7.10. The comparison of both devices in the negative branch shows how difficult it is for an ohmic contact to show a drastic change in resistance. On the other hand, the device with a rectifying Schottky-contact has a significantly larger potential to exhibit a huge resistance variation between on- and off-state, because the off-current is orders of magnitude smaller.

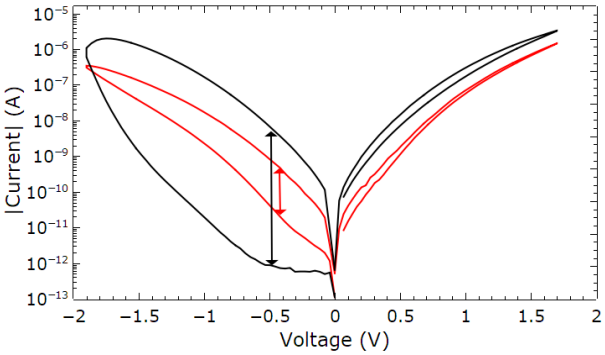


Figure 7.10: Comparison between Ti_xO_y/Au (red) devices and Ti_xO_y/Ag/Au (black) devices. Clearly visible is the huge difference in absolute current level and the increased hysteresis in the negative branch.

7.2 Niobium-Oxide Double Barrier Memristive Devices

The previous section demonstrated that larger barrier heights and the resulting Schottky contact could positively influence the resistive switching by increasing the ratio between the off- and on-state, due to a significantly increased off-resistance. A further aspect is the strong influence of the barrier height of a Schottky contact on the on-resistance, where small changes lead to an exponential increase or decrease of the conductivity. Another advantage is the need for a high off-resistance in neuromorphic circuits to reduce the power consumption in neuromorphic circuits [YSS13a].

Due to the large electron affinity of titanium oxide, the device exhibited ohmic properties. Consequently, a material had to be found which has a lower electron affinity to develop a device with a pronounced Schottky-barrier. It was feasible to use niobium oxide because it also is a transition metal oxide and has a broad range of suboxides. Typical electron affinities are around 4 eV, but range from $\approx$ 1.4 eV [ZWHW09] for Nb_3O to 4 [AMWC13] - 4.7 [GH80] for Nb_2O_5 . The lower electron affinity indicates that it is very probable to form a Schottky-contact with the Au-electrode. For a direct comparison with the previous device, Nb/Al-Al_2O_3/Nb_xO_y/Au devices with a niobium oxide thickness of $\approx$ 2.5 nm (comparable to the titanium oxide devices) were fabricated (Figure 7.11).

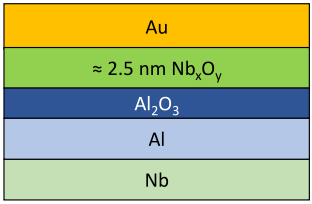


Figure 7.11: Schematic layer stack of Nb_xO_y-based memristive devices.

7.2.1 Niobium-Oxide Characterization

Figure 7.12a shows a typical resistance map of such a wafer for a voltage of 1.6 V. Clearly visible is the rotational symmetry of the resistance, with a valley of low resistance devices in the center, surrounded by a circle of high resistance devices. Towards the edge of the wafer, the device resistance decreases again.

The resistance plot below the map (Figure 7.12c) shows the device resistance for ± 1.6 V from the dashed rectangle. The resistance for both polarities is almost identical towards the edges of the wafer. For the inner 40 mm, the curves separate, with a large resistance for -1.6 V and a lower resistance for +1.6 V. This shows that the rectifying properties – which were the reason for the use of niobium oxide – is only present for devices in the center of the wafer. This resistance distribution across the wafer cannot be explained with the thickness of the niobium oxide (shown in Figure 7.12d, measured using ellipsometry).

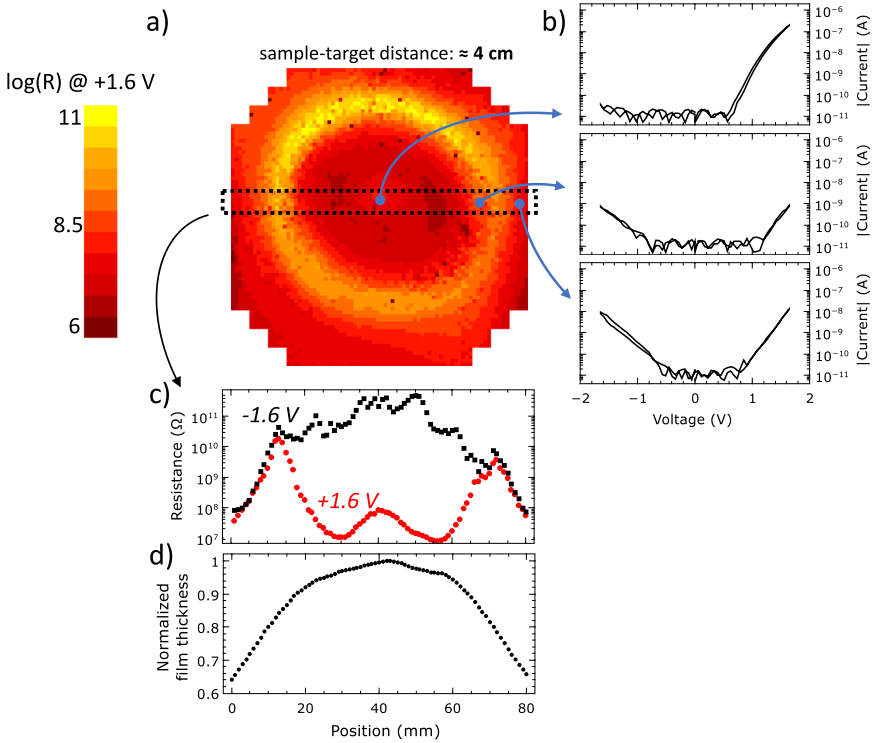


Figure 7.12: a Resistance map of Nb/Al-Al_2O_3/Nb_xO_y/Au devices on a 100 mm wafer. Each square shows the color coded resistance of one device (resolution: 1 mm × 1 mm). **b** Characteristic I-V-curves of the individual regions on the wafer. **c** Resistance across the dashed rectangle (averaged over five devices) for positive (red dots) and negative (black dots) voltages. **d** Normalized Nb_xO_y thickness close to the black rectangle.

7.2.2 Memristive Properties of Al_2O_3/Nb_xO_y/Au Devices

Figure 7.13 shows a typical I-V-curve with a large memristive effect. At first, the voltage was swept from 0 V to 3 V and afterwards back to 0 V. Subsequently, the voltage was decreased from 0 V to -2 V and back to 0 V. The device is initially in its high resistance state, and the positive voltage sweep leads to a decrease in device resistance (the *set*-process). The R_{off}/R_{on}-ratio (or I_{on}/I_{off}) is a common figure of merit to describe the magnitude of the hysteresis, which is approximately 200 at 0.6 V. For negative voltages, the current increases significantly, indicating that the rectifying properties observed in the initial / off-state are not observed anymore. For a further decrease in voltage, the slope of the current decreases, indicating that the device resistance is already increasing (*reset*). On the way back to 0 V, it can be seen that the rectifying property of the device for negative voltages is re-established during the reset process.

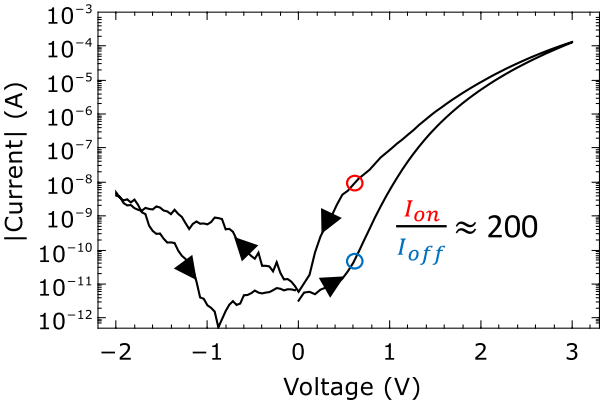


Figure 7.13: I-V curve for larger voltages exceeding the threshold voltages necessary to induce resistive switching. The arrows indicate the direction of the voltage sweep. The I_{on}/I_{off} ratio shows that the device resistance changes by a factor of 200.

Several attempts were made to increase the yield, i.e. the number of devices on the wafer which show resistive switching seen in Figure 7.13. The result of one examplary experiment is shown in Figure 7.14, where the target-sample distance was increased from 4 cm to 5 cm. Similar to Figure 7.12, the resistance map shows the resistance at +1.6 V. The rotational symmetry remains, but several exemplary I-V-curves in Figure 7.14b show, that no rectifying behavior can be observed anymore.

This is shown quantitatively in the resistance across the wafer (Figure 7.14c) shows the resistance for ± 1.6. For comparison, the resistance of the previous sample at 1.6 V is shown in gray. The difference between both samples is striking, because the resistance for positive voltages increased significantly and is now almost as large as the resistance for negative voltages.

This experiment did not lead to an increase in yield, because the resistance for positive voltages *increased*, diminishing the rectifying properties and consequently the resistive switching characteristics. Nevertheless, the film homogeneity did in fact improve, which can be seen in the normalized thickness in Figure 7.14. Besides the lower variation in the center of the wafer, the thickness at the edges of the wafer is larger compared to the initial target configuration.

This experiment is an important indicator for the highly sensitive nature of the reactive deposition of niobium oxide, and that even moderate changes lead to significant changes in the device properties.

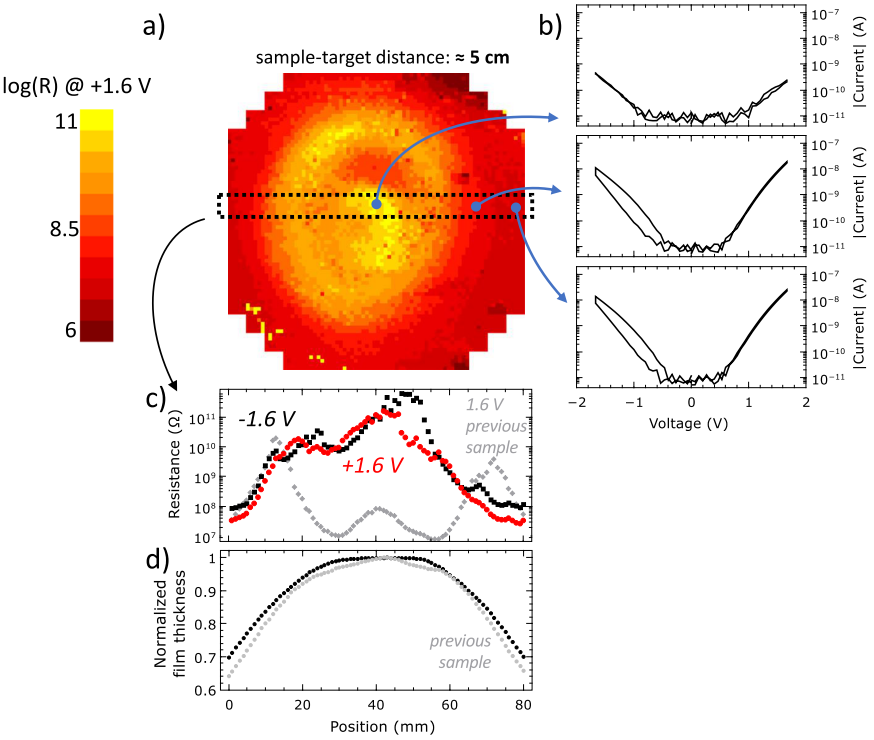


Figure 7.14: **a** Resistance map of Nb/Al-Al_2O_3/Nb_xO_y/Au devices with an increased target height. **b** Characteristic I-V-curves of the individual regions on the wafer. **c** Resistance across the dashed rectangle for positive (red dots) and negative (black dots) voltages. For comparison, the grey dots show the resistance of the previous sample for +1.6 V. **d** Normalized Nb_xO_y thickness close to the black rectangle.

Figure 7.15 highlights the changes of the diode properties in the low voltage regime for the on- and off-state. In the off-state, the device acts as a rectifying diode with a defined threshold voltage. In the on-state, besides the resistance decrease, the threshold voltage disappeared, allowing the device to carry larger currents even for low voltages. For negative voltages, the rectifying properties of the device disappeared, with currents comparable to positive voltages. After the the voltage is further decreased and the device is reset, the device shows again rectifying behavior.

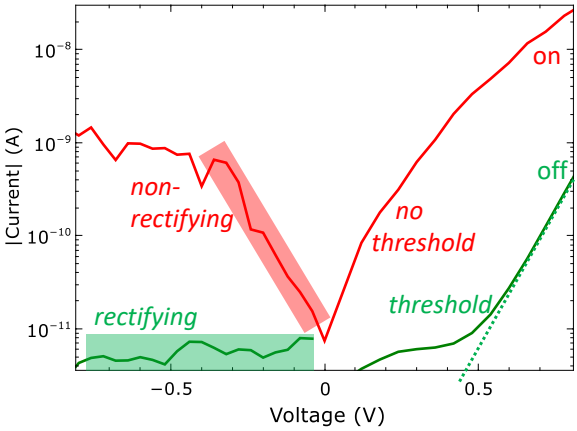


Figure 7.15: Details of the previous I-V curve highlight the changed device properties. While the device exhibits rectifying properties and a threshold voltage for the current in forward direction in the off-state, the on-state, on the other hand, neither shows rectifying behavior nor a threshold voltage.

Figure 7.16 shows the dependence of the applied voltages and sweep rates (i.e. the time necessary for one cycle) on the hysteresis. Figure 7.16a shows the time/sweep rate dependence on the hysteresis. The different values for the integration time lead to the given effective sweep rates. To neglect transient effects, a quasi-static sweep rate was chosen ($\approx$ 30 mV/s). For reference, I-V

curves for significantly larger sweep rates (500 mV/s) are shown as well. The strong difference in hysteresis is clearly visible. In order to quantitatively compare the resistive switching, R_{off}/R_{on} values measured at 0.6 V are given in the inset. It ranges from a factor of ≈ 20 for the fastest sweep rate to a factor of ≈ 4500 for the slowest sweep rate.

Figure 7.16b shows the influence on the applied maximum voltage for a constant sweep rate. These three curves clearly show the non-linearity in switching because the magnitude of the resistive switching is highly voltage dependent. Although not shown here, voltages below 1.5 V showed no hysteresis.

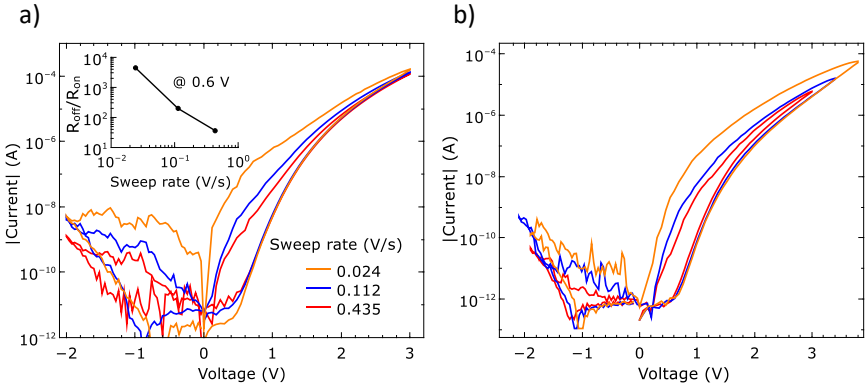


Figure 7.16: Changes in memristive behavior depending on applied sweep rate and voltages. **a** Three I-V curves for different sweep rates (0.435, 0.112 and 0.024 V/s). The increase in hysteresis with decreased sweep rate (i.e. longer time per cycle) is illustrated in the inset. The significance of the time dependence is emphasized by the double logarithmic axis. **b** The voltage dependence in forward direction strongly influences the current hysteresis.

7.2.3 Resistance Dependence on History of Applied Voltages

One of the main properties of memristive devices is the resistance dependence on the history of charge or voltage applied to the device. This property is of course fulfilled by every memristive device on a local scale. The previously discussed silver device, for example, will be in the high resistance state if a positive voltage was previously applied and in the low resistance state if a negative voltage was applied. No information however is retained from previous cycles. Thus, only information on the immediate past are available. It is of interest to study the behavior of memristive devices with analog switching. The double barrier device described here possesses analog set and reset behavior. The following description may not be applicable to devices where one of these two is not completely analog. Figure 7.17 shows several cycles for two sets of applied voltages. On the left hand side, the voltages were chosen to guarantee a complete reset of a device. On the right hand side, the set voltage was the same but the reset voltage was lower and not sufficient to completely reset the device to its initial state. The direct comparison shows that the on and off state on the left side stay almost constant over 100 cycles, while even 25 cycles are sufficient to increase the on- and off-state by an order of magnitude.

At first glance, this could be considered to be a disadvantage of this device. This is true – at least for memory applications – while this offers another degree of freedom for neuromorphic applications. Depending on the implementation of set and reset in such a circuit, the observed characteristics allows the device to not only carry information of the current state, but also on the previous cycles. Compared to the silver devices, where only the current state (on or off) is retained. Another advantage is the similarity to long term potentiation (LTP) and depression (LTD), which are responsible for the weight adjustment in biological synapses. The LTP and LTD leads to

an increase or decrease in synaptic strength due to frequent or seldom usage of these synapses. The over-time increasing current of Figure 7.17b could successfully emulate this principle.

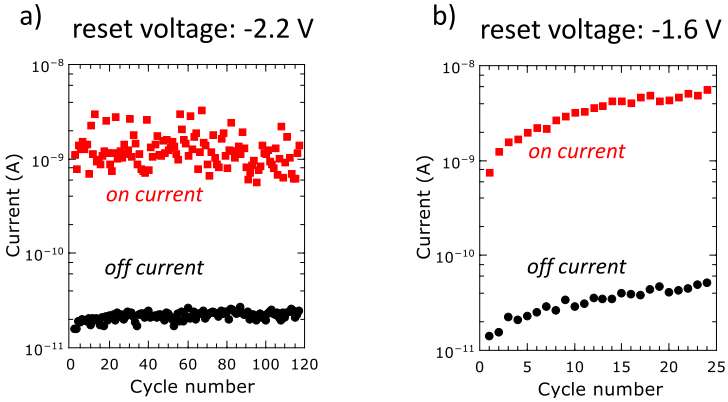


Figure 7.17: Cycling comparison for a set voltage of 3 V and different reset voltages. **a** 120 cycles for a reset voltage of -2.2 V, with barely no change in average off- and on-current. **b** a lower reset voltage of -1.6 V leads to an insufficient reset, and a slow increase in overall current for off- and on-current.

7.3 Simulation

7.3.1 Possible Switching Mechanisms

It is possible to determine the switching mechanism by analyzing the slope of the resistance × area product. In order to investigate this area dependency, voltage sweeps on different areas were conducted (Figure 7.18). A horizontal line (slope=0) indicates a homogeneous switching mechanism. A slope larger zero indicates a filament-based resistive switching, discussed in chapter 6.

This indicates that the switching mechanism for this double barrier memristive device is independent of the area, and probably no filaments are formed during switching. Since a filament growth is excluded, only a few possible physical effects remained.

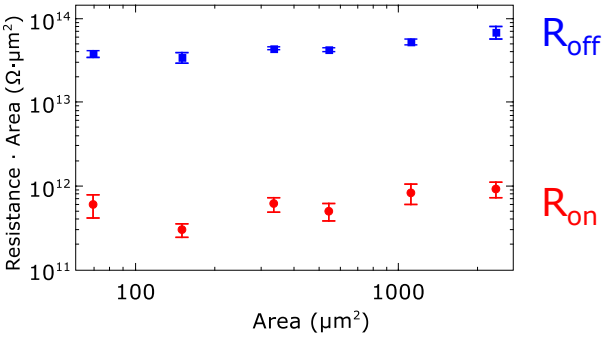


Figure 7.18: The resistance × area plot indicates that the observed change in resistance occurred homogeneously. The blue squares represent the initial state and the red squares represent the on state.

Figure 7.19 shows again a typical material stack of the double barrier memristive device, with its functional materials like Al_2O_3 being the tunnel barrier and Nb_xO_y as the ionic conductor. Figure 7.19a schematically shows the resistive switching by trap states in the niobium oxide. In this scenario, electrons are trapped and released during voltage application. Depending on the trap configuration (charged / uncharged), the observed electrical resistance can either decrease (low resistance state) or increase up to the initial resistance (high resistance state).

Another explanation for the observed change in resistance could be the field-induced drift of negatively charged oxygen ions inside the niobium oxide layer (Figure 7.19b). In the *set*-process, the field generated by the positive voltage applied to the gold electrode would lead to a drift of negatively charged oxygen ions towards the gold electrode. The following decrease in

barrier height due to the negatively charged ions would decrease the observed device resistance. During the *reset*-process, the accumulated ions at the gold electrode would be forced back towards the opposite electrode.

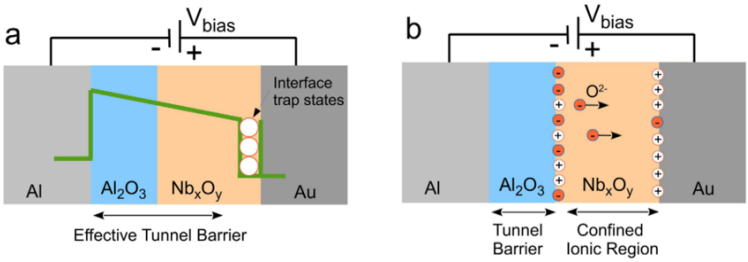


Figure 7.19: Two possible scenarios can explain the observed resistive switching effects. **a** Trap states, for example, at the Nb_xO_y interface, which are charged and discharged during voltage application. **b** The drift of oxygen ions under applied electric field could change the Schottky barrier height, which increases or decreases the device resistance and thus the memristive behavior.

7.3.2 Influence of the Individual Barriers

In order to compare the contribution of the individual barriers, the I-V-curves of three devices with different barrier configurations are shown in Figure 7.20.

- The first sample (*Tunnel barrier*) does not have a Schottky barrier because Nb was used instead of Au for the top electrode (Figure 7.20a).
- The second sample (*Schottky barrier*) does not have a tunnel barrier because the Nb_xO_y was directly deposited on the Nb bottom electrode (Figure 7.20b).
- The last sample (*Double barrier*) is the previously described memristive device with tunnel- and Schottky barrier (Figure 7.20c).

The tunnel barrier device lacks the rectifying diode properties and shows a nearly symmetrical current for positive and negative voltages. No resistive switching was observed with this device (Figure 7.20a).

The Schottky barrier device shows a strong asymmetry which can be explained by the Schottky barrier. For this device, resistive switching was observed but the change in resistance was significantly lower than in the double barrier device (Figure 7.20b).

As previously discussed, the double barrier device shows a strong asymmetry and at the same time has the largest change in resistance. The comparison of these three devices indicates the necessity for two energy barriers to achieve resistive switching (Figure 7.20c).

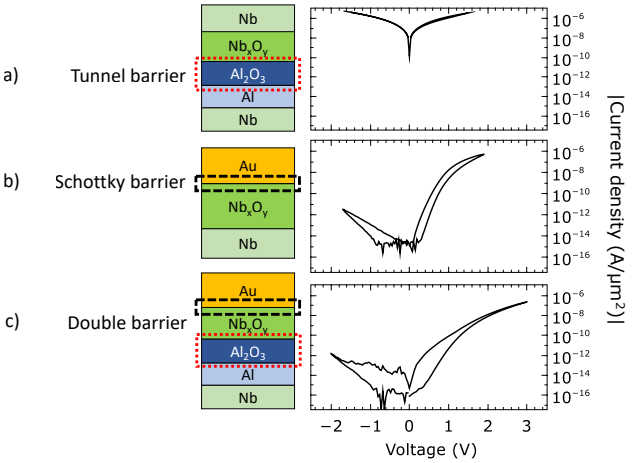


Figure 7.20: Comparison between several barrier variations. **a** Tunnel barrier device with no Schottky barrier and a large current with no resistive switching. **b** Schottky barrier device with no tunneling barrier and rectifying properties and a small memristive effect. **c** Double barrier device with Schottky and tunneling barrier and the largest hysteresis.

The retention, i.e. the resistance state evolution with time, which can be stored by a memristive device, is another important property. Unlike memory applications, neuromorphic applications typically do not require a retention of ten years or more [YSS13a]. Nevertheless, a retention of several days to weeks is still necessary. This is investigated by first setting the device to the on-state and measuring the time-dependence of the resistance. Figure 7.21 shows the retention measurement for the Schottky-barrier and the double barrier device. To compare both devices, the resistance of each device was normalized to its initial resistance.

Both curves start with a resistance which is several orders of magnitudes lower than the initial state. For the double barrier device, we see a continuous increase in resistance, while the Schottky device has a nearly constant resistance for the first $\approx$ 1000 seconds. After 1000 seconds, the Schottky device shows a sudden increase in resistance. This leads to a nearly complete reversal to the off-state after only 10000 seconds.

The resistance plateau of the Schottky device seems to make it a suitable device, but the abrupt change in resistance limits its usage to applications which operate in the order of minutes.

Although the resistance increases constantly in the double barrier device, the continuous nature makes this less harmful for analog neuromorphic circuits than the sudden resistance change of the Schottky device. Furthermore, the resistance takes significantly longer to asymptotically reach the off-state. The suitability of the retention is shown in section 8.3, where the retention of 35 devices within a pattern classification circuit is analyzed.

Going one step further, the continuously increasing resistance is sometimes considered to be an intrinsic feature of some memristive devices [CJK$^+$11, CLH$^+$13], because it integrates a *forgetting rate*, which is similarly found

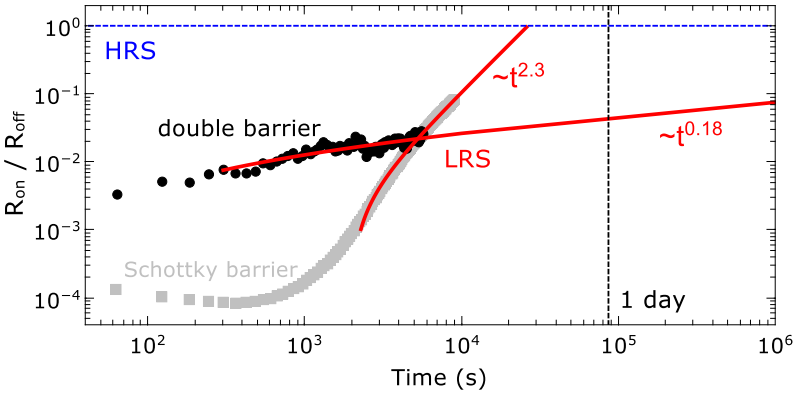


Figure 7.21: Retention measurement of the double barrier (black points) and Schottky-only (grey points) device. For reference, the dashed line shows $R_{on}/R_{off} = 1$ for the high resistance state is shown.

in mammal brains (e.g. long term depression), which is important for the actual functioning of the brain [MCD+98]. An interesting example is a learning rule proposed by Oja in 1982 [Oja82]. This learning rule would overcome the problem of unbound growth in synaptic coupling strengths in several neuron models. In this learning rule, the coupling growth shows asymptotic stability due to a forgetting rate which becomes stronger with an increase in synaptic efficacy. The asymptotic increase in resistance can be considered as an hardware implementation of Oja's rule. The dependence of the resistance state on the retention is not studied in detail here, but Monte-Carlo simulations of the double barrier device indicate that this behavior can be expected. The resistance decrease during the set-process leads to an increasing concentration gradient proportional to the resistance change.

7.3.3 Requirements for Simulation Model

To describe the memristive properties of the device, a lumped circuit model was developed. This allows to model complex physical effects with a circuit consisting of simple devices known from electrical engineering [BMCH99, MBC+00].

An important requirement for this kind of model is the voltage drop across the individual layers, to assess the influence on resistive switching. Here, a capacitive divider with experimentally acquired parameters will be used.

In order to calculate the capacities in the capacitive divider, several approaches are possible. The use of literature values for aluminum oxide and niobium oxide is a simple, but error-prone possibility. The permittivity of materials highly depends on the thickness and deposition conditions. Since literature values are mostly reported for bulk layers, they were not considered to be sufficiently accurate for the nanometer-thin films used here.

One experimental method to measure the capacities is the fabrication of devices, which contain only aluminum oxide or niobium oxide. This method has several disadvantages: First of all, the fabrication of the aluminum oxide layer does not allow a significant variation in thickness, since the oxidation of aluminum in an oxygen atmosphere is a self-limiting effect. Furthermore, the resistance of devices with only aluminum oxide was too low for an accurate capacitance measurement. The most striking disadvantage of this method is the independent examination of the capacity. Although the values might be correct for the deposited films themselves, it cannot be ruled out that the aluminum oxide / niobium oxide multilayer exhibits different capacities. The obvious difference lies in the deposition conditions, for example in a different interface roughness or electrical properties.

This problem was solved by fabricating several Al_2O_3/Nb_xO_y multilayer devices, with a variation in Nb_xO_y thickness ranging from 1 to 20 nanometers, while the thickness of the aluminum oxide remained constant. This procedure is commonly used for the calculation of interfacial capacitances in capacitors [ELBW04]. The total capacitance of the devices is given by

$$\frac{1}{C_{total}} = \frac{1}{C_{Al2O3}} + \frac{1}{C_{NbxOy}(d)}$$

or

$$\frac{1}{C_{total}} = \frac{1}{C_{Al2O3}} + \frac{d_{NbxOy}}{A\epsilon\epsilon_0}$$

and the capacity of the aluminum oxide layer can be estimated for an extrapolation of d_{NbxOy} to 0 nm. By measuring the capacity for multiple thicknesses and plotting the inverse in dependence of the niobium oxide thickness, the capacity for a device with 0 nm niobium oxide thickness can be extrapolated (i.e. a device with only aluminum oxide, see the leftmost stack in Figure 7.22). Using these values, the capacity of aluminum oxide was estimated as $\approx 2.1 \cdot 10^{-14} F/\mu m^2$, and the capacity for a ≈ 2.5 nm niobium oxide layer is $\approx 1.7 \cdot 10^{-14} F/\mu m^2$.

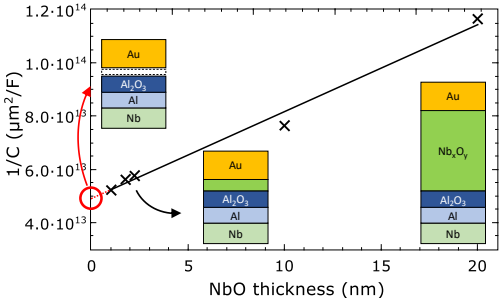


Figure 7.22: Determination of the Al_2O_3/Nb_xO_y double layer capacity. For the accurate measurement of the capacity, both layers are necessary. This requires the fabrication of several devices with a varying Nb_xO_y thickness. After the capacity of these devices is measured, the capacity is extrapolated for a device with 0 nm Nb_xO_y, yielding the capacity of the Al_2O_3. The schematically drawn stacks show devices with different Nb_xO_y-thicknesses.

7.3.4 Lumped-Circuit Model Simulation

This simulation model was partially developed by Lukas Kolberg during his Bachelor thesis.

With these values for the capacitve divider, it was possible to approximate the voltage drop across the important layers. Only an excerpt of the results are shown here, but the simulation model is extensively described in

> Mirko Hansen, Martin Ziegler, Lucas Kolberg, Rohit Soni, Sven Dirkmann, Thomas Mussenbrock, and Hermann Kohlstedt. "A double barrier memristive device", *Scientific Reports*, **5**, 2015.

Figure 7.23 shows the stack of the double barrier memristive device with its relevant layers and a proposed circuit representation.

A voltage controlled current source was used to describe the tunneling barrier, because the current depends non-linearly on the voltage across the aluminum oxide layer. Using the potential across the tunnel barrier (known from the capacitive divider), it is possible to calculate the current through the barrier.

The contribution from the niobium oxide is modeled by a resistor in parallel to the capacitor (C_I). The resistor describes the bulk resistance of the niobium oxide. The resistor leads to a linear dependence, unlike the current source, between the niobium oxide potential and its layer capacitance.

The rectifying properties of the Schottky-contact are described using a diode in series to the previous components.

Figure 7.23b shows the simulated I-V-curve with the assumption that the Schottky barrier height at the Nb_xO_y/ Au interface and the tunneling

distance through the Al_2O_3 tunneling barrier is changed during the set- and reset-process.

The influence of the varying tunneling distance can be seen in Figure 7.23c, where this effect was turned off during the simulation and only the variation in Schottky barrier height was simulated. The significant variation between these curves indicate, that the change in tunneling distance cannot be neglected. This was furthermore confirmed using the Monte Carlo simulations in the following section.

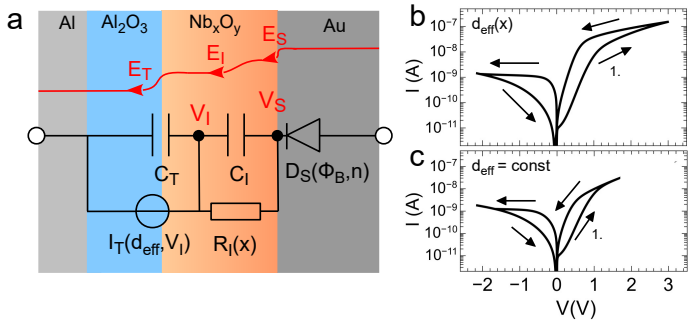


Figure 7.23: a Schematic layer sequence and corresponding electrical representation in the lumped circuit model. The simulation results show the dependence on **b** a variable tunneling distance and a change in the Schottky barrier height and **b** with a constant tunneling distance. [HZK+15]

7.3.5 Monte-Carlo Simulation

The simulations in this section were conducted by Sven Dirkmann and Thomas Mussenbrock.

This collaboration lead to a joined paper. [DHZ+16]

Another approach to simulate the memristive device are Monte-Carlo-Simulations. These simulations were conducted by Sven Dirkmann and Thomas Mussenbrock and allowed a direct investigation of the role of the ion transport for the resistive switching. One simulation result is shown in Figure 7.24, adapted with permission of Sven Dirkmann [DHZ+16].

The I-V-curve is in accordance with experimental measurements with similar parameters. The neighboring schematics show the state of charges for different voltages. In this simulation, it was assumed that positively charged ions/defects are not mobile, while negatively charged ions (i.e. oxygen ions) can move under an applied electric field. The blue arrows indicate the current average ion position. Initially, the device is in the high resistance state and the ions are randomly distributed and the average ion position is in the middle of the niobium oxide. With increasing voltage, negatively charged ions drift towards the gold electrode and adsorb at the interface. The electric field resulting from this charged displacement leads to a decrease of the Schottky-barrier height and is responsible for the decrease in resistance. If the voltage is decreased to 0 V, the adsorbed ions remain at the interface and the device is in the low resistance state. For small negative voltages, the ions remain at the interface. For increasing negative voltages, the reversed polarity forces the adsorbed ions back towards the opposite electrode. At minus 2 V, most adsorbed ions are detached from the gold electrode. An increase back to 0 V leads to an ion distribution which represents the off (or initial)

device state. These simulations support the above described experimental results and discussion. Further simulations [DHZ+16] (not shown here) of the retention yielded very similar results as the experimental results (as shown in Figure 7.21).

Two assumptions were made for the lumped and the kinetic Monte-Carlo simulations: The change in resistance occurs due to the variation in tunneling distance and the modification of the Schottky-barrier height due to the movement of oxygen ions. The lumped circuit model was able to support this theory because it yielded similar I-V curves. The kinetic Monte-Carlo simulations not only resulted in similar I-V curves, but showed very similar retention behavior of the on-state. It has to be emphasized that the simulation of two different device characteristics using a single model is a novel and challenging task, but increases the reliability of the model.

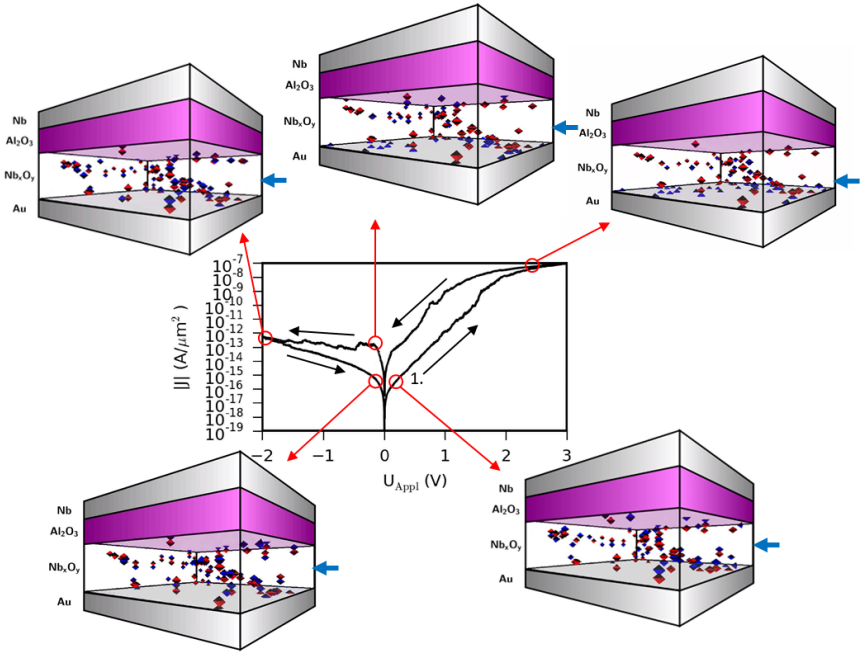


Figure 7.24: Monte-Carlo simulation conducted by Sven Dirkmann, implementing the resistive switching in the double-barrier memristive device using a variable tunnel distance and oxygen ion movement. The resulting I-V curve is shown in the center, while the schematics show the state of the device at different voltages. Blue and red dots indicate mobile negative and static positive charges, respectively. (Adapted with friendly permission of Sven Dirkmann.)

Chapter 8

Integration of Memristive Devices into Crossbar-Arrays

8.1 Transition from Single Devices to Crossbar-Arrays

After the successful development of niobium oxide double barrier device, its abilities to be used in a crossbar array were investigated. In such a crossbar array, the memristive devices are not individually contacted with top and bottom electrode but share top and bottom electrodes. This leads to a significantly increased number of devices per area and reduces the number of connections to address a large number of devices. Further details can be found in section 3.1. The filament-based silver memristive devices were not integrated into crossbar arrays, because it was intrinsically clear that this is not feasible. Due to the symmetric and ohmic I-V-curve in the low resistance state, a small number of devices in the on-state would be sufficient to affect neighboring devices negatively. This is a common problem for memristive devices and is discussed extensively in the literature [LRKW10, YSS13a, BSS$^+$17]). Since the double barrier device does not suffer from these problems, it is the first feasible candidate.

Due to the different mask layout, it was not possible to measure a complete array using the wafer prober. Thus, the crossbar arrays were wirebonded

to custom PCB sample holders and measured using the measurement setup described in sections 5.3 and A.3. The measurement program was extended to control a microcontroller, which addressed the rows and columns of the crossbar array.

Figure 8.1a) shows a typical resistance map of a memristive crossbar array. Figure 8.1b) shows in red an I-V-curve from a memristive crossbar array. The grey I-V-curve was measured on a wafer with a comparable memristive device using the single-contact mask described in section 3.1. The good agreement between both curves highlights the usability of these devices for crossbar arrays, because no distortions due to sneak paths or similar problems are visible. The lower noise floor can be explained by the different measurement setups (i.e. shorter cables to the devices and better shielding). Nevertheless, a problem of the first fabricated crossbar arrays is shown in the histogram in Figure 8.1c). This histogram quantitatively shows that the resistance spread is rather large in the initial state.

A possible explanation is illustrated in Figure 8.2, where the dimensions of the previous devices and the crossbar array are compared. On the left hand side, a resistance map of individual devices from the center of a wafer is shown, with one contact size per mm^2. On the right hand side, a single crossbar array with 256 devices is shown. The length of the black scale bar below the maps is 4 mm and 100 µm, respectively. It is evident that the significant increase in device density (300 devices per mm^2) makes it impossible to interpolate from the single devices to the crossbar arrays. There are now 300 devices on the same area, where previously only one contact was. The variation observed in the crossbar arrays could not be resolved and was thus not visible. [3]

[3] The densities given here for the crossbar arrays should not be mixed up with the number of devices on one wafer. In the active part of a crossbar array $\approx$ 300 devices are concentrated on 1 mm^2. If the density for the complete wafer is calculated (taking into account the overhead by contact pads and extra spaces for dicing lines), the density is reduced to 53 devices per mm^2.

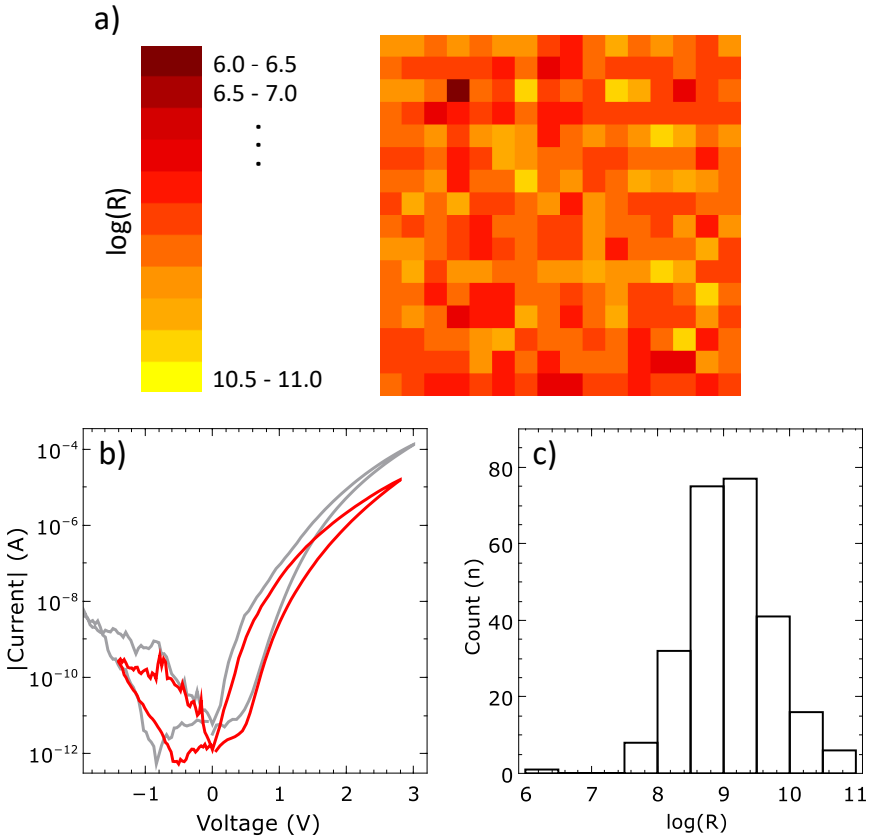


Figure 8.1: Measurements on memristive crossbar arrays. **a** Mask layout. **b** Resistance map of the crossbar array measured at ≈ 0.8 V. **c** An individual I-V curve showing a comparable resistive switching compared to the previous single contacts.

The first application of these crossbar arrays is the pattern classification circuit described in section 8.2. The pattern classification network requires a crossbar array with devices, which can have multiple resistance states. The iterative learning procedure would be impossible with devices that possess

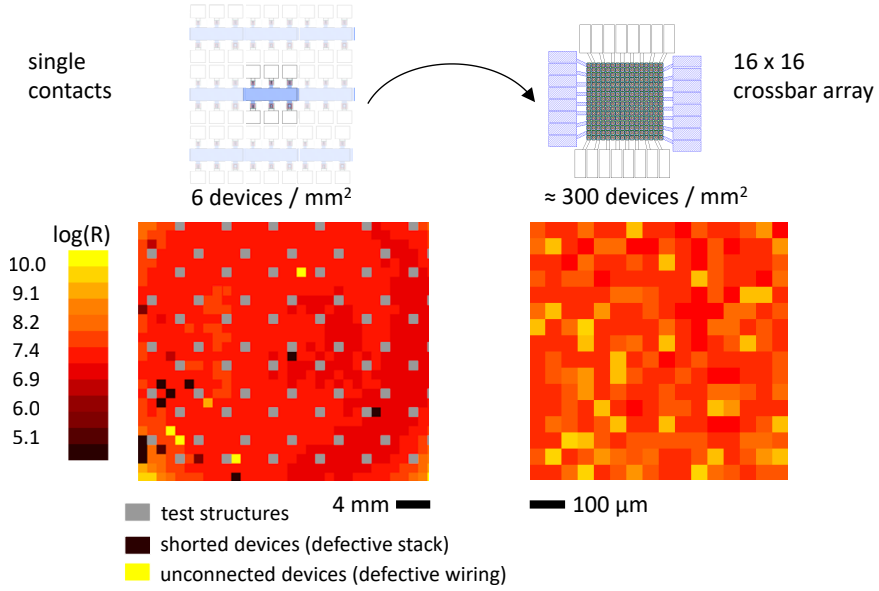


Figure 8.2: Comparison between the device density of single devices and crossbar arrays. The significantly increased contact density makes variations visible, which were not resolved previously due to the lower resolution.

a digital or binary switching mechanism. For this circuit it is important to know how these devices change their resistance in dependence of the number of applied voltage pulses. Figure 8.3 shows the response of two memristive devices on set and reset pulses. In order to yield meaningful results, five set and reset pulse sequences were applied. A device starts in the high resistance state and it can be seen that the first set pulse has the biggest impact on the device resistance. All further set pulses, further decrease the device resistance, but their influence decreases with every pulse. Afterwards the reset pulses increase the resistance again with similar course. Both devices have the same characteristics, although the absolute values differ. This measurement

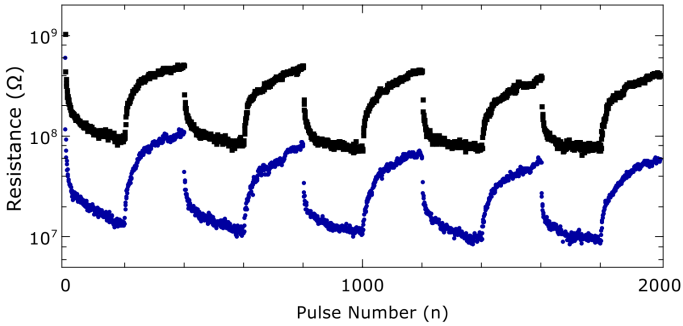


Figure 8.3: Pulse measurements demonstrating the analog switching mechanism of this device. Shown is the resistance development after five cycles of 200 set- and reset pulses each, with the device resistance measured at a voltage of 0.9 V. (Set pulses: 4.5 V for 110 ms, reset pulses: -1.5 V for 300 ms.)

indicates the pulse dependent multilevel ability, which allows the device to operate in an analog fashion.

Summarizing these results, arrays composed of these devices would make it possible to decrease or increase the weight of a stored pattern over time (with several set or reset cycles). Without this multilevel, analog switching, the device resistance would switch immediately, after the first set or reset pulse, into the low or high resistance state. The observed analog switching property is often also called multilevel resistance state, indicating the state development by several set or reset pulses as shown in Figure 8.3.

8.2 Application: Pattern Classification

The previous section described a simple circuit with a single memristive device emulating the anticipation exhibited by amoebas. In this section, a more advanced circuit for pattern recognition with numerous memristive devices is implemented in hardware. Applications like pattern recognition are considered as promising candidates to enhance classical computing schemes by abilities which would typically require immense computing power. In recent years, deep neural networks made unforeseeable progress in many fields (e.g. speech and pattern recognition) [HDY+12]. Nevertheless, this is only possible with a massive amount of centralized computing power. These approaches are commonly *not* inspired by neuro-biological learning processes. Different computing paradigms try to emulate these brain-inspired mechanisms to solve complicated problems using smaller and energy efficient systems.

8.2.1 Device Requirements

In this section, a neuromorphic pattern recognition/classification circuit is presented, which was first proposed by Querlioz et al. [QBG11]. It shows very promising simulation results for the recognition of hand-written numbers. To fabricate the required number of memristive devices, it was necessary to create new lithography masks with 16×16 crossbar arrays. This is described in section 8 in more detail. In order to address the devices in the wire bonded crossbar-array, it was necessary to build a circuit which multiplexes the input signals to the individual devices. This is described in more detail in section 5.3.

The question arose, which device would suit the intended application best. It became evident quickly that the silver devices could not be used in this

circuit without significant circuit overhead. The missing non-linearity in the I-V-curve (ohmic on-state, very low set-voltage) would require additional on-chip selector devices for each device. This would require CMOS technology which is not available in the Kiel Nanolab. These selector devices would electrically connect only the currently addressed memristive device, and the low resistance of the neighboring devices does not influence the current device. Without these selector devices, the low resistance state of the other devices would short-circuit large parts of the crossbar-array.

The double barrier memristive device on the other hand is a suitable candidate to fulfill these requirements. Due to the high non-linearity and high resistance in the on- and off-state, the previously mentioned problems do not apply. Another advantage is the steady resistance change proportional to the amplitude and time of the applied voltage. This feature allows a learning process which progressively trains the network over several iterations. This is hardly possible with the silver devices, because even moderate set pulses would lead to an immediate and drastic change in resistance.

8.2.2 Network Description

The major components of the neuromorphic circuit are shown in Figure 8.4. In this exemplary description, patterns with 3×3 pixels are used. There are, however, no limits concerning either the size or restrictions on the number of rows and columns. The patterns to be learned are initially in a human-readable 2D representation (8.4i). These 2D patterns are then transformed into a 9×1 vector (8.4ii). This 1D representation is not necessary in principle, but facilitates the graphical visualization of multiple receptive fields in a crossbar structure, because there is one column for every receptive field in the array. Each pixel from the input pattern is fed into a pre-neuron, which stochastically decides, whether the value of this pixel is an active part of

the pattern. This would be especially important if not only black and white pixels were used, but grey-scale values to allow a more natural representation of real i.e. hand written numbers. Because only black and white pixels are used here, the output of a pre-neuron is always "1" for a black pixel and "-1" for a white pixel (8.4iii). The next step requires the current resistances of the crossbar array. Thus, the current of each device is measured by applying a 300 ms 0.9 V pulse and the resistance is calculated. In the next step, the contribution of each memristive device towards the receptive fields stored in an individual column is calculated.

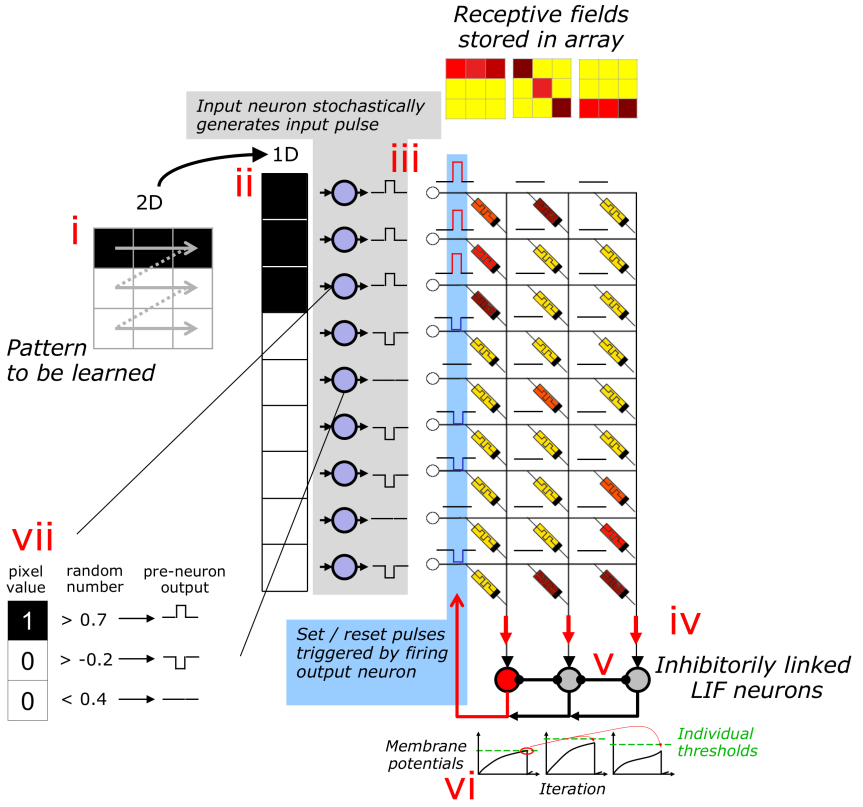


Figure 8.4: Schematic circuit for the pattern recognition network. The input pattern is transformed from the 2D to a 1D representation. These pixels are applied to pre-neurons, which, depending on the pixel weight, lead to a positive or negative pulse. Depending on the sign of the individual pre-neuron's spike, the current measured from each memristive device is either added or subtracted from the total column current. This column current charges a capacitor (the membrane potential), which is part of the leaky-integrate-and-fire neuron (similar to Figure 2.6) inside the output neuron. If the membrane potential reaches a threshold, this output neuron fires and resets the integration for all output neurons. Depending on the output state of the pre- and the post-neuron, the corresponding memristive device is either unaltered, set or reset.

For the calculation of the column current, the individual currents are weighted by the pre-neuron output. If the pre-neuron's output was "1", the current is added towards the total column current (8.4iv). If the pre-neuron's output value was "-1", the current is subtracted from the column current. This can be explained by describing the task of the column current. It should be proportional to the similarity of the applied pattern and the individual column. In order to achieve this, the current of the pixels that are not present in the applied pattern are subtracted from the column current. Their contribution is penalized because these devices are not an active part of the pattern and should have a very high resistance. In the ideal case, the high resistance of these devices would not affect the calculation of the column current. If, however, the device is *wrongly* in the low resistance state, the significant negative current decreases the column current, indicating that the pattern in this column is not similar to the applied pattern.

This column current is fed to the post-neuron and leads to an increase in the membrane potential of the leaky integrate-and-fire neuron (see section 2.3). An important component for the output neurons is the "winner-takes-it-all" approach. This means that the firing output neuron resets the other output neurons' membrane potentials and the integration phase starts again for all output-neurons (8.4v). This means that the pattern stored in this column is similar to the input pattern. The reset of the membrane potential requires an automatic adjustment of the individual output neuron's threshold voltage. This threshold is dynamically adjusted in order to guarantee that not a single post-neuron fires all the time, while others never to fire at all. By increasing the threshold for frequently firing post neurons, their future probability to fire is decreased. On the other hand, the threshold is decreased for seldom firing post-neurons to increase the probability to fire.

Below the post-neurons, the development of the membrane potentials is shown (8.4vi). The green dashed line shows the threshold necessary for the

individual output neuron to fire. In this example, the left neuron reaches the threshold voltage first, which leads to a reset of the membrane potential for all output neurons.

The lower left part of Figure 8.4 (8.4vii), shows the pre-neuron's calculation procedure. On the left are three pixels of the input pattern and their corresponding weight. In the middle is a random number, which was individually generated for each pre-neuron. If the pixel weight is positive and larger than the random number, a positive pre-spike is generated. If the pixel weight is negative and larger than the random number, a negative pre-pulse is generated. On the other hand, if the weight is smaller than the random number, no pre-pulse is generated.

Depending on the state of the pre- and post-neuron's output, four cases for each memristive device can be distinguished (Table 8.1). The two important scenarios are 3. and 4., which increase (reset) the device resistance because the pixel *is not* part of the pattern and decrease (set) the device resistance because the pixel *is* part of the pattern.

	Pre-neuron fires	Post-neuron fires	Pulse applied to device	Result
1.	×	√	×	*nothing*
2.	↑	×	×	*nothing*
3.	↓	√	↓	Reset device (corresponding input pixel is white)
4.	↑	√	↑	Set device (corresponding input pixel is black)

Table 8.1: Pulses applied to the memristive device depending on the state of pre- and post neuron. ×: no pulse, ↑: positive pulse, ↓: negative pulse, √: post-neuron active.

After the respective neuron fired, the memristive devices, where the pre- and post-neuron had a positive output, are set using a 100 ms 3.9 V pulse.

The memristive devices having a pre-neuron with negative output and a post-neuron with positive output are reset, because these devices do not contain an active pixel in the input pattern. After these set- and reset operations, the state of the receptive fields (i.e. the resistance of the crossbar array) is measured. Afterwards, the training procedure for the next input pattern starts again, repeating the procedure described above.

The next section describes the development for three input patterns and five receptive fields with 6×6 pixel patterns.

8.2.3 Simulation

> The simulation part of this section was conducted by Finn Zahari during his Bachelor thesis and his time as student assistant.

Although the general suitability of the double barrier device was assumed in section 8.2.1, it is not clear whether the resistive switching properties (e.g. device variability, on/off-ratio etc.) are sufficient for a successful hardware integration of this learning network.

First of all, the resistance change in dependence on voltage pulses with different amplitudes and widths was evaluated. This is important for the circuit-integration, because the resistive switching will be induced by voltage pulses.

The following variables were investigated for the pulse application:

1. a fixed pulse duration with a variable amplitude (Figure 8.5a), and
2. a fixed voltage and a variable pulse duration (Figure 8.5b) for the set process;
3. a fixed pulse duration and a variable voltage (Figure 8.5c) for the reset process.

Each pulse was applied 1000 times and the device resistance was measured before and after voltage pulse application. The previously observed non-linearity can here be seen as well. In all three scenarios, an exponential dependency on the variable can be seen.

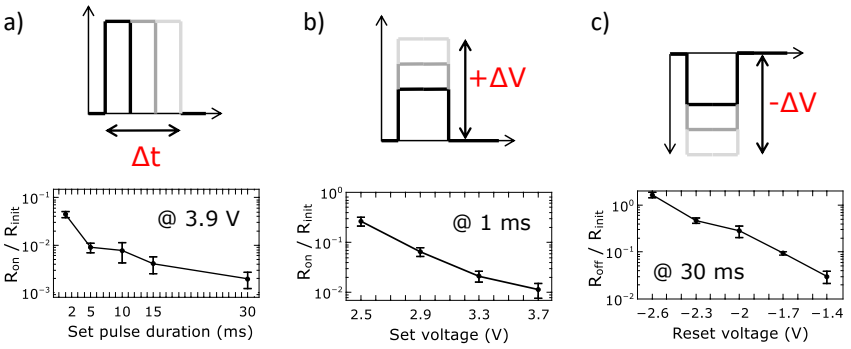


Figure 8.5: Resistance change in dependence on 1000 applied set and reset pulses with **a** different pulse durations **b** different set voltages and **c** different reset voltages.

In the second step, these results were fitted using a hebbian plasticity model, described in more detail in Ref. [ZRH+15]. Afterwards, a simulation of the learning network shown in Figure 8.4 was conducted, described in references [ZHM+15] and [HZZK17] in more detail. Only some of the important results are shown here.

The input patterns were taken from the MNIST dataset, which contains hand written numbers from 250 writers [LBBH98]. Figure 8.6 shows the resulting receptive fields of 50 output neurons after the learning phase. Each receptive field consists of 28 × 28 pixels. A very interesting observation highlights the need for more output neurons than input patterns. The first two receptive fields both show the number "2". Nevertheless, both receptive fields were trained to different *variants* of the number "2", which simplifies the classification task for the network. If, on the other hand, only one receptive field is given for each input pattern, the recognition rate decreases significantly, because now *all* variants of the number "2" would have to be included in one receptive field [QBG11, HZZK17].

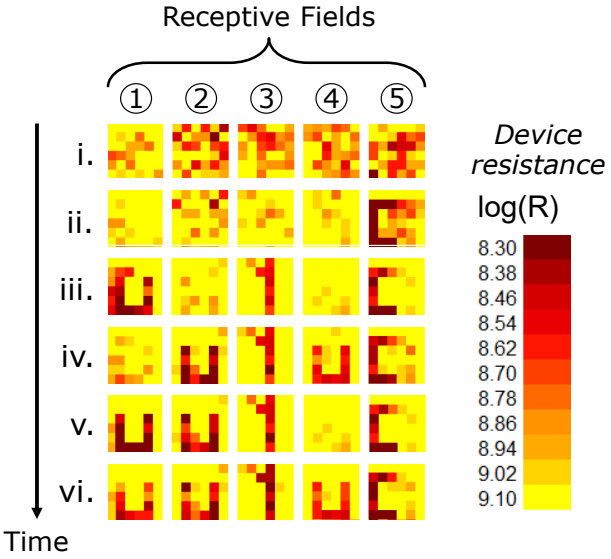


Figure 8.6: Simulation results with 50 receptive fields for handwritten numbers from the MNIST-dataset.

An important criterion for the network performance is the tolerance to defective devices either due to fabrication problems or destruction during switching. Figure 8.7 differentiates four cases, where the resistance is either too low (Figure 8.7a) or too high (Figure 8.7b). For both scenarios, the recognition rate is shown for one (blue curves) and ten (red curves) receptive fields affected by defective devices.

The nearly unchanged recognition rate for the blue curve (only one receptive field affected by defective devices) are very similar, which can be explained easily: Even if one of ten fields is completely distorted, the remaining nine fields remain perfectly readable.

If all ten fields are affected by defective devices, both curves decrease significantly with an increasing number of defective devices, although the

descent varies between the low- and high resistance scenario. This can be explained by the *column current* discussed earlier. The column current depends on the resistance of the memristive devices in each receptive field. Since the contribution of defective low resistance devices to the column current is larger than for defective high resistance[4], even few defective low resistance devices lead to a significant decrease in recognition rate. If all devices are defective, the resulting recognition rate is the same in both cases.

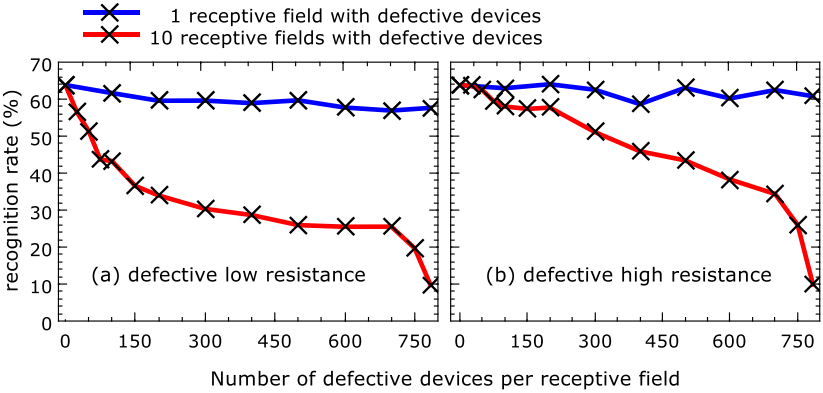


Figure 8.7: Influence of defective devices on recognition rate.

8.2.4 Hardware Implementation

The receptive fields in the simulation contained 784 memristive devices each, and in total 7840 devices for 10 output neurons and 392.000 devices for

[4] A parallel connection of resistors is dominated by the smallest resistor. The total resistance of a receptive field with defective low resistance is close to the resistance of the defective devices, while the total resistance of a receptive field is close to the regular resistance.

50 output neurons. An important question is, which crossbar-array size is possible. Up to this point, only individual devices with rather huge dimensions (see section A.1) were used. The new mask was designed as small as possible, with sufficient safety margins to keep the alignment procedure during lithography as simple as possible. Due to the lack of experience with the new crossbar-structure, only 16 × 16 arrays were designed. Another important aspect is the wiring bonding, since even 32 connections for this type of array make the bonding procedure difficult.

These design decision lead to a significant decrease in number of patterns and to smaller receptive fields. Nevertheless, this implementation serves as a proof-of-principle, which is not limited to small systems.

The small receptive fields have one major drawback, because only black and white patterns instead of gray scale images can be used. Gray scale patterns like in the MNIST dataset would have utilized the analog switching and multi-state capability of the double barrier memristive device, which is one its most interesting features.

8.2.5 Training Phase

Figure 8.8 shows three 6 × 6 pictures with different characters (1,c,u). The receptive fields necessary to learn these characters are of the same size (6 × 6). Because the network features unsupervised learning, it is reasonable to use more receptive fields than input characters. This adds another degree of freedom for the network to increase the number of receptive fields for characters that need an increased learning effort. The use of 5 receptive fields with each 6 × 6 pixels requires a crossbar-array with 180 devices. For this purpose, 180 devices were selected out of 256 devices of the crossbar-array and rearranged into five 6 × 6 sub-arrays. These three patterns are just

examples and can be replaced with any other pattern, which can be drawn using 6 × 6 pixels. Additionally, these characters were chosen adequately to guarantee that they are not too similar. If the size of the receptive fields is too small, the characters look more "artificial" and do not resemble real written characters. If the resolution is increased, the details of each character will automatically lead to fewer similar pixels.

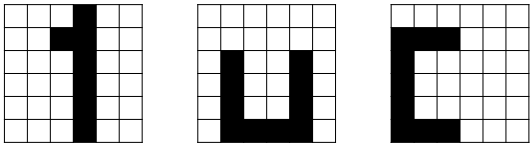


Figure 8.8: 6 × 6 pixel images of the symbols to be applied to the network.

Figure 8.10 shows the learning process for three input characters and five output receptive fields at six instances in time. The first row (i.) shows the initial state of the six receptive fields. The second row (ii.) shows that the fifth receptive field already started to learn the letter "c". The other receptive fields show that the devices of receptive fields, which were not triggered, are reset (higher resistance and brighter color). After more iterations, the number one was learned additionally. The first receptive field, on the other hand, has been triggered by "c" and "u" in the past, because the overlapping characters yield this pattern. In the next iteration (row iv.), however, this pattern vanished because the wrong pixels discourage the further strengthening of this pattern. This is intended, because pixels with strong weights in the receptive field, which are not present in the input pattern, negatively contribute to the threshold voltage. If the contribution from the positive pixels do not outweigh the negative pixels, the receptive fields will over time forget the current pattern. During the last cycles (rows v. and vi.), this receptive field was changing between "c" and "u", but now the "u" seems to be favored over the "c", and continues with this pattern

until the end of the learning phase. Visible in the last row (vi.) is the final state of the receptive fields after the training phase.

It has to be emphasized that the input patterns were not directly assigned to the receptive fields, but merely *offered* to the network, and the network decided, where it would fit best. This of course means that the initial decision, which receptive field represents which pattern is totally random. Figure 8.9 compares supervised and unsupervised learning. Without the *unsupervised* learning procedure, the patterns would only be "written" directly to the receptive fields. This would require a huge training set with labeled patterns (e.g. most probably a human-being who assigns each pattern with the respective character). The unsupervised network, on the other hand, can be fed with unlabeled patterns, and the network assigns the patterns accordingly. After the training phase, only a small labeled dataset is necessary to create the correct association of a receptive field with the character that was learned.

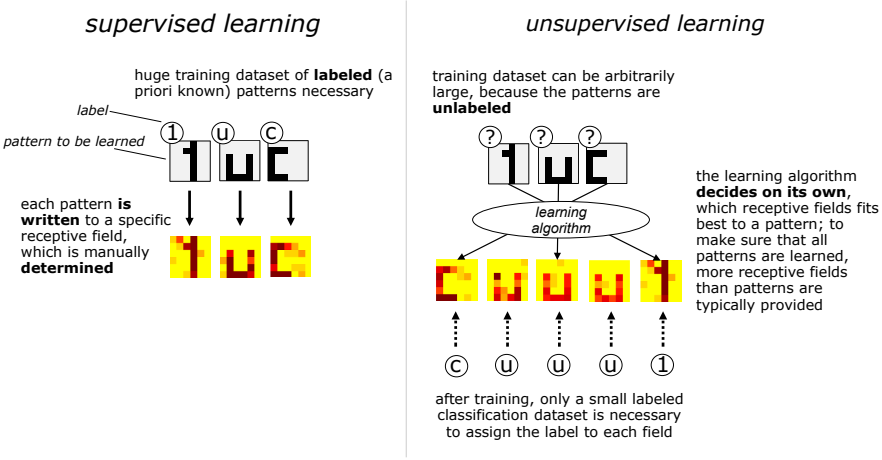


Figure 8.9: Comparison between supervised and the here used unsupervised learning algorithms.

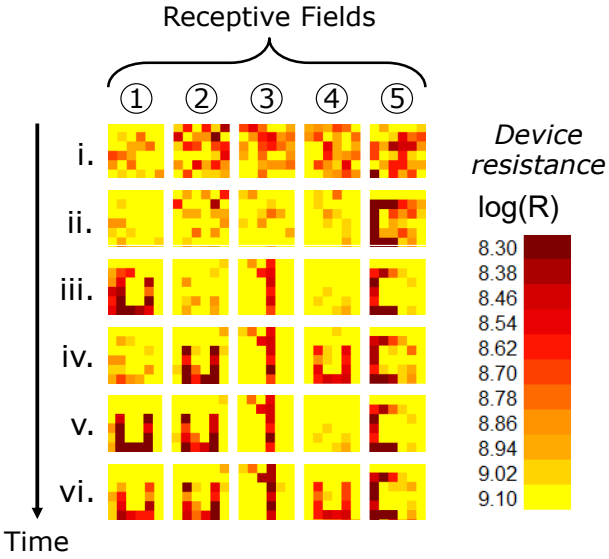


Figure 8.10: The development of the receptive fields for input symbols "1", "c", "u". Due to the unsupervised learning, more output receptive fields (i.e. columns) than input symbols are available. The first row shows the initial state before learning (random resistance). The next rows show the receptive fields at interesting instances in time. The last row shows the final state of the receptive fields, where all three applied input symbols were successfully learned. The scale bar shows the resistance measured at 0.9 V.

8.3 Retention of Receptive Fields

The retention, or the ability for a memristive device to retain its resistance, was already shown in Figure 7.21 for an individual device. This property is of course also important for the learned weights of the network. Figure 8.11a shows how an assembly of 35 devices in the on-state develops over time. For this measurement, the learning procedure was stopped at some point and the state of the receptive fields was repeatedly measured. Unlike the retention measurement in section 7.3.2, the variation between on- and off-state was

only a factor of 10 (because the devices were not driven on purpose to the lowest resistance state). Apart from the second "u", nearly all characters can be clearly distinguished for a period of 40 hours. The shorter retention of the second "u" can be explained with the learning history of this receptive field, because it was less often applied to the receptive field. This indicates, although not studied in detail, that there seems to exist a correlation between the set strength and the ability to retain the resistance state.

Figure 8.11b shows a quantitative analysis of the resistance development for the devices in the on-state from the receptive field with the letter "c". Similar to the single device retention measurement, the resistance initially increases rapidly, but starts to saturate after some time.

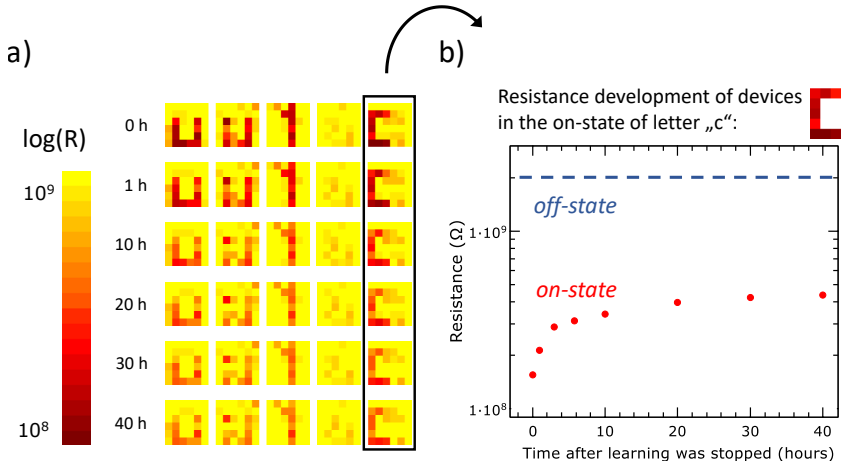


Figure 8.11: Development of on-resistance state after the learning phase was stopped. **a** It can be clearly seen that even after 40 hours the symbols in most of the receptive fields remain readable. The not recognizable letter "u" was less often learned, explaining the shorter retention. **b** Quantitative analysis of the resistance development of the devices in the on-state for letter "c".

Chapter 9

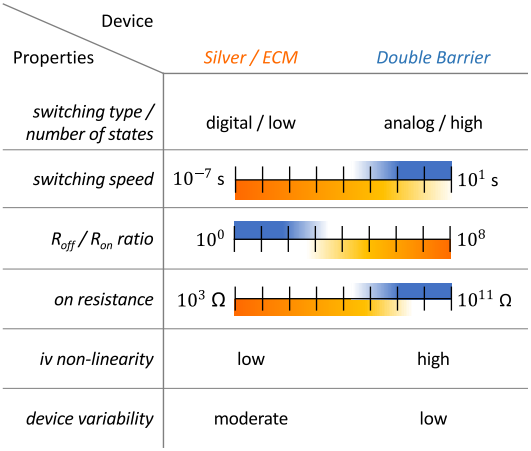
Conclusion

The aim of this thesis was the development of analog memristive devices for the integration in electroforming-free crossbar arrays. To reach this goal, different memristive devices were investigated to increase the understanding on the device properties and requirements.

To accommodate the needs of different neuromorphic applications, two memristive devices were developed with complementary properties. The first device is based on the well-known ability of silver to create a metallic filament in an insulating layer. The second device features a novel interface-based memristive device with an ultra-thin (2.5 nm) niobium oxide layer between a tunneling barrier and a Schottky-barrier. The differences of both devices are illustrated in the following comparison:

Both devices have a huge bandwidth for various parameters, which simplifies the integration into neuromorphic circuits. The silver device shows digital switching due to the creation of silver filaments, while the niobium oxide device is able to gradually adjust its resistance due to the movement of ions in niobium oxide.

Another remarkable difference lies in the switching speed. The silver device is able to change from the off- to the on-state in about 1 microsecond. The niobium oxide device, on the other hand, requires at least milliseconds for a reasonable change in resistance. Although this makes the device unsuitable for memory applications, it is typically considered advantageous



for neuromorphic applications. In contrast to the immediate and drastic resistance change of the silver device, this slow, gradual resistance decrease is more comparable to the weight change of synapses in the brain.

The resistive switching of the double barrier niobium oxide device can be explained by the drift of oxygen ions towards the Schottky-barrier and the resulting change in interface properties. This changes the rectifying properties in the off-state to an almost ohmic current transport in the on-state. This has been observed for different contact sizes equivalently, strongly indicating that this effect occurs homogeneously and not as a localized filament.

The development and characterization of these memristive devices was improved by the implementation of an automated wafer prober. This allowed extensive automated measurements of a huge number of devices without time consuming manual labor. A custom analysis software was developed for wafer-level measurements.

To underline the usability of both devices, they were implemented into neuromorphic circuits. The filament-based silver devices were used in a

circuit to emulate the anticipation behavior of amoeba. This was only possible because the device is able to change its resistance over several orders of magnitude in a very short time. Furthermore, this serves as a good example for the variability in requirements of different neuromorphic applications.

The highly non-linear I-V-characteristic of the double barrier memristive allowed the integration in passive 16×16 devices crossbar arrays without selector devices. These crossbar arrays are among the first to enable a forming-free operation and analog switching properties. Besides the tenfold increase in packaging density, the simplified electrical connection enable neuromorphic circuits with a significantly larger number of devices.

These memristive crossbar arrays were implemented in a circuit for pattern classification, using 180 memristive devices on a single crossbar array. The circuit was able to successfully classify and assign individual input patterns to several 6×6 fields in the crossbar array. This was achieved using an unsupervised learning algorithm, which needed no external input to choose the best number of output fields and the best assignment of input patterns to individual output arrays. This is the first step towards a hardware implementation using electroforming-free, analog memristive devices, and shows that the highly critical step from simulation to hardware realization is possible with high quality devices. Furthermore, it demonstrates the strengths and prospects of the newly developed memristive crossbar arrays.

The memristive devices fabricated in this thesis contributed to the DFG-funded research project FOR2093, by providing measurements for the generation of SPICE, Monte-Carlo and Wave-digital simulations. Apart from the applications shown here, the memristive devices were integrated in numerous neuromorphic oscillator- and ASIC-circuits.

Chapter 10

Scientific Vita

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2002 - 2005	Apprenticeship (industrial electronics technician)
2005 - 2006	General higher education qualification (Allgemeine Hochschulreife) (Rendsburg)

2006 - 2012	Study of Electrical Engineering and Information Technology at Kiel University (Germany) (12 semesters)
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List of Publications

1. M. Hansen, M. Ziegler, H. Kohlstedt, A. Pradana, M. Raedler, and M. Gerken "UV capillary force lithography for multiscale structures", in *Journal of Vacuum Science & Technology B* (2012).
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5. M. Ziegler, M. Hansen, M. Ignatov, and H. Kohlstedt, "Building memristive neurons and synapses", in *Circuits and Systems, IEEE International Symposium* (2014).
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Appendix A

Appendix

A.1 Detailed Description of Mask Layouts

Figure A.1 shows on the left side the complete wafer. The large crosses and squares visible on the left and right hand side aid the alignment between wafer and mask at a macroscopic level for the lithography. This pre-alignment simplifies the microscopic alignment of wafer and mask, because the alignment structures will already be in close vicinity.

The wafer is logically structured into 232 5×5 mm cells. This grid size was chosen in order to yield a high resolution, even if, in the later stages during the wafer characterization, only one contact of each cell would be measured. On the right hand side, one of these 232 cells is shown. The highly ordered grid structure (1×1 mm) was continued here as well. On the left of each subcell, the row and column number of the individual subcell is written. Apart from positions (2,2) and (5,5) all other 23 subcells contain each six memristive devices. The other two subcells contain test structures to troubleshoot fabrication problems. All three types of subcells are shown in Figure A.2.

The subcell containing the memristive devices is shown in Figure A.2a. The rectangular electrode in the center is the common bottom electrode for all six devices. Each contact has two different contact sizes. If the masks

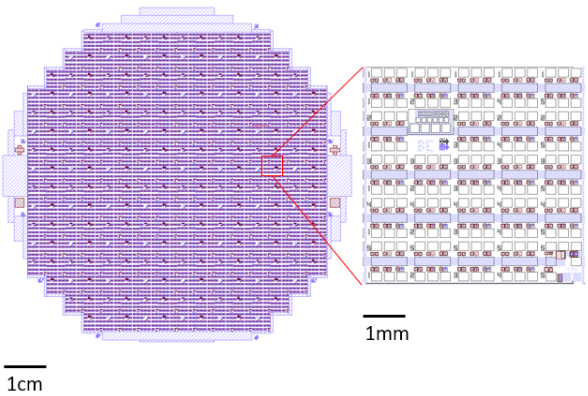

Figure A.1: Full mask layout for 4 inch wafers and one of the 232 subcells (5×5 mm).

are used as shown here, contacts with an area ranging from 100 μm^2 to 2500 μm^2 can be used. If, however, during the last metallization step the mask shown here in black, is shifted by 100 μm, devices with contact areas from 25 μm^2 to 200 μm^2 can be used. This approach was used because it was not clear initially which contact sizes later on would give the best results. If wet etching is used, the isotropic etching leads to a decrease in contact area size which cannot be neglected.

The test structures of Figure A.2b are available after the second (of four) lithographic steps. After etching, these structures can be used as memristive devices. The large area surrounding the squares is the bottom electrode, while the squares are the top electrode. If a tip of a micromanipulator is placed carefully on top of these squares (to avoid pinching through the top electrode), the memristive properties of the fabricated devices can be evaluated without the remaining fabrication steps. This was regularly used during the fabrication of totally new devices because it is typically not clear in the beginning weather the fabricated stacks exhibit memristive properties.

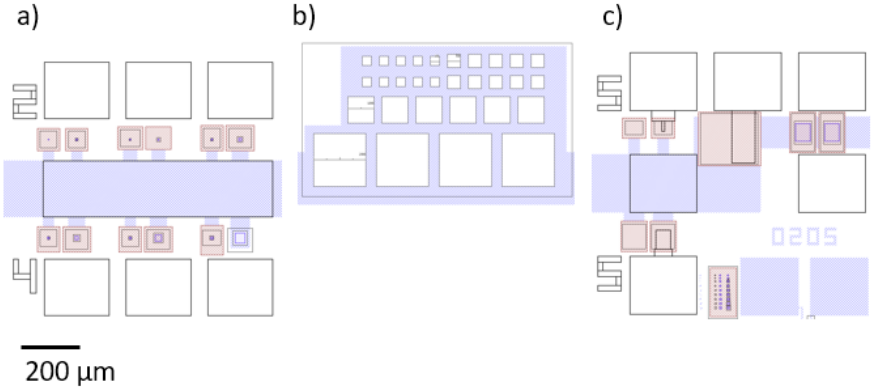

Figure A.2: Different types of subcells in each 5×5 mm cell. **a** Memristive devices with six different areas. 23 of 25 subcells contain this type of cell. **b** Simple structures to evaluate electrical properties of the devices before the wafer is fully processed. **c** Test structures to evaluate the quality of the fabrication process.

If this is not the case, the time consuming next steps could be avoided. According to section 3, all necessary components of the active memristive layers are deposited during the first deposition step. The question arises why the following steps are actually necessary: It cannot be stressed enough that this step requires very careful operation of the micromanipulator, which makes it very hard to achieve reproducible measurements. Furthermore, automatic measurements or wire bonding of devices is impossible. All these problems are avoided with the help of the next steps, which create a contact pad next to the device. This makes it impossible to damage the device by directly contacting it.

Figure A.2c contains three types of test structures. The first type contains three devices, where the insulation resistance for three different areas can be measured. Although this measurement is not always done, it is very helpful to measure the insulation resistance if the memristive devices themselves

show an explainable low resistance. A common reason for low resistance devices is a problem during the deposition of the insulation.

The next set of test structures is connected across the top electrode. This is important to guarantee that the contact resistance between the wiring metallization and the top electrode creates low resistance connection. This can be problematic in cases, where a material which easily oxidizes in air is used as the top electrode. Although the cleaning step before the deposition of the wiring should remove this native oxide, failure to do so would be visible in this measurement.

The previous masks were primarily used for the characterization of memristive properties and basic neuromorphic circuits. In order to achieve a larger number of memristive devices, it was necessary to use a different type of mask layout. The layout is described in more detail in section 3.1. Unlike the previous mask, there are no test structures to get the highest density of crossbar arrays (Figure A.3).

Using this type of layout, it was possible to get in total $\approx$ 320,000 devices on one wafer (the previous single contacts allowed only $\approx$ 32,000 contacts). Although it is possible to cut the wafer into individual chips containing each one crossbar array, this was not done in order to make handling of the diced samples easier. Typically, samples of 6.6×6.6 mm containing nine crossbar arrays were used.

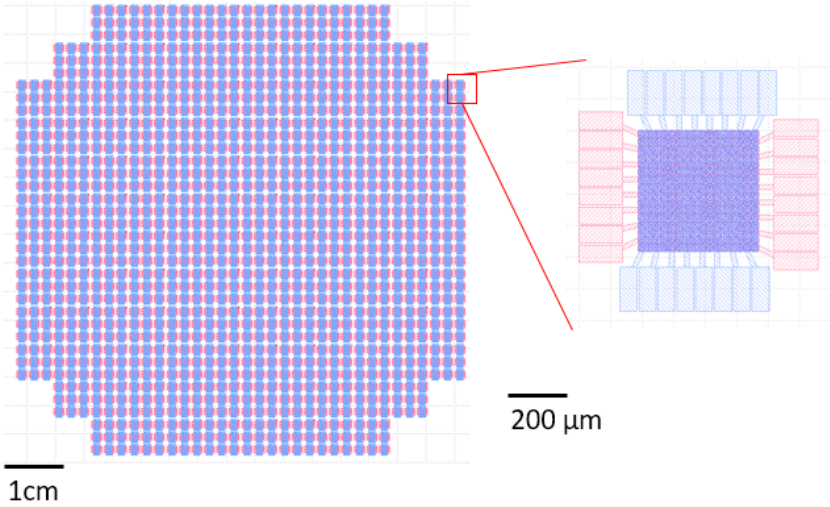

Figure A.3: Complete wafer layout with memristive crossbar arrays and single crossbar array with 256 devices.

A.2 Resistance Distribution of Reactively Sputtered Materials

The resistance maps in this section were recorded during this PhD thesis and show the vast differences which can be observed using reactive sputtering.

Thick Aluminum Oxide

Figure A.4 shows the influence of the sputtering on a rotating sample. The resistance map shows the distribution of the resistance across a wafer with oxidized aluminum. Similar to the fabrication of the Josephson junctions in chapter 7.1.2, niobium and aluminum is sputtered and afterwards oxidized. Due to the self-limitation of the aluminum oxidation[RKGG00], only the first $\approx$ 1-2 nm are converted into aluminum oxide. In order to fabricate aluminum oxide layers with a larger resistance, two more aluminum layers ($\approx$ 0.7 nm) were sputtered and oxidized. This leads to thicker aluminum layer and an increase in resistance. While the first aluminum oxide layer will be independent of the sputtered aluminum thickness, the thickness of the additional aluminum oxide layers will depend on the deposition rate across the wafer. The influence of the sample rotation during sputtering can be clearly seen in the resistance distribution in the wafermap, where the resistance is largest in middle (thicker aluminum) and decreases towards the left and right hand side of the wafer (thinner aluminum).

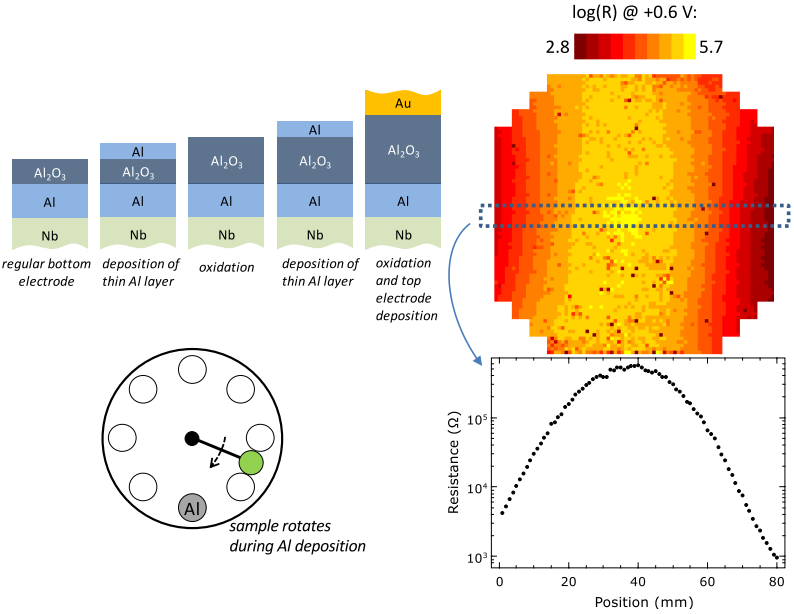

Figure A.4: Resistance map of Nb/Al/Al_2O_3/Au devices.

Aluminum Nitride

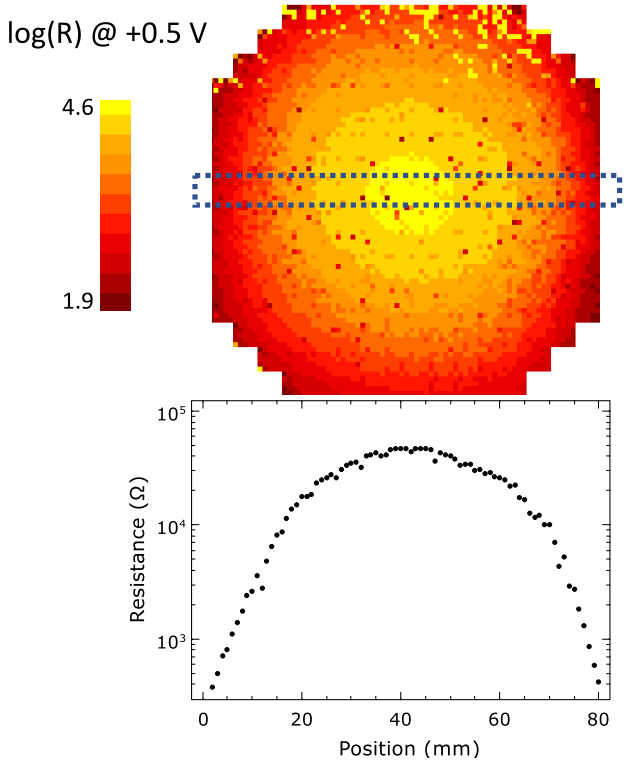

Figure A.5: Resistance map of reactively sputtered AlN-films

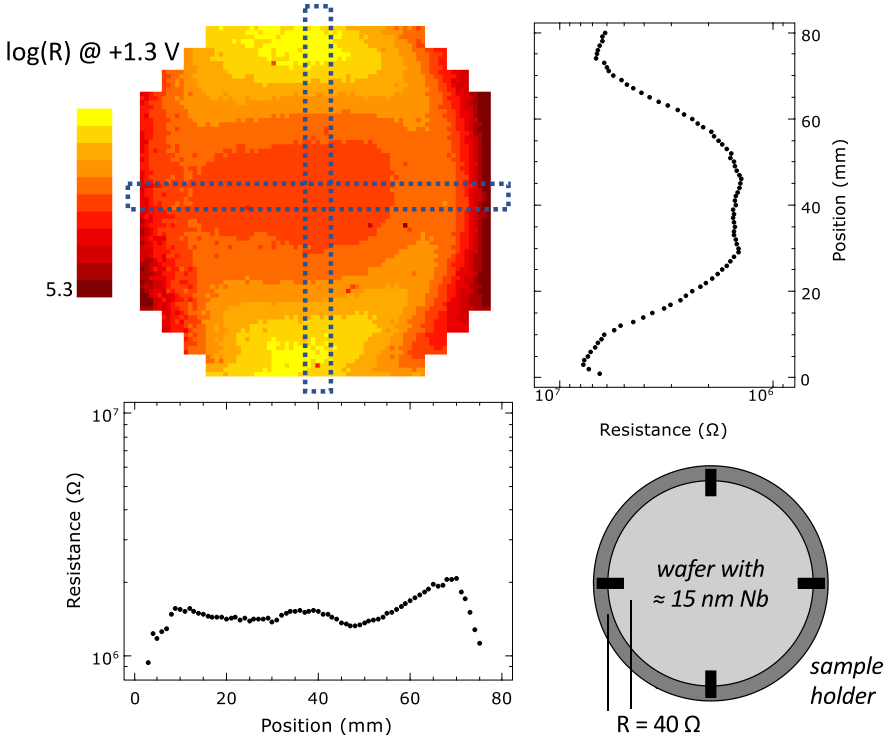

Figure A.6: Resistance map of Nb/Al-Al_2O_3/Nb_xO_y/Au devices on an electrically connected substrate. Deposition conditions similar to the samples of Figure 7.12.

A.3 Multiplexing Circuit to Address Wire-Bonded Crossbar Arrays

The only feasible way to connect crossbar arrays is via bond wires on a PCB sample holder. This sample holder is then placed into a zero insertion force socket (ZIF). These sockets are connected to analog switches as shown in Figure A.7. The circuit consists of eight analog switches (4×4 connections for top and bottom electrode). The input signal for top and bottom electrode is applied to the input-SIDE of all analog switches. This voltage is applied to the selected device by selectively turning a switch for top and bottom electrode. Since only one device was going to connect it in this variant of the circuit, the selection was simplified in order to avoid 32 connections from a microcontroller to the circuit. By using a 4-to-16 converter, the microcontroller only has to apply four bit binary value ("0000"...."1111") to the converter. This address selection has an additional advantage, because only one analog switch (for each electrode) can be turned on at a time. This avoids complications due to programming or timing errors due to several simultaneously turned on switches. The analog switches used were carefully selected: The analog switches come in a multitude of variance and have different advantages and disadvantages, which had to be evaluated. The most trivial possibility would be to take lowest resistance switches, because this would resemble the typical wire connection the most. This however is problematic because this low resistance is achieved by using very large MOSFETs and are accompanied by large parasitic capacitors. The capacities might later on disturb the operation due to the transient behavior of the applied voltage. Analog switches for signal transmission with some kOhm resistances might disturb the switching behavior. If the current through the switch and the memristive device is large (> 100 μA), the voltage drop across the switch decreases the voltage available to the memristive device. While this might be acceptable for linear resistors (because it can

be compensated by adjusting the voltage), this is impossible to take into account for highly non-linear devices like, for example, memristors. Due to the exponentially increasing current, the voltage applied to the memristive device would decrease rapidly. Thus, analog switches with an on resistance of $\approx 20\ \Omega$ were used.

The sample holder itself went through several iterations in order to facilitate the bonding procedure. The contact pads for the top and bottom electrodes on the crossbar die surround the contacts in blocks of eight pads. Each of these blocks is ≈ 1 mm wide because the contacts on the PCB cannot be spaced so close together.

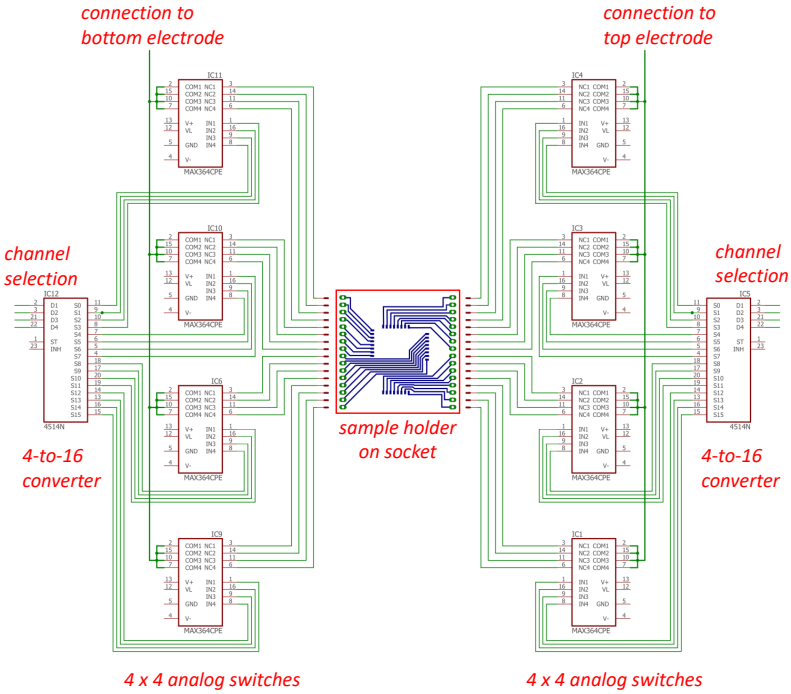

Figure A.7: Schematic of the circuit for the connection of 16×16 crossbar arrays. The individual connections are established using analog switches for every connection. The individual device is selected by a microcontroller, which applies a four bit value to a 4-TO-16 converter, which selects the individual connection. This is done separately for the top and bottom electrode.

A.4 Printed-Circuit-Board (PCB) fabrication

For the fabrication of sample holders and electronic circuits, it was necessary to fabricate printed-circuit-boards (PCB). These PCB consist of either of single or double-sided copper layers. With the help of a PCB design software (Autodesk Eagle), the layout of the circuits was created and printed onto semi-transparent paper. These printouts were then sprayed with Toner-Density-Spray to increase the density of the black colour. Afterwards, a very common procedure which is comparable to the lithography done on wafers, was performed. The printed foils were placed on the photoresist-covered copper layers and exposed to UV light. The exposed parts were developed in an aqueous sodiumhydroxide solution (1 wt. %). In the next step, the copper was etched off in a ferric chloride solution. In order to ensure a homogeneous etching rate, the etching bath was either agitated or the PCB was constantly brushed. The latter procedure usually led to the best results because the additional mechanical abrasion led to increased etching rates and thus reduced the critical under-etching of the structures. With careful design and processing, traces with a thickness of ≈ 0.3 mm are possible.

A.5 Deposition Parameters

step	description	pre-time	sputtering	misc
402	Nb sputtering	25 s	360 W; 25 sccm Ar; 15 s	
419	Al sputtering	30 s	100 W; 40 sccm Ar; 150 s	4 rotations
261	Al oxidation	-	-	100 mbar; 1200 s

Table A.1: Pre-sputtering conducted prior to sample deposition.

step	description	pre-time	sputtering
-5144	transfer to Nb	-	-
402	Nb sputtering	25 s	360 W; 25 sccm Ar; 15 s
419	Al sputtering	30 s	100 W; 40 sccm Ar; 70 s; 2 rotations
-4457	transfer to OK	-	-
261	Al oxidation	-	*100 mbar; 1200 s*
491	pre-sputtering Nb_xO_y	30 s	100 W; (7,23) sccm (Ar, O2); 25 s
-5744	transfer to Nb	-	-
491	Nb_xO_y deposition	30 s	100 W; (7,23) sccm (Ar, O2); 25 s
-4443	transfer to Au	-	-
496	Au deposition	10 s	50 W; 10 sccm Ar; 60 s
-4351	transfer to loadlock	-	-
402	cleaning of Nb target	25 s	360 W; 25 sccm Ar; 15 s

Table A.2: Typical deposition procedure for double barrier memristive devices.

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