

Thermally-Compensated Modulation Strategies for Modular Power Converters

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M. Sc. *Youngjong Ko*

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1. Committee: Prof. Marco Liserre, Dr.-Ing.
 2. Committee: Prof. Joachim Böcker, Dr.-Ing.
 3. Committee: Prof. Peter A. Höher, Dr.-Ing.
 4. Committee: Prof. Thomas Meurer, Dr.-Ing.
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English Summary

Power electronics converters are widely employed in various fields to take the advantages of controllability and high energy conversion efficiency. Especially, a modular structure is getting attention, which inherently exhibits a constitution of multiple basic cells rated for a lower power. This feature not only allows the reduced voltage and current slew rate but also provides the flexibility in power scalability. In addition, the redundancy of the modular structure enables an easy fault tolerant operation. Nevertheless, the reliability issue has been intensively argued in literature due to the higher number of power semiconductor devices and capacitors, which show the highest failure rate in power electronics systems.

Based on the Physics-of-Failure approach, it has been revealed that the thermal stresses, mean junction temperature and junction temperature swing, are highly responsible for the major failures of the power semiconductor devices. Therefore, it is motivated to compensate the thermal stresses in order to achieve a longer lifetime. The active thermal control methods have been considered, since they can be simply adopted by a software. However, the existing methods technically intend to increase the losses for compensating the temperature swing, which implies a limited lifetime improvement and a decreased efficiency.

Considering the modular converter consisting of modular inverter and DC/DC converter, two active thermal control methods based on modulator are proposed: multi-frequency and discontinuous modulations, for performing the power routing, which aims at controlling a loading power of each module. The DC/DC converters connected in parallel can have a different loading according to their remaining useful lifetime, which shall aim at either prolonging the lifetime of the whole system or planning maintenance. Remarkably, the discontinuous modulation allows to improve not only the reliability of the DC/DC converters by the power routing but also that of the inverter by reducing its losses. Consequently, the thermal compensation is achieved with a lower mean junction temperature and a higher efficiency.

As another device prone to failure, electrolytic capacitors are mainly degraded due to the thermal stresses, which are determined with equivalent series resistance and capacitor current. Therefore, the major task is to reduce the capacitor ripple current. The optimal DC-link design approach has been introduced in literature to reduce either low-frequency components caused by a power flow or high-frequency components due to switching behavior. However, a clear relation between the frequency of the capacitor current and the thermal stresses has not been investigated yet.

The power converter for deriving the relation is proposed, which can inject a designated AC current and DC bias voltage to a capacitor under test. For clear result, Total Harmonic Distortion (THD) is considered as a major criterion in designing the topology. The multi-level converter is most suitable, since it achieves a lower THD with a lower filter. In addition, a lower voltage drop on the filter allows the use of a lower DC-link voltage and lower blocking voltage rated power devices. Also, the proposed control scheme enables to simultaneously regulate two parameters, AC current and DC bias voltage. Through the setup, the correlation between the current frequency and the hot-spot temperature is experimentally derived.

Deutsch Kurzfassung der Arbeit

Stromrichter sind in verschiedenen Feldern weit verbreitet, um die Vorteile der Regelbarkeit und der effizienten Umwandlung auszunutzen. Insbesondere modulare Strukturen sind attraktiv, da sie grundsätzlich eine Zusammensetzung aus multiplen Basis-Zellen, ausgelegt für eine geringe Leistung, sind. Diese Eigenschaft ermöglicht nicht nur reduzierte Spannungs- und Stromanstiegsraten, sondern auch Flexibilität in der Leistungsskalierbarkeit und im Fehlertoleranz-Betrieb. Es wurde jedoch sehr intensiv über den Zuverlässigkeitsaspekt diskutiert und zwar aufgrund der höheren Anzahl an Leistungshalbleitern und Kapazitäten, welche die höchsten Fehlerraten in leistungselektronischen Systemen aufweisen.

Basierend auf dem "Physics-of-Failure" Ansatzes ist bekannt, dass die thermischen Belastungen - durchschnittliche Sperrschichttemperatur und Sperrschichttemperatur Zyklen - in einem hohen Maße verantwortlich für die meisten Fehler der Halbleiter sind. Daher ist es begründet, die thermische Belastung zu reduzieren, um eine längere Lebenszeit zu ermöglichen. Die aktiven thermischen Regelungs-Methoden werden berücksichtigt, da sie softwarebasiert realisierbar sind. Jedoch beabsichtigen existierenden Methoden eine Erhöhung der Verluste zur Kompensation der thermischen Zyklen.

Für den modularen Stromrichter, bestehend aus modularen Umrichter und DC-DC Wandler, werden zwei aktive thermische Regelungen vorgeschlagen: Multifrequenz Modulation und Diskontinuierliche Modulation (DPWM) zum Leistungsrouting um das Leistungsprofil jedes Moduls zu regeln. Die parallelen DC-DC-Wandler können in Abhängigkeit ihrer verbleibenden Lebenszeit unterschiedlich belastet werden. Dies wird genutzt um entweder die verbleibende Lebenszeit des Systems zu verlängern oder Reparaturarbeiten zu vollziehen. Bemerkenswerterweise führt die DPWM zu einer Verbesserung der Zuverlässigkeit des DC-DC-Wandlers durch das Leistungsrouting und zu einer Verbesserung des Umrichters durch eine Reduktion der Verluste. Folglich wird die thermische Kompensation mit einer geringeren durchschnittlichen Sperrschichttemperatur und einer höheren Effizienz realisiert.

Ein weiteres fehleranfälliges Bauteil ist der Elektrolytkondensator, der vorwiegend durch thermischen Stress degradiert wird, welcher durch den äquivalenten Serienwiderstand und den Kapazitätsstrom bestimmt ist. Daher muss der Ripplestrom durch die Kapazität verringert werden. Der optimale Designansatz des DC-Zwischenkreises wurde in der Literatur eingeführt, um entweder die niederfrequenten Komponenten oder die hochfrequenten Komponenten zu reduzieren. Jedoch wurde der eindeutige Zusammenhang zwischen der Frequenz des Kapazitätsstromes und der thermischen Belastung bisher nicht untersucht.

Der Zusammenhang wird mittels eines Stromrichters hergeleitet. Dieser kann einen vorgesehenen AC-Strom und eine DC-Spannung in eine Testkapazität einspeisen. Für ein eindeutiges Ergebnis ist der THD-Wert zu berücksichtigen. Der Multi-Level-Stromrichter erzielt geringere THD-Werte bei kleineren Filtern, welche eine reduzierte Zwischenkreisspannung ermöglichen und somit die Verwendung von geringer ausgelegten Bauteilen. Das Parallel-Regelungs-Schema ermöglicht die Regulierung von zwei Parametern simultan. Die Korrelation zwischen Stromfrequenz und der Temperatur ist experimentell abgeleitet.

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Used symbols and abbreviations

General symbols

u or $u(t)$ Instantaneous value

Superscripts

*

Reference

th

Order

Subscripts

avg	Average
bal	Value under balanced condition
ce	Collector-emitter
d	diode
dc	DC-link
g or $grid$	grid
j	Junction
jc	Junction to case
max	Maximum value
min	Minimum value
ov	Additional loading
pk	Peak value
sw	Switching
t	Total
th	Thermal
tr	Transistor
AC	Alternating current
DC	Direct current
L	Filter inductor
LV	Low-voltage
MV	Medium-voltage

Special symbols

a, b, c Constants for curve fitting

a_1, a_2, a_3 Constants for lifetime model

α, β, γ	Weibull parameters
α_1, β_1	Fourier first-order coefficients
C	Capacitance
C_D	Capacitance for dielectric loss
C_{th}	Thermal capacitance
δ	Effective duty cycle
δ_d	Effective duty cycle for diode
δ_{ov}	Effective duty cycle for additional loading cell
δ_{tr}	Effective duty cycle for transistor
δ_{un}	Effective duty cycle for unloading cell
ΔI_L	Amplitude of switching ripple current on filter inductor
ΔT	Temperature variation
$\Delta T_{c,a}$	Temperature difference between case and ambient
$\Delta T_{h,a}$	Temperature difference between hot-spot and ambient
ΔT_j	Amplitude of thermal cycling
D	Accumulated damage
D_i	Damage by i^{th} stress level
E_a	Activation energy
$E_{avg,sw}$	Average switching energy
$E_{d,off}$	Switching turn-off energy of diode
$E_{d,sw}$	Switching energy of diode
$E_{ov,sw}$	Switching energy of additional loading cell
E_{sw}	Switching energy
$E_{tr,off}$	Switching turn-off energy of transistor
$E_{tr,on}$	Switching turn-on energy of transistor
$E_{tr,sw}$	Switching energy of transistor
$E_{un,sw}$	Switching energy of unloading cell
$f_{0,LV}$	Frequency of low-voltage grid
f_{Ic}	Frequency of capacitor test current
f_{sw} or f_S	Switching frequency
$F(t)$	Unreliability
h_{11}, h_{12}, h_{13}	Amplitude of fundamental carrier harmonics group
i_g	Grid current
$i_{link,c}$	DC-link capacitor current
$i_{link,g}$	DC-link current in grid side
$i_{link,m}$	DC-link current in machine side
$i_{C,ac}$	AC current for capacitor test
I_c	Collector current
I_{pk}	Peak value of current
J_{2n-1}	Bessel function of order $2n - 1$
K	Number of total cells
K_B	Boltzmann constant
m	order of carrier harmonics

$m_{1,off}$	Offset component of cell 1 for discontinuous modulation
$m_{2,off}$	Offset component of cell 2 for discontinuous modulation
$m_{3,off}$	Offset component of cell 3 for discontinuous modulation
m_c	Clamped modulation signal
$m_{c,off}$	Offset component for clamped modulation
m_f	Fundamental component of discontinuous modulation signal
m_{nc}	Non-clamped modulation signal
$m_{nc,off}$	Offset component for non-clamped modulation
m_{offset}	Offset component for discontinuous modulation
m_{ATC}	Modulation signal for active thermal control
m_{THD}	Modulation signal for power quality improvement
M	Modulation index
M_1, M_2, M_3	Modulation index of each cell
M_{bal}	Modulation index under balanced condition
M_c	Modulation index for clamped signal
M_{nc}	Modulation index for non-clamped signal
M_{ov}	Modulation index for additional loading
M_{un}	Modulation index for unloading
n	order of modulation signal harmonics
n_i	Number of cycle for i^{th} stress level
N	Number of additional loading cells
N_f	Number of cycle to failure
L	Lifetime
L_0	Lifetime at nominal condition
L_S	Equivalent series inductance
ω_0	Pulsation of modulation signal
ω_c	Pulsation of carrier signal
ϕ	Power factor angle
P	Active power
P_1, P_2, P_3	Loading power of each path
P_{cd}	Conduction loss
P_d	Total loss of diode
$P_{d,cd}$	Conduction loss of diode
$P_{d,sw}$	Switching loss of diode
P_{load}	Loading power
P_{loss}	Power loss
$P_{nominal}$	Nominal power
$P_{ov,cd}$	Conduction loss of additional loading cell
P_{pd}	Power dissipation
P_{sw}	Switching loss
$P_{sys,t}$	Total system power loss
P_t	Total power loss of single device
P_{tr}	Total loss of transistor

$P_{tr,cd}$	Conduction loss of transistor
$P_{tr,sw}$	Switching loss of transistor
P_{un}	Loading power of unloading cell
$P_{un,cd}$	Conduction loss of unloading cell
$P_{LV,DC}$	Active power in low-voltage DC grid
$P_{LV,S}$	Active power of storage system in low-voltage DC grid
P_{MV}	Active power in medium-voltage grid
Q_{MV}	Reactive power in medium-voltage grid
r_{d0}	Equivalent resistance of diode
R_f	Frequency-dependent resistance of dielectric layer
r_{tr0}	Equivalent resistance of transistor
R_0	Resistance of capacitor terminal, taps and foils
R_p	Insulation resistance
R_t	Temperature-dependent resistance
$R_{t,b}$	Temperature-dependent resistance at base temperature
R_{th}	Thermal resistance
$R_{th,jc}$	Thermal resistance between junction to case
R_D	Resistance for dielectric loss
R_{ESR}	Equivalent series resistance
R_{LV}	Resistive load in low-voltage grid
R_{MV}	Resistive load in medium-voltage grid
R_S	Equivalent series resistance
θ_i	Relative phase of i^{th} cell
t_{on}	On-state period
T	Temperature
T_0	Temperature at test condition
T_a	Ambient temperature
T_b	Base temperature
T_c	Case temperature
T_j	Junction temperature
$T_{j,mean}$ or T_m	Mean junction temperature
T_s	Hot-spot temperature
T_{sw}	Switching period
φ	Clamping angle
v_1, v_2, v_3	AC side voltage of each cell
$v_{1,1}, v_{2,1}, v_{3,1}$	Fundamental component of each cell
$v_{1,3}, v_{2,3}, v_{3,3}$	Third harmonic component of each cell
v_c	Fundamental component of clamped modulation
v_g	Grid voltage
v_{inv}	Inverter AC side voltage
$v_{m,ac}^*$	Output of current control
v_{nc}	Fundamental component of non-clamped modulation
$v_{C,r}$	Ripple voltage of capacitor under test

v_L	Voltage drop on filter inductor
V_0	Nominal voltage
V_1, V_2, V_3	Amplitude of main harmonics for each cell
V_a	Applied voltage
V_{base}	Reference DC-link voltage used for $E_{sw} - I_c$ characteristic
V_{ce0}	Initial value of collector-emitter voltage (on-state voltage)
V_{ce}	Collector-emitter voltage (on-state voltage)
V_{dc}	DC-link voltage
$V_{dc,1}, V_{dc,2}, V_{dc,3}$	DC-link voltage for each cell
V_f	Diode forward voltage
V_{f0}	Initial value of diode forward voltage
V_{grid}	Amplitude of grid voltage
V_m^*	Final reference of parallel control
$V_{m,dc}^*$	Output of voltage control
V_C	Capacitor voltage
$V_{C,dc}$	DC bias voltage of capacitor under test
$V_{MV,AC}$	Amplitude of medium-voltage grid
$V_{MV,DC}$	Medium-voltage DC-link voltage
$V_{LV,AC}$	Amplitude of low-voltage grid
$V_{LV,DC}$	Low-voltage DC-link voltage
V_S	Source voltage
$Z_{th,jc}$	Thermal impedance between junction to case

Abbreviations

Al-Cap	Aluminum Electrolytic Capacitor
BPF	Band-Pass Filter
CAN	Controller Area Network
CHB	Cascaded H-Bridge
CTE	Coefficient of Thermal Expansion
CUT	Capacitor Under Test
DBC	Direct Bonded Copper
DCM	Distributed Commutations Modulation
DFT	Discrete Fourier Transformation
DPWM	Discontinuous Pulse Width Modulation
DUT	Device Under Test
EMI	Electro-Magnetic Interface
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
Ext-DCPWM	Extended Double Carrier Pulse Width Modulation
FFT	Fast Fourier Transformation

HB	H-Bridge
HV	High-Voltage
IGBT	Insulate Gate Bipolar Transistor
LMS	Least Mean Square
LV	Low-Voltage
MEA	More Electric Aircraft
MLC-Cap	Multi-Layer Ceramic Capacitor
MOSFET	Metal Oxide Semiconductor Field Transistor
MPPF-Cap	Metalized Polypropylene Film Capacitor
MPPT	Maximum Power Point Tracking
MV	Medium-Voltage
NPC	Neutral Point Clamped
NR	Newton-Raphson
PCC	Point of Common Coupling
PF	Power Factor
PI	Proportional-Integral
PMSG	Permanent Magnet Synchronous Generator
PMSM	Permanent Magnet Synchronous Machine
PMV	Power Manipulating Variables
PoF	Physics-of-Failure
PR	Proportional-Resonance
PSPWM	Phase-Shifted Pulse Width Modulation
PV	Photovoltaic
PWM	Pulse Width Modulation
QAB	Quadruple Active Bridge
RMS	Root Mean Square
SF	Sensitivity Factor
SRM	Switched Reluctance Machine
SSC	Stacked Switched Capacitor
SST	Solid-State Transformer
ST	Smart Transformer
STATCOM	Static Synchronous Compensator
S-TRU	Smart Transformer-Rectifier Unit
SVM	Space Vector Modulation
TAB	Triple Active Bridge
THD	Total Harmonic Distortion
TRU	Transformer-Rectifier Unit
TSEPs	Temperature Sensitive Electric Parameters
WT	Wind Turbine
WTHD	Weighted Total Harmonic Distortion
ZVS	Zero-Voltage Switching

1 Introduction

Failure rate of power electronics converters is typically referred as 'bathtub' in time domain as shown in Fig. 1.1, where the observed (overall) failure rate reflects the three failure rates: early, random and wear-out (fatigue) failure rate [1, 2]. In the following, the characteristics of each failure rate is simply introduced, considering the typical lifetime of a system.

- Early failure is mainly caused due to either incompatible operating conditions such as continuous exposure to over-voltage, -current and -temperature or improper mechanical installations such as incorrect fixation and poor soldering, thus, the high failure rate is shown at the beginning of operation. However, this failure is recently disregarded with advanced manufacturing and debugging process.
- Random failure is mainly related to single event of extremely over-voltage or -current, which shall be randomly occurred in the whole lifetime. Therefore, it is difficult to predict and prevent the failure and expressed as a low and constant rate.
- **Wear-out (fatigue) failure** is a result of ageing mechanisms over time, its failure rate is therefore increasing at the end of life. Remarkably, there has been continuous efforts to model and predict the wear-out failure and it has been identified that the major failure mechanisms are closely related to thermal stresses [3].

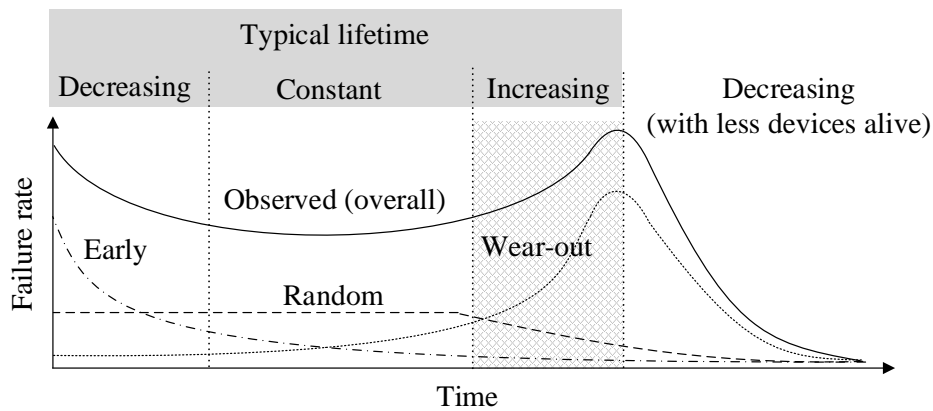


Figure 1.1: Typical failure rate of power electronics systems.

This section motivates the needs of strategy development, which targets at addressing the wear-out failures, so as to achieve a highly reliable power converter by reducing the thermal stresses caused by a mission profile. Here, the reliability is defined as the ability of a system to perform its intended functions for a desired period. The representative reliability-related strategies, which have been conducted in literature, are briefly introduced to formulate the research proposal of the thesis. The structure of the thesis is then presented and the publications during this study are finally listed.

1.1 Reliability of Power Electronics Converters

The power electronics converters are employed in various industrial applications that require better energy conversion efficiency and control performance. These are achieved with help of the innovative technologies in power semiconductor devices and digital signal processors [4, 5, 6]. One of the most popular applications has been, over a decade, on the renewable energy system fed by either wind or sun, as a part of the effort to resolve the global warming issue. The number of their installation and the power capacity of individual system have been continuously increasing [7, 8]. This trend has imposed a requirement of more reliable system in order to be competitive with the market requirements (safety, maintenance costs and energy losses) and to ensure the uninterrupted power supply (power security). On the other hand, the increase of renewable energy systems and new loads such as electric vehicle charging stations, lead challenges for the present grid due to a fast changed power flow direction. This paradigm calls for a new concept of the grid [9]. The Smart Transformer (ST) is one of the promising solution as providing a potential possibility for a significant flexible power flow management with DC grid connectivity [10]. Nevertheless, one of the most important challenge, which has been argued in [11], is to achieve enough reliability to compete with line-frequency passive transformers. Consequently, the reliability has become one of the important and essential performance evaluation metrics of the power converters in addition to the conventional metrics such as the energy efficiency, the power quality and the power density.

According to real field experiences, the power converter is one of the parts most prone to failures in the renewable energy system, being reported 13 % of failure in Wind Turbine (WT) [12] and 37 % in Photovoltaic (PV) systems [13]. More precisely, power semiconductor devices and capacitors are most prone, and they are responsible for 20 % and 34 % of failure, respectively, among the components contained in the power converter [14]. Therefore, they can be referred as the reliability-critical components and become the casting voter for the whole system's lifetime.

In order to evaluate the reliability, the pure failure statistics method has been widely applied in electronic system applications, which utilizes data obtained from reliability tests with a large number of components. The failure rate is regarded as Failure In Time (FIT). However, the FIT reliability metric does not provide any comprehensive information about the required lifetime of single component and it is application-dependent. Moreover, the constant failure rate is only applicable in the constant failure region of the bathtub curve shown in Fig. 1.1. Consequently, the constant failure rate methods are regarded as inapplicable for power electronics applications [15], since the wear-out process is non-linear and dependent on various factors.

In order to better estimate the lifetime of a component, B_x lifetime is used, which is defined as time at which x percentage of components are failed and is calculated from the unreliability curve, $F(t)$, given by

$$F(t) = 1 - \exp \left[- \left(\frac{t - \gamma}{\eta} \right)^\beta \right] \quad (1.1)$$

where α , β and γ are the Weibull parameters and t is time [16].

The Physics-of-Failure (PoF) approach, which provides a better understanding of wear-out failure and an evaluation of the reliability performance, has been proposed [17]. With PoF models, the wear-out of power electronics components can be estimated considering the operating environmental conditions and the mission profile.

The lifetime characteristics of a power semiconductor with PoF lifetime model is shown in Fig. 1.2, where the B_{20} lifetime is indicated as lifetime metrics.

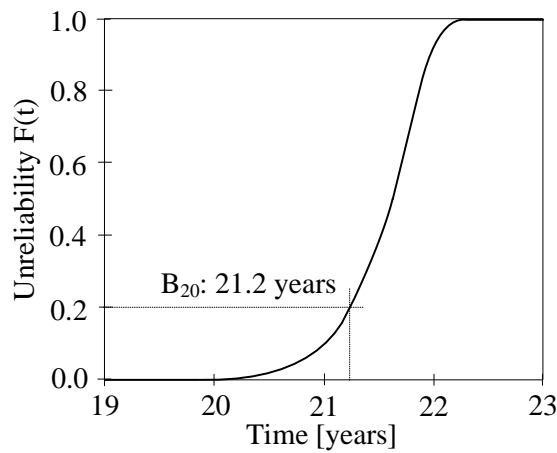


Figure 1.2: Unreliability curve of power semiconductor with PoF model.

On the other hand, it has been found that, the failure mechanisms of power semiconductor devices and capacitors are highly dependent on thermal stresses [17, 18, 19]. In literature works, various strategies to delay the thermal-dependent failures have been proposed and they can be generally divided into two approaches: hardware- and software-oriented.

- Reliability-oriented design aims at achieving a sufficient robustness of each component or a system by making up for its deficiencies through the hardware design approach. In the power converters, cooling system [20], power module package [21, 22] and interconnection [23] have been considered as a possible candidate.
- **Active thermal control** utilizes a software based modulation or algorithm to modify the loss-related variables with the purpose of reducing the thermal stresses [24, 25].

The active thermal control is cost-effective solution compared with the hardware-oriented approach, but it could require either an accurate estimation of the junction temperature or an advanced technique to directly measure the junction temperature. On the other hand, the reliability needs to be evaluated. A PoF based lifetime model [17], which is derived from an accelerated aging test [26, 27, 28], is widely applied in order to estimate the accumulated damage under a mission profile. In addition, since the mission profile of renewable energy

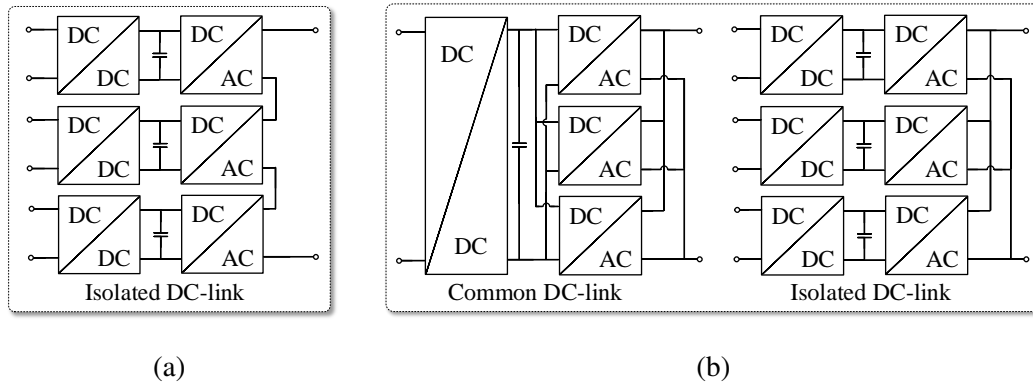


Figure 1.3: Configuration of modular converters: (a) series connection and (b) parallel connection.

systems and ST application, is neither constant nor predictable, a cycle counting method is utilized to decompose the profile [15, 29].

In this thesis, the modular converters are considered, which are categorized in accordance with the AC-side connection: series and parallel as shown in Fig. 1.3. The advantage of these modular converters are described in the below.

- Flexible voltage and power scalability.
- Flexible fault tolerance strategy with redundancy cells.
- Reduced Electro-Magnetic Interface (EMI) emission by lower dv/dt and dil/dt .
- Smaller output filter requirement.
- Multi-level AC output voltage (only for the series connection).

As aforementioned, the series and parallel modular converters feature attractive strength compared with non-modular converters. However, there has been concern about the reliability of the modular converters due to the higher number of power devices and capacitors, which show the highest failure rate in power converter systems [14]. In order to address the reliability issue, it would be worth to mention the general operation and maintenance strategy for the modular converters: once one of cells fails, the damaged cell is immediately replaced to a prepared cell in stock, while the damaged cell is sent to maintenance and consequently becomes available again from the stock. Thus, the system is able to keep a continuous operation. This procedure is visualized in Fig. 1.4 [11]. Here, reasonably and remarkably, it can be deduced that each cell in the modular converter shall exhibit different aging (degradation) by nature and it would become non-negligible with the year of operation. Further, control strategies of the modular converter depending on its applications contribute to accelerating this unbalanced aging situation. As examples, for the ST application, the phase-shedding concept was proposed to improve the energy efficiency in light load, in which each cell is individually activated or deactivated depending on a required total power [11]. For the large-scale PV application, in fact, the unbalanced power among the cells in the modular converter is inherently unavoidable due to the non-uniform environmental condition, especially non-uniform irradiation by partial shading. In addition, each cell individually performs its own

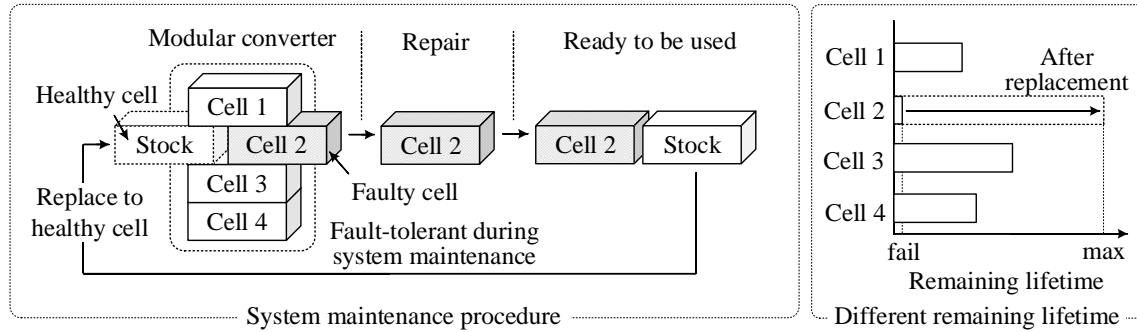


Figure 1.4: Operation and maintenance strategy for the modular converters: replace the faulty cell to the healthy cell in stock, repair the faulty cell and send to stock to be re-used and different remaining lifetime of each cell by the maintenance (left), and different remaining lifetime of each cell during the year of operation (right).

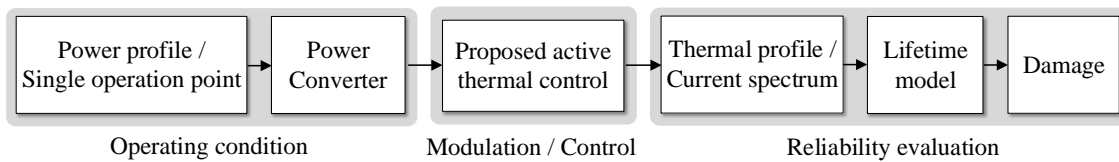


Figure 1.5: Framework to evaluate the reliability-oriented strategy, where power and thermal profile are considered for power semiconductor devices, whereas the current spectrum is analyzed in single operating point for capacitor.

MPPT algorithm to maximize the generated energy from respective PV panels [30, 31]. Hence, the processed power by each cell must be unbalanced by the control strategies.

To conclude, it is reasonable to define that the modular converter is *a system with different aged cells* and based on this, it is derived that the reliability of the whole system can be improved if the oldest cell's remaining lifetime is prolonged [11].

As a first part of this thesis, the active thermal control strategies for power semiconductor devices are proposed, which perform the power routing in the modular converters. The effect of the proposed methods on the reliability improvement is validated through estimating the accumulated damage. In a second part, the reliability of capacitors is addressed and the relation between the capacitor current (stressor) and the thermal stresses is experimentally derived. For this, the laboratory setup for generating the high frequency current as the stressor is designed and its control algorithm is proposed.

1.2 Research Proposal

The research proposal focuses on 1) investigating active thermal control based on modulations and 2) identifying their influence on the reliability through estimating the damage with an arbitrary mission profile. The framework for this objective is shown in Fig. 1.5, which

consists of following three steps: apply an operating condition to the power converter → implement the proposed methods → verify the obtained thermal profile → derive the accumulated damage. This thesis mainly handles the reliability of two components: power semiconductor devices and capacitors. In the first part, the thermally compensated modulation strategies for power semiconductors are proposed. Second, the correlation between the reliability of capacitor and its current is derived through the proposed power converter.

Target I: Thermally-compensated modulation strategies for power semiconductors

The main goal of the proposed active thermal control is to reduce the thermal stresses, mean junction temperature and junction temperature swing, caused by a mission profile. Especially, for the considered applications of the ST and the renewable energy systems, the junction temperature swing is the most critical failure reason due to a fluctuated profile. Two different modulation methods: multi-frequency and variable-clamping angle discontinuous, are proposed for the series modular converter with isolated DC-link, which consists of the Cascaded H-Bridge (CHB) converter and the DC/DC converters. Here, the modular converter is referred as a system with different aged cells and it is reasonable because of a maintenance and replacement of failed cells during years of operation.

The proposed methods are based on an uneven power loading among the paralleled paths on purpose, which is so-called as the power routing, in accordance with the remaining useful lifetime. Through the power routing, the loading on the weakest DC/DC converter is reduced, which leads to a significantly improved remaining useful lifetime, whereas other DC/DC converters processing additional power are further damaged. Therefore, the power routing concept shall achieve an improved average lifetime of the whole system or an efficient maintenance schedule. The multi-frequency modulation exploits the third harmonics to extend the DC-link voltage utilization and consequently, to improve the power imbalance capability. However, the multi-frequency modulation cannot properly handle the damage of DC/DC converters and CHB cells, simultaneously. In order to address this, the discontinuous modulation is proposed, where the clamping angle is manipulated to achieve the power routing and its power imbalance capability is further improved compared with the multi-frequency method. Remarkably, since the discontinuous method reduces switching losses of the CHB converter, its thermal stresses can be as well relieved. This feature supports a possibility of which the lifetime for both the DC/DC converters and the CHB converter can be managed. Furthermore, apart from the power routing, the discontinuous modulation is applied to the system with only CHB converter and the parallel modular converters, proposing the variable-clamping angle methods to compensate the thermal cycling.

One of the remarkable advantages of the CHB converter is the higher equivalent switching frequency when the phase-shifted carriers are applied under the balanced condition. However, as the above methods restrict the balanced modulation index among the cells, leading to increased carrier harmonics. Therefore, its influence on the power quality needs to be discussed. The conventional variable-carrier angle phase-shifted modulations to improve the

power quality under the unbalanced condition are studied and based on this, the method taking into account the discontinuous behavior is finally proposed, which aims at reducing the carrier harmonics.

Target II: Influence of current frequency on capacitor's lifetime

One of the major function of the DC-link capacitor is to filter high-order harmonics components, which are generated by the switching behavior of connected power converters. The electrolytic capacitor is most widely used in various applications as providing a higher capacitance and power density at a relatively low cost. However, the electrolytic capacitor suffers from the degradation due to the electrolyte evaporation caused by an internal additional heating. Since the additional heating is generated by capacitor current and equivalent series resistance, it has been of interest to reduce the capacitor current. However, a clear correlation between the capacitor current and the reliability is missing.

In order to identify the major current harmonics in DC-link capacitor, the capacitor current in the parallel modular converters are theoretically analyzed as a case study. Further, each harmonics of the current are decomposed for analyzing its individual influence on the hot-spot temperature. This result shall contribute not only to figure out which harmonics component has the highest impact on the temperature variation but also to provide a guide-line for developing solutions to minimize the temperature increase.

A power converter and its control strategy are proposed, which aims at generating a single sinusoidal current at a designated frequency. A challenge in designing the converter is to produce as pure sinusoidal current as possible, i.e. to achieve lower harmonic distortion, which is necessary to derive a clear relation between the current's frequency and the temperature variation. In addition, a DC bias voltage needs to be applied to the capacitor under test, leading to another challenge in the control strategy, since two control parameters, AC current and DC voltage, need to be simultaneously regulated.

Finally, it would be worth to mention that since the thermal impedance of capacitors is significantly higher compared with the power semiconductor devices, the core temperature of capacitors is not sensitively varied by a fluctuating mission profile. Consequently, it is reasonable to consider the average energy losses instead of the instantaneous power losses for the reliability evaluation of capacitors.

1.3 Structure of the Thesis

The structure of the thesis is shown in Fig. 1.6, along with the related publications during this study. Section 2 introduces the modular converters in the ST and renewable energy systems applications, discusses the reliability issue and motivates the necessary of active thermal control methods. In section 3, the reliability of power semiconductors is discussed, including the thermo-dependent failure mechanisms for the typical wire-bonded structure. Further, the lifetime model based on the PoF approach and the accumulated damage estimation are

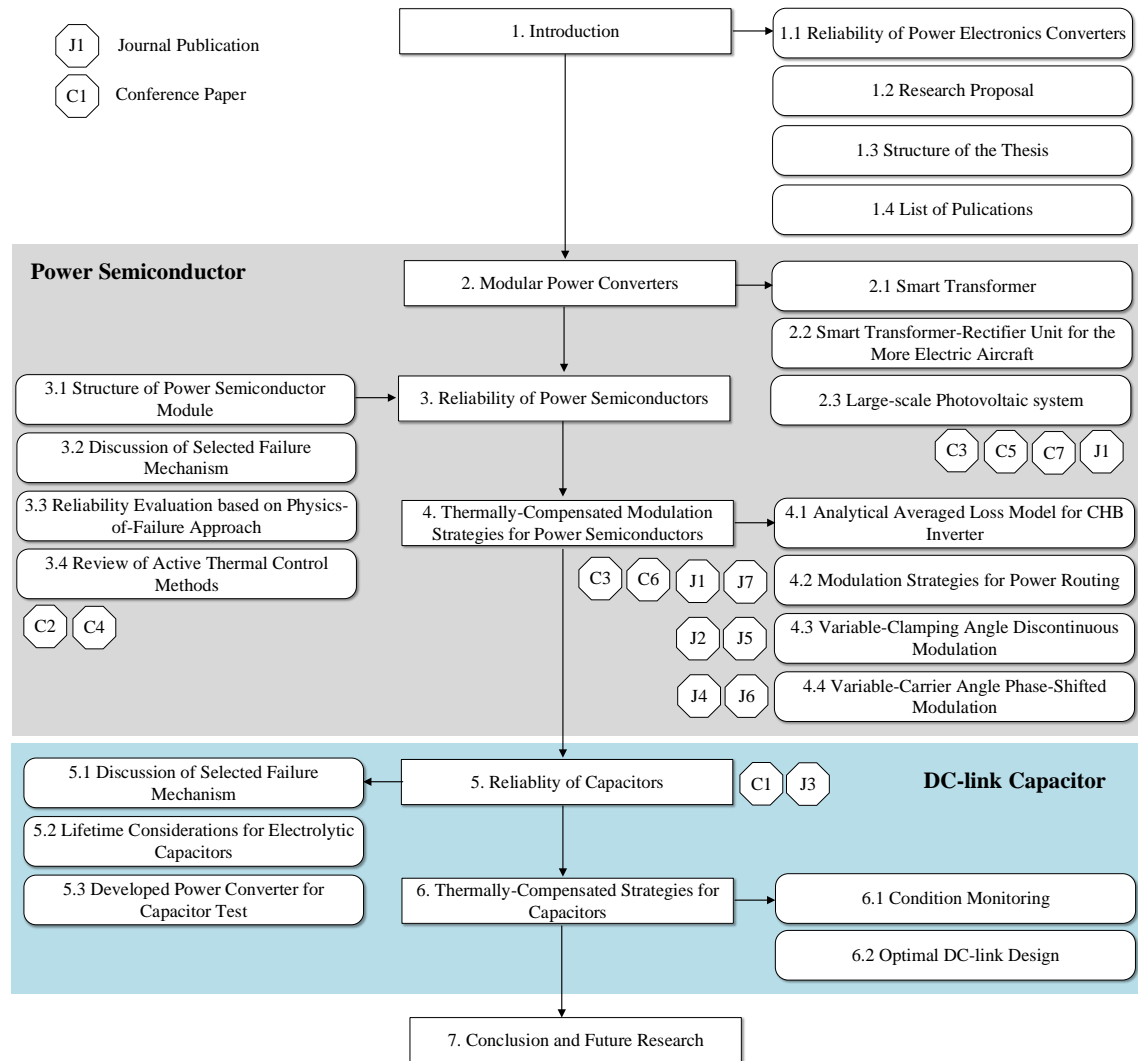


Figure 1.6: Structure of the thesis and related publications.

introduced, which will be used for estimating the effect of the active thermal control methods proposed in section 4. Followed by, the existing active thermal control methods are reviewed, discussing their constraints.

The active thermal control methods for power semiconductor devices are proposed in section 4, which are the multi-frequency modulation and variable-clamping angle discontinuous modulation. The influence of each method on the loss distribution is analyzed with the analytical averaged loss model, and their capability in terms of the number of cells thermally compensated, is analytically evaluated. Further, the effect of each method on the lifetime is demonstrated by means of the lifetime model introduced in section 3 and on the junction temperature is experimentally verified. Apart from the reliability, the variable-carrier angle method for the CHB inverter is proposed in order to ensure the power quality when the proposed active thermal control methods are applied.

On the other hand, section 5 and 6 study on the reliability of DC-link capacitors. In section 5, three types of capacitors, which are typically used in the DC-link application, are introduced and their electrical characteristics and major failure mechanisms are discussed. Especially,

with the lifetime model of electrolytic capacitor, the root-cause of the degradation is highlighted to motivate the need to investigate the clear relation between the capacitor current and the reliability. The capacitor test setup, which aims at emulating the AC capacitor current and the DC bias voltage, is proposed and consequently, the correlation between the capacitor current' frequency and the hot-spot temperature variation is derived. In section 6, the existing methods to reduce the capacitor current are reviewed.

Section 7 concludes this thesis, followed by future research topic in order to reinforce this work.

1.4 List of Publications

A list of the papers, which have been published or are in press during this study, is given as follows:

Journal papers

- J1 Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Power Routing for Cascaded H-Bridge Converters," in *IEEE Transaction on Power Electronics*, vol. 32, no. 12, pp. 9435-9446, Dec. 2017.
- J2 Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Thermally Compensated Discontinuous Modulation Strategy for Cascaded H-Bridge Converters," in *IEEE Transaction on Power Electronics*, vol. 33, no. 3, pp. 2704-2713, March 2018.
- J3 Y. Ko, H. Jedtberg, G. Buticchi, and M. Liserre, "Analysis of DC-Link Current Influence on Temperature Variation of Capacitor in a Wind Turbine Application," in *IEEE Transaction on Power Electronics*, vol. 33, no. 4, pp. 3441-3451, April 2018.
- J4 Vito G. Monopoli, Y. Ko, G. Buticchi, and M. Liserre, "Performance Comparison of Variable-Angle Phase-Shifting Carrier PWM Techniques," in *IEEE Transaction on Industrial Electronics*, vol. 65, no. 7, pp. 5272-5281, July 2018.
- J5 Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Discontinuous Modulation Based Active Thermal Control of Power Electronic Modules in Wind Farms," in *IEEE Transaction on Power Electronics*, vol. 34, no. 1, pp. 301-310, Jan. 2019.
- J6 Vito G. Monopoli, A. Marquez, Jose I. Leon, Y. Ko, G. Buticchi, and M. Liserre, "Improved Harmonic Performance of Cascaded H-Bridge Converters with Thermal Control," in *IEEE Transaction on Industrial Electronics*, vol. 66, no. 7, pp. 4982-4991, July 2019.
- J7 Y. Ko, V. Raveendran, M. Andresen, and M. Liserre, "Thermally-Compensated Discontinuous Modulation for MVAC/LVDC Building Blocks of Modular Smart Transformers," in *IEEE Transaction on Power Electronics*, Early Access, 2019.

Conference papers

- C1 Y. Ko, H. Jedtberg, G. Buticchi, and M. Liserre, "Topology and Control Strategy for Accelerated Lifetime Test Setup of DC-Link Capacitor of Wind Turbine Converter," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2016.
- C2 Y. Ko, B. Benkendorff, G. Buticchi, and M. Liserre, "Reactive Power Control to Improve Reliability of High Wind Power Converters Connected in Parallel," 2016 The European Wind Energy Association (EWEA), Hamburg, Germany, 2016.
- C3 Y. Ko, M. Andresen, G. Buticchi, L. Concari, and M. Liserre, "Multi-frequency power routing for cascaded H-Bridge Inverters in Smart Transformer Application," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016.
- C4 Y. Ko, M. Andresen, G. Buticchi, J.S. Lee, and M. Liserre, "Modulation Strategy for Highly Reliable Cascade H-Bridge Inverter Based on Discontinuous PWM," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 2017.
- C5 Y. Ko, A. Chub, L. Costa, M. Andresen, and M. Liserre, "Smart Transformer Universal Operation," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018.
- C6 Y. Ko, V. Raveendran, M. Andresen, and M. Liserre, "Discontinuous Modulation based Power Routing for Modular Smart Transformers," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 2018.
- C7 G. Buticchi, Y. Ko, M. Liserre, and C. Gerada, "A Smart Transformer-Rectifier Unit for the More Electric Aircraft," 2018 International Symposium on Industrial Electronics (ISIE), Cairns, Australia, 2018.

2 Modular Power Converters

The modular power converters are getting a lot of attention in various application fields such as Smart Transformer (ST), renewable energy system and traction [32, 33, 34] as an alternative to the conventional non-modular converters. The non-modular converters require power semiconductor devices, which have a full-voltage blocking capability. This means that the voltage and current slew rate would be increased, namely high dv/dt and di/dt , as the rated power of converters is increasing. Further, using standard commercialized power devices could be restricted in higher voltage applications. On the contrast, the modular converters inherently exhibit a constitution of multiple basic cells, of which required blocking voltage (or current) is divided by the number of cells. This feature enables to overcome the drawbacks of the non-modular converters in addition to the advantages presented in section 1.

In the following, the representative applications of the modular converters: the Smart Transformer (ST) and the large-scale Photovoltaic (PV) are first introduced, which are shown in Fig. 2.1.

2.1 Smart Transformer

The Solid-State Transformer (SST) that was first introduced in 1968 by McMurry, is a concept based on power semiconductor technologies [10]. Although the SST was supposed to replace the standard line-frequency transformers between the medium-voltage grid and the low-voltage grid, it has not been applied in real fields due to the constraints in terms of cost, volume, efficiency and reliability. Since then, today's advanced technology of the power semiconductor serves possibilities to achieve a medium-frequency operation, which enables to reduce size and weight of the SST, and a higher efficiency [35]. Furthermore, the SST has high potential to enable a DC connectivity and to provide various services such as bidirectional power flow and reactive power support for both medium-voltage and low-voltage grids, requiring the need for control and communication functions. Consequently, it leads to a concept of the ST [35].

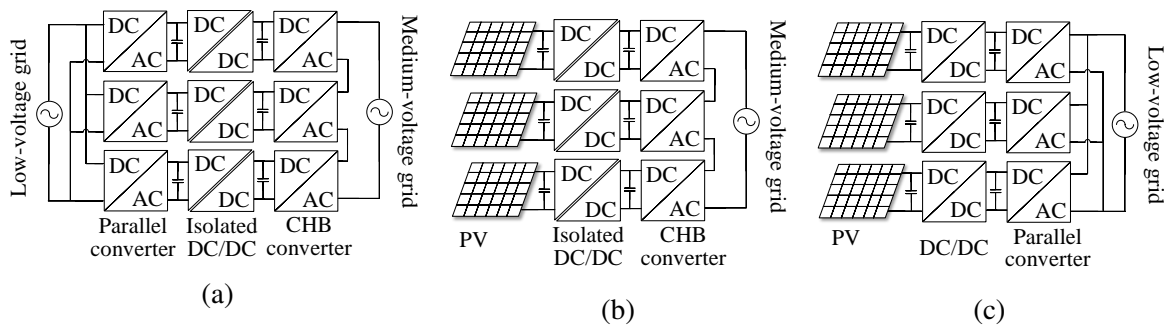
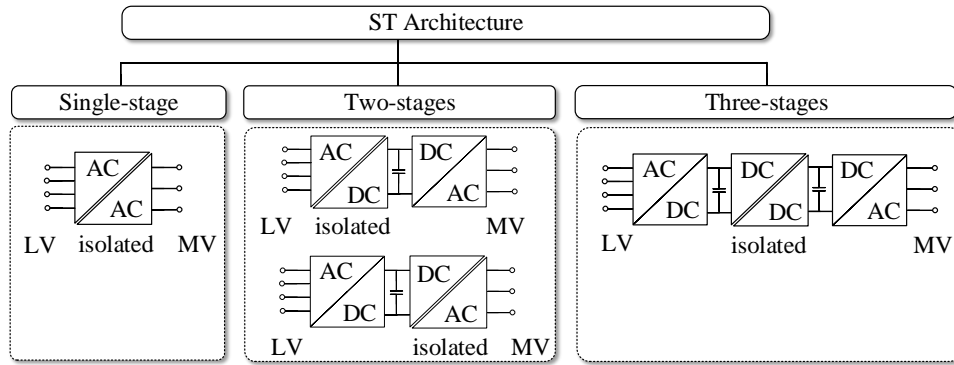
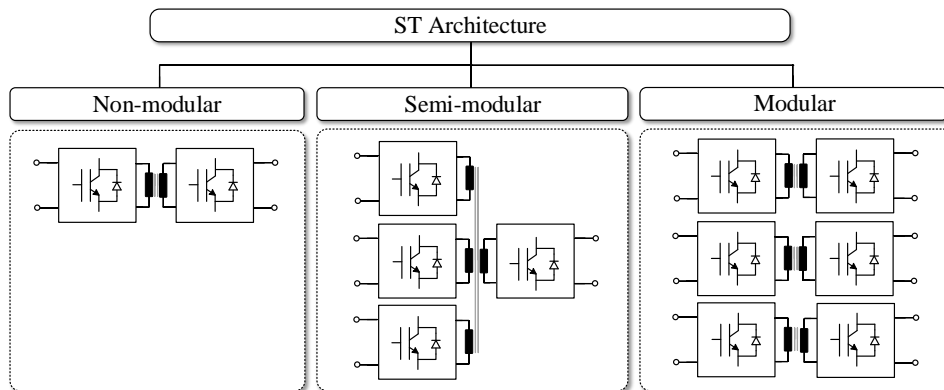


Figure 2.1: Applications of the modular converters: (a) ST with parallel and series converters and large-scale PV with (b) series converter and (c) parallel converter.



(a)



(b)

Figure 2.2: Classification of the ST architecture in accordance with (a) the number of power conversion stages and (b) modularity.

As one of the critical issues, there is a discussion on the ST architecture [36], which is typically categorized depending on 1) the number of power conversion stage: single-, two- and three-stage as shown in Fig. 2.2 (a) and 2) the modularity: non-modular, semi-modular and modular as shown in Fig. 2.2 (b). An example respective to each configuration is also shown.

The single-stage concept is based on the direct power conversion between medium-voltage and low-voltage grids, providing the galvanic isolation. This is usually achieved by matrix converter topologies [37], of which advantage is a higher power density at a lower cost as eliminating a bulky DC-link capacitors. However, due to the lack of DC-link, the medium- and low-voltage grids are strongly coupled like the passive transformers as well as there is no available DC grid connectivity, which is essentially required in the current grid paradigm. In the two-stages architecture, the galvanic isolation can be provided either in medium- or low-voltage side and depending on this, one of DC grid connectivity is available (i.e. with the medium-voltage side galvanic isolation the low-voltage DC grid is provided, whereas the medium-voltage DC grid is available) [36]. In addition, the full grid services can be possibly provided. On the other hand, current source converters realize the two-stages architecture without the DC-link capacitors [38]. In this case, the energy storage is made

magnetically (inductors) instead of electrically (capacitors). Even though the current source converters are capable to provide the grid services, there are still doubts about their performance such as losses, common mode voltages and the security in case of emergency shut-down. The three-stages architecture is based on the isolated DC/DC converter between the medium-voltage DC-link and the low-voltage DC-link [35], which implies a possibility of both medium-voltage and low-voltage DC grid connectivity. Moreover, there is a high flexibility for choosing the medium-voltage and low-voltage side converters topology and for a control strategy to serve all required grid services. However, a higher number of power semiconductor devices and capacitors are needed, which could be translated into the reliability issue.

The another classification is the modularity. The non-modular architecture requires a lower number of power semiconductor devices, but a higher voltage blocking capability for the medium-voltage side converter. Furthermore, a larger output filter is required due to a high dv/dt , the scalability in power and voltage is unavailable and the application of fault tolerance schemes is inherently limited [39, 40]. The semi-modular concept is only applicable in the isolation stage by means of a medium-frequency transformer with multiple windings. This multi-winding transformer enables to reduce the number of transformers and to use devices rated for lower voltage, since several power converter cells can be connected in parallel or series to the same transformer [41]. The full modular concept is based on the use of several building blocks, which are connected in parallel and/or in series. Modular power converters commonly enable to adopt fault tolerant schemes and scalability in power and voltage. However, a higher number of components, such as transformer cores, power semiconductor devices and capacitors, is needed [35, 42].

The medium-voltage side converter is challenged because it should be able to handle the medium-voltage grid that is ranged from 2.3 kV to 35 kV depending on different countries [43]. One intuitive solution is to use the well-established topologies for the low-voltage applications like the two-level converter. This solution is only achievable with high voltage rated devices [44, 45, 46] or by connecting multiple low-voltage rated devices in series [47, 48, 49]. However, the medium-voltage rated devices are not only limited on the market but also higher blocking voltages in combination with higher switching frequencies present drawbacks such as higher switching losses, bigger filter size and higher Electro-Magnetic Interface (EMI) emission. Furthermore, it has been mentioned that the series connected devices could arise the problem of the switching synchronization [48, 49]. In order to avoid such issues, the modular multi-level converters, particularly the Cascaded H-Bridge (CHB) converter are widely considered for the medium-voltage stage as enabling to facilitate the power devices rated for the lower voltage. Moreover, by the isolated DC/DC stage that operates at medium-frequency, the reduced size and weight are achievable with a higher energy efficiency by means of the soft-switching techniques. Finally, the whole system is structured by the semi-modular three-stages architecture, where the medium-voltage side is addressed by the CHB converter (series modular converter), the isolated DC/DC converter facilitates the low-voltage DC connectivity and the low-voltage side is achieved by parallel modular converter for higher current capability.

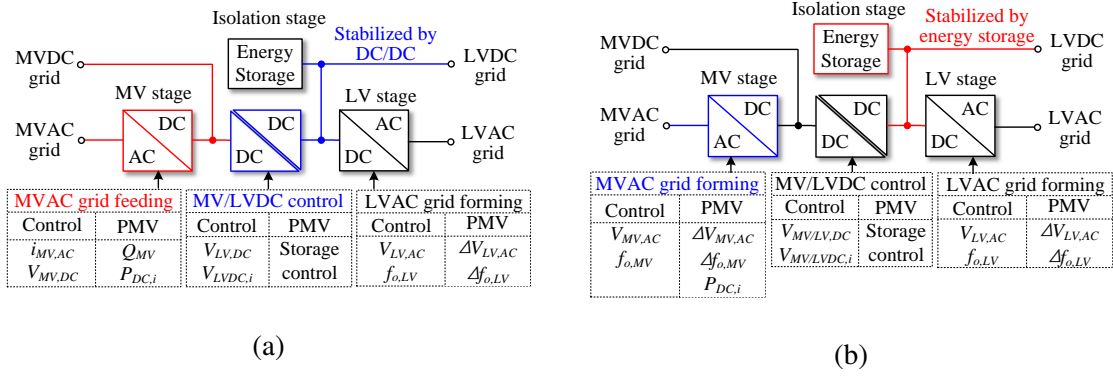


Figure 2.3: Potential operation scenarios with control and PMVs: (a) medium-voltage grid-feeding and low-voltage grid-forming and (b) both medium-voltage and low-voltage grid-forming.

In addition to the architecture, the operation scenario for the ST needs to be discussed, depending on the condition of the medium-voltage grid. In the context of the micro-grid concept, the grid-feeding and -forming mode have gained attention. The grid-feeding mode makes the power converter to operate as grid-tied converters to control the grid current, whereas the grid-forming mode targets to generate a stable grid voltage with voltage amplitude and frequency commands [50, 51, 52]. These operation modes are expected to be applied for the ST. The grid-feeding mode is typically applied only to the medium-voltage side under a stiff medium-voltage grid condition, however, in accordance with the medium-voltage grid condition, the grid-forming mode might be required. Meanwhile, the low-voltage side converters always operate in the grid-forming mode. A resulting challenge is occurred when both converters are operated in the grid-forming mode, as requiring control strategies to balance the power flow in the entire system and to supply all loads with a limited active power. Here, the limited active power can be addressed by either the DC grid or the energy storage systems. One of the possible opportunities is to control the amplitude and frequency of the AC grids, where the amplitude is exploited to vary the load consumption of impedance loads and the frequency variation is acting on the droop control of the distributed generators, potentially either increasing or decreasing the generation [53, 54, 55].

Considering the three-stages architecture, two possible operation scenarios are shown in Fig. 2.3: 1) medium-voltage grid-feeding and low-voltage grid-forming and 2) medium-voltage grid-forming and low-voltage grid-forming.

The first scenario is shown in Fig. 2.3 (a), where the medium-voltage side converter is connected to a stiff medium-voltage grid in the grid-feeding mode and exchanges the active and reactive power, P_{MV} and Q_{MV} , performing the control of the grid current, $i_{MV,AC}$, and the medium-voltage DC-link, $V_{MV,DC}$. The isolated DC/DC converter performs the control of the low-voltage DC-link, $V_{LV,DC}$, whereas the low-voltage side converter generates the low-voltage grid in the grid-forming mode with controlling its amplitude, $V_{LV,AC}$, and frequency, $f_{o,LV}$.

The second scenario is shown in Fig. 2.3 (b), where there is no stiff medium-voltage grid.

Table 2.1: Technical specification of the developed ST demonstrator

System		CHB		QAB	
Power	90 kW (30 kW×3)	Switching frequency	10 kHz	Switching frequency	20 kHz
AC voltage	2600 V _{ll} 1500 V _{ln}	Si-IGBT	1200 V / 40 A	SiC-Mosfet	LV side: 1200 V / 60 A MV side: 1200 V / 40 A
MVDC	2400 V (800 V×3)	Capacitor bank	750 uF (each cell)	Leakage inductance	75 uH
LVDC	800 V	Filter inductance	1 mH	Transformer	1:1:1:1

Hence, the ST needs to form both medium- and low-voltage grids, namely, both side converters are in the grid-forming mode. To make this scenario to be feasible, the active power needs to be fed by a DC grid and/or a storage system, ensuring the balanced generation and consumption. However, this may not be possible for all realistic operation modes and thus, it leads that the power production and consumption in the grids are targeted to be properly manipulated. To do so, the different commands defined as Power Manipulating Variables (PMVs) in the three-stages, are described along with potential solutions to influence the power consumption. Therefore, the power balancing capability and the maximized availability of the grid with extended operation time can be achieved. Remarkably, the active power in the grid can be manipulated by controlling the amplitude of the grid voltage, $\Delta V_{MV,AC}$. For example, the active power consumption is reduced with a reduction of the grid voltage amplitude in case of a constant impedance load. Here, it should be noted that the estimated potential to reduce or increase the amplitude without violating the grid codes is expected to be $\Delta V_{MV,AC} = \pm 10\%$, following the IEC 38 standard [53, 54].

The ST conceptualization is another challenging task because of numerous choice options such as the number of power stages, power converter topology and DC grid availability. Moreover, the ST is intended to perform an advance control in order to serve the required ancillary services to the grid. As mentioned before, the three-stage architecture, which is composed of the CHB converter for the medium-voltage stage and a multiple active bridge for the isolation stage, has been intensively considered, as not only enabling to offer the degree of freedom for control system but also providing the galvanic isolation with a high efficiency [56, 57]. The architecture for demonstrator is shown in Fig. 2.4, which is based on the 7-level CHB and the Quadruple Active Bridge (QAB) converter. One unit is used per phase, resulting then in three units for assembling the entire three-phase architecture. The specification and parameters used in each converter are presented in Table 2.1, which are decided with [41].

For the CHB converter, the switching frequency of 10 kHz is chosen, which is a recommended value for the used Si IGBT IKW40N120T2. Remarkably, employing the phase-

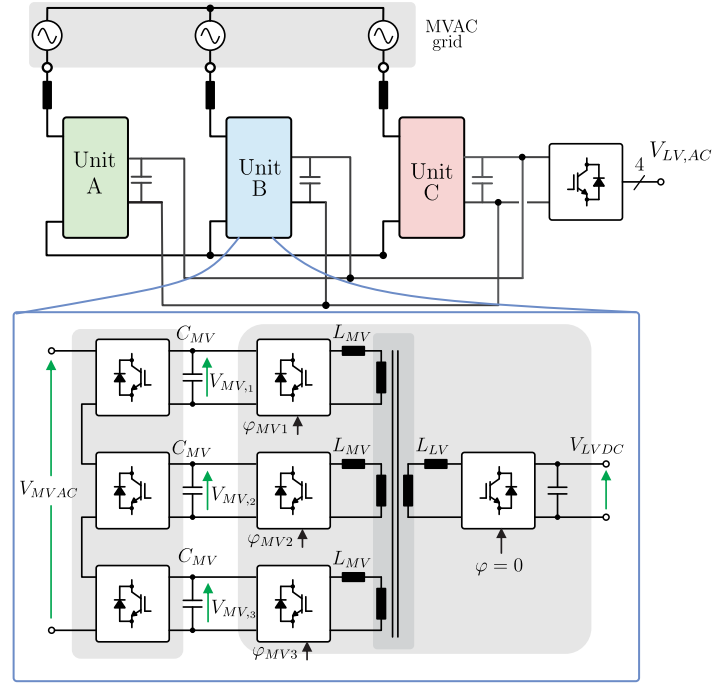


Figure 2.4: ST architecture and circuit of the power unit used to implement the entire system.

shifted carriers leads to a higher effective frequency of 60 kHz on the filter, which allows the filter size reduction. The QAB converter, on the other hand, has a switching frequency of 20 kHz, which provides a good trade-off between magnetic elements volume and isolation issues due to the partial discharge [58]. The SiC MOSFET C2M0040120D for the medium-voltage side and C2M0025120D for the low-voltage side, are employed.

In terms of the control strategy, considering the scenarios in Fig. 2.3, the isolated DC/DC converter aims at controlling either the low-voltage or medium-voltage DC-link, depending on the operation mode in Fig. 2.3. Therefore, a resulting challenge is that the control objective of the DC/DC converter needs to be changed from the low-voltage to the medium-voltage DC-link or vice versa (compare the control objective of the DC/DC stage in Fig. 2.3 (a) and (b)). Considering the operation scenario in Fig. 2.3 (b), the control strategy for each stage is proposed as shown in Fig. 2.5. The control block diagram for the medium-voltage side converter in the grid-forming mode is shown in Fig. 2.5 (a), which has the cascaded structure with the Proportional-Integral (PI) loop to generate the grid voltage and the Proportional-Resonance (PR) loop for controlling the grid current. The final reference from the current controller is fed to each cell of the CHB converter. Fig. 2.5 (b) presents the control block for the low-voltage side converter, which is always in the grid-forming mode, and the control scheme is similar with that of the CHB in the grid-forming mode. Finally, a control algorithm for the isolated DC/DC converter shown in Fig. 2.5 (c) performs to balance the voltages of all DC-links. Here, the QAB in Fig. 2.4 is considered as the isolated DC/DC converter. The remarkable advantage of this strategy for the DC/DC stage is that its control block diagram is unnecessary to change in according with switching the operation mode.

The proposed control algorithm in the above is simulated with a varied power flow as shown in Fig. 2.6. Here, the resistive load in both medium-voltage and low-voltage grids is con-

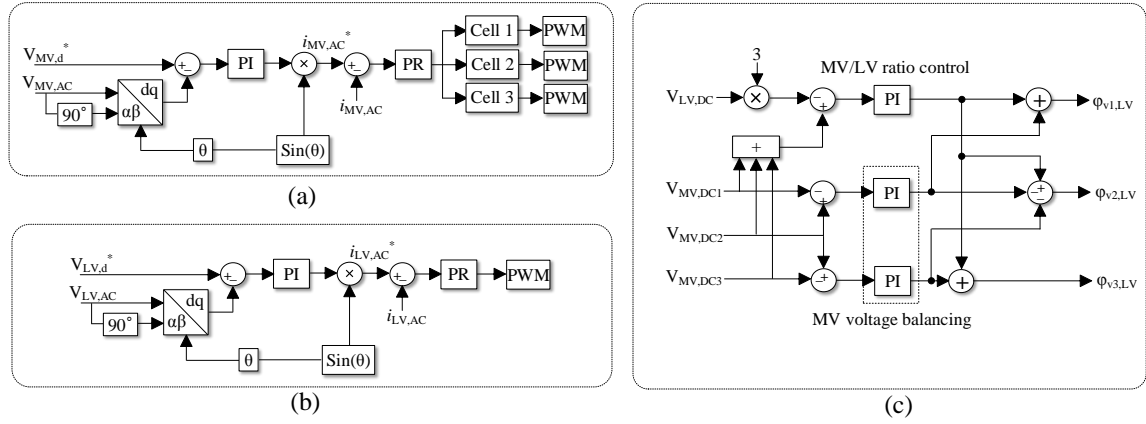


Figure 2.5: Control block diagram for the scenario in Fig. 2.3 (b): (a) CHB converter in the medium-voltage grid-forming mode, (b) low-voltage side converter in the grid-forming mode and (c) QAB to control the medium- and low-voltage DC-link.

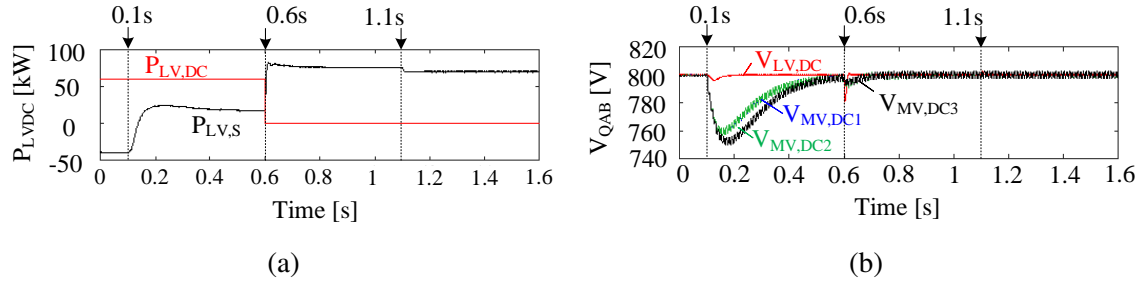


Figure 2.6: Simulation of the proposed control algorithm of the QAB with power step variations: (a) active power of low-voltage DC-link, $P_{LV,DC}$ and storage system, $P_{LV,S}$ and (b) low-voltage DC-link, $V_{LV,DC}$, and medium-voltage DC-link, $V_{MV,DC}$.

nected and the leakage inductance of the the QAB, which are unbalanced by 20%, is considered in order to show a robustness.

The considered scenario is like this: at $t = 0.1 s$, a load step in the medium-voltage grid occurs ($R_{MV} = 480 \Omega \rightarrow R_{MV} = 87 \Omega$) and at $t = 0.6 s$ the power injection from the low-voltage DC grid is stopped. The last occurrence at $t = 1.1 s$ is a load step in the low-voltage grid from $R_{LV} = 50 \Omega \rightarrow R_{LV} = 11.5 \Omega$.

As shown in Fig. 2.6 (a), the low-voltage DC grid is injecting the active power $P_{LV,DC} = 60$ kW from 0 to 0.6 s and afterward there is no active power injection from the grid. Meanwhile, the storage system is balancing the active power by injecting or absorbing active power, $P_{LV,S}$, over the whole period. Under this power flow variation, the voltage balancing controller rejects all disturbances caused by the power variations as shown in Fig. 2.6 (b). In addition, it can be seen that the voltage variations of the low-voltage DC-link and the medium-voltage DC-link are coupled, as it is targeted by the controller.

The related medium-voltage and low-voltage grids and their currents are shown in Fig. 2.7 (a), along with the same power fluctuation in the above. In order to reduce the power consumption and therefore, increase the time for this potential operation mode with the control of the PMVs, the grid amplitude is controlled. This is shown in Fig. 2.7 (b). For minimizing

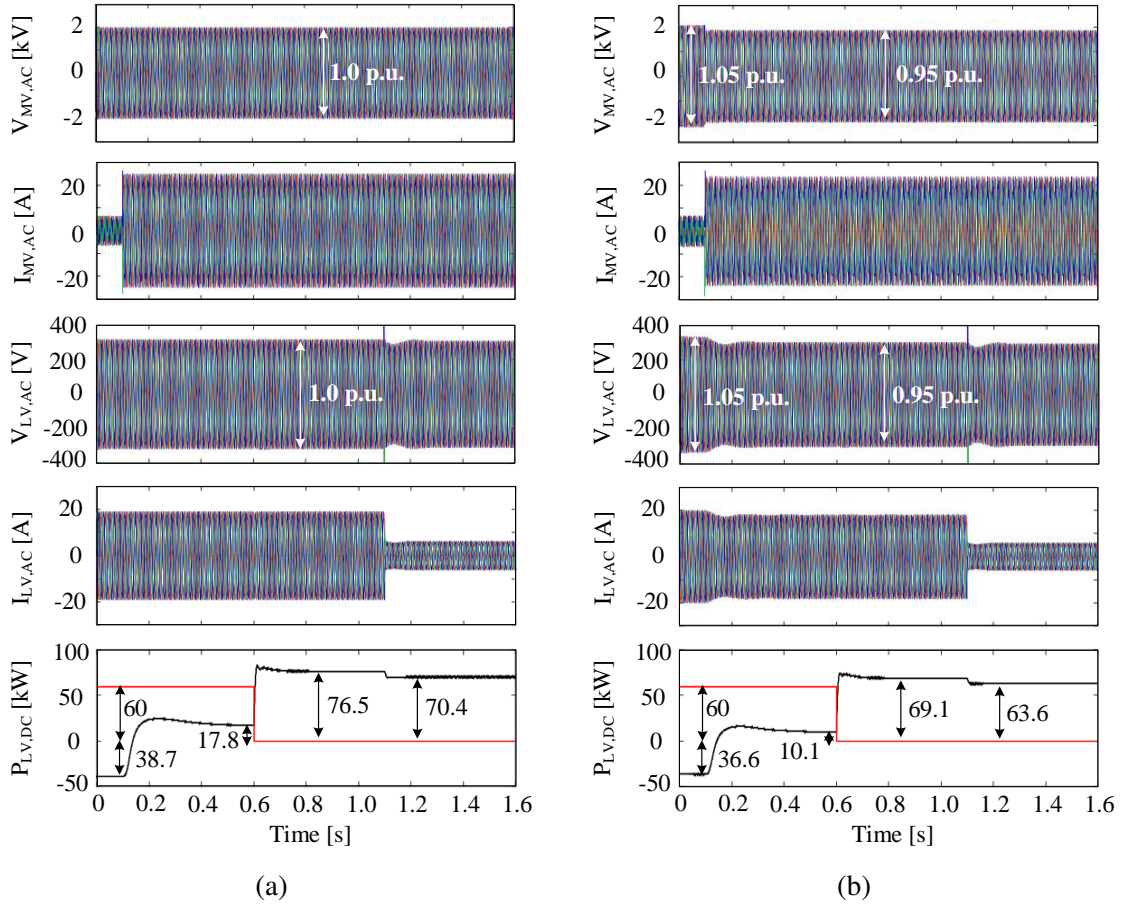


Figure 2.7: Simulation of the power consumption of the low-voltage and medium-voltage grid by means of grid voltage amplitude control: (a) for controlling the medium-voltage and low-voltage grids to 100 % (b) by adapting the PMV in the medium-voltage and low-voltage grids to 105 % (for $0 < t < 0.1$ s) and 95 % (for $0.1 < t < 1.6$ s).

the power transfer of the energy storage system, the amplitude of the grid voltage is increased to 105 % of the nominal value in the low-voltage grid and the medium-voltage grid for the time when the energy system is absorbing power (0 to 0.1 s). As it can be seen, the voltage increase affects a reduction of the power in the storage system $P_{LV,S} = -38.7$ kW \rightarrow -36.6 kW (by 5 %) before $t = 0.1$ s and even by 56 % at $t = 0.5$ s.

On the other hand, the voltage is reduced to 95 % when the power transfer of the storage system reverses from 0.1 to 1.6 s, resulting in the reduced power consumption in the grids. After $t = 0.6$ s, when the grid is only consuming power, the reduction of the grid voltage affects a reduction of the power consumption by ≈ 10 %.

As a conclusion, the control of the grid voltage amplitude can effectively increase or reduce the power consumption, which is particularly powerful for grids with generation and consumption with a comparable power rating.

The developed demonstrator is shown in Fig. 2.8 and its preliminary functionality is validated in the grid-forming mode operation. As shown in Fig. 2.9, the CHB and QAB converters are locally controlled by their own controller, which is called as a slave controller,

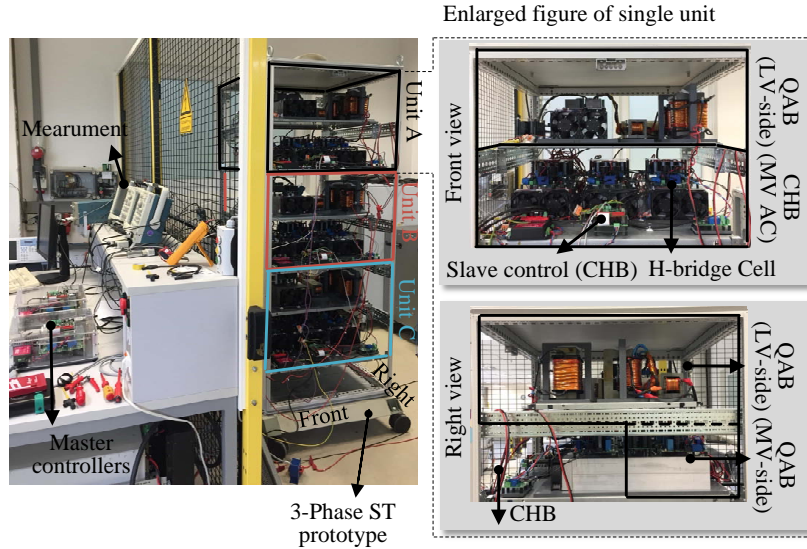


Figure 2.8: Demonstrator of three-phase smart transformer consisting of single unit per phase.

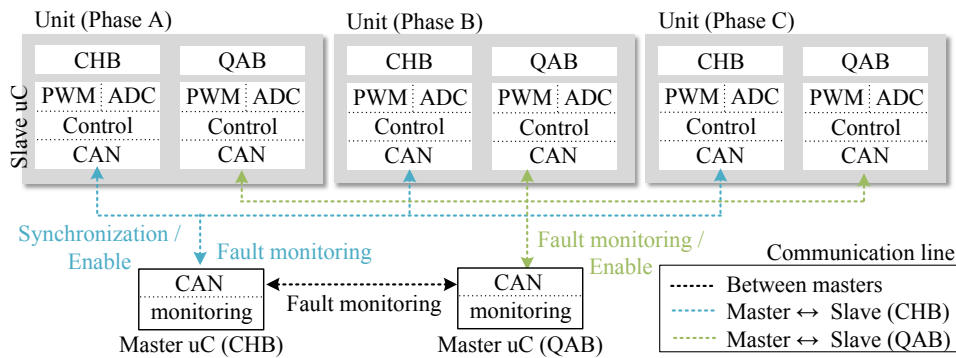


Figure 2.9: Network structure among master/local controllers via CAN protocol.

and the communication network among the slave and master controllers are illustrated as well. The slave controllers for the CHB need to be synchronized in order to generate the three-phase voltage (120° displacement) in addition to the central management for enabling and fault monitoring, whereas those for the QAB converter perform solely for the central management. The Controller Area Network (CAN) 2.0B protocol is employed for this purpose.

Fig. 2.10 shows the preliminary result of the availability for medium-voltage operation with RL-load, where a DC source supplies 500 V to the low-voltage DC and the total medium-voltage DC of 1500 V is regulated by the QAB converter. As it is shown in Fig. 2.10 (a), the CHB output voltage before the filter evidently has the 7-level voltages, the output current is $2.5 A_{peak}$ and the medium-voltage DC-link of 500 V. The QAB operation in the medium-voltage and low-voltage sides is shown in Fig. 2.10 (b), where it can be noticed that there is a phase difference between the medium-voltage and low-voltage side to process the power.

The control performance for the grid-forming mode with the proposed algorithm is verified

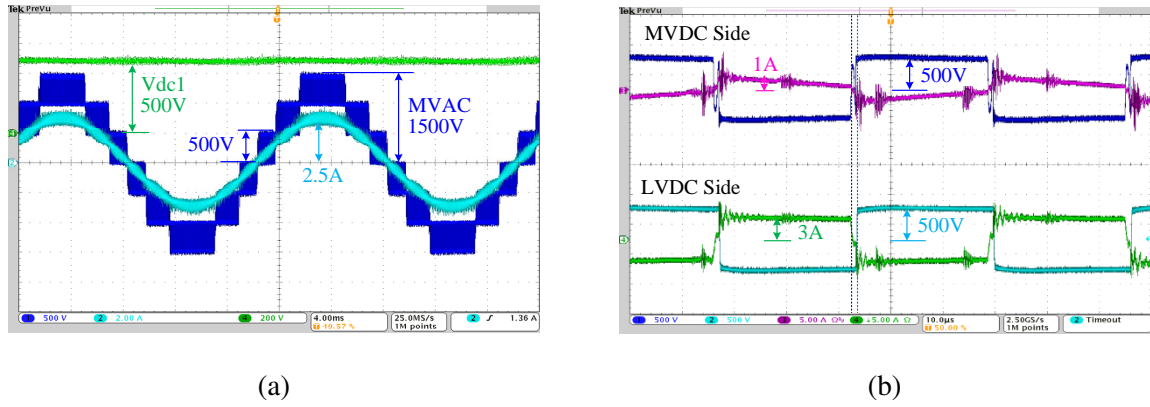


Figure 2.10: Verification of preliminary operation with DC-link of 1.5 kV and RL-load: (a) CHB DC-link voltage of one cell (green), AC output voltage (blue) and current (light blue) and (b) QAB medium-voltage (upper) and low-voltage (bottom) side voltage and current.

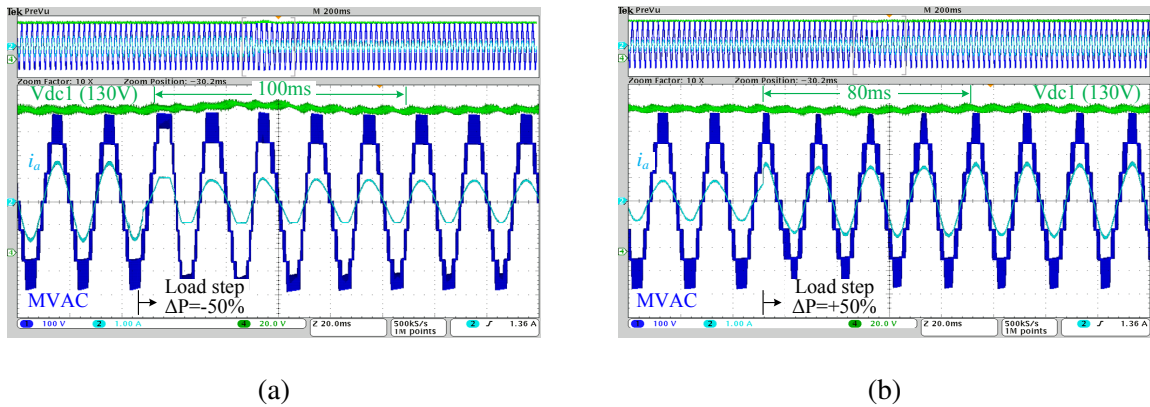


Figure 2.11: Dynamic response of the grid-forming mode control with load step change: (a) $\Delta P = -50\%$ and (b) $\Delta P = +50\%$.

by a step load change of $\pm 50\%$ as shown in Fig. 2.11, where the medium-voltage DC-link is 390 V and the medium-voltage grid is controlled to maintain 230 V. The settling time is between 80 and 100 ms (12.5-10 Hz) and the fluctuation of around 0.1 p.u. in the DC voltage is observed during the dynamics in both cases.

Finally, the three-phase operation is demonstrated by synchronizing the slave controllers via the CAN network and the output voltages, which are exactly displaced by 120° with adjacent voltages, are achieved as shown in Fig. 2.12.

2.2 Smart Transformer-Rectifier Unit for the More Electric Aircraft

In the framework of the More Electric Aircraft (MEA), an efficient and flexible power distribution system is of paramount importance. Considering the presence of both AC and DC

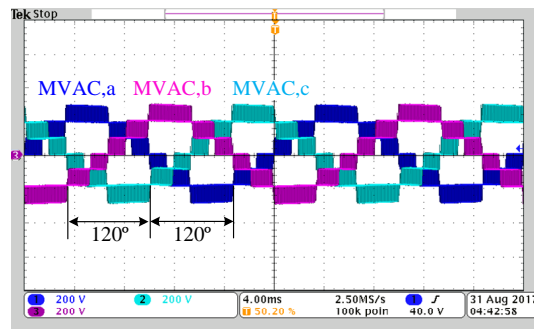


Figure 2.12: Verification of synchronization of the CHB converter's local controller in each phase for three-phase operation.

loads at multiple voltage levels, the distribution system of the most modern aircraft is intrinsically hybrid. In this scenario, the simplest approach is to use a Transformer-Rectifier Unit (TRU) based on a low-frequency transformer followed by passive rectifiers to perform the AC/DC conversion. This solution, however, is intrinsically uni-directional, introduces current harmonics in the AC side and can have a considerable size. In the following, the use of a Smart-TRU, which is based on the modular multi-level converter (CHB) and the isolated multi-port DC/DC converter (QAB), is proposed. This solution is supposed not only to solve the issues of the traditional TRU but also to increase the controllability is proposed.

As presented before, the CHB converter has advantages such as the modularity, the possibility to adopt low-voltage devices, the reduced output harmonic distortion and easy of control. One of its biggest disadvantages, on the other hand, is the necessity to provide isolated DC-links to all the H-bridge cells and the need for the isolating transformer to be designed for the full rating voltage. However, if the CHB is adopted for low-voltage applications, this constraint of the transformer isolation is not anymore relevant and the transformer can be optimized for efficiency and power density (i.e., primary and secondary windings can be overlapped to minimize the stray inductance and the AC losses). Using a multi-level converter for an avionic application with DC-link of 270 V would also allow the usage of low-voltage devices with excellent on-state characteristics, still retaining all the advantages of the modular architecture.

The QAB converter has been proposed to be used in aircraft systems in several works [59, 60], since its multi-port characteristic makes it as a suitable candidate to interface different power sources and to guarantee the power exchange among the DC buses. The control algorithm that is proposed in Fig. 2.5 for the QAB to regulate DC-link voltages, is applicable for this application.

The CHB plus QAB converter solution has several degrees of freedom, because the AC side is three-phase and the QAB can be used in 3-1 (three ports AC and one DC) or in 2-2 (two ports for AC and DC) mode. Fig. 2.13 shows how the converter can be used to realize a three port AC/DC+DC converter, with one AC port and two DC ports. The biggest advantage of this kind of approach is the possibility to connect a generator directly to two bus bars, as

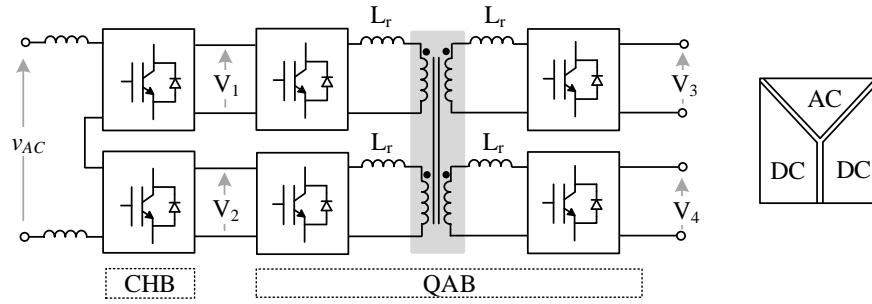


Figure 2.13: Three ports (one AC and two DC ports) modular S-TRU.

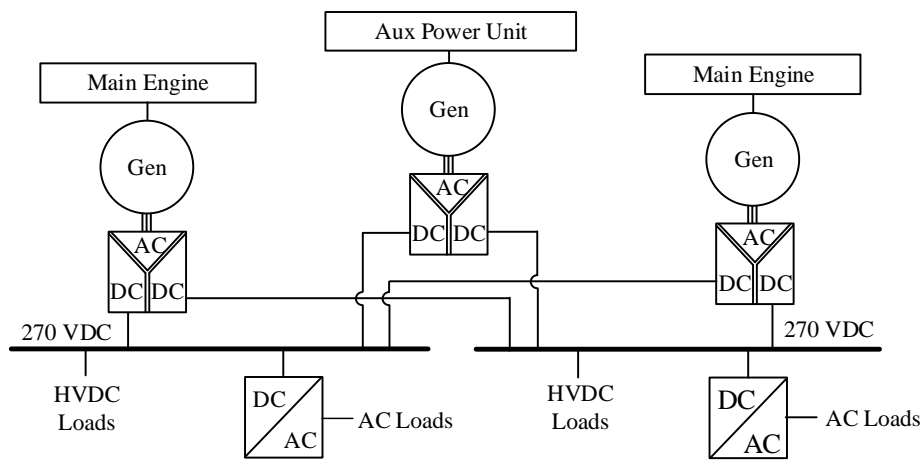


Figure 2.14: Example of an hybrid electrical power distribution systems with S-TRU.

shown in Fig. 2.14. The internal power sharing of the QAB allows for different power to be distributed to the bus bars. This solution has several degrees of redundancy:

- The three-phase AC/DC is composed of six H-bridges with an intrinsic fault tolerant capability.
- Since there are three QAB converters, the fault of one QAB does not interrupt the power flow to the DC buses.
- If a generator ceases to function, the QAB still allows for the power exchange between the bus bars, allowing for seamless transition to a post-fault condition.

This solution replaces the solid-state switches, allowing for the virtual connection of the whole electrical power distribution system (with benefits in terms of better utilization of the generators) but still guaranteeing the galvanic isolation.

In order to test experimentally the operation of the Smart-TRU (S-TRU), especially under a fault condition in a CHB cell, a single-phase prototype is used. The prototype features three CHB cells and one QAB converter, comprising of the medium-frequency transformer. Fig. 2.15 shows the schematic of the experimental setup. A DC power supply is connected to the DC port and a Resistive-Inductive (RL) load is connected to the AC port. If a fault

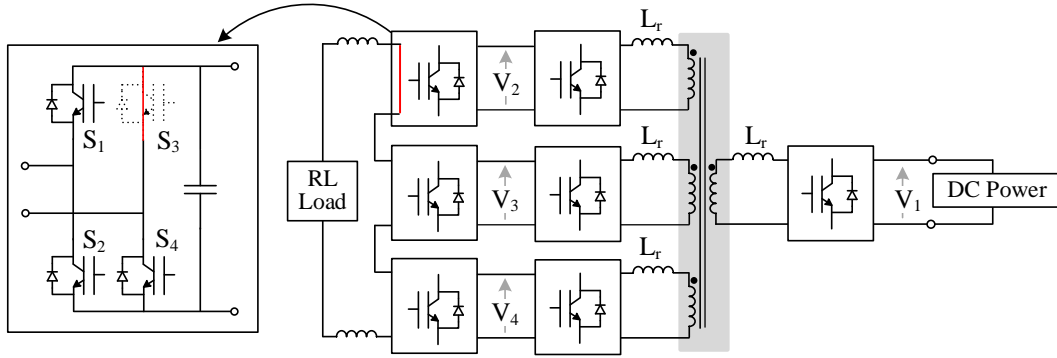


Figure 2.15: Schematic of the setup for the experiment in case the faulty cell is bypassed by forcing an output zero vector.

occurs, e.g., short-circuit of the switch S_3 , the H-bridge outputs zero voltage by disabling switches S_2 and S_4 and switching on S_1 . During this transition, the QAB port can still be operational, controlling the voltage. After the fault, it can be switched off and the QAB can be reconfigured into a Triple Active Bridge (TAB). A similar procedure can be adopted in the case of an open-circuit fault.

The condition that has to be analyzed is the post-fault operation of the S-TRU in terms of having unchanged output voltage and DC output voltage. This experiment is shown in the following figures. Fig. 2.16 (a) shows the AC current and the overall output voltage of the CHB when a fault happens at the time $t = 0$ s. The remaining CHB cells increase the duty cycles and the current amplitude is unaffected. A higher ripple appears due to the reduction of the effective switching frequency. Fig. 2.16 (b) shows that at time $t = 0$ s the faulty cell is bypassed. Fig. 2.16 (c) shows the particular of the DC-link voltages at the moment of the fault. Although the power consumption changes abruptly, the QAB control still regulates the DC voltage.

Fig. 2.17 (a) and Fig. 2.17 (b) shows the waveforms of the QAB during the transition. The top waveforms refers to the cell that increases its loading, while the bottom waveforms refers to the excluded cell. These experiments show how the control of the QAB always regulates the DC voltage regardless the output power.

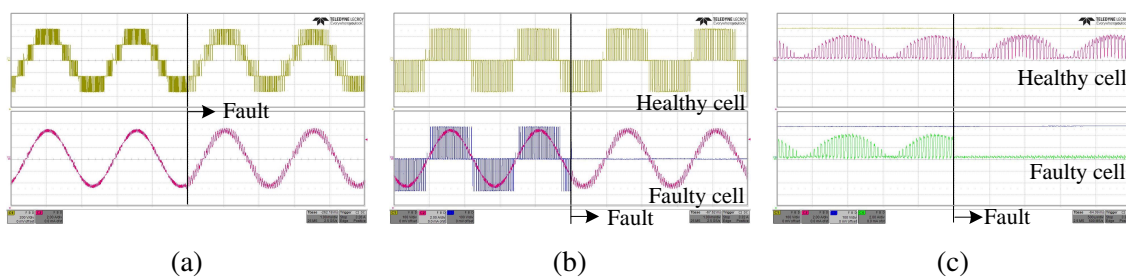


Figure 2.16: Experimental results when one cell is excluded due to failure: (a) AC current and output voltage of the CHB, (b) AC voltage and current of the CHB cells and (c) DC voltage and AC current of the CHB cells.

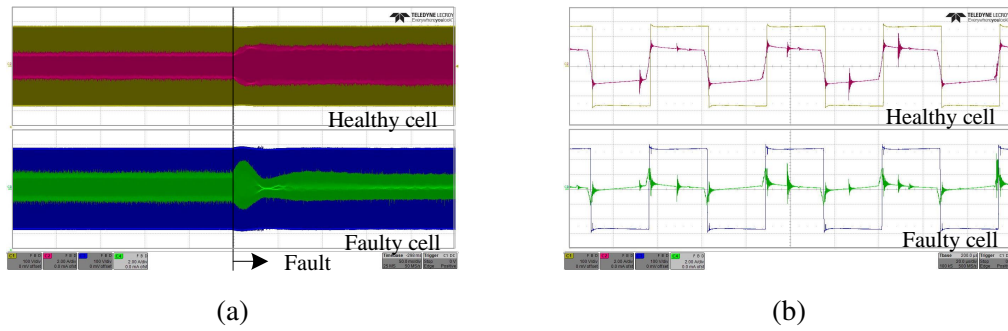


Figure 2.17: Experimental results when one cell is excluded due to failure: (a) Envelope of high frequency waveforms of voltage and current and (b) enlarged high frequency waveforms of voltage and current.

2.3 Large-scale Photovoltaic system

As a countermeasure for the recent environmental issue and the limited fossil resources, the demand for renewable energies has been continuously increasing over the past few decades. Remarkably, the statistics for the renewable electricity capacity growth is presenting the total 805 GW during 2011-2016, where the Wind Turbines (WTs) and solar PVs are responsible for 285 GW and 260 GW, respectively [61]. The PV is evidently one of the most attractive renewable energy sources, contributing to zero-emission generation and benefits of limited mechanical challenges compared with the WTs.

The power converters play an important role in grid-connected PV systems not only to regulate the grid currents but also to maximize the generated power from PV modules with Maximum Power Point Tracking (MPPT) algorithms. Similar to the ST application, the architecture for PV system can be categorized depending on the number of the power conversion stage: single-stage (DC/AC) and two-stage (DC/DC and DC/AC) as shown in Fig. 2.18 (a) and (b), respectively [62]. Here, the non-isolated DC/DC stage can be employed for the low-voltage grid application (see Fig. 2.1 (c)). However, for the medium-voltage operation, the isolated DC/DC stages are essentially required in order to electrically insulate

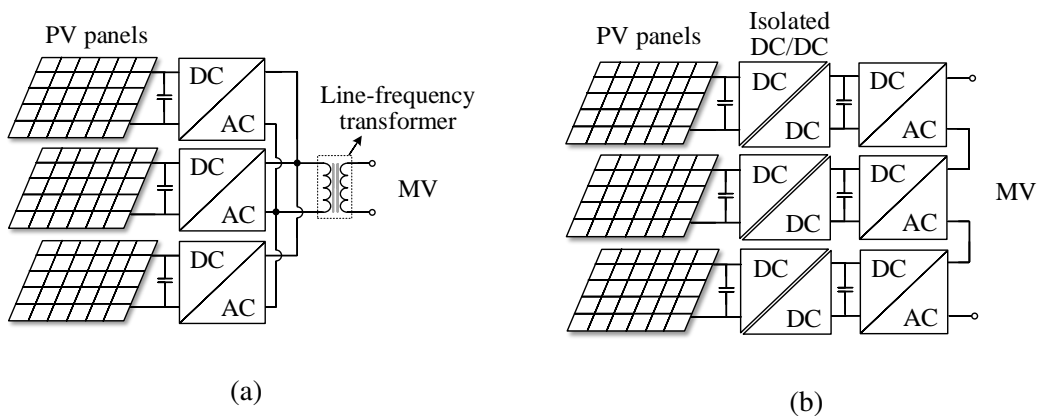


Figure 2.18: Modular architectures for large-scale PV system depending on the number of power conversion: (a) single-stage and (b) two-stage [62].

the PV module frames from the medium-voltage grid, because currently PV modules on the market are able to withstand below 1 kV [63]. Additionally, by employing the DC/DC stages operating at medium-frequency as shown in Fig. 2.18 (b), the size and weight for passive components can be significantly reduced compared with the single-stage system adopting line-frequency counter components shown in Fig. 2.18 (a) [64].

In addition, for large-scale PV systems, the modular converters have been intensively considered as one of the most suitable solution. This is because, for non-modular architectures, the centralized PV modules (series-parallel combination of multiple PV modules), which stands over a large area, brings inefficient energy generation due to mismatched environment conditions among the multiple modules such as partial shading and temperature [62, 65]. By employing the modular converters, each PV module (or string) can be connected to a respective DC/DC converter, permitting to independently perform the MPPT algorithms and consequently, improving the energy generation regardless the mismatched environment conditions [30, 31]. Here, this scenario can be translated to that each path shall be differently loaded, hence, each cell would have different degradation in nature by the year of operation.

3 Reliability of Power Semiconductors

Power semiconductor technology such as Insulate Gate Bipolar Transistor (IGBT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which are widely used in various applications [66, 67, 68], enables to achieve a higher power conversion efficiency with a flexible controllability. Nevertheless, since it has been reported that the power semiconductor devices are one of the most prone components to failures in power systems [14], their reliability issue is emerging to ensure a power security and to prevent extra cost for maintenance. Hence, it has created the need to clearly understand the root-cause of the failures and to explore innovative approaches to guarantee a longer operation time (i.e. high reliability) under harsh environment. The outcomes from two projects, LESIT (Leistungs Elektronik Systemtechnik und Informations technologie) (1993-1995) and RAPSDRA (1995-1998), are the representative references to address the root-cause of failures and the reliability evaluation. In the LESIT project [26], it was concluded that the thermal cycling highly affects the number of cycle to failure, providing the thermo-mechanical based lifetime model. Further, the RAPSDRA project showed the influence of the thermal cycling period on the thermal related failure mechanisms [69].

In this section, the selected failure mechanisms, which are especially thermo-dependent, are described, considering an inner structure of the power module. Then, referring the results from the above projects, the relation between the thermal stresses and the failures is discussed in order to motivate the necessity to achieve the reduced thermal stresses for the high reliable device. Finally, the conventional active thermal control methods are reviewed and categorized depending on the application level, addressing their constraints on the real-field implementation.

3.1 Structure of Power Semiconductor Module

The power semiconductor devices, which are in a module configuration, are widely employed for most of applications with economic feasibility by means of providing the electrical connection among several power semiconductor chips and circuits within an individual module [70]. Moreover, the module type features to effectively dissipate generated heat to a cooling system and to protect from harmful ambient influences, offering easy and reliable mechanical connectivity [71]. The power device module is typically standardized, in accordance with a package structure, into a wire-bonded and a press-pack type [3, 70]. The wire-bond type is available in wide power range with reasonable price [72], implying that it is further applicable in various applications than the press-pack type that is lying only in extreme high power range with higher cost. In this thesis, the wire-bonded type is therefore under study to address its reliability issue.

The cross-section of the standard wire-bonded module is shown in Fig. 3.1 [73, 74], consisting of a base plate, a substrate, power semiconductor chips (IGBT and diode) and bond wires. The base plate serves to spread the heat generated from the power semiconductor

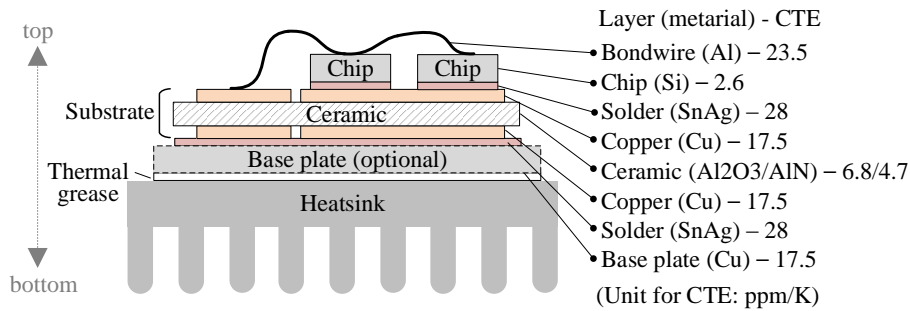


Figure 3.1: Cross section for DBC substrate structure of power module and CTE for a corresponding layer [73, 74].

chips by means of a providing a wide contact area to the heat sink and this is usually made of the copper (Cu). The substrate is usually constructed in a sandwich form (bottom copper-ceramic-upper copper), so called as Direct Bonded Copper (DBC). The upper copper has a certain circuitry pattern to conduct current, while the bottom one is plain to be soldered on the base plate and consequently to provide a good thermal conductivity. The ceramic is usually made of aluminum oxide (Al₂O₃) or aluminum nitride (AlN) in order to provide electrical insulation between the power semiconductor chips and the heat sink. The bottom side of the power semiconductor chips are soldered onto the upper copper of the substrate and the top of the chips is metalized to offer electrical connection through the bond wires. Finally, the power module is filled with silicone gel or epoxy resin for insulation against dust and water and then, cased by plastic to provide electrical insulation [73, 74].

Focusing on the reliability issue, the failure mode can be divided into the catastrophic failures caused by over-voltage, over-current or over-temperature (random failure) and the accumulated ageing failure caused by thermo-mechanical stress (wear-out failure). To address the failure mechanisms due to the accumulated ageing, it needs to understand the reasons of the thermo-mechanical stress. Seeing Fig. 3.1, the heat is basically produced from the power semiconductor chips as a results of the conduction and switching losses, and this is dissipated to the heat sink through the base plate in order to protect the power semiconductor chips from over-temperature [75]. Moreover, it can be recognized that the Coefficient of Thermal Expansion (CTE), which is material dependent parameter, is different for each adjacent layers. This means that the thermal cycle causes a different repeated physical expand and shrink in all layers, forcing the mechanical stress in joint between adjacent layers [76]. Consequently, the power modules, which are under a power fluctuation causing the thermal cycle for a long time, experience the wear-out failure due to the accumulated thermo-mechanical stress [28, 76].

3.2 Discussion of Selected Failure Mechanisms

The major failure mechanisms of the power device are introduced: the bond wire fatigue, the solder fatigue, the metallization reconstruction, and the gate oxide failure [73, 74, 77].

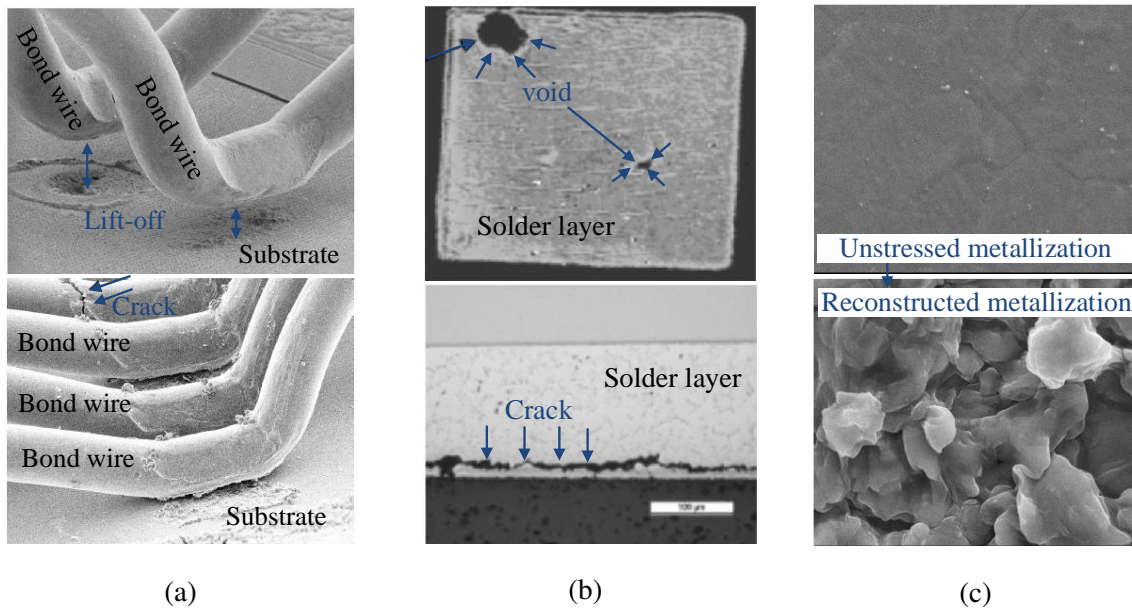


Figure 3.2: Images of selected failure mechanisms for (a) bond wire fatigues (top: lift-off, bottom: crack), (b) solder layer fatigues (top: void expansion, bottom: crack) and (c) metallization reconstruction (top: smooth surface before reconstruction, bottom: rough surface due to reconstruction) [77].

Bond wire fatigue is one of the most frequent failure mechanisms, thus, the main limiting of the power device's lifetime. The bond wire is usually made of aluminum (Al) whose CTE is 23.5 ppm/K, and its one side is soldered on the power semiconductor chip that is made of silicon (Si) featuring 2.6 ppm/K. This is the largest mismatch among the materials constituting the power device, implying that the connection between them could be the weakest point due to the heaviest thermo-mechanical stress. There are two typical failure types related to the bond wire fatigue, bond wire lift-off and crack as shown in Fig. 3.2 (a). Further, once one of these failures is initiated in one of several bond wires, the current distribution is altered and the remaining bond wires should handle a higher current density. This situation accelerates the failure mechanism with a higher thermal stress on the remaining bond wires.

In order to prevent the bond wire related failures, several strategies based on the bond wire design and the packaging method have been discussed. The optimal design of the wire geometric was introduced in [23] and in this context, the optimal wire length was theoretically derived with the thermo-mechanical model. In [78], the copper bond wire was employed in order to provide a better thermal performance of the bond wire. On the other hand, the direct-lead-bonding structure was shown in order to replace the bond wire, which provides a wider bonding area and reduces the contact resistance [79], and in [21] the packaging method with a flexible circuit board was investigated. However, these strategies are based on a physical approach bringing economical issue due to increased cost for new material and manufacturing process.

Solder layer fatigue is another major failure mechanism, which is usually occurred in two solder joints, between power semiconductor chips and substrate and between substrate and

Table 3.1: Summary of the selected failure mechanisms

Failure Mechanism	Failure location	Main failure causes
Bond wire fatigue	Bond wire (Crack), Bond wire joint connection (lift-off between DBC-Bond wire-Chip)	Thermal cycle , Mean temperature
Solder layer fatigue	Solder joint (Chip-DBC-base plate)	Thermal cycle , Mean temperature
Metallization reconstruction	Metallized layer on the top of chips	Thermal cycle , Mean temperature, Current density
Gate oxide failure	IGBT oxide, Oxide/substrate interface	Mean temperature, Electric field , Current density

base plate. Similar to the bond wire fatigue case, the thermo-mechanical stress is applied to the solder joints due to the CTE mismatch with the thermal cycling, consequently resulting in the solder interface crack and the expanded void as shown in Fig. 3.2 (b). These degradations accelerate this fatigue and/or other failures like the bond wire fatigue and the metallization reconstruction as a result of increasing the thermal impedance and power losses due to a higher collector-emitter voltage, thus, in turn increasing the junction temperature on the power semiconductor chips.

As an effort to improve the strength of solder layer, the solder interfaces were replaced by silver (Ag) sintering technology in order to provide a better thermal conductivity [80] and several separated small size substrates were structured instead of one larger substrate in order to disperse the mechanical stress [22]. However, these solutions require a high-degree of manufacturing process, beside, the root-cause cannot be solved.

Metallization reconstruction is occurred in the metallization layer, which is etched on the power semiconductor chip in order to obtain a direct electrical connection. The reason for this fatigue is as well the mechanical stress caused by the thermal cycling, which is far beyond its elastic limit of the materials (normally aluminum). The exposure to this high mechanical stress for a long time causes either the extrusion of the aluminum grain or the voids formation at the grain boundary, which is occurred by a mechanism of the diffusion creep, the grain boundary sliding, or the plastic deformation, as shown in Fig. 3.2 (c). Consequently, this reconstruction increases the metal sheet resistance, namely a higher thermal impedance due to the rough surface, which would initiate and accelerate other failure mechanisms.

Gate oxide failure is caused by a deterioration of the oxide film as either an initial defect causing early failure or a long-term failure. Hence, the mechanism for each oxide film breakdown can be divided into two reasons, the high electric field exceeding a dielectric breakdown withstand voltage that causes the immediate failure and the relatively low electric field but being continuously applied for a long time that causes the quality degradation of the oxide film over time.

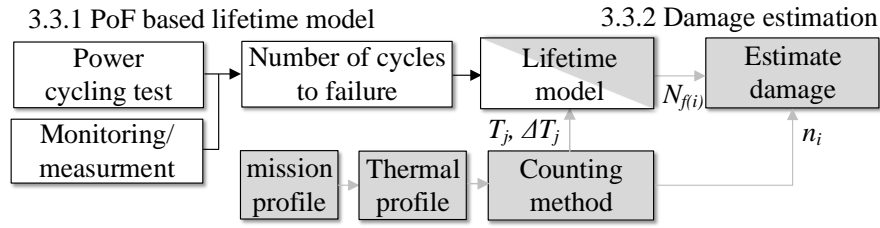


Figure 3.3: Methodology for the reliability evaluation.

To sum up, the table 3.1 describes the selected failure mechanisms, pointing out the the corresponding failure locations and highlighting the major failure cause. As it can be seen, the thermal stress is mainly responsible for the bond wire fatigue, the solder layer fatigue and the metallization reconstruction. Based on this, it can be concluded that the lifetime of power semiconductor devices can be modeled by taking the thermal stress as a critical affecting factor into account. In addition, the efforts to reduce the thermal stress is required in order to improve the reliability.

3.3 Reliability Evaluation based on Physics-of-Failure Approach

A methodology, which is for mapping the thermal stress to the lifetime, is discussed on the basis of the major failure mechanisms presented in the previous section. Fig. 3.3 shows the whole structure of the methodology, which can be divided into two parts: deriving a lifetime model based on the Physics-of-Failure (PoF) approach and estimating an accumulated damage translated from a mission profile. First, the lifetime model is derived, following the review of the power cycling test and the healthy status monitoring methods. Then, the accumulated damage estimation based on the derived lifetime model is presented. A thermal network is discussed to translate a mission profile into a thermal profile and a counting method is used to decompose the thermal profile. In this thesis, the PoF based lifetime model and the damage estimation are utilized in order for evaluating an effect of the proposed method on the lifetime improvement.

3.3.1 Lifetime model based on the Physics-of-Failure

The lifetime model have been derived based on either physical or analytic approach [25]. The physical approach enables to deeply reflect physical mechanisms but it is difficult to obtain a correct and comprehensive model due to a non-linearity and strong coupling between parameters within the power device. On the other hand, the analytic approach can be much simply performed by fitting ageing data from a power cycle or a thermal cycle test, even though the physical relation of the failure mechanisms is not clearly emerged. Because of the great advantage of the simplicity, the analytic approach has been widely utilized in the lifetime estimation of the power semiconductor devices [81, 82, 83].

The power cycle test, which is to apply a periodical thermal stress to a Device Under Test (DUT), is a widely employed method to understand the relation between the failure mechanisms and the thermal stress and consequently, to derive the lifetime model (i.e. number of cycle to failure that is so-called as PoF based lifetime model) [84]. For this purpose, a high thermal cycling with a high mean temperature, which are close to a rated value, is usually applied in order to accelerate the ageing process. This enables to obtain results within a reasonable testing duration. Basically, there are two means for the accelerated test, the DC current and the AC current approach [70, 84]. As it can be expected, for the first approach the thermal stress is imposed by a DC current supplier, while the DUT is always turned on [85, 86, 87]. Hence, this approach is referred as passive method and the simplest one in a configuration and operation of the test setup. However, the DUT is not under realistic operating conditions as only the conduction losses are devoted to generate the thermal stress and the influence of the switching losses and the high DC-link voltage are not taken into consideration. In addition, a high current amplitude is required for achieving a high thermal cycling with a short cycle period, since only the conduction losses contribute to the temperature increase. Therefore, an overloaded current distribution in the bond wires could be caused, which disturbs to obtain correct results. Otherwise, a long test period is needed with a lower current amplitude, which prevents to obtain results within a feasible period.

On the other hand, the AC current approach, which is so-called as active method [88, 89, 90], allows the DUT to act like a single-phase Pulse Width Modulation (PWM) converter. Hence, the DUT can be under a further realistic operating condition by reflecting both the conduction and switching losses. In addition, the switching frequency, fundamental frequency or power factor can be as a control parameter at the expense of a complex configuration of the test setup and relatively expensive cost [70]. As the final point, strategy for the power cycle test is an important factor and in [86], the effect of the four different strategies was investigated: the constant turn-on and -off time, the constant case temperature, the constant power loss and the constant temperature swing, concluding that each strategy derives a different number of cycle to failure. Therefore, it is essential to decide or to design the control strategy, intensively considering a target failure mechanism and application.

During the accelerated ageing test, it is essentially required to assess the degradation of the DUT so as not only to halt the test once it reaches a failure criteria but also to identify the failure mechanisms. This is typically achieved through identifying a variation of its junction temperature or electrical data in on- or off-line [91, 92, 93, 94]. The junction temperature can be directly measured by an infrared camera [95], thermocouples or optical fibers [96] in case the inside of the power device is accessible with an open module. Here, the open module should be unobstructive to a cooling conditions and uniformly coated with a known emissivity to ensure a correct temperature measurement [70]. As another possibility to monitor the failure indicators, the Temperature Sensitive Electric Parameters (TSEPs) are measured, which exploits the characteristic of varied parasitic electrical parameters by the degradation [97]. The TSEPs, which are commonly measured, are the collector-emitter voltage [93, 94] for estimating the damage of the bond wires and the internal gate resistance, which is located on the chip itself [98, 99], besides, there are various methods such as the gate threshold

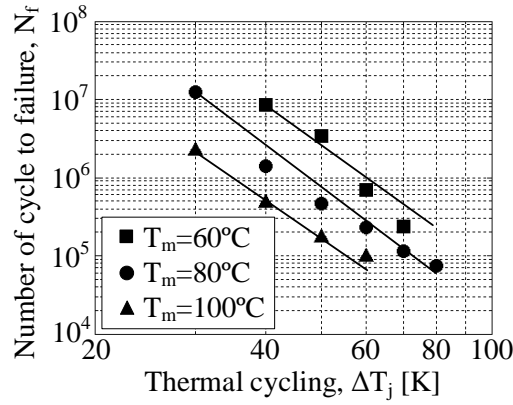


Figure 3.4: Number of cycles to failure as function of mean junction temperature and thermal cycling [26].

voltage [100], the leakage current [101], and switching characteristics [102, 103, 104].

The power cycling test was first introduced in the LESIT project [26] for investigating the relation between the reliability of the power device and the thermal stresses, which was followed by plenty of researches strongly supporting that the thermal stresses are closely related to the reliability. Fig. 3.4 evidently presents the influence of the thermal stresses on the reliability. The higher mean junction temperature and the thermal cycling amplitude result in the lower number of cycle to failure and vice versa. Based on Fig. 3.4 and the Coffin-Manson Arrhenius model [26, 17], the lifetime model of the power device can be expressed with the number of cycle to failure, N_f , in respect to the mean junction temperature, $T_{j,mean}$, and the thermal cycling amplitude, ΔT_j , as

$$N_f = a_1 \cdot (\Delta T_j)^{-a_2} \cdot e^{\frac{a_3}{T_{j,mean}}} \quad (3.1)$$

where a_1 and a_2 are parameters related with physical characteristics of the power device, which are obtained from the experimental data, and a_3 is a constant which can be calculated with the activation energy ($7.8 \cdot 10^4 \text{ Jmol}^{-1}$ or $\approx 0.8 \text{ eV}$) and the Boltzmann constant ($8.314 \text{ J/mol}\cdot\text{K}$).

The lifetime model in (3.1) is employed in this thesis in order to validate the effect of the proposed method on the lifetime improvement. However, advanced models have been derived based on the above model in [25, 105, 106]. For example, the Norris-Landzberg model considers thermal cycle frequency and the Bayerer model takes heating time, loading current, bond wire diameter and module block voltage into account.

3.3.2 Accumulated damage estimation

As shown in Fig. 3.3, the first stage of an accumulated damage estimation with a specific mission profile, is a translation from the power profile to a respective thermal profile. The junction temperature, T_j , can be obtained from (3.2), which is a simplified and widely used

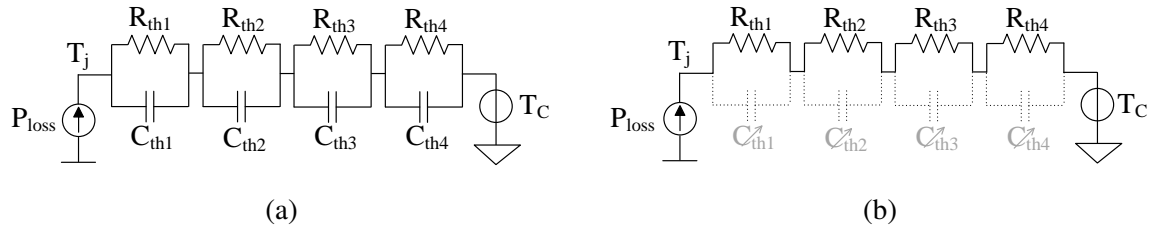


Figure 3.5: Cauer four layers thermal network for (a) short time scale and (b) medium and long time scale analysis.

model with the consideration of a single path from the junction to the case for thermal transfer.

$$T_j = Z_{th,jc} \cdot P_{loss} + T_c \quad (3.2)$$

where $Z_{th,jc}$ presents the thermal impedance between the junction to the case, P_{loss} is the power losses followed by the power profile and T_c is the case temperature. This junction temperature model is visualized in Fig. 3.5 (a), where the thermal impedance is modeled by a chain of thermal resistors and thermal capacitors.

On the other hand, the thermal profile can be analyzed with three time scales: short, medium and long time scale [15], where each time scale is defined as below.

- Short time scale (from *millisecond* to *second* range) means junction temperature fluctuations caused by the fundamental frequency of power converter, for example, it is 50/60 Hz for the grid-connected applications.
- **Medium time scale** (from *minute* to *hour* range) presents low frequency junction temperature fluctuations caused by a varied input and output power of the power converter. For example, wind speed and sun irradiation can be a major cause for the renewable energy systems.
- Long time scale (from *day* to *year* range) is junction temperature fluctuations with very low frequency, which is followed by environment conditions such as ambient temperature variation.

In fact, all of time scale should be comprehensively considered in order to evaluate a respective influence of the thermal profile in each time scale, which contributes to derive a further precise damage estimation, since the thermal profile in each time scale differently consumes the lifetime. However, for the sake of simplicity, the thermal profile is considered only in the medium time scale, where the thermal capacitors in the junction temperature model (see Fig. 3.5 (a)) can be negligible. Therefore, the model is simplified as shown in Fig. 3.5 (b), only considering the thermal resistors. Furthermore, the thermal resistance is considered as a constant by ignoring its variation due to the degradation. This is reasonable since the ageing process is much slower than the medium time scale.

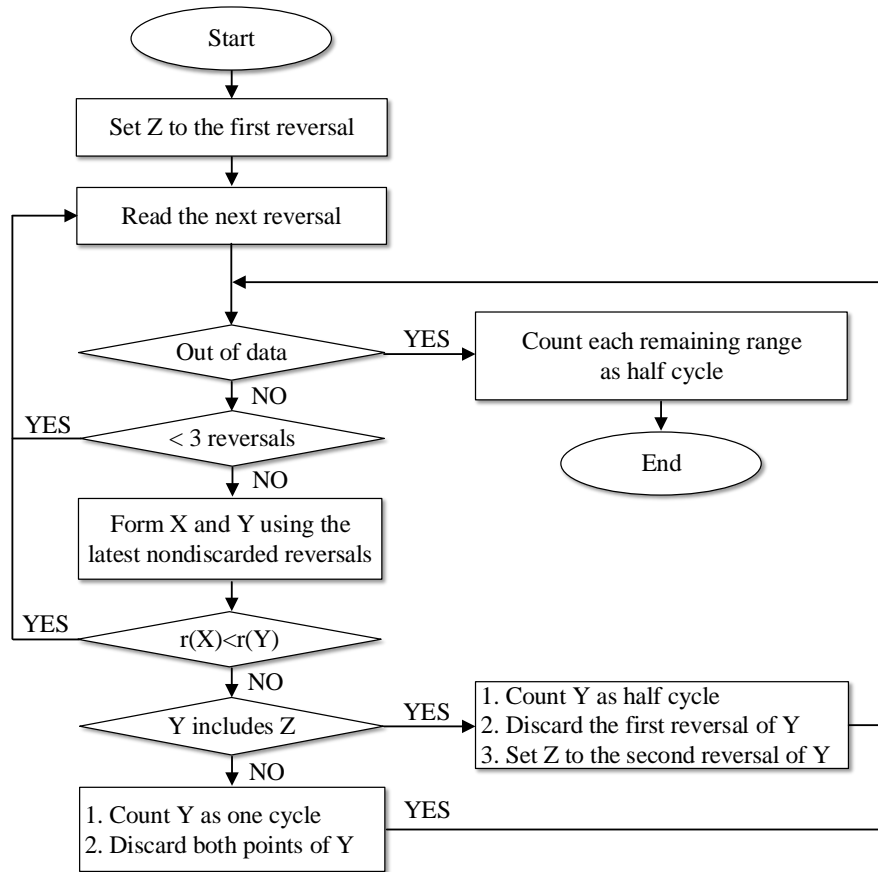


Figure 3.6: Flowchart for the rainflow counting algorithm.

Consequently, assuming that the case temperature is a constant, the variation of the junction temperature is solely dependent on the power losses as

$$T_j = R_{th,jc} \cdot P_{loss} + T_c. \quad (3.3)$$

The fluctuated thermal profile in time domain implies that it is superimposed of various stress level (i.e. combination of diverse mean junction temperature and thermal cycling amplitude). However, the lifetime model in (3.1) is able to handle only a single thermal cycling at once, which is not sufficient to be immediately applied for the fluctuated profile.

A pre-counting method to extract each thermal cycling needs to be applied in order to facilitate the lifetime model. The rainflow counting algorithm is a statistical method for analyzing the process of random load (thermal profile) in a manner that defines a cycle as a closed hysteresis loop. Hence, each closed hysteresis loop has a strain range (amplitude of temperature swing) and mean stress (mean temperature) [25, 107]. The flowchart is shown in Fig. 3.6, where

- The first and second points are collectively called X.
- The second and third points are collectively called Y.

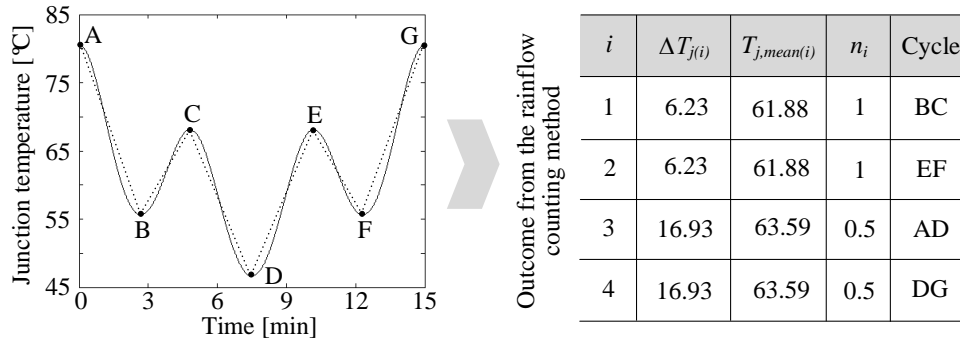


Figure 3.7: A simple thermal profile as an example and the result of the rainflow counting method.

- In both X and Y, the points are sorted from earlier to later in time, but are not necessarily consecutive in the reversal sequence.
- The range of X, denoted by $r(X)$, is the absolute value of the difference between the amplitude of the first point and the amplitude of the second point. The definition of $r(Y)$ is analogous.

In this flowchart, three consecutive points are checked to determine whether a cycle is formed or not, following the basic rules:

- The low amplitude cycles are separated from the high amplitude ones.
- A counted cycle is discarded and the remaining points are connected together.
- The remaining residue is counted until all the points are exhausted.

As a case study, a simple thermal profile shown in Fig. 3.7 (left) is considered and each cycle is extracted through the flowchart as shown in Fig. 3.7 (right). The detailed sequence for the profile is attached in appendix 9.1.2. On the basis of the outcome from the counting method, firstly, the number of cycle to failure, $N_{f(i)}$, for each thermal stress level, i , is calculated by (3.1) and then, the damage, D_i , by each thermal stress level can be obtained by (3.4), by taking the number of extracted cycles for each thermal stress level, n_i [108].

$$D_i = \frac{n_i}{N_{f(i)}} \quad (3.4)$$

Finally, since the wear-out failure is a result of the accumulated damage, it needs to add up the consumed damages by each of the detected thermal cycles and this can be accomplished with the Miner's rule as

$$D = \sum_{i=0} D_i \quad (3.5)$$

where each damage, D_i , is linearly accumulated and the device is expected to fail when the accumulated damage, D , reaches to 1 [82].

3.4 Review of Active Thermal Control Methods

The thermal stresses caused by a mission profile are the immediate cause for the wear-out failures. To address the thermal stress reduction without additional and over-designed hardware or to minimize the hardware efforts, the concept of the active thermal control has been established, which is based on a software manipulating the loss-related variables. In this section, the conventional active thermal control methods are reviewed and categorized according to the application level: control, modulator and device level as shown in 3.8, and their constraints are discussed in the following.

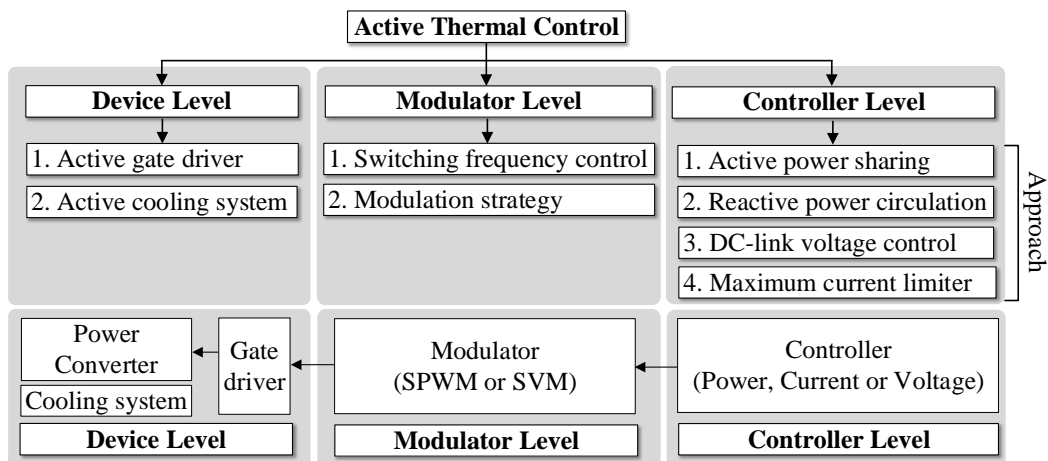


Figure 3.8: Classification of active thermal control according to application level: controller, modulator and device level.

3.4.1 Controller level

As the first and second approach in Fig. 3.8, the active power sharing and the reactive power circulation methods are restricted only to the paralleled power electronics building blocks. The active power sharing method in [109, 110] exploited the unbalanced power loading based on the junction temperature in order to improve the overall system efficiency as well as the reliability, instead of equally sharing the total power among parallel converters. However, its capability is limited to the available active power from the converters and there still is an issue for the overloaded converter to be exposed to higher thermal stresses. On the other hand, the reactive power considerably influences on the loss distribution by modifying both of the voltage and current amplitude and phase angle. Since this method uses the reactive power, its capability is independent on the available active power. The reactive power circulation method in [111] utilized these merits to compensate the temperature swing of the most stressed device by increasing its generated losses, considering the three-level Neutral Point Clamped (NPC) converter. However, this method prevents for the junction temperature to cooling down and increases the thermal stresses of other devices.

For the traction drive application with the Permanent Magnet Synchronous Machine (PMSM), the dynamic DC-link voltage method (the third approach in Fig. 3.8) was proposed in [112],

which aims at adjusting the voltage level depending on the required PMSM terminal voltage (i.e. depending on the torque-speed operating point). Consequently, the losses for the converter and motor could be significantly reduced at the low speed range with the lower DC-link voltage. However, the dynamic performance of the voltage controller would be constraint on the capability and in addition, the stability of an overall control structure with the variable DC-link voltage would bring another issue.

Finally, the current limit approach was applied in [24, 113], in combination with the switching frequency control in the modulator level category. In [24], the current limit value was determined by the Proportional-Integral (PI) closed loop to limit the amplitude of the temperature swing, as assisting the switching frequency control. For the traction application in [113], the efficiency and torque could be maximized, achieving the thermal management.

3.4.2 Modulator level

The modulator level directly handles loss-dependent variables as a control parameter to modify the loss distribution, therefore, this is application-invariant but could be dependent on the power converter topology.

It is well-known that the switching frequency highly affects the switching losses, implying that it can be a good candidate of the control parameter for the active thermal control. Based on this, the literature of [114, 115, 116] exploited the switching frequency to heating up the junction temperature when the loading power is decreasing. Therefore, the thermal cycling by the fluctuating power loading can be compensated. However, the energy efficiency becomes lower as well as the mean junction temperature is settled at a higher level. To avoid these shortcoming, the switching frequency was controlled in an opposite way in [117, 118]. Furthermore, [119] proposed the combined method of the switching frequency control and the discontinuous modulation for the traction application to achieve the further reduced mean temperature. However, the above approaches employing the variable switching frequency make the current spectrum to be varied, implying a difficulty for the filter design to comply with the power quality requirement.

As another approach, the thermal distribution among the power devices are relocated to relieve the stress of devices under the highest stress level. By the Distributed Commutations Modulation (DCM) [120], the device switching frequency could be minimized with the evenly distributed thermal loading among cells in the Cascaded H-Bridge (CHB) converter for all range of the modulation index. Similar to this, the new series of the Space Vector Modulation (SVM) for the three-level NPC converter was proposed in [121], which enable to effectively relocate the device stress within the moderate modulation index range. Hence, the stress on the clamping diode and the inner devices, which are the most stressed devices, could be relived. However, these methods are highly dependent on the converter topology, which restricts the universal applicability.

Table 3.2: Categorization of the conventional active thermal control methods

Level	Approach	Principle	Constraints
Controller Level	Power sharing	Redistribute stress	1. Parallel converter 2. Stress migration
	Reactive power circulation	Heating up (increase losses)	1. Parallel converter 2. Higher mean temperature
	DC-link voltage control	Reduce losses	1. Traction application 2. Low control stability
	Current limiter	Limit power	1. Limit power capability
Modulator Level	Varied switching frequency	Heating up or Cooling down	1. Varied current spectrum 2. Low control stability 3. Higher mean temperature
	DCM	Reduce losses	1. CHB configuration
	SVM (new sequence)	Redistribute losses	1. 3-level NPC configuration
Device Level	Active gate driver	Heating up (increase losses)	1. Hardware effort 2. Higher mean temperature
	Active cooling	Heating up (increase losses)	1. Additional hardware 2. Higher mean temperature

3.4.3 Device level

The device level technically requires some hardware effort in the electric/electrical engineering point of view. Therefore, it is not a pure software-based approach unlike the control and modulator level.

In literature works, it has been revealed that the characteristic of the gate signal from a gate driver highly affects the generated losses of power device [122, 123, 124]. Based on this fact, the active gate driver approach was derived. In [125], a specified schematic of the gate driver was proposed in order to regulate the gate voltage that is related to the conduction losses. On the other hand, the two step gate driver concept was proposed in [126] to manipulate the switching losses by adjusting the slew rate of the switching voltage and current with the variable turn-on time. However, the above approaches require the supreme design efforts for the gate driver because the gate signal should be precisely and sensitively controlled. Moreover, the gate driver might need to be re-designed, considering the intrinsic characteristic of different power devices.

The approach of controlling the cooling fan speed was proposed in [20]. The strategy is to heating up the device when a loading power is lower, by means of decreasing the fan speed, whereas the fan speeds up under a higher loading power. This strategy allows the temperature to be stable regardless of the mission profile, but with increased mean temperature.

The reviewed and categorized active thermal control methods are summarized in Table 3.2, describing the principle and constraints of each approach. As it can be seen, there are three

principle to reduce the thermal stresses: reducing losses to cooling down during high power operating point, increasing losses to heating up during low power operating point and redistributing losses.

3.5 Summary

On the basis of the wire-bonded structure of power modules, it has been addressed that the mismatch of the CTE between materials of the adjacent layer is the most critical reason for the thermo-mechanical stress, which causes the wear-out failures.

The linear accumulated damage estimation that involves the thermal network, the lifetime model and the rainflow counting method, were introduced as the evaluation methodology for the proposed method. In the following section 4, this methodology is employed in order to show the effect of the proposed active thermal control methods by estimating the accumulated damages under an arbitrary mission profile.

Finally, the conventional active thermal control methods have been reviewed and categorized according to the application level (controller, modulator and device level), pointing out the principle and constraints of each method. The most critical constraint of each level is defined in Table 3.3.

Table 3.3: Major constraint of each level

Application level	Major constraint
Controller	Application-dependent
Modulator	Topology-dependent
Device	Hardware effort required

4 Thermally-Compensated Modulation Strategies for Power Semiconductors

Considering the modular converters that are composed of unequally aged cells, the active thermal control methods based on modulator are proposed, which aims at prolonging the remaining useful lifetime of the most aged cells. The proposed methods target at the series and parallel modular converters, respectively, as below.

- For the parallel modular converter:
 - 4.2.1 *Power routing* based on multi-frequency modulation
 - 4.2.2 *Power routing* based on discontinuous modulation
- For the series and parallel modular converters:
 - 4.3 *Variable-clamping angle* discontinuous modulation

The proposed methods manipulate the loss-related parameters so as to achieve the reduced thermal stresses of the target cell. The analytical averaged loss model is first derived, which is to identify the influence of the proposed methods on the loss distribution, followed by their principle, capability and accumulated damage analysis. Furthermore, the influence of the proposed methods on the power quality is as well discussed.

4.1 Analytical Averaged Loss Model for Cascaded H-Bridge Inverter

It is well-known that the power loss estimation of power converters in design process is essentially required as significantly contributing to achieve an enhanced design like higher efficiency, smaller size and lower cost. Furthermore, to address the thermal-dependent failures of power devices, their power losses need to be accurately analyzed, since the thermal stresses are very closely associated with the power losses [127].

The power losses of power device are basically composed of two parts: switching losses and conduction losses. The switching losses were conventionally calculated by using the collector current–blocking voltage ($I_c - V_{dc}$) switching characteristics [128, 129], but further convenient approach based on the switching energy–collector current ($E_{sw} - I_c$) has been widely employed in many literature [130, 131, 132]. The estimation of the conduction losses

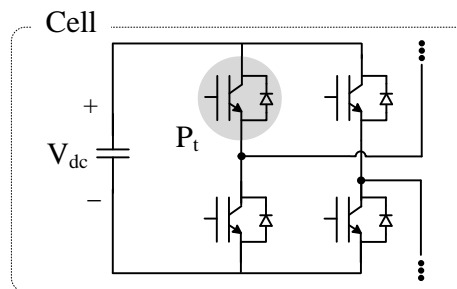


Figure 4.1: Considered power device in the CHB converter for the loss model.

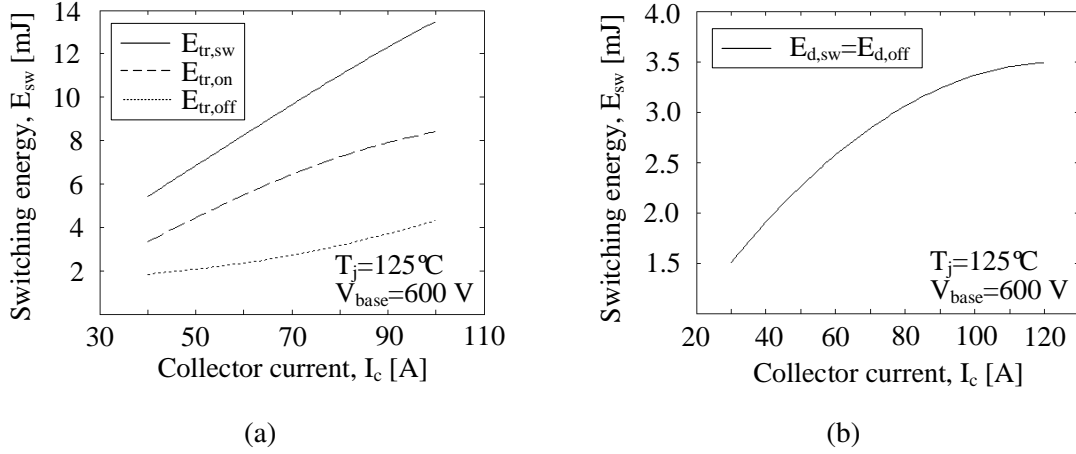


Figure 4.2: Switching energy characteristic as a function of the collector current ($E_{sw} - I_c$ curve) for (a) IGBT and (b) diode (part number: IXYB82N120C3H1).

is generally conducted with the on-state voltage–collector current ($V_{ce} - I_c$) characteristic linear approximation [128]. In this section, based on the $E_{sw} - I_c$ and $V_{ce} - I_c$ characteristics approximation approaches, the analytical averaged loss model is established, which is for the CHB converter modulated with the Phase-Shifted Pulse Width Modulation (PSPWM). Hence, the derived model, P_t , considers only the upper device in the first leg as shown in Fig. 4.1 and the whole system loss, $P_{sys,t}$, can be simply obtained by multiplying the number of used power devices, $4K$, as

$$P_{sys,t} = 4K \cdot P_t = 4K \cdot (P_{sw} + P_{cd}) \quad (4.1)$$

where K is the number of cells. For instance, K is 3 for the 7-level CHB converter. Here, the P_{sw} and P_{cd} represent the switching and conduction losses, respectively, which are derived in the following.

4.1.1 Switching losses

The switching energy characteristic as a function of the collector current ($E_{sw} - I_c$ curve) is illustrated in Fig. 4.2, which is obtained from a datasheet (part: IXYB82N120C3H1). Generally, a sum of the turn-on and -off energy is considered to analyze the total switching losses for Insulate Gate Bipolar Transistor (IGBT), whereas the diode's total switching losses treat only the turn-off energy (i.e. reverse recovery energy), since their turn-on energy is relatively and negligibly low compared with the turn-off energy. Hence, the total switching energy during one complete switching cycle, $E_{tr,sw}$ for IGBT and $E_{d,sw}$ for diode, is expressed by

$$\begin{cases} E_{tr,sw} = E_{tr,on} + E_{tr,off} & \text{(for IGBT)} \\ E_{d,sw} = E_{d,off} & \text{(for diode)} \end{cases} \quad (4.2)$$

where the subscript tr and d represent *transistor* and *diode*, respectively. Assuming that the switching energy is linearly proportional to a DC-link voltage, the total switching energy can be approximated to a second-order equation with respect to the collector current as

$$E_{sw} = \frac{V_{dc}}{V_{base}} \cdot (a \cdot I_c^2 + b \cdot I_c + c) \quad (4.3)$$

where the V_{dc} is the DC-link voltage, the V_{base} is a reference voltage used for $E_{sw} - I_c$ curve derivation in the datasheet, the I_c represents the collector current and the a , b and c are curve fitting constants. Here, the E_{sw} can be substituted with either $E_{tr,sw}$ or $E_{d,sw}$. Further, assuming that the switching events are evenly distributed over a fundamental period (i.e. switching frequency is much higher than the fundamental frequency), the averaged switching energy, $E_{avg,sw}$, is found by the integration of the switching energy in

$$\begin{aligned} E_{avg,sw} &= \frac{1}{2\pi} \int_{\theta_1}^{\theta_2} E_{sw} d\theta \\ &= \frac{1}{2\pi} \cdot \frac{V_{dc}}{V_{base}} \int_{\theta_1}^{\theta_2} (a \cdot I_c^2 + b \cdot I_c + c) d\theta \end{aligned} \quad (4.4)$$

where the $[\theta_1, \theta_2]$ is an angle interval, in which the device switches during the fundamental period. Finally, the switching losses can be derived by multiplying the average switching energy and the switching frequency as

$$\begin{aligned} P_{sw} &= E_{avg,sw} \cdot f_{sw} \\ &= \left[\frac{1}{2\pi} \cdot \frac{V_{dc}}{V_{base}} \int_{\theta_1}^{\theta_2} (a \cdot I_c^2 + b \cdot I_c + c) d\theta \right] \cdot f_{sw}. \end{aligned} \quad (4.5)$$

For the CHB converter operated with the continuous and sinusoidal modulation signal, the angle interval is either $[0, \pi]$ for the upper device or $[\pi, 2\pi]$ for the lower device (see Fig. 4.1) and it should be mentioned that the switching losses for both devices are identical. Further, it is assumed that the collector current, I_c , is sinusoidal with the amplitude, I_{pk} , as

$$I_c = I_{pk} \cdot \sin(\theta). \quad (4.6)$$

Therefore, by substituting (4.6) into (4.5) and considering the upper device (i.e. angle interval= $[0, \pi]$), the averaged switching losses can be derived through

$$P_{sw} = \left[\frac{V_{dc}}{V_{base}} \cdot \frac{1}{2\pi} \int_0^{\pi} (a \cdot (I_{pk} \cdot \sin(\theta))^2 + b \cdot (I_{pk} \cdot \sin(\theta)) + c) d\theta \right] \cdot f_{sw}. \quad (4.7)$$

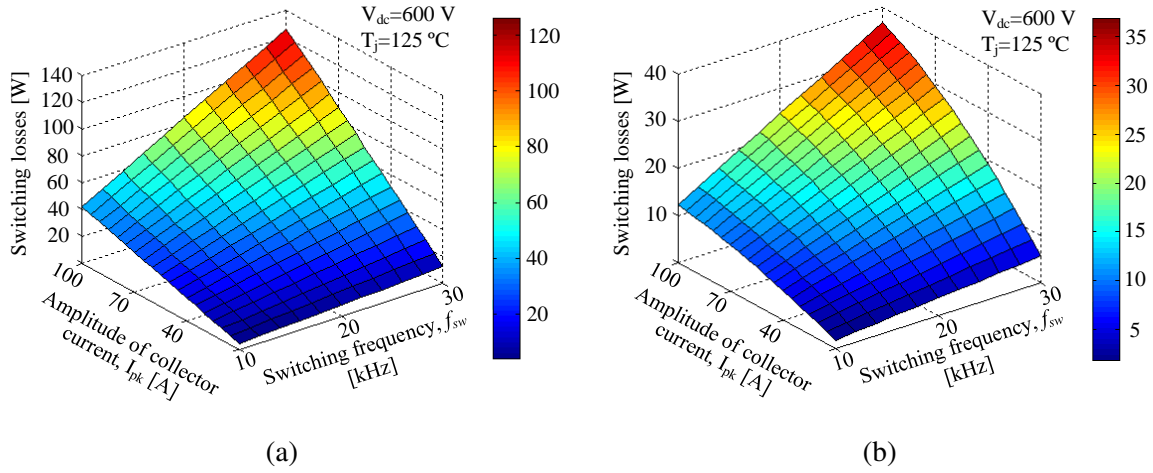


Figure 4.3: Analytic averaged switching losses of (a) IGBT and (b) diode (part number: IXYB82N120C3H1).

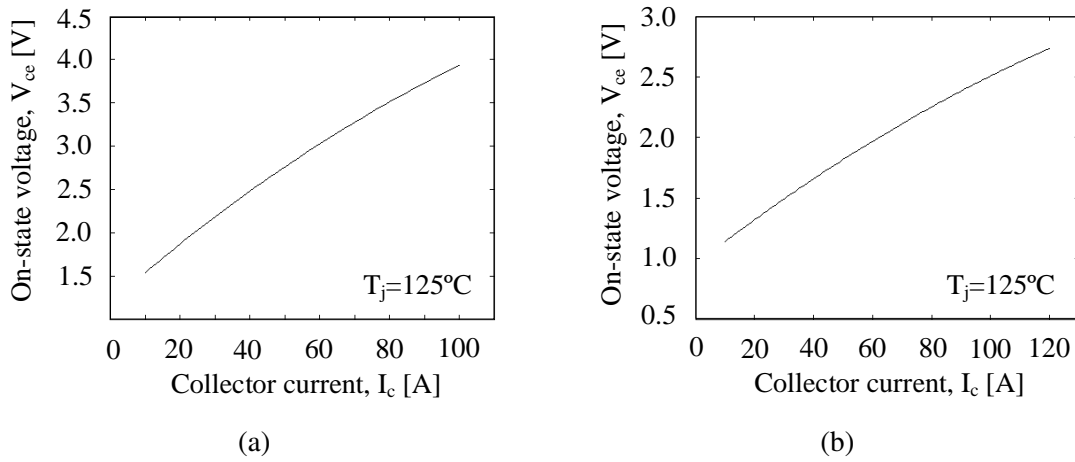


Figure 4.4: On-state voltage–collector current ($V_{ce} - I_c$) characteristic curve for (a) IGBT and (b) diode (part number: IXYB82N120C3H1).

As it can be seen, the switching losses are directly affected by the DC-link voltage, the collector current and the switching frequency. Remarkably, the DC-link voltage and the switching frequency is linearly proportional to the switching losses.

Based on the above (4.7), the switching losses are calculated under the DC-link voltage of 600 V as a function of the switching frequency and the collector current. Finally, the result for the IGBT and the diode is shown in Fig. 4.3 (a) and (b), respectively.

4.1.2 Conduction losses

Similar to the previous case, the approximation approach of the $V_{ce} - I_c$ characteristic curve can be employed to derive the averaged conduction loss model. The $V_{ce} - I_c$ curve for the IGBT and the diode, which is obtained from the datasheet, is shown in Fig. 4.4 (a) and (b), respectively, and this is usually approximated by a linear line as

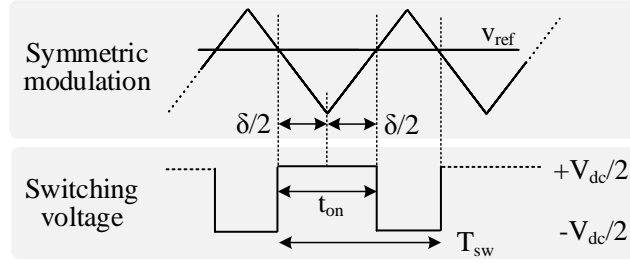


Figure 4.5: Symmetric modulation and switching voltage of the IGBT.

$$\begin{cases} V_{ce} = V_{ce0} + I_c \cdot r_{tr0} & (\text{for IGBT}) \\ V_f = V_{f0} + I_c \cdot r_{d0} & (\text{for diode}) \end{cases} \quad (4.8)$$

where the V_{ce0}/V_{f0} is the device initial voltage drop and the r_{tr0}/r_{d0} is the equivalent resistance to represent the linear region of device voltage drop.

Before deriving the model, it should be mentioned that the converter is modulated with the symmetric modulation strategy shown in Fig. 4.5 [132]. A voltage reference, v_{ref} , is expressed in

$$v_{ref} = \frac{V_{dc}}{2} \cdot M \cdot \sin(\theta + \phi) \quad (4.9)$$

where M is the modulation index and ϕ presents the Power Factor (PF) angle. Assuming that the switching frequency is much higher than the fundamental frequency, the average output voltage can be considered to be equal to the voltage reference. Hence, the effective duty cycle, $\delta = t_{on}/T_{sw}$, of the IGBT that switches between $\pm V_{dc}/2$ can be defined as

$$\begin{aligned} \frac{V_{dc}}{2} \cdot M \cdot \sin(\theta + \phi) &= \frac{V_{dc}}{2} \left(\frac{t_{on}}{T_{sw}} - \frac{T_{sw} - t_{on}}{T_{sw}} \right) \\ \Rightarrow \delta_{tr} = \frac{t_{on}}{T_{sw}} &= \frac{1}{2} [1 + M \cdot \sin(\theta + \phi)] \end{aligned} \quad (4.10)$$

where δ_{tr} is the effective duty cycle for the IGBT and that for the diode, δ_d , is easily obtained by the fact that the IGBT and diode are complementary conducted. This is expressed in

$$\delta_d = 1 - \delta_{tr} = \frac{1}{2} [1 - M \cdot \sin(\theta + \phi)]. \quad (4.11)$$

The average conduction losses over the fundamental period can be found as the integral of the instantaneous conduction loss during the angle interval, $[\theta_1, \theta_2]$, where the device carries the current, as expressed in

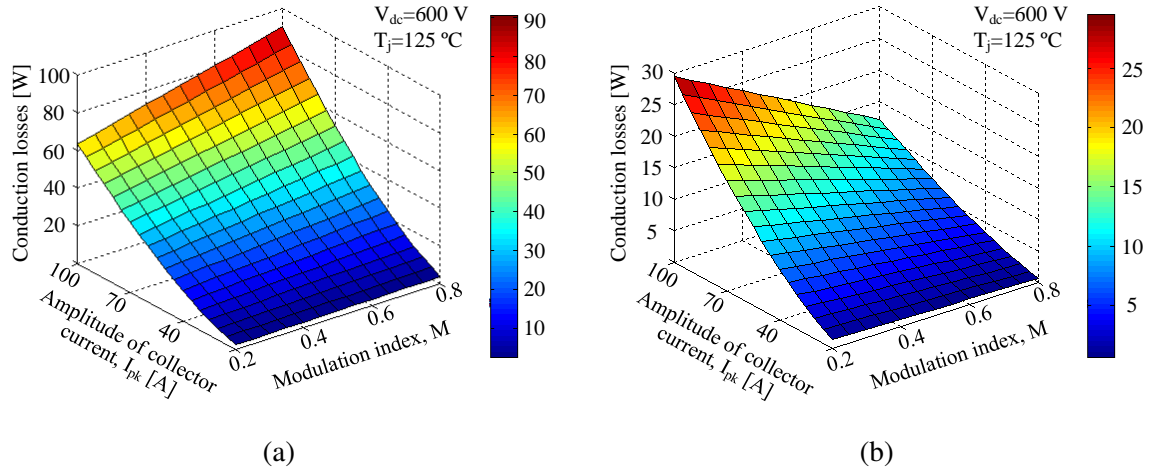


Figure 4.6: Analytic averaged conduction losses of (a) IGBT and (b) diode with $PF = 1$ (part number: IXBY82N120C3H1).

$$P_{cd} = \frac{1}{2\pi} \int_{\theta_1}^{\theta_2} \delta \cdot I_c \cdot V_{ce} d\theta. \quad (4.12)$$

Finally, by substituting (4.6), (4.8) and either (4.10) for the IGBT or (4.11) for the diode into (4.12) and considering the angle interval of $[0, \pi]$, the averaged conduction losses of the IGBT, $P_{tr,cd}$, and the diode, $P_{d,cd}$, can be calculated by

$$\begin{cases} P_{tr,cd} = \frac{1}{2\pi} \int_0^{\pi} \frac{1}{2} [1 + M \cdot \sin(\theta + \phi)] \cdot I_{pk} \cdot \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \\ P_{d,cd} = \frac{1}{2\pi} \int_0^{\pi} \frac{1}{2} [1 - M \cdot \sin(\theta + \phi)] \cdot I_{pk} \cdot \sin(\theta) \cdot (V_{f0} + I_c \cdot r_{d0}) d\theta \end{cases} \quad (4.13)$$

Through this equation, it is identified that the conduction losses are a function of the switching function of the modulation index, the collector current and PF angle. Fig. 4.6 shows the calculated conduction losses of the IGBT and the diode depending on the modulation index and the collector current, assuming the unit PF.

4.2 Modulation Strategies for Power Routing

The modular converter structure inherently presents the different power paths since each CHB cell is fed by a respective DC/DC converter as shown in Fig. 4.7. To the current state, several techniques to guarantee the equally distributed power loading have been studied in order to share the stress identically [133, 134, 135]. However, based on that the modular converter is the system composed of differently aging cells during the year of operation, the concept to equally distribute the loading power is not relevant at all to address the reliability improvement of the modular converters.

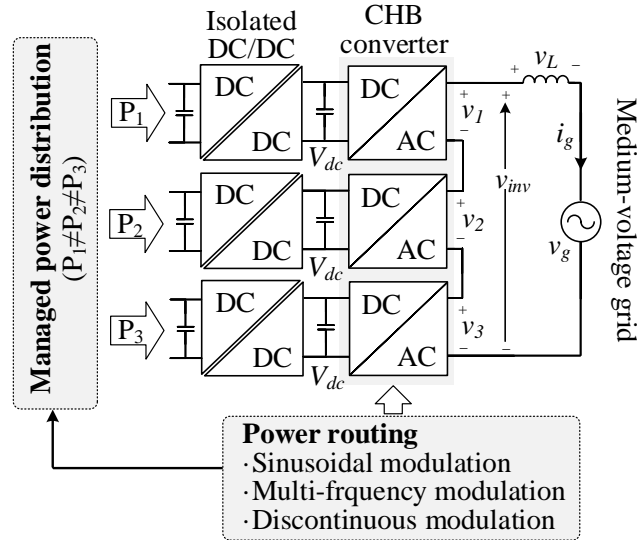


Figure 4.7: Concept of the power routing based active thermal control.

As an optimal solution for the reliability-oriented operation, the parallel paths can be unequally loaded depending on the remaining useful lifetime of DC/DC converter so as to delay as much as possible the failures of the weakest converter by shifting its loading. This concept refers the *active thermal control by means of power routing* [11]. Here, it is assumed that the health status is informed with proper monitoring methods. The power routing concept is illustrated in Fig. 4.7, in which the CHB converter performs the power routing modulation in order to manage the loading power of each DC/DC converter (i.e. $P_1 \neq P_2 \neq P_3$).

A sinusoidal modulation is a straightforward way, where each CHB cell has different modulation index. This is demonstrated in Fig. 4.8 when the modulation index under the balanced condition is 0.8 as a case study, where v_1 , v_2 and v_3 are the cell voltage, v_{inv} is the total converter voltage, v_L is the voltage drop across the filter inductor, and v_g presents the grid voltage. In case of the balanced condition shown in Fig. 4.8 (a), the modulation index for each cell is identical ($M_1 = M_2 = M_3$), while equally sharing the total voltage ($v_{inv} = v_1 + v_2 + v_3$, $v_1 = v_2 = v_3$) and consequently equally loading the total power. On the other hand, as shown in Fig. 4.8 (b), the unbalance power loading is realized by the unequal modulation index. However, remarkably, the maximum capability of the unbalance power is intensively restricted to the DC-link voltage margin that is recommended to be designed as low as possible due to the efficiency, filter size and power quality reasons. Further, in the maintenance's point of view, it could be beneficial to completely unloading (i.e. deactivation) a damaged DC/DC converter, which is highly limited to achieve by the sinusoidal modulation.

In the following, two modulation methods: multi-frequency and discontinuous modulation are proposed, which aim at maximizing the power routing capability, furthermore, enabling the deactivation of a damaged path.

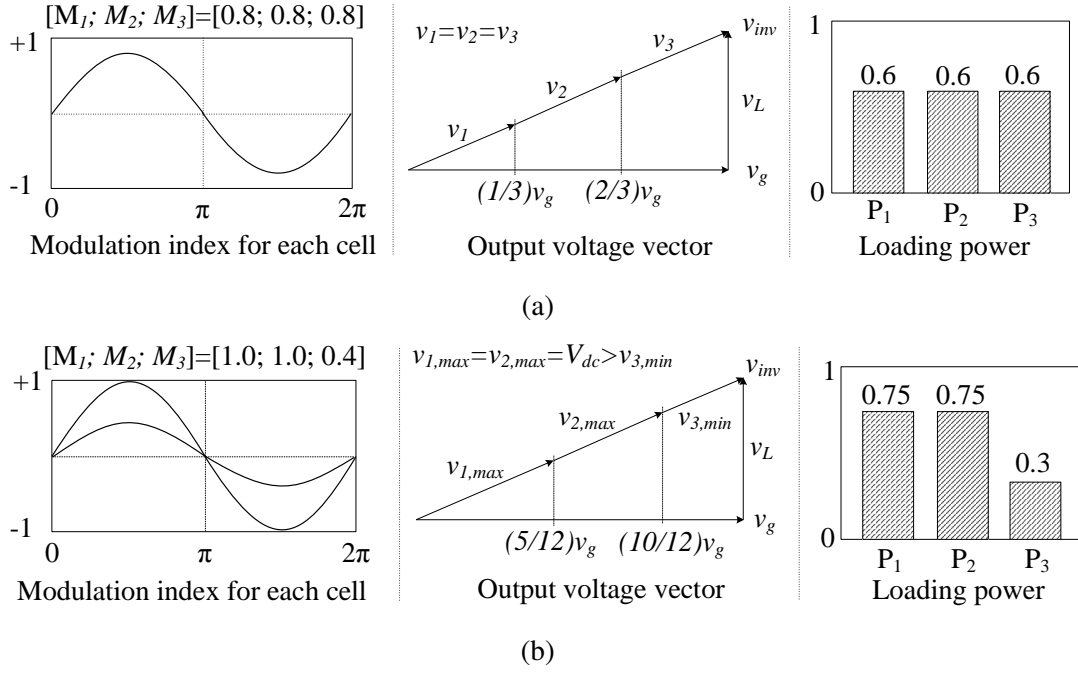


Figure 4.8: Limited power routing capability of the sinusoidal modulation when the modulation index under the balanced condition is 0.8: Modulation index for each cell (left), respective voltage vector (middle) and power distribution (right) under (a) balanced condition and (b) maximum unbalanced condition.

4.2.1 Multi-frequency modulation

A third harmonic voltage is utilized in order to extend the DC-link voltage utilization, which allows the improved power routing capability. In order to maximize the capability, an optimal amplitude of the third harmonic needs to be derived and it is in fact identical to the mathematical derivation for the third harmonic injected modulation in [136]. The modulation signal with the additional third harmonic, m_{ov} , which is for additional loading cells, is expressed in

$$m_{ov} = M_{ov} \cdot \sin(\theta) + k \cdot M_{ov} \cdot \sin(3\theta) \quad (4.14)$$

where M_{ov} is the modulation index for additional loading cells and the maximum modulation index is obtained with $k = 1/6$, leading to the maximum linear modulation index up to $M_{max,ov} = 2/\sqrt{3}$. This enables to increase the maximum loading by 15.5 % approximately. Meanwhile, it is necessary to compensate the third harmonic voltage utilized for the additional loading so as to ensure the sinusoidal voltage in the total output voltage, v_{inv} . This can be accomplished by means of unloading cells, which are modulated with the negative third harmonic voltage as expressed in

$$m_{un} = M_{un} \cdot \sin(\theta) - N \cdot k \cdot M_{ov} \cdot \sin(3\theta) \quad (4.15)$$

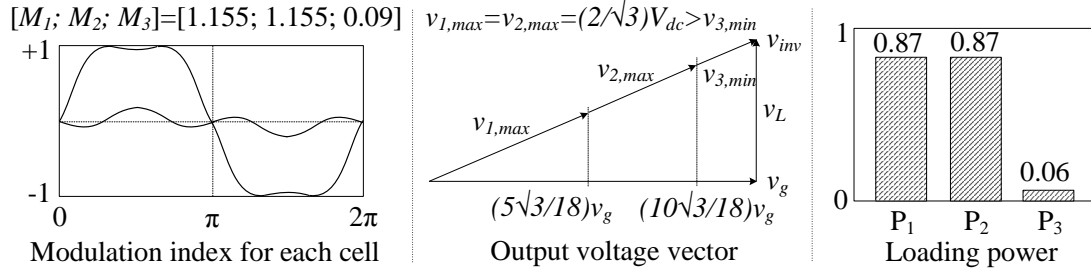


Figure 4.9: Maximum power routing capability of the multi-frequency modulation when the modulation index under the balanced condition is 0.8: Modulation index for each cell (left), respective voltage vector (middle) and power distribution (right).

where M_{un} is the modulation index for the unloading cells and N represents the number of additional loading cells. Consequently, since the CHB cells are connected in series, the total output voltage can be found by the summation of each cell's output voltage as

$$v_{inv} = V_{dc} \cdot [N \cdot M_{ov} + (K - N) \cdot M_{un}] \cdot \sin(\theta) \quad (4.16)$$

where K is the total number of cells and the below condition should be always satisfied in order to maintain the total power.

$$\begin{cases} \text{Condition I: } [N \cdot M_{ov} + (K - N) \cdot M_{un}] = K \cdot M_{bal} \\ \text{Condition II: } M_{un} \leq M_{bal} \leq M_{ov} \end{cases} \quad (4.17)$$

where M_{bal} is the modulation index when the loading is equally distributed (i.e. it is the ratio between the total DC-link voltage and the grid voltage). The multi-frequency modulation is visualized in Fig. 4.9 and remarkably, it can be noticed that the third harmonic voltage is in phase with the fundamental voltage and the maximum loading is improved to 0.87, which is higher by 15.5 % than the sinusoidal modulation (see Fig. 4.8 (a)).

Fig. 4.10 illustrates an arbitrary case in order to demonstrate the operation with the multi-frequency modulation, assuming that one of the DC/DC converters (in path 3) shows far higher degradation than the others. In this scenario, instead of equally loading all cells ($P_1 = P_2 = P_3$) as shown in Fig. 4.10 (a), unloading the power path 3 enables to postpone the time to the failure ($P_1 = P_2 > P_3$). This is demonstrated in Fig. 4.10 (b), where the the third harmonic voltage is internally compensated while processing the fundamental power to the grid.

The power imbalance capability of the proposed method is evaluated compared with the sinusoidal modulation. The available maximum modulation index, M_{max} , is inherently restricted to the modulation method, where it is 1 by the sinusoidal and 1.15 by the multi-frequency. On the other hand, the available minimum modulation index is defined as a function of the maximum modulation index and the total number of cells by

$$M_{min} = K \cdot M_{bal} - N \cdot M_{max}. \quad (4.18)$$

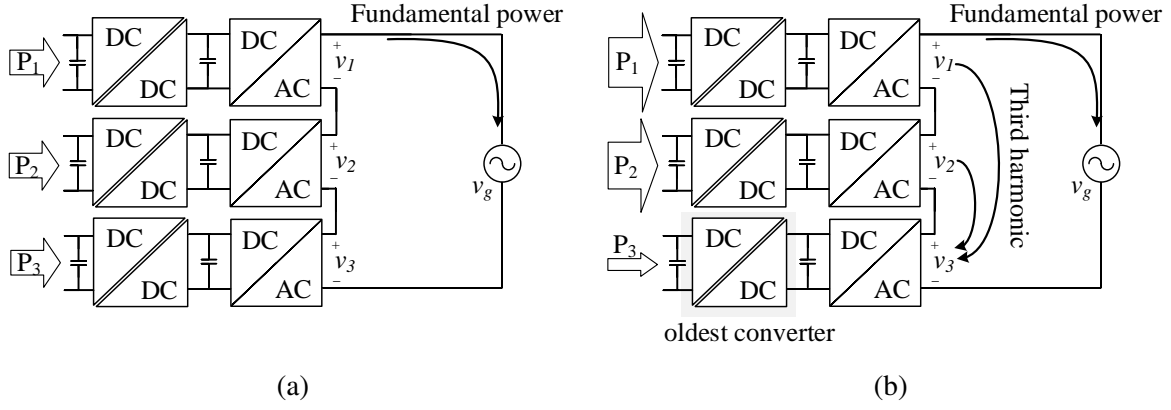


Figure 4.10: Demonstration of the multi-frequency modulation. (a) Balanced loading ($P_1 = P_2 = P_3$) and (b) unbalanced loading ($P_1 = P_2 > P_3$) when the DC/DC converter in the path 3 is oldest as an example.

Based on the above, the available maximum and minimum power loading, which is normalized by the balanced loading, can be found in

$$\begin{cases} P_{max} = \frac{M_{max}}{M_{bal}} \cdot P_{bal}, \\ P_{min} = \frac{M_{min}}{M_{bal}} \cdot P_{bal} = \left(K - N \cdot \frac{M_{max}}{M_{bal}} \right) \cdot P_{bal}. \end{cases} \quad (4.19)$$

The potential of the power routing capability is benchmarked in terms of the maximum and minimum power imbalance. It is shown in Fig. 4.11 as a function of the balanced modulation index, M_{bal} , with the assumption of $K = 3$ and $N = 2$. As decreasing the balanced modulation index, the further maximum loading becomes possible (see Fig. 4.11 (a)) and the minimum loading is reduced (see Fig. 4.11 (b)), and vice versa. The available maximum loading with the multi-frequency is improved by approximately 15 % within the considered modulation index range (0.7-0.9). Hence, it can be concluded that the proposed method explicitly shows the improved performance compared with the sinusoidal method.

Fig. 4.12 further generalizes the power imbalance capability as a function of the number of cells, where the horizontal axis is the number of unloading cells and the vertical one represents their available minimum loading. For both methods, the available minimum loading is increasing with the higher number of unloading cells as the number of additional loading cells is proportionally reduced. Remarkably, focusing on the number of completely unloaded cells, the proposed method can allow more number of the DC/DC converters to be deactivated, keeping the whole system's operation. For example, the maximum 7 cells can be deactivated with the total 23 cells, whereas only 4 cells by the sinusoidal method. This capability shall be one of the most attractive features for a scheduled maintenance, ensuring the power security.

The implementation of the multi-frequency method is achieved with an additional open-loop control nested in the standard current controller as shown in Fig. 4.13. Here, $v_{1,1}$, $v_{2,1}$ and

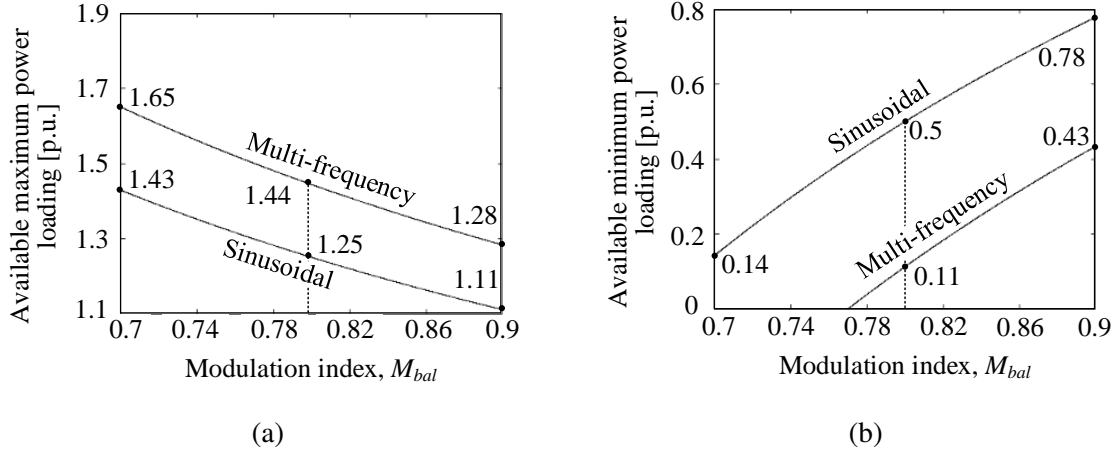


Figure 4.11: Capability of power imbalance as a function of balanced modulation index, M_{bal} : (a) maximum and (b) minimum loading ($K=3$ and $N=2$).

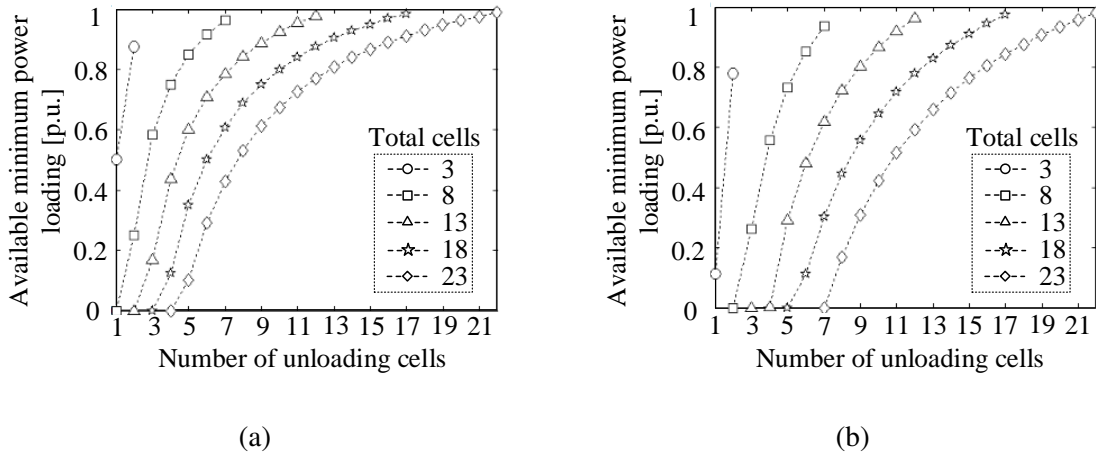


Figure 4.12: Capability of power imbalance as a function of the total number of cells and the number of the unloading cells by (a) sinusoidal and (b) multi-frequency modulation ($M_{bal} = 0.8$).

$v_{3,1}$ are the fundamental component for cell 1, 2 and 3, respectively, and $v_{1,3}$, $v_{2,3}$ and $v_{3,3}$ are the third harmonic component for each cell. The fundamental components are determined with the power reference, P^* , which is fed from the power routing block generating the power reference for each cell, $[P_1; P_2; P_3]$. Based on the power reference, the fundamental modulation index for each cell is obtained in the reference calculation block as

$$M_{x,1} = \frac{M_{bal}}{P_{bal}} \cdot P_x^* \quad (4.20)$$

where the subscription x can be 1, 2 or 3 to represent each cell and P_{bal} is the power under the balanced condition. The third harmonic components are determined by (4.14) and (4.15) for additional loading and unloading cell, respectively. The final voltage of each cell, v_1 , v_2 and v_3 , is obtained by a summation of the fundamental and the respective third harmonics components.

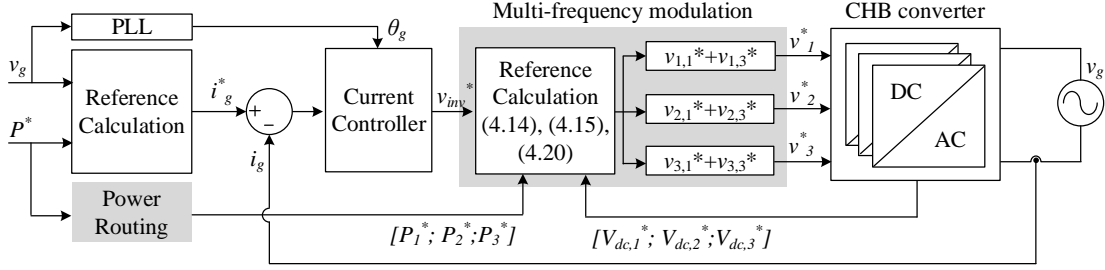


Figure 4.13: Control block diagram including the multi-frequency power routing.

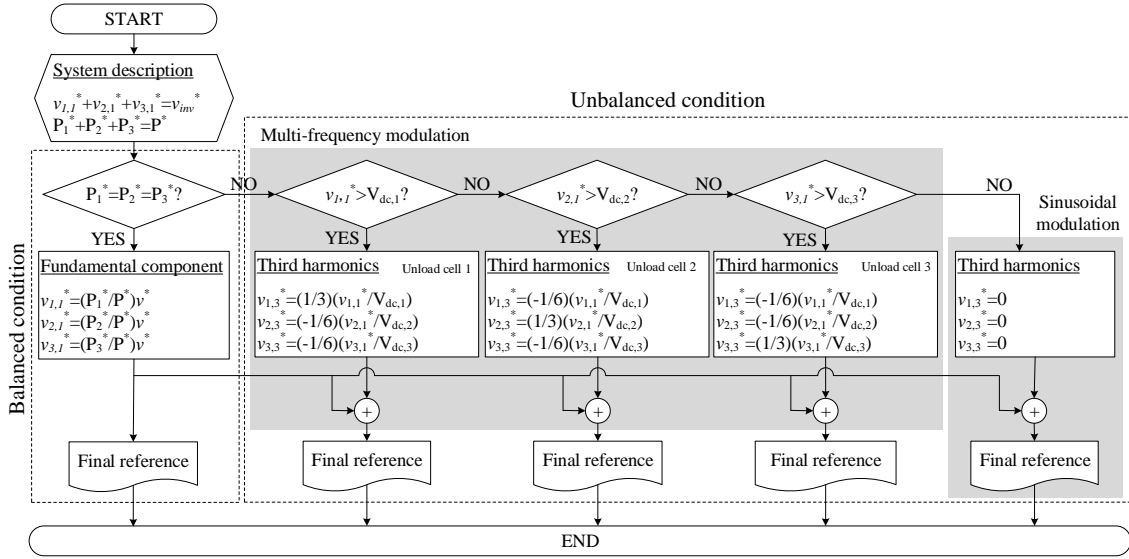


Figure 4.14: Flowchart for the power routing with the multi-frequency modulation, considering one of cells needs to be unloaded.

The flowchart for applying the power routing with the multi-frequency is shown in Fig. 4.14, in which only one cell needs to be unloaded for the sake of simplicity. Once the reference power for each cell is different ($P_1^* \neq P_2^* \neq P_3^*$), the power routing is activated and it is determined whether the multi-frequency method should be applied or not depending on the fundamental components. If the fundamental component for one of cells exceeds than a respective DC-link voltage, the multi-frequency method is activated, otherwise, the sinusoidal method is applied.

The effect of the multi-frequency based power routing on the accumulated damage of the DC/DC converters is demonstrated in Fig. 4.15, where it particularly aims to prevent power fluctuations in path one under a mission profile with rapidly fluctuating power as a case study. A converter designed for an ambient temperature $T_a = 40^\circ\text{C}$ and the maximum junction temperature $T_{j,max} = 90^\circ\text{C}$ under full load, is assumed. The power routing results in a reduced thermal fluctuation on the power semiconductors in that path, while the fluctuations in the other paths are increased. As a result, the damage caused by the thermal cycling is reduced to one fifth for the unloaded path, while the highly loaded paths undergo approximately three times more damage. It needs to be pointed out, that the capability of controlling the stress

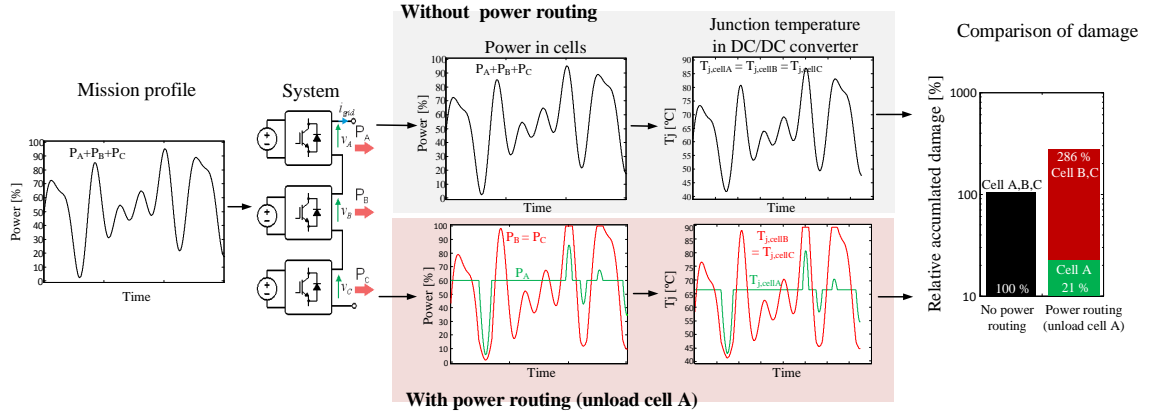


Figure 4.15: Effect of multi-frequency modulation based power routing on the thermal loading and the normed damage caused in the power semiconductors in the DC/DC converters.

depends highly on the system design and the mission profile. With only small variations in the power, the thermal fluctuations can be completely eliminated from cells, while high fluctuations, such as in the presented case study affect all cells.

The generated losses on the DC/DC converters are proportionally affected by amount of the loading power, hence, their thermal stresses can be directly managed by means of the power routing. However, the losses on the CHB cells are independent on the loading power as they are connected in series, meaning that the total current is always shared regardless of the power routing. Hence, it shall be identified the influence of the power routing on the loss distribution of the CHB cells.

Based on the switching and conduction loss models with the sinusoidal modulation, those with the multi-frequency modulation can be derived. In fact, the switching loss model with the multi-frequency modulation is identical with the previous one in (4.7), since the switching losses are independent on the modulation method if it is of continuous modulation. Therefore, the switching loss model for additional loading and unloading cells are identical with (4.7). On the other hand, the conduction losses are closely related to the modulation function, δ . It leads to re-define the modulation function in (4.12) for the multi-frequency and it is expressed in (4.21), assuming that $K=3$ and $N=2$.

$$\begin{cases} \delta_{ov} = \frac{1}{2} \pm \frac{1}{2} \left[M_{ov} \cdot \sin(\theta) + \frac{M_{ov}}{6} \cdot \sin(3\theta) \right], \\ \delta_{un} = \frac{1}{2} \pm \frac{1}{2} \left[M_{un} \cdot \sin(\theta) - \frac{M_{ov}}{3} \cdot \sin(3\theta) \right] \end{cases} \quad (4.21)$$

where δ_{ov} and δ_{un} are for the additional and unloading cell, respectively, the plus/minus signs belong to the IGBT and the diode, respectively. Finally, by substituting (4.21) to (4.12) the conduction loss model with the multi-frequency modulation is found by

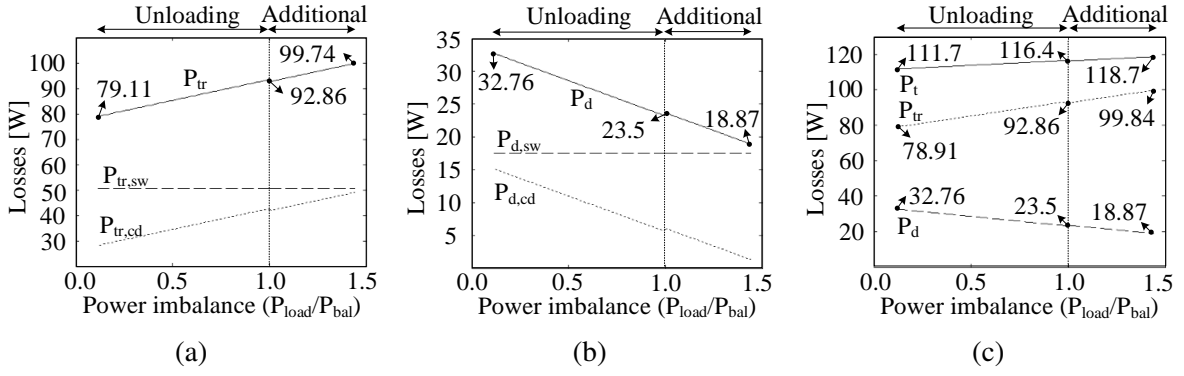


Figure 4.16: Loss distribution as a function of the power imbalance (P_{load}/P_{bal}): (a) IGBT, (b) diode and (c) total losses (Condition: Table 4.1).

$$\begin{cases} P_{ov,cd} = \frac{1}{2\pi} \int_0^\pi \delta_{ov} \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta, \\ P_{un,cd} = \frac{1}{2\pi} \int_0^\pi \delta_{un} \cdot I_{pk} \sin(\theta) \cdot (V_{f0} + I_c \cdot r_{d0}) d\theta \end{cases} \quad (4.22)$$

where $P_{ov,cd}$ and $P_{un,cd}$ are for additional and unloading cell, respectively.

The loss distribution in accordance with the power imbalance is illustrated in Fig. 4.16, where the subscript sw and cd are the switching and conduction losses, and the subscript tr , d and t represent the IGBT, diode and total losses, respectively. The operation condition for this analysis is described in Table 4.1. As mentioned before, the switching losses of both IGBT and diode are independent on the amount of the power loading and it is validated in Fig. 4.16 (a) and (b) (i.e. $P_{tr,sw}$ and $P_{d,sw}$ are constant regardless of the power loading), whereas their conduction losses are highly dependent on the power imbalance. As shown in Fig. 4.16 (a) the IGBT losses are proportional to the loading power, whereas the diode losses are inverse proportional to that as shown in Fig. 4.16 (b). Therefore, the summation of the IGBT and diode losses, P_t , is hardly affected by the loading power (see Fig. 4.16 (c)). In this case, the variation of the total losses is from -4.5 % to 2.3 %, while that of IGBT and diode is from -14.8 % to 7.4 % and from -46.2 % to 90.1 %, respectively.

As a consequence, the power routing has not only an impact on the stress distribution of the DC/DC converters but also the CHB cells, especially, the additional loading will accelerate the degradation of IGBTs in the respective CHB cells as well as the respective DC/DC converters. Thus, the degradation of both the DC/DC converters and the CHB cells cannot be considered at a same time. In conclusion, the targets of stress reduction for the DC/DC converter and CHB cell can either be complementary or lead to a conflict of objectives.

As illustrated in Fig. 4.10, the third harmonic voltages are internally compensated them-

Table 4.1: Operation condition for the analysis of the proposed methods.

V_{dc}	I_g	f_{sw}	M_{bal}	K	N	PF	T_j
600 V	60 A	20 kHz	0.8	3	2	1	125°C

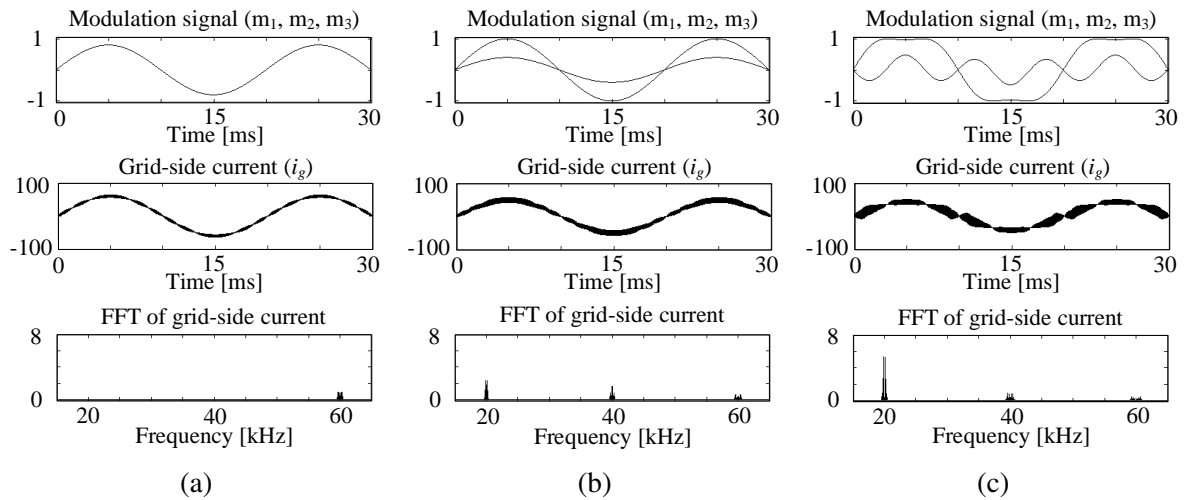


Figure 4.17: Influence of the power routing on grid-side current: modulation signals (top), grid-side current (middle) and its frequency spectrum (bottom) under (a) balanced condition and unbalanced condition with (b) sinusoidal and (c) multi-frequency modulation (Condition: Table 4.1).

selves within the CHB converter cells (i.e. $v_{1,3} + v_{2,3} + v_{3,3} = 0$). However, the high order harmonics caused by switching behavior is varied and thus, affecting the Total Harmonic Distortion (THD) of the grid-side current. This is demonstrated in Fig. 4.17. The balanced loading condition is shown in Fig. 4.17 (a) and only the sixth-order carrier harmonic component exists in the current spectrum, which is the most attractive advantage of the PSPWM under the balanced operation condition (i.e. equal DC-link voltage and same modulation signal for each cell). On the other hand, the imbalance loading by the sinusoidal modulation is shown in Fig. 4.17 (b), where the envelope of the current ripple is wider compared to the first case due to the existence of the second- and the fourth-order carrier harmonics. The different modulation signal for the power routing causes these harmonics. Further, the multi-frequency method is responsible for the further increased current ripple with the increased second-order carrier harmonics as shown in Fig. 4.17 (c).

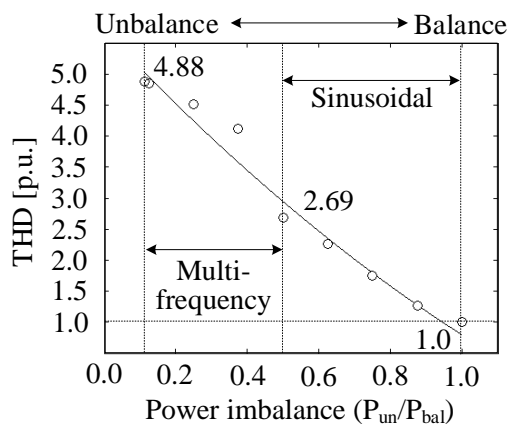


Figure 4.18: Normalized THD of the grid-side current with the multi-frequency method as a function of the power imbalance (Condition: Table 4.1).

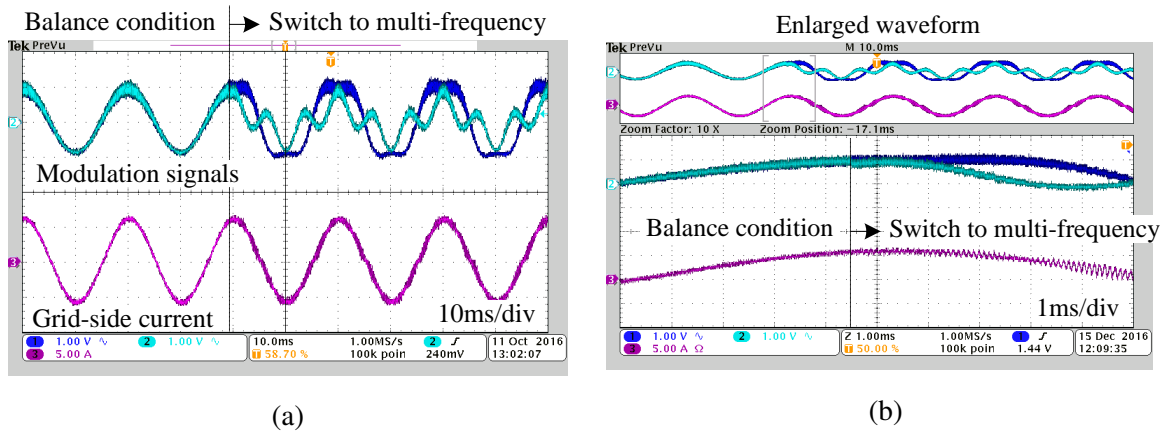


Figure 4.19: Dynamic response for the activation of the multi-frequency modulation: (a) step change from balanced to the maximum unbalanced and (b) enlarged waveform ($M_{bal}=0.9$, $K=3$ and $N=2$).

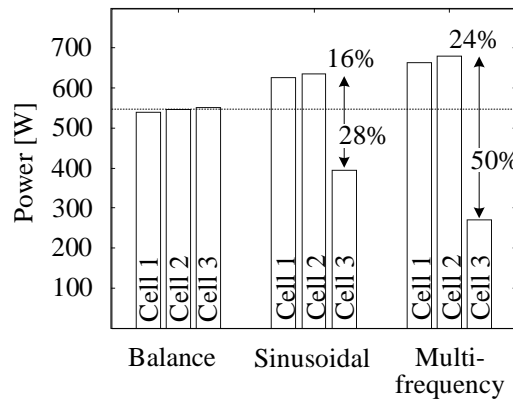


Figure 4.20: Power measurement of each path under balanced and unbalanced by the sinusoidal and the multi-frequency ($M_{bal}=0.9$, $K=3$ and $N=2$).

The dependence of the THD and the power imbalance is identified in Fig. 4.18, where the THD is normalized by that in the balanced condition. As increasing the power imbalance, the THD is getting worse and it is 4.88 times higher at the worst case (at the maximum imbalance). As a conclusion, the THD performance decreases with the imbalance due to the increased second- and fourth-order carrier harmonics, even though the third-order harmonic component is completely compensated among the cells.

The electric measures of the multi-frequency power routing are demonstrated and its capability in terms of the imbalance loading is validated with a developed laboratory prototype shown in appendix 9.1.1, where $M_{bal}=0.9$, $K=3$ and $N=2$ are chosen for the following experimental results.

The transition between the sinusoidal and multi-frequency modulation is identified in Fig. 4.19. It is shown that the transition is seamlessly conducted without any special technique under a stepwise change, which is remarkable feature allowing the multi-frequency method to be simply accomplished by the open-loop as aforementioned.

For the validation of the power routing capability, the power of each path is measured as

shown in Fig. 4.20. By the identical modulation index, the power is equally processed among cells whereas the sinusoidal method enables to unload cell by 28 %. Further, the multi-frequency method can remarkably improve the power imbalance capability, leading to the minimum unloading power by 50 %.

4.2.2 Discontinuous modulation

The discontinuous modulation techniques have been usually employed in order to improve the energy conversion efficiency by reducing the switching losses. The reduced switching losses in the discontinuous modulation can be accomplished by clamping output voltage of a converter at either a positive or negative DC-link voltage with the *third-order harmonics* component [137, 138].

In this section, a novel discontinuous modulation scheme is proposed with the purpose of the power routing in the modular converter, remarkably reducing the losses of CHB converter. The proposed method features two variants of modulation signal:

- Clamped modulation, m_c , for additional loading (Fig. 4.21 (a))
- Non-clamped modulation, m_{nc} , for unloading (Fig. 4.21 (b))

Similar to the conventional methods, the proposed modulation signals can be obtained by a summation of the fundamental component, m_f , and offset component, m_{off} , but remarkably, the *first-order harmonic* is used as the offset component. This is the key feature of the proposed method, which enables to manipulate the processed power of each path depending on the clamping angle, φ . Furthermore, since the added offset components are internally compensated themselves in the CHB converter like the multi-frequency method (refer to Fig. 4.10), the offset components do not appear completely in the total output voltage.

Since the degree of the power imbalance is determined by the clamping angle, it needs to analyze a relation between them. The two modulation signals are mathematically expressed. First, the clamped modulation can be divided and expressed in accordance with three regions by

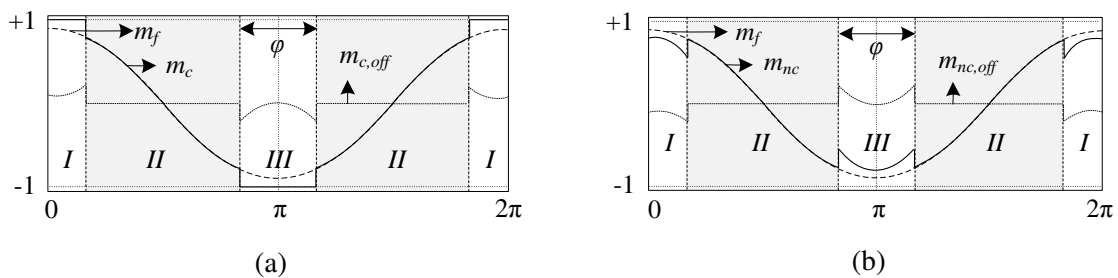


Figure 4.21: The proposed discontinuous modulation strategy, which has two variants: (a) clamped modulation, m_c , for additional loading and (b) non-clamped modulation, m_{nc} , for unloading.

$$m_c = \begin{cases} M_c \cdot \cos(\theta) + m_{c,off} = \pm 1 & \text{(Region I \& III)} \\ M_c \cdot \cos(\theta) & \text{(Region II)} \end{cases} \quad (4.23)$$

where

$$m_{c,off} = \pm 1 - M_c \cdot \cos(\theta) \quad (4.24)$$

where M_c is the modulation index for clamped cells, θ is the angular frequency of the fundamental component and the plus/minus signs belong to the region I and III, respectively. In the same manner, the clamped modulation is described by

$$m_{nc} = \begin{cases} M_{nc} \cdot \cos(\theta) + m_{nc,off} \\ = [M_{nc} + \frac{N}{K-N} \cdot M_c] \cdot \cos(\theta) \mp \frac{N}{K-N} & \text{(Region I \& III)} \\ M_{nc} \cdot \cos(\theta) & \text{(Region II)} \end{cases} \quad (4.25)$$

where

$$m_{nc,off} = \frac{N}{K-N} \cdot (M_c \cdot \cos(\theta) \mp 1) \quad (4.26)$$

where M_{nc} represents the modulation index for non-clamped cells, K is the number of the total cells, N is the number of the non-clamped cells and minus/plus signs are for the region I and III, respectively. Here, it is worth noticing that the offset components for clamping and non-clamping modulation must have an identical clamping angle and a summation of their amplitude must be zero, so that they can be completely compensated themselves.

As it can be expected from Fig. 4.21, the modulation signals are expressed with various harmonics components due to the discontinuous regions. However, only the fundamental frequency component is used to transfer power between AC and DC side and therefore the fundamental component of the modulation signals needs to be derived for the power routing capability analysis. Since the modulation signals are a periodic function, they can be expressed in the Fourier series and the fundamental component is derived by calculating the first-order coefficients expressed in (4.27).

$$\begin{cases} \alpha_1 = \frac{1}{\pi} \int_{\theta_1}^{\theta_2} f(\theta) \cos(\theta) d\theta \\ \beta_1 = \frac{1}{\pi} \int_{\theta_1}^{\theta_2} f(\theta) \sin(\theta) d\theta \end{cases} \quad (4.27)$$

where α_1 and β_1 are the Fourier coefficients for the fundamental component, θ is the angular frequency of the fundamental component and $f(\theta)$ is the target signal function. Once the coefficients are obtained, the fundamental component of the target signal v_f can be found as

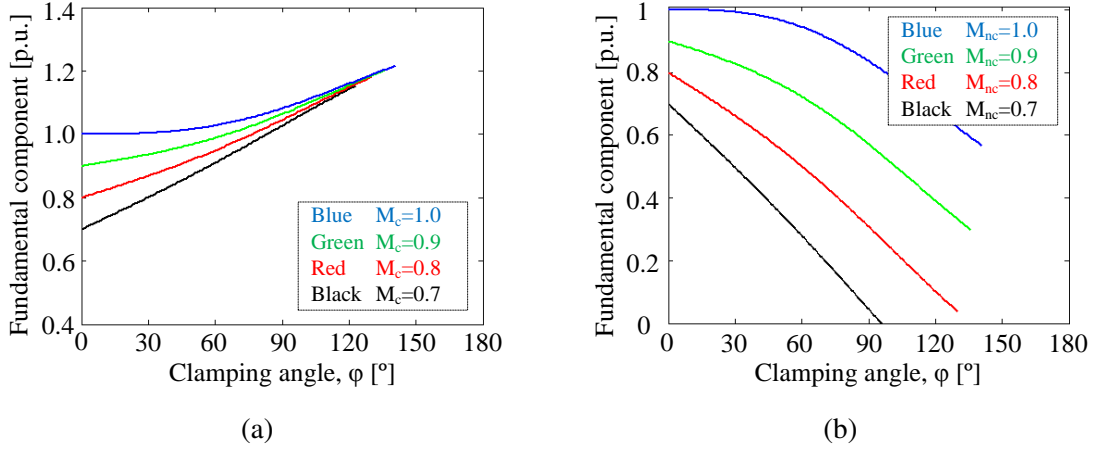


Figure 4.22: The fundamental component as a function of the clamping angle: (a) $v_{f,c}$ and (b) $v_{f,nc}$, where the hatched region is prohibited due to the over-modulation ($M_c=M_{nc}$, $K=3$ and $N=2$).

$$v_f = \sqrt{\alpha_1^2 + \beta_1^2}. \quad (4.28)$$

Based on the above equations from (4.24) to (4.28), the fundamental component of each modulation signal as a function of the clamping angle is finally derived by

$$\begin{cases} v_{f,c}(\varphi) = \frac{1}{\pi} \cdot \left[M_c \cdot (\pi - \varphi - \sin(\varphi)) + 4 \cdot \sin\left(\frac{\varphi}{2}\right) \right] \\ v_{f,nc}(\varphi) = \frac{1}{\pi} \cdot \left(\frac{N}{K-N} \right) \cdot M_c \cdot (\varphi + \sin(\varphi)) + M_{nc} - \frac{4}{\pi} \cdot \left(\frac{N}{K-N} \right) \cdot \sin\left(\frac{\varphi}{2}\right) \end{cases} \quad (4.29)$$

where $v_{f,c}$ and $v_{f,nc}$ represent the fundamental component of the clamped and non-clamped modulation, respectively. This is visualized in Fig. 4.22, showing the influence of the clamping angle on the fundamental components, $v_{f,c}$ and $v_{f,nc}$ in Fig. 4.22 (a) and (b), respectively. Even though the clamping angle can be ranged from 0° to 180° , it is limited due to the over-modulation of the non-clamped cell and this is indicated in hatched region (the constraint due to over-modulation will be discussed in detail). Therefore, the maximum clamping angle is differently determined in accordance with the modulation index and consequently, the available maximum and minimum fundamental as shown in Fig. 4.22.

- Case 1: $M_c=M_{nc}=1 \rightarrow \max. v_{f,c}=1.22, \min. v_{f,nc}=0.56$ ($\max.\varphi=141.1^\circ$)
- Case 2: $M_c=M_{nc}=0.9 \rightarrow \max. v_{f,c}=1.205, \min. v_{f,nc}=0.29$ ($\max.\varphi=136.5^\circ$)
- Case 3: $M_c=M_{nc}=0.8 \rightarrow \max. v_{f,c}=1.185, \min. v_{f,nc}=0.03$ ($\max.\varphi=130.8^\circ$)
- Case 4: $M_c=M_{nc}=0.7 \rightarrow \max. v_{f,c}=1.154, \min. v_{f,nc}=0.0$ ($\max.\varphi=123.1^\circ$)

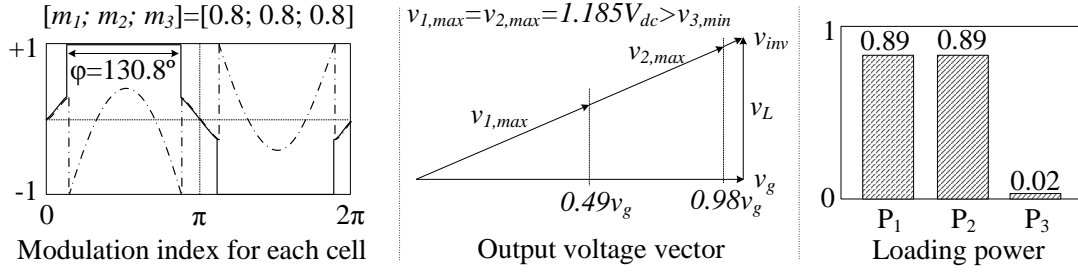


Figure 4.23: Power routing capability of the discontinuous modulation when the clamping angle is 130.8° and all of modulation index is equal to 0.8: Modulation signal for each cell (left), respective voltage vector (middle) and power distribution (right).

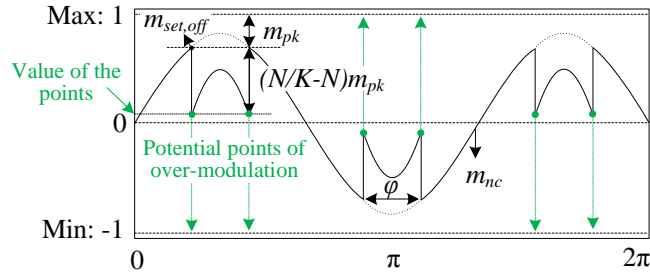


Figure 4.24: Constraint of the proposed discontinuous modulation due to a possible over-modulation of the non-clamped modulation, m_{nc} .

As shown in Fig. 4.22 (b), the non-clamped cell can be completely unloaded in case of the modulation index of 0.7. This capability of completely unloading shall be beneficial in case one of the DC/DC converters needs to be replaced due to a malfunction.

The discontinuous modulation is demonstrated in Fig. 4.23, in which the modulation signal (left), the respective voltage vector (middle) and power distribution (right) for each cell when all of modulation index is equal to 0.8 and the clamping angle is 130.8° . Remarkably, the minimum power loading is extended up to 0.02 compared with the 0.06 by the multi-frequency method under the identical condition.

As mentioned before, the constraint due to the over-modulation needs to be discussed in order to avoid the converter to be operated in a non-linear region. Assuming the CHB converter of which total number of cells is K and N cells are additionally loaded, the modulation signals can be expressed by a summation of the fundamental and the offset components as

$$\begin{cases} m_{c(i)} = m_f + m_{off,c} & (i = 1, 2, \dots, N) \\ m_{nc(j)} = m_f + \left(\frac{N}{K-N}\right) m_{off,nc} \\ \quad = m_f - \left(\frac{N}{K-N}\right) m_{off,c} & (j = 1, 2, \dots, K-N) \end{cases} \quad (4.30)$$

where m_c and m_{nc} are the modulation signals for additional loading i -th cell and unloading

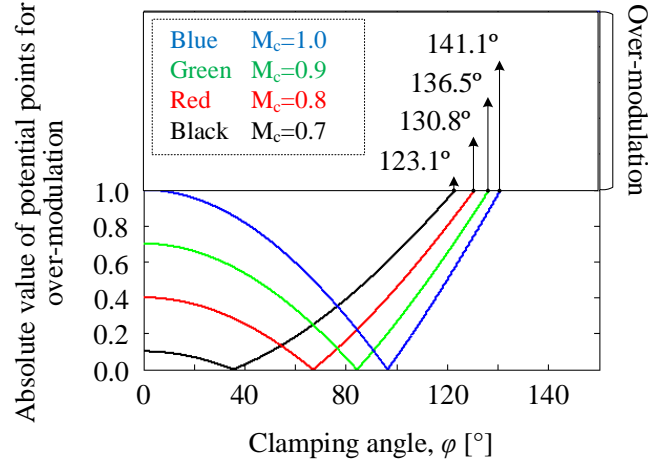


Figure 4.25: Value of the potential point for the over-modulation in Fig. 4.24 as a function of the clamping angle and the modulation index ($M_c=M_{nc}$, $K=3$ and $N=2$).

j -th cell, respectively. Among the two modulation signals in (4.30), only the m_{nc} causes the over-modulation due to the factor $N/(K-N)$. This is exemplified in Fig. 4.24, in which the potential points of the over-modulation are indicated and they are dependent on the clamping angle and the factor $N/(K-N)$. Namely, the points are being pushed towards the boundary as increasing the clamping angle and the number of the additional loading cells. Therefore, the condition, which the points must be within the boundary ± 1 , needs to be satisfied for the linear modulation and it is expressed in

$$\begin{aligned} & \left| m_{set,off} - \left(\frac{N}{K-N} \right) (1 - m_{set,off}) \right| \leq 1 \\ \Rightarrow & \left| \left(\frac{N}{K-N} \right) - \left(\frac{K}{K-N} \right) \cdot M_c \cdot \cos\left(\frac{\varphi}{2}\right) \right| \leq 1 \end{aligned} \quad (4.31)$$

where

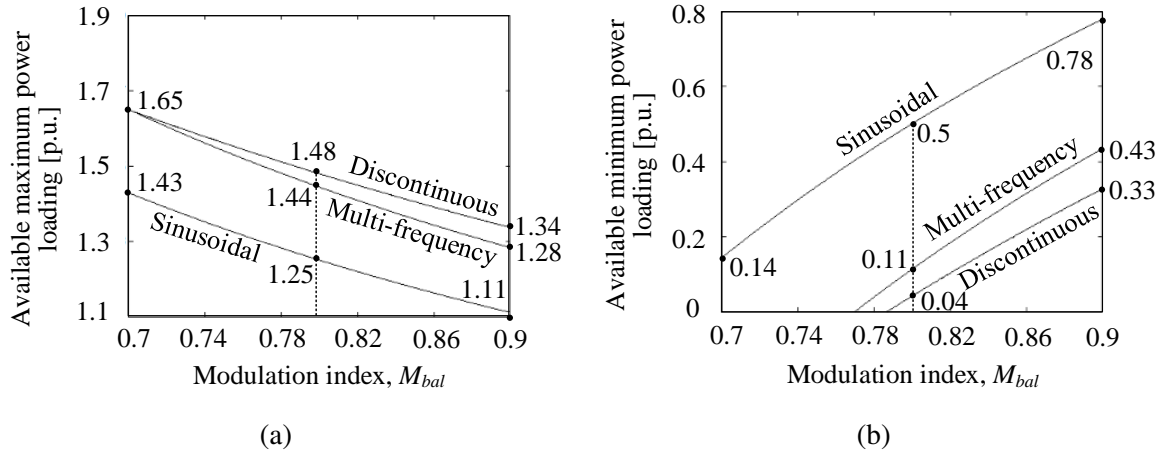
$$m_{set,off} = M_c \cdot \cos\left(\frac{\varphi}{2}\right). \quad (4.32)$$

Based on (4.31), the value of the potential points is illustrated in Fig. 4.25 as a function of the clamping angle and the modulation index. As increasing the clamping angle, the value of the potential points reaches to zero and then towards to the opposite boundary.

The maximum power routing capability in dependence of the modulation index is summarized in Table 4.2, considering the constraint. The higher nominal modulation indexes allow a higher maximum clamping angle, resulting in a higher fundamental component, $v_{f,max}$. However, it should be pointed out that the power imbalance capability is improved with the smaller modulation index as shown by the ratio between the modulation index and the maximum fundamental component, $v_{f,max}/M_c$. As an example, the maximum loading is 165 %

Table 4.2: The maximum power routing capability under different modulation index ($K=3$ and $N=1$).

$M_c = M_{nc}$	φ_{max} [°]	$v_{f,max}$ [p.u.]	$v_{f,min}$ [p.u.]	$v_{f,max}/M_c$ [p.u.]
0.7	123.1	1.154	0.00	1.65
0.8	130.8	1.185	0.03	1.48
0.9	136.5	1.205	0.29	1.34
1.0	141.1	1.220	0.56	1.22

Figure 4.26: Capability of power imbalance as a function of modulation index: (a) maximum and (b) minimum loading ($K=3$ and $N=2$).

when the modulation index is 0.7, whereas it is 122 % with the 1.0 modulation index. Furthermore, the non-clamped cell can be completely unloaded in case of the modulation index of 0.7 ($v_{f,min} = 0$). This complete unloading power is beneficial, because it enables to keep the whole system operational with a lower number of cells, e.g. in case some of DC/DC cells are failed and under maintenance.

Fig. 4.26 shows the potential of the power routing capability as a function of the modulation index, where the maximum loading is in Fig. 4.26 (a) and the minimum loading is in 4.26 (b). Compared with the multi-frequency modulation, the capability is further improved, especially, when the modulation index is high. The capability for the additional loading is 4.6 % higher at the modulation index of 0.9.

Finally, the potential for the unloading power capability is generalized as a function of the total number of cells and the number of the unloading cells in Fig. 4.27. Compared with the multi-frequency method in Fig. 4.12 (b), the number of cells completely unloaded is same apart from only the case of 13 total number of cells, where the number of cells that are completely unloaded is 4 instead of 3 by the multi-frequency method.

The implementation of the discontinuous method is straightforward by realizing it with an additional open-loop control nested in the standard current controller as shown in Fig. 4.28. The clamping angle of the offset components, $m_{1,off}$, $m_{2,off}$ and $m_{3,off}$, is determined with the power reference for each cell, $[P_1; P_2; P_3]$, which are fed from the power routing block,

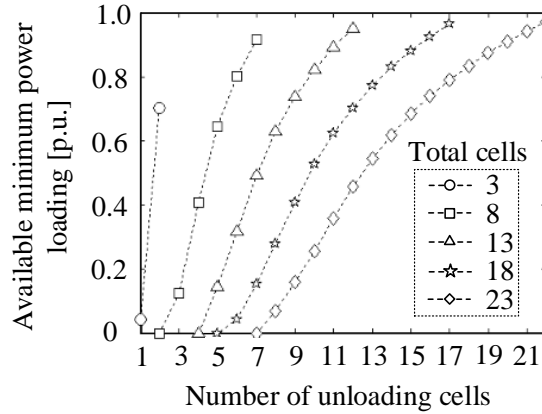


Figure 4.27: Potential for the unloading power capability as a function of the total number of cells and the number of the unloading cells by the discontinuous modulation ($M_c=M_{nc}=0.8$).

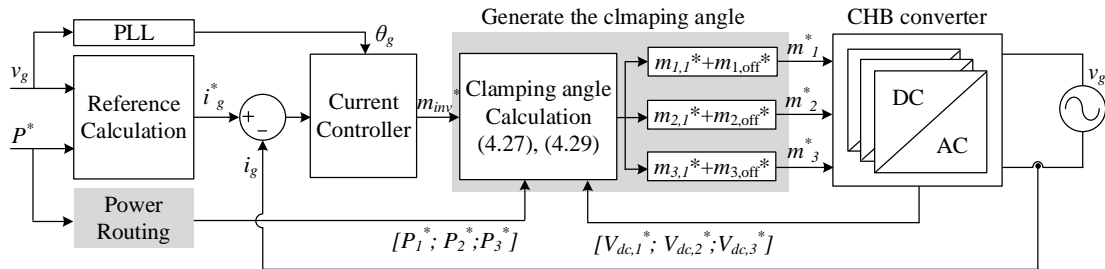


Figure 4.28: Control block diagram including the discontinuous modulation based power routing.

while the fundamental modulation index, $m_{1,1}$, $m_{1,2}$ and $m_{1,3}$, are from the current controller and all of them is equal to $m_{inv}/3$. The final reference for each cell, m_1 , m_2 and m_3 , which is calculated by a summation of the fundamental and the offset components, is fed to a respective cell.

Fig. 4.29 illustrates the flowchart for the discontinuous modulation based power routing, assuming that only one cell is unloaded among total three cells for a simple explanation. The fundamental component for each cell is always identical (i.e. $m_{1,1}=m_{2,1}=m_{3,1}$) and the proper clamping angle is calculated for a targeted power imbalance, also considering the maximum clamping angle to avoid the over-modulation. In case of $\varphi \leq \varphi_{max}$, the offset component is generated with the φ , otherwise, it is limited to φ_{max} . Finally, the additional loading cells are modulation with the clamped modulation and the unloading cell is with the non-clamped modulation.

As presented in the previous section, the power routing affects not only the stress of the DC/DC converters but also that of the CHB converter. Hence, the loss distribution with the discontinuous modulation also needs to be identified. First, contrary to the multi-frequency method, the switching losses are varied with the discontinuous modulation and the switching energy is expressed in

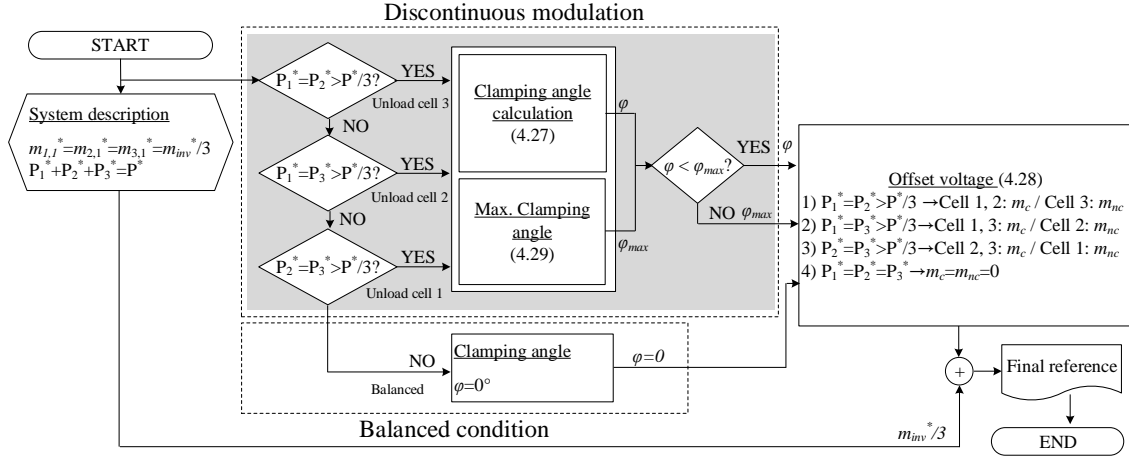


Figure 4.29: Flowchart for the power routing with the discontinuous modulation, considering one of cells needs to be unloaded ($K=3$ and $N=2$).

$$\left\{ \begin{array}{l} E_{ov,sw} = \frac{V_{dc}}{V_{base}} \cdot \frac{1}{2\pi} \left[\int_{\varphi/2}^{\pi-\varphi/2} (a \cdot (I_{pk} \cdot \sin(\theta))^2 + b \cdot (I_{pk} \cdot \sin(\theta)) + c) d\theta \right. \\ \quad \left. + \int_{(\pi+\varphi/2)}^{2\pi-\varphi/2} (a \cdot (I_{pk} \cdot \sin(\theta))^2 + b \cdot (I_{pk} \cdot \sin(\theta)) + c) d\theta \right], \quad (4.33) \\ E_{un,sw} = \frac{V_{dc}}{V_{base}} \cdot \frac{1}{2\pi} \int_0^{\pi} (a \cdot (I_{pk} \cdot \sin(\theta))^2 + b \cdot (I_{pk} \cdot \sin(\theta)) + c) d\theta. \end{array} \right.$$

Here, $E_{ov,sw}$ represents the switching energy of the additional loading cell and $E_{un,sw}$ is the switching energy of the unloading cell. For the additional loading cell, the switching energy is only generated during the outside of the clamping region, $[\varphi/2; \pi - \varphi/2]$ and $[\pi + \varphi/2; 2\pi - \varphi/2]$, since there is no switching behavior during the clamping region. In fact, for the unloading cell the switching energy is identical with that with the sinusoidal modulation. Consequently, it can be expected that the switching losses for the unloading cell is constant, whereas that for the additional loading cell is varied with the clamping angle.

To derive the conduction loss model, the modulation function for the discontinuous modulation is defined in

$$\left\{ \begin{array}{l} \delta = \frac{1}{2} \pm \frac{1}{2} \cdot M \cdot \sin(\theta) \\ \delta_{ov} = 1 \\ \delta_{un} = \frac{1}{2} \pm \frac{1}{2} \left[\left(1 + \frac{N}{K-N} \right) \cdot M \cdot \sin(\theta) - \frac{N}{K-N} \right] \end{array} \right. \quad (4.34)$$

where δ is for the outside of clamping angle, $[\varphi/2; \pi - \varphi/2]$ and $[\pi + \varphi/2; 2\pi - \varphi/2]$, δ_{ov} and δ_{un} are respectively for the clamped region of the clamped and non-clamped modulation, $[0; \varphi/2]$, $[\pi - \varphi/2; \pi + \varphi/2]$ and $[2\pi - \varphi/2; 2\pi]$, and plus/minus belongs to IGBT and

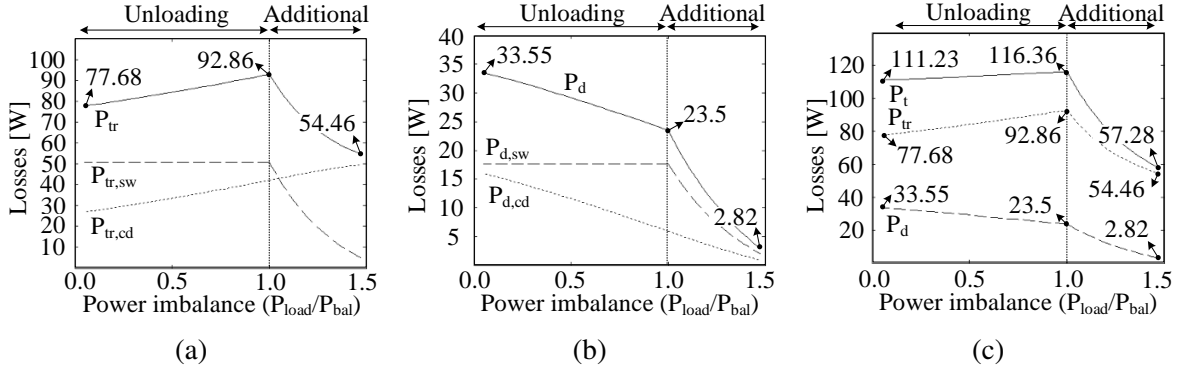


Figure 4.30: Loss distribution as a function of the power imbalance (P_{load}/P_{bal}): (a) IGBT, (b) diode and (c) total losses (Condition: Table 4.1).

diode, respectively. Finally, by substituting (4.34) to (4.12), the conduction loss model with the discontinuous modulation is derived as

$$\left\{ \begin{array}{l}
 P_{ov,cd} = \frac{1}{2\pi} \left[\int_0^{\varphi/2} \delta_{ov} \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \right. \\
 \quad + \int_{\varphi/2}^{\pi-\varphi/2} \delta \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \\
 \quad - \int_{\pi-\varphi/2}^{\pi+\varphi/2} \delta_{ov} \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \\
 \quad + \int_{\pi+\varphi/2}^{2\pi-\varphi/2} \delta \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \\
 \quad \left. + \int_{2\pi-\varphi/2}^{2\pi} \delta_{ov} \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \right] \\
 P_{un,cd} = \frac{1}{2\pi} \left[\int_0^{\varphi/2} \delta_{un} \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \right. \\
 \quad + \int_{\varphi/2}^{\pi-\varphi/2} \delta \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \\
 \quad + \int_{\pi-\varphi/2}^{\pi+\varphi/2} \delta_{un} \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \\
 \quad + \int_{\pi+\varphi/2}^{2\pi-\varphi/2} \delta \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \\
 \quad \left. + \int_{2\pi-\varphi/2}^{2\pi} \delta_{un} \cdot I_{pk} \sin(\theta) \cdot (V_{ce0} + I_c \cdot r_{tr0}) d\theta \right]
 \end{array} \right. \quad (4.35)$$

where $P_{ov,cd}$ and $P_{un,cd}$ are the conduction losses for the additional and unloading cell, respectively, and it can be noticed that both are affected by the clamping angle.

By using (4.33) and (4.35), the loss distribution as a function of the power imbalance is identified in Fig. 4.30 (a), (b) and (c) for the IGBT, the diode and the total losses, respectively,

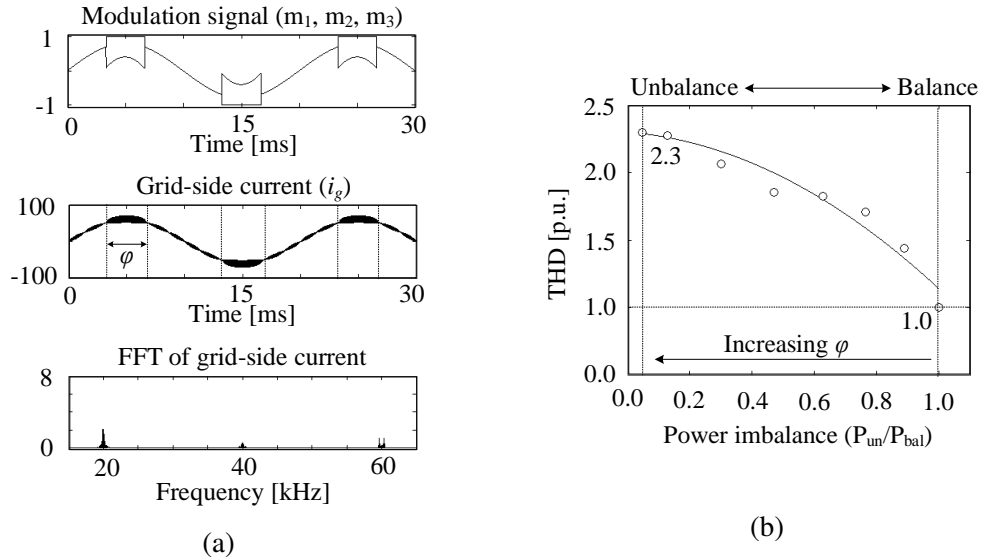


Figure 4.31: (a) Influence of the discontinuous modulation on grid-side current: modulation signals (top), grid-side current (middle) and its frequency spectrum (bottom) and (b) Normalized THD of the grid-side current with the discontinuous method as a function of the power imbalance (Condition: Table 4.1).

under the operation condition in Table 4.1. For IGBT shown in Fig. 4.30 (a), its switching losses, $P_{tr,sw}$, are constant for the unloading cell (by the non-clamped signal), whereas that is decreasing as increasing the loading power (by the clamped signal). The conduction losses, $P_{tr,cd}$, are proportional to the loading power and consequently, the total losses of IGBT, P_{tr} are decreased with the power imbalance regardless of additional and unloading power. As shown in Fig. 4.30 (b), the conduction losses of diode, $P_{d,cd}$, are inversely proportional to the power loading and the trend of the switching losses is same with that of IGBT. Hence, the total losses of diode, P_d are decreased with the additional loading, whereas that is increased as the loading power is decreasing. Finally, the total losses, P_t are shown in Fig. 4.30 (c) and it is significantly reduced with the additional loading while it is slightly decreasing with the unloading. This feature is attractive for the CHB converter's reliability as its stress can be reduced while the power routing is performed for the DC/DC converters. In addition, the reduced losses allow a higher energy efficiency than the previous modulations (sinusoidal and multi-frequency).

The offset components are internally compensated so that the total output voltage does not have the offset components. However, similar to the multi-frequency method, since the modulation signal for each cell is different, the second- and fourth-order carrier harmonics appear in the output voltage, resulting with a lower THD performance. This is demonstrated in Fig. 4.31 (a), showing the modulation signal for each cell, the grid-side current and its frequency spectrum. The THD as a function of the degree of the power imbalance is identified in Fig. 4.31 (b) and the performance is decreasing as the higher power imbalance, namely as increasing the clamping angle. With the maximum clamping angle of 130° , the worst THD is 2.3 times higher than that of the balanced case. This is approximately 2 times better performance, compared to the result of the multi-frequency method in Fig. 4.18.

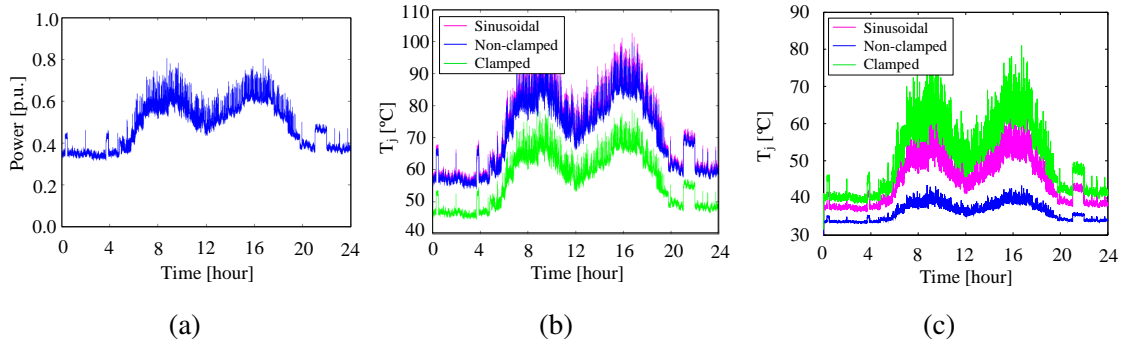


Figure 4.32: (a) One day mission profile and junction temperature profile of (b) a CHB cell and (c) a DC/DC converter with the clamping angle of 60° ($K = 3$ and $N = 2$).

The impact on the lifetime of both CHB and DC/DC converters is analyzed under an arbitrary mission profile for a day as shown in Fig. 4.32 (a). Considering the mission profile, the estimated junction temperature for power semiconductors in a CHB cell is illustrated in Fig. 4.32 (b) by the sinusoidal modulation and the clamped and non-clamped modulation with a fixed clamping angle of 60° . Here, it is assumed that the ambient temperature is constant at 25°C and the designed maximum junction temperature is 110°C . With the sinusoidal modulation, the maximum junction temperature reaches up to 102.8°C , whereas that of the non-clamped and clamped modulation lies around 99.8°C and 78.7°C , respectively. Remarkably, the discontinuous modulation enables to reduce the junction temperature of both non-clamped and clamped cells. On the other hand, the case for the DC/DC converters is depicted in Fig. 4.32 (c). The maximum junction temperature with the sinusoidal modulation lies at 65.4°C , whereas that of the additional loading and unloading converter is 82°C and 43.5°C , respectively.

Fig. 4.33 (a) and (b) shows the normalized accumulated damage as a function of the clamping angle for CHB and DC/DC converter, respectively, considering the mission profile. As shown in Fig. 4.33 (a) for the CHB cells, both clamped and non-clamped modulation allow the reduced damage, especially, with the 60° clamping angle, more than 90% damage

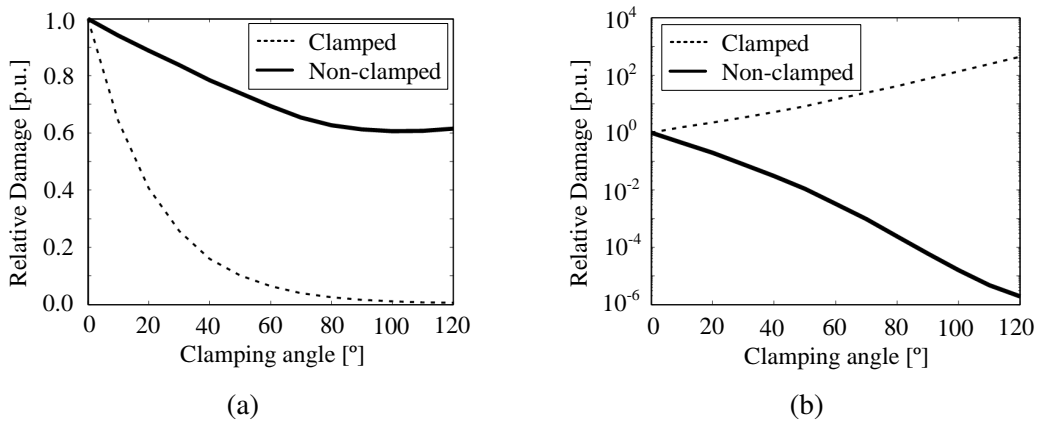


Figure 4.33: Estimated damage of (a) CHB and (b) DC/DC converters, considering the mission profile in Fig. 4.32 (a) ($K = 3$ and $N = 2$).

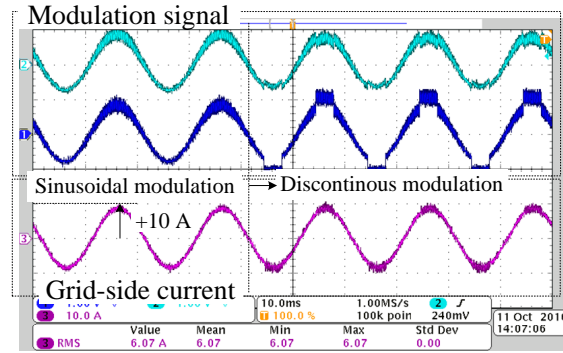


Figure 4.34: Dynamic response for the activation of the discontinuous modulation: from the balanced condition to the unbalanced condition with $\varphi=60^\circ$.

reduction is obtained in the clamped CHB cell and about 30 % damage reduction in the non-clamped cell. On the other hand, the variation in the accumulated damage of the DC/DC converters is shown in Fig. 4.33 (b), where the vertical axis is represented in logarithmic scale. The clamping angle of 60° results in 14 times increase in the accumulated damage of overloaded converter, whereas the unloaded converter has a damage reduction of $1/300$.

Consequently, the discontinuous modulation based power routing can actively control the lifetime of the individual cells of the whole system (i.e. both CHB and DC/DC converters). The lifetime of all CHB cells and unloaded DC/DC converters can be improved with the discontinuous modulation. The overloaded DC/DC converters are stressed more which results in a lower lifetime. However, the proposed strategy results in the lifetime increase of the ones with lowest remaining useful lifetime of cells in the system, leading to a net increase in the system lifetime and a possibility to manage a maintenance schedule.

The electric measures of the discontinuous modulation are demonstrated with a developed laboratory prototype shown in appendix 9.1.1, where $M_c=M_{nc}=0.8$, $f_{sw}=20$ kHz, $K=3$ and $N=2$ are chosen for the following experimental results.

The dynamic response when the modulation method is transferred from the sinusoidal to the discontinuous method is identified in Fig. 4.34 and it is obviously seen the modulation method is seamlessly switched between. Therefore, the method can be simply implemented without any special control efforts.

The power routing capability is validated in Fig. 4.35 (a), where the solid line is obtained from the theoretical analysis in Fig. 4.22 and the value from the experimental results is indicated in circle. As the clamping is increasing, the loading power of cells modulated by the clamped signal is increasing, whereas that of cell with the non-clamped signal is reducing. Finally, the effect of the clamping angle on the thermal stress is validated in Fig. 4.35 (b), where CHB_{nc} and CHB_c are the CHB cell modulated with the non-clamped and clamped signal, respectively, and DC_{nc} and DC_c are the DC/DC converter associated with the CHB cell modulated with the the non-clamped and clamped signal, respectively. Here, it should be mentioned that the junction temperature is directly measured with open modules which provide the access to the semiconductors. The entire system for the thermal

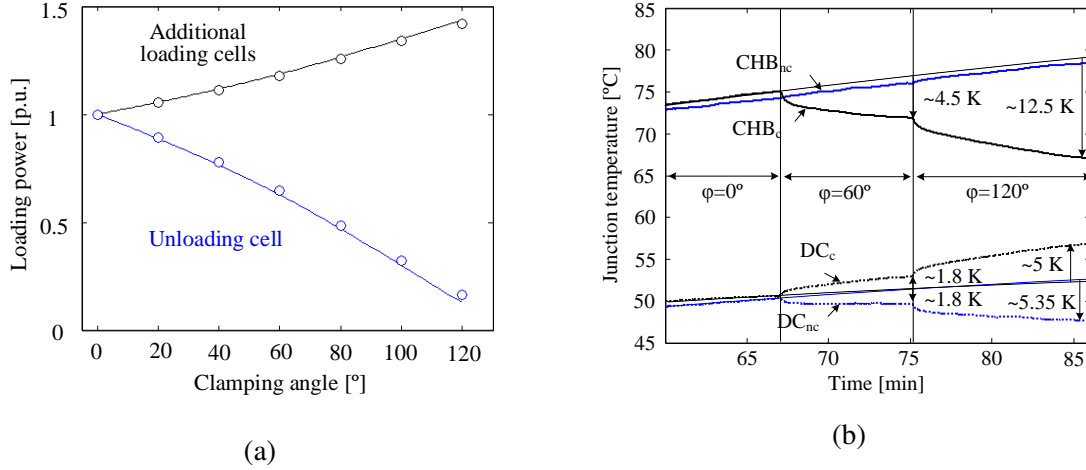


Figure 4.35: (a) Power routing capability and (b) effect of clamping angle on the junction temperature.

test is composed of 5-level CHB converter and two isolated DC/DC converters (shown in appendix 9.1.1). The DC-link voltage of each cell is 150 V and output current is $10 A_{peak}$. As increasing the clamping angle to 60° and 120° , the junction temperature of the clamped CHB cell is decreased by 4.5 K and 12.5 K, respectively. On the other hand, since the DC/DC converter that is connected to the clamped CHB cell processes additional loading, its junction temperature is increased by 1.8 K and 5 K, respectively, whereas the unloading DC/DC converter's thermal stress is reduced.

4.2.3 Influence of the active thermal control methods on DC-link capacitor's current spectrum

The active thermal control strategies exploit the modified modulation signals for each cell. For the multi-frequency modulation, the third-harmonic component is used (see Fig. 4.9), whereas the offset component is added for the discontinuous modulation (see Fig. 4.21). This implies that the modified modulation signals shall differently influence on the DC-link capacitor current for each cell.

The DC-link capacitor currents in the balanced condition, the additional loading cell and the unloading cell are shown in Fig. 4.36, along with a respective frequency spectrum. Here, the switching frequency of each cell is 20 kHz. Remarkably, the capacitor currents mainly has even-order harmonics of the switching frequency and in the balanced condition, the second-order harmonic has the highest value. Fig. 4.36 (a) shows the case with the multi-frequency modulation. For both additional and unloaded cells, the second-order harmonic is decreased. The influence of the discontinuous modulation is shown in Fig. 4.36 (b). The harmonics in the additional loading cell is reduced, whereas only the fourth-order harmonic of the unloaded cell is decreased.

Consequently, it has been revealed that the proposed modulation methods for power semiconductors' reliability modify the DC-link capacitor current spectrum. This modified spectrum

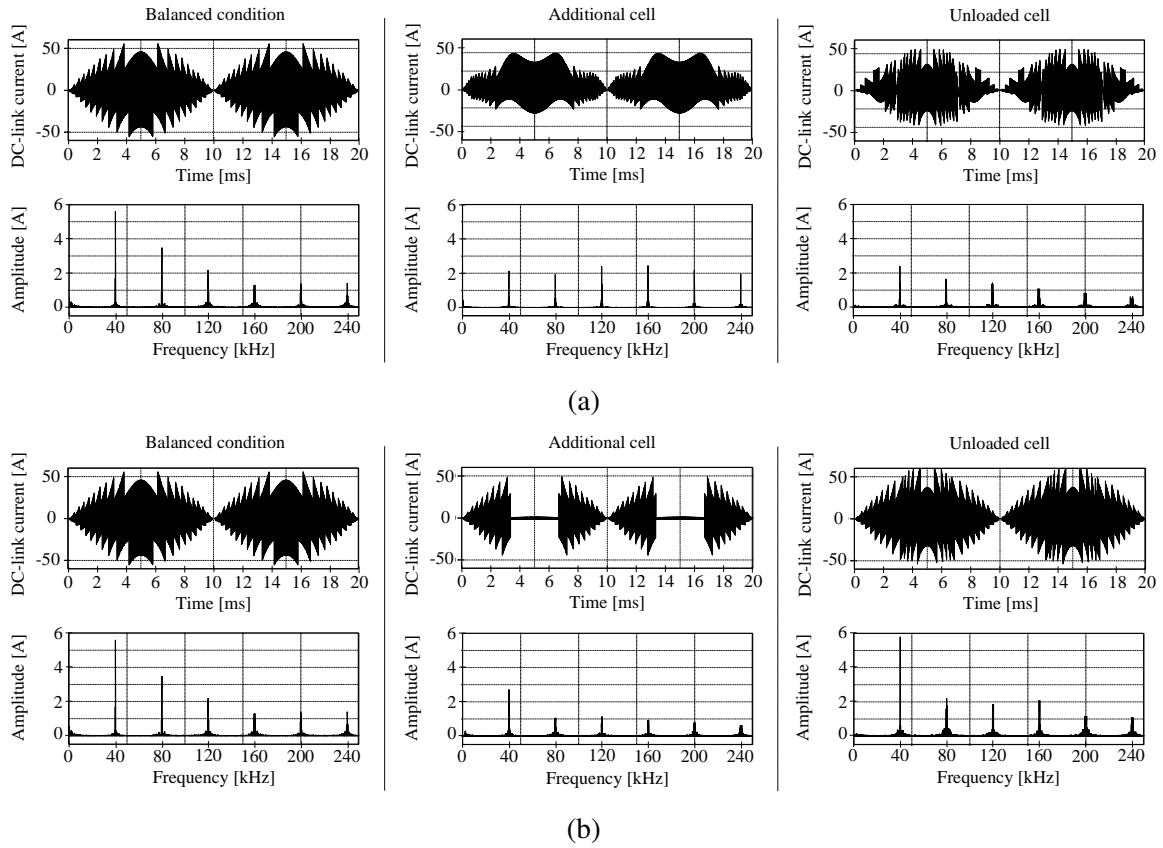


Figure 4.36: DC-link current in balanced condition (left), additional loading cell (middle) and unloading cell (right) by (a) multi-frequency modulation and (b) discontinuous modulation with 60° clamping angle.

definitely influences on the thermal stress of capacitors. From this, an open research topic is derived, which explores the influence of the proposed method on the capacitors’ thermal stress and further, proposes a method to consider the thermal stress of both devices, power semiconductors and capacitors.

4.3 Variable-Clamping Angle Discontinuous Modulation

In this section, the variable-clamping angle discontinuous modulation strategy is proposed, which is applicable to both the series and parallel modular converters.

4.3.1 Variable-clamping angle discontinuous modulation for the series modular converter

The reliability of only CHB converter is addressed, assuming that it is composed of differently aged cells. The discontinuous modulation, which has been proposed in the previous section, is one of the attractive candidate, since the losses of the IGBT and diode can be accordingly manipulated as shown in Fig. 4.30, whereas in case of the multi-frequency method, the loss distribution for the IGBT and the diode is inversely varied (see Fig. 4.16). Therefore,

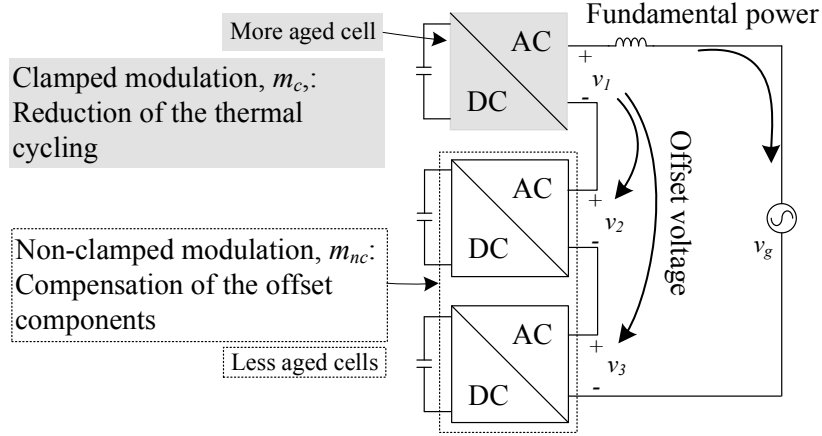


Figure 4.37: Concept of the proposed discontinuous modulation in order to reduce the thermal stresses of more aged cell.

it is reasonable that the discontinuous modulation is chosen for the active thermal control of the CHB converter.

Referring to Fig. 4.21, the concept for the CHB converter is illustrated in Fig. 4.37, in which the most aged cell is modulated by the clamped modulation to reduce the thermal stresses, whereas the others are operated with the non-clamped modulation to compensate the offset component. For this, the *variable-clamping angle* strategy is proposed in order to compensate the thermal cycling in the most aged cell.

The variable-clamping angle method exploits the clamping angle as the control variable for manipulating the switching losses, consequently which aims at compensating the total losses. The total losses, P_t , are a summation of the conduction losses, P_{cd} , and the switching losses, P_{sw} , which can be represented as a function of the loaded power, P_{load} , and the clamping angle, φ as expressed in

$$P_t(P_{load}, \varphi) = P_{cd}(P_{load}, \varphi) + P_{sw}(P_{load}, \varphi). \quad (4.36)$$

As analyzed in [139], the modulation methods only marginally affect the total conduction losses. Therefore, (4.36) can be expressed with the modified term for the conduction losses with (4.37), which results in a straight-forward relation between the total losses and the clamping angle.

$$\underbrace{P_{total}(P_{load}, \varphi)}_{\varphi\text{-dependent}} = P_{cond}(P_{load}) + \underbrace{P_{sw}(P_{load}, \varphi)}_{\varphi\text{-dependent}} \quad (4.37)$$

Here, the loading power is determined by a mission profile, meaning that the power of the converter cannot be manipulated without reducing the loading power. However, the clamping angle has a degree of freedom to be controlled as highlighted in the equation. This feature provides a possibility to manage the total losses regardless of the loading power.

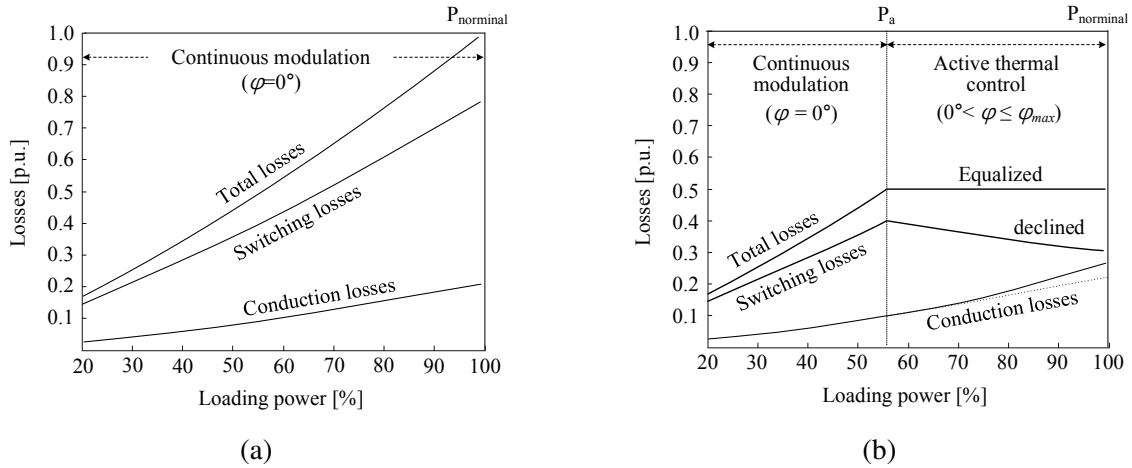


Figure 4.38: Example of the loss distribution (a) with the sinusoidal modulation and (b) with the variable-clamping angle strategy to compensate the thermal cycling of more aged converters by equalizing the total losses for a certain power range ($P_a - P_{nominal}$ as a case study).

Fig. 4.38 (a) visualizes the dependence of the losses on the power, and it can be intuitively expected that thermal cycling will be caused by power variations during system operation. The proposed method of using the clamping angle expressed in (4.37), targets to equalize the total losses for a specific power range ($P_a \leq P_{load} \leq P_{nominal}$) as shown in Fig. 4.38 (b), where the clamping angle is varied from 0° to φ_{max} . This so-called *variable-clamping angle*. Whereas, the continuous modulation ($\varphi=0^\circ$) is adopted out of the active thermal control region ($0 \leq P_{load} \leq P_a$). Moreover, the proposed method features the reduced losses in the active thermal control region (heavy load), while keeping the same loss distribution in a light load region, compared with that by the continuous modulation. This is a remarkable advantage not only for the target to reduce the thermal stresses but also for the better efficiency.

For a better understanding of the effect on the thermal cycling reduction, Fig. 4.39 shows the expected junction temperature of power semiconductor under a specific power profile. As it can be expected, the junction temperature fluctuations are dependent on the specific power profile without the active thermal control (see Fig. 4.39 (a)), whereas the thermal cycling can be reduced in the active thermal control range ($P_a < P_{load} < P_{nominal}$ in Fig. 4.38) as shown in Fig. 4.39 (b).

The capability is investigated in terms of 1) the maximum number of thermally compensated cells, 2) the influence of system design parameter and 3) the optimal active thermal control.

1) Maximum number of thermally compensated cells

Referring to (4.31), the maximum number of thermally compensated cells (i.e. modulated by m_c) is derived as a function of the total number of cells and the modulation index in Fig. 4.40. As it can be seen, the proposed method is further capable with the higher modulation index, which implies a lower DC-link voltage in grid-connected converters. Therefore, this feature would be an additional advantage, since the lower DC-link voltage allows the lower

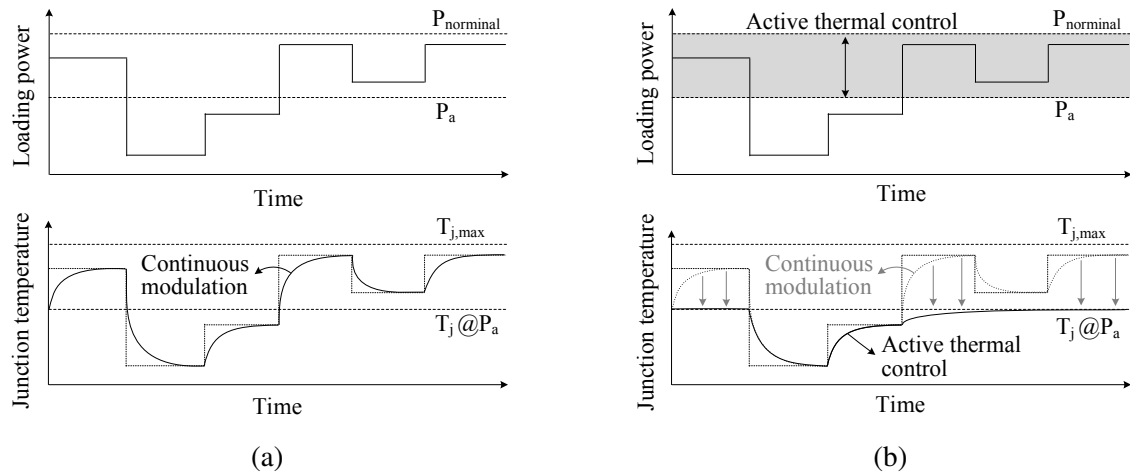


Figure 4.39: Schematic junction temperature variation (bottom) under a fluctuating power profile (top) with (a) the sinusoidal modulation and (b) the proposed variable-clamping angle.

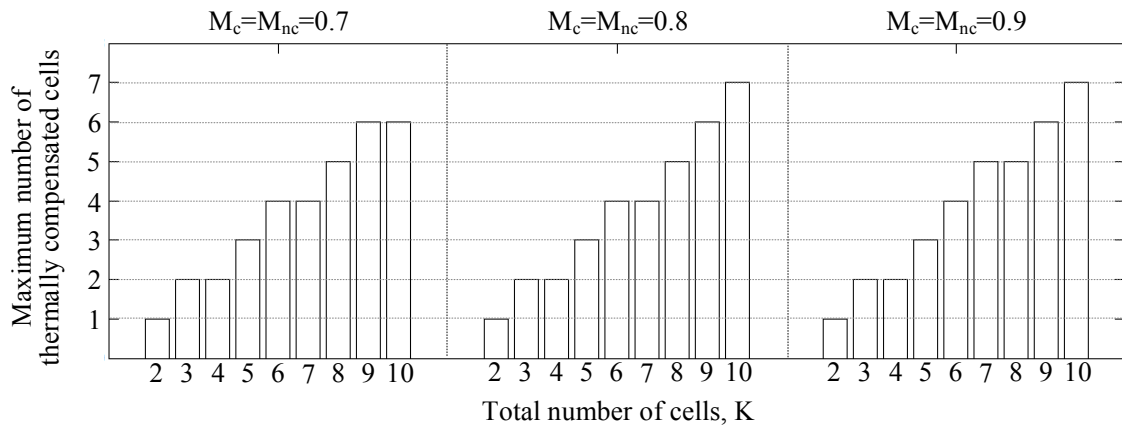


Figure 4.40: Thermal compensation capability depending on the number of cells and the modulation index.

switching losses.

2) Influence of system design parameters

The switching losses that are the target to be modified for the active thermal control, depend on the switching frequency and the DC-link voltage as presented in (4.7). Hence, it is obvious that these design parameters have an influence on the potential of the active thermal control algorithm.

The available active thermal control region is shown in Fig. 4.41 (a) as a function of the switching frequency, where the region is normalized on that with the switching frequency of 5 kHz. As increasing the switching frequency, the area becomes larger and for 25 kHz switching frequency, the potential active thermal control region is almost twice. Fig. 4.41 (b) shows the DC-link voltage's influence on the available active thermal control region, where the vertical axis is normalized on the value when the ratio between the grid voltage

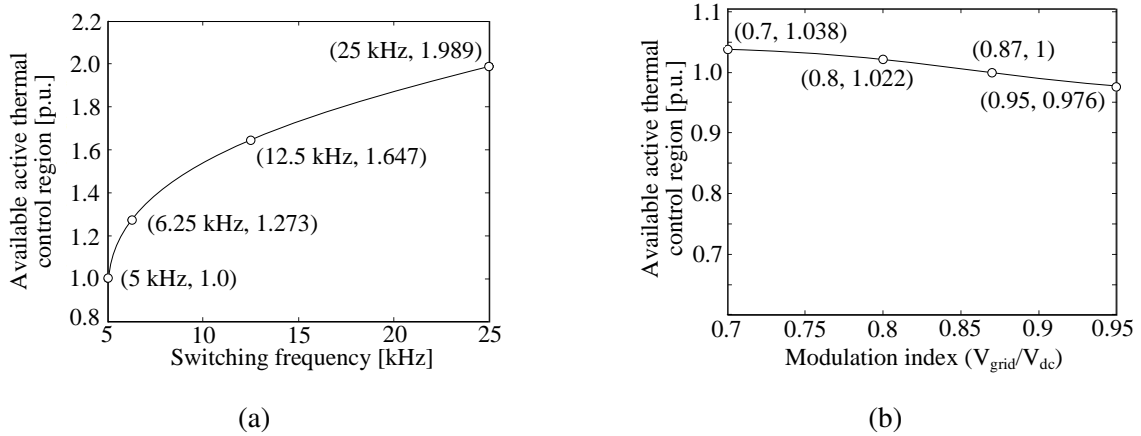


Figure 4.41: Influence of (a) switching frequency and (b) DC-link voltage on capability of the active thermal control area.

and the DC-link voltage is $V_{grid}/V_{dc} = 0.87$. The variation is 6.2% (from 103.8 to 97.6%) as increasing the modulation index from 0.7 to 0.95. The influence of the DC-link voltage is relatively low, compared with the switching frequency.

From the above analysis, it can be concluded that the higher switching frequency and the higher DC-link voltage allow the active thermal control region to be larger. However, these design parameters should be carefully determined because the higher design values generate more losses, leading to a higher mean junction temperature.

3) Optimal active thermal control strategy

It is necessary to analyze how the application of active thermal control is affecting the lifetime consumption of power semiconductors, which would lead to an optimal control law for the tuning of the controller. For this purpose, the active thermal control region is moved for the predefined power profile as shown in Fig. 4.42. The range of active thermal control region is fixed to 20% of the rated power and the region is moved from (50, 70)% to (80,

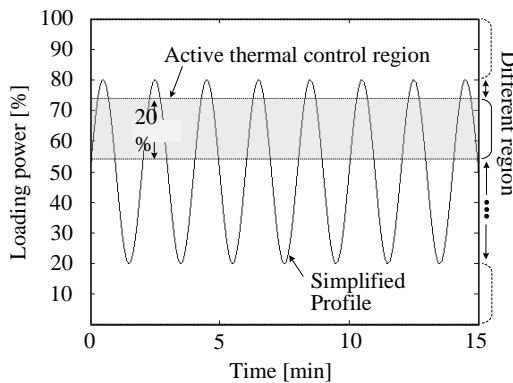


Figure 4.42: A simplified power profile with different active thermal control regions to identify its impact on the lifetime.

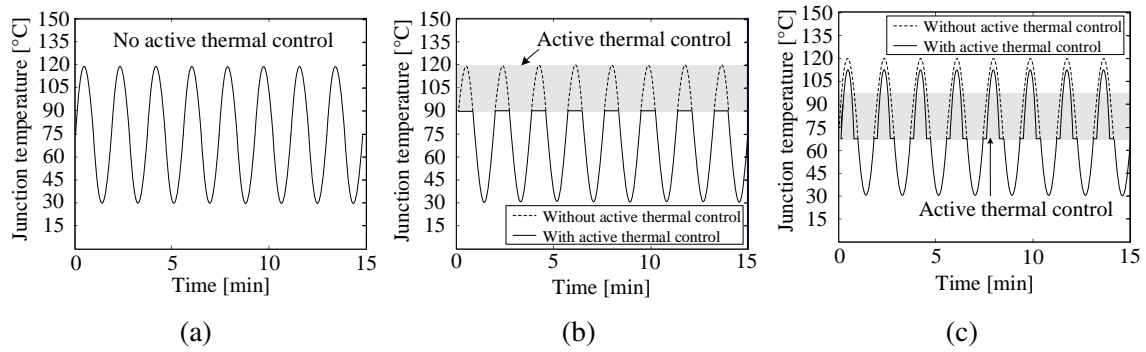


Figure 4.43: Expected junction temperature depending on different active thermal control regions: (a) Case 1, (b) Case 2 and (c) Case 3.

100) % with a step of 2.5 %. This enables to identify the effect of the region, leading to three representative cases defined as:

- Case 1: No active thermal control: (80, 100) %
- Case 2: The clamping region covers the profile by reaching the top of the profile or partly covers the top of the profile: (60, 80) - (77.5, 97.5) %
- Case 3: The clamping region completely covers the profile but does not reach the top of the profile: (50, 70) - (57.5, 77.5) %

These three cases are visualized in Fig. 4.43 with the according junction temperature variation. Fig. 4.44 shows the accumulated damage derived with (3.1) and (3.5) for the power semiconductors in the different cases. The first case is without the active thermal control and its damage is defined as 1 per-unit. For the second case, the highest reduction of the accumulated damage is observed, especially, when the active thermal control region is reduced from 60 to 80 %. In the third case, the damage is reduced because of a smaller thermal swing compared with the first case but the damage increases compared with the second case. As a conclusion, the clamping region of the proposed active thermal algorithm should be located in the area covering the peak of the power profile to effectively improve the lifetime.

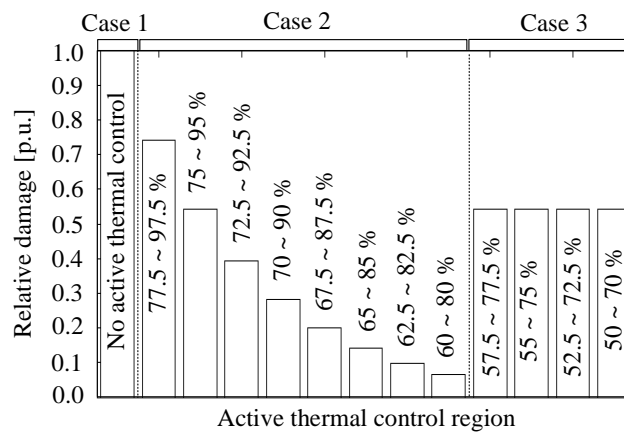


Figure 4.44: Accumulated relative damage with the different clamping regions .

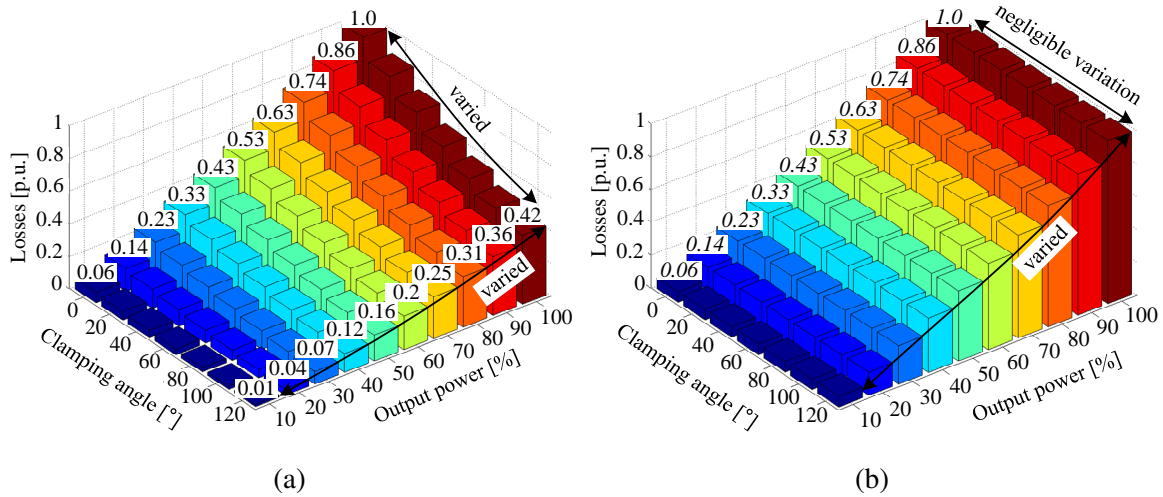


Figure 4.45: Loss distribution as a function of output power and the clamping angle with (a) the clamped signal and (b) the non-clamped signal (Part: DP25H1200T101667).

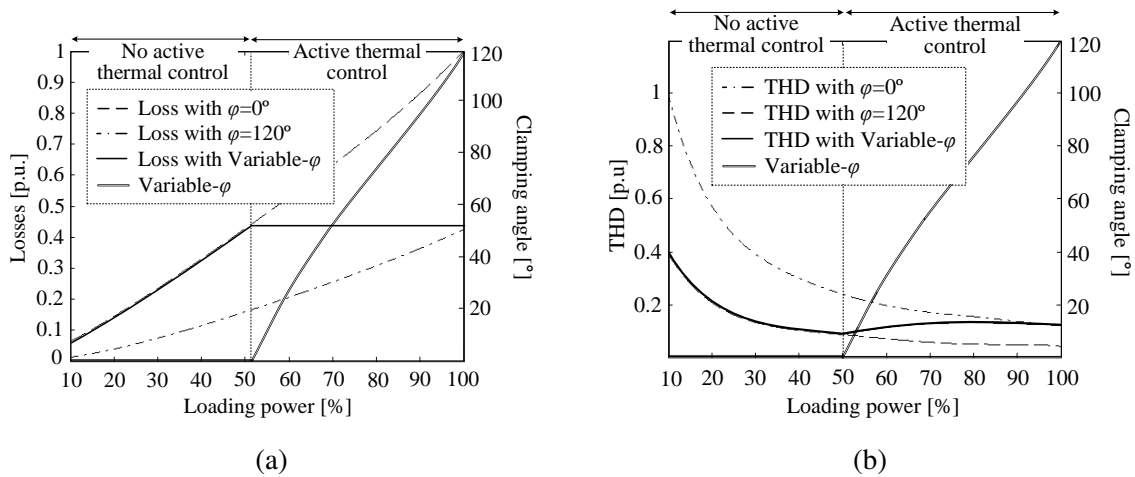


Figure 4.46: (a) Active clamping angle in order to equalize loss distribution and (b) THD with the active clamping angle to equalize the losses from 50 % to 100 % power (Part: DP25H1200T101667).

The loss distribution is demonstrated with the power device DP25H1200T101667, where the operating condition, $V_{dc}=150$ V (450 V in total), $f_{sw}=23$ kHz, $M_c=M_{nc}=0.8$, $PF=1$, is considered. Since the clamping angle is considered as a control variable to compensate the thermal cycling, its relation to the losses is shown in Fig. 4.45 as a function of the output power. As shown in Fig. 4.45 (a), the loss distribution by the clamped modulation, m_c , depends not only on the output power but also on the clamping angle, whereas the loss distribution by the non-clamped modulation, m_{nc} , only depends on the output power as shown in Fig. 4.45 (b). Therefore, the variable-clamping angle concept allows the active thermal control for the more aged cells, hardly affecting the reliability of the other healthy cells.

The relation between the output power and the generated losses is shown in Fig. 4.46 (a), when the clamping angle is 0° and 120° , respectively, and two losses are different in the entire power range. Therefore, it is derived that the losses can be equalized within this boundary

(from the minimum losses with 120° to the maximum losses with 0°), once the clamping angle is properly controlled. As an example, the loss distribution is equalized from 50 % to the nominal output power as drawn in solid line, and this is achieved with the clamping angle varied from 0° to 120° as drawn in double solid line. Further, it should be mentioned that the active thermal control can be set for other regions, depending on the most frequent operating condition.

The variable-clamping angle is tuned to equalize the losses from 50 % to 100 % power and its corresponding THD are shown in Fig. 4.46 (b). The clamping angle is non-linearly varied from 120° to 0° as the output power decreases from 100 % to 50 %, whereas in below 50 % power, the clamping angle is fixed to 0° . Meanwhile, the THD is determined following the clamping angle as the solid line.

The variable-clamping angle discontinuous modulation is applied under a mission profile with fluctuating power as shown in Fig. 4.47. Like the case of the multi-frequency modulation, a constant ambient temperature $T_a = 40^\circ\text{C}$ and a design for the maximum junction temperature of $T_{j,max} = 90^\circ\text{C}$ is assumed. In the first case, the sinusoidal modulation is applied, resulting that the junction temperature of each cell is identical. On the other hand, in the second case, the active clamping period is used as shown in Fig. 4.46 (a). The clamping angle is set to $\varphi = 0^\circ$ for an output power lower than 50 %, whereas the clamping angle is controlled to hold the junction temperature constant for a power higher than 50 %. This results in a less junction temperature fluctuation for the cell, $T_{j,cellA}$, while that of other cells is kept at the similar level with the sinusoidal modulation case. Namely, the lifetime of cell A can be prolonged without affecting the lifetime of cell B and C. Finally, the thermal stress reduction is quantified with the Rainflow counting and linear damage accumulation. It can be seen, that the damage for the cell A is reduced to approximately 1 % of the prior damage, while the other cells keep their damage unchanged. Consequently, an expected lifetime increase for the cell A by a factor of 100 is achieved.

The proposed method is validated by measuring the junction temperature of a power module. The developed prototype shown in appendix 9.1.1. The impact of the clamping angle is presented in Fig. 4.48 with a fixed power at 80 %. As mentioned before (see Fig. 4.45), the junction temperature of the clamped cell is influenced by the clamping angle. The IGBT junction temperature is reduced approximately by 2.7°C with the 60° clamping angle and 4.7°C with the 120° clamping angle, while for the freewheeling diode, the temperature decreases approximately by 3.2°C and 6.1°C with 60° and 120° clamping angle, respectively. On the other hand, the influence on the junction temperature of the non-clamped cell is negligible. This result matches well with the loss distribution analysis.

The temperature variation is dependent on the output power as presented in Fig. 4.49, where the clamping angle is set to 0° . The temperature is reduced by 6.1°C and 3.7°C in the IGBT and diode, respectively, with the power changed from 40 % to 80 %, whereas 3.1°C and 1.7°C is changed when the power is reduced from 80 % to 60 %. With the above temperature profile in Figs. 4.48 and 4.49, it is expected that the temperature variation caused by the power change can be compensated with the clamping angle.

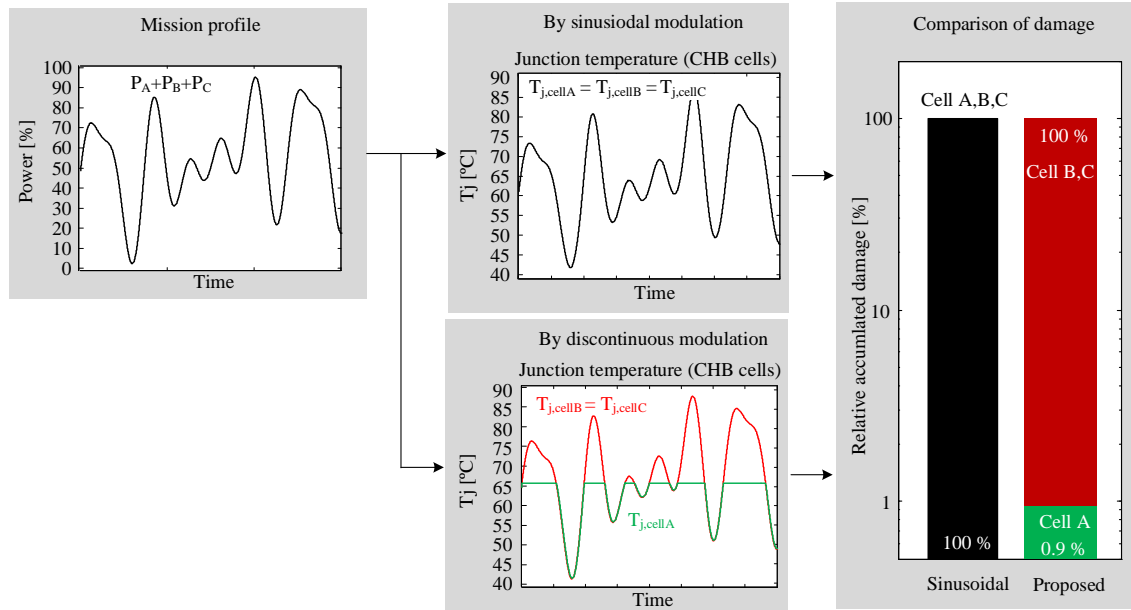


Figure 4.47: Estimation of accumulated damage of the CHB converter cells depending on modulation methods: sinusoidal modulation (top) and variable-clamping angle discontinuous modulation (bottom).

Finally, the active clamping angle is adopted to compensate the junction temperature variation at different powers as shown in Fig. 4.50. While the temperature of the clamped cell is compensated, the non-clamped cell shows a similar temperature profile to Fig. 4.49. In the compensated profile in Fig. 4.50, the temperature of the IGBT is reduced by 79 % (power changed from 40 % to 80 %) and by 64 % (power changed from 60 % to 80 %) as shown in Fig. 4.50 (a), while the temperature variation on the diode is almost equalized as shown in Fig. 4.50 (b).

4.3.2 Variable-clamping angle discontinuous modulation for the parallel modular converters

The active thermal control based on the discontinuous modulation is applied to parallel modular converters. The configurations in Fig. 4.51 (a) and 4.51 (b) are considered. Fig. 4.51 (a) is widely adopted in high power grid-connected applications [140, 141], whereas the multiple galvanically isolated converters shown in Fig. 4.51 (b) are commonly applied in wind farms and solar parks. For addressing the reliability of these converters, each converter connected to the Point of Common Coupling (PCC) is expected to have a different useful remaining lifetime.

The proposed method aims at not only achieving the remaining useful lifetime increase but also maintaining good power quality at the PCC. The modulation strategy consisting of two different modulation signals is shown in Fig. 4.52. The modulation signal for the thermal cycling compensation is shown in Fig. 4.52 (a) and named as m_{ACT} , while Fig. 4.52 (b) is the modulation signal (m_{THD}) for improving the power quality. Therefore, these modulation

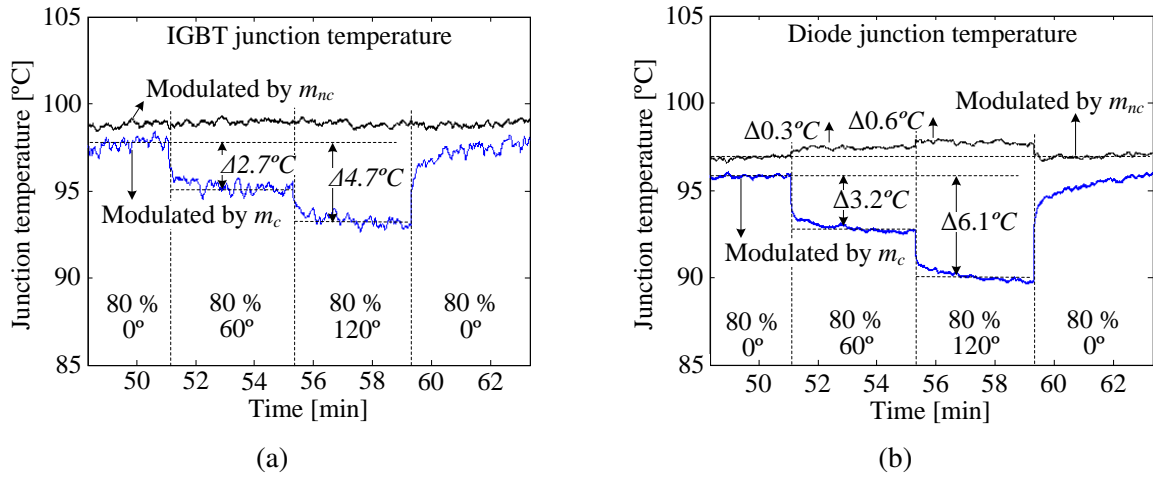


Figure 4.48: Impact of the clamping angle on the junction temperature of (a) IGBT and (b) diode ($P_{load}=80\%$).

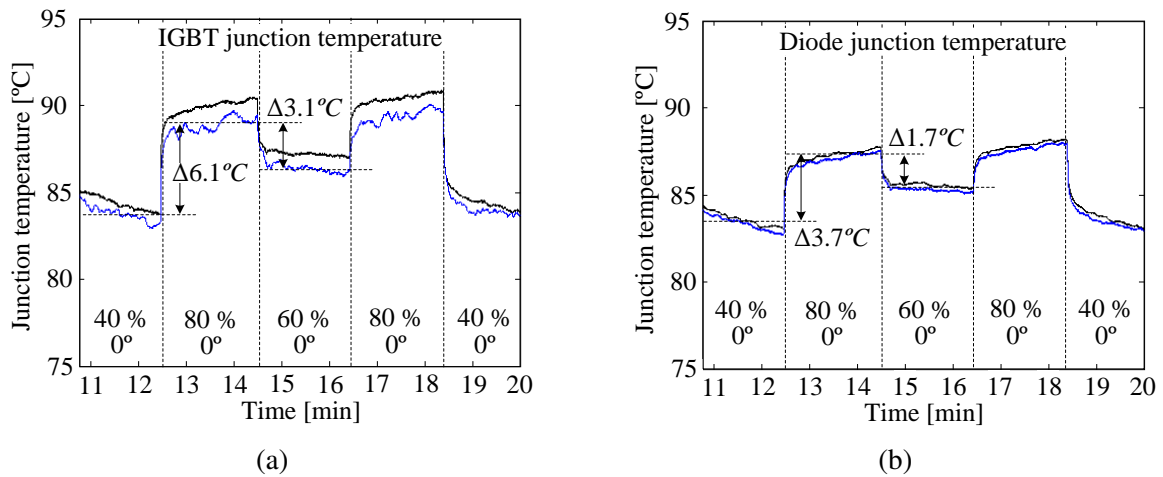


Figure 4.49: Variation of (a) IGBT and (b) diode junction temperature in accordance with output power ($\varphi=0^\circ$).

signals are injected depending on their lifetime, e.g. the converter with the lower remaining useful lifetime is modulated by m_{ACT} , whereas a converter with a higher remaining useful lifetime is modulated with m_{THD} . It is worth to mention that the power losses for the converter modulated by m_{THD} is comparable to the case of the continuous modulation, meaning that its lifetime is unaffected.

Fig. 4.53 shows the total currents simulated for two cases, assuming that the modulating carrier signals for each converter are synchronized. The first case uses only the signal m_{ATC} for both converters, while the second case modulates one converter with m_{ATC} and the other with m_{THD} , respectively. As it can be seen in the results, the ripple current is around 3 A for the first case and the current is distorted by the discontinuous behavior as shown in Fig. 4.53 (a). However, the distortion is reduced with the proposed modulation signal as well as the ripple current is reduced to 1.7 A as shown in Fig. 4.53 (b).

Fig. 4.54 identifies the THD performance of two cases as a function of the clamping angle and the loading power. As shown in Fig. 4.54 (a), the modulation signal m_{ATC} negatively

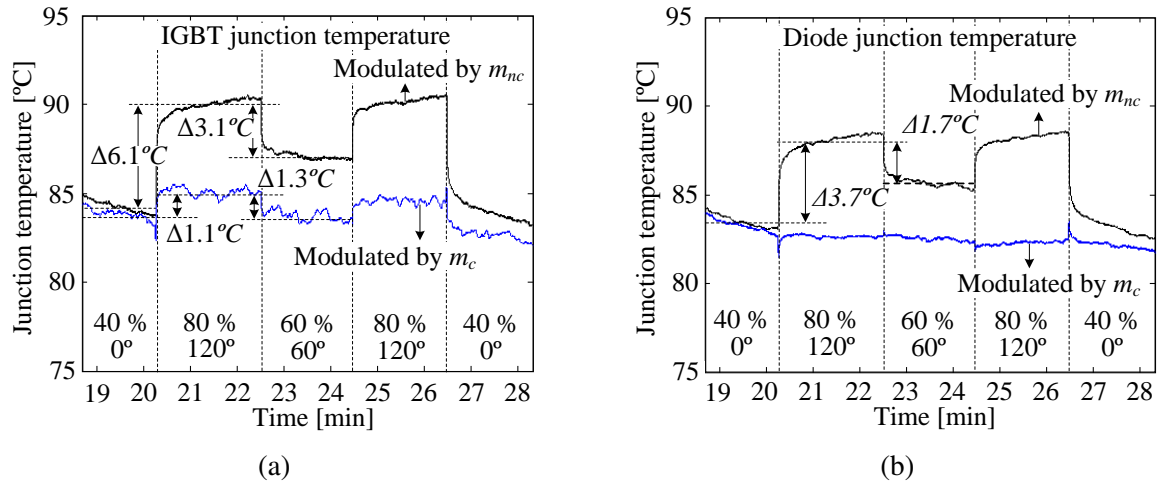


Figure 4.50: Compensation of (a) IGBT and (b) diode junction temperature with the variable-clamping angle method.

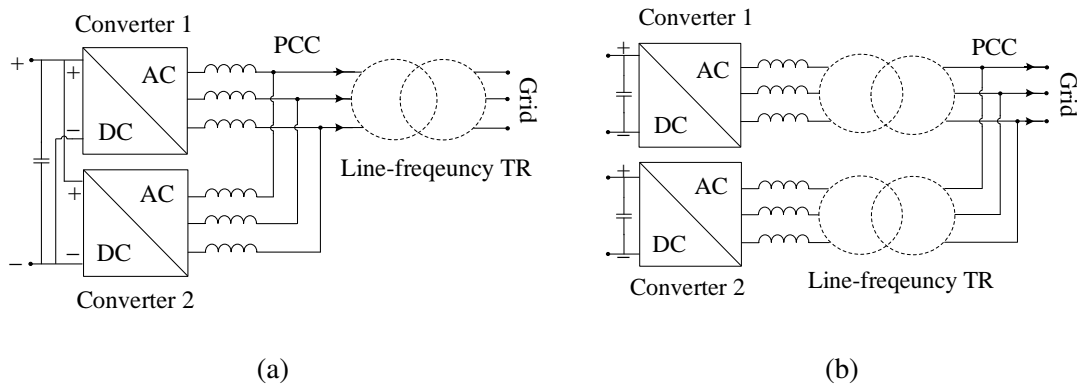


Figure 4.51: Configurations of the paralleled converters connected to a same PCC: (a) with common DC-link and (b) with separated DC-link.

affects the THD performance. An increasing clamping angle impairs the performance. The THD of the output current is decreased by 43 % in case of 100 % power, and by 46.8 % (from 3.61 to 5.3) when the power is 50 %. This might be undesired in grid-connected applications, since a bigger filter would be required in order to fulfill the grid-code. The second case is evaluated in Fig. 4.54 (b). The performance is significantly improved in comparison with Fig. 4.54 (a) with the reduced ripple current as shown in Fig. 4.53.

The potential of the proposed method is validated with the loss distribution, considering the well established two-level converter for the grid-connected application. For this simulation, the switching frequency is set to 5 kHz, the DC-link voltage to 650 V and the power module DP25H1200T101667 (1200 V/25 A) is chosen. It is assumed that the power flows from the DC-link to the electric grid with the unity power factor.

The loss distribution as a function of the clamping angle and the loaded power is shown in Fig. 4.55, where the losses are normalized by that at the nominal power with the clamping angle of 0° . As it is expected, the losses are affected by the processed power and the clamping angle. This gives the opportunity to equalize the generated losses regardless of the processed

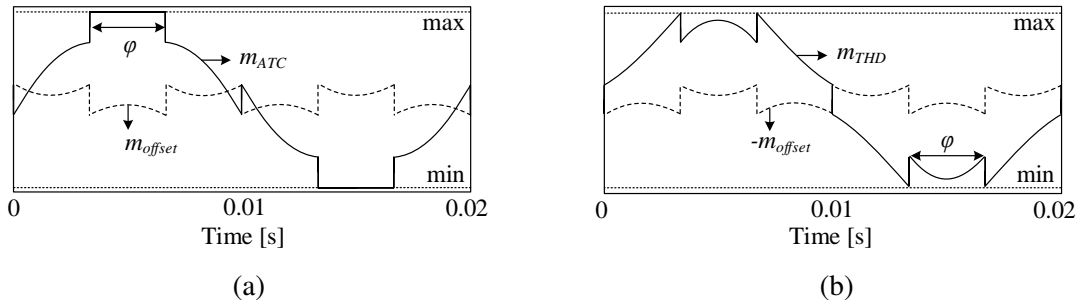


Figure 4.52: Proposed modulation signal having two variants: (a) m_{ATC} for the active thermal control for more aged converter and (b) m_{THD} for another converter to improve the power quality.

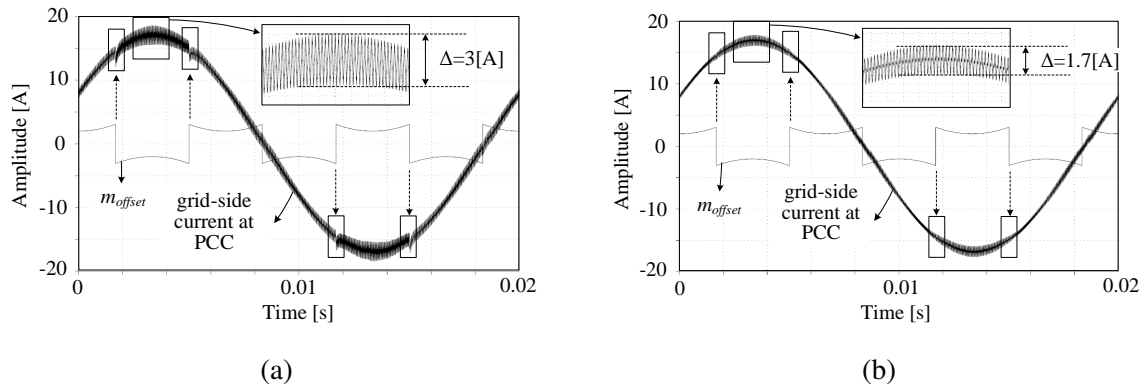


Figure 4.53: Simulated current waveform in case (a) both converters are modulated by m_{ATC} and (b) the more aged converter is modulated with m_{ATC} and the less aged converter is modulated by m_{THD} .

power.

The proposed strategy is developed in Fig. 4.56, based on the loss distribution in Fig. 4.55. The difference between the loss distribution with 0° and 60° clamping angle implies that the losses can be equalized within these boundaries by means of the active clamping angle. The points obtained by simulation are indicated with dots and the curve fitting is drawn in double solid line. In this frame work, the active thermal control region is set between 75.8 % and the nominal power, but it can also be set between 40 % and 54 % depending on frequent fluctuating power range in a considered power profile.

For a demonstration of the active thermal control in a mission profile with highly fluctuated power, the effect of the thermal stress reduction is tested. The example mission profile is shown in Fig. 4.57 and the junction temperature without the proposed algorithm and with the application of active thermal control is simulated. For the application of active thermal control, the clamping region is set to cover the peak power (76 % to 96 % in Fig. 4.56). In comparison to the case without the active thermal control, the damage is reduced to 21 % by the proposed method and this results in a lifetime enhancement of 476 % ($= 100/0.21$). Furthermore, it would be worth to mention that the proposed method does not have a large effect on the efficiency, but still achieves the lower losses than that with the

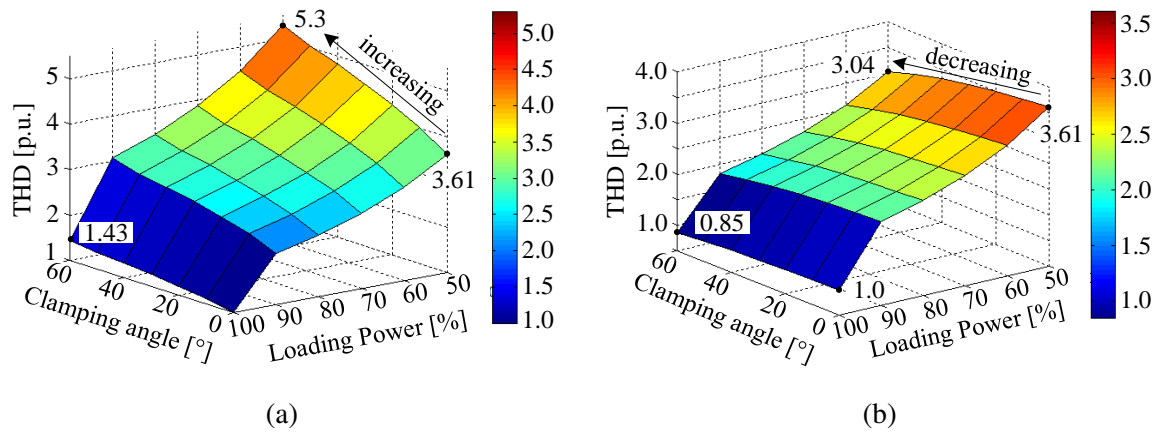


Figure 4.54: THD of the grid-side currents when (a) both converters are modulated by m_{ATC} and (b) each converter is modulated by m_{ATC} and m_{THD} , respectively.

sinusoidal modulation (reduced by 4.3 %). Finally, it should be mentioned that the results in Fig. 4.57 is not intrinsic attribute, namely, the reduction of the accumulated damage would be different under different power profiles.

The impact of the clamping angle on the thermal stress is shown in Fig. 4.58 with thermal images, showing the thermal distribution in the entire region of the power module. The temperature of the IGBT is much higher than that of the diode due to higher losses. Remarkably, it can be observed that the maximum temperature is gradually decreasing by a wider clamping angle. In case of the IGBT from 97.4°C to 92.3°C and for the diode from 86.4°C to 83.6°C.

The proposed concept for compensating the thermal cycles is implemented under a power profile. Fig. 4.59 (a) shows the thermal cycling affected by the power variation from 75.8% → 100% → 60% → 75.8% → 100% without the active thermal control. Accordingly, the deviation of the junction temperature in the IGBT is 3.9°C, 6.4°C, 2.1°C and 4.1°C. Fig. 4.59 (b) shows the junction temperature measurement for the implemented ac-

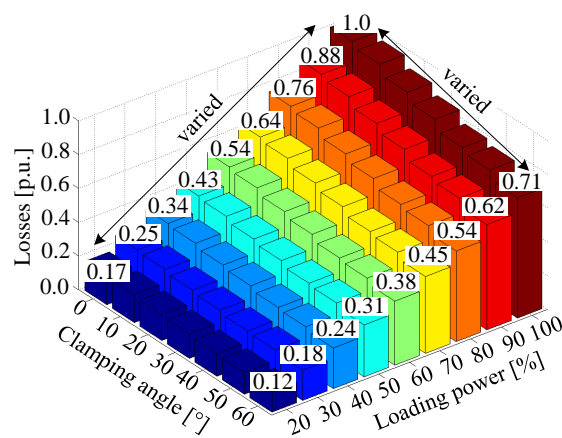


Figure 4.55: Loss distribution as a function of the clamping angle and the loaded power (Part: DP25H1200T101667).

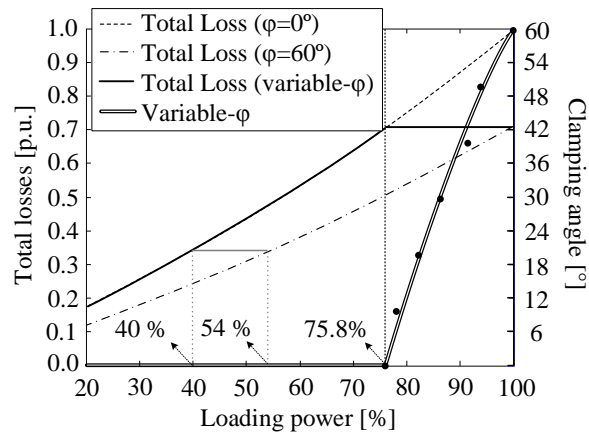


Figure 4.56: Active thermal control strategy to equalize the total losses in the high power range for the two-level converter (Part: DP25H1200T101667).

tive thermal controller, whereby the region is defined from 75.8 % to 100 % (see Fig. 4.56). The temperature variation within the active thermal control region (1 \rightarrow 2 and 4 \rightarrow 5) is almost completely compensated, whereas the variation outside the region is 3.5°C (2 \rightarrow 3) and 2.2°C for the variation from (3 \rightarrow 4). In the same way, the thermal cycling in the diode is compensated by the active thermal control.

4.4 Variable-Carrier Angle Phase-Shifted Modulation

One of the most attractive advantages of the CHB converter is the higher equivalent switching frequency, which can be achieved only under the balanced operating condition with the PSPWM. However, in many practical applications, the balanced condition of equal DC-link voltages and equal modulation signals for each cell can be hardly achieved [142, 143]. To overcome this limit of the original PSPWM that employs the symmetrically displaced carriers, the different variants of the PSPWM were proposed, which are using a different value of the shifting angle for each carrier (so-called as *variable-carrier angle* PSPWM). In [144], the

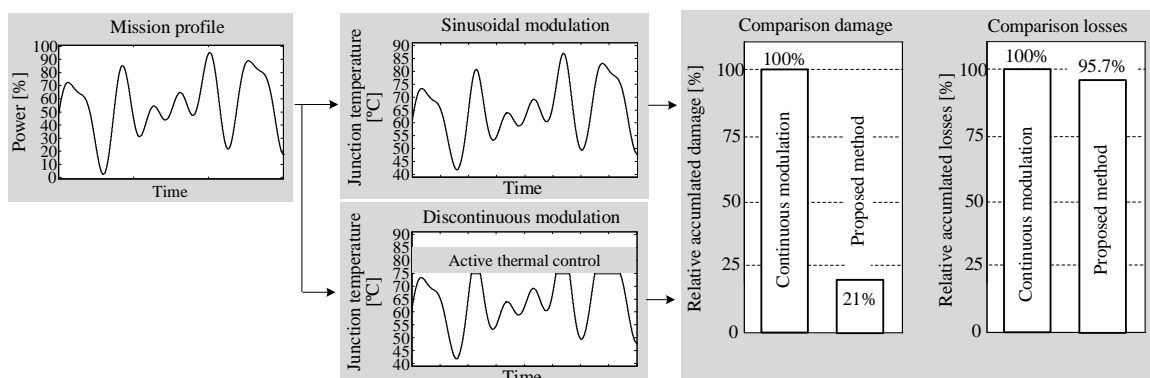


Figure 4.57: Comparison of accumulated damage and losses for a typical 2-level 3-phase converter under an arbitrary mission profile: by the sinusoidal modulation (top) and by the variable-clamping angle discontinuous modulation (bottom).

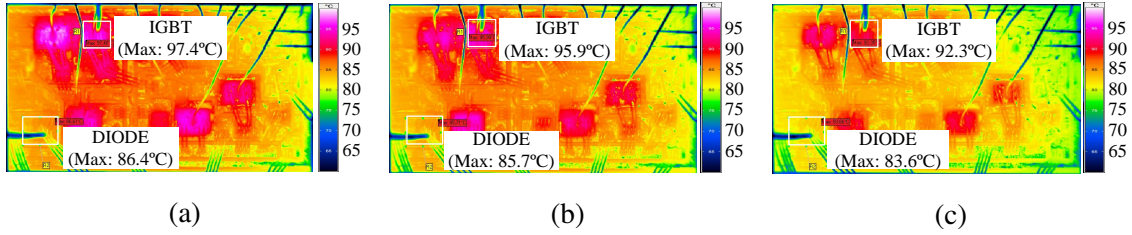


Figure 4.58: Thermal image of the open module at the nominal power with (a) $\varphi = 0^\circ$, (b) $\varphi = 30^\circ$, (c) $\varphi = 60^\circ$.

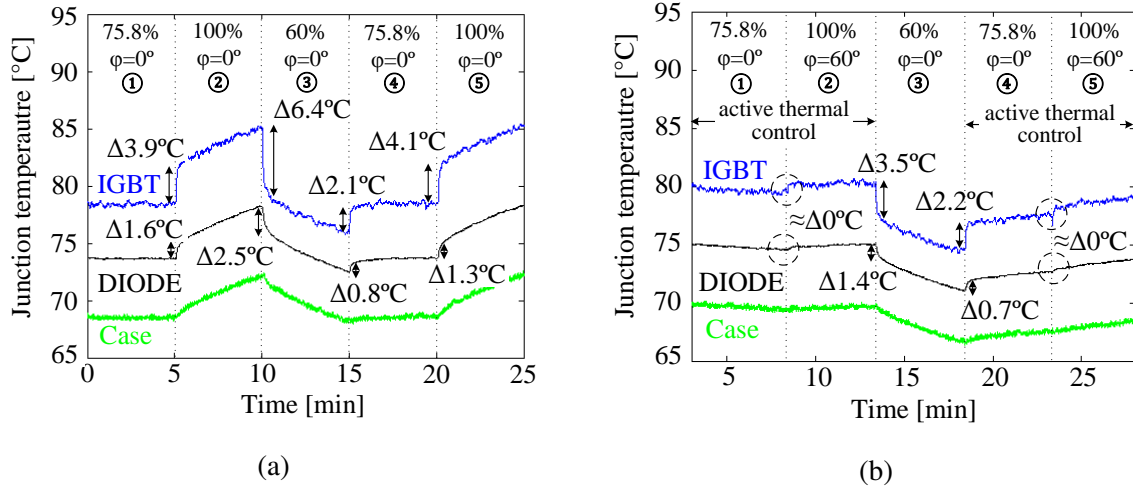


Figure 4.59: Measurement of the junction temperature under varying power (a) without applying active thermal control (with continuous modulation) and (b) with the proposed active thermal control algorithm.

harmonic cancellation is achieved when the DC-link voltages for each cell are unbalanced, resulting in the improved Weighted Total Harmonic Distortion (WTHD) of the overall output voltage. Followed by, the technique considering unequal DC-link voltages and unequal modulation signals for the Static Synchronous Compensator (STATCOM) application, was proposed in [145]. This technique can eliminate the main harmonic component. In [146], the technique based on the Fourier series approach was presented, considering unequal DC-link voltages and unequal modulation signals. This technique allows the cancellation of the first carrier harmonics group.

This section analyzes the WTHD performance of three variable-carrier angle PSPWM techniques proposed in [144, 145, 146], considering three cases of unbalanced operational conditions: 1) unequal DC-link voltages and equal modulation signals, 2) equal DC-link voltages and unequal modulation signals and 3) unequal DC-link voltages and unequal modulation signals. Finally, based on this result, a new technique for the discontinuous modulation is proposed in order to improve the WTHD performance.

4.4.1 Variable-carrier angle phase-shifted modulation techniques

- Symmetric PSPWM

Under the balanced operating condition, the carrier harmonic groups up to $2K^{th}$ -order are completely canceled out for K cascaded cells with the typical symmetric carrier phase-shifted modulation. This feature can be identified by the double Fourier integral analysis, which leads to the following expression for the multi-level AC-voltage of the CHB converter in

$$\begin{aligned}
 v_{inv}(t) &= K \cdot V_{dc} \cdot M \cdot \cos(\omega_0 t) \\
 &+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} \cdot J_{2n-1}(m\pi M) \cdot \cos([m+n-1]\pi) \\
 &\times \sum_{i=1}^K \cos(2m\omega_c t [2n-1] \omega_0 t + 2m\theta_i)
 \end{aligned} \tag{4.38}$$

Here, V_{dc} is the DC-link voltage of each cell, M is the modulation index, ω_0 is the pulsation of the modulating signal, m and n are the orders of carrier and modulating signal harmonics, J_{2n-1} is the Bessel function of order $2n-1$, ω_c is the pulsation of the carrier signal and θ_i is the relative phase of leading leg of the i^{th} cell. In the above equation, the symmetric phase shift allows all carrier group to be compensated apart from the carrier group of $2K$ as expressed in

$$\begin{aligned}
 v_{inv}(t) &= K \cdot V_{dc} \cdot M \cdot \cos(\omega_0 t) \\
 &+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} \cdot J_{2n-1}(m\pi M) \cdot \cos([m+n-1]\pi) \\
 &\times \cos(2Km\omega_c t [2n-1] \omega_0 t).
 \end{aligned} \tag{4.39}$$

However, the critical limitation of the symmetric PSPWM is that the perfectly balanced operation is required.

- Technique A [144]

The *technique A* considers a case of unequal DC-link voltages and equal modulation signals and this is expressed in

$$\begin{aligned}
 v_{inv}(t) &= M \sum_{i=1}^K V_{dc,i} \cdot \cos(\omega_0 t) \\
 &+ \frac{4}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} \cdot J_{2n-1}(m\pi M) \cdot \cos([m+n-1]\pi) \\
 &\times \sum_{i=1}^K V_{dc,i} \cdot \cos(2m\omega_c t [2n-1]\omega_0 t + 2m\theta_i).
 \end{aligned} \tag{4.40}$$

In order to compensate the carrier harmonics produced by each cell, the third line in the above equation must become zero as

$$\sum_{i=1}^K V_{dc,i} \cdot \cos(2m\omega_c t [2n-1]\omega_0 t + 2m\theta_i) = 0. \tag{4.41}$$

Therefore, the phase shift angle should satisfy the below conditions in

$$\begin{cases} \sum_{i=1}^K V_{dc,i} \cdot \cos(2m\theta_i) = 0 \\ \sum_{i=1}^K V_{dc,i} \cdot \sin(2m\theta_i) = 0 \end{cases} \tag{4.42}$$

where $2m\theta_i$ represents the phase of all the carrier harmonics (center and sidebands) belonging to the m^{th} carrier group produced by the i^{th} cell. It should be mentioned that the above condition is valid for all harmonics in a same carrier-order group, because the harmonics in the same carrier-order group vary their amplitude of same quantity as the index n varies in (4.40). Consequently, the attractive advantage of this technique is that it is possible to cancel out all the harmonics of the same carrier group.

Considering three cascaded cells ($K = 3$), the first carrier-order group can be completely canceled out, once the modified phase shift angles are applied, which satisfy the condition in (4.42). This is re-written for $K = 3$ in

$$\begin{cases} V_{dc,1} + V_{dc,2} \cdot \cos(\theta_2) + V_{dc,3} \cdot \cos(\theta_3) = 0 \\ V_{dc,2} \cdot \sin(\theta_2) + V_{dc,3} \cdot \sin(\theta_3) = 0 \end{cases} \tag{4.43}$$

Finally, the solution of the (4.43) is found in

$$\begin{cases} \cos(\theta_2) = \frac{1}{2} \left(\frac{-V_{dc,1}^2 - V_{dc,2}^2 + V_{dc,3}^2}{V_{dc,1}^2 V_{dc,2}^2} \right) \\ \cos(\theta_3) = \frac{1}{2} \left(\frac{-V_{dc,1}^2 + V_{dc,2}^2 - V_{dc,3}^2}{V_{dc,1}^2 V_{dc,3}^2} \right) \end{cases} \quad (4.44)$$

However, the angles, θ_2 and θ_3 , are valid only when the following conditions in (4.45) are satisfied and it is evident that the validity region of this technique is influenced by the DC-link voltages.

$$\begin{cases} |V_{dc,1} - V_{dc,2}| \leq V_{dc,3} \leq V_{dc,1} + V_{dc,2} \\ |V_{dc,1} - V_{dc,3}| \leq V_{dc,2} \leq V_{dc,1} + V_{dc,3} \end{cases} \quad (4.45)$$

- Technique B [145]

The *technique B* is suitable for a case of unequal DC voltages and unequal modulation signals, resulting in the voltage expression as

$$\begin{aligned} v_{inv}(t) &= \sum_{i=1}^K M_i \cdot V_{dc,i} \cdot \cos(\omega_0 t) \\ &+ \frac{4}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} \cdot \cos([m+n-1]\pi) \\ &\times \sum_{i=1}^K J_{2n-1}(m\pi M_i) \cdot V_{dc,i} \cdot \cos(2m\omega_c t [2n-1]\omega_0 t + 2m\theta_i). \end{aligned} \quad (4.46)$$

Unlike (4.40), since the cancellation condition is not same for all harmonics in a same carrier harmonic group, the harmonics cancellation within a whole group cannot be achieved. Instead, the *technique B* allows to compensate the sum of the main harmonics that have $2(f_c/f_0) \pm 1$ harmonic order (i.e. $m = 1$ and $n = [0; 1]$). The amplitude of these main harmonics depends on both DC-link voltage and modulation signal of each cell as expressed in

$$V_i = \frac{2}{\pi} \cdot V_{dc,i} \cdot J_{2n-1}(\pi M_i). \quad (i = 1, 2, \dots, K) \quad (4.47)$$

Therefore, considering $K = 3$, the main harmonics can be compensated in case the condition in (4.48) is satisfied.

$$\begin{cases} V_1 + V_2 \cdot \cos(\theta_2) + V_3 \cdot \cos(\theta_3) = 0 \\ V_2 \cdot \sin(\theta_2) + V_3 \cdot \sin(\theta_3) = 0. \end{cases} \quad (4.48)$$

Finally, the solution to the equations in (4.48) is found as

$$\begin{cases} \cos(\theta_2) = \frac{1}{2} \left(\frac{-V_1^2 - V_2^2 + V_3^2}{V_1^2 V_2^2} \right) \\ \cos(\theta_3) = \frac{1}{2} \left(\frac{-V_1^2 + V_2^2 - V_3^2}{V_1^2 V_3^2} \right). \end{cases} \quad (4.49)$$

Similar to the previous technique, the angles, θ_2 and θ_3 , are only valid when the following conditions in (4.50) are satisfied.

$$\begin{cases} |V_1 - V_2| \leq V_3 \leq V_1 + V_2 \\ |V_1 - V_3| \leq V_2 \leq V_1 + V_3 \end{cases} \quad (4.50)$$

- Technique C [146]

The *technique C* considers a case of unequal DC voltages and unequal modulating signals, but unlike the *technique A* and *B*, this technique is based on the Fourier series of the pulses. Considering the symmetrical sampled unipolar PWM (i.e. the pulse is centered in $T_{sw}/2$ as a square waveform), the overall AC voltage, which is produced every carrier period, can be expressed in

$$v_{inv}(t) = \sum_{i=1}^K \left[D_i \cdot V_{dc,i} + \sum_{k=1}^{\infty} \frac{2V_{dc,i}}{k\pi} \cdot \sin(k\pi D_i) \cdot \cos(k\omega t + k\theta_i) \right] \quad (4.51)$$

where D_i is the duty ratio of the i^{th} cell. The *technique C* can completely eliminate the fundamental carrier harmonic group.

Considering $N = 3$, the sum of the fundamental carrier harmonic group can become null in case the following condition in (4.52) is satisfied.

$$\begin{cases} h_{11} + h_{12}\cos(\theta_2) + h_{13} \cdot \cos(\theta_3) = 0 \\ h_{12} \cdot \sin(\theta_2) + h_{13} \cdot \sin(\theta_3) = 0 \end{cases} \quad (4.52)$$

where

$$h_{ki} = \frac{2V_{dc,i}}{k\pi} \cdot \sin(k\pi D_i), \quad (4.53)$$

which is a coefficient for i^{th} cell and k^{th} harmonic order. Finally, the solution to (4.52) is derived as

$$\begin{cases} \cos(\theta_2) = \frac{1}{2} \left(\frac{-h_{11}^2 - h_{12}^2 + h_{13}^2}{h_{11}^2 h_{12}^2} \right) \\ \cos(\theta_3) = \frac{1}{2} \left(\frac{-h_{11}^2 + h_{12}^2 - h_{13}^2}{h_{11}^2 h_{13}^2} \right). \end{cases} \quad (4.54)$$

However, the valid angles, θ_2 and θ_3 , are obtained only when the following conditions in (4.55) are satisfied.

$$\begin{cases} |h_{11} - h_{12}| \leq h_{13} \leq h_{11} + h_{12} \\ |h_{11} - h_{13}| \leq h_{12} \leq h_{11} + h_{13} \end{cases} \quad (4.55)$$

4.4.2 Performance comparison of the three techniques

The performance of the three techniques is compared under three unbalanced operating conditions described in the below.

- Case I: $V_{dc,i} = [100; 80; 60]$ V and $M_i = [0.8; 0.8; 0.8]$
- Case II: $V_{dc,i} = [100; 100; 100]$ V and $M_i = [0.5; 0.7; 0.9]$
- Case III: $V_{dc,i} = [70; 50; 40]$ V and $M_i = [0.95; 0.9; 0.85]$

Case I: UNEQUAL DC-link voltages and EQUAL modulation signals

The symmetrical PSPWM cannot eliminate the first and second carrier harmonic group as shown in Fig. 4.60 (a) and presents the WTHD value of 0.0569 %. On the other hand, all three techniques completely cancel out the first carrier harmonic group, while the second carrier group is increasing as shown in Fig. 4.60 (b). Hence, these techniques achieve the reduced WTHD of 0.0447 %, namely, the WTHD is improved by 21.44 %. It is noticed that the carrier shift angles calculated by all three techniques are same, since they are equivalent

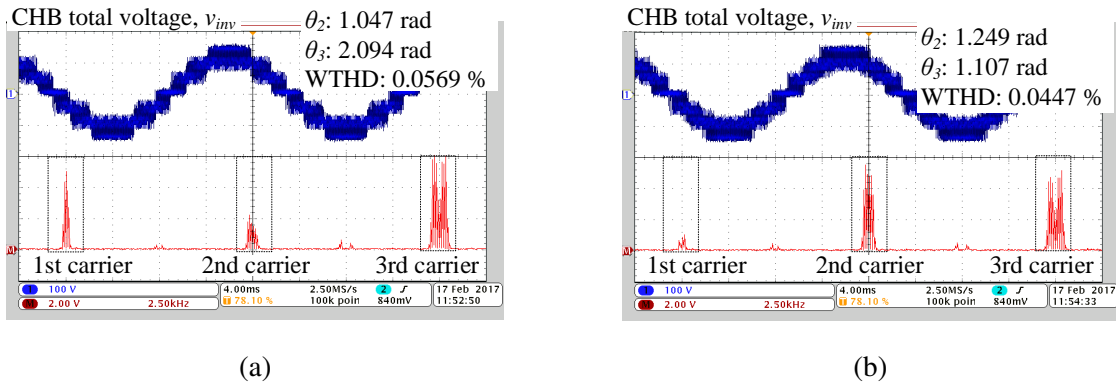


Figure 4.60: Multi-level AC voltage of CHB converter and its frequency spectrum under the operating condition of case 1: (a) symmetrical PSPWM, (b) technique A, B, and C.

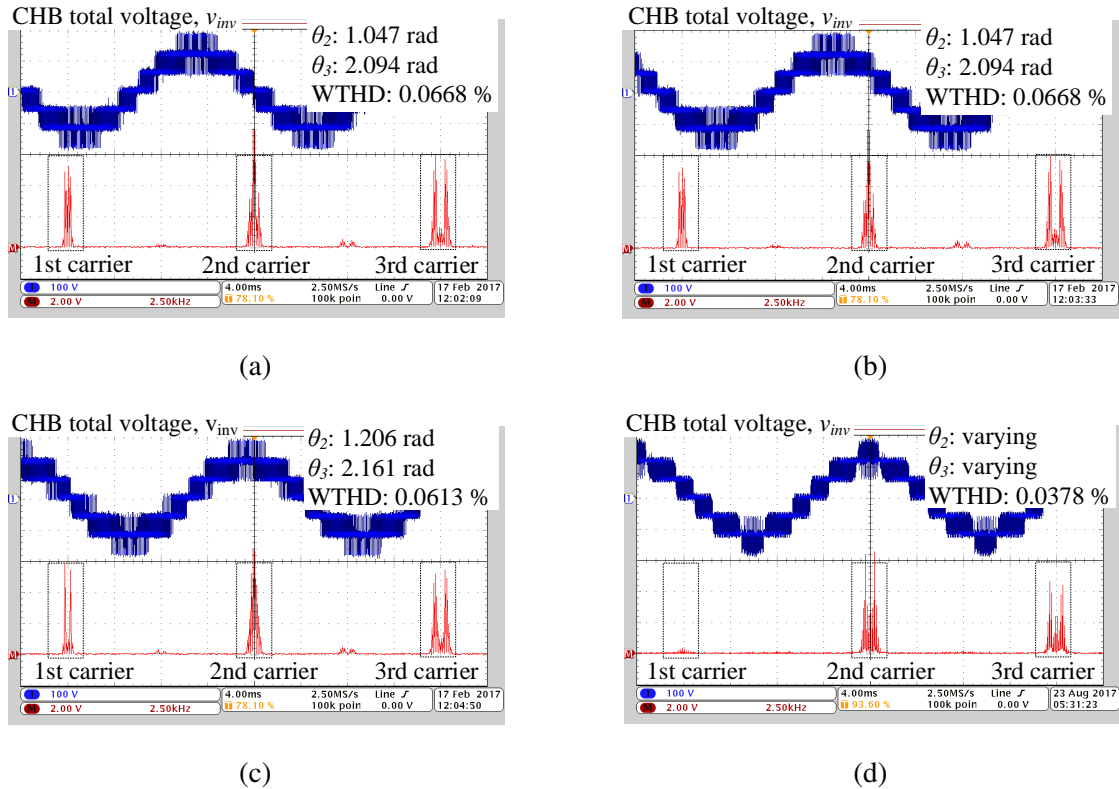


Figure 4.61: Multi-level AC voltage of CHB converter and its frequency spectrum under the operating condition of case 2: (a) symmetrical PSPWM, (b) technique A, (c) technique B and (d) technique C.

under this operating condition.

Case II: EQUAL DC-link voltages and UNEQUAL modulation signals

As shown in Fig. 4.61 (a), the symmetrical PSPWM presents the 0.0668 % WTHD value, showing the first and second carrier harmonic groups. In fact, since the *technique A* does not consider the unequal modulation signals, the phase shift angles and the WTHD value are same with the symmetrical PSPWM as shown in Fig. 4.61 (b). On the other hand, the *technique B* makes the main harmonics in the first carrier group, $2f_{sw} \pm 1$, to be compensated, resulting in the decreased WTHD to 0.0613 % (decreased by 8.23 %) as shown Fig. 4.61 (c). Under this operating condition, the *technique C* shows the best performance. The first carrier harmonics group is remarkably decreasing as shown in Fig. 4.61 (d), resulting in the 0.0378 % WTHD (decreased by 44 %).

Case III: UNEQUAL DC-link voltages and EQUAL modulation signals

The WTHD is 0.0479 % with the symmetrical PSPWM as shown in Fig. 4.62 (a), whereas the *technique A* improves the WTHD value to 0.044 % by diminishing the harmonics of the first carrier group as shown in Fig. 4.62 (b). Fig. 4.62 (c) shows the waveforms with the *technique B* that reduces effectively the harmonics of $2f_{sw} \pm 1$, resulting in the improved

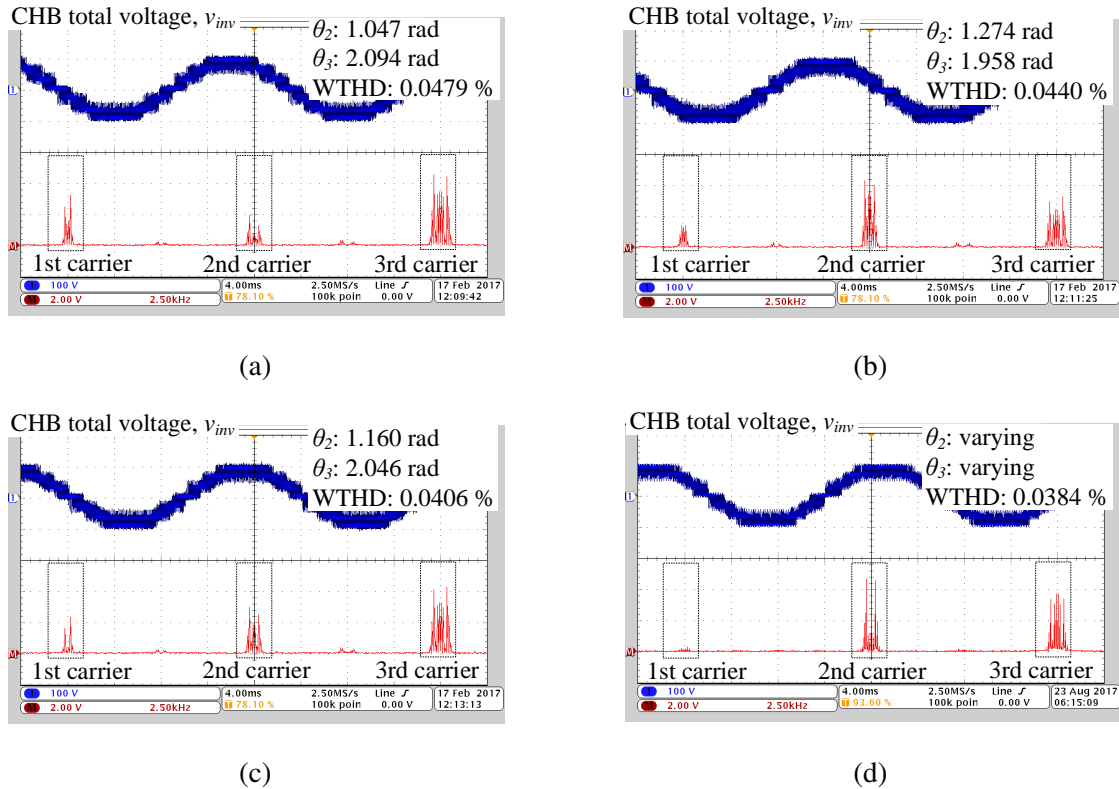


Figure 4.62: Multi-level AC voltage of CHB converter and its frequency spectrum under the operating condition of case 3: (a) symmetrical PSPWM, (b) technique A, (c) technique B and (d) technique C.

performance of 0.0406 %. The *technique C* allows the fundamental carrier harmonics to be completely compensated as shown in Fig. 4.62 (d), resulting in the 0.0384 % WTHD. All techniques can improve the WTHD performance compared to the symmetrical PSPWM technique. For the *technique A*, the WTHD is improved by 8.14 %, whereas for the *technique B* and *C*, it is improved by 15.24 % and 19.83 %, respectively.

On the other hand, the above conditions consider the constant DC-link voltage, but the DC-link voltage in single-phase converters inherently has the second-order harmonic, for example, 100 Hz for the grid-connected system. The influence of the harmonic on the performance of three techniques is investigated in Fig. 4.63, showing the frequency spectrum with the constant DC-link voltage (top) and with the second-order voltage (bottom), of which amplitude is 5 V, under the three unbalanced operating conditions.

For the case 1 (Fig. 4.63 (a)), focusing on the results with the second-order harmonic in the DC-link voltage, all techniques still manage to compensate the first-order carrier harmonics group, but their performance is diminished and the first-order group still exists. As shown in Fig. 4.63 (b) for the case 2, the *technique A* already loses the ability with the constant DC-link voltage. The main effect of the *technique B* is to cancel out the main side band harmonics (indicated with arrow). However, the components are not completely eliminated when the second-order harmonic is present in the DC-link voltage. On the other hand, the *technique C* shows a similar performance in both cases. For case 3, the *technique A* is not

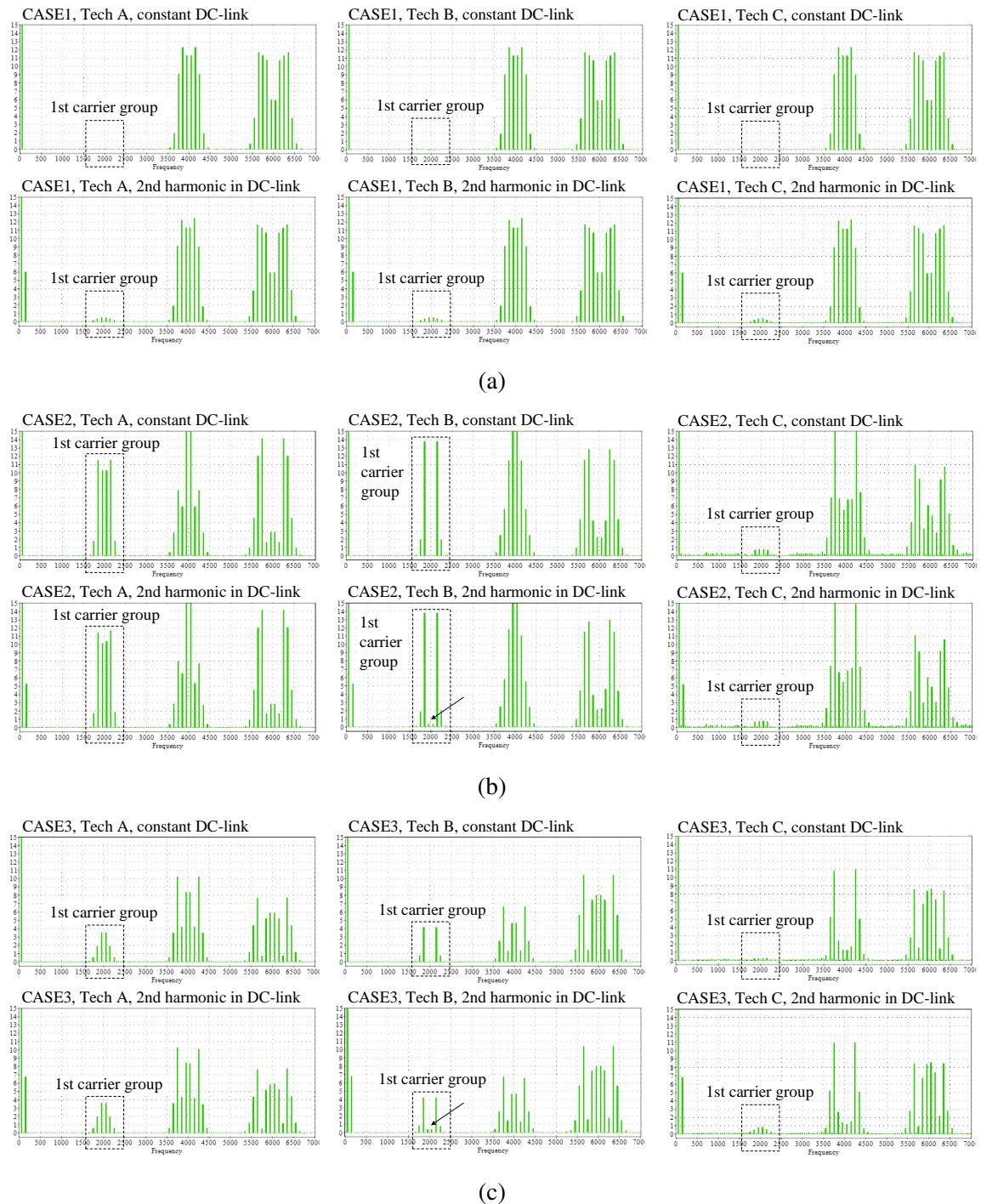


Figure 4.63: Frequency spectrum of CHB output voltage produced by the three considered techniques in case of (a) unequal DC voltages and equal modulating signals (case 1), (b) equal DC voltages and unequal modulating signals (case 2) and (c) unequal DC voltages and unequal modulating signals (case 3) without the second-order harmonic (top) and with the second-order harmonic on DC-link voltage (bottom).

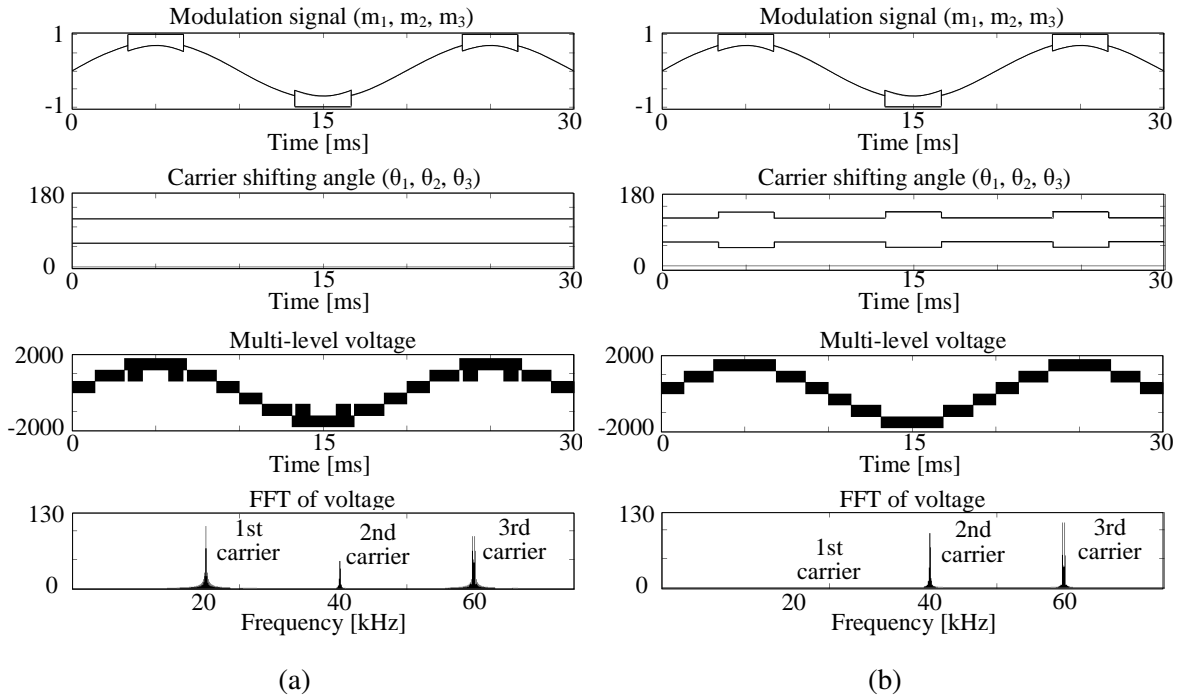


Figure 4.64: Analysis of frequency spectrum by (a) symmetric carrier phase angle and (b) proposed variable-carrier phase angle, with the discontinuous modulation when the clamping angle is 60° .

effective similar to the case 2, whereas the performance of *technique B* and *C* decreases due to the second-order harmonics, showing harmonics belonging to the first-order carrier group as shown in Fig. 4.63 (c).

4.4.3 Variable-carrier angle phase-shifted modulation for the discontinuous active thermal control method

The proposed discontinuous modulation in the previous section inherently features the unbalanced operating condition as exploiting different modulation signals for each cell. Further, it has been shown in Fig. 4.31, that the power quality is decreasing. A new variable-carrier angle phase-shifted modulation is proposed, which is applicable to the discontinuous method. In fact, the phase shift angles are calculated based on the *technique C*, because the discontinuous modulation signals are not sinusoidal. Namely, the instantaneous modulation signal, D , should be considered instead of the modulation index, M , in the *technique A* and *B*.

Considering three cascaded cells, it is assumed that one cell of them is additionally load- ing and the DC-link voltages are equal as a case study. In Fig. 4.64, the modulation signal for each cell, carrier shifting angles, AC voltage of the CHB converter and its frequency spectrum are shown, when the clamping angle is 60° . With the typical symmetric carrier phase angles, $[\theta_1, \theta_2, \theta_3]=[0^\circ, 60^\circ, 120^\circ]$, the first and second carrier harmonic groups appear due to the clamping regions as shown in Fig. 4.64 (a). On the other hand, the effect of the variable-carrier phase angle is identified in Fig. 4.64 (b), in which θ_1 is fixed

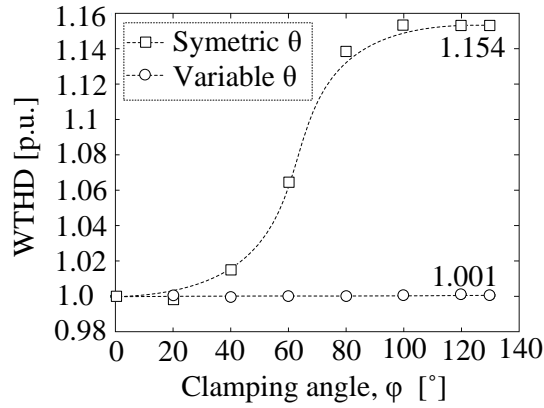


Figure 4.65: Effect of the variable-carrier angle method with the discontinuous modulation on the WTHD performance.

at 0° , θ_2 is varied between 60° and 45° and θ_3 is altered between 120° and 135° ($[\theta_1, \theta_2, \theta_3] = [0^\circ; 60^\circ; 120^\circ] \leftrightarrow [0^\circ; 45^\circ; 135^\circ]$). Since only 2-cells are switching within the clamping regions, the modified carrier phase angles allow that the first carrier harmonic group is completely compensated.

The effect of the variable-carrier angle method on the WTHD performance is shown in Fig. 4.65, where the value is normalized by that with 0° clamping angle. As the clamping angle is increasing, the WTHD is worse with the symmetric angle method and it is increased by 15.4 % with the clamping angle of 130° . On the other hand, the WTHD is almost unaffected by the clamping angle, when the variable-carrier angle method is applied. As it is seen, only 0.1 % is increased with the 130° clamping angle.

4.5 Summary

This section has proposed the active thermal control methods for power semiconductors in the modular converters, which are defined as a system with a different aged cell.

The two approaches based on the modulator level have been considered. The first approach is the power routing that enables the unequally distributed power loading on purpose among different paths connected in parallel. The multi-frequency modulation has been proposed, which improves the power imbalance capability by 15.5 % compared with the typical sinusoidal modulation, resulting in the higher number of deactivated cells (around 1.5 times). However, the multi-frequency method limits to address the reliability of the whole system. This issue has been addressed with the discontinuous modulation that enables to serve the power routing with modifying the loss distribution of CHB converter cells. The power imbalance capability cannot be only improved by around 5 % compared with the multi-frequency modulation but also the losses of CHB converter can be reduced remarkably. Considering the fluctuating mission profile and the 60° clamping angle, it has been demonstrated that the accumulated damage of the clamped cell can be reduced by more than 90 % and 30 % reduction in the non-clamped cell. On the other hand, the unloaded DC/DC converter has a damage reduction of 1/300, while the additional loading is increasing the damage 14 times.

The variable-clamping angle discontinuous modulation has been introduced, which targets to improve the CHB converter's reliability. The clamping angle is exploited as a control variables to modify the generated losses and it has been demonstrated that the thermal cycling caused by a fluctuating power profile can be completely compensated. Through the capability analysis for the maximum number of thermally compensated cells, it has been revealed that a lower DC-link voltage is beneficial. Considering an extremely fluctuating profile, the proposed method can reduce the accumulated damage to 1 % compared with the typical sinusoidal modulation. Also, it has been validated that the variable-clamping angle discontinuous modulation is applicable to the parallel converters.

Finally, the influence of the proposed active thermal control methods on the power quality has been addressed with the variable-carrier angle phase-shifted modulation. The three existing techniques have been reviewed and compared under different unbalanced conditions. Based on this, the variable-carrier angle method for the discontinuous modulation has been proposed and it has been identified that the WTHD performance can be improved by completely eliminating the first carrier harmonic group.

5 Reliability of Capacitors

Capacitors are essentially employed for DC-link in all of voltage source converters such as DC/DC, AC/DC, DC/AC and AC/DC/AC, in order to maintain a stable voltage, to balance the instantaneous power between input and output ports and to decouple different converters in a system [147]. Three types of capacitors listed in the below are widely used, which feature different characteristics for electrical and mechanical specifications, cost efficiency and reliability.

- Aluminum Electrolytic Capacitor (Al-Cap)
- Metalized Polypropylene Film Capacitor (MPPF-Cap)
- Multi-Layer Ceramic Capacitor (MLC-Cap)

The performance of each type is comprehensively compared in Fig. 5.1, in terms of electrical, thermal and economical properties: cost, capacitance, rated voltage, rated ripple current, maximum core temperature, energy density (i.e. capacitance per volume), Equivalent Series Resistance (ESR), capacitor stability. One of the most attractive properties for the Al-Caps is a high capacitance at a relatively low cost, allowing a higher energy density (see Fig. 5.1 (a)). This characteristic is from the high dielectric strength and thinness ($\approx 0.01\mu\text{m}$) of the aluminum oxide dielectric layer [148]. In addition, the high capacitance-voltage rating (220000 μF -600 V) and operating temperature encourage the Al-Caps to be widely applied in various applications. On the other hand, the major drawback of the Al-Caps is a shorter life, which is limited by temperature variation sensitivity due to electrolyte evaporation. This leads to the capacitance variation from -40 % to +5 % for temperature changes from -40°C to 105°C with variation of conductivity and viscosity. This performance degradation is also referred as the increased ESR and reduced rated ripple current capability.

The MPPF-Caps are remarkable for the lowest ESR, which leads to the highest ripple current capability as shown in Fig. 5.1 (b). Therefore, they facilitate for applications suffering from high DC-link ripple current such as a Switched Reluctance Machine (SRM)

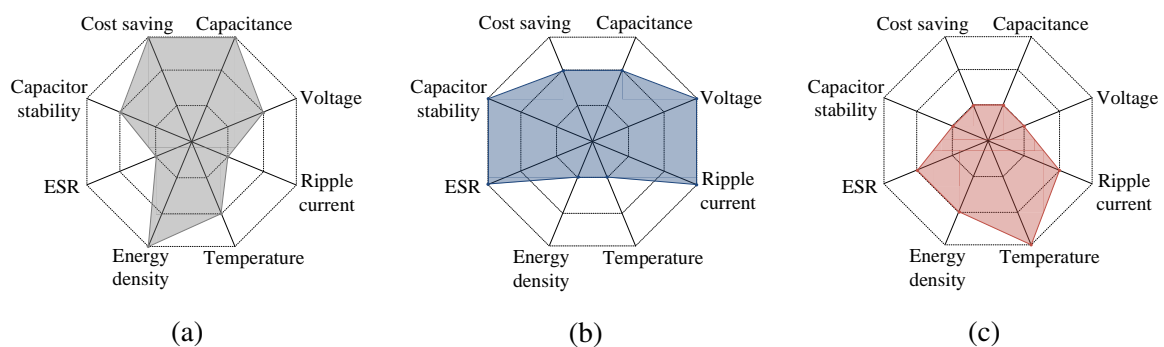


Figure 5.1: Performance comparison of three types of capacitor for DC-link applications: (a) Al-Caps, (b) MPPF-Caps and (c) MLC-Caps (inner: inferior, middle: intermediate, outer: superior) [147].

drive [148]. Furthermore, they have the highest rated voltage and capacitor stability under a wide environmental changes, because they are structured based on solid metal with the self-healing characteristic. However, the lowest energy density and moderate capacitance limit the MPPF-Caps to be employed for the high power applications, leading to a bulky DC-link design with increased cost to meet the energy storage and capacitance requirement.

As shown in Fig. 5.1 (c), the MLC-Caps show superior performance for the operating temperature and it is over 200°C by the customized component [149], making them attractive for high temperature applications such as aerospace. Moreover, they have high potential to achieve compactness with high dielectric strength (up to 400000) [148]. The performance for the ripple current and ESR is intermediate. However, their use is restricted by the expense of precious metal for electrodes and especially, they are suffered from the lowest rated voltage and capacitance for high power and high voltage applications.

5.1 Discussion of Selected Failure Mechanism

It is well known that DC-link capacitors are one of the most frequent failure components in power converter systems. Moreover, nowadays, the emerging industry fields such as renewable systems, aerospace and automobile are pushing the strict constraint of the DC-link design on its volume to achieve the trends for high power density. Consequently, this brings to challenges for the capacitors to be exposed under more harsh environments such as high ambient temperature and high humidity. Therefore, the reliability issue is received higher attention and thus, it needs to investigate the major root-cause of failures as a starting point.

The primary cause of the Al-Caps' degradation is the electrolyte evaporation, which is mainly caused by additional internal heating. The internal heating is generated by capacitor current, i_C , and ESR with limited heat dissipation and ambient temperature, T_a . Once the volume of the electrolyte is reduced, the ESR is increasing and the capacitance is decreasing, which causes increased internal power losses. Finally, the core temperature is further increasing and the degradation is accelerated [150]. This procedure is shown in Fig. 5.2 (a).

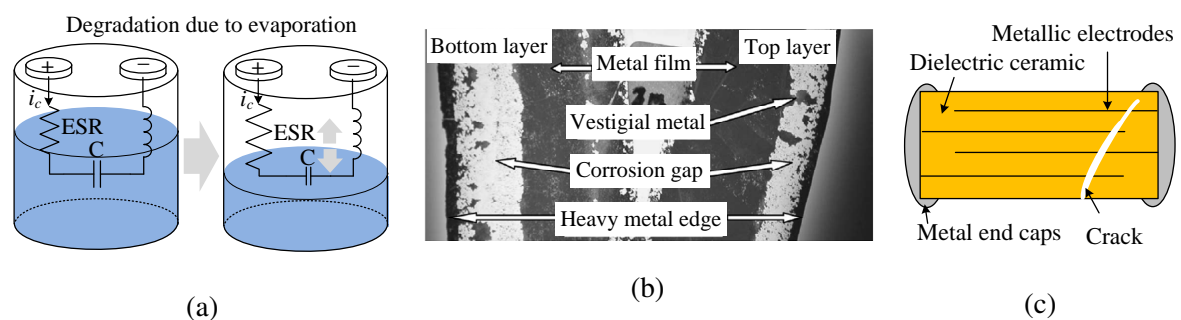


Figure 5.2: Selected failure mechanism: (a) electrolyte evaporation for Al-Caps, (b) corrosion for MPPF-Caps [150] and (c) insulation degradation due to cracking for MLC-Caps.

Table 5.1: Failure mechanisms and critical stressors [147].

Capacitor type	Failure mechanisms	Critical stressors
Al-Caps	Self-healing dielectric breakdown	V_C, T_a, i_C
	Disconnection of terminals	Vibration
	Dielectric breakdown of oxide layer	V_C, T_a, i_C
	Electrolyte vaporization (wear-out)	T_a, i_C
	Electrochemical reaction (wear-out)	V_C
MPPF-Caps	Self-healing dielectric breakdown	$V_C, T_a, dV_C/dt$
	Connection instability by heat contraction of a dielectric film	T_a, i_C
	Reduction in electrode area caused by oxidation of evaporated metal due to moisture absorption	Humidity
	Dielectric film breakdown	$V_C, dV_C/dt$
	Self-healing due to over-current	T_a, i_C
	Moisture absorption of by film	Humidity
	Dielectric loss (wear-out)	$V_C, \text{humidity}, T_a, i_C$
MLC-Caps	Dielectric breakdown	V_C, T_a, i_C
	Cracking; damage to capacitor body	Vibration
	Insulation degradation, micro-crack in ceramic (wear-out)	$V_C, T_a, i_C, \text{vibration}$

For the MPPF-Caps, the dielectric loss with corrosion is the major failure mechanism as shown Fig. 5.2 (b), where the humidity is mainly responsible together with the ambient temperature, applied voltage and ripple current. This is because thin metalized layer (typically less than 100 nm) is vulnerable to the corrosion by penetrated moisture through a mechanical tear and wear of casing. In [151], it was revealed that corrosion is further advanced at the outer layers than the inner layers, which results in the separation of metalized film from heavy edge and consequently, the reduction of capacitance. Another failure mechanism is the self-healing dielectric breakdown, which is occurred due to over-voltage at local weak points. Their self-healing capability recovers the full ability except for a slight reduction of capacitance, if the dielectric breakdown is occurred at local weak point. However, as the weak points are increasing, the capacitance gradually decreases until the end of life.

The major degradation of the MLC-Caps is the insulation capability reduction caused by the decreased thickness of the dielectric layers and/or the cracked ceramic as shown in Fig. 5.2 (c). Once the degradation of insulation is initiated, a high leakage current is caused by a high voltage and the failure mechanism is accelerated with the effect of the avalanche breakdown, causing thermal runs away rapidly.

The selected failure mechanisms for each type are summarized in Table 5.1, highlighting the wear-out failures in bold. There are two wear-out failures for the Al-Caps, electrolyte vaporization and electrochemical reaction. The electrolyte vaporization is caused by the

thermal stresses, whereas the applied voltage is responsible for the electrochemical reaction. Further, It should be remarked that the primary causes for the most of failure mechanisms are the electrical stresses of V_C and i_C and the ambient temperature. For the MPPF-Caps, the dielectric loss is the major mechanism, which is initiated by penetrated moisture (humidity) and accelerated by the electrical stress, V_C and i_C . As it can be recognized, unlike the Al-Caps, the humidity is highly responsible for most of failure mechanisms of MPPF-Caps, while the electrical stresses partly contribute. The MLC-Caps are degraded by the insulation degradation due to micro-crack in ceramic layers, which could be caused by mechanical stress (vibration) or/and electrical stress (V_C and i_C). The mechanical stress is further critical than the electrical stresses. However, the electrical stresses are still partly responsible for most of failures.

5.2 Lifetime Considerations for Electrolytic Capacitors

Electrolytic capacitor is widely employed in the DC-link applications to take its attractive feature of the high power density at lower cost compared with other capacitors. However, the electrolytic capacitor suffers from the short lifetime due to the electrolyte evaporation caused by thermal stresses. Consequently, it is motivated to derive a clear correlation between the capacitor current and the thermal stresses. In this section, the equivalent model of the electrolytic capacitor is briefly introduced, followed by a discussion about the lifetime model to highlight the influence of capacitor current on the lifetime. Then, the capacitor test setup is proposed, which aims at investigating a relation between the ripple current frequency and the hot-spot temperature.

5.2.1 Aluminum Electrolytic Capacitor

The aluminum electrolytic capacitor is typically constructed with two aluminum electrodes, which are separated by a paper impregnated with ethylene glycol. The surface of the anode and cathode electrodes is then electrochemically formed with an oxide layer (Al_2O_3) to serve as the dielectric material. Finally, these two electrodes are etched and wound into a cylindrical shape and therefore, enabling the large capacitance per volume characteristic [152].

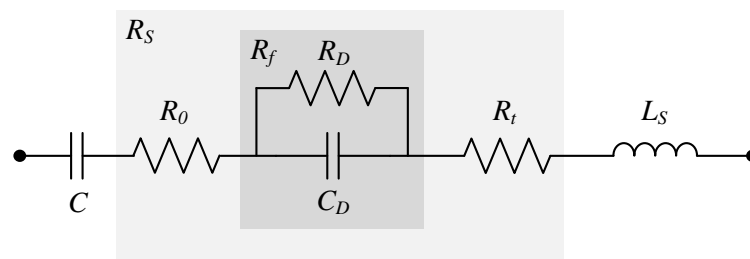


Figure 5.3: Simplified equivalent model of the electrolytic capacitor.

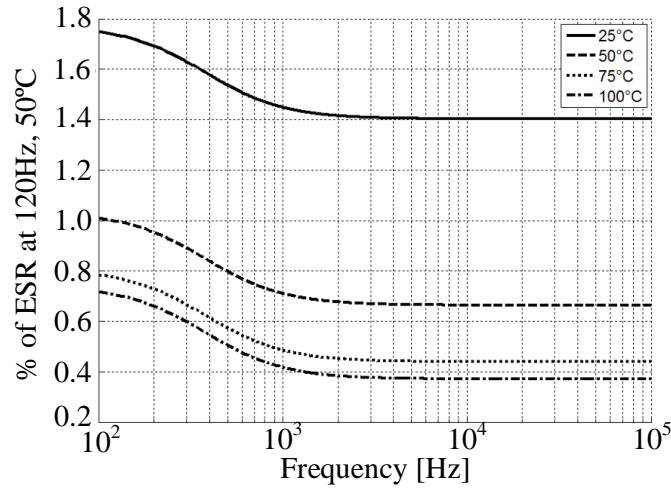


Figure 5.4: ESR curve as a function of frequency and temperature [153].

Based on this structure, the electrolytic capacitor can be simply modeled as a combination of capacitors, a resistor and an inductor as shown in Fig. 5.3, where C is the capacitance, R_S is the Equivalent Series Resistance (ESR) and L_S is the Equivalent Series Inductance (ESL) that is due to the wound structure [153]. Here, it should be mentioned that the ESL is neglected in the following analysis with the assumption that the capacitor is operated below its resonance frequency. Therefore, only the ESR represents the real part of the capacitor's impedance, which can be decomposed into three parts as

$$R_S = R_0 + R_f + R_t \quad (5.1)$$

where R_0 is the combined constant resistance of terminals, tabs and foils, R_f represents the frequency-dependent resistance of the dielectric layer, which is composed by C_D and R_D that account for the losses caused by the dielectric, and R_t is the temperature-dependent part due to the characteristics of the employed electrolyte [147, 153]. Further, the conductivity increases as temperature is increasing since the viscosity of the electrolyte varies, leading to a reduction in ESR due to R_t . This effect can be modeled by

$$R_t = R_{t,b}(T_b) \cdot e^{\frac{T_b - T_s}{SF}} \quad (5.2)$$

where $R_{t,b}$ is R_t at base temperature T_b , T_s is the hotspot temperature of the capacitor, and SF denotes a capacitor dependent temperature sensitivity factor [153]. In Fig. 5.4, the ESR is plotted as a function of the frequency for different temperatures in accordance to [153]. As discussed before, it can be seen that the ESR decreases as temperature increases. Moreover, it can be noted that increasing frequencies also lead to a decrease in ESR due to R_f .

5.2.2 Impact of capacitor current on lifetime

For the capacitor's lifetime estimation, the empirical lifetime models have been mostly employed [17]. The model is described in (5.3), which considers the influence of the operating temperature and applied voltage as major stressors.

$$L = L_0 \cdot \left(\frac{V_a}{V_0} \right)^{-m} \cdot \exp \left[\left(\frac{E_a}{K_B} \right) \cdot \left(\frac{1}{T} - \frac{1}{T_0} \right) \right] \quad (5.3)$$

where L_0 denotes the lifetime at nominal values as given in the manufacturer's datasheets, V_0 and V_a are the nominal voltage and the applied voltage, respectively, m accounts for the manufacturer dependent voltage factor, E_a is the activation energy, K_B is the Boltzmann's constant (8.62×10^{-5} eV/K), and T_0 and T are the temperature in Kelvin at test condition in the datasheets and at operation, respectively. Hence, it is essential to monitor the hot-spot temperature inside the capacitor for the lifetime estimation, which can be derived by a summation of the ambient temperature and the additional heating due to power dissipation as

$$T = T_a + \Delta T = T_a + P_{pd} \cdot R_{th} \quad (5.4)$$

where T_a denotes the ambient temperature, ΔT is the additional heating caused by the power dissipation P_{pd} and the thermal resistance from hot-spot to ambient of the capacitor R_{th} . Furthermore, the power dissipation is mainly caused by the capacitor current, I_C , and the ESR, R_{ESR} , as presented in

$$P_{pd} = I_C^2 \cdot R_{ESR}. \quad (5.5)$$

However, the capacitor current in the DC-link applications is a superimposition of harmonics and the ESR exhibits a frequency dependent behavior, leading to a necessary for the knowledge of the capacitor current at the corresponding frequencies for the correct calculation of the power dissipation [154, 155]. Therefore, by knowing the capacitor current harmonics with a spectral analysis, the power dissipation can be calculated by

$$P_{pd} = \sum_{i=1}^n I_{C,i}^2 \cdot R_{ESR,i} \quad (5.6)$$

where $I_{C,i}$ and $R_{ESR,i}$ denote the ripple current and the ESR at frequency harmonic i , respectively, with $i = 1, 2, \dots, n$.

To conclude, the capacitor current in the DC-link applications with the power converters is a combination of harmonics components, while the ESR is varied in according to the frequency as shown in Fig. 5.4. Therefore, it is of interest to experimentally verify the influence of the ripple current frequency on the hot-spot temperature that highly affects the lifetime as expressed in (5.3).

5.3 Developed Power Converter for Capacitor Test

The idea, which is for verifying the influence of the capacitor current on the hot-spot temperature, is to individuate via simulations the capacitor current spectrum and to reproduce them with the capacitor test setup. For this purpose, the parallel modular converter shown in Fig. 5.5 is considered, which is for Wind Turbine (WT) application as a case study.

The actual current profile in the DC-link capacitor is analyzed based on the previous studies in [155, 156, 157], considering one cell of paralleled cells. The capacitor current, $i_{link,c}$, can be calculated by the subtraction between the machine-side current, $i_{link,m}$, and the grid-side current, $i_{link,g}$, as expressed in

$$i_{link,c}(t) = i_{link,m}(t) - i_{link,g}(t) \quad (5.7)$$

where the subscript c denotes the capacitor-side, the subscript m is the machine-side and the subscript g is the grid-side. Referring [156], the capacitor current can be mathematically expressed in (5.8). The derivation of machine- and grid-side current equations is also presented in appendix 9.1.3.

$$\begin{aligned}
i_{link,c}(t) = & \sum_{\eta=1}^3 \frac{I_m}{2} \cdot \cos(\omega_m t + \phi_{\eta,m} - \phi_{0,m}) + \\
& \frac{2}{\pi} \cdot \sum_{n=1}^{\infty} \frac{1}{n \left(\frac{\omega_m}{\omega_{sw}}\right)} \cdot J_n \left(n \left(\frac{\omega_m}{\omega_{sw}} \right) \frac{\pi}{2} m_{a,m} \right) \cdot \sin \left(n \frac{\pi}{2} \right) \cdot \cos(n(\omega_m t + \phi_{pwm,m})) \\
& + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \frac{1}{m} \cdot J_0 \left(m \frac{\pi}{2} m_{a,m} \right) \cdot \sin \left(m \frac{\pi}{2} \right) \cdot \cos(m(\omega_{sw} t + \phi_{pwm,m})) \\
& + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{q} \cdot J_n \left(q \frac{\pi}{2} m_{a,m} \right) \cdot \sin \left((m+n) \frac{\pi}{2} \right) \cdot \cos(m(\omega_{sw} t + \phi_{pwm,m}) + n(\omega_m t + \phi_m)) \\
& - \sum_{\eta=1}^3 \frac{I_g}{2} \cdot \cos(\omega_g t + \phi_{\eta,g} - \phi_{0,g}) \\
& + \frac{2}{\pi} \cdot \sum_{n=1}^{\infty} \frac{1}{n \left(\frac{\omega_g}{\omega_{sw}}\right)} \cdot J_n \left(n \left(\frac{\omega_g}{\omega_{sw}} \right) \frac{\pi}{2} m_{a,g} \right) \cdot \sin \left(n \frac{\pi}{2} \right) \cdot \cos(n(\omega_g t + \phi_{pwm,g})) \\
& + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \frac{1}{m} \cdot J_0 \left(m \frac{\pi}{2} m_{a,g} \right) \cdot \sin \left(m \frac{\pi}{2} \right) \cdot \cos(m(\omega_{sw} t + \phi_{pwm,g})) \\
& + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{q} \cdot J_n \left(q \frac{\pi}{2} m_{a,g} \right) \cdot \sin \left((m+n) \frac{\pi}{2} \right) \cdot \cos(m(\omega_{sw} t + \phi_{pwm,g}) + n(\omega_g t + \phi_g))
\end{aligned} \quad (5.8)$$

Based on (5.8), the three currents, $i_{link,m}$, $i_{link,g}$ and $i_{link,c}$, of 2 MW WT are simulated under four different operating points. The specification of the system and the operation points are described in appendix 9.1.4. Further, it is assumed that the carriers of machine- and grid-side converters are synchronized to cancel out the first-order carrier harmonics in the capacitor. The power factor of the machine-side is set to 0.98, since no magnetizing current needs to

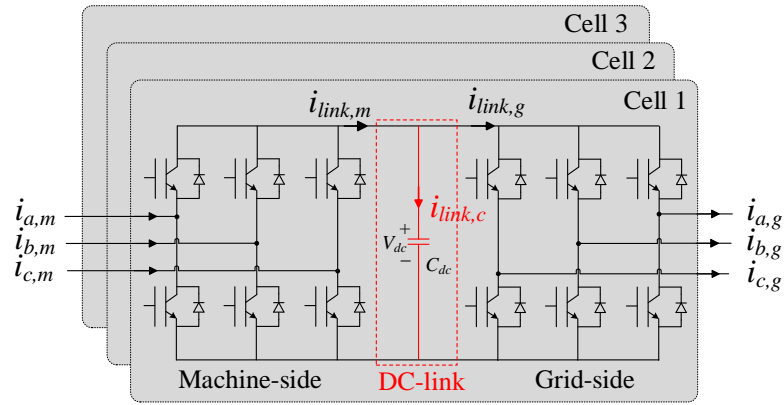


Figure 5.5: Parallel modular converter for the analysis of DC-link current spectrum.

be provided to Permanent Magnet Synchronous Generator (PMSG) [158, 159]. The current waveforms of the machine-, grid-, and capacitor-side are shown in Fig. 5.6, along with their harmonic spectrum. Focusing on the harmonic spectrum, while the machine- and grid-side current contain both low-order harmonics and high-order harmonics as shown in Figs. 5.6 (a) and (b), it can be observed that the harmonics of the capacitor-side current are dominantly distributed at high order harmonics as shown in Fig. 5.6 (c).

On the other hand, the power factor of the grid-side could be controlled within a defined boundary by the German grid code [111, 160]. Following the definition of variant 1, the boundary of the power factor angle in the grid-side, which is presented in (5.9), is considered.

$$\begin{aligned}
 -48.99^\circ \leq \varphi_{0,g} \leq 67.38^\circ \\
 (-0.54 \leq PF \leq 0.25)
 \end{aligned}
 \tag{5.9}$$

In Fig. 5.7, the harmonics variation of the capacitor current is shown in accordance with the operating point (generated power) and the power factor of the grid-side. The harmonics amplitude accordingly increases by the increased power as shown in Fig. 5.7 (a). Fig. 5.7 (b) shows the influence of the power factor on the capacitor-side current spectrum, the side-band harmonics are increased with the lower power factor. As a conclusion, the high order harmonics of around $a \cdot f_s$ mainly affects the lifetime of DC-link capacitors, where f_s is the switching frequency and a is the integer.

The power converter for the capacitor test should aim at injecting a single sinusoidal current at the high frequency range to a Capacitor Under Test (CUT). Two possible converters: H-Bridge (HB) and Cascaded H-Bridge (CHB) shown in Fig. 5.8, are discussed in terms of structure complexity, Total Harmonic Distortion (THD), filter size, and required source voltage. The major challenge is to achieve the given test requirements of the high frequency sinusoidal currents with a low THD and the high DC bias voltage on the CUT. Here, it should be mentioned that the low THD is beneficial to further clear correlation between the

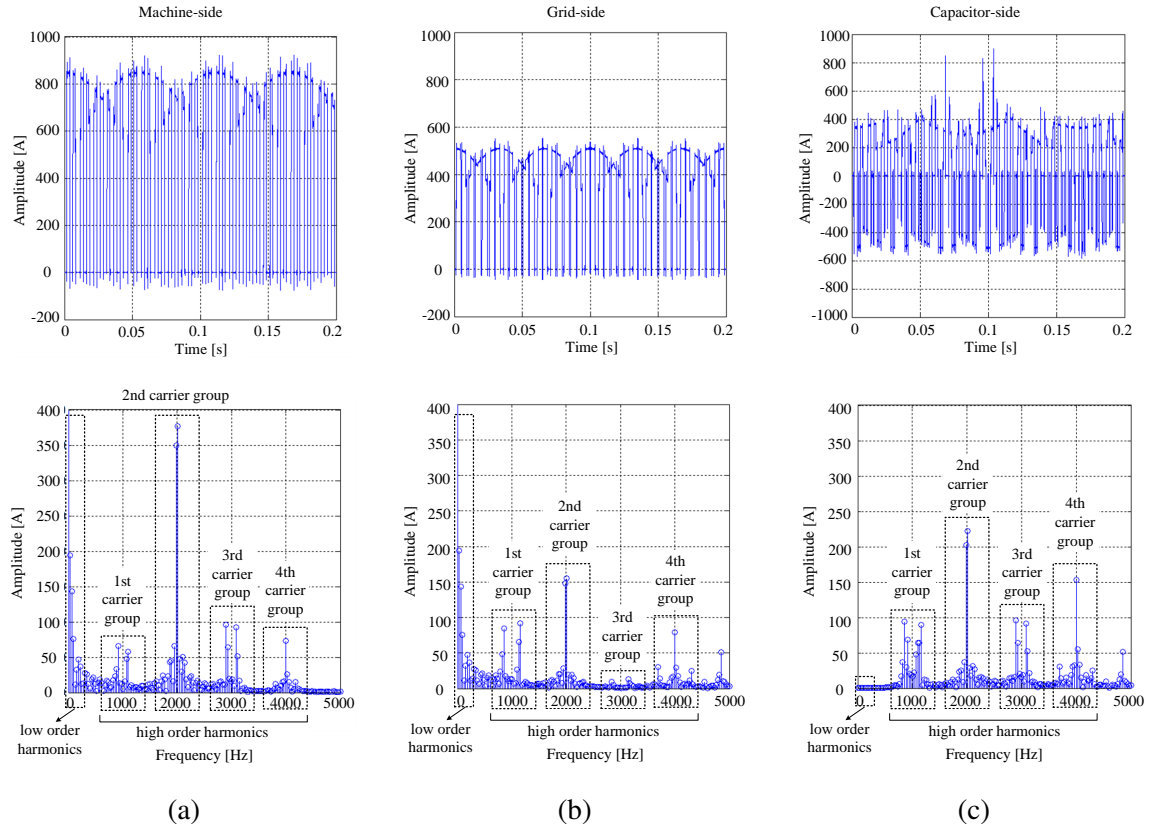


Figure 5.6: Simulated current waveform and its harmonic spectrum in (a) machine-side, (b) grid-side, and (c) capacitor under operating point no. 2 of Table 9.3 in appendix 9.1.3.

frequency and the temperature variation. The HB converter in Fig. 5.8 (a) is considered for the system complexity point of view, because this can be realized with one-third less number of power devices and voltage sources in comparison with the CHB converter. On the other hand, the CHB converter in Fig. 5.8 (b) is composed of three H-Bridge cells connected in series. The cascaded structure allows the multilevel output voltage and the three times lower source voltage for each cell. In addition, the six times higher equivalent switching frequency can be achieved with the phase shifted modulation. These features make the filter inductance to be reduced (by multilevel voltage and high equivalent switching frequency) and the commercially available switching devices to be acceptable to generate the high DC bias voltage on the CUT (by lower source voltage for each cell). Consequently, although the HB topology is much simple and the less number of devices are used, the advantages of the CHB converter cannot be matched by the HB converter.

The THD performance of each converter is evaluated by a mathematically derived equation, which is a function of the filter inductance and the switching frequency. The DC bias voltage of the CUT, $V_{C,dc}$, can be defined by

$$V_{C,dc} = 6 \cdot V_S \cdot (M - 0.5) \quad (5.10)$$

where the V_S is the source voltage and the M presents the modulation index whose range is

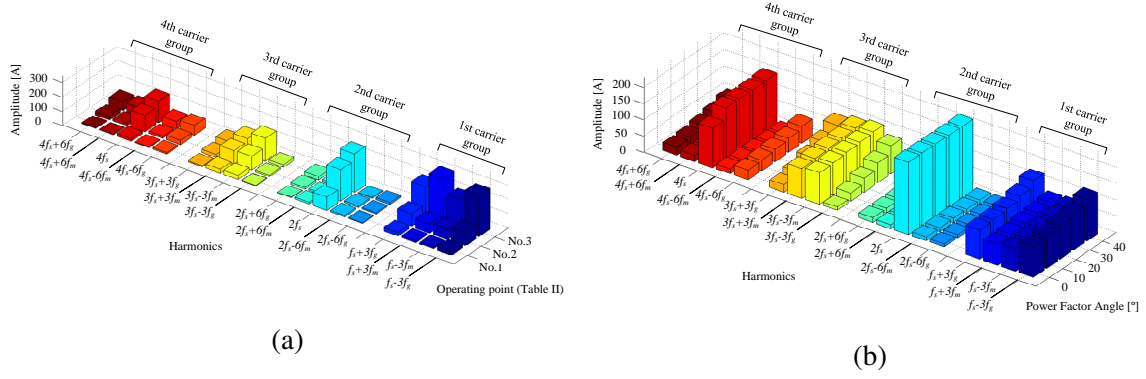


Figure 5.7: Harmonics distribution of DC-link capacitor current depending on (a) generated power and (b) power factor angle of grid-side.

from zero to one. The voltage drop across the filter inductor, V_L , is determined by a relation between V_S and $V_{C,dc}$ as expressed in

$$V_L = 3 \cdot V_S - V_{C,dc} \quad (5.11)$$

Then, the switching ripple current of each converter is given in

$$\Delta I_L = \frac{3 \cdot V_L \cdot M}{L \cdot f_S} \quad (\text{for HB}) \quad (5.12)$$

$$\Delta I_L = \frac{V_L \cdot M}{L \cdot f_S} \quad (\text{for CHB})$$

where the L is the filter inductance and the f_S denotes the device switching frequency.

By substituting (5.10) and (5.11) into (5.12), the switching ripple current can be defined as a function of L , f_S , and M in (5.13), assuming that the V_S is constant.

$$\Delta I_L(L, f_S, M) = \frac{3 \cdot V_S \cdot (1 - M) \cdot M}{L \cdot f_S} \quad (\text{for HB}) \quad (5.13)$$

$$\Delta I_L(L, f_S, M) = \frac{V_S \cdot (1 - M) \cdot M}{L \cdot f_S} \quad (\text{for CHB})$$

Consequently, the THD can be determined by

$$THD = \frac{\Delta I_L(L, f_S, M)}{|i_{C,ac}|} \quad (5.14)$$

The THD of each converter is shown in Fig. 5.9 as a function of the filter inductance with different switching frequencies, where the M is fixed to 0.5 for the simplicity. In order to

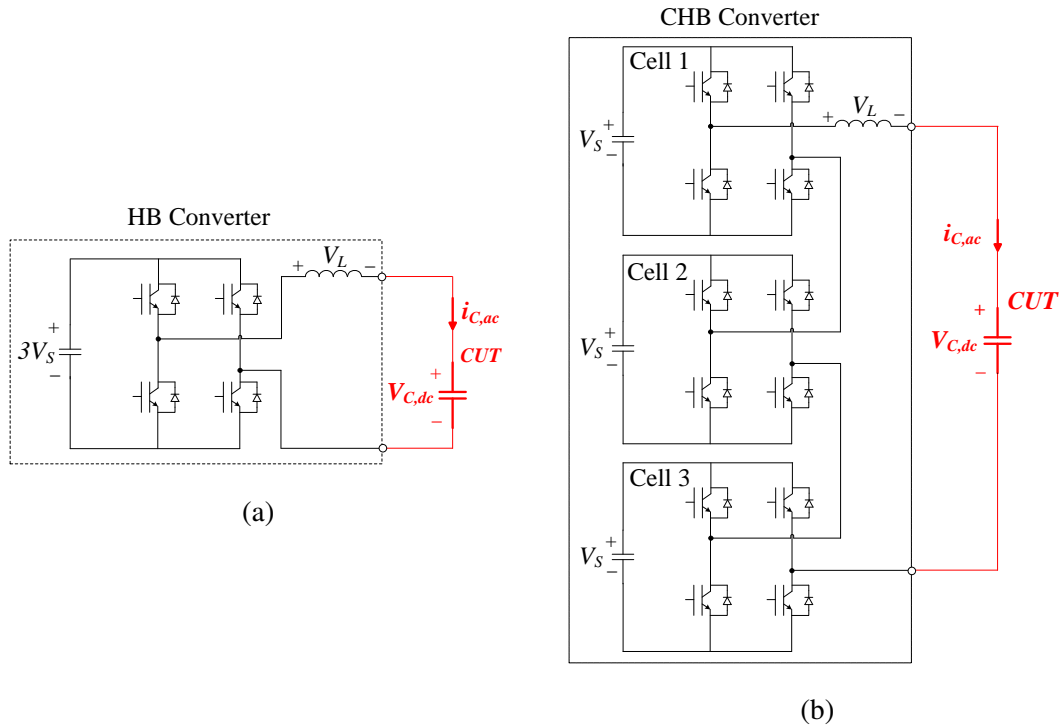


Figure 5.8: Possible converters for capacitor test: (a) HB and (b) CHB converter.

achieve the same THD performance with the HB, either a bigger filter inductance or a higher switching frequency needs to be chosen. However, the bigger filter inductance leads to a lower effective DC bias voltage on the CUT due to a higher voltage drop across the filter, which implies a higher source voltage to be required. Even if the filter inductance is reduced by employing the higher switching frequency, this could be limited by the commercially available power devices. The relation between the total source voltage and the voltage drop on the filter inductor is presented in (5.15), and this should be satisfied in order to provide the $i_{C,ac}$ in combination with the $V_{C,dc}$.

$$V_S \geq V_{C,dc} + 2 \cdot \pi \cdot f_{Ic} \cdot L \cdot i_{C,ac} \quad (5.15)$$

where f_{Ic} denotes the fundamental frequency of $i_{C,ac}$.

Based on this analysis, it is concluded that the CHB converter is the reasonable solution for this purpose and its advantages are summarized in the below.

- Better THD performance
- Lower filter inductance and size
- Slower switching frequency
- Lower source voltage
- Lower block voltage of the power devices

In the control point of view, a challenge is that the sinusoidal current, $i_{C,ac}$, and the DC bias voltage, $V_{C,dc}$, on the CUT should be simultaneously controlled. This can be performed by the proposed parallel control strategy shown in Fig. 5.10 (a). As shown in Fig. 5.10 (b), the

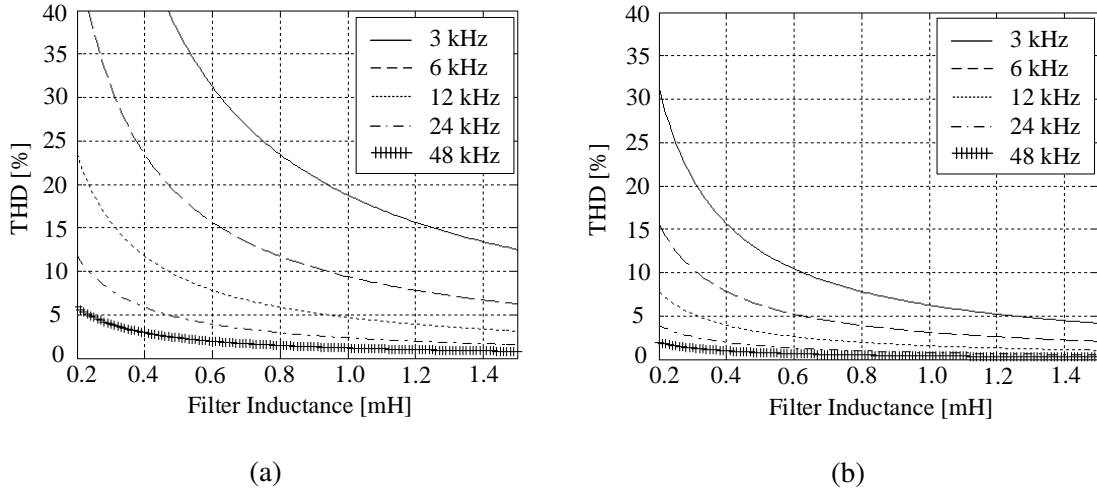


Figure 5.9: THD as a function of filter inductance under different switching frequencies in case of (a) HB and (b) CHB converter.

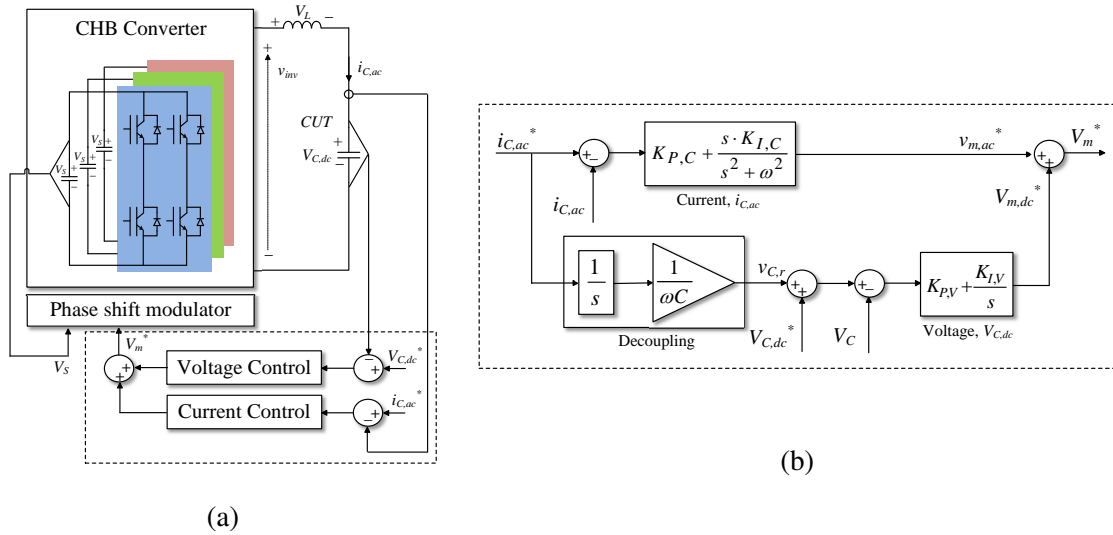


Figure 5.10: (a) Concept of parallel control strategy and (b) its control block diagram.

current and voltage control are accomplished by means of the Proportional-Resonance (PR) and the Proportional-Integral (PI) loop, respectively, and the final reference, V_m^* , is obtained by the summation of their output as expressed in

$$\begin{aligned} V_m^* &= V_{m,dc}^* + v_{m,ac}^* \\ &= V_{m,dc}^* + V_{m,ac}^* \cdot \cos(\omega t + \phi) \end{aligned} \quad (5.16)$$

where the $V_{m,dc}^*$ is the output of the voltage control loop, the $v_{m,ac}^*$ is the output of the current control loop, the ω is the angular frequency, and the ϕ denotes the initial phase. On the other hand, the two control loops are highly coupled due to the parallel structure, resulting in a conflicting target. This is caused by the sinusoidal current, $i_{C,ac}$, that imposes an undesirable

ripple voltage on the DC bias voltage, $V_{C,dc}$, as shown in

$$V_C = V_{C,dc} + v_{C,r} \quad (5.17)$$

where $v_{C,r}$ is the ripple component that is coupled with the current. Hence, this component should be eliminated and can be expressed by the capacitance of the CUT and the current reference as

$$v_{C,r} = \frac{1}{s} \cdot \frac{1}{\omega C} \cdot i_{C,ac}^* \quad (5.18)$$

By adding the above (5.18) to the reference of the DC bias voltage, $V_{C,dc}^*$, and then substituting it by the measured voltage, V_C , only DC component can be fed to the voltage controller as

$$V_{C,dc} = (V_{C,dc}^* + v_{C,r}) - V_C \quad (5.19)$$

Finally, it is worth noting that the proposed control block in Fig. 5.10 (b) provides only single sinusoidal current in order to analyze its effect on the temperature. However, the real current profile could be synthesized with additional PR current controllers to combine the impacts of several harmonic components. Moreover, the feedback controller could be mathematically designed with consideration of the system non-linearity for precise and stable performance by [161]. Finally, the presented analysis can be adopted to other applications that feature DC-link capacitors, like the uninterrupted power supplies (UPS) [162].

The typical configuration of a DC-link capacitor bank is shown in Fig. 5.11 [163]. In case of a DC-link capacitor tank with several branches in parallel sharing the overall current, degradation will still lead to an increasing ESR of the respective capacitor, but since the impedance of the respective branch will increase accordingly, the current sharing within the capacitor tank will change. The current will not be shared equally anymore, but branches with less aged capacitors and therefore lower impedance values will carry more current than branches with more aged capacitors. Thereby, the aging of the more stressed capacitors will be increased due to the higher power dissipation and the subsequent increased temperature stress, leading to a reduction in lifetime of the overall capacitor tank. In order to eliminate this influence, a single capacitor in the capacitor bank is targeted in the following.

The performance of the developed setup with the proposed control algorithm is verified (the setup is shown in appendix 9.1.1). As stated previously, the challenge is to simultaneously generate the high frequency sinusoidal current in few kHz and to regulate the DC bias voltage. The proposed control strategy is verified in Figs. 5.12 (a) and (b) with controlled currents of 2 kHz and 3 kHz at the bias voltage of 150 V, respectively. The paralleled control strategy with the decoupling term allows the two parameters, the sinusoidal current and the DC bias voltage, to be independently handled. This is confirmed through showing the dynamic characteristic in Fig. 5.13. Fig. 5.13 (a) shows the case of the voltage control from

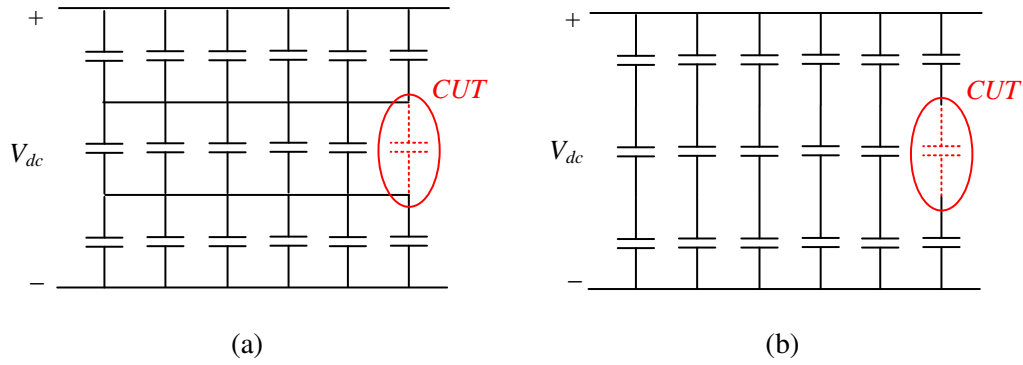


Figure 5.11: Typical schemes of capacitor bank in a back-to-back converter: (a) internally paralleled and (b) not internally paralleled.

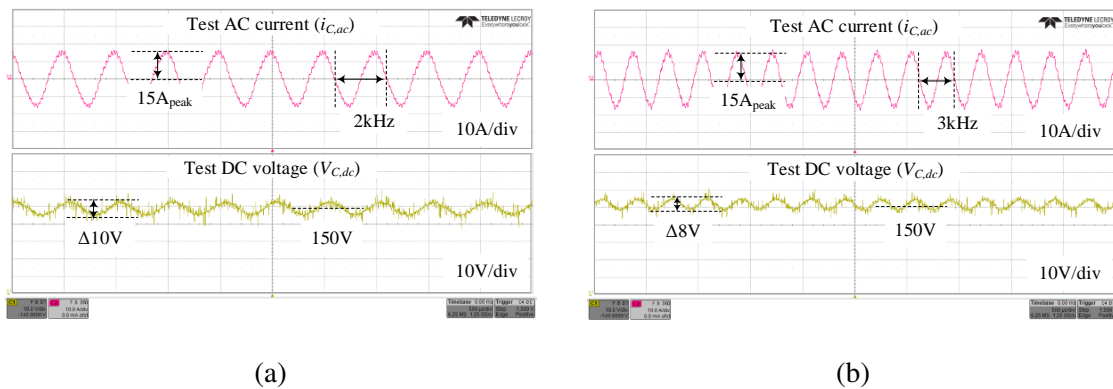


Figure 5.12: High frequency sinusoidal current of (a) 2 kHz and (b) 3 kHz at DC bias voltage of 150 V.

150 V to 200 V with the fixed current at 15 A_{peak} . The opposite case that the current is regulated from 15 A_{peak} to 21 A_{peak} while the voltage is fixed at 150 V, is shown in Fig. 5.13 (b). As it can be seen in the both cases, the change of one parameter does not affect the control performance of another parameter.

In Fig. 5.14 (a), the ESR of the CUT (Aluminum electrolytic capacitor 4500 μF , 500 V) measured at different frequencies is depicted and this is done with LCR meter. As it can be seen, the ESR shows the frequency dependent behavior as shown in Fig. 5.4. In order to verify the capabilities of the test setup at room temperature, constant amplitude ripple currents of 14.3 A are applied to the CUT at different fundamental frequencies and the resulting hot-spot temperatures are measured. The temperature differences between hot-spot and ambient $\Delta T_{h,a}$ and case and ambient $\Delta T_{c,a}$, respectively, are shown in Fig. 5.14 (b). In this context, the case temperature refers to the temperature measured at the side of the capacitor can. Since the amplitude of the applied ripple current is fixed, it is expected that the curve of the hot-spot temperature shows a proportional behavior to the measured curve of the ESR as shown in Fig. 5.14 (a). As can be seen from Fig. 5.14 (b), the progression of the measured temperature curves of both, $\Delta T_{h,a}$ and $\Delta T_{c,a}$, respectively, matches well the expectations.

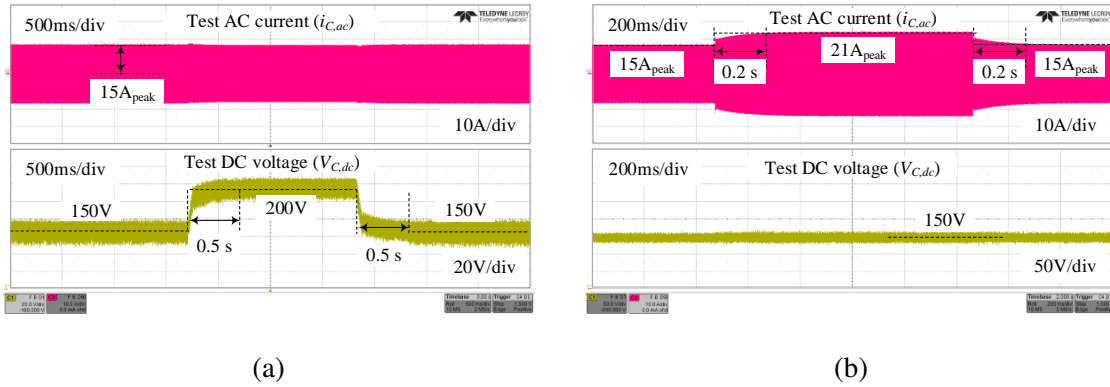


Figure 5.13: Effect of the feed-forward term on decoupling two control parameters: dynamic characteristic of (a) DC bias voltage control and (b) sinusoidal current control.

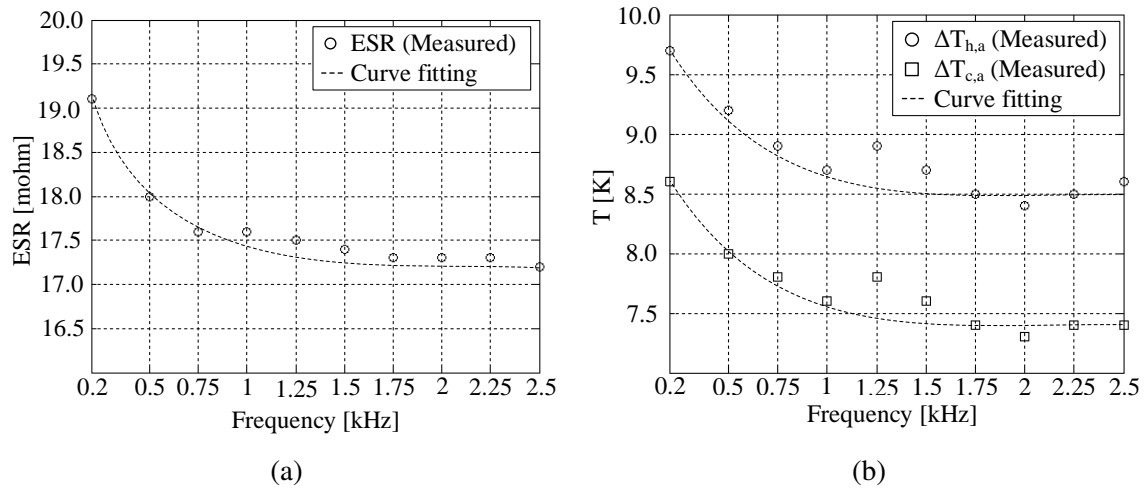


Figure 5.14: (a) ESR measurement of CUT and (b) Measurement of differences between core and ambient temperatures ($\Delta T_{h,a}$) and case and ambient temperatures ($\Delta T_{c,a}$) at constant amplitude sinusoidal currents at different fundamental frequencies.

5.4 Summary

The reliability of capacitor has been addressed, investing the electrical characteristics and failure mechanisms for three types of capacitor: electrolytic, film and ceramic capacitors. Especially, focusing on the electrolytic capacitor, its lifetime model has been discussed, which considers an applied voltage and a core temperature as the major stressors. Since the core temperature is determined by the capacitor losses, which are caused by the capacitor current and the ESR, it has been motivated to derive the clear correlation between the capacitor current and the core temperature variation.

The power converter for testing the electrolytic capacitor has been proposed, which is for injecting the AC current at high frequency range and the DC bias voltage. The AC current and the DC bias voltage were defined with the actual profile in the parallel modular converters as a case study. From this, it has been concluded that the capacitor current features switching frequency harmonics. The major challenge in the converter design is to achieve a

lower THD, which shall be helpful to derive the further clear correlation between the current frequency and the temperature increase. The CHB converter has been chosen as the most suitable topology for the purpose, since it can achieve as a lower THD as possible with a lower filter size. In addition, the lower source voltage and switching devices can be used by the lower voltage drop on the filter. The another challenge is on the controller design, as requiring to simultaneously regulate both the AC current and the DC voltage. The parallel control scheme with the decouple term has been proposed and it has been experimentally validated that each control variable can be individually controlled. The experiment results show the correlation between the current frequency and the hot-spot temperature, concluding that the curve of the temperature variation is proportional to the measured curve of the ESR.

6 Thermally-Compensated Strategies for Capacitors

The DC-link capacitors have significant responsibility not only for the reliability but also for the volume, weight and cost of power converters, leading to many researches aiming at reducing the required capacitance followed by achieving high reliable system. Especially, the strategies to achieve higher reliability can be categorized into three as below:

- Advanced capacitor technology – new manufacturing and dielectric materials
- **Condition monitoring – off-line and on-line solutions**
- **Optimal DC-link design – passive and active solutions**

The advanced capacitor technology definitely contribute to overcome the limitations of the present products, but it is out of scope for the power electronics engineering field. Hence, the latter two strategies, condition monitoring and optimal DC-link design, are studied in the following. The category for these two strategies is shown in Fig. 6.1.

6.1 Condition monitoring

The condition monitoring strategy is based on the regular check-up of the functionality of target device by means of monitoring the electrical precursors, which indicate its degradation (i.e. healthy status), instead of the direct physical access to interior that is normally limited by a package in real fields. The criterion of end-of-life, which is typically used for each type of capacitor, is described in Table. 6.1. Here, C is the capacitance, ESR is the equivalent series resistance, DF is the dissipation factor, R_p is the insulation resistance and the subscript 0 represents the initial value. For the electrolytic capacitor, the capacitance and ESR are the widely used indicators, and it is referred that the end-of-life is reached when either the capacitance is reduced by 20 % or the ESR increases to 200 % compared with their initial value. The capacitance and dissipation factor are used for estimating the condition of the film capacitor, where their failure is occurred when the capacitance is decreased by 5 % or the dissipation factor reaches the value 3 times higher than the initial value. The lifetime of the ceramic capacitor is evaluated by degradation of the capacitance, dissipation factor or

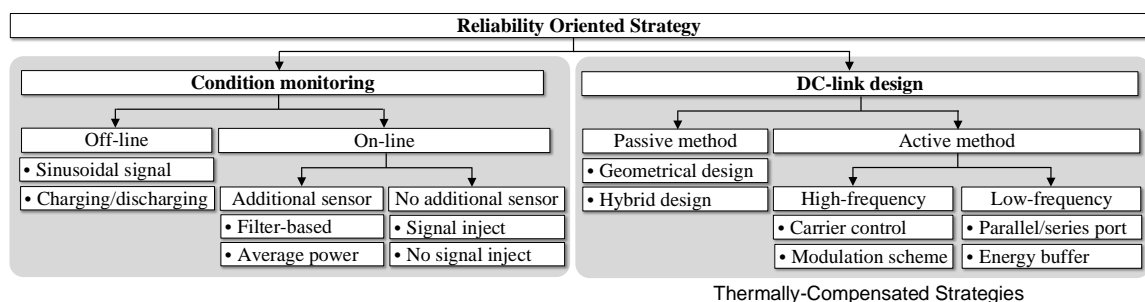


Figure 6.1: Reliability oriented strategies: condition monitoring, optimal DC-link design and their representative methodologies.

Table 6.1: Electrical parameters as healthy status indicator and criterion of end-of-life [147]

	Electrolytic capacitor	Film capacitor	Ceramic capacitor
Precursor	C, ESR	C, DF	C, DF, R_p
Criterion	$C/C_0 < 0.8$ $ESR/ESR_0 > 2$	$C/C_0 < 0.95$ $DF/DF_0 > 3$	$C/C_0 < 0.9$ $DF/DF_0 > 2$ $R_p < 10^7 \Omega$

insulation resistance, and the failure is considered with the decreased capacitance to 90 %, the increased dissipation factor to 200 % or the insulation resistance lower than $10^7 \Omega$.

Coming back to the point for the condition monitoring method, there are two approaches, off-line and on-line, to measure the precursors (see Fig. 6.1).

As it can be expected from the off-line, the method is accomplished by physically taking out a capacitor under test from a main circuit and then, the capacitor is investigated with a RLC network analyzer or a specific experimental setup to inject a desirable current or voltage at a certain frequency [164]. Although the first method is much simpler to be applied, the latter method has been widely employed, because it is application-independent and various analysis methods can be applied to achieve further accurate estimation of the capacitor parameters. The experiment setup, which is composed of a DC source, a signal generator, a power amplifier and input non-inductive resistor as shown in Fig. 6.2, has been used in most of literature proposing the off-line method [164, 165, 166, 167, 168, 169]. The practical technique to estimate the intrinsic ESR value of the electrolytic capacitor was proposed in [165], which is based on the graphical analysis of the data obtained by injecting the sinusoidal signal. It was claimed that this method is simple and shows enough accuracy to determine the end-of-life. However, since the signal at high frequency (near a resonance frequency of capacitor) is used, the results cannot be compared with an information provided by manufacturer, which is typically obtained at 120 Hz. In order to overcome this drawback, the Newton-Raphson (NR) based method was proposed in [166], which allows results very close to the measured values by a precise LCR meter at 120 Hz. Further, the ESR is frequency-dependent and its accurate value at an operating point is required in a design process. The Laplace based method was proposed in [167], which enables to estimate the ESR in wide range of frequencies from 120 Hz to 1 kHz. However, the above methods are prone to high frequency noises, which is inevitable in the practical test and causes the low estimation accuracy. In order to eliminate

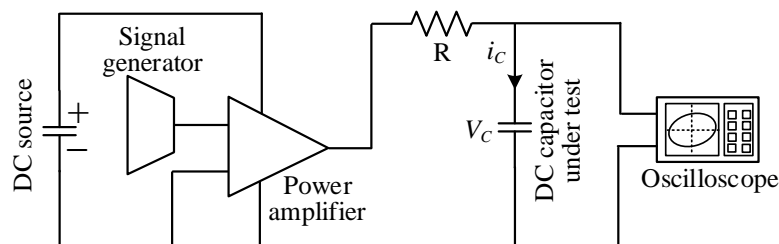


Figure 6.2: Scheme of the experimental setup to inject a designated signal for the off-line methods [164, 165, 166, 167, 168, 169].

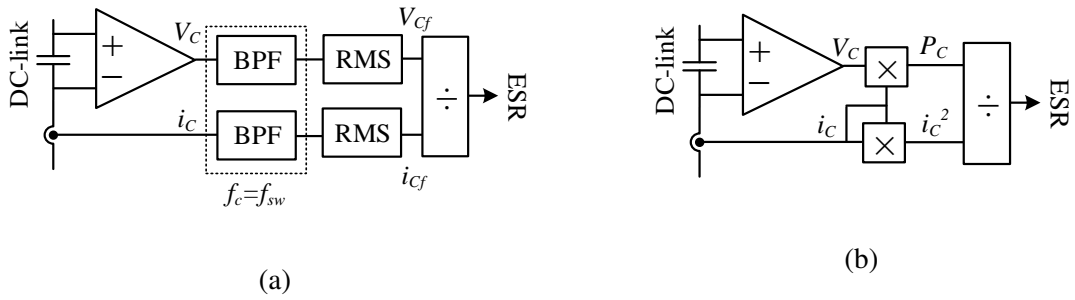


Figure 6.3: ESR estimation scheme for the additional sensor based on-line methods: (a) BPF based method [170] and (b) averaged power based method [171].

the influence of the high frequency noise, the Discrete Fourier Transformation (DFT) based method was proposed in [168] and it shows a higher accuracy compared with the Laplace based method in [167]. In [169], the capacitance and intrinsic ESR values were computed using the Least Mean Square (LMS) algorithm under two test methods of the sinusoidal signal and the charging/discharging method, concluding that the first method is better for the ESR estimation, whereas the latter one is further suitable for the capacitor estimation.

Even though the off-line based methods are simple and cost effective, they inherently have the critical constraints on the practical application due to causing the interrupted operation. It implies that the variation of load and temperature during the system operation is ignored, which is important factor to obtain a reliable estimation of the capacitor parameters [152]. Therefore, most of research has been focused on the on-line method in order to avoid the physical disconnection from a main circuit and consequently, to regularly perform the monitoring. Showing Fig. 6.1, the on-line methods can be categorized into two representative approaches based on: sensor and circuit model.

For the on-line approaches, the additional sensor based methods technically utilize the capacitor voltage and current information, which is obtained by direct measurement. Here, it would be worth to mention that the DC-link voltage is typically measured for a voltage control loop, whereas a current sensor needs to be additionally equipped to acquire the ripple current flowing into the capacitor. Therefore, it can be regarded that the sensor based methods incur the additional hardware efforts and cost.

To estimate the intrinsic ESR and capacitance of the electrolytic capacitor from the measured voltage and current information, the method utilizing the Band-Pass Filter (BPF) was proposed in [170]. The Root Mean Square (RMS) values of the voltage and current, which are filtered at a ESR dominant frequency range (normally switching frequency), were utilized to calculate the ESR by V_{cf}/i_{cf} . The scheme for this method is shown in Fig. 6.3 (a). Similarly, the capacitance is estimated by using the band-pass filtered values centered at 120 Hz, where the capacitance is dominant. On the other hand, in [171], the method using the average power was proposed, which can offer a reasonable estimation performance without any filters. As shown in Fig. 6.3 (b), the ESR is calculated by $(V_C \cdot i_C)/i_C^2 = P_C/i_C^2$, where the V_C and i_C are the RMS values. However, as mentioned before, the sensor based methods es-

essentially require an additional current sensor and/or analog circuit, which shall be connected in series with a DC-link and consequently, causing additional parasitic inductance.

The no additional sensor based methods estimate the capacitor parameters based on a mathematical model of Pulse Width Modulation (PWM) switching converter, instead of additional sensors or circuits. Hence, no additional parasitic inductance and no hardware efforts are needed. However, it is necessary to derive an exact system model, which could be complex and need to make numerous efforts for some applications.

For the DC/DC converter in a Photovoltaic (PV) system, the method to estimate the parameters of the capacitor located in the PV cells output was proposed, which utilizes the voltage difference between different sampling instants [172]. Since the voltage is already sensed for the Maximum Power Point Tracking (MPPT) algorithm, the additional hardware is avoided. However, the estimation can be effectively performed only when the MPPT control is settled (i.e. steady state). In [173], the capacitance of the film capacitor, which is in the AC/DC/AC converter for the traction application, was estimated by observing the discharging characteristics of the capacitor. On the other hand, the on-line method with injecting an AC signal was proposed in [174], considering the AC/DC/AC converter for the drive application. The AC signal, which is controlled by the converter, is injected into the DC-link during no-load condition and then, its capacitance is calculated with the extracted AC voltage and current on the DC-link with help from the digital filters and LMS algorithm. For the drive application, a pulse signal is injected to the DC-link in the AC/DC/AC converter [152, 175], when the motor is stopped. The DC-link voltage and the stator current, which are measured when the pulse signal injected by the converter, are utilized for the capacitor parameters estimation.

However, the above methods still limit the number of estimation. The on-line method for the film capacitor in aerospace drive application was proposed in [176], which can be performed independently of variations in torque and speed. The method uses the information of DC-link voltage and current to estimate the capacitance, which are readily measured for the control. In addition, the most attractive feature is that the method can be continuously performed without affecting a normal operation, allowing the possibility to record a gradual profile of capacitor degradation.

6.2 Optimal DC-link design: passive and active approaches

A proper DC-link (bank) design is very attractive solution to improve the reliability, since the extended lifetime can be achievable by minimizing the capacitor ripple current, i.e. reducing thermal stresses. For a better understanding, it is worth to address the ripple current generation mechanisms, which are typically composed of low-frequency and high-frequency ripple current as shown in Fig. 6.4. The low-frequency ripple current is occurred due to an imperfect power flow between input and output ports, whereas the PWM switching of converters directly connected to the DC-link causes the high-frequency ripple current. Therefore, many researches have devoted to an optimal design solution to reduce the low-frequency and/or

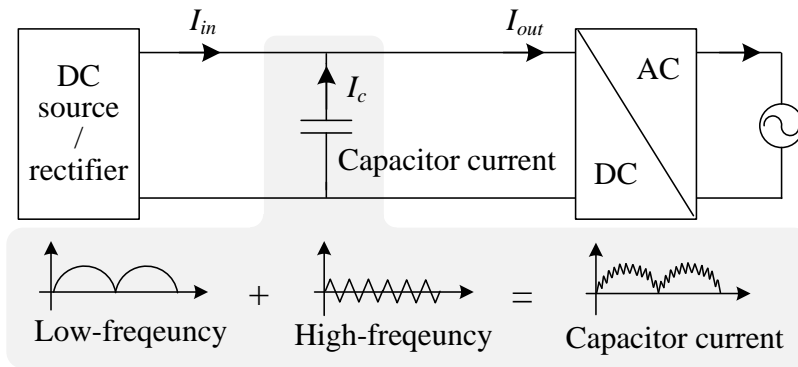


Figure 6.4: Capacitor ripple current, which is composed of low-frequency and high-frequency components.

high frequency ripple current with hardware and/or software approaches, which can be categorized into passive and active solutions.

For the passive solution, as lower parasitic inductance as possible is highly desirable in order to reduce the over-voltage on both the capacitors and the relevant switching devices, which also affects their degradation [147]. In addition to this, the geometric approach, which takes into account the spacing and arrangement of capacitors, was introduced in order to serve better cooling performance, revealing that the aspect ratio, pitch and stagger arrangement can improve a cooling performance by 10 to 20 % [177]. Further, in [178, 179], the hybrid DC-link bank was proposed, which integrates the electrolytic capacitor and the film capacitor in order to exploit their different frequency characteristics. The film capacitors provide the high frequency harmonics caused by the switching converters, while the electrolytic capacitors guarantee only to achieve the high energy density. Consequently, it results in the significantly reduced thermal stress of the electrolytic capacitors, which can translate to the extended lifetime.

The active approaches, which aim at reducing the high-frequency ripple current, are based on a modulation scheme and most of methods has exploited the fact that the DC-link current is determined by a relative phase of carriers for each converter in a back-to-back converter [180, 181]. The specific algorithm was introduced in [180]. The proper carrier phase angles to minimize a target harmonics are determined based on the analytical expression of the switching harmonics current in the DC-link. Subsequently, the control algorithm, which adjusts both the frequency and phase of carriers, was proposed in [181]. However, the major disadvantage of these methods is that a specific operating relationship between the converters connected to the same DC-link is required to make these approaches effective. The modulation strategy named as Extended Double Carrier Pulse Width Modulation (Ext-DCPWM), was proposed in [182], considering the two-level converter. The proposed method shows not only the 40 % reduced RMS ripple current but also 50 % reduced switching losses, compared with the typical space vector method. On the other hand, the influence of carrier types such as triangular, saw-tooth and reverse saw-tooth, on the ripple current was investigated in [183], considering the DC/DC converter.

As mentioned before, the DC-link voltage also has the low-frequency ripple current, which does not only contribute to the lifetime consumption but also to the low power density (i.e. bulky DC-link design). The active DC-link methods, which are so-called as topological based methods, treat with the low-frequency ripple current by means of employing additional ripple power port. For the single-phase DC/AC inverter, an auxiliary bidirectional buck-boost converter, which is connected in parallel to the DC-link, was used to compensate the 100 Hz ripple current, resulting in the 50 % volume reduction of the whole system [184, 185]. Whereas, the concept of the series connected ripple port was proposed in [186], providing the advantage of realization with lower power capacity devices compared with the parallel concept. On the other hand, the dc-link was directly replaced by a Stacked Switched Capacitor (SSC) energy buffer with high energy buffering ratio [187] and consequently, enabling to achieve a higher effective energy density. The above active DC-link solutions allow the reduced energy storage capability, however, additional circuit and control scheme are required, leading to new potential failures.

6.3 Summary

In this section, the existing solutions for improving the capacitor's reliability have been reviewed. This is summarized in Table 6.2, pointing out the principle, advantage and disadvantage for each method. The off-line monitoring methods essentially need to take out a test unit, resulting in the interruption of system operation and the limited number of inspection. On the other hand, the on-line monitoring methods enable the regular (or continuous) inspection with the expense of the complex algorithm and additional sensors. Unlike the monitoring methods, the optimal design methods aim at reducing the capacitor ripple current to reduce the thermal stresses, hence, it is closer to the active thermal control concept. For the passive methods, the hardware design efforts are required for the geometric design of a DC-link bank to achieve a better cooling performance or the hybrid design to exploit the different electric features of each capacitor type. On the other hand, the active methods are performed by modulation or control algorithm with additional power port.

Table 6.2: Categorization of the capacitor reliability oriented methods.

Category	Condition monitoring	
Approach	Off-line	On-line
Principle	Physically taking out a test unit and injecting a test signal	Using the measured voltage and current data
Advantage	<ol style="list-style-type: none"> 1. Simple 2. Cost effective 	<ol style="list-style-type: none"> 1. No requirement of the physical disconnection 2. Regular (or continuous) monitoring
Disadvantage	<ol style="list-style-type: none"> 1. Interrupted operation 2. Limited number of inspection 	<ol style="list-style-type: none"> 1. Complex algorithm 2. Additional sensor (only for additional sensor method)
Category	Optimal DC-link design	
Approach	Passive	Active
Principle	Ripple current reduction by <ol style="list-style-type: none"> 1. Geometrical or 2. Hybrid design 	Ripple current reduction by <ol style="list-style-type: none"> 1. Modulation or 2. Control method
Advantage	<ol style="list-style-type: none"> 1. Simple 2. No control requirement 	<ol style="list-style-type: none"> 1. Flexible control ability
Disadvantage	<ol style="list-style-type: none"> 1. Additional cost and hardware efforts 	<ol style="list-style-type: none"> 1. Complex algorithm 2. Additional hardware

7 Conclusion and Future Research

7.1 Conclusion

In this thesis, the reliability of power converters has been discussed, which is the critical challenge not only to ensure the power security and safety but also to reduce the maintenance costs. Especially, the failures of power semiconductor devices and capacitors are targeted, in which it has been reported that they are the most prone components in the power converters to failures. The failure rate of 20 % for the power semiconductors and 34 % for the capacitors is shown, approximately, in the industries.

In section 2, the modular converter was defined as the system with different aged cells, considering the typically used maintenance and control strategy in the Smart Transformer (ST) and the large-scale Photovoltaic (PV). This leads to the conclusion that the different remaining useful lifetime of each cell needs to be properly managed in order to improve the whole system's reliability and to economically schedule a maintenance.

To address the reliability of power semiconductor devices, the wear-out failure mechanisms such as the bond wire fatigue, the solder layer fatigue, the metallization reconstruction and the gate oxide failure have been studied in section 3, considering the typical wire-bonded structure. From this, it was presented that the thermal stresses are the root-cause of such failures. The influence of thermal stresses on the lifetime was highlighted with the Physics-of-Failure (PoF) based lifetime model, which takes the mean junction temperature and the amplitude of thermal cycling into account as the major failure causes. Further, the reliability evaluation methodology has been introduced, which involves the lifetime model, the thermal network, the counting method and the accumulated damage estimation. The thermal network in the medium time scale was shown, since a mission profile ranged from minutes to hours is considered as the major source of the thermal stresses in this thesis. The translated thermal profile from the thermal network is decomposed to each thermal stress by the rainflow counting method and its outcomes are fed to the accumulated damage calculation based on Miner's rule. This lifetime evaluation methodology has been employed to validate the effects of the proposed active thermal control methods in section 4.

The active thermal control methods were reviewed and categorized in accordance with the application level: controller, modulator and device level, pointing out the major constraint of each level. The device level methods require additional hardware efforts, whereas the modulator and controller levels are dependent on a targeted topology and application. In section 4, the modulator based active thermal control methods: the multi-frequency modulation and the discontinuous modulation, are proposed for achieving the power routing in the modular converter structured by the Cascaded H-Bridge (CHB) and DC/DC converters.

The multi-frequency modulation exploiting the third harmonic voltage extends the DC-link voltage utilization by 15.5 %, which allows the improved power imbalance capability. By this, the number of cells completely unloading can be increased by 40 – 60 % compared with the typical sinusoidal modulation. The effect on the accumulated damage of the DC/DC

converters has been analyzed under the arbitrary fluctuated mission profile. The damage of thermally compensated converter can be reduced to 20 %, whereas others are additionally damaged to three times. However, the multi-frequency modulation limits to handle the lifetime of the DC/DC converters and the CHB cells, simultaneously. This limitation has been dealt with the discontinuous modulation, which manipulates the clamping angle not only to perform the power routing for the DC/DC converters but also to reduce the generated losses of the CHB cells. Further, the power imbalance capability is better by 5 % than the multi-frequency modulation. The demonstrated accumulated damage has confirmed the possibility to manage the whole system's lifetime. By the clamping angle of 60°, the damage of clamped and non-clamped CHB cells can be reduced by around 90 % and 30 %, respectively. In case of the DC/DC converters, a unloaded converter has a damage reduction up to 1/300, whereas additionally loaded converters has 14 times more damage.

Apart from the power routing, the variable-clamping angle discontinuous modulation has been proposed, which aims at completely compensating the thermal cycling of the CHB converter. The case study with the significantly fluctuating power profile show that the accumulated damage of a thermally compensated cell can be reduced to 1 % compared with the typical sinusoidal modulation, while that of non-compensated cells is not affected. Further, this concept has been also validated for the parallel modular converter, showing the reduced accumulated damage to 21 %.

On the other hand, the proposed methods negatively affect the power quality of the CHB converter, since they utilize the different modulation signals for each cell. To address this, the existing methods that are based on variable-carrier phase angles, have been experimentally validated in terms of the Weighted Total Harmonic Distortion (WTHD) under the different unbalanced operating conditions. Based on this result, the variable-carrier angle modulation has been proposed, which is applicable for the discontinuous modulation. It has been shown that this proposed method guarantees the comparative WTHD with that under the ideal balanced condition.

In section 5, the reliability of capacitors has been discussed with investigating the major failure mechanisms of three types of capacitor: electrolytic, film and ceramic capacitors. Especially, focusing on the electrolytic capacitor, it has been concluded that the root-cause of the failures is closely related to the electrolyte evaporation by the thermal stresses. Through the equivalent model and the lifetime model, the impact of capacitor current on the reliability was discussed, leading to the motivation to derive the correlation between the capacitor current and the thermal stresses.

The power converter for capacitor test has been proposed in order to experimentally derive the clear correlation between the frequency of capacitor current and the hot-spot temperature. In the DC-link applications, the capacitor current only has high frequency harmonic components caused by the switching behavior. Hence, the setup is required to generate the high frequency AC current and the DC bias voltage on the capacitor under test. The resulting challenge was on the hardware design. To address this, two possible configurations of the H-Bridge (HB) and CHB converter have been compared and it has been concluded that the

CHB converter is beneficial as allowing the lower THD with a lower output filter (around three times lower to achieve a same THD performance). In addition, the lower blocking voltage devices can be employed with the help of the series modular structure. Another challenge was the control algorithm, which needs to regulate the AC current and DC voltage, simultaneously. The control-ability for the both control targets has been achieved by the proposed parallel control strategy. Through the developed setup, it has been revealed that the hot-spot temperature is increasing as the current frequency is decreasing, following the frequency-dependent ESR curve.

The reliability oriented strategies: condition monitoring and optimal DC-link design, have been reviewed in section 6. The condition monitoring is passive approach, which only focuses on estimating the degradation of a target device in either off- or on-line. On the other hand, the optimal DC-link design approach aims at actively reducing the capacitor current. In the hardware design point of view, the physical and electrical characteristics have been considered to serve a better thermal dissipation and to take the electrical advantages of different types of capacitor. In addition, the modulation based methods has been presented, which aims at reducing the high frequency harmonic components caused by the switching behavior. These methods do not require any hardware efforts, but their application is strictly limited to the converter configuration. Finally, the methods using auxiliary converter were discussed. The low frequency harmonic components caused by power flow can be reduced, additionally allowing to reduce a required capacitance. However, the additional hardware and the complex control algorithm are required, which could be new potential failures.

7.2 Future Research

In this section, the future research topics/ideas in order to reinforce the outcomes of this thesis are briefly described.

- **Generalization of the active thermal control**

In section 4.2 and 4.3, the multi-frequency method and the discontinuous method have been proposed and analyzed in terms of power routing capability and influence on loss distribution. However, the analysis has been performed for the system with three cells, assuming that one of cells needs to be thermally compensated. In this context, it is necessary to explore a generalized analysis/method, which can consider a system with higher number of cells and various scenarios of reliability requirement.

- **Experimental verification of the active thermal control on the lifetime of power semiconductor**

In section 4.2 and 4.3, the proposed active thermal control methods have been experimentally validated in terms of their feasibility and influence on the junction temperature, whereas their impact on the lifetime has been theoretically demonstrated. Therefore, it is of interest to experimentally validate the impact of the active thermal control on the lifetime, i.e. number of cycle to failure. This will be performed with the help of accelerated ageing test approaches,

which consider real operation environments such as cooling system, full DC-link and PWM behavior. In addition, an online condition monitoring system also needs to be developed to detect the wear-out failure.

- **Advanced active thermal control strategy for both power semiconductors and DC-link capacitors**

The active thermal control algorithms were proposed in many literature, which are for either the power semiconductor or the capacitor. However, as presented in section 4.2, the active thermal control methods for the power semiconductor affect the current spectrum of capacitor. Further, it can be expected that the active thermal control for the capacitor shall influence on the reliability of power semiconductors. Therefore, it is potential research topic to investigate deeply the influence of active thermal control methods on non-targeted device. Followed by, active thermal control strategy, which considers both components, needs to be proposed.

- **Active thermal control strategy without expense of low power quality**

The total harmonic distortion of power converter output voltage is one of the most important criterion in order to meet a required power quality and to reduce a filter size. To address this, the variable-carrier angle methods were studied and their limitation with ripple components in DC-link voltage was figured out. One potential topic is to propose a method, which considers the ripple components. Further, since the investigated variable-carrier methods are only applicable to the series modular converter, a consideration of various power converter configuration can be of interest.

- **Experimental evaluation of influence of capacitor current on lifetime**

In section 5, the power converter for testing the capacitor was designed and though this, the correlation between the current frequency and the hot-spot temperature was derived. This experiment was motivated based on that the reliability of capacitor is highly associated with the thermal stresses. However, this relation between the reliability and the thermal stresses has been mostly established by applying the thermal stresses through temperature chamber. In addition, the capacitor under test has been drilled to accelerate its degradation. This means that the capacitor is not under actual operating condition, not considering the capacitor current. Therefore, it is interesting to investigate experimentally an actual impact of the current frequency on the lifetime with the capacitor test setup. For this, the accelerated test approach can be employed with help of condition monitoring system.

8 References

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9 Attachment

9.1 Appendix

9.1.1 Developed experimental setup

The setup shown in Fig. 9.1 is used to implement and verify the multi-frequency and discontinuous modulation strategies for the power routing. The setup consists of the seven-level Cascaded H-Bridge (CHB) converter controlled by the micro-processor 'MPC5643L' and the power analyzer 'Yokogawa WT1800' to measure the loading power of each cell. The voltage and current waveforms are captured with the oscilloscope 'Lecroy HDO6104-MS'.

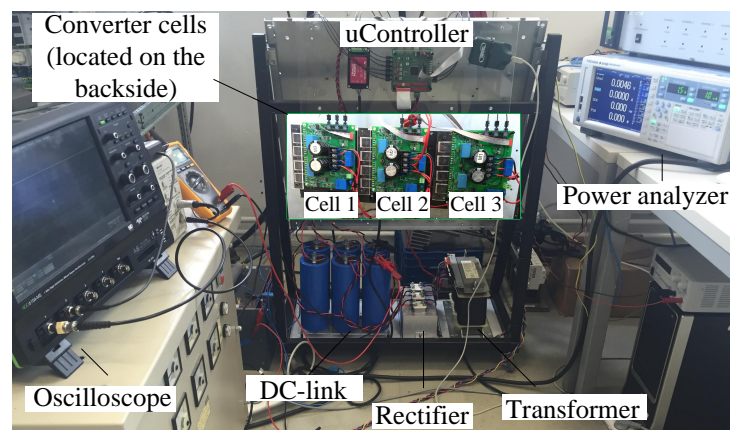


Figure 9.1: Developed laboratory setup featuring the seven-level CHB converter and the power analyzer to validate the power routing concept.

Fig. 9.2 shows the five-level CHB plus DAB converter with open modules. The effect of the power routing method is validated through this setup by measuring directly the junction temperature. The temperature is measured with a temperature monitoring system of fiber optic sensors 'OTG-F' and signal conditioner 'ProSens'.

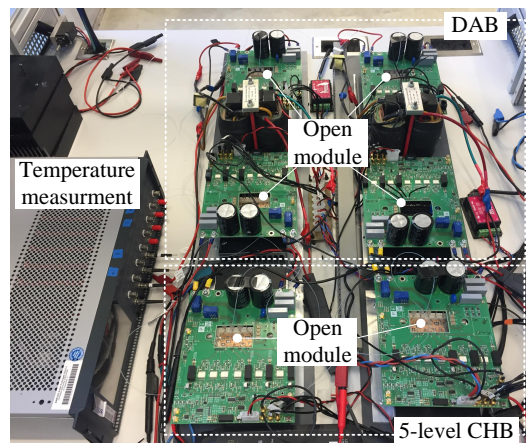


Figure 9.2: Laboratory setup of five-level CHB and DAB with open modules.

The variable-clamping angle method is validated by the setup shown in Fig. 9.3. The setup is composed of the seven-level CHB converter with open modules 'DP25H1200T101667', which is controlled by 'dSPACE', and a temperature monitoring system of fiber optic sensors 'OTG-F' and signal conditioner 'ProSens'. The voltage and current waveforms are captured with the oscilloscope 'Lecroy HDO6104-MS' and the load step change is performed by the electric load 'Chroma 63804'.

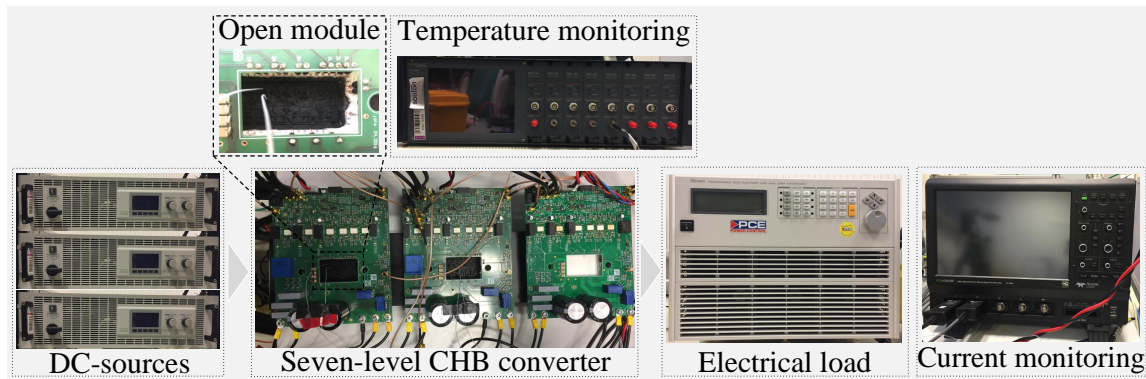


Figure 9.3: Developed laboratory setup of seven-level CHB converter with open modules to measure the junction temperature of IGBT modules.

The three-phase converter setup is shown in Fig. 9.4 with the open module to validate the discontinuous modulation method for the parallel modular converter. The used equipments are identical with Fig. 9.3.

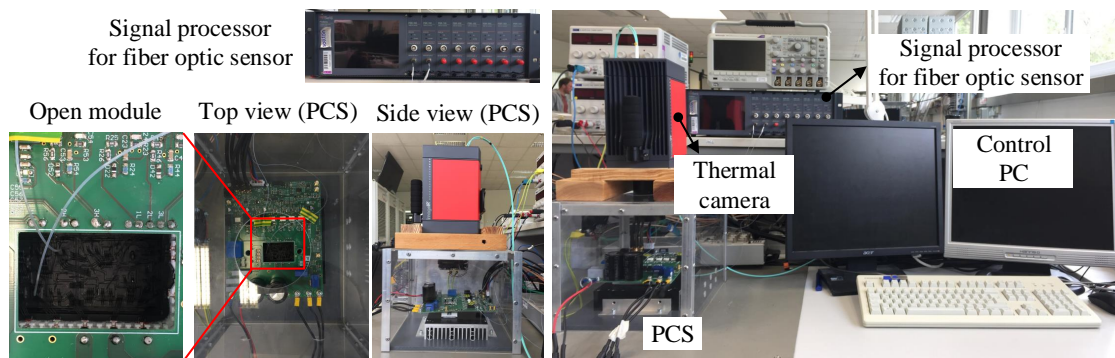


Figure 9.4: Three-phase converter with open module to validate applicability of the active thermal control to the parallel modular converter.

Fig. 9.5 shows the setup that aims at testing capacitors. The setup consists of the seven-level CHB converter controlled by the micro-processor 'MPC5643L' and the temperature chamber to keep the ambient temperature at a same level during a test. The hot-spot temperature of the capacitor is directly measured through fiber optic sensors 'OTG-F' and signal conditioner 'ProSens'. The voltage and current waveforms are measured by the oscilloscope 'Tektronix MSO 4034'.

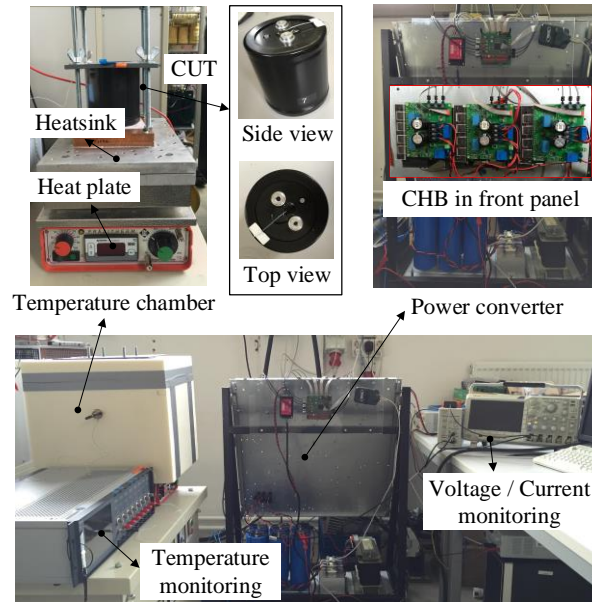


Figure 9.5: Power converter for capacitor test.

9.1.2 Rainflow counting algorithm

Table 9.1: Sequence of the rainflow counting method for the thermal profile in Fig. 3.7.

Step	Z	Reversals	Out of data	< 3 reversals	Y	r(Y)	X	r(X)	r(X) < (Y)	Z in Y	Actions
1	A	A, B, C	No	Yes	AB	24.87	BC	12.46	Yes	-	1. Read the next reversal
2	A	A, B, C, D	No	Yes	BC	12.46	CD	21.46	No	No	1. Count BC as one cycle 2. Discard B and C
3	A	A, D	No	No	-	-	-	-	-	-	1. Read the next reversal
4	A	A, D, E	No	Yes	AD	33.87	DE	21.46	Yes	-	1. Read the next reversal
5	A	A, D, E, F	No	Yes	DE	21.46	EF	12.46	Yes	-	1. Read the next reversal
6	A	A, D, E, F, G	No	Yes	EF	12.46	FG	24.87	No	No	1. Count EF as one cycle 2. Discard E and F
7	A	A, D, G	No	Yes	AD	33.87	DG	33.87	No	Yes	1. Count AD as half cycle 2. Discard A
8	D	D, G	Yes	-	-	-	-	-	-	-	1. Count DG as half cycle

9.1.3 Calculation of DC-link current in back-to-back converter

The time varying switched DC-link machine- and grid-side currents are expressed as a summation of each phase currents multiplied by their corresponding switching function as

$$i_{link,m}(t) = \sum_{\eta=1}^3 I_m \cos(\omega_m t + \varphi_{\eta,m} - \varphi_{0,m}) \cdot S_{\eta,m}(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{pwm,m}), \quad (9.1)$$

$$i_{link,g}(t) = \sum_{\eta=1}^3 I_g \cos(\omega_g t + \varphi_{\eta,g} - \varphi_{0,g}) \cdot S_{\eta,g}(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{pwm,g}).$$

The switching function of each phase can be formed by the phase voltage function ($v_{\eta,m}$) as

$$S_{\eta,m}(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{pwm,m}) = \frac{v_{\eta,m}(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{pwm,m})}{V_{dc}}, \quad (9.2)$$

$$S_{\eta,g}(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{pwm,g}) = \frac{v_{\eta,g}(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{pwm,g})}{V_{dc}}.$$

The $v_{\eta,m}$ and $v_{\eta,g}$ are expressed as a function of the time, the fundamental frequency, the switching frequency, the phase of three-phase voltages, and the phase of the PWM carrier signal by

$$\begin{aligned} \frac{v_{\eta,m}(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{pwm,m})}{V_{dc}} &= \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{1}{n \left(\frac{\omega_m}{\omega_{sw}}\right)} J_n \left(n \left(\frac{\omega_m}{\omega_{sw}}\right) \frac{\pi}{2} m_{a,m} \right) \\ &\sin \left(n \frac{\pi}{2} \right) \cos(n(\omega_m t + \varphi_{\eta,m})) + \frac{2}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0 \left(m \frac{\pi}{2} m_{a,m} \right) \sin \left(m \frac{\pi}{2} \right) \\ &\cos(m(\omega_{sw} t + \varphi_{pwm,m})) + \frac{2}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{q} J_n \left(q \frac{\pi}{2} m_{a,m} \right) \sin \left((m+n) \frac{\pi}{2} \right) \\ &\cos(m(\omega_{sw} t + \varphi_{pwm,m}) + n(\omega_m t + \varphi_m)), \end{aligned} \quad (9.3)$$

$$\begin{aligned} \frac{v_{\eta,g}(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{pwm,g})}{V_{dc}} &= \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{1}{n \left(\frac{\omega_g}{\omega_{sw}}\right)} J_n \left(n \left(\frac{\omega_g}{\omega_{sw}}\right) \frac{\pi}{2} m_{a,g} \right) \\ &\sin \left(n \frac{\pi}{2} \right) \cos(n(\omega_g t + \varphi_{\eta,g})) + \frac{2}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0 \left(m \frac{\pi}{2} m_{a,g} \right) \sin \left(m \frac{\pi}{2} \right) \\ &\cos(m(\omega_{sw} t + \varphi_{pwm,g})) + \frac{2}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{q} J_n \left(q \frac{\pi}{2} m_{a,g} \right) \sin \left((m+n) \frac{\pi}{2} \right) \\ &\cos(m(\omega_{sw} t + \varphi_{pwm,g}) + n(\omega_g t + \varphi_g)) \end{aligned}$$

where $q = m + n(\omega_m/\omega_{sw})$. Finally, by substituting (9.2) and (9.3) into (9.1), the $i_{link,m}$ and $i_{link,g}$ are obtained.

9.1.4 2 MW wind turbine system specification and simulation condition

The specification of 2 MW wind turbine system, which consists of the machine-side, DC-link and the grid-side, is described in Table 9.2, which is considered for the DC-link current analysis.

Table 9.2: Specification of wind turbine system.

Machine-side (PMSG)	Rated power	2 MW
	Rated voltage	690 V
	Rated frequency (f_m)	50 Hz
	Number of pole	4
	Switching frequency	1 kHz
DC-Link	Capacitance (C_{dc})	10 mF
	Voltage (V_{dc})	1100 V
Grid-side	Line-to-line voltage	690 V
	Frequency (f_g)	50 Hz
	Switching frequency (f_s)	1 kHz

The considered operating points of the 2 MW wind turbine system, which is a function of the generated power, is described in Table 9.3, which is used to identify their impact on the DC-link current spectrum.

Table 9.3: Considered operating points to identify their impact on current spectrum.

No.	Power (kW)	Machine-side (PMSG)		Grid-side	
		Rotating speed (rpm)		Current per phase (A)	
1	128	600 (20 Hz)	266	106	
		Current per phase (A)			
2	432	900 (30 Hz)	600	360	
		Current per phase (A)			
3	1024	1200 (40 Hz)	1066	853	
		Current per phase (A)			
4	2000	1500 (50 Hz)	1666	1666	
		Current per phase (A)			

9.2 Curriculum Vitae

Name:

Youngjong Ko

Date of birth:

21 May 1985

Place of birth:

Daejeon

Nationality:

South Korea

Education:

2001 - 2004: Daeseong High School, Daejeon, South Korea

Course of study:

2004 - 2009: Bachelor of Science (B.Sc.) at the Electrical and Computer Engineering in Ajou University, Suwon, South Korea

2010 - 2012: Master of Science (M.Sc.) at the Electrical and Computer Engineering in Ajou University, Suwon, South Korea

Work experience:

2012 - 2015: Work experience as power electronics R&D engineer, South Korea

2015 - Present: Scientific staff member at the Chair of Power Electronics at the Christian-Albrechts-Universität zu Kiel