

Control of Smart Transformer-fed Distribution Grid

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Zhixiang Zou

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Kiel, den 10. April 2019

Zhixiang Zou

1. Gutachter:	Prof. Marco Liserre, Ph.D.
2. Gutachter:	Prof. Xiongfei Wang, Ph.D.
3. Gutachter:	Prof. Dr.-Ing. Johanna Myrzik
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Deutsche Kurzfassung der Arbeit

Das Verteilnetz unterliegt erheblichen Veränderungen durch die Nutzung dezentraler Energiequellen und neuer Verbraucher wie Elektrofahrzeuge. Die zunehmende Verbreitung dieser Energiesysteme hat zu Problemen im Management des Stromnetzes geführt, z.B. auftretender Rückleistungsfluss, Verletzung der Spannungsgrenzen, verminderte Netzqualität, verringerte Systemträgheit etc. Um den zukünftigen Netzproblemen zu begegnen, stellt der ST (engl. smart transformer) aufgrund der Steuerungs- und Kommunikationsfunktionalitäten und der Dynamik eine vielversprechende Lösung dar, das Netzmanagement zu verbessern und die Hosting-Kapazität der verteilten Energiesysteme zu erhöhen.

Die Spannungsregelung ist eines der wichtigsten Themen für die ST-Anwendung im Niederspannungsnetz. Der ST LV-Umrichter (engl. low voltage) ermöglicht die direkte Regelung der Spannung in Bezug auf Amplitude und Frequenz und bestimmt im Zusammenspiel mit den Netzkomponenten die Performance und Stabilität des LV ST-gespeisten Netzes. Aus Sicht der Regelung stellen sich aber Herausforderungen: Wechselwirkungen mit verteilten Energiesystemen, Netzresonanzen, stabiler Betrieb mit Netzsynchrosation und hohe Stromqualität bei der Bereitstellung von Netzservices.

Die Regelungssysteme dezentraler Energiesysteme sind anfällig für Wechselwirkungen mit der Spannungsregelung des ST LV-Umrichters, was zu Leistungseinbußen führen kann. Aus diesem Grund wird eine Stabilitätsanalyse verschiedener Spannungsregelungsstrategien durchgeführt, um eine optimale Lösung sowie eine Auslegung zu finden, die einen sicheren Betrieb garantiert.

Um Instabilitäten aufgrund von Resonanzproblemen zu vermeiden, kann eine Netzimpedanz-Veränderung mittels ST LV-Umrichter implementiert werden, die eine aktive, dämpfungsbasierte Lösung zur Verminderung von Netzresonanzen ist. Zur Berücksichtigung verschiedener Resonanzphänomene wird ein Resonanzschätzverfahren entworfen und in die Spannungsregelung sowie in die aktiven, dämpfungsbasierten Lösungen integriert. Das Schätzverfahren kann für die Analyse im Frequenzbereich durch Vektoranpassung ausgelegt werden, so dass eine Online-Stabilitätsmargenschätzung für das Niederspannungsnetz realisiert wird.

Für auftretende Probleme durch die Netzsynchrosation wird ein Netzumrichter-Modell höherer Ordnung unter Berücksichtigung von Synchronisationseffekten entwickelt, das eine erhöhte Genauigkeit gegenüber dem konventionellen Kleinsignalmodell aufweist und durch das die Oberschwingungsstabilität sowohl bei stationären als auch bei großen Phasenstörungen analysiert werden kann. Ein auf virtueller Impedanz basiertes Stabilisierungsverfahren mittels ST LV-Umrichter wird eingeführt, um die durch die Netzsynchrosation verursachte Instabilität eines ST-gespeisten Netzes zu vermeiden.

In dieser Arbeit wird eine Spannungsregelung vorgeschlagen, bei der Oberschwingungen während Schwankungen der Netzfrequenz eliminiert werden. Dies ermöglicht es dem LV ST-gespeisten Netz, eine hohe Stromqualität zu gewährleisten, wenn frequenzbasierte Netzservices vom ST bereitgestellt werden. Das Szenario des frequenzadaptiven ST-gespeisten Netzes wird vorgestellt und die Stabilität des Gesamtsystems bei Variationen der Netzfrequenz analytisch und experimentell untersucht.

English Summary

At present, the distribution grid is undergoing significant changes due to the utilization of distributed energy resources and new loads, like electric vehicles. The increasing penetration of these resources has caused issues in the management of the electric grid, for instance, reverse power flow and voltage violation, power quality violation, decreased system inertia, and so on. To cope with the emerging grid issues, the Smart Transformer (ST) is a promising solution, which can benefit the grid management and increase the hosting capacity of distributed energy resources, due to its control and communication functionalities and dynamic.

The voltage control is one of the most important topics for the ST application in the distribution grid. The ST LV converter enables direct control of the LV grid voltage waveforms in terms of amplitude and frequency. This control, interacting with the connected appliances, determines the performance and stability of the LV ST-fed grid. Though ST can well address grid issues, challenges from the point of view of control are encountered: control interactions with distributed resources, grid resonances, stable operation with grid synchronization, and high power quality during provision of grid services. To address these problems, the knowledge of power system, power electronics and control is combined in this work.

The control systems introduced by distributed energy resources are prone to interact with the voltage control of ST LV converter, which could lead to performance degradation. For this reason, stability assessment of different voltage control strategies is performed for the ST LV converter, in order to find an optimal solution as well as design consideration ensuring stable operation.

As an opportunity to avoid instability, especially resonance issue, grid impedance reshaping by means of ST LV converter can be adopted, which is an active damping-based solution for alleviating the resonances of LV grid. To deal with different resonance phenomena, a resonance estimation method is designed and included in the voltage control as well as with the active damping-based solutions. This estimation can be interpreted for frequency-domain analysis by vector fitting so that an online stability margin estimation for LV grid can be obtained.

For emerging issues caused by grid synchronization, a more accurate model with higher-order of grid converter considering synchronization effects is developed. This model is able to analyze harmonic stability during both steady-state and large phase perturbation, and thus it is an extension of the conventional small-signal model. Based on this, a virtual impedance-based stabilization method by means of ST LV converter is introduced to avoid instability of a ST-fed grid caused by the synchronization.

Harmonic elimination for the voltage control during fundamental frequency variation, is proposed. This allows the LV ST-fed grid to maintain good power quality when frequency-based services are provided by the ST. The scenario of frequency adaptive ST-fed grid is demonstrated and the stability of the overall system during frequency variation is investigated analytically and experimentally.

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General symbols

General symbols

$u(t), u$	Time-variant variable
\tilde{u}	Oscillation component
U	Constant or dc quantity
Δu	Small-signal perturbation
\mathbf{u}	Vector
(s)	Laplace domain operator
(t)	Time domain operator
(z^{-1})	Discrete domain operator
\mathbf{G}	Transfer function matrix

Superscripts

$\theta 1$	Synchronization term during small phase perturbation
$\theta 2$	Synchronization term during large phase perturbation

Subscripts

$1, \dots, 8$	PWM switching signals
a, b, c, n	Phase a, b, c, n
α, β	α - and β -components in stationary reference frame
d, q	d - and q -components in synchronous reference frame
dd, dq, qd, qq	dd -, dq -, qd -, and qq -components of transfer function matrix
max	Maximum
min	Minimum
MV	Medium voltage
LV	Low voltage

Special symbols

a_0, a_1	Coefficients of digital LPF
A_k	Lagrange coefficients
a_m	New poles of VF
C_f	Filter capacitance of ST LV converter
C_{ff}	Filter capacitance of DER converter
C_{LVDC}	dc-link capacitance of ST LV converter

C_{MV}	Filter capacitance of ST MV converter
C_{MVDC}	dc-link capacitance of ST MV converter
C_r	Capacitance of tank circuit
D	Disturbance
d, e	Coefficient of the rational function for VF
d_{dab}	Phase shift ratio of DAB
D_{LPF}	Damping factor of LPF
d_{MV}	Disturbances of MV converter
E	Control error
F	Fractional order of FORC
f	Fundamental frequency
f_{dcs}	Switching frequency of dc/dc converter
f_{LV}	Frequency of LV grid
f_{max}	Frequency upper limit of ST-fed grid
f_{min}	Frequency lower limit of ST-fed grid
f_n	Sweeping frequency
f_s	Sampling frequency
f_{res}	Resonant frequency of <i>LCL</i> filter
G_c	Transfer function of feedback control
G_{cc}	Transfer function of current control of DER
G_{Cf}	Transfer function of filter capacitance of ST LV converter
G_{Cff}	Transfer function of filter capacitance of DER
G_{cl}	Closed-loop transfer function of ST LV converter and its control
G_d	Transfer function of computation and PWM delay
G_e	Error transfer function
G_f	Transfer function of filter
G_{forc}	Transfer function of FORC
G_i	Transfer function of current reference block as well as PLL
$G_{i,i}$	Transfer function of current inner loop of ST LV converter
G_{in}	Transfer function of inner loop and LV converter
$G_{in,nff}$	Transfer function of inner loop and LV converter without feedforward
G_{LEF}	Transfer function of LEF
G_{Lf}	Transfer function of filter inductance of ST LV converter
G_{1f}	Transfer function of phase lead element for CRC
G_{L1f}	Transfer function of converter-side filter inductance of DER
G_{L2f}	Transfer function of grid-side filter inductance of DER
G_{LPF}	Transfer function of LPF
G_{MVf}	Transfer function of filter of MV converter
G_{MVop}	Open-loop transfer function of dc voltage control of MV converter
G_{op}	Open-loop transfer function of ST LV converter and its control
$G_{op,DER}$	Open-loop transfer function of DER converter and its control
$G_{op,LEF}$	Open-loop transfer function of ST LV converter with LEF-based active damping
$G_{op,LPF}$	Open-loop transfer function of ST LV converter with LPF-based active damping

G_{ops}	Open-loop transfer function of a feedback control
$G_{o,v}$	Transfer function of voltage outer loop of ST LV converter
G_{PIMV}	Transfer function of current control of MV converter
$G_{PI dc}$	Transfer function of dc voltage control of MV converter
$G_{PLL,cl}$	Closed-loop transfer function of PLL
$G_{PLL,op}$	Open-loop transfer function of PLL
G_{rc}	Transfer function of CRC
H	Closed-loop transfer function of a feedback control
H_{MV}	Closed-loop transfer function of current control of MV converter
H_{PLL}	Response from $\Delta v'_q$ to $\Delta \theta'$
$I(s)$	Closed-loop transfer function of current control
i	Grid current of DER converter using L filter
i'	Transformed current of DER converter
i_C	Capacitor current of ST LV converter
i_{dab}	DAB current
i_g	Grid-side current of DER converter using LCL filter
i_h	Threshold of ST harmonic current
i_L	Inductor current of ST LV converter
$i_{L,1}$	Inductor current of DER converter
i_{LV}	rms value of ST current
I_{max}	Maximum current of ST LV converter
i_{MV}	Current of ST MV converter
i_{MVDC}	dc current of ST MV converter
i_{MVh}	Harmonic current reference of ST MV converter
i_{oh}	Harmonic content of ST current
I_{ref}	Amplitude of current reference
i_{ref}	Fundamental current reference
i_{5ref}	5-th harmonic current reference
i_{7ref}	7-th harmonic current reference
i_{src}	Current of SRC
i_{ST}	Load current of ST LV converter
K_{dab}	Ratio between phase shift and active power
k_{dc}	Open-loop gain of dc voltage control of MV converter
k_{ic}	Integral gain of DER current control
$k_{i,i}$	Integral gain of ST current inner loop
k_{iMV}	Integral gain of current control of MV converter
k_{ipll}	Integral gain of PLL
$k_{i,o}$	Integral gain of ST voltage outer loop
k_{MVq}	Gain of voltage control of MV converter
k_{pc}	Proportional gain of DER current control
k_{pdc}	Proportional gain of dc voltage control of MV converter
$k_{p,i}$	Proportional gain of ST current inner loop
k_{pMV}	Proportional gain of current control of MV converter

$k_{p,o}$	Proportional gain of ST voltage outer loop
k_{ppll}	Proportional gain of PLL
k_{rc}	Control gain of (C/FO)RC
k_{rMV}	Control gain of harmonic control of MV converter
k_{rLV}	Control gain of harmonic control of LV converter in $dq0$ frame
k_{rLVh}	Gain of h -order resonant controller of LV converter in abc frame
L	Period of a periodic signal
L_f	Filter inductance of ST LV converter
L_{f1}	Converter-side filter inductance of DER converter
L_{f2}	Grid-side filter inductance of DER converter
L_g	Grid inductance
L_{MV}	Filter inductance of ST MV converter
L_n	Inductance of neutral line of ST LV converter
L_r	Inductance of tank circuit
m_{MV}	Modulation index of ST MV converter
m_{MV1}	Modulation index related to fundamental of MV converter
$m_{MV(n-1),(n+1)}$	Modulation index related to $n - 1$ th and $n + 1$ th harmonics of MV converter
m_{LV}	Modulation index of ST LV converter
m_{LV1}	Modulation index related to fundamental of LV converter
$m_{LV(n-1),(n+1)}$	Modulation index related to $n - 1$ th and $n + 1$ th harmonics of LV converter
N	Order of CRC
n	Ratio of high-frequency transformer
N_i	Integer order of FORC
N_2	Steps of PLL delay
p	Instantaneous active power
P_1	Nominal active power of DER
P_2	Active power of DER during ancillary services
P_{dab}	Power transferred through DAB
P_{dc}	Output of dc-link controller
P_{max}	Maximum power transferred dc/dc converter
P_{min}	Minimum power transferred dc/dc converter
P_{ref}	Active power reference
$p(s)$	Vector used in VF
Q	Digital LPF for CRC
q	Instantaneous reactive power
Q_1	Nominal reactive power of DER
Q_2	Reactive power of DER during ancillary services
Q_{ref}	Reactive power reference
q_m	Initial poles of VF
R	Reference input
r_m, \tilde{r}_m	Coefficients of rational function of VF method
R_d	Damping resistor
R_{MV}	Parasitic resistor of filter of MV converter

R_{MVDC}	Equivalent resistor of MVDC connection
R_n	Remainder of n -th order FD
R_v	Virtual resistor
S	Switching signal of power converter
s	Instantaneous apparent power
S_n	Rated power of power converter
T_{dab}	Time constant of DAB
T_I	Time constant of current control integrator of MV converter
T_{Idc}	Time constant of dc voltage control integrator of MV converter
T_m	Impedance ratio at PCC
T_{MV}	Time constant of MV converter's filter
T_s	Sampling time
T_{xdc}	Three sampling times, defined for the dc voltage control design
u_{MV}	Reference voltage of MV converter
U_r	Control output of CRC
v	Grid voltage
v'	Transformed grid voltage
v_1, v_2	Primary and secondary voltages of high-frequency transformer
$v_{dc,ref}$	Reference voltage of dc-link of DER converter
$v_{eq,g}$	Equivalent voltage of distribution grid
v_f	Rational function of VF method
V_h	Voltage amplitude for frequency sweep
V_{LV}	Voltage amplitude of LV grid
v_{LV5}	5th harmonic voltage content of LV grid
v_{LV7}	7th harmonic voltage content of LV grid
v_{LVDC}	dc-link voltage of ST LV converter
$V_{LVDC,ref}$	Reference voltage of ST LV dc-link
v_{MV}	Voltage of MV grid
v_{MVDC}	dc-link voltage of ST MV converter
$V_{MVDC,ref}$	Reference voltage of ST MV dc-link
v_n	Rated voltage of power converter
v_r	Reference voltage of DER converter seen by grid
v'_r	Reference voltage of DER converter seen by PLL
v_{ref}	Reference voltage of ST LV converter
$v_{ref,hf}$	Voltage reference at f_n
v_{rms}	rms value of voltage
v_{ST}	Voltage of ST LV converter
Y	System output
$Y(s)$	Equivalent admittance of DER converter
Y_{eq}	Equivalent admittance of LV grid
$Y_{eq,AL}$	Equivalent admittance of active load converter
$Y_{eq,DER}$	Equivalent admittance of DER converter
$Y_{eq,PL}$	Equivalent admittance of passive load

Y_f	Transfer function of FIR
$Z_{eqST,LEF}$	Equivalent impedance of ST LV converter with LEF-based active damping
$Z_{eqST,LPF}$	Equivalent impedance of ST LV converter with LPF-based active damping
Z_f	Impedance of ST output filter
Z_{ff}	Impedance of DER output filter
Z_g	Grid impedance
Z_{in}	Input impedance of LV grid
Z_l	Line impedance between ST LV converter and PCC
Z_{ll}	Line impedance between DER and PCC
Z_o	Output impedance of ST LV converter
α	Phase lead compensation angle (rad)
φ	Phase shift of DAB
$\lambda_{1,2}$	Eigenvalues of characteristic loci
ω_0	Fundamental frequency of PLL (rad)
ω_c	Cut-off frequency (rad)
ω_f	Phase lead compensation frequency (rad)
ω_n	Natural frequency of a second-order system (rad)
ω_{ref}	Reference frequency of LV grid (rad)
ω_{res}	Resonant frequency of LV grid (rad)
ϕ_{max}	Phase lead compensation (rad)
σ	Real part of dominant pole
$\sigma(s)$	Scalar used in VF
θ_0	Actual phase angle
θ'	Phase angle of PLL
$\Delta\theta$	Phase jump of grid voltage
$\Delta\theta'$	Phase displacement between grid phase and PLL detected phase
Θ_1	Terms related to synchronization during small phase perturbation
Θ_2	Terms related to synchronization during large phase perturbation
$\Delta\theta_p$	Initial grid phase perturbation
ζ	Damping ratio of a second-order system
ζ_d	Damping ratio of dominant pole

Abbreviations

ST	Smart Transformer
DER	Distributed Energy Resource
STATCOM	Static Synchronous Compensator
OLTC	On-load Tap Changer
HV	High Voltage
MV	Medium Voltage
LV	Low Voltage

PLL	Phase-locked Loop
FORC	Fractional Order Repetitive Control
EV	Electric Vehicle
ACC	Alternating Current Control
BESS	Battery Energy Storage System
DSO	Distribution System Operator
SST	Solid-State Transformer
ICT	Information and Communication Technology
MG	Micro Generator
WT	Wind Turbine
PV	Photovoltaic
AMI	Advanced Metering Infrastructure
IED	Intelligent Electronics Device
SRF	Synchronous Reference Frame
SOGI	Second-order Generalized Integrator
FLL	Frequency-locked Loop
NPC	Neutral-Point Clamped
MMC	Multilevel Modular Converter
CHB	Cascaded Half Bridge
PI	Proportional Integral
PR	Proportional Resonant
HPF	High-Pass Filter
DAB	Dual Active Bridge
SRC	Series Resonant Converter
UPS	Uninterrupted Power Supply
PCC	Point of Common Coupling
RFF	Reference Voltage Feedforward
MFF	Measured Voltage Feedforward
CC	Capacitor-current
IC	Inductor-current
LC	Load- and inductor-current
SCR	Short-circuit Ratio
PWM	Pulse Width Modulation
CCF	Converter-current Feedback
GCF	Grid-current Feedback
RTDS	Real Time Digital Simulator
FACTS	Flexible Alternating Current Transmission System
DFT	Discrete Fourier Transform
LPF	Low-pass Filter
LEF	Lead Element Filter
VF	Vector Fitting
PF	Power Factor
BW	Bandwidth

ADC	Analog-to-digital Converter
CVR	Conservation Voltage Reduction
IMP	Internal Model Principle
CRC	Conventional Repetitive Control
FD	Fractional Delay
FIR	Finite Impulse Response

1 Introduction

This chapter motivates the smart transformer (ST)-fed grid and its voltage control as well as stability analysis, and formulates the research proposal of the thesis. The structure of the thesis is explained and the publications related to the different chapters are highlighted.

1.1 Motivation for ST-fed Grid

The increasing installation of distributed energy resources (DERs) in recent years is expected to have a significant impact on the conventional power system. The power generation of DERs can benefit the distribution grid to some extent, for instance, release the burden of power transmission and reduce the power losses. Nevertheless, these advantages are valid when the penetration level is limited. In Germany for example, the share of electricity produced from DERs is about 30 % in 2015 and the government is working towards an ambitious plan that aims to achieve 80 % share of gross electricity production in 2050. When the penetration level of DERs is high, the integration of DERs challenges the hosting capacity of the grid and arises technical and economical problems. From a energy management standpoint, power flow in a distribution grid could be utterly changed by the power injection of local DERs, leading to changes of planning, operation, and protection of the grid. From the control point of view, the massive connection of DERs aggravates the severity of energy management, increasing the complexity of power control and power flow optimization. Moreover, critical issues such as voltage limit violation, current congestion, unintentional islanding could emerge due to the intermittent nature of DERs. Furthermore, high level penetration of DERs introduces considerable amount of power electronics interfaces, for instance, grid converters, which employ control and output filters, and therefore could incur problems like control interactions, resonances, power quality violation, and harmonic instability.

Several solutions have been proposed in the literature to address the issues. For system level, various systematic solutions like microgrids, multi-carrier energy systems, and demand management, have been proposed, to enhance the hosting capability and energy management when considerable amount of DERs are connected, meanwhile the current congestion and unintentional islanding problems can be alleviated. For device level, various dynamic voltage regulators including capacitor banks, static synchronous compensator (STATCOM), static VAR compensator, and on-load tap changer (OLTC) have been installed, to regulate the grid voltage under different level of DERs penetration. Moreover, active filter and active damper have been introduced to the grid so that the power quality violation and harmonic instability can be largely avoided. To well coordinate system and device level solutions, communication infrastructures including data center and communication networks are developed in the grid.

Different from the existing solutions, each of which can target one or some specific issues, the ST provides a systematic solution to address all the above-mentioned issues at

the same time and facilitate management of distribution grid. Essentially, the ST is a power-electronics-based solid-state transformer, being adopted as intelligent substation with control and communication functionalities, which interfaces medium voltage (MV) grid and low voltage (LV) one. Compared to the conventional distribution grid, the ST-fed grid offers connection to hybrid grid and is able to significantly improve the demand-response balance. In addition, various ancillary services can be provided to MV/LV grids, which make it possible to increase the reliability and hosting capacity of the electric grid. More importantly, these upcoming services enable the ST-fed grid to more rapidly adjust resources to meet the evolving and unpredictable requirements from utility and customers.

1.2 Motivation for Voltage Control of ST-fed Grid

The ST-fed grid could help solving system-level challenges, however the ST represents control-level challenges itself. One of the main challenges of the ST comes from its LV grid: the LV ST-fed grid is likely to suffer from the interactions between ST LV converter and the increasing grid-converter-based devices. These interactions including the control interaction (i.e., interactions between the ST voltage control and different power/current controllers of local converters), synchronization interaction (i.e., interaction between the ST voltage control as well as line impedance and grid synchronization of local converters), and resonance interaction (i.e., interaction between the ST filter and output filters of local converters). Another main challenge is the control performance degradation when the ST offering ancillary services to grid. For instance, when overload or reverse power flow happens, the ST LV converter can change the LV grid frequency with the purposes of achieving power sharing among different DERs and establishing power balance between production and consumption of LV grid. However, the harmonic elimination capability of the voltage control would be compromised during frequency variation. This leads to the power quality violation and value degradation of ancillary services.

To cope with the challenges, modeling, analysis, and design of voltage control for ST LV converter considering the grid features are necessary. Previous research works for voltage control design and analysis are mainly for voltage-controlled applications supplying loads in a limited dimension, for instance, uninterruptible power supply. Thus, the interactions and the grid features have been seldom considered in these works. On the other hand, most of the existing voltage control strategies for grids/microgrids are usually designed for the fundamental frequency and can hardly maintain acceptable performance during frequency change.

With these considerations, a comprehensive model and analysis on different voltage control strategies are required by including the new features like interactions with grid converters and extended grid size. Optimum voltage control and design considerations are expected to be obtained for the stable operation of the ST-fed grid. In addition to the fundamental voltage control, harmonic elimination scheme has to be designed and able to adapt to frequency variation.

1.3 Motivation for Stability Analysis of ST-fed Grid

The interactions mentioned in the previous paragraph tend to have instability issues, which are characterized by harmonic distortions or oscillations, typically ranging from hundreds of hertz to kilohertz. Modeling and stability analysis of a ST-fed grid are the key to well study the stability issues caused by different aspects. One powerful methodology to investigate stability issues in power-electronics-based power system is the impedance-based stability theory. Impedance-based stability theory uses the ratio between grid impedance and the equivalent impedance of the studied plant (e.g., grid converters) to justify the stability condition of the overall system. The theory was firstly used in a microgrid, where a grid-forming converter and two grid-feeding converters construct the whole system. By using the impedance-based approach, the stability problems of such a microgrid can be identified based on the developed impedance-based model, which reduces computation burden comparing with the other analytical methodologies, for instance, state-space model and eigenvalue analysis.

For the ST-fed grid, not only the stability issues incurred by the above-mentioned factors need to be identified by using the impedance-based approach, but also the stability problems could be addressed or largely avoided by control and services. One possibility to alleviate the stability issues in LV ST-fed grid is to apply control schemes (e.g., active damping, virtual impedance) to the ST LV converter to modify the equivalent grid impedance. In this way, the ratio between grid impedance and the equivalent impedance of LV grid is possibly moving from the unstable region to the stable one. Furthermore, the ST LV converter is able to be functioned as an impedance estimator with the aid of frequency analysis algorithms so that the ratio between the grid impedance and the LV grid impedance can be estimated online, which facilitates real-time stability analysis when intermittent devices integrating with the grid.

1.4 Research Proposal

This thesis aims to work on four different targets:

Target I: Modeling and control of ST LV converter for stable operation

The first objective is to model the ST LV converter and the connected LV grid, and study the control performance and system stability when different voltage control strategies for LV converter are used. The outcomes of this task are to find an optimal voltage control strategy of the ST LV converter and control considerations for the LV ST-fed grid for stable operation.

Target II: Resonance damping and identification of LV ST-fed grid

The second research objective is to investigate the stability issues caused by the resonances in a ST-fed grid, and offer solutions to damp the grid resonances by means of ST LV converter. The outcomes of this task are to propose active-damping-based stabilization methods which

can be seamlessly integrated with the voltage control strategy of ST LV converter, and an online resonance identification method that facilitates the stabilization methods adapting to resonance variation.

Target III: Modeling and stability analysis of phase-locked loop (PLL)-synchronized converter

The third research objective is to consider the PLL effects of the interfaced grid converters to the performance and stability of the ST-fed grid. The outcomes of this task are to develop an accurate model of grid converter considering the effects of PLL, and use it for harmonic stability analysis. Stabilization method to address the PLL-related issue is proposed by means of the ST LV converter.

Target IV: Frequency adaptive control of LV ST-fed grid

The fourth research objective is to maintain good power quality of ST-fed grid during frequency variation. The frequency variation of the LV ST-fed grid is due to the provision of ancillary services, for instance, services for overload and reverse power flow. The outcome of this task is to design a frequency adaptive voltage control strategy for the LV converter, guaranteeing power quality and stable operation.

1.5 Structure of the Thesis

The structure of the thesis is shown in Fig. 1.1.

The concept of smart transformer is introduced in Chapter 2, aiming to systematically address the all grid issues. It can optimally manage the grid and meanwhile offer ancillary services, and the control structure as well as communication requirements of the selected ancillary services are presented in this chapter.

Detailed control strategies for the three-stage ST is described in Chapter 3, in particular, the control design procedures of the MV and LV converters are explained. Four issues related to the LV converter as well as the LV grid in control level are discussed in this chapter.

Chapter 4 aims at addressing the first control issue: control interaction and harmonic instability. Different multiloop voltage control strategies for the LV converter and different control strategies for the grid converters in LV grid are reviewed. The performance and stability of the LV ST-fed grid are evaluated when different control combinations are applied, by using generalized Nyquist criterion. An optimal voltage control strategy for LV converter and control considerations for other components of LV grid are presented in this chapter.

Chapter 5 aims at addressing the second control issue: resonance damping and identification. The stability issues of a LV grid caused by the resonances are described in this chapter. To better reveal the issues in frequency domain, the combination of block diagram matrix and impedance-based model of grid converter is introduced and Nyquist stability criterion is utilized to identify the critical points. Active damping based impedance reshaping methods by

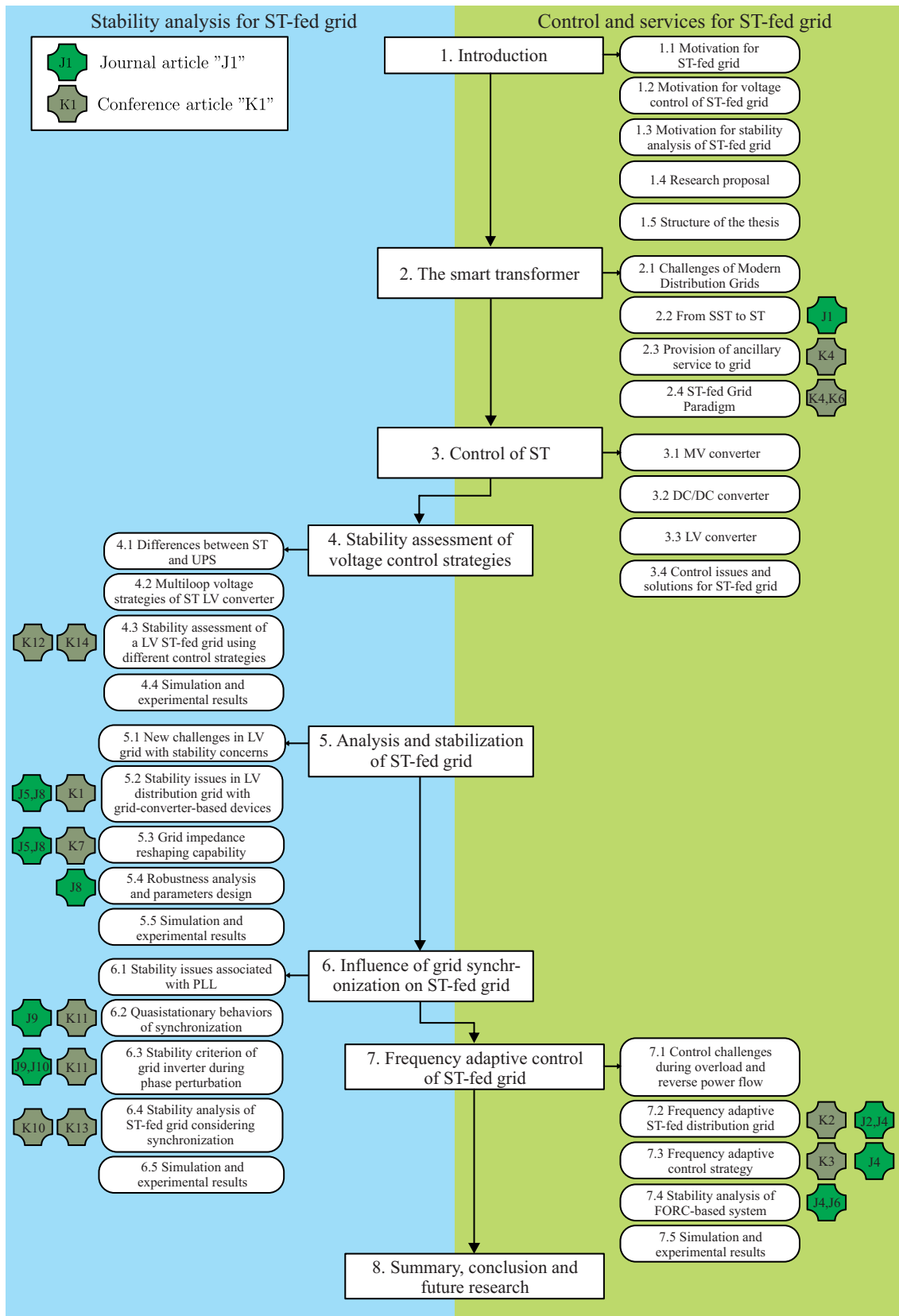


Figure 1.1: Structure of the thesis and the related publications.

means of ST LV converter are illustrated, which are able to stabilize the LV grid. Online resonance identification based on vector fitting is proposed and equipped with the stabilization methods, in order to adapt to the resonance variation.

Chapter 6 aims at addressing the third control issues: modeling and stability of grid converter considering synchronization. A higher-order model of PLL-synchronized grid converter is developed in this chapter, which can more accurately describe the system behavior (especially for stability analysis) during large phase perturbation. The effects of the grid synchronization on the ST-fed grid with stability concern is explained and a virtual-impedance-based stabilization method via the ST LV converter is proposed to address the PLL-related stability issues.

Chapter 7 aims at addressing the fourth control issues: harmonic control strategies for grid frequency variation. This issue comes with the frequency variation during some ancillary services, for instance the services for overload and reverse power flow. To offer good power quality, a frequency adaptive control - fractional-order repetitive control (FORC) is proposed in this chapter and implemented in the voltage/current control systems of the ST-fed grid. The stability issues during frequency variation are discussed and the stability range of the FORC is provided.

In Chapter 8, the results are summarized and concluded before an outlook on future work is given.

1.6 Assignment of Publications to the Chapters of this Thesis

The publications related to this thesis are assigned to the different chapters in the following, which is additionally visualized in Fig. 1.1. A complete list of the publications related to this thesis is given in the attachment.

- Chapter 2 presents the concept of ST and ST-fed grid considered in [J1] and different scenarios, control and communication requirements reviewed in [K4] and [K6]
- Chapter 4 compares different multiloop voltage control strategies with stability concerns considered in [K12] and [K14]
- Chapter 5 is based on the conference publications [K1], [K7] and the journal articles [J5], [J7]
- Chapter 6 contains the second-order model of grid converter developed in the conference publication [K11] and the journal articles [J9], [J10], and the stability analysis depicted in [K10] and [K13]
- Chapter 7 includes the frequency adaptive ST-fed grid scenario and the FORC control design based on the conference publications [K2], [K3] and the journal articles [J2], [J4], [J6]

2 The Smart Transformer

This chapter starts with the grid level issues caused by the DERs, EV charging stations and other devices with grid converters. The Smart Transformer concept is then introduced to address the grid issues in a general way. Selected ST-fed grid paradigms and grid services are illustrated in this chapter.

2.1 Challenges of Modern Distribution Grids

The contemporary distribution network is undergoing major changes. One major change is to introduce massive new electric components, like DERs and electric vehicles (EVs), in the recent decades. The concept of DERs is usually referring to any generator of limited size (roughly 10 MW or less) which is interconnected at the substation, distribution feeder or customer end [1]. Common DERs include photovoltaic, wind turbines, fuel cells, small and micro-turbines, and internal combustion engines. Due to the benefits to the distribution grid [1], the share of electricity produced from DERs is increasing drastically these years. Take Germany for example, the share of electricity produced from DERs is about 30 % in 2015 and the government is working towards an ambitious plan that aims to achieve 80% share of gross electricity production in 2050 [2]. The DERs provide several benefits to the distribution grids and the transmission grids, including 1) reduce transmission and distribution capacity; 2) reduce transmission losses; 3) improve reliability of utilities; 2) voltage support and power quality improvement.

However, the increase of DERs and EVs challenges the hosting capacity of the distribution grid and arises technical and economical problems. In a traditional distribution grid, energy is flowing from the main grid or bulk power system to the medium voltage grids and low voltage ones. When massive amount of DERs and EVs will be integrated in the distribution grid, the load consumption will be satisfied locally, the power flow in the power system would be changed, from grid management point of view. This impacts on the power system in terms of planning, operation, and protection [3, 4]. The intermittent nature of DERs and EVs further aggravates the severity of energy management, increasing the complexity of power control and power flow optimization. Moreover, control systems and passive filters are usually required for the grid-interfaced converters of DERs. The interactions among these control systems can incur potential stability and power quality issues [1]. Massive passive filters of the grid converters also introduce potential resonances and further worsen the harmonic stability issues [5].

In general, the main challenges of DER penetration to the distribution grid can be summarized by [3, 4, 6, 7, 5, 8, 9]:

- control interactions among converters
- resonances and power quality violations
- cables and transformer overload

- reverse power flow and voltage violations
- decreased system inertia
- greater demand variability
- higher fault current and protection system coordination

These issues compromise the stable operation and deteriorate the power quality of the distribution grid, and meanwhile create difficulties in power and load management. To address these issues, several solutions have been proposed in the literature, for example, harmonic stability assessment to identify the instability caused by control interactions; resonance damping methods to alleviate the resonance issues; power/load management with the aid of control and battery energy storage system (BESSs) to limit reverse power flow and avoid transformer overload. However, all the solutions in the literature target at specific grid issue. To deal with each issue, each solution requires specific control structure, algorithm, and infrastructure. None of them provides a general and systematic approach to solve all the issues.

Different to these solutions, the Smart Transformer concept, is a systematic approach trying to address all the issues at the same time and explore the grid potentials. This concept is firstly proposed by the HEART project [10]. The main idea is to use a solid-state transformer (SST) with control and communication functionalities that not only to step-down the voltage level from MV grid to LV one, but also to provide ancillary services to both MV and LV grids upon the requests from the utilities and customers. The ST will behave as a central point in a distribution grid, regulating energy flow and information flow simultaneously, and coordinating with intelligent devices in the grid. To participate grid management and provide ancillary services, appropriate control architectures, control strategies, and suitable communication technologies are the three key factors, which will be discussed in this chapter.

2.2 From Solid-state Transformer to Smart Transformer

A SST, or power electronic transformer, is essentially an ac-to-ac converter. The earliest concept of SST can be traced back to the patent of McMurray in 1968, which conceives a device based on solid-state switches that behaves in the same manner as a conventional power transformer [11]. The concept was further extended by Brooker in 1980, which solicits the SST to provide the voltage transformation functions of a conventional electrical power transformer with waveform conditioning capability [12]. A practical application for the SST firstly emerge in 1990 in traction systems, where weight and volume reduction are highly desirable. In contrast, the classical solutions were usually based on low frequency transformers, which led to a very bulky, heavy, and inefficient system. In this regard, SST technology could offer several benefits, such as volume and weight reduction (from 20 to 50 %) and efficiency improvement (from 93 to 96 %).

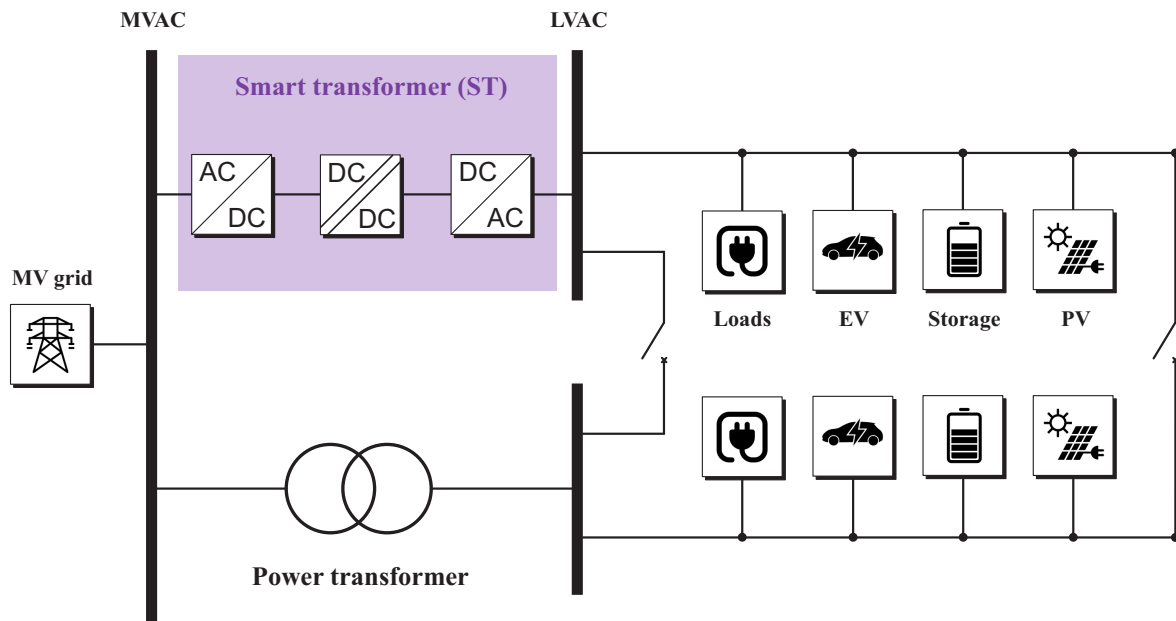


Figure 2.1: A Smart Transformer-fed grid.

With the help of the latest technologies of power electronics, and applying information and communication technology (ICT) to distribution grid, the potential to implement new functions in the forms of ancillary services on the SSTs is much higher. The SST is expected to replace the conventional power transformer, connecting the MV grid to the LV grid, and offer dc connectivity and services to both LV and MV grids. The combination of control and communication functions make the device a smart SST or, a smart transformer.

In this context, a ST in substation can play the key role in the distribution grid. By using optimized grid management strategies, ST can benefit the voltage control, power regulation, and energy storage management of BESSs. A benchmark grid is shown in Fig. 2.1, coupling with a variety of DERs, EVs, storages and loads. Being a three-stage SST, the MV side and LV side of ST are decoupled up to a certain extent depending on the installed storage, which essentially block the propagation of wideband harmonics and disturbances from one grid to the other.

The ST can not only independently operate in a radial network configuration, similar to the conventional power transformer, but also in a meshed grid operation. During the meshed grid operation, the ST can mesh the LV grids, being ringed at the LVAC buses or at the terminal of the LV ac feeders. The meshed grid configuration has high potential to optimize the power flow in the network, avoiding or postponing the reinforcements of distribution grids.

2.3 Provision of Ancillary Services to Distribution Grid

The ST can provide ancillary services to different levels of a distribution grid: the MV grid, the LV grid, and in future the dc grid. A ST-fed benchmark grid with the ancillary services is shown in Fig. 2.2, along with the control and communication requirements. It is important stressed that the STs will not likely be mass produced in the short term, and they are expected

to be installed in only a few power grid nodes. In this regard, the ST in the benchmark grid is being interconnected to the MV grid in parallel with other two distribution transformers.

Control scenarios and associated communication are two essential elements for the ST-fed grid, which ensures a more reliable and resilient electric grid and better quality services [14]. As shown in Fig. 2.2, the ST can host the data center which offers services to the grid. On the MV side, the ST regulates current absorption from the utility, delivering active power demanded from the loads in the LV grids. The reactive power represents a degree of freedom for the ST: it can be controlled separately from phase to phase and is able to be decoupled from the LV reactive power request due to the dc links. This feature enables a basic service - the possibility to work with unity power factor - and advanced services including harmonic compensation and voltage support on the MV side. With reactive power compensation, the ST can support the voltage profile in the MV grid in critical conditions and solve grid congestion by active on single phase base. In case of high harmonic distortion, the ST can work as an active power filter, reducing the stress on the HV/MV transformer and improving the power quality of the MV grid. Another ancillary service of the MV side dc can be the reverse power flow limitation. When the power generation of the DERs in the LV grid exceeds the power consumptions of the loads, the power flow reverses in the MV/LV substation, leading to a voltage increase in the MV grid. The ST can interact with local generators, increasing the grid frequency to decrease the power injection of the DER, thereby avoiding the reverse power flow condition. The dc/dc stage interfaces the two dc links. In particular, the MV dc link is controlled by the ac/dc stage, which also manages the MV dc connection. The dc/dc converter handles the balancing between the two stages, also managing the LV dc grid. In the LV side, the ST controls the voltage waveforms on the grid. The ST has to generate sinusoidal and balanced three phase voltages at substation level independently from the connected load. Similar to the MV side, additional services can be offered to the grid by interacting with local loads and generators by means of voltage amplitude and frequency control. These parameters can influence load power consumption and generation. Possible applications are overload ST control and reverse power flow limitation control. The ST has limited overload capability and the constraints lie on the semiconductor temperature. If the current increases, the semiconductor temperature can exceed the maximum limit. Thus, the ST can decrease grid frequency to activate the generator's droop controllers and increase generation. If insufficient, the ST can exploit the dependency of the consumed active and reactive load powers on the voltage.

According to the control requirements listed in Fig. 2.2, MV and LV customers can flexibly subscribe services tailored by ST while have very limited impact on the other feeders/grids. From the grid resilience perspective, these services effectively avoid the cascaded blackout, achieving a self-healing grid [15]. Each ancillary service requires not only basic control strategies but also other supporting control strategies. For instance, for the grid identification and resonance damping service, basic control strategy like voltage/current multiple-loop control is needed for the LV converter, active damping and grid impedance measurement are additionally required to achieve the service. In addition, supporting tools such as advanced metering infrastructure (AMI), intelligent electronics devices (IEDs), ICT, etc., should be

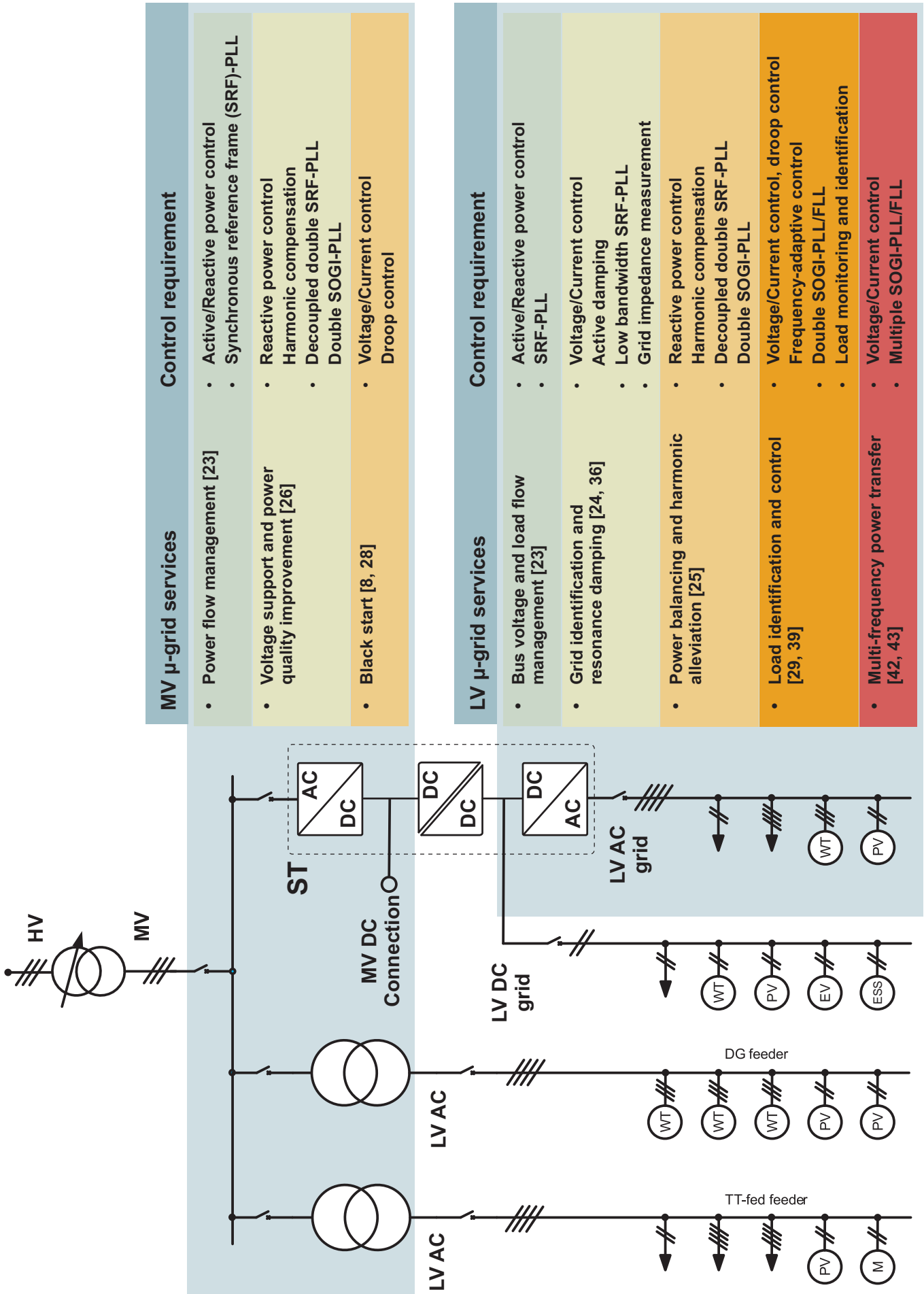


Figure 2.2: ST-fed grid with associated services [13].

integrated with the ST-fed grid to facilitate services and reinforce the grid.

The communication network in the ST-fed grid guarantees more robust data acquisition and more direct control objectives. Once a reliable communication network is realized, more competitive services can be applied to the MV and LV customers. The ST is supposed to be the key component to emerge and manage all the available resources in terms of services, algorithms, and grid data within the ST-fed grid, and is able to allocate them to the distributed appliances in need or allow distributed appliances to access these shared resources. The virtual aggregation of resources is especially suitable for the services which rely on considerable data processing capacity and abundant grid information. It can avoid additional control and measurements implemented locally, which saves the cost and maintenance of local appliances. More importantly, these upcoming services enable the ST-fed grid to more rapidly adjust resources to meet the evolving and unpredictable requirements from utility and customers.

2.4 ST-fed Grid Paradigm

To adapt to the evolution of future electric grids, the vision of the application of ST in the electric grid are different from either the centralized or the decentralized paradigms in history. It is expected that the ST could provide a semi-decentralized solution to the grid since the ST is able to interact with both the utility components and also the local customers' appliances on the basis of their needs. In general, the advent of ST drives the control center delegating more functionalities to the lower level, so that 1) relieves the control and data burdens of control center; 2) empowers the consumers with more choices and better services. In this section, control structures for selected ancillary services will be reviewed, associating with control schemes and requirements.

2.4.1 Node Voltage and Power Flow Management

One of the challenges posed by the penetration of renewables is the reverse power flow. As a result, overvoltage and current congestion would occur, causing the disconnection of DERs and potential damage to local appliances. In [16], this problem is addressed by equipping a ST with the capability of node voltage management. When a ST is associated to the DERs, the node voltage as well as current flow can be well regulated by curtailing the active and reactive power. Moreover, the ST allows the voltage and power profiles to be managed in per-phase mode, enabling the unbalanced power injection to the grid in case of the presence of unbalanced overload of MV grid, with voltage and current limit violations. In this way, the distribution grid can be managed in a more efficient way than in the case of the traditional transformer is adopted.

The system configuration and control structure are illustrated in Fig. 2.3. The ac/dc power converters of ST are controlled by a power control outer loop and a current control inner loop

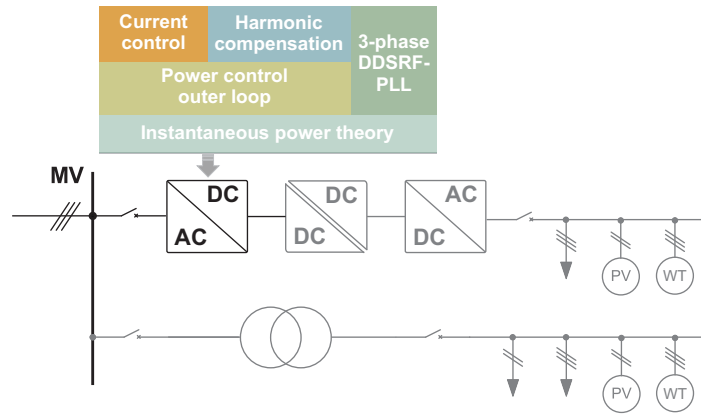


Figure 2.4: Voltage support and power quality improvement by means of ST.

control mode to voltage control mode so that it can provide stiff voltage to other feeders when the HV and MV breakers are switch off. As a result, the other feeders remain connecting to the grid by shedding non-critical loads. The scenario operation demands sufficient grid data during the transient stage to make sure the ST can fast and seamlessly take the responsibility of supporting the overall distribution grid. This scenario is particularly helpful to supply critical loads and black start procession.

2.4.3 Grid Identification and Resonance Damping

The massive integration of DERs poses resonances resulting compromised stability and power quality. In a ST-fed distribution grid, the ST offers the opportunity to identify and dampen the grid resonances [21, 22]. Seen from Fig. 2.5, the ST LV side dc/ac inverter can act as a grid impedance measurement and propose tailored active damping solutions. Depending on the characteristics of grid resonance, the ST can offer series active damping by using its dc/ac inverter or solicit one of the DERs providing shunt active damping. Usually, a multiloop-based active damping is used in ST LV side dc/ac to achieve series active damping. The damping factor of the LV grid is determined by the control coefficients of the inductance current inner loop. It is worth noting that the ST series damping is able to attenuate resonances within a wide range (e.g. between 0.1 kHz to 10 kHz) and therefore benefits the vast majority of grid-interfaced appliances.

Unlike the series active damping, the shunt active damping is more likely to deal with the resonances in certain buses. The DER receives the resonance information which is identified and broadcast by the ST, utilizes customized filter-based damping methods to handle it. A study case of DER with the functionality of shunt active damping is presented in [23], where the notch filter active damping is utilized to mitigate the impedance resonance at certain frequency. Based on the accurate impedance information, the DER can participate in resonance damping requiring no trial-and-error iterations. Due to the robustness of notch filter damping, the bandwidth of broadcasting network is not very stringent.

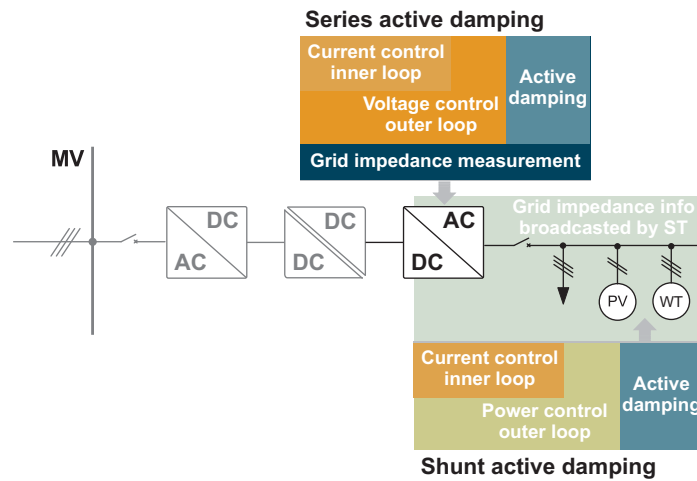


Figure 2.5: Control structure for grid identification and resonance damping scenario.

2.4.4 Load Identification and Control

One of the advantageous aspects of ST is the decoupling between MV and LV grids thanks to the presence of dc links. It allows the ST to modify the LV side voltage waveform to interact with the DERs and loads with very limited impact on the MV grid. In [24, 25], two complementary control algorithms have been proposed to adapt the frequency and voltage to the power generation and consumption in order to achieve better power sharing and deal with some practical issue, such as overload and reverse power flow. Meanwhile, the load/power sensitivity to voltage and frequency should be identified to enable smooth operation during the LV frequency/voltage regulation. With these considerations, a combined load identification and control has been proposed and implemented through the ST [26]. The control structure of the ST as well as DERs for this scenario has been described in Fig. 2.6. Based on the real-time load identification, the LV side frequency/voltage references are accordingly modified by following predefined curves, for example, the power/frequency curve. To inform local DERs, the frequency/voltage information will be broadcast by the ST to the LV grid. Following the frequency information, local DERs are thereby able to change power output by using droop control.

A further application on this topic is the frequency adaptive ST-fed distribution grid [27]. The before-mentioned frequency control is implemented in the ST. A frequency adaptive repetitive control scheme along with a double second-order generalized integrator (SOGI)-PLL are adopted to maintain good voltage/current control performance under variable frequency condition. The proposed system provides a promising approach to address practical issue during load peaks and overcapacity of DERs.

2.4.5 Multi-Frequency Power Transfer

The multi-frequency power transfer concept is derived from the frequency modulation in telecommunication where multiple frequencies are used to transmit information within a medium among several sender and receivers. In presence of ST, more than one frequency

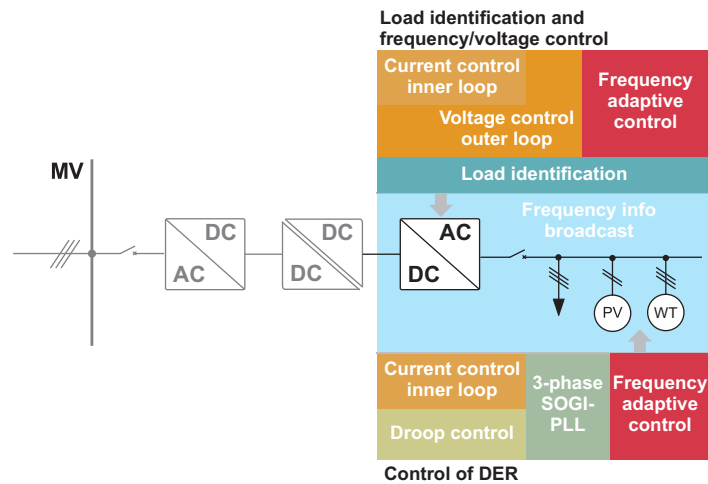


Figure 2.6: Coordinated frequency and voltage overload control of ST-fed grid.

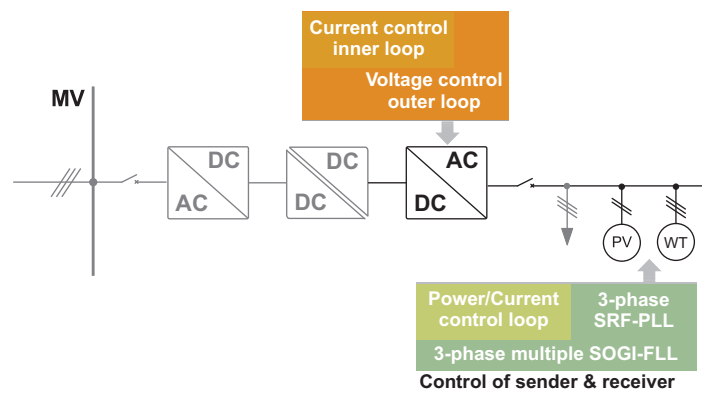


Figure 2.7: Control structures of ST dc/ac converter and power sender as well as receiver in multi-frequency power transfer scenario.

voltage/current waveforms can be modulated and used to send power from one point to another of the LV grid. Unlike the traditional distribution transformer, the harmonics for power transfer has very limited impact on the ST lifetime, ST losses, and MV grid as well as MV breakers. In [28] and [29], fundamental frequency and third harmonic have been chosen as carrier frequencies in a ST-fed distribution grid to achieve the sophisticated power transfer. The basic control structure is shown in Fig. 2.7, where the voltage/current multiloop control is used for LV side dc/ac inverter, while the power control is used for the grid-interfaced converters of DERs. In order to "decode" the power at different frequencies, multiple double SOGI Frequency-Locked Loops (SOGI-FLLs) are employed for frequency detection. Known the frequency, a SRF-PLL with the same characteristic frequency is utilized to detect the phase angle for each frequency. The combination of SOGI-FLL and SRF-PLL facilitates the accurate power transfer and at the same time eases the communication between sender and receiver.

2.5 Summary of the Chapter

The increasing penetration of renewables poses new challenges and research issues on the power grids. This chapter has highlighted a promising approach, the ST-fed grid, to address the coming up issues and enhance the grid capability in terms of hosting capacity, efficiency, reliability, resilience, and safety. To make this futuristic electric network a reality, control scenarios have been proposed, which are exploiting new opportunities and potentials of the existing power system.

In this chapter, the ancillary services provided by the ST-fed grid are introduced and the control requirements are described. For the selected ancillary services, the scenario and control structures as well as control schemes are discussed. In the following chapters, the detailed control strategies to achieve these ancillary services will be given. The basic control schemes like power/current control and voltage/current control for different ST stages will be illustrated in Chapter 3.

3 Control of Smart Transformer

The ST has a three-stage structure as shown in Fig. 3.1, including MV converter stage, dc/dc converter stage, and LV converter stage. For the MV converter, it regulates the power/current absorption from the MV grid and deliver active power demanded from the loads in the LV grid. The dc/dc stage interfaces the two dc links, transferring the power from the MV to the LV side and regulating the voltage of the LV dc-link. For the LV converter, it controls the voltage waveforms of the LV grid to be sinusoidal and balanced independent from the load dynamics. In this chapter, the detailed control strategies of all the three stages will be illustrated. Since the main focuses of this thesis are on the LV converter, the modeling and control design of the LV converter will be analyzed in particular. Existing control issues of the LV converter will be listed in this chapter.

3.1 MV Converter

The candidates of the ST MV converter include the following topologies: neutral-point clamped (NPC) converter, multilevel modular converter (MMC), and cascaded half bridge (CHB) converter, shown in Fig. 3.2. These converters are able to work with medium voltage level (e.g., 10 kV), while using low voltage semiconductor components. For the CHB converter, a series of low voltage CHB cells are connected to reach the voltage level of each phase of a MV grid. Each cell has its own dc/dc converter, meaning the system lacks of a common MVDC connection, which is the main limitation for the upcoming MVDC distribution grid. In contrast, the MMC has the superiority that it offers a common MVDC connection, while it requires bulky dc-link capacitors as well as more complicated control structure.

Since the motivations of this thesis are not about typologies but control systems, the detailed discussions on the hardware will be neglected and a general equivalent converter with the control schemes are provided in Fig. 3.3. The MV converter has two main control objectives: one is to control the voltage of the MVDC connection, and the other is to regulate the power on the MVAC side. To achieve the control objectives, a multiple control structure is used which includes a power and dc voltage outer loop and a current inner loop. Essentially, the control scheme keeps the power balance between the MVAC grid and the MVDC connection. During normal operation, when the ST is operated with unity power factor, the reactive power setpoint of the MV converter (Q_{ref}) is set to be zero. In case of ancillary services, for instance, voltage support or harmonic filtering in MV grid, the ST can provide reactive power or harmonic injection. Usually, the reactive power setpoint can be obtained from a local controller like V/Q droop controller or from a centralized controller; the harmonic injection setpoint can be calculated by a local controller based on the instantaneous $p-q$ theory.

The two-loop control structure for the MV converter is presented in Fig. 3.4, where $V_{MVDC,ref}$ and Q_{ref} are the MVDC voltage and reactive power set-points for the outer loop, the current

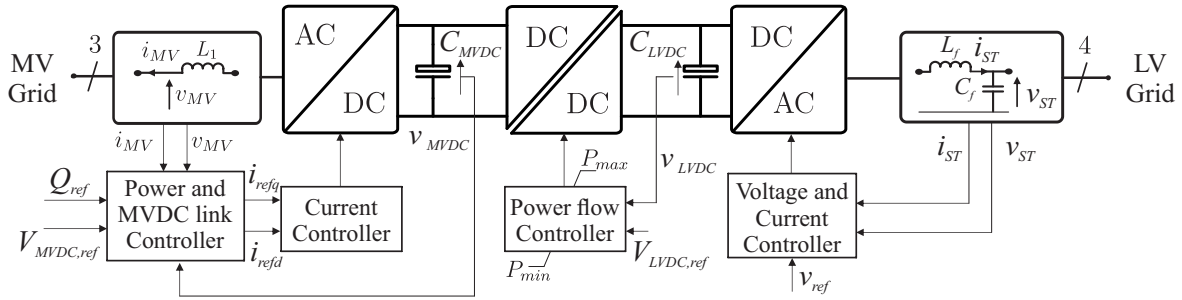


Figure 3.1: Schematic diagram of a three-stage smart transformer.

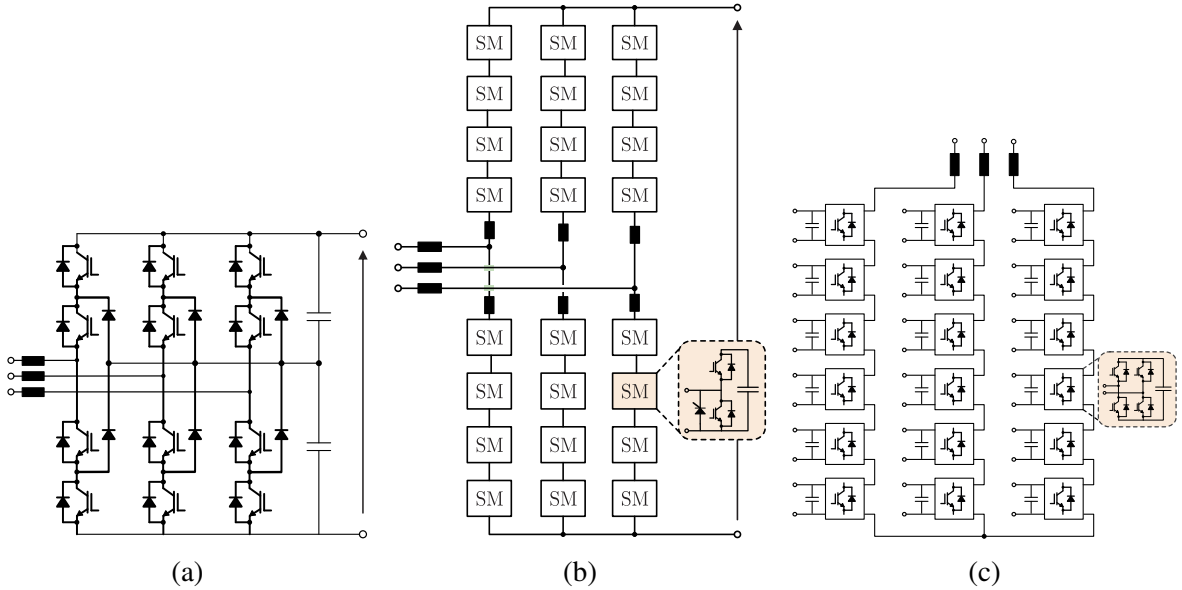


Figure 3.2: Topology candidates for ST MV converter: (a) NPC converter, (b) MMC, and (c) CHB converter.

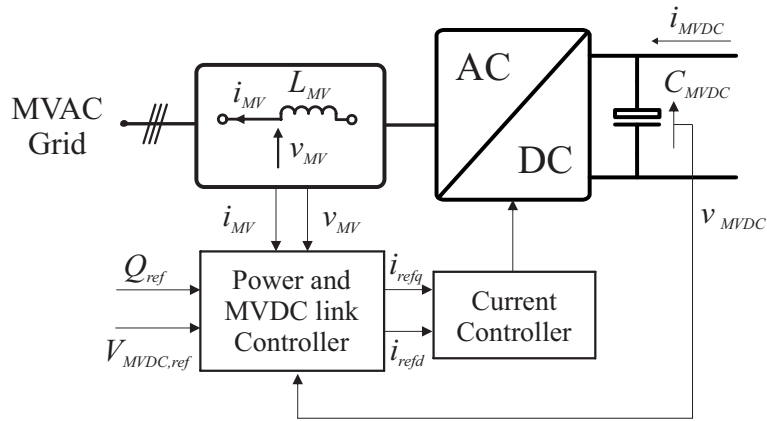


Figure 3.3: Control scheme for the MV converter.

references for the inner loop is generated from the outer loop and the current it then controlled in in dq frame. In detail, the dc voltage control is a PI controller that can track the MVDC voltage reference and create the d -axis current reference i_{refd} ; a common example for the reactive power control is to use an open-loop function linking the desired MVAC grid voltage amplitude v_{rms} to the q -axis current reference i_{refq} . Depending on the required ancil-

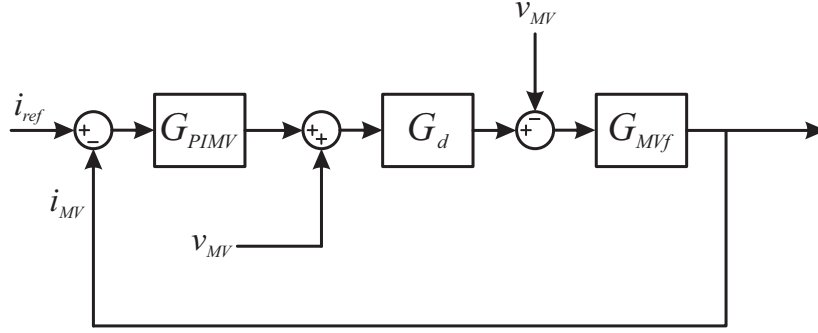


Figure 3.5: Simplified control block diagram for the MV converter current control.

As it is a typical oscillatory second-order system, it yields

$$\omega_n^2 = \frac{2k_{pMV}}{3T_s L_{MV}} \quad (3.4)$$

$$\zeta \omega_n = \frac{1}{3T_s}$$

where ω_n and ζ are the natural frequency and the damping ratio of the system. Choosing to have a system optimally damped, where $\zeta = 0.707$, it leads to $k_{pMV} = \frac{L_{MV}}{3T_s}$.

The second step is to design the control parameters of the dc voltage control outer loop. When the current control loop is adjusted to be optimally damped, the inner loop as well as the plant can be simplified by a first-order approximation as (3.5) within the dc voltage control design procedure.

$$H_{MV} \approx \frac{1}{1 + 3T_s s} \quad (3.5)$$

The transfer function of the MV dc-link can be obtained based on the small-signal modeling. Considering the instantaneous power balance for the MV converter in dq frame under a no-loss condition, the following equation holds:

$$\frac{3}{2}(v_{MVd}i_{MVd} + v_{MVq}i_{MVq}) = -v_{MVDC}C_{MVDC} \frac{dv_{MVDC}}{dt} + v_{MVDC}i_{MVDC} \quad (3.6)$$

The small-signal linearization leads to

$$\frac{3}{2}(V_{MVd}\Delta i_{MVd}) = -V_{MVDC}C_{MVDC} \frac{dv_{MVDC}}{dt} + \Delta v_{MVDC}I_{MVDC} \quad (3.7)$$

where V_{MVd} , V_{MVDC} , and I_{MVDC} are the dc quantities of v_{MVd} , v_{MVDC} , and i_{MVDC} , Δi_{MVd} and Δv_{MVDC} are the small-signal perturbations of i_{MVd} and v_{MVDC} . The steady-state MVDC equivalent resistance can be defined by $R_{MVDC} = V_{MVDC}/I_{MVDC}$. Assuming $V_{MVDC} \cong \sqrt{3}V_{MVd}$, the transfer function from Δi_{MVd} to Δv_{MVDC} (i.e., the plant of dc voltage control) can be obtained as following:

$$\frac{\Delta v_{MVDC}}{\Delta i_{MVd}} = \frac{\sqrt{3}}{2} \frac{R_{MVDC}}{1 - R_{MVDC}C_{MVDC}s} \quad (3.8)$$

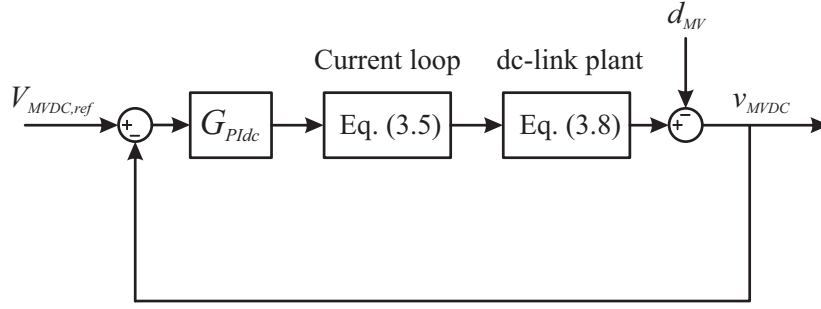


Figure 3.6: Control block diagram for the MV converter dc-link voltage control.

On the basis of the simplified current control system and the MV dc-link, the small-signal model of the dc voltage control loop can be obtained and shown in Fig. 3.6, where $G_{PI_{dc}}$ is the transfer function of the PI controller, and d_{MV} is the disturbances from both the dc-link current and the MV voltage. Based on Fig. 3.6, the open-loop transfer function of the dc voltage control is:

$$G_{MVop} = \frac{\sqrt{3}}{2} \frac{k_{pdc}(1 + T_{Idc}s)}{T_{Idc}s(1 + 3T_s s)C_{MVDC}s} \quad (3.9)$$

obtaining by considering $R_{MVDC}C_{MVDC} \gg 3T_s$, and k_{pdc} and T_{Idc} are the proportional gain and the integral time constant of the PI controller.

Defining $k_{dc} = \frac{\sqrt{3}}{2} \frac{k_{pdc}}{T_{Idc}}$, one can obtain the renewed open-loop transfer function as

$$G_{MVop} = \frac{k_{dc}(1 + T_{Idc}s)}{s^2(1 + 3T_s s)} \quad (3.10)$$

It is worth noting that the phase of the open loop transfer function at the crossover frequency towards -180° when $T_{Idc} = 3T_s$, which indicates the phase margin of the overall system is zero, and thus the system would present unstable behaviors. To obtain the maximum phase margin, which in turn will result in optimum damping of the dc voltage loop, the main idea of the "symmetric optimum" method is to choose the crossover frequency at the geometric mean of the two corner frequencies. In this regard, the Bode diagram shows symmetry with respect to the crossover frequency, as shown in Fig. 3.7.

The open-loop transfer function of (3.10) can be rewritten in the frequency-domain as followings:

$$20\log_{10} |G_{MVop}(j\omega)| = 20\log_{10} \left| \frac{k_{dc}}{(j\omega)^2} \frac{1 + j\omega T_{Idc}}{1 + j\omega T_{xdc}} \right| \quad (3.11)$$

where $T_{xdc} = 3T_s$.

Applying the logarithm properties, one can draw the two separate trends as shown in Fig. 3.8. The double poles trend and the trend with one pole-zero combination are represented by the blue line and the red one, respectively. The magnitude plot of the double poles is the blue line with a slope of -40 dB per decade. For the pole-zero combination, it is expected $T_{xdc} \ll T_{Idc}$, meaning the zero has been moved to much lower frequency than the pole, in order to make a stable situation. The magnitude plot of the pole-zero combination is the horizontal red line at 0 dB since at low frequencies the T_{Idc}/T_{xdc} term is small and can be

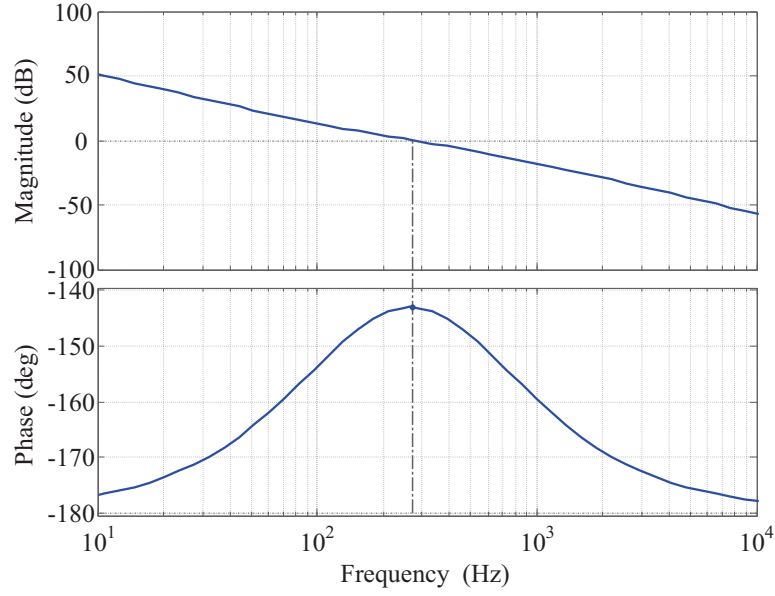


Figure 3.7: Bode diagram of the open-loop transfer function of the dc-link voltage control with the symmetric optimum concern.

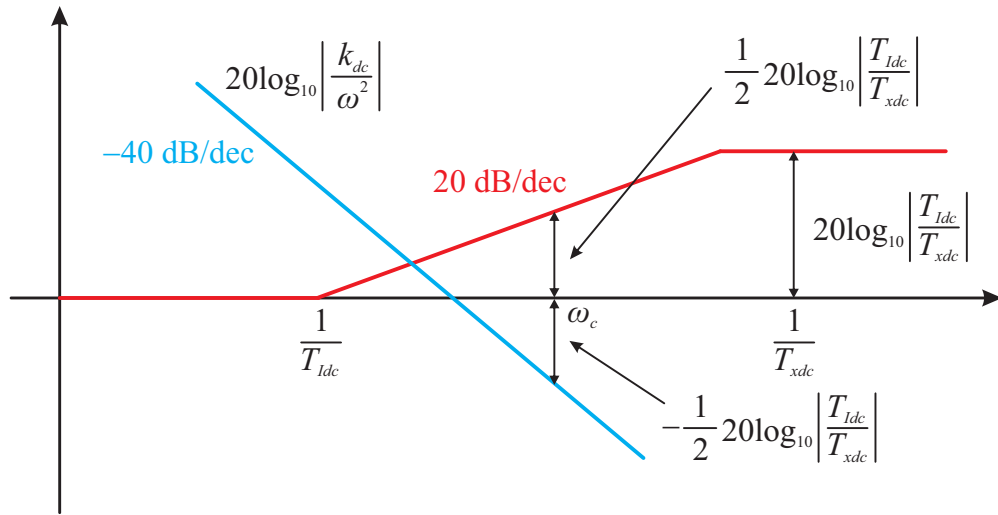


Figure 3.8: Magnitude diagram of the open-loop transfer function of the dc-link voltage control at the neighborhood of ω_c .

neglected; the 20 dB/decade rise of the zero is arrested by the 20 dB/decade drop of the pole, resulting in a horizontal magnitude plot for frequencies above the zero location since at high frequencies the T_{Idc}/T_{xdc} term dominates and the decibel gain expression above simplifies to $20 \log_{10} |T_{Idc}/T_{xdc}|$. According to the "symmetric optimum" method, the transfer function at ω_c should be around 0 dB, which is

$$20 \log_{10} |G_{MVOP}(j\omega_c)| = 20 \log_{10} \left| \frac{k_{dc}}{(j\omega_c)^2} \frac{1 + j\omega_c T_{Idc}}{1 + j\omega_c T_{xdc}} \right| = 0 \quad (3.12)$$

Thus, it leads to

$$\frac{k_{dc}}{\omega_c^2} = \sqrt{\frac{T_{xdc}}{T_{Idc}}} \quad (3.13)$$

Since the cut-off frequency can be calculated by

$$\omega_c = \sqrt{\frac{1}{T_{Idc}T_{xdc}}} \quad (3.14)$$

The coefficient of k_{dc} is then obtained by

$$k_{dc} = \omega_c^2 \sqrt{\frac{T_{xdc}}{T_{Idc}}} = \frac{1}{T_{Idc}T_{xdc}} \sqrt{\frac{T_{xdc}}{T_{Idc}}} \quad (3.15)$$

The proportional gain of the PI regulator is given as

$$k_{pdc} = \frac{2C_{MVDC}}{\sqrt{3}} \sqrt{\frac{1}{T_{Idc}T_{xdc}}} \quad (3.16)$$

In an actual grid, the grid voltage could be distorted due to the presence of harmonic sources. Under this circumstance, the ST MV converter still has to guarantee its three-phase current i_{MV} sinusoidal with low harmonic distortion. The pair of PI controllers in Fig. 3.4 for current control is then not enough for harmonic elimination. To achieve the target, the harmonic controller has to be included in the current control loop which aims at mitigating harmonics in specific frequency range, for instance, 5th, 7th, 11th, 13th, 17th, and 19th harmonics that are common in grid. An example of harmonic controller for 5th-7th harmonic elimination is shown in Fig. 3.9. Here, nested frames, i.e., two frames rotating at 6ω and -6ω , are implemented with the main synchronous frame. It is worth noting that the 5th and 7th harmonics are not possible to be eliminated by using only a 6ω rotating frame, since for 5th harmonic $-5\omega - \omega = -6\omega$ and for 7th harmonic $7\omega - \omega = 6\omega$. In both frames, the received signals after transform are dc signals and thus integrators are implemented to achieve zero steady-state error. During normal operation, the harmonic current references i_{5refdq} , i_{7refdq} are set to zero. Similarly, with proper transform and configuration, other harmonics like 11th-13th and 17th-19th can be mitigated in this way, and the output signals (i.e., $m_{MV(n-1),(n+1)abc}$) from the corresponding controllers can be added to the output signals of Fig. 3.4.

In addition, the ST is able to compensate harmonics generated from other feeders, like an active power filter, based on the instantaneous p - q theory [30]. The instantaneous apparent power can be defined in $\alpha\beta$ frame as

$$s = v \cdot i^* = (v_\alpha + jv_\beta) \cdot (i_\alpha - ji_\beta) = (v_\alpha i_\alpha + v_\beta i_\beta) + j(v_\beta i_\alpha - v_\alpha i_\beta) \quad (3.17)$$

where $v_{\alpha/\beta}$ and $i_{\alpha/\beta}$ are the voltage and current in $\alpha\beta$ frame. The active and reactive power can be sorted in two separate equations:

$$\begin{aligned} p &= v_\alpha i_\alpha + v_\beta i_\beta \\ q &= -v_\beta i_\alpha + v_\alpha i_\beta \end{aligned} \quad (3.18)$$

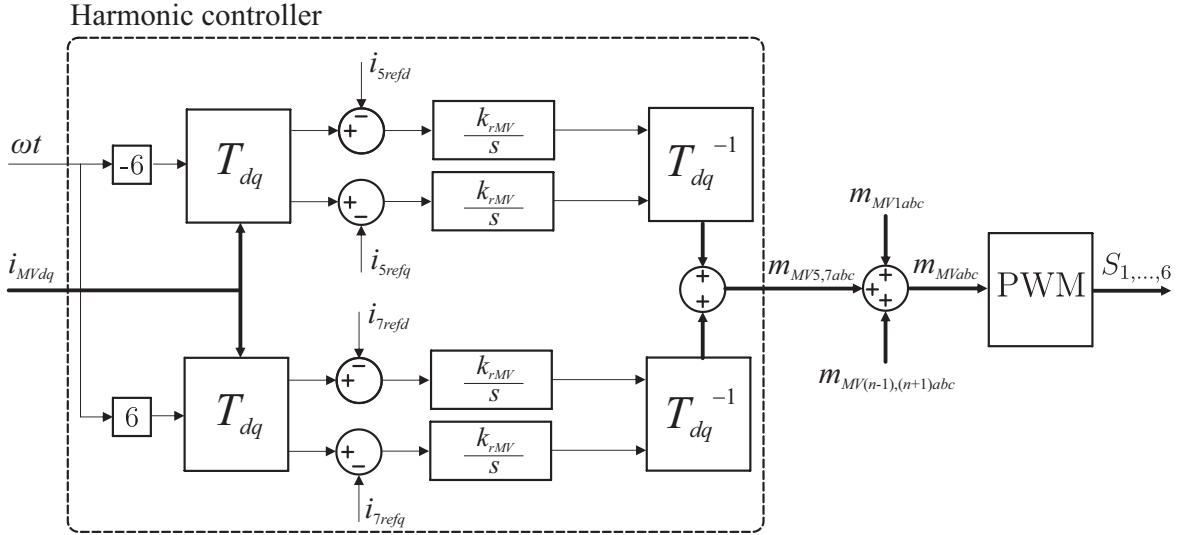


Figure 3.9: Harmonic controller for current control loop with 5th and 7th harmonic elimination using 6th and -6th dq reference frames nested in the main.

which can be rewritten in matrix form as

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (3.19)$$

Provided the instantaneous active and reactive power are known, the current references in $\alpha\beta$ frame can be obtained by inverting the matrix in (3.19), which is

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} p \\ q \end{bmatrix} \quad (3.20)$$

In case of current harmonic content, the instantaneous active and reactive powers include dc components and power oscillations. To compensate the harmonics in grid, the power oscillations must be compensated by the ST MV converter. For this reason, a high-pass filter is implemented to obtain the power oscillations from the power calculations done by (3.19). The outcome is the oscillation components of the instantaneous power (\tilde{p} and \tilde{q}), which are related to the harmonic content and should be compensated by the ST. Meanwhile, the output of the MV dc-link controller (p_{dc}) indicates the power losses of the MV converter, and therefore it should also be counted during compensation. Based on (3.20), the current references for compensation can be calculated by

$$\begin{bmatrix} i_{ref\alpha} \\ i_{ref\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} \tilde{p} + p_{dc} \\ \tilde{q} \end{bmatrix} \quad (3.21)$$

The references in $\alpha\beta$ frame are then transformed to the dq frame so that the current control in Fig. 3.4 with harmonic controller in Fig. 3.9 can be directly applied. The detailed control scheme is shown in Fig. 3.10.

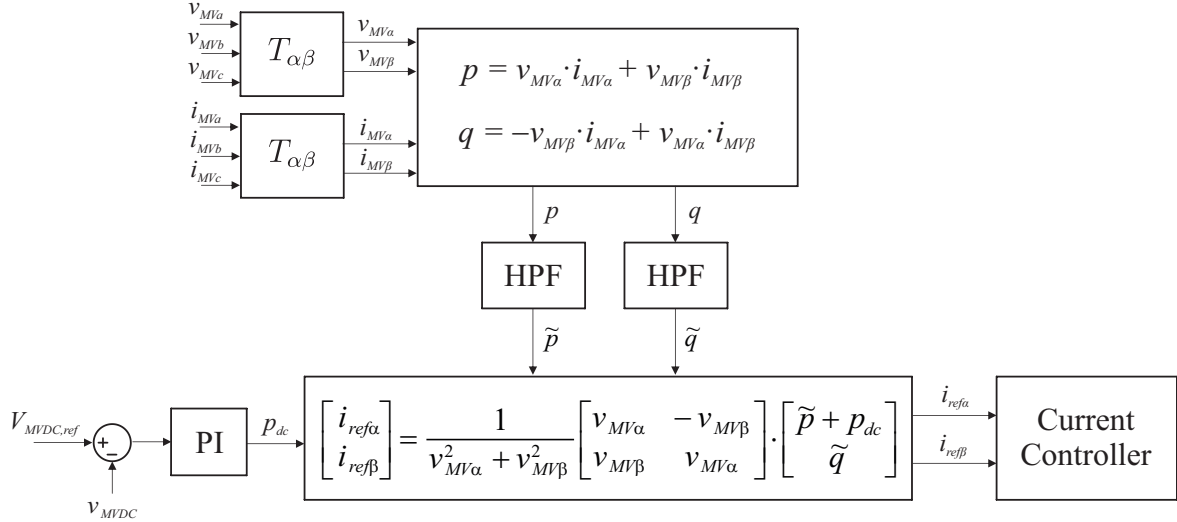


Figure 3.10: Harmonic current reference generation for MV converter based on instantaneous p - q theory.

3.2 DC/DC Converter

The dc/dc converter of ST guarantees the galvanic isolation between the MV grid and the LV one. To achieve the galvanic isolation and meanwhile voltage step-down, a high-frequency transformer is interposed between the two dc stages. The size of the transformer can be significantly reduced by using transformer the voltage at high frequency, which can reach to few tens of kHz. Comparing to the conventional power transformer, this represents a key advantage especially the installation in a city substation, where the space is particularly limited. Two common topologies are usually used for the dc/dc converter of ST, which are dual active bridge (DAB) and series resonant converter (SRC).

The main control objective of the dc/dc converter for ST is to regulate the power flow from MV side to LV dc connection, so that the dc-link voltage of the LV converter can be maintained constant. To achieve this goal, a power flow controller is implemented as shown in Fig. 3.11, where the LV dc-link voltage is controlled following the setpoint $V_{LVDC,ref}$. In the following section, the detailed control strategies for both DAB and SRC will be presented.

3.2.1 Dual Active Bridge

The DAB is a dc/dc converter which can regulate the power flow between the MVDC and the LVDC stages. The DAB circuit is shown in Fig. 3.12a, consisting of two converters: primary and secondary converters, which switch with same frequency, and its working principle is shown in Fig. 3.12b. When the primary converter switches and imposes the high-frequency transformer $v_1 = v_{MVDC}$, and the voltage at the secondary side $v_2 = -v_{LVDC}$, which leads to the increasing of the current i_{dab} , increasing from the negative to a positive value. When the secondary converter switches and imposes the transformer $v_2 = v_{LVDC}$, considering the transformer ratio, the voltage difference is zero thus the current remain constant. As soon as the primary converter switches and imposes the transformer a negative voltage $v_1 = -v_{MVDC}$,

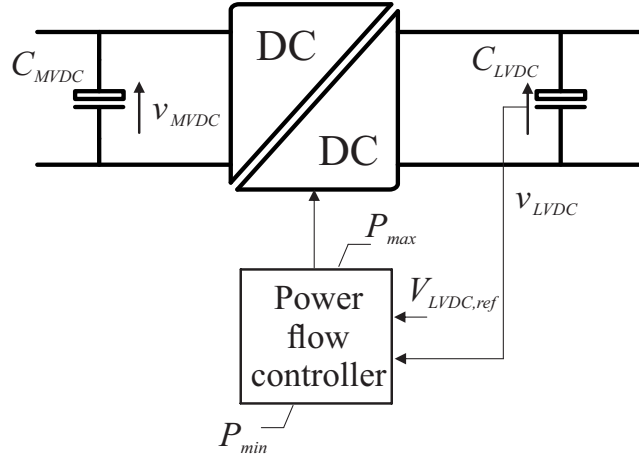


Figure 3.11: Control scheme for the dc/dc converter.

the current i_{dab} starts to decrease, from the positive value to a negative value. Afterwards, when the secondary converter switches and imposes a negative voltage $v_2 = -v_{LVDC}$, the current again keeps constant due to zero voltage difference. It can be noticed that the current is determined by the angle shift φ , meaning the energy transferring between the primary side and the secondary side can be adjusted by regulating φ . The power transfer between the primary bridge and the secondary bridge can be expressed by [31]

$$P_{dab} = \frac{v_{MVDC}v_{LVDC}}{2nf_{dcs}L_r}d_{dab}(1 - d_{dab}) \quad (3.22)$$

where $n < 1$ is the transformer ratio, f_{dcs} is the switching frequency, L_r is the leakage inductance of the transformer, and d_{dab} is the phase shift ratio ($d_{dab} = \varphi/\pi$).

The detailed control block diagram of a DAB is shown in Fig. 3.13, where the power flux between the two dc stages is regulated by a PI controller. The output of the PI controller is the angle shift d_{dab} which determines the transferring power in the high frequency transformer. Here, a first-order transfer function with time constant T_{dab} is used to represent the DAB converter. The reference power P_{dab} is then obtained and limited by the upper limit P_{max} , which is determined by the ST power rating, and the lower limit P_{min} . When the ST allows bi-directional power flow, the value of lower limit P_{min} can be set equal to $-P_{max}$. If the reverse power flow is not desired, P_{min} equals to zero. The DAB current can be calculated from the transfer power P_{dab} divided by the amplitude of LV dc-link voltage V_{LVDC} . The LV dc-link voltage is then obtained by multiplying the DAB current with the dc plant transfer function.

3.2.2 Series Resonant Converter

The SRC is another possible topology with lower complexity (shown in Fig. 3.14a) that can regulate power flow between the two dc stage. A resonant tank (i.e., a LC circuit) is needed in the primary side of the high-frequency transformer, which is able to smooth from the square waveform of the voltage. The bridge in the secondary side is a diode rectifier, which

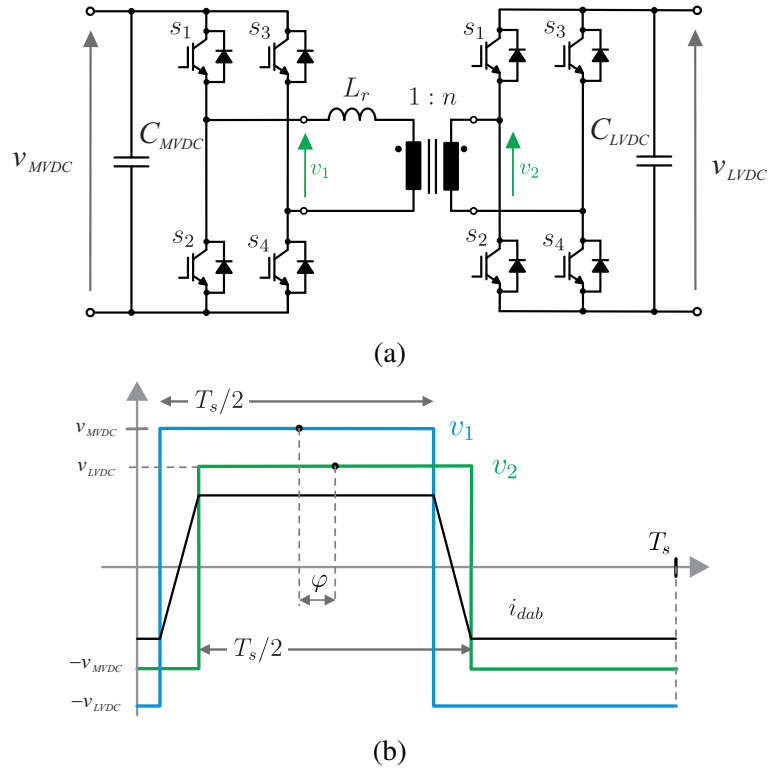


Figure 3.12: DAB: (a) circuit and (b) working principle.

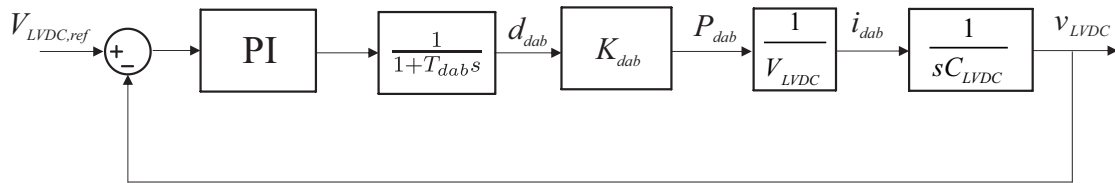


Figure 3.13: Control block diagram of a DAB.

does not allow reverse current flow in such a circuit. The SRC is operated in discontinuous-conduction-mode, and its switching frequency is slightly below the resonant frequency of the resonance tank so that primary side can achieve zero-voltage current and low-current switching, the output diodes achieve zero-current switching [32]. An example of the voltage and current waveforms of the SRC primary side is shown in Fig. 3.14b. When the primary side conducts, the resonance tank is excited and the current i_{src} flows with the resonant frequency. Commonly, the SRC behaves as an idealized "dc transformer", where the ratio between the output voltage and the input voltage is fixed. In this regard, when the MVDC voltage is constant, the LVDC voltage can be obtained based on the voltage ratio.

3.3 LV Converter

Due to the presence of single-phase loads, four-wire TT -systems are usually required, where the 4th wire is needed for connection between one phase and the neutral. With this consideration, the LV converter topologies for ST have to include the 4th wire for the neutral conductor path. One possibility is to use the mid-point of the LVDC connection to form the 4th wire

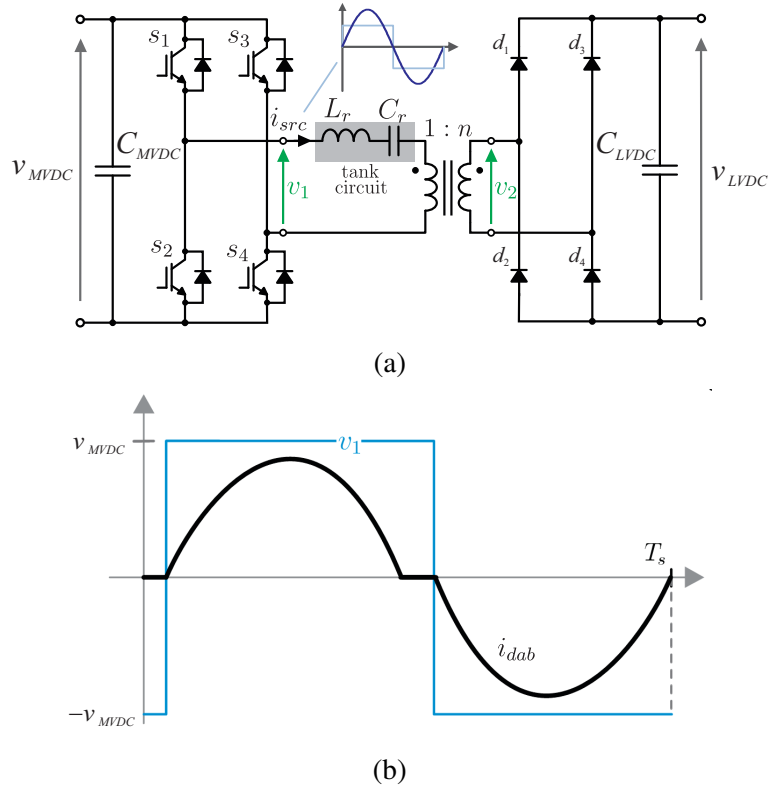


Figure 3.14: SRC: (a) circuit and (b) working principle.

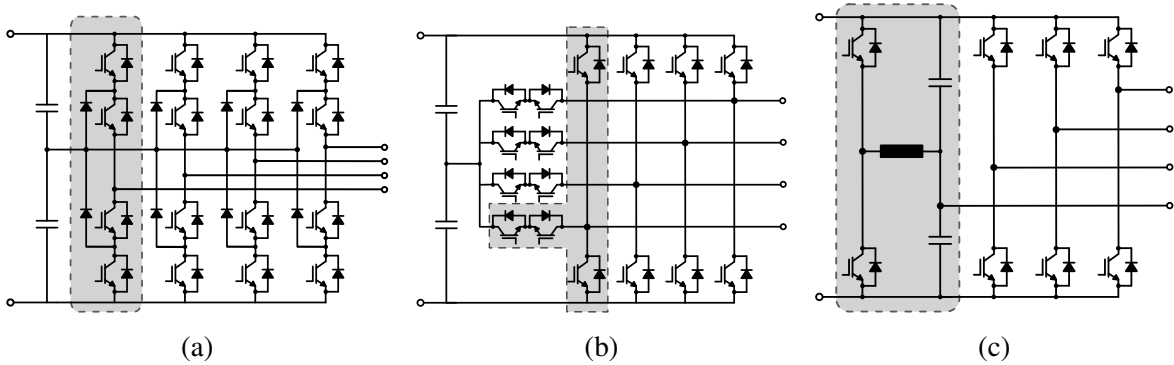


Figure 3.15: Topologies for ST LV converter: (a) NPC, (b) T-type converter, (c) four-leg voltage-source converter.

connection. However, one of the drawbacks of this solution is the uneven energy distribution between the upper and the lower leg of the dc-link capacitor, leading to dc voltage unbalance and neutral point deviation, which further incurs performance degradation of the ST LV converter. Another solution is to introduce dc-link voltage control that aims at reducing dc voltage unbalance and oscillation, and one additional converter leg is in need. Three different candidates for the LV converter are shown in Fig. 3.15, which are four-leg NPC converter, four-leg T-type converter, and four-leg voltage-source converter.

The main control objective of the LV converter is to provide three-phase sinusoidal waveform with constant amplitude and frequency to the LV grid regardless the load dynamics, meanwhile maintaining good power quality. To achieve this target, multiple-loop voltage

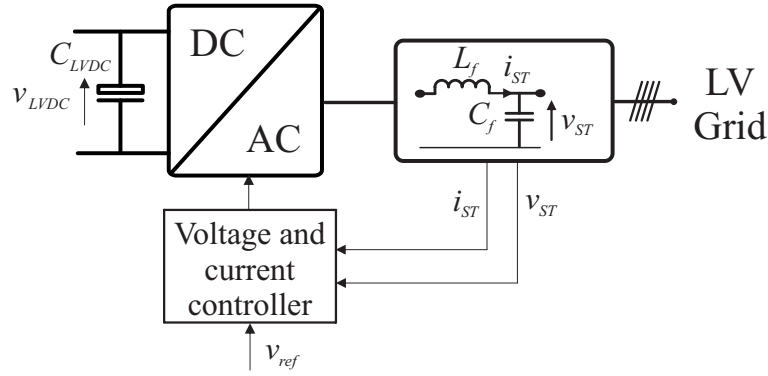
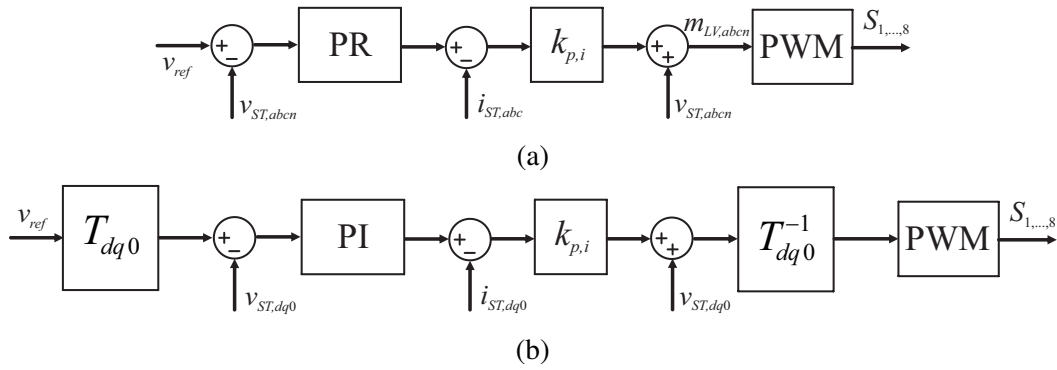


Figure 3.16: Control scheme of LV converter.

Figure 3.17: Control strategies for ST LV converter: (a) in abc -frame and (b) in $dq0$ -frame.

control strategy as shown in Fig. 3.16 can be used since it is easy to implement and presents good steady-state as well as dynamic performance. The voltage reference v_{ref} can be fixed or it can vary depending on the ancillary services requested from the ST LV grid. The detailed control scheme of the LV control is shown in Fig. 3.17, where a voltage outer loop and a current inner loop are used. Two frames: $dq0$ -frame and abc -frame could be implemented in the control system of the LV converter. Depending on the frames, both PI and PR controllers can be used for the outer loop: PI can well regulated the dc signals so that can be used for $dq0$ -frame, while PR is designed for controlling sinusoidal signals and thus can be used for abc frame. For the inner loop, a proportional controller or a PI controller is usually used to minimize the current error. To improve the dynamic performance, a voltage feedforward is added, the feedforward signal can either obtain from the reference voltage or from the measured voltage.

The ST LV converter has to provide voltage waveforms with low harmonic distortion independently from the load current. When only a PR or PI control is used as Fig. 3.17, the system is not able to well reject the current harmonics from the load (which can be regarded as disturbances), causing the voltage waveforms with distortions. As a result, the harmonic control scheme has to be included to alleviate the harmonic issue of LV voltage control. Depending on the different frames, two different harmonic control schemes can be applied as shown in Fig. 3.18. For the abc -frame, a set of parallel resonant controllers can be added to eliminate different-order harmonics in voltage as shown in Fig. 3.18a. For the $dq0$ -frame, nested frames presented in the previous section can be introduced to the voltage control sys-

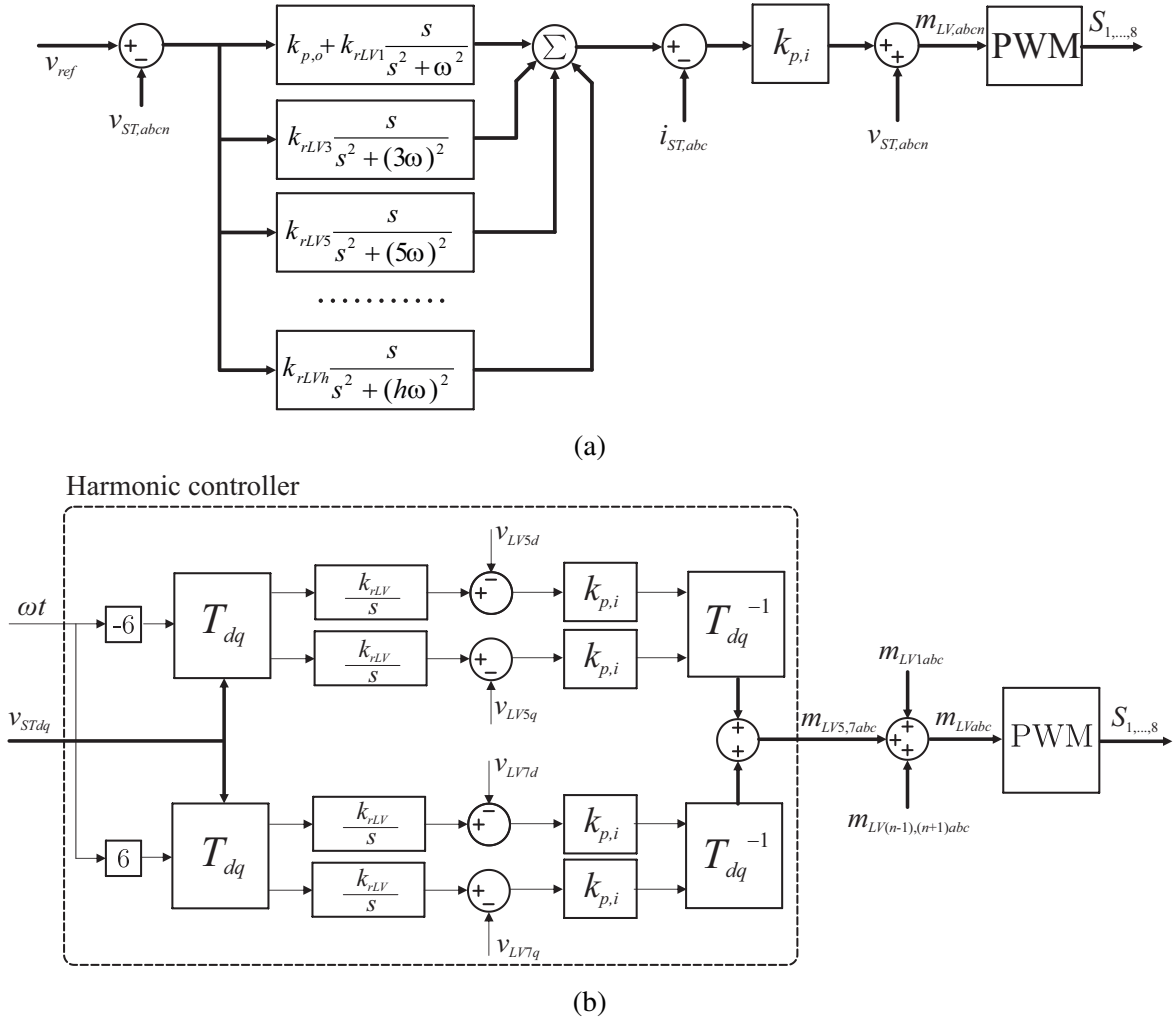


Figure 3.18: Harmonic control strategies for ST LV converter: (a) in *abc*-frame and (b) in *dq0*-frame.

tem, and an example of harmonic controller for 5th-7th harmonic elimination is presented in Fig. 3.18b. Other harmonics can be eliminated by implementing with other nested frames.

In practical implementation, both parallel resonant controllers in *abc*-frame and nested frames in *dq0*-frame have disadvantages. To eliminate multiple frequencies harmonics, a large number of resonant controllers or *dq* transformations are needed, which causes heavy computation burden and tuning complexity for control design. Based on the internal model principle, repetitive control is a way that can achieve zero steady-state error tracking of any periodic signal and is far more ease to implement [33]. The control scheme of the repetitive control in continuous time domain is shown in Fig. 3.19a, where a periodic signal with period of L can be well regulated by using an internal model e^{-Ls} . In practical, where a digital control system is used, the repetitive control scheme in discrete domain shown in Fig. 3.19b can be used. Here, a N -step delay is used to replace e^{-Ls} , and $N = f_s/f$, where f_s and $f = 1/L$ are the sampling frequency and the fundamental frequency, respectively. Repetitive control can offer promising accurate control performance, acceptable computation burden and low control design complexity. More importantly, repetitive control can be seamlessly integrated with different controllers including PI and PR, and can be implemented in various frames

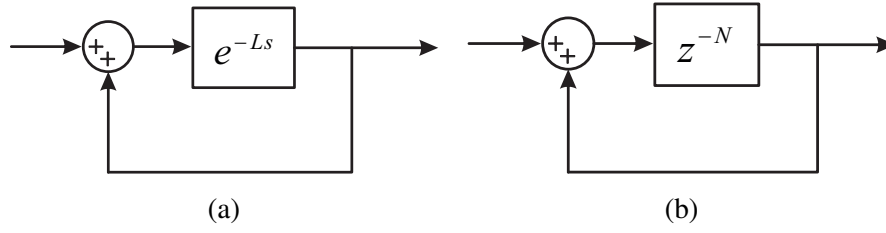


Figure 3.19: Repetitive control in: (a) continuous time domain and (b) discrete domain.

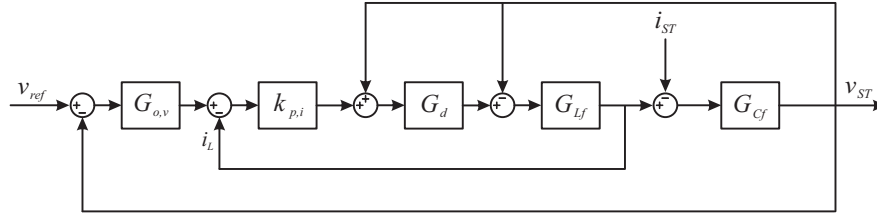


Figure 3.20: Block diagram of LV converter using multiple loop control scheme.

including both abc - and $dq0$ -frames for harmonic elimination.

Based on Fig. 3.19a, the transfer function of the repetitive control can be written by

$$G_{rc}(s) = \frac{e^{-Ls}}{1 - e^{-Ls}} = -\frac{1}{2} + \frac{1}{L} \cdot \frac{1}{s} + \frac{2}{L} \sum_{h=1}^{\infty} \frac{s}{s^2 + (h\omega)^2} \quad (3.23)$$

It can be seen that the repetitive control can be summarized as a set of resonant controllers plus a PI controller.

To design a multiple-loop voltage control with good performance, two design criteria should be fulfilled [34]. The outer voltage loop controller is designed with specified bandwidth and error-tracking requirements based on a given plant including the inner current loop. Then, the inner current controller is tuned with consideration of its influences on the generated new plant (including the designed outer loop) and its disturbance rejection capability. It is worth noting that different voltage feedforward schemes (i.e., measured and reference voltage feedforward) and different current inner loop feedback schemes (i.e., inductor-, capacitor-, and load-current) can be used in the multiple-loop voltage control. Nevertheless, the design procedures of them are very similar so that only one scheme which uses the measured voltage feedforward and the inductor-current inner loop will be discussed here. Chapter 4 will dedicate to make the comprehensive analysis of all the combinations for multiple-loop voltage control.

The control block diagram of the voltage control using the measured voltage feedforward and the inductor-current inner loop is presented in Fig. 3.20, where $G_{o,v}$ is the transfer function of the voltage outer loop controller, which can be either a PR controller (in abc -frame) or a PI controller (in $dq0$ -frame). Based on the block diagram, the transfer function of the inner loop can be obtained, which is

$$G_{in}(s) = \frac{G_d k_{p,i}}{L_f C_f s^2 + G_d k_{p,i} C_f s + 1 - G_d} \quad (3.24)$$

where L_f and C_f are the inductance and capacitance of the LC filter, $k_{p,i}$ is the inner loop gain, and G_d is the equivalent computational and PWM delay. If the voltage feedforward is not used, the transfer function of the inner loop will be

$$G_{in_nff}(s) = \frac{G_d k_{p,i}}{L_f C_f s^2 + G_d k_{p,i} C_f s + 1} \quad (3.25)$$

The Bode diagram of the inner loop is plotted in Fig. 3.21. In Fig. 3.21a, the Bode diagrams of inner loop with and without voltage feedforward are compared. It can be seen that the utilization of voltage feedforward can well damp the resonance caused by the LC -filter. When different inner loop gains are used, the Bode diagrams of inner loop are shown in Fig. 3.21b. It can be observed that the system bandwidth can be widened by increasing $k_{p,i}$. Moreover, seen from (3.24), the damping ratio can be defined as $\zeta = G_d k_{p,i} C_f / (2\sqrt{L_f C_f})$, which indicating that the higher $k_{p,i}$, the better damped system can be achieved.

When outer loop controller is included, the transfer function of the overall system can be written by

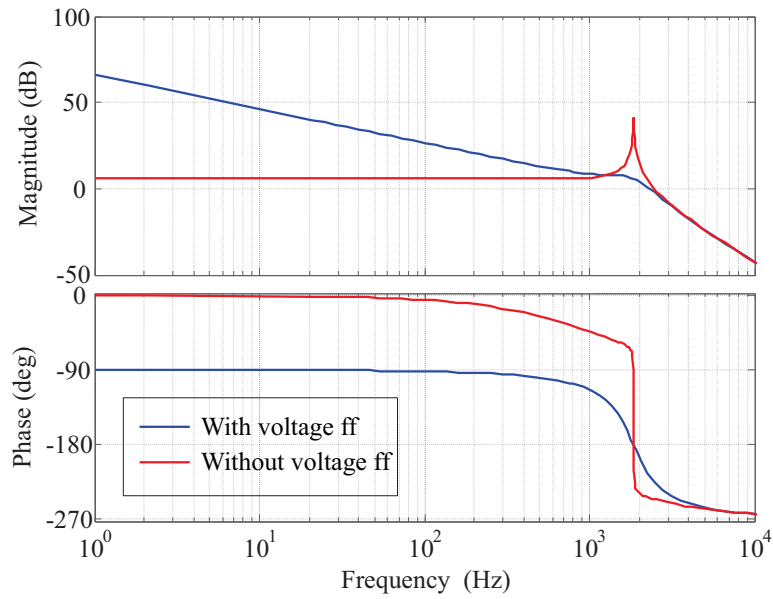
$$G_{op}(s) = G_{o,v} \cdot G_{in} = \frac{G_d k_{p,i} (k_{p,o} s + k_{i,o})}{L_f C_f s^3 + G_d k_{p,i} C_f s^2 + (1 - G_d) s} \quad (3.26)$$

where $k_{p,o}$ and $k_{i,o}$ are the proportional and integral gains of the outer loop PI controller. The gain of the voltage outer loop controller can be designed by considering with the designated bandwidth and steady-state error. However, it is worth noting that the phase margin of the overall system reduces when increasing the outer loop gain. The open-loop Bode diagram of the overall system is shown in Fig. 3.22a. It can be seen that, if the inner loop gain is fixed, the bandwidth and the control gain of the system can be slightly modified by changing the outer loop gain, but the phase margin can be drastically changed. The pole map of the closed-loop system when increasing $k_{p,o}$ is presented in Fig. 3.22b, where the pair of the dominant poles are moving from the left half plane to the right. As a result, a trade-off must be made between control performance and system stability. For instance, in this case, the final bandwidth of 900 Hz and phase margin of 78.5° are designed for the control system.

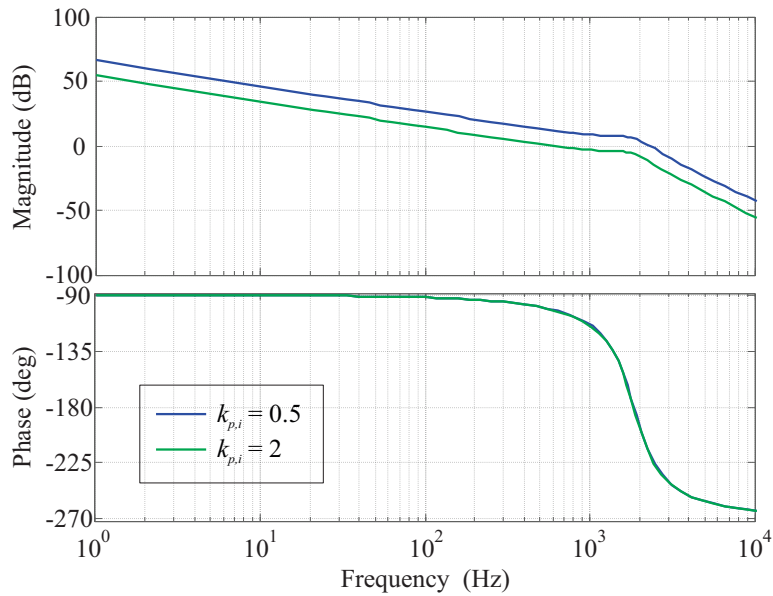
When the repetitive control being plugged in, the open-loop Bode diagram of the overall system is shown in Fig. 3.23. It can be seen that high gains at fundamental frequency and interesting harmonic frequencies have been introduced in the magnitude of the Bode diagram. This feature allows the voltage control system to well control the fundamental voltage and meanwhile eliminate the harmonics up to Nyquist frequency.

3.4 Control Issues and Solutions for LV ST-fed Grid

The control strategies of the three-stage converters ensure normal operation of the ST. However, when coming to a ST-fed distribution grid, addition control issues will be expected. In this section, four control issues and solutions for the LV ST-fed grid are to be discussed, considering the ancillary services and increasing DERs and EV charging stations in LV grid.



(a)



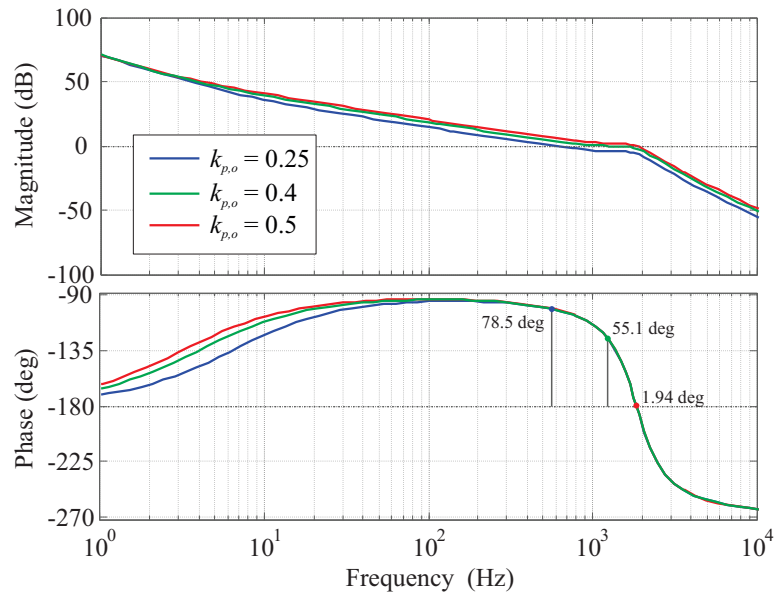
(b)

Figure 3.21: Bode diagram of closed current inner loop: (a) with/without voltage feedforward and (b) with different inner loop gain.

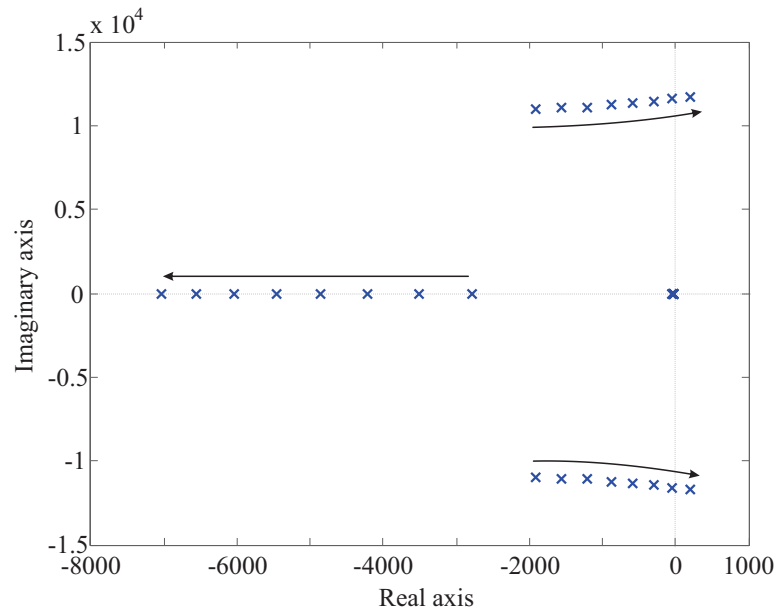
For better understanding, a diagram of control issues and the chapters which try to address the corresponding issues are presented in Fig. 3.24.

3.4.1 Control Interactions and Harmonic Instability

The control interactions among grid converters of different DERs, namely the interactions among different grid-following converters, have drawn wide attention. In particular, researchers are focusing on system modeling, control design, and stability assessment. When ST is utilized in the distribution grid, the interactions between ST converter and grid-converter-based devices (e.g., DERs) are important as well. Different to the previous topics, this one is



(a)



(b)

Figure 3.22: Effects of the outer loop gain: (a) open-loop Bode diagram of the overall system and (b) root locus when varying $k_{p,o}$.

to investigate the interactions between a grid-forming converter and grid-following converters. Fig. 3.24 illustrates the interactions between the ST and local devices: the blue arrow indicates the impacts of ST controller on grid converters, while one of the red arrows is the impacts of current controllers of the grid converters on ST. The mutual interactions could lead to performance degradation and harmonic instability of the LV grid. In addition, the interactions of the controllers with the passive components such as line impedance in the distribution network could further alter the grid features including stability conditions. Until now, this issue has seldom been studied.

To address this issue, stability assessment of a LV ST-fed grid will be carried out in Chap-

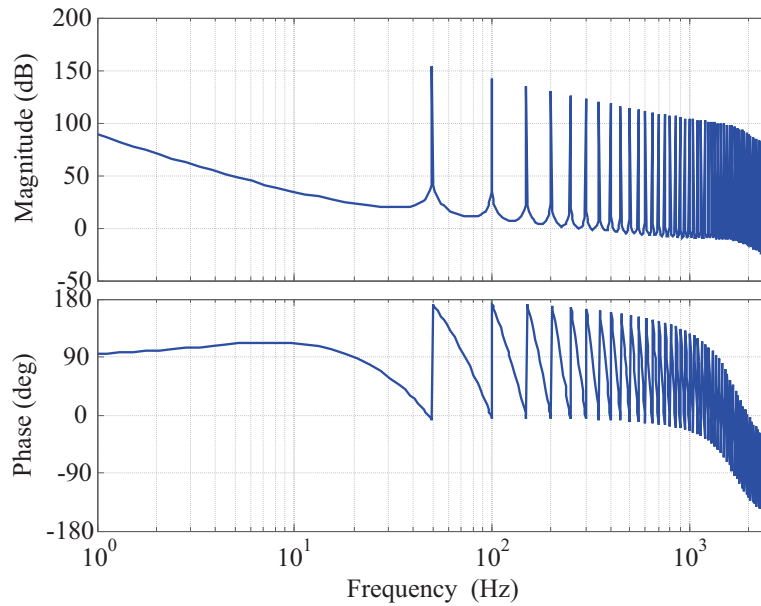


Figure 3.23: Block diagram of LV converter using multiple loop control plus repetitive control.

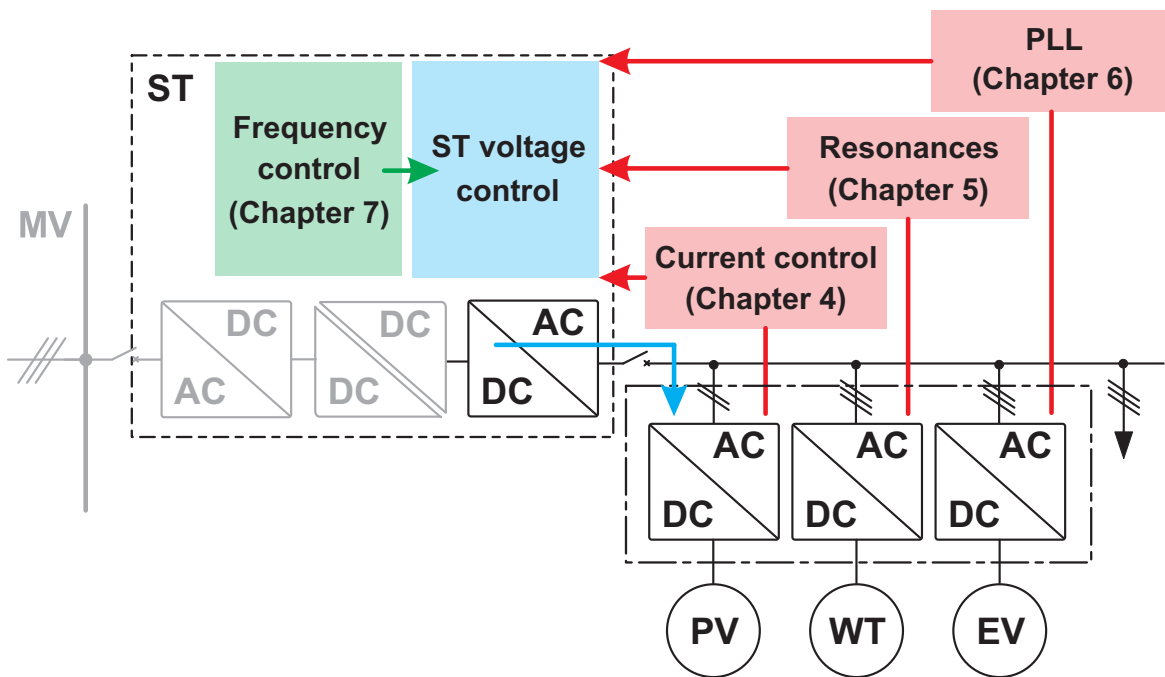


Figure 3.24: Interactions between ST and grid converters in a ST-fed grid.

ter 4, where the impacts of different components like passive loads, grid converters, and line impedance will be considered. The impacts of different multiple-loop voltage control strategies on the system stability will be studied in order to find an optimal solution for the ST LV converter. The optimal solution will guarantee the stable operation of a ST-fed grid under most conditions.

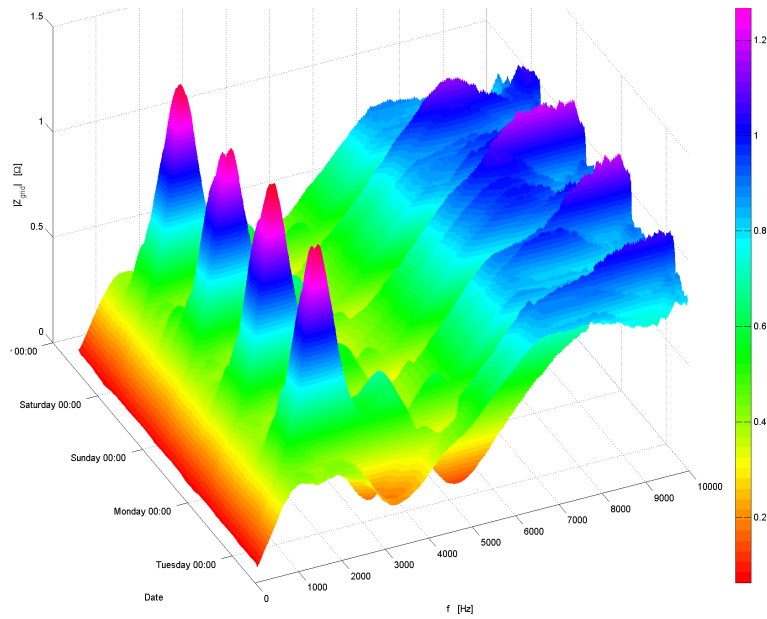


Figure 3.25: Grid impedance magnitude versus time and frequency in an actual low voltage distribution grid [35].

3.4.2 Resonance Damping and Identification Methods

The resonances in the LV grid cause problems in terms of oscillations and power quality violation. The intermittent nature of DERs and EVs further aggravates this issue: the resonant peaks in grid are not fixed but vary with time and number of the interconnection components [35]. An example of the grid impedance profile of an actual low voltage distribution grid in Germany is shown in Fig. 3.25. 49 private household customers and 14 photovoltaic power plants are connected to the measuring point. It clearly shows that multiple resonances appear in this grid and the resonant peaks vary continuously with time. The varying grid resonances will complicate the control design and compromise the system stability.

To solve the problem, online grid impedance estimation method [36, 37] will be proposed for the ST LV converter in Chapter 5. Based on the grid impedance information, adaptive control and filter-based active damping with adaptive feature are proposed and implemented in the ST LV converter, in order to well damping the resonances and provide a better grid environment for the connected grid converters.

3.4.3 Modeling and Stability of Grid Converter Considering PLL

Grid synchronization such as PLL is necessary for the grid converters to delivery power to the grid. Recent literature reveals that PLL could have negative effects on the system stability [38]. One main reason to cause instability is due to the incremental negative resistance in the qq -axis when increasing the PLL bandwidth. As shown in Fig. 3.26, the self impedance Z_{qq} behaves as a negative resistance when considering the effects of PLL and it varies with different PLL bandwidths. It can be seen that a higher PLL bandwidth yields a wider range of negative resistance behavior, which is easier to trigger system instability.

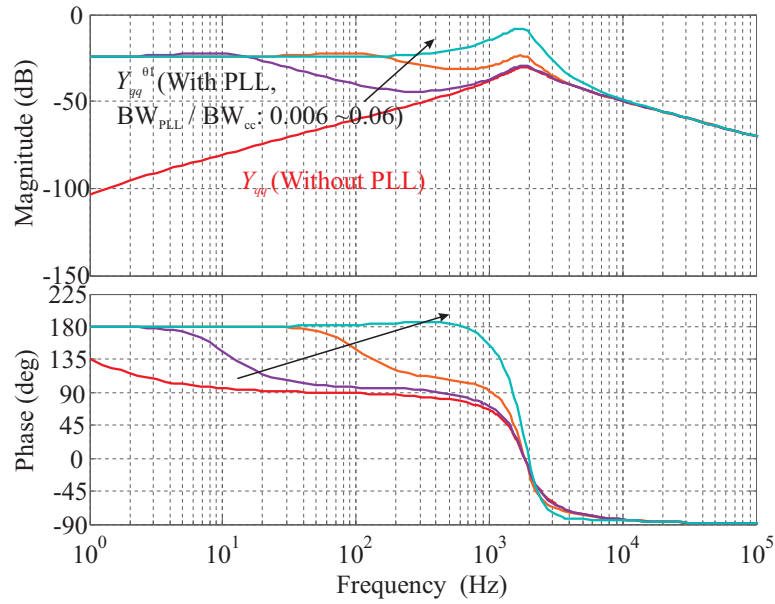


Figure 3.26: Equivalent qq -impedances of a grid converter in dq -frame with different PLL bandwidth.

At present, modeling and stability analysis of PLL-synchronized grid converter in a distributed grid have been well studied. However, no one studies the impacts of PLL on the stability of ST-fed grid until now. To bridge the gap, a model of a simplified ST-fed grid considering the PLL effects will be developed in Chapter 6, and the stability issues will be identified by using appropriate stability criterion. Since the ST can online reshape its output impedance, possible stabilizing method for the PLL issue will be proposed in the chapter.

In addition, another limitation of the existing models in the literature is they are developed for static analysis, namely only small-signal perturbations are considered in the modeling and linearization. These models are not possible to accurately reveal the system behaviors and stability during transient, for example, when the grid voltage has a large phase jump because of fault. To address the issue, a more accurate model with higher approximation order for large phase perturbation will be proposed in Chapter 6. Stability criterion based on the proposed model will be presented to assess the system stability during phase transient.

3.4.4 Harmonic Control Strategies for Grid Frequency Variations

Repetitive control can well eliminate harmonics when the fundamental frequency is fixed. However, in a ST-fed grid, ancillary services can be offered to the LV grid by interacting with local loads and generators by means of voltage amplitude and frequency control. Thus, the grid frequency is time-varying within a certain range, usually following the grid requirements and standards. Under the circumstance, the period N of the repetitive control will be no longer always an integer but often fractional in the case of a fixed sampling rate, which is hard to implement in a digital system. One of the solutions is to use variable sampling frequencies to ensure the integer period of N is always the same in the presence of grid

frequency variations. Nevertheless, a variable sampling rate will significantly increase the real-time implementation complexity of the control systems.

To address this issue, a simple and compact structure frequency adaptive FORC has been proposed, derived from the internal model principle and able to provide high control performance with arbitrary frequency. The detailed voltage control strategy with FORC for the ST LV converter will be presented in Chapter 7. In this way, the ST LV converter can provide sinusoidal voltage waveforms to the LV grid during the frequency variations. The design criterion of the voltage control with the FORC is presented in the chapter. Two scenarios: ST overloading and reverse power flow, have been studied, validating the effectiveness of the proposed control strategy in the two scenarios.

3.5 Summary of the Chapter

This chapter illustrates the control schemes for all the three stages of a ST, especially the control for the ST LV converter which is one the main focuses of this thesis. 4 main control issues of the ST LV converter have been discussed:

- control interactions and harmonic instability
- resonance damping and identification methods
- modeling and stability of grid converter considering PLL
- harmonic control strategies for grid frequency variations

These control issues challenge the performance and stable operation of a LV ST-fed grid, and degrade the quality of ancillary services. At it will be seen in the following chapters, the 4 chapters are aiming to address the 4 control issues, meanwhile maintaining the key features of the basic control of ST LV converter.

4 Stability Assessment of Voltage Control Strategies in Low Voltage Smart Transformer-fed Grid

Apart from the ancillary services, the ST LV converter behaves as a grid-forming converter which generates sinusoidal and balanced three-phase voltages at substation during operation of the LV side ST-fed grid. The voltage control of the ST LV converter interacts with the appliances as well as their control systems in the LV grid, especially the control of local grid converters as shown in Fig. 4.1. With the target to obtain stable operation for the ST-fed grid, this chapter assesses the stability under various operating conditions, when different voltage control strategies are employed in the ST LV converter. Based on the stability conditions, dynamics, and power quality, this chapter aims at finding an optimal voltage control strategy for the ST LV converter and providing design guidelines as well as considerations for such grid with stability concern.

4.1 Differences Between ST and Uninterrupted Power Supply

The primary purpose of ST voltage control is similar to that of the conventional voltage-controlled applications, such as uninterrupted power supply (UPS) [39], which has been adopted for critical loads against unintentional grid disturbance or faults. In general, UPS has been employed in specific fields, for instance, data centers, hospitals, and small-size industry parks, while the most recent trend is the increasing utilization of the UPS in the microgrids [40]. Many research efforts have been put on the voltage control strategies of UPS and numerous voltage control strategies have been proposed for this application, such as hysteresis control [41], deadbeat control [42], sliding mode control [43], and multiple feedback loop (multiloop) control [44]. However, high switching stress or inaccurate elimination of harmonics may occur due to random switching frequency for hysteresis control, sensitivity to inaccurate parameters for deadbeat control, and failure in dealing with equilibrium jitter for sliding mode control. Due to the ease of implementation and excellent steady-state/dynamic performance, the multiloop voltage control becomes one of the most popular strategies in the UPS application [44, 45, 46]. Moreover, the structure of the multiloop control allows the advanced control functionalities like load control [47], frequency adaptive control [48], and so on, to be easily integrated for providing services to distribution grid. Among the existing multiloop control strategies, the effects of the inner loop feedback have been well studied and it is reported that the load- and inductor-current feedback control presents the best performance in terms of dynamic performance, fundamental steady-state error and harmonic elimination [46].

Nevertheless, the conclusions drawn in the literature are mainly based on the linear loads (e.g., RLC loads) and nonlinear loads (e.g., bridge rectifier). Unlike UPS, usually considering passive loads, one major change of the ST-fed LV grid paradigm is the increasing installation of grid-converter-based devices (like DERs and EV charging stations as shown

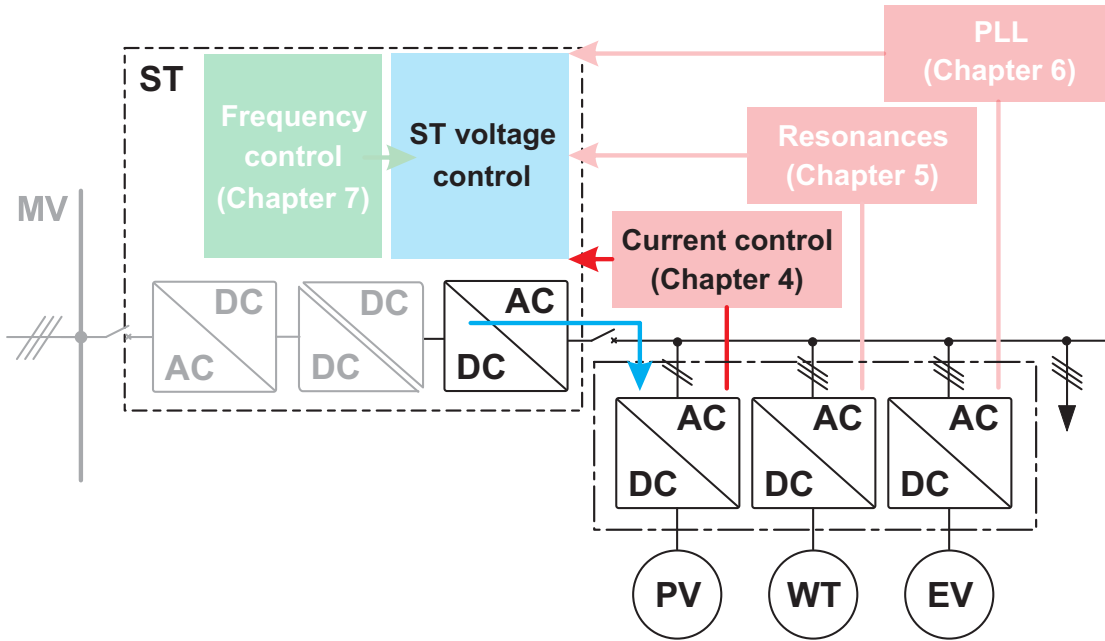


Figure 4.1: Research focus of Chapter 4: control interactions between ST LV converter and local grid converters.

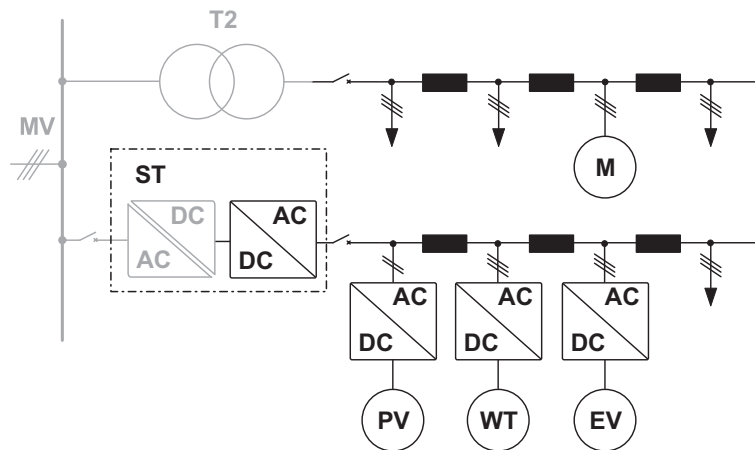


Figure 4.2: Configuration example of a ST-fed grid.

in Fig. 4.2) and the expanded dimension of the supplied grid. Therefore, the ST LV converter is connected to a LV grid with more sophisticated impedance profile. An example of the impedance profile measured from a German LV grid is presented in Fig. 4.3. It can be seen that the equivalent impedance can be no longer represented by simple combination of RLC loads. Moreover, the dimension of the supplied grid is much wider than the systems which are supplied by the UPS. The expansion of the grid dimension could further aggravate the issues and also pose the question that whether the conclusions as well as experiences from the UPS application would be valid in the ST-fed grid.

By employing control system and output filters, grid converters introduce control dynamics and filter resonances into the grid, imposing new challenges including resonance issues, harmonic oscillations, and harmonic stability [1, 5, 49]. Meanwhile, the effects of the line impedance in the distribution network could alter the grid characteristics including stability

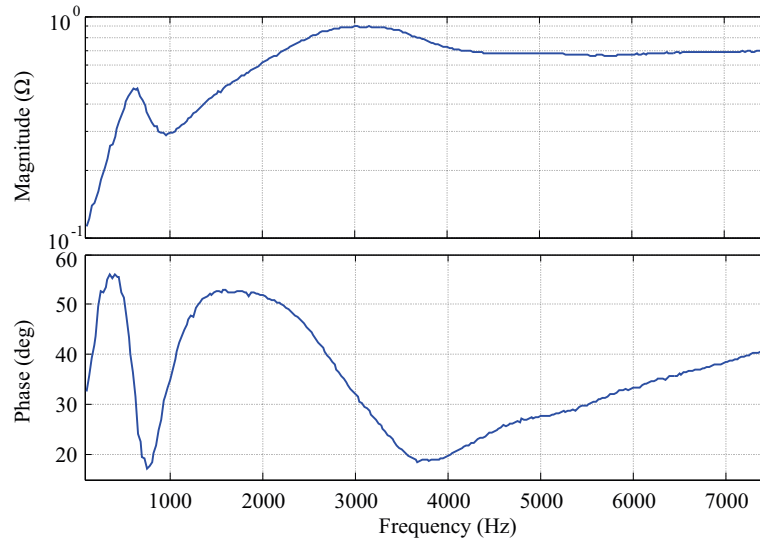


Figure 4.3: Profile of system impedance from a German LV grid.

conditions of the grid. With these considerations, the interactions between the ST LV converter and the LV grid should be taken into account in the process of evaluation of voltage control strategies, in order to obtain an optimum control strategy for ST. The test of the optimal control in a distribution grid or microgrid is necessary to validate the effectiveness of the voltage control in a real-size system. Therefore, a CIGRÉ benchmark grid is chosen as the testbed for the validation.

In general, this chapter will give a comprehensive study of different multiloop voltage control for ST LV converter with stability concerns. To study the effects of LV grid on the system stability, a complete analysis considering the passive loads, grid converters (with different control strategies/sensor positions, under different operation conditions), and line impedance are given. An equivalent admittance matrices is used to describe the characteristics of LV network. The equivalent admittance matrices are then included in the control and stability analysis so that the effects of the loads and power electronics interfaces can be well considered. One feature of the grid-converter-based devices is that they could be deactivated under some circumstances, for instance, converter faults, grid converters for PV panels during night, and so on. This condition of grid converter has seldom be considered in other voltage-controlled applications, but is importance and critical for the stable operation of ST-fed grid.

4.2 Multiloop Voltage Control Strategy of ST LV Converter

The configuration of a ST-fed grid is shown in Fig. 4.2, where a three-stage solid-state transformer is utilized and various types of grid-converter-based devices as well as loads are connected to the ST LV side. The ST has the capability to offer a decoupling control of MV and LV grid and therefore it is assumed that the LV grid is independent from the effects of the MV one in the following. This section will firstly review the existing multiloop voltage control strategies for the conventional application: UPS, and the appropriate candidates will

be selected for the control of the ST LV converter. The methodology for control analysis and stability assessment of the ST-fed grid will then be briefly introduced.

4.2.1 Classification of Voltage Control Strategy of ST LV Converter

Detailed system configuration of the ST LV converter is shown Fig. 4.4, where L_f and C_f are the inductor and capacitor of the LC -type filter; L_n is the inductor of the neutral line; Z_l represents the equivalent line impedance between the ST and the point of common coupling (PCC). A three-phase four-leg converter is selected as the ST LV converter since this topology can well suppress the common-mode voltage and dc voltage oscillation, thus can significantly improve the lifetime of the dc capacitors [50]. To achieve sinusoidal and balanced three-phase voltage at PCC, the voltage control can be realized with the multiloop voltage control strategy (consisting of a voltage-controlled outer loop and a current-controlled inner loop) in the $dq0$ -frame. PI controllers are used for both the voltage outer loop and the current inner loop.

Among the most common multiloop voltage control strategies in the literature, two different voltage feedforward schemes: reference voltage feedforward (RFF) and measured voltage feedforward (MFF), are usually considered for the voltage-controlled outer loop; and three possibilities: capacitor-current (CC) feedback, inductor-current (IC) feedback, and load- and inductor-current (LC) feedback, are employed for the current-controlled inner loop. In [46], it is shown that the capacitor-current feedback and the load- and inductor-current feedback are equivalent in terms of transfer function, and they offer the best performance in terms of dynamic performance, fundamental steady-state error and harmonic elimination for the UPS application. Nevertheless, for the ST LV converter, this conclusion would be questioned when considering the new features like protection requirements, wide installation of grid converters on the LV side, and increasing grid dimension. For instance, from the protection perspective, one of the weaknesses of the capacitor-current feedback is that it cannot incorporate overcurrent protection. In this regard, the capacitor-current feedback is not suitable for the ST-fed grid, only the inductor-current feedback and the load- and inductor-current feedback will be taken into account as the candidates in the followings. On the other hand, the voltage feedforward schemes also play an important role on the voltage control performance in terms of dynamics and stability. As seen in the control design of the previous chapter, the measured voltage feedforward can well damp the resonance so that it presents better stability condition than the one without voltage feedforward. Nevertheless, the choice of the voltage feedforward schemes has been seldom concerned in the literature. A comprehensive study of different multiloop strategies is thereby needed to facilitate the control design of the ST LV converter.

4.2.2 Interaction Between ST LV Converter and LV Grid

In conventional distribution grid, the output impedance of the transformer is one of the most important indices that determines power efficiency, short-circuit ratio (SCR), and voltage

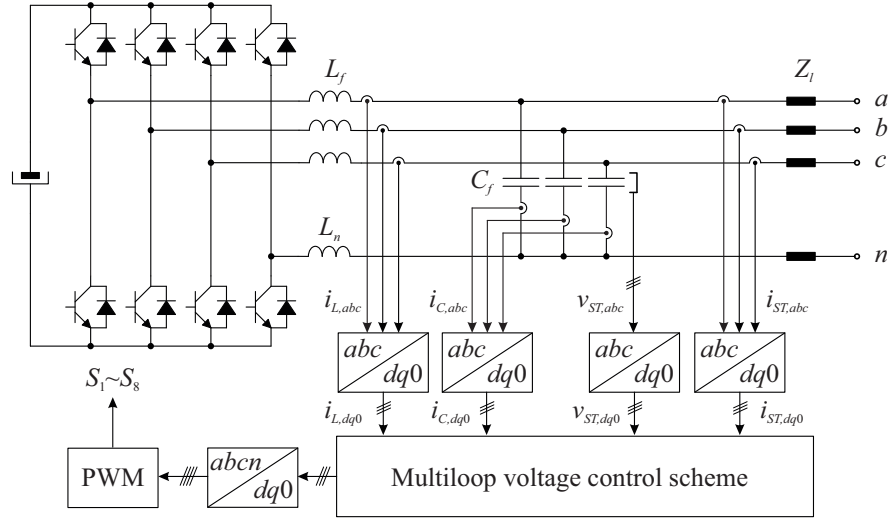


Figure 4.4: System configuration and control structure of ST LV side converter.

regulation capability [51]. Likewise, the equivalent impedance of the ST LV converter determines these indices of a ST-fed grid as well. Moreover, the stability and loading effects of the LV grid can be determined by the equivalent impedance. For better understanding, a LV ST-fed grid can be represented by two subsystems connected in series as shown in Fig. 4.5, where Z_o is the output impedance of the ST LV converter and Z_{in} represents the input impedance of the overall LV grid. According to the theory given in the literature [52], the stability of the overall ST-fed grid can be determined by the impedance ratio at the PCC, namely determined by $T_m = Z_o/Z_{in}$. If $|Z_{in}| \gg |Z_o|$ for all frequencies, the effects from the LV grid is negligible and the stability of the ST-fed grid will depend mainly upon the stability of the ST LV converter itself. For the conventional voltage-controlled applications (e.g., UPS), where passive loads are dominant, the systems are easier to meet the impedance ratio requirement during nominal operation. Depending on the known load rating, the voltage control as well as the filter design of those applications can be well planned and therefore less likely to suffer from the stability issues due to interactions.

However, in an actual distribution grid, $|Z_{in}|$ relies on the passive loads and grid converters with "plug-and-play" feature and both the load profiles and the connected grid converters change frequently. Therefore, it is often impossible for the grid to fulfill $|Z_{in}| \gg |Z_o|$ under all scenarios. When $|Z_{in}| < |Z_o|$, the interactions between the ST LV converter and the LV grid can not be ignored any more, which could incur stability problems and performance degradation. In this case, stability criterion should be applied to identify the stability issues and meanwhile provide guidelines for the control design of the ST LV converter.

To well assess the stability conditions, several methodologies based on the small-signal analysis can be utilized. Among them, eigenvalue-based analysis and impedance-based stability analysis are the two most common methods [53]. In particular, the impedance-based stability analysis is an attractive way to analyze stability issues of power system with the integration grid converters. This approach is originally derived from the design of input filter of dc/dc converters [54]. Instead of systematically analyzing the eigenvalues of the state matrix, the

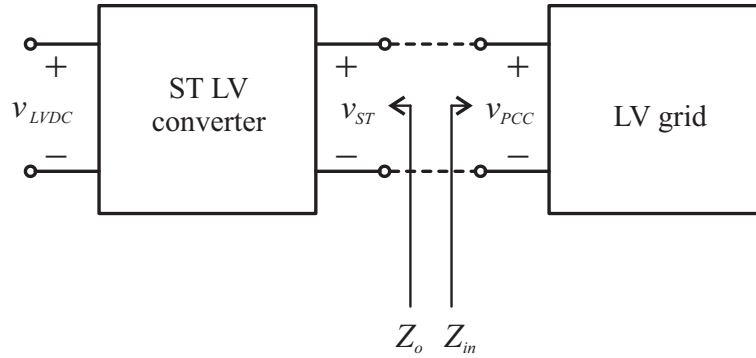


Figure 4.5: Equivalent cascaded subsystem for a ST-fed grid.

impedance-based stability analysis predicts the system stability at each PCC of the component or the equivalent system impedance. Thus, it avoids the formulation of the state matrix of the entire system and the contribution of each component to the system stability can be easily assessed in the frequency domain. In this thesis, analysis of open-loop one-line block diagram with the equivalent admittance of LV grid is carried out. This approach is also derived from the impedance-based theory, sharing identical characteristics from the transfer function point of view. Compared to the conventional impedance-based stability analysis, this method uses the open-loop transfer function instead of the equivalent impedance of the ST LV converter, in order to better reveal and target the stability issues in the frequency domain.

In the impedance-based analysis, the Nyquist stability criterion is one of the most common methodologies to analyze the stability based on the impedance ratio [55]. It has been widely used to study the harmonic stability issues between source and load in the dc system or the ac system in the stationary frame. Nevertheless, when coupled terms and asymmetric features emerge in the synchronous frame, the generalized Nyquist criterion that based on the relationship between the output and the input impedance matrices [56], should be taken into account for stability assessment.

4.3 Stability Assessment of a LV ST-fed Grid Using Different Control Strategies

This section describes the stability analysis when passive loads and grid converters being connected to the LV grid. A one-line block diagram of the ST LV converter is illustrated in Fig. 4.6. All the candidates of the multiloop voltage control strategies mentioned in the previous section including reference voltage feedforward (blue dashed line), measured voltage feedforward (green dashed line), inductor-current feedback (black solid line), and load- and inductor-current feedback (red dashed line + black solid line), have been demonstrated in the one-line block diagram. For clarity, all the bold letters in the blocks represent corresponding transfer function matrices instead of transfer functions. The open-loop transfer function matrix can be easily obtained based on the block diagram, for instance, when the measured

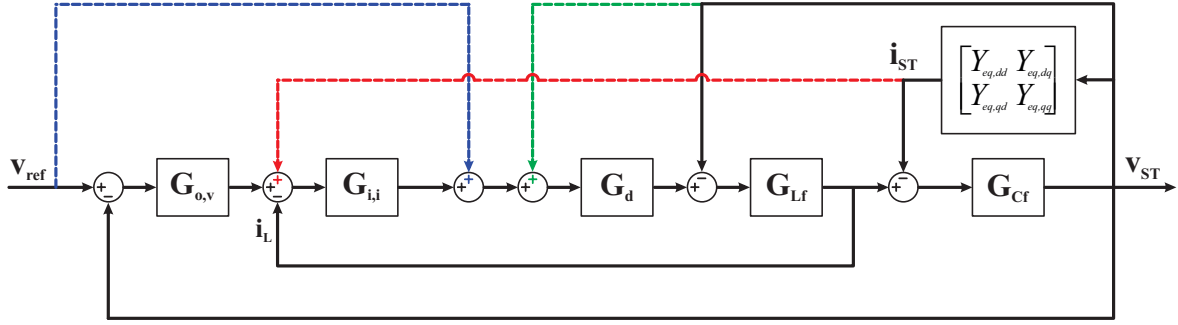


Figure 4.6: Generalized block diagram of multiloop voltage control for ST LV converter.

voltage feedforward and the inductor-current is chosen, the expression is

$$\mathbf{G}_{op} = \mathbf{G}_d \mathbf{G}_{o,v} \mathbf{G}_{i,i} \mathbf{G}_{Lf} \cdot [\mathbf{G}_{Lf}(\mathbf{I} - \mathbf{G}_d) + \mathbf{Y}_{eq} + \mathbf{G}_{Cf}^{-1} + \mathbf{G}_{Lf} \mathbf{G}_d \mathbf{G}_{i,i} (\mathbf{Y}_{eq} + \mathbf{G}_{Cf}^{-1})]^{-1} \quad (4.1)$$

where \mathbf{G}_{Lf} and \mathbf{G}_{Cf} are the transfer function matrices of the LC -type filter, $\mathbf{G}_{o,v}$ and $\mathbf{G}_{i,i}$ indicate the transfer function matrices of the voltage outer loop and the current inner loop controllers (PI controllers) in the synchronous frame, \mathbf{G}_d represents the transfer function matrix of the computation and PWM delay.

When the measured voltage feedforward and the load- and inductor-current feedback is chosen, the open-loop transfer function matrix is given by

$$\mathbf{G}_{op} = \mathbf{G}_d \mathbf{G}_{o,v} \mathbf{G}_{i,i} \mathbf{G}_{Lf} \cdot [\mathbf{G}_{Lf}(\mathbf{I} - \mathbf{G}_d) + \mathbf{Y}_{eq} + \mathbf{G}_{Cf}^{-1} + \mathbf{G}_{Lf} \mathbf{G}_d \mathbf{G}_{i,i} \mathbf{G}_{Cf}^{-1}]^{-1} \quad (4.2)$$

When the reference voltage feedforward and the inductor-current feedback is chosen, the open-loop transfer function matrix is given by

$$\mathbf{G}_{op} = \mathbf{G}_d \mathbf{G}_{Lf} (\mathbf{G}_{o,v} \mathbf{G}_{i,i} + \mathbf{I}) \cdot [\mathbf{G}_{Lf} + \mathbf{Y}_{eq} + \mathbf{G}_{Cf}^{-1} + \mathbf{G}_{Lf} \mathbf{G}_d \mathbf{G}_{i,i} (\mathbf{G}_{Cf}^{-1} + \mathbf{Y}_{eq})]^{-1} \quad (4.3)$$

When the reference voltage feedforward and the load- and inductor-current feedback is chosen, the open-loop transfer function matrix is given by

$$\mathbf{G}_{op} = \mathbf{G}_d \mathbf{G}_{Lf} (\mathbf{G}_{o,v} \mathbf{G}_{i,i} + \mathbf{I}) \cdot [\mathbf{G}_{Lf} + \mathbf{Y}_{eq} + \mathbf{G}_{Cf}^{-1} + \mathbf{G}_{Lf} \mathbf{G}_d \mathbf{G}_{i,i} \mathbf{G}_{Cf}^{-1}]^{-1} \quad (4.4)$$

The equivalent admittance of the LV grid in dq frame can be written by

$$\mathbf{Y}_{eq} = \begin{bmatrix} Y_{eq,dd} & Y_{eq,dq} \\ Y_{eq,qd} & Y_{eq,qq} \end{bmatrix} \quad (4.5)$$

and can be included in the one-line block diagram so that the effects of the LV grid on the ST LV converter can be studied by the impedance-based theory and the (generalized) Nyquist criterion.

Based on the block diagram, the impedance matrix of the ST LV converter can be obtained by the relationship between \mathbf{i}_{st} and \mathbf{v}_{st} . Comparing to the diagonal elements, the magnitude

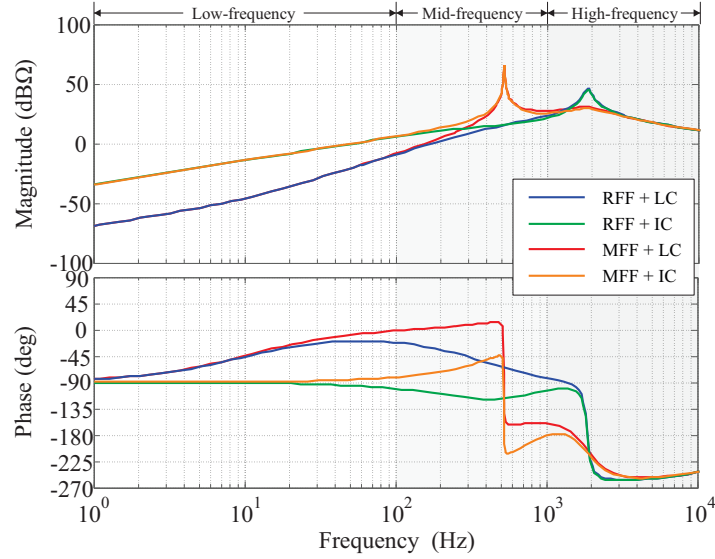


Figure 4.7: Equivalent impedance of ST LV converter using different multiloop voltage control strategies.

of the nondiagonal elements of the ST LV impedance are negligible. The impedance characteristics of the diagonal elements, using the two different voltage feedforward schemes (reference voltage feedforward and measured voltage feedforward) and the two different current feedback schemes (inductor-current and load- and inductor-current) are shown in Fig. 4.7. When different voltage control strategies are utilized, it is shown that all impedances at the dc reach pretty low level due to the utilization of the PI controllers, which means all the voltage strategies can well regulate the voltage at the fundamental frequency in the abc frame with low fundamental steady-state error. In the low-frequency range, the effects of the inner loop are dominant, it can be seen that the impedance using the load- and inductor-current is much lower than the one using the inductor-current, indicating the load- and inductor-current can better reject/eliminate the noises and low-order harmonics due to the lower impedance at these frequencies. Besides, in the mid-frequency range, the influences of the feedforward play the main role, while the effects of the current inner loop schemes are minor as in the figure both the magnitudes and the phases are overlapping when the feedforward scheme is fixed. It can be seen that the impedance using the reference voltage feedforward is lower than that of measured voltage feedforward, showing the reference voltage feedforward presents better control performance in this frequency range. In the high-frequency range, different control strategies present similar impedance behavior.

4.3.1 LV Grid Dominated by Passive Loads

When the LV grid is dominated by passive loads, the magnitudes of the diagonal elements of \mathbf{Y}_{eq} is much larger than those of the nondiagonal elements, and therefore the nondiagonal elements can be omitted during analysis. The block diagram in d - and q -axis can be studied separately thanks to the negligible coupling effects, and the Nyquist criterion can be applied to the assessment. From the point of view of equivalent impedance, a higher ST LV

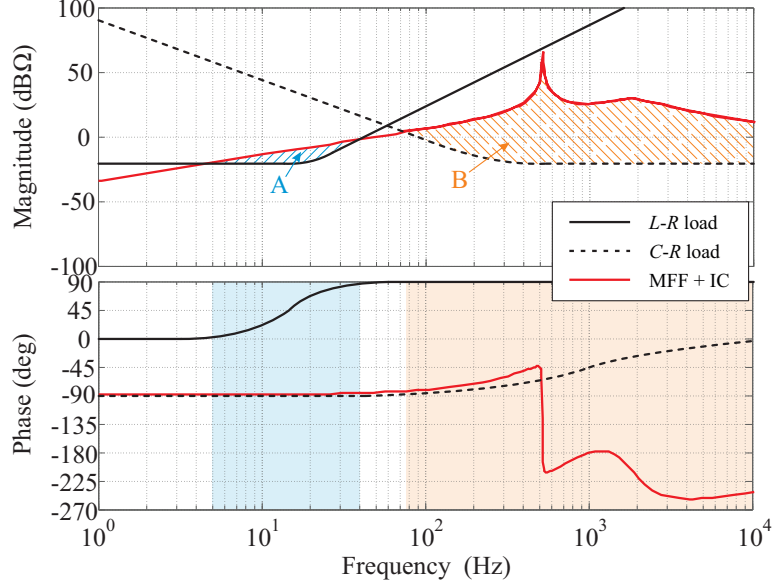


Figure 4.8: Critical region of \mathbf{G}_{op} using different multiloop voltage control strategies under various load conditions.

Table 4.1: Dominant Pole Information of Different Strategies With Various Passive Loads

	Inductive loads				Capacitive loads			
	RFF+IC	RFF+LC	MFF+IC	MFF+LC	RFF+IC	RFF+LC	MFF+IC	MFF+LC
σ	-921	-925	-3800	-3810	-4020	-4080	-4400	-4450
ζ_d	0.0765	0.0768	0.311	0.312	0.123	0.123	0.135	0.135

converter impedance markedly rises the chance that $|Z_o|$ could exceed $|Z_{in}|$ for some frequencies, especially at the resonant frequency, which could lead to stability issues. The equivalent impedance of the LV grid is commonly inductive, with low magnitude in the low-frequency range and high magnitude in the mid- and the high-frequency range, showing by the black solid line of Fig. 4.8. It can be seen that $|Z_{in}| > |Z_o|$ can be easily maintained in the mid- and the high-frequency range if the inductive LV grid has been well planned. However, take the impedance using the measured voltage feedforward and the inductor-current as an example, $|Z_{in}| < |Z_o|$ could happen in the low-frequency range (as Region A shown in Fig. 4.8). Since $\angle Z_{in}$ of the L - R load varies from 0° to 90° , the phase of the overall system ($\angle Z_o - \angle Z_{in}$) at the corner frequency of the L - R could close to or even cross -180° , leading to unstable conditions [52]. On the other hand, when capacitive passive loads are dominant, for instance, capacitor bank is connected, the magnitude in the low-frequency range is high and the ones in the mid- and the high-frequency range would be lower as shown by the black dashed line of Fig. 4.8. It is seen that $|Z_{in}| > |Z_o|$ can be easily maintained in the low-frequency range, while could no longer be fulfilled in the mid- and the high-frequency range (as Region B shown in Fig. 4.8). Nevertheless, since $\angle Z_{in}$ of the C - R load varies from -90° to 0° , the phase of the overall system could be easily maintained above -180° , which indicates the stability issue is not critical during capacitive load conditions.

The stability conditions of all the multiloop control strategies under different passive load

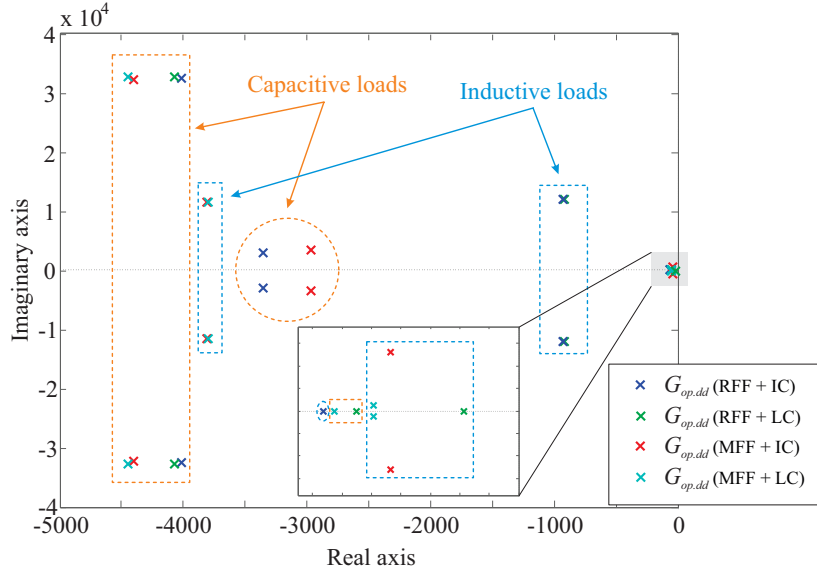


Figure 4.9: Pole maps of \mathbf{G}_{op} using different multiloop voltage control strategies under various load conditions.

Table 4.2: System Parameters

Symbol	Quantity	Value
L_f	filter inductance of ST	5.03 mH
C_f	filter capacitance of ST	1.5 μ F
L_{f1}	DER converter-side filter inductance	5.03 mH
C_{ff}	DER filter capacitance	1.5 μ F
L_{f2}	DER grid-side filter inductance	0.5 mH
R_d	damping resistor of grid converter	2 Ω
$k_{p,o}$	proportional gain of ST outer loop (nominal)	0.167
$k_{i,o}$	integral gain of ST outer loop (nominal)	333.3
$k_{p,i}$	proportional gain of ST inner loop	5.33
$k_{i,i}$	integral gain of ST inner loop	33.3
k_{pc}	proportional gain of current control of grid converter	15
k_{ic}	integral gain of current control of grid converter	50

conditions can be further studied by the Nyquist criterion, giving better understanding. In the case studies, system parameters illustrated in Table 4.2 are used. According to the Nyquist stability criterion, the system stability relies on the Nyquist plot and the right half plane poles of the open-loop system. In detail, if the system is stable, the number of counter-clockwise encirclements of $(-1, j0)$ in the Nyquist plot must be equal to the number of open-loop poles in the right half plane [57]. All the Nyquist plots of $G_{op,dd}$ do not encircle $(-1, j0)$ and the pole maps of $G_{op,dd}$ of all case studies are presented in Fig. 4.9. It can be seen that the dominant poles when capacitive loads are connected (encircled by orange dashed line) are further away from the imaginary axis than the dominant poles when inductive loads are connected (encircled by blue dashed line). During capacitive loads connection, the measured voltage

feedforward can present a more stable operation than the reference voltage feedforward, observing from the locations of the dominant poles. The load- and inductor-current inner loop also can offer more stable operation than the inductor-current in this case. During inductive loads connection, the measured voltage feedforward is still better than the reference voltage feedforward in terms of stability, however the inner loop effects are nearly identical since the dominant poles with different inner loops are overlapping each other. For better comparisons, the information of the dominant poles including the real parts σ and the damping ratio ζ_d of different multiloop control strategies with various loads are given in Table 4.1.

4.3.2 LV Grid Dominated by Grid Converters

Looking at the equivalent Norton models, the equivalent admittances of both grid-converter-based active loads and grid-converter-based distributed generations would be identical, if same control and system parameters are used. In this regard, a general system configuration for the grid converters are shown in Fig. 4.10, where *LCL*-type filter is utilized for better harmonic rejection. A power control loop including active/reactive power control and dc voltage control is employed to regulate active/reactive power injection as well as the dc-link voltage, a current inner loop implemented in the synchronous frame is used to track the current references generated by the power outer loop. Depending on the relationship between *LCL* resonant frequency and sampling frequency, two different current sensor positions as well as current control strategies can be utilized for such grid converters [58]. When the resonant frequency f_{res} is smaller than $f_s/6$ (f_s is sampling frequency), the converter-current feedback (CCF, shown by the magenta dashed lines) is recommended to maintain stability. In case of $f_{res} \in (f_s/6, f_s/2)$, the grid-current feedback (GCF, shown by the orange dashed lines) should be employed to guarantee the system staying in the stable region. The block diagrams of the control systems are presented in Fig. 4.11. Due to the asymmetric features of control systems, the *d*- and *q*-axis block diagrams are separately presented. To simplify the analysis, in this chapter the bandwidth of PLL and dc-link voltage controller can be designed to be lower than the system fundamental frequency so that it has negligible effects on the control performance as well as stability [38]. Further studies shows the effects of the PLL mainly pose on the *q*-axis block diagram and *q*-axis admittances. The detailed model and analysis are given in Chapter 6.

It is worth noting that the control systems of the grid converters are not always included in the ST-fed grid, for instance, when grid converter is tripped by faults or grid converters for photovoltaic during the night. Under the circumstances, due to the deactivation of the grid converters, the effects of the control are no longer on the grid, only the *LCL*-type filters can be seen from the PCC that connecting to the grid. Since the *LCL*-type filter is usually symmetric and the coupling terms are negligible, it can be studied by the same way used in the passive loads analysis. The Nyquist plots of $G_{op,dd}$ with different multiloop strategies do not encircle $(-1, j0)$ and the pole maps of $G_{op,dd}$ of all case studies are presented in Fig. 4.12a. It can be seen that a pair of conjugate poles are introduced by the *LCL* resonance, which have been highlighted in the figure, and they are insensitive to the selection of different control

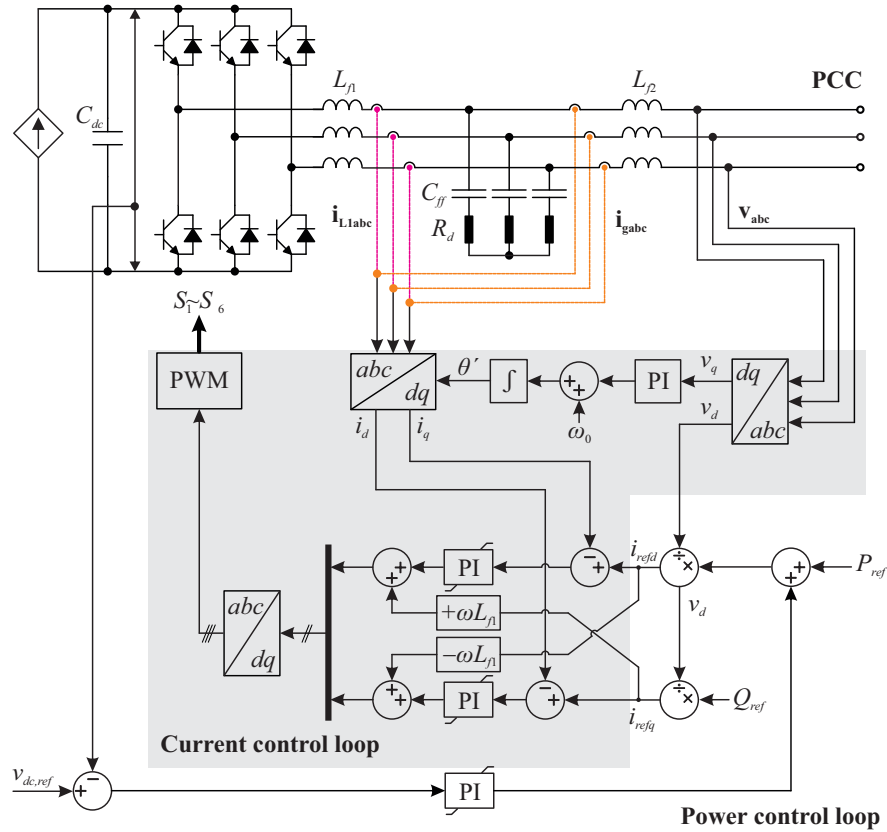


Figure 4.10: Basic control structure of a grid converter.

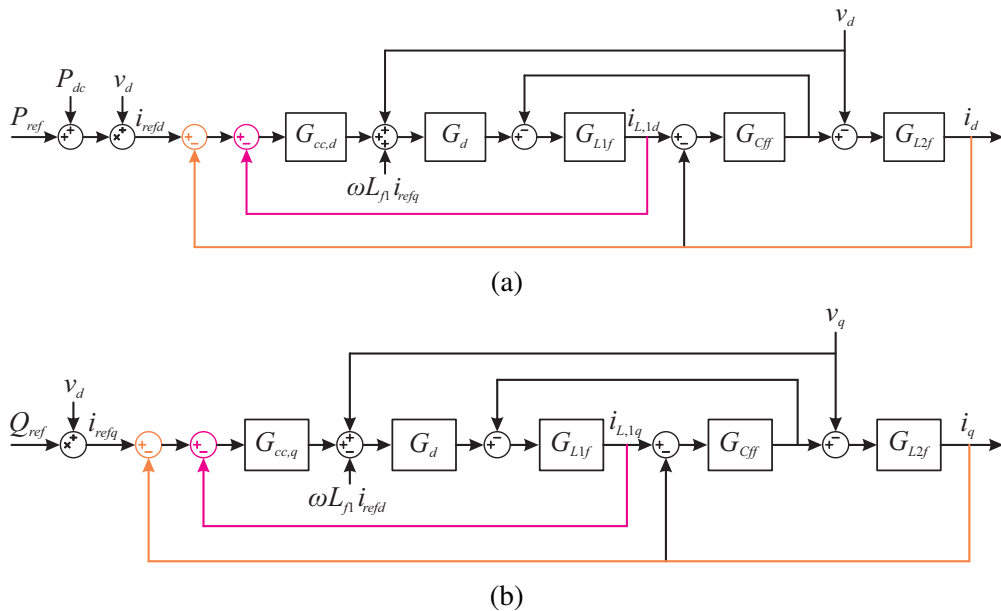
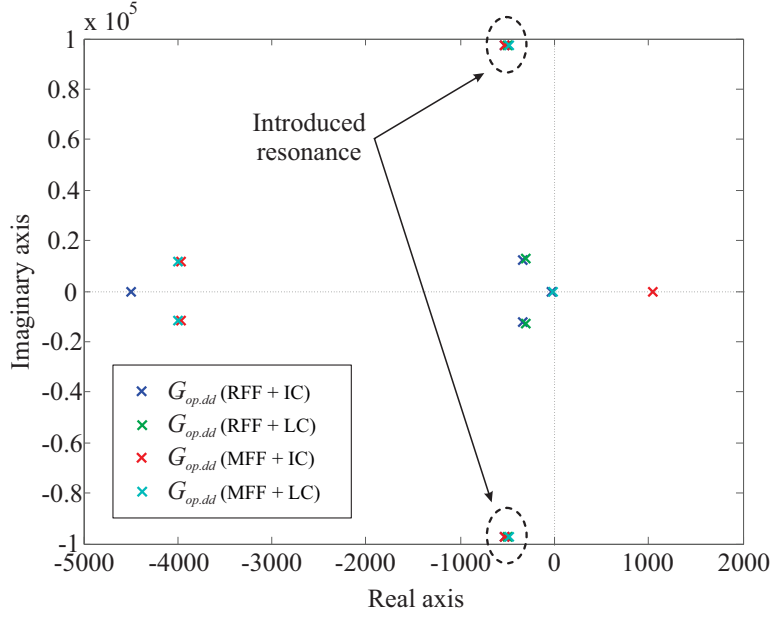
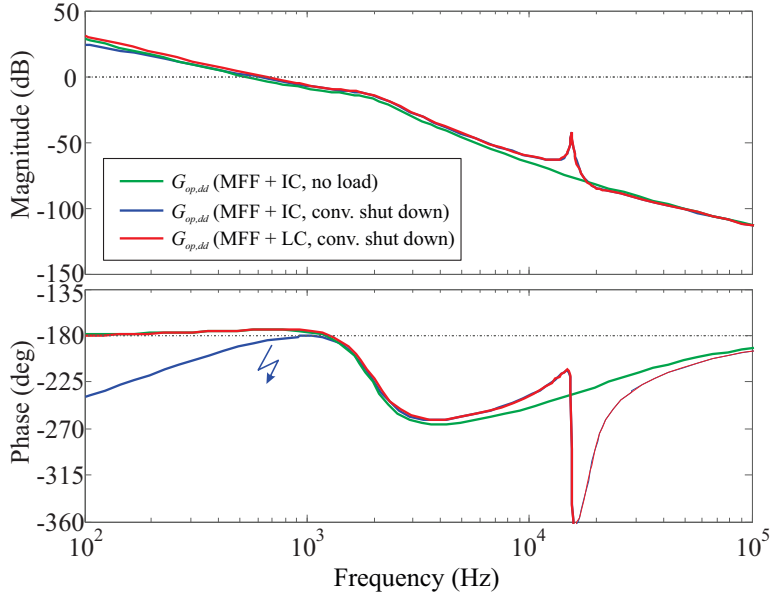


Figure 4.11: Block diagram of power/current control for grid converter in the synchronous frame: magenta feedback - converter-current feedback, orange feedback - grid-current feedback.

strategies. Similar to the passive loads case studies, the dominant poles of the measured voltage feedforward are much further away from the imaginary axis than those of the reference voltage feedforward. However, it is worth noting that the inductor-current inner loop could suffer from stability issues, since one of the poles on the real axis could shift to the



(a)



(b)

Figure 4.12: Stability analysis of a ST-fed grid when the grid converters being shut down: (a) pole maps of $G_{op,dd}$ when different multiloop strategies are used and (b) Bode plots of $G_{op,dd}$ when different multiloop strategies are used.

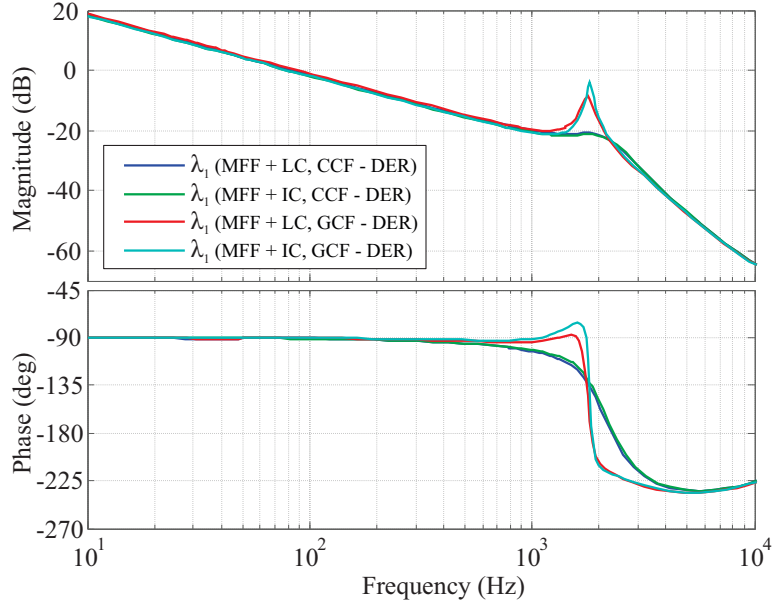
right half plane. To better reveal the issues, the Bode plots of $G_{op,dd}$ with different multiloop strategies are shown in Fig. 4.12b. The green curve is the open-loop Bode plot of the ST LV converter when no load is connected. When the *LCL*-type filter is connected to the grid, it can be seen that a resonance has been introduced while it is not critical due to the negative magnitude at the resonant frequency. The critical point appears in the low-frequency range when the inductor-current inner loop is used. A significant phase lagging is introduced and the minimal phase margin is likely to be negative, leading the system to be unstable. When the load- and inductor-current inner loop is used, the problem is no longer there, the overall system can maintain stable if the ST LV converter itself has sufficient phase margin.

During normal operation, the control systems of the grid converters are included in the ST-fed grid, and the effects of the LV grid with grid converters on the ST LV converter can be studied by including the full equivalent admittance matrix \mathbf{Y}_{eq} considering both control and physical filters. Because of the asymmetric and coupling features of \mathbf{Y}_{eq} , the generalized Nyquist criterion is used for the stability assessment and performance evaluation. The system stability can be determined based on the pole maps and the Nyquist diagrams of its eigenvalues. Namely, if $\mathbf{G}_{\text{op}} = \begin{bmatrix} G_{op,dd} & G_{op,dq} \\ G_{op,qd} & G_{op,qq} \end{bmatrix}$ has no right half plane poles, the system is asymptotically stable if and only if the eigenvalues of the characteristic loci fulfill the Nyquist stability criterion. Here, the eigenvalues can be derived by [56]:

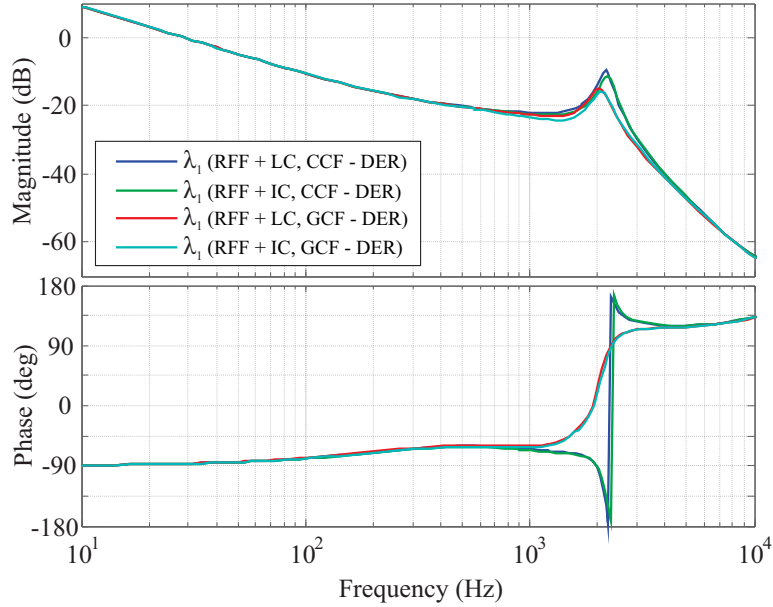
$$\lambda_{1,2} = \frac{G_{op,dd} + G_{op,qq}}{2} \pm \sqrt{\left[\frac{G_{op,dd} - G_{op,qq}}{2}\right]^2 - G_{op,dq}G_{op,qd}}. \quad (4.6)$$

The influences of two different inner loop feedback schemes are studied and the frequency responses of the eigenvalues of \mathbf{G}_{op} are shown in Fig. 4.13. In this study, all the eight possible scenarios, including four different multiloop control strategies and two different controls of grid converters, are considered. It can be seen that different inner loop feedback schemes present almost the same behaviors in the frequency domain, when the feedforward scheme and the control of grid converter are fixed. Take the measured voltage feedforward as an example (Fig. 4.13a), when a converter-current feedback converter is connected, the frequency response using the load- and inductor-current (blue curve) is overlapping with the response using the inductor-current (green curve). Likewise, when a grid-current feedback converter is connected, the frequency responses of the two different inner loop feedback schemes are overlapping as well. With this consideration, only one of the inner loop feedback schemes (i.e., load- and inductor-current scheme) is needed for the stability analysis in the followings, which saves the analysis efforts.

Then, the stability when the ST LV converter using two different voltage feedforward schemes are studied. In both case studies, the Nyquist plots of the eigenvalues do not encircle $(-1, j0)$, but some poles of the diagonal elements of \mathbf{G}_{op} locate on the right half plane. In Fig. 4.14b, a converter-current feedback converter is connected to the PCC, it can be seen that both $G_{op,dd}$ and $G_{op,qq}$ have a pair of conjugate poles locate on the right half plane when the reference voltage feedforward is applied, indicating the system is unstable, while all poles of \mathbf{G}_{op} locate on the left half plane when the measured voltage feedforward is used. In Fig. 4.14a, a grid-current feedback converter is connected to the PCC, it can be seen that the pair of conjugate poles using both feedforward schemes shift leftwards compared to Fig. 4.14b, especially the poles of the reference voltage feedforward move from the right half plane to the left, showing a significant improvement of stability. Under this condition, though the system is stable regardless of the feedforward schemes, it is worth noting that the damping ratios of the dominant poles using the measured voltage feedforward is 5-time larger than the ones using the reference voltage feedforward.



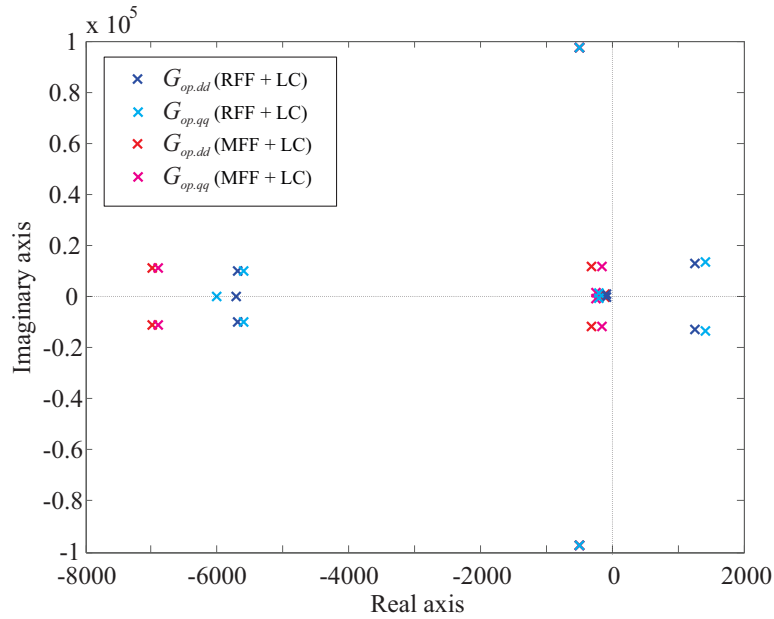
(a)



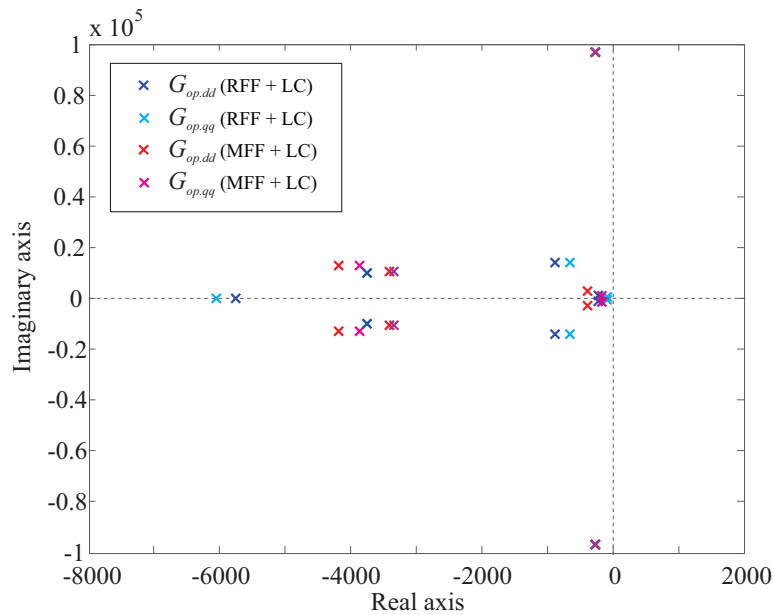
(b)

Figure 4.13: Frequency responses for λ_1 of \mathbf{G}_{op} when different multiloop voltage control strategies are applied: (a) combination of the measured voltage feedforward and different inner loop schemes and (b) combination of the reference voltage feedforward and different inner loop schemes.

The parameter sensitivity to the control gain variation is studied and the root loci using the two different voltage feedforward schemes are shown in Fig. 4.15, where the blue curves indicate the measured voltage feedforward and the red ones indicate the reference voltage feedforward. For simplicity, only the root loci of $G_{op,dd}$ are given while the root loci of other elements present the same behavior. To ensure the grid is stable initially, a grid-current feedback converter is connected to the LV grid and the control gains of the voltage controller start from their nominal value (i.e., 1 p.u.) and keep increasing with a 1 p.u. step. It is shown that a pair of conjugate poles are moving towards the imaginary axis when the control gains



(a)



(b)

Figure 4.14: Stability analysis of the ST LV converter when different voltage feedforward schemes are applied: (a) pole maps of \mathbf{G}_{op} when a converter-current feedback converter is connected and (b) pole maps of \mathbf{G}_{op} when a grid-current feedback converter is connected.

increase for both feedforward schemes. Meanwhile, for the measured voltage feedforward, a pair of conjugate poles in the lower frequency shift towards left when increasing control gain. The gain range of the reference voltage feedforward scheme is much narrower than that of the measured voltage feedforward scheme, where in this study the gain using the measured voltage feedforward can reach up to 15 p.u. maintaining stable operation, while the gain using the reference voltage feedforward can only reach up to 4 p.u. with the stability concern.

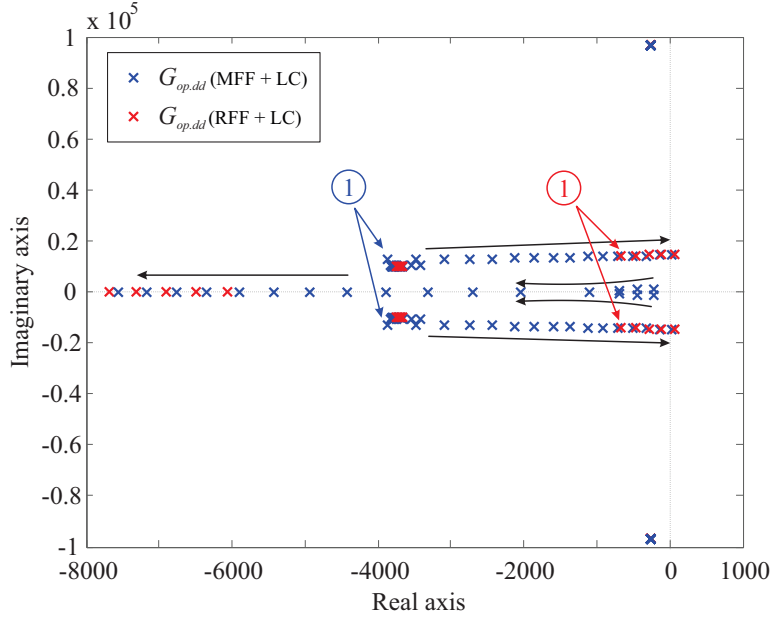


Figure 4.15: Parameter sensitivity analysis when different voltage feedforward schemes are applied: blue - measured voltage feedforward, red - reference voltage feedforward.

The dynamics performance of different voltage feedforward schemes are evaluated and the closed-loop transfer function matrix of the ST LV converter is defined by

$$\mathbf{G}_{cl} = \mathbf{G}_{op} \cdot [\mathbf{I} + \mathbf{G}_{op}]^{-1}. \quad (4.7)$$

The frequency responses for the eigenvalues of \mathbf{G}_{cl} are illustrated in Fig. 4.16. Initially, the control gains for both voltage feedforward schemes are at their nominal value (i.e., 1 p.u.), the frequency responses for λ_1/λ_2 are shown by blue curves (the reference voltage feedforward) and green curves (the measured voltage feedforward), respectively. It can be seen that the reference voltage feedforward offers higher bandwidth than the measured voltage feedforward with the same gain. Since the gain range of the measured voltage feedforward is much higher than that of the reference voltage feedforward, a larger voltage control gain (e.g., 5 p.u., which is far away the gain limit 15 p.u. with stability concern) is implemented to the measured voltage feedforward scheme and its frequency responses of λ_1/λ_2 are represented by red curves, and the responses as well as the bandwidth are approaching those of the reference voltage feedforward. Moreover, it can be observed that the reference voltage feedforward has a resonance in the high-frequency range and the measured voltage feedforward has one in the mid-frequency range, but the measured voltage feedforward can employ a larger gain to well alleviate the resonance and therefore is less likely to suffer from harmonic stability or resonance issue.

4.3.3 Impacts of Line Impedance

In an actual distribution network, the effects of line impedance play an important role on the system stability. The root loci of the overall system with the measured voltage feedforward

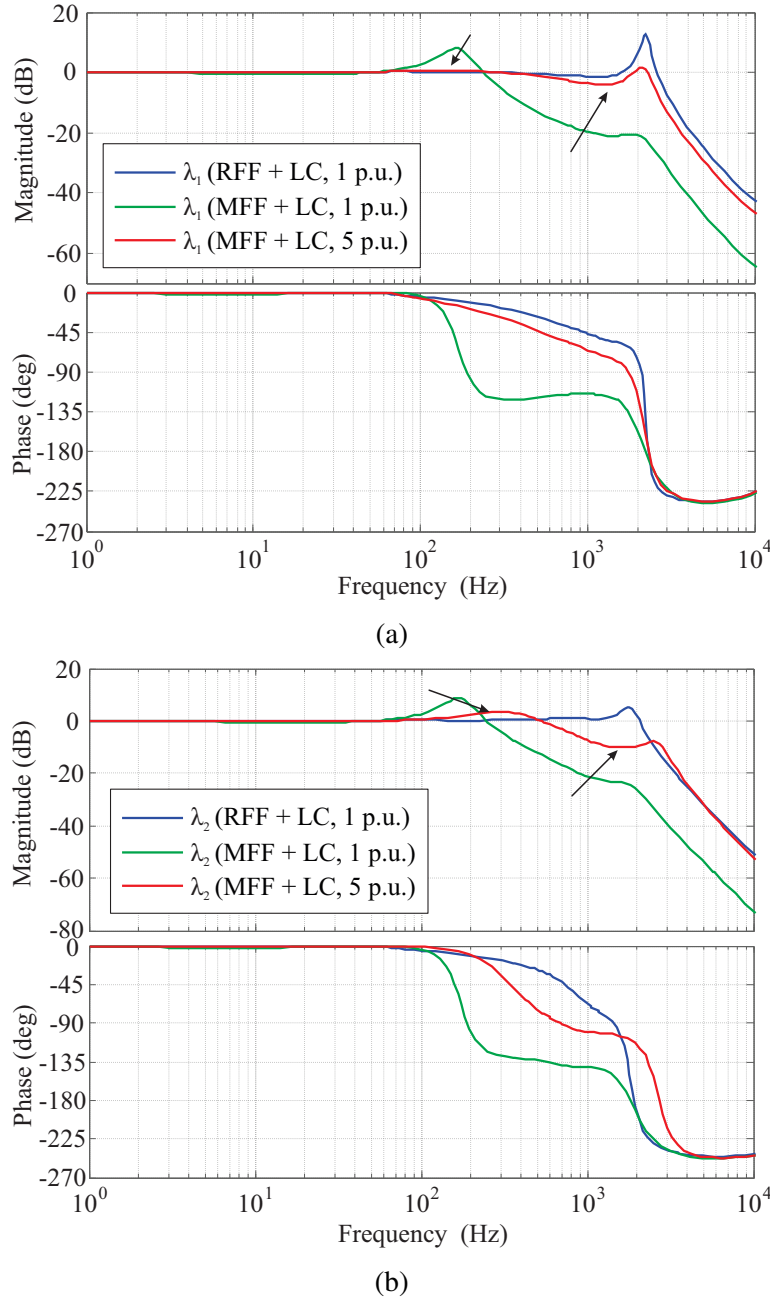


Figure 4.16: Frequency responses of \mathbf{G}_{cl} with different control gains: (a) λ_1 and (b) λ_2 .

when considering different line impedances are presented in Fig. 4.17. In Fig. 4.17a, different line lengths between the ST and the PCC are studied, where the line length varies from 50 m to 700 m. It can be seen that both pairs of the conjugate poles are moving leftwards when increasing the line length, indicating the overall system is more stable when the line between the ST and the PCC is longer. Different X/R ratios are investigated, changing from 0.5 to 1, and shown in Fig. 4.17b. It can be seen that one pair of the conjugate poles are not sensitive to the variation of the X/R ratio, while the other pair of the conjugate poles shift towards the imaginary axis, indicating the system is more stable with lower X/R ratio. From the root loci, it is found that the system stability can be improved by increasing the resistive components of the network.

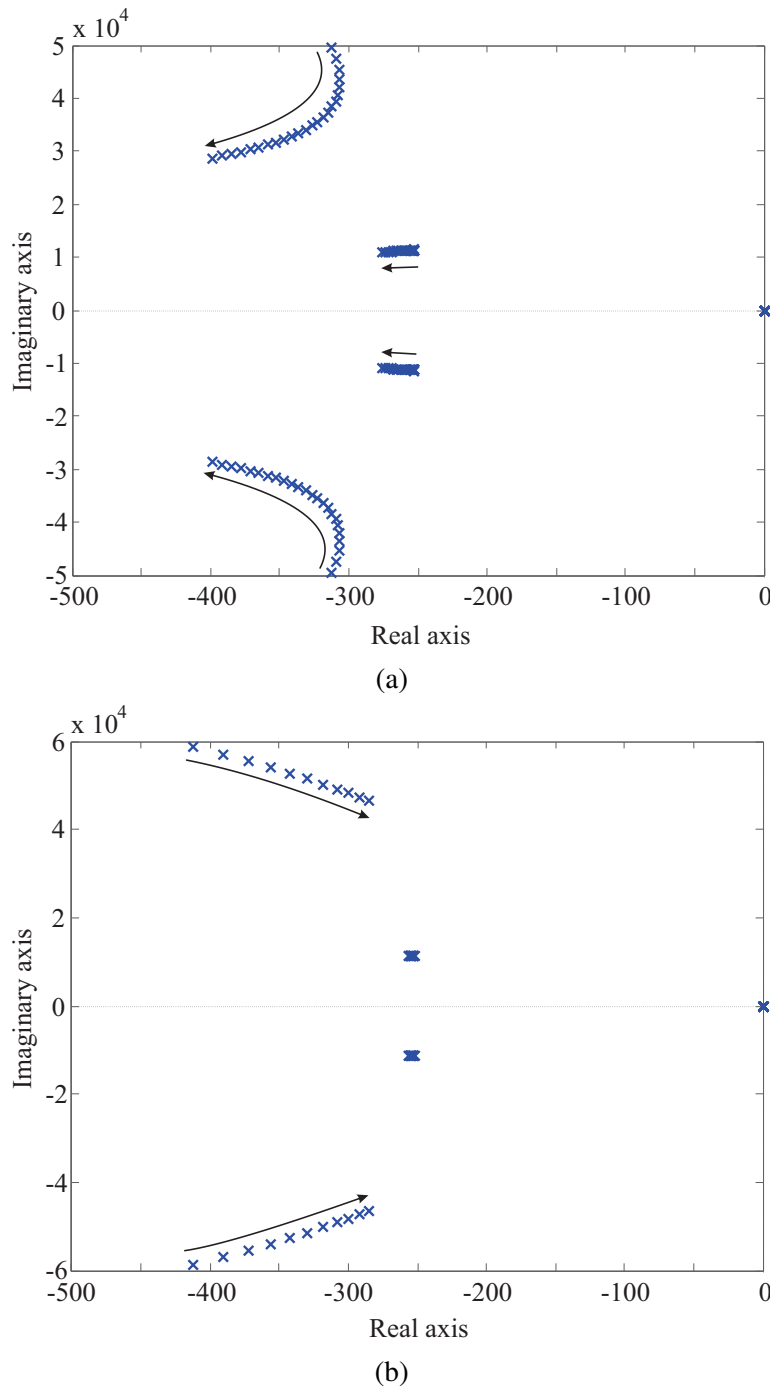


Figure 4.17: Root loci of the overall system with measured voltage feedforward when effects of line impedance are considered: (a) varying line length and (b) varying X/R ratio.

4.4 Simulation and Experimental Results

To test the above-mentioned multiloop voltage control, a CIGRÉ 18-Bus benchmark grid, shown in Fig. 4.19, is employed and implemented in MATLAB/Simulink with the aid of PLECS toolbox. Under the testbed, it is possible to study the features and verify the analysis in an extended grid. Furthermore, a ST-fed laboratory grid prototype has been developed and experimental results are given in the followings.

4.4.1 Case Study

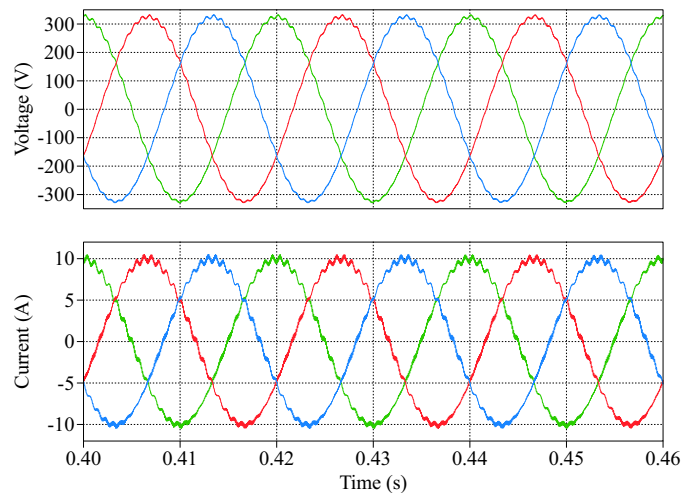
Case study is carried out in a radial distribution grid via MATLAB/Simulink with the aid of PLECS toolbox. In this case study, a ST LV converter represents the voltage source of the grid and a grid converter is connected to the terminal. Different line lengths and types are configured for the grid, while the system as well as control parameters for the ST and the grid converter remain the same.

Two different line types with different X/R ratios are configured between the ST and the PCC of the grid converter, and the line length is 60 m. When the UG-01 type line ($R(\Omega/km) = 0.163$, $X(\Omega/km) = 0.136$, $X/R = 0.83$) is used, as seen in Fig. 4.18a, the overall system tends to be unstable, where the PCC voltage and the current of the grid converter are oscillating. When the UG-02 type line ($R(\Omega/km) = 0.266$, $X(\Omega/km) = 0.151$, $X/R = 0.57$) is used, as seen in Fig. 4.18b, it can be noticed that the X/R ratio reduces and the overall system can maintain stable operation. However, when the UG-02 type line is shortened, i.e., 35 m, shown in Fig. 4.18b, the instability phenomenon can be observed again in both PCC voltage and converter current.

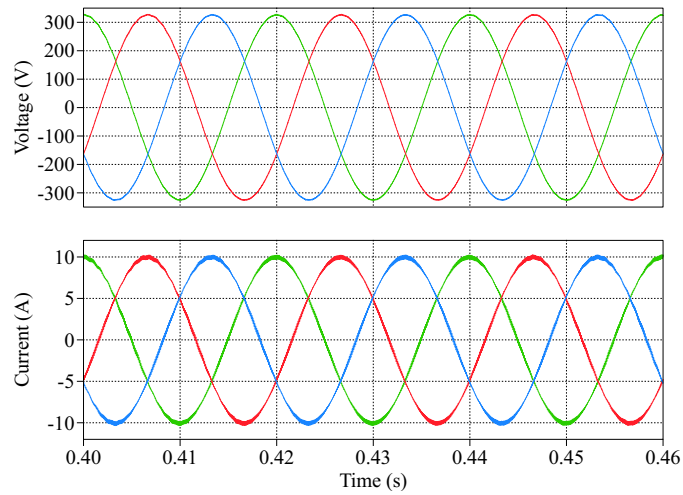
Then, a CIGRÉ 18-Bus benchmark grid, shown in Fig. 4.19, is employed and implemented in MATLAB/Simulink with the aid of PLECS toolbox. The configuration of the CIGRÉ 18-Bus benchmark grid is referring to [59]. The detailed cable configuration including cable types and lengths of the benchmark grid are illustrated in Table 4.3 and Table 4.4. The ST has been used in the benchmark grid and the ST LV converter is connected to Bus R01, being the voltage source of the benchmark grid. Various types of passive loads are connected to Bus R11, R15, R16, R17, and R18. Grid-converter-based devices are connected to Bus R15 and R18. In the following case study, the load- and inductor-current scheme is adopted as the inner loop feedback, and the measured voltage feedforward and the reference voltage feedforward are tested with the phase margin of 45° during standalone mode. Two scenarios are tested under the CIGRÉ grid to evaluate the performance of different voltage feedforward schemes in an extended grid.

In the first scenario, the connected passive loads are dominant (i.e., 1 p.u.) and the generation of the grid converters are low, which is 0.6 p.u., the shortage of the power is supplied by the main grid through the ST. Here, the nominal power is 75 kW. At $t = 0.5$ s, the voltage feedforward scheme of the ST LV converter switches from the measured voltage feedforward to the reference voltage feedforward. The voltage waveforms using the measured voltage feedforward and the reference voltage feedforward are shown in Fig. 4.20a and Fig. 4.20b, respectively. Comparing the voltage waveforms, it can be seen that the switch of the feedforward scheme does not affect the bus voltages in the CIGRÉ grid and the grid can maintain stable operation with both feedforward. The spectrum of the voltage at Bus R01 shown in Fig. 4.20c further confirms it, showing the power quality of the voltage with both feedforward is at the same level when the passive loads are dominant.

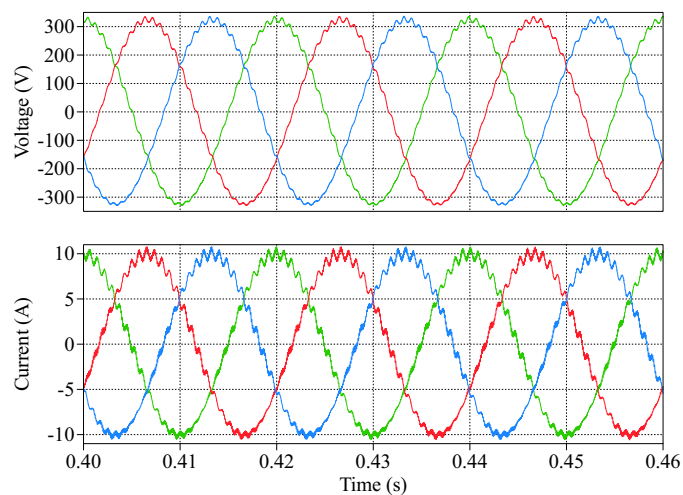
In the second scenario, the power converters are dominant in the LV grid, the consumption of the passive loads (i.e., 0.6 p.u.) are lower than the generation of the power converters



(a)



(b)



(c)

Figure 4.18: PCC voltage and injected current of grid converter with different line lengths and types: (a) UG-01, $X/R = 0.83$, 60 m, (b) UG-02, $X/R = 0.57$, 60 m, and (c) UG-02, $X/R = 0.57$, 35 m.

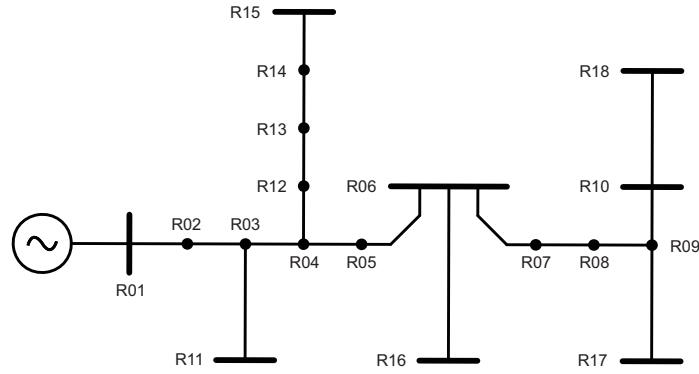


Figure 4.19: CIGRÉ benchmark microgrid, adapted from [59].

Table 4.3: Line Configuration

Name	From	To	Cable	Length (m)
<i>L-01</i>	<i>R-01</i>	<i>R-02</i>	<i>UG-01</i>	35
<i>L-02</i>	<i>R-02</i>	<i>R-03</i>	<i>UG-01</i>	35
<i>L-03</i>	<i>R-03</i>	<i>R-04</i>	<i>UG-01</i>	35
<i>L-04</i>	<i>R-04</i>	<i>R-05</i>	<i>UG-01</i>	35
<i>L-05</i>	<i>R-05</i>	<i>R-06</i>	<i>UG-01</i>	35
<i>L-06</i>	<i>R-06</i>	<i>R-07</i>	<i>UG-01</i>	35
<i>L-07</i>	<i>R-07</i>	<i>R-08</i>	<i>UG-01</i>	35
<i>L-08</i>	<i>R-08</i>	<i>R-09</i>	<i>UG-01</i>	35
<i>L-09</i>	<i>R-09</i>	<i>R-10</i>	<i>UG-01</i>	35
<i>L-10</i>	<i>R-03</i>	<i>R-11</i>	<i>UG-04</i>	30
<i>L-11</i>	<i>R-04</i>	<i>R-12</i>	<i>UG-02</i>	35
<i>L-12</i>	<i>R-12</i>	<i>R-13</i>	<i>UG-02</i>	35
<i>L-13</i>	<i>R-13</i>	<i>R-14</i>	<i>UG-02</i>	35
<i>L-14</i>	<i>R-14</i>	<i>R-15</i>	<i>UG-02</i>	30
<i>L-15</i>	<i>R-06</i>	<i>R-16</i>	<i>UG-06</i>	30
<i>L-16</i>	<i>R-09</i>	<i>R-17</i>	<i>UG-04</i>	30
<i>L-17</i>	<i>R-10</i>	<i>R-18</i>	<i>UG-05</i>	30

(i.e., 1 p.u.) in the LV grid, and thus reverse power flow happens in this case. At $t = 0.5$ s, the voltage feedforward scheme of the ST LV converter switches from the measured voltage feedforward to the reference voltage feedforward, and the voltage waveforms before and after the switch are shown in Fig. 4.21a and Fig. 4.21b, respectively. In Fig. 4.21a, the bus voltages in the CIGRÉ grid can maintain stable operation with good power quality when the measured voltage feedforward is used. In Fig. 4.21b, the bus voltages start to oscillate leading to instability when the reference voltage feedforward is used.

Table 4.4: Cable Types

Type	R' (Ω/km)	X' (Ω/km)	R'/X'
UG-01	0.163	0.136	1.199
UG-02	0.266	0.151	1.762
UG-04	1.541	0.206	7.481
UG-05	1.111	0.195	5.697
UG-06	0.569	0.174	3.270

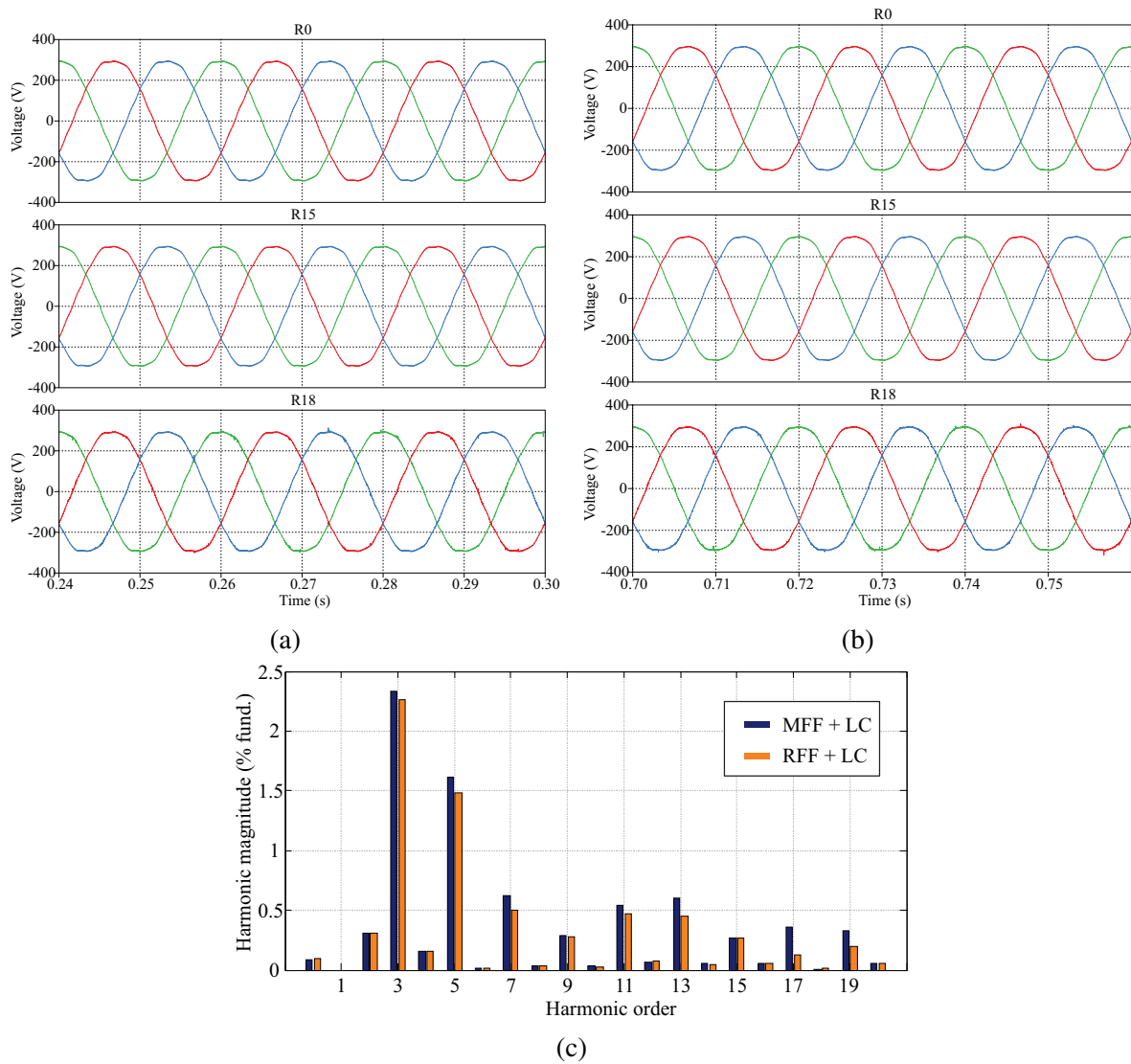


Figure 4.20: Bus voltages of a CIGRÉ benchmark grid when passive loads are dominant in the LV grid when the ST uses: (a) voltage waveforms using the MFF, (b) voltage waveforms using the reference voltage feedforward, and (c) spectrum of Bus R01.

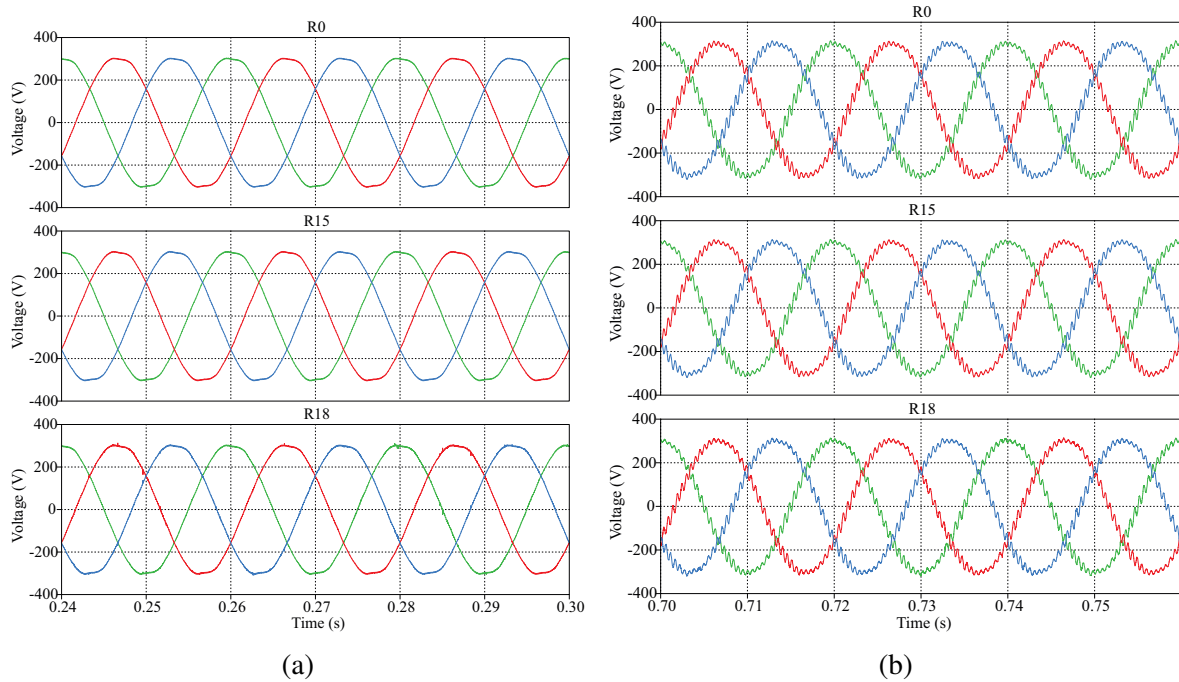


Figure 4.21: Bus voltages of a CIGRÉ benchmark grid when power converters are dominant in the LV grid when the ST uses: (a) measured voltage feedforward and (b) reference voltage feedforward.

4.4.2 Experimental Validation

To verify the effectiveness of the theoretical analyses, experimental validations have been carried out in a laboratory ST-fed grid as shown in Fig. 6.19. Two Danfoss inverters are used for the ST LV side converter and the power converter. The control strategy of Fig. 4.6 for the ST converter has been implemented in a dSPACE. For the sake of convenience, the control of the power converter has been achieved by the same dSPACE 1006 processor board as well. Linear and nonlinear loads are connected to the PCC of LV grid. The system parameters are listed in Table 7.3.

The influences of different inner feedback loop schemes are studied and the results are shown in Fig. 4.23. A grid-current feedback converter is connected to the LV side to guarantee stability. An online control switch has been used to switch from one inner loop to the other, where the switch signal is illustrated by the green curve: low level - the inductor-current, high level - the load- and inductor-current. It can be seen that the three-phase ST voltage waveforms (shown in Fig. 4.23a) before and after the switch present similar stability condition. From the spectrum analysis (shown in Fig. 4.23b), it indicates that both current inner loops present similar level of power quality.

Then, a grid converter is connected to the PCC. Before evaluating different voltage feedforward schemes, the control gain of the voltage control strategy with the measured voltage feedforward is studied. In previous analysis, it is indicated that the measured voltage feedforward with lower gain presents resonance peak in the mid-frequency range and could lead to instability, while higher control gain can eliminate it. In Fig. 4.24a, the control gain of

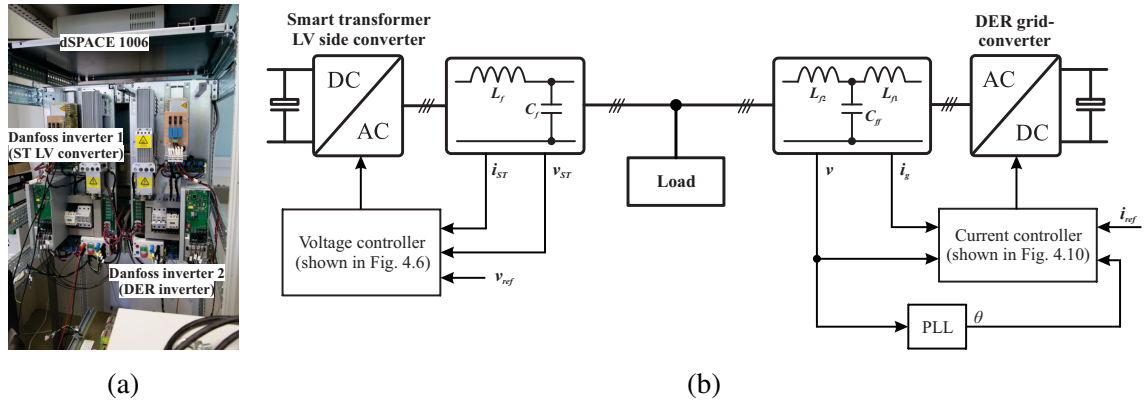


Figure 4.22: Laboratory setup: (a) photo and (b) configuration and control schematics.

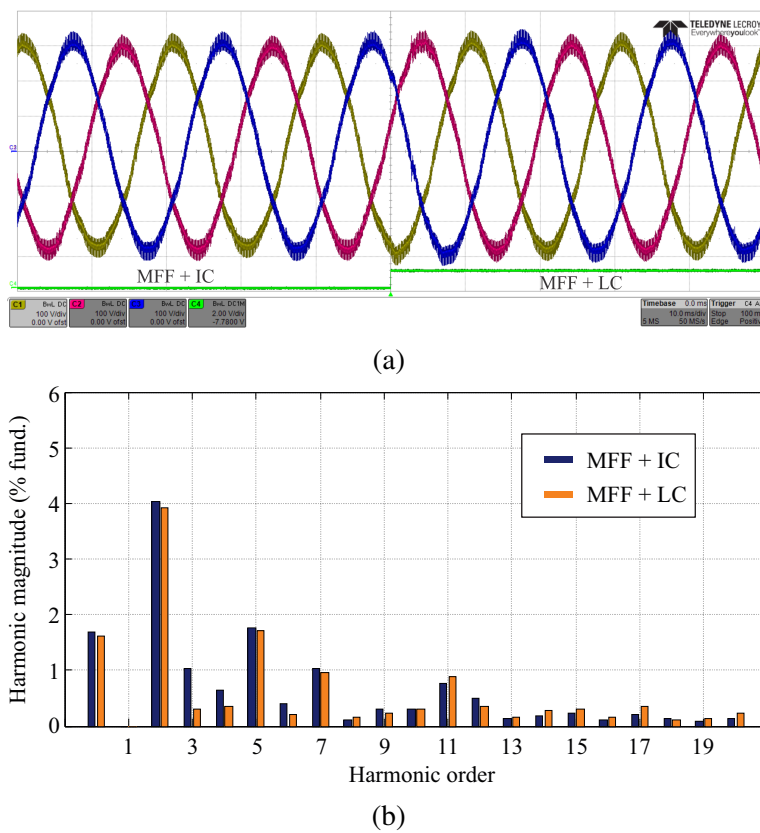


Figure 4.23: Experimental results of the ST output voltage with different inner loop schemes when grid converter is connected (time: 10 ms/div, voltage: 100 V/div).

1 p.u. is used and it can be seen that the voltage and current are highly distorted and oscillated, indicating harmonic instability occurs. In Fig. 4.24b, the control gain of 5 p.u. is used and both the voltage and the current are stable with good power quality. As a result, for the measured voltage feedforward, high control gain (5 p.u.) is used in the following evaluation and comparisons.

When a converter-current feedback grid converter is connected to the LV grid, the waveforms of three-phase ST voltage and current (phase A) with different feedforward schemes are shown in Fig. 4.25. The load- and inductor-current feedback scheme is used for the inner loop. It can be seen that the voltage and current are oscillating when the reference voltage

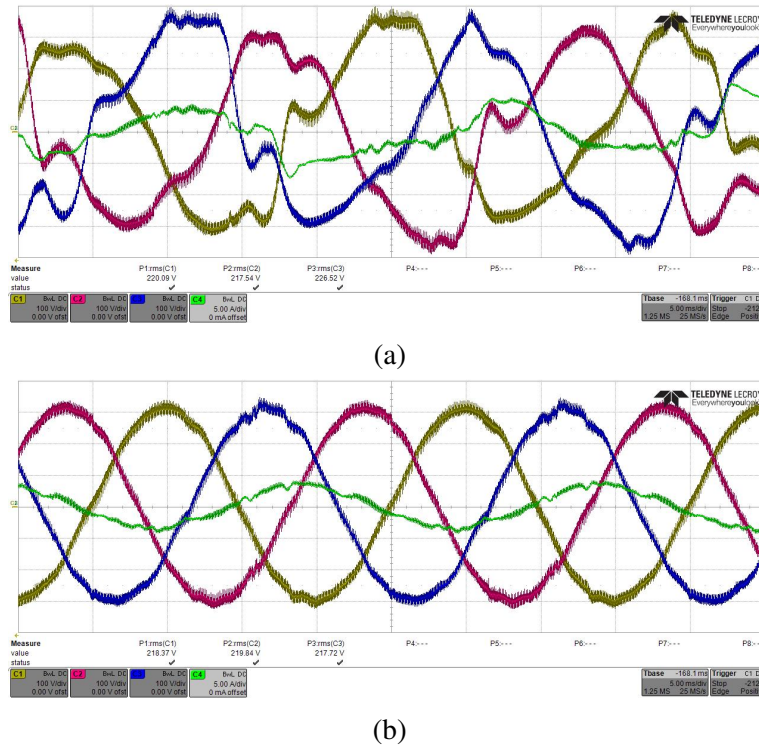


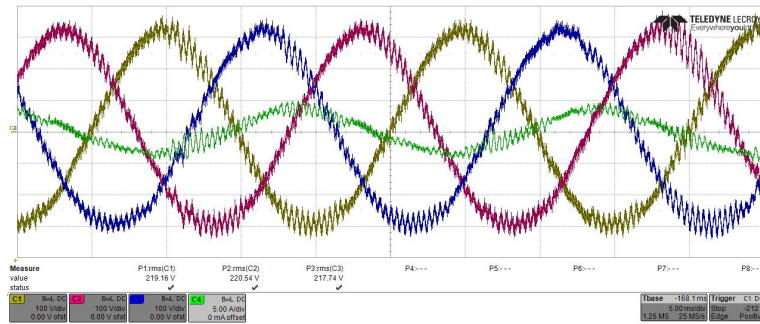
Figure 4.24: Experimental results of the three-phase ST output voltage and current (phase A) with measured voltage feedforward scheme when a converter-current feedback grid converter is connected (time: 5 ms/div, voltage: 100 V/div, current: 5 A/div): (a) small control gain (1 p.u.) and (b) high control gain (5 p.u.).

feedforward is used, indicating instability occurs, while the grid can maintain stable when the measured voltage feedforward is applied. This indicates the ST-fed grid has to employ the measured voltage feedforward for maintaining stability when the converter-current feedback grid converters are connected to the LV grid.

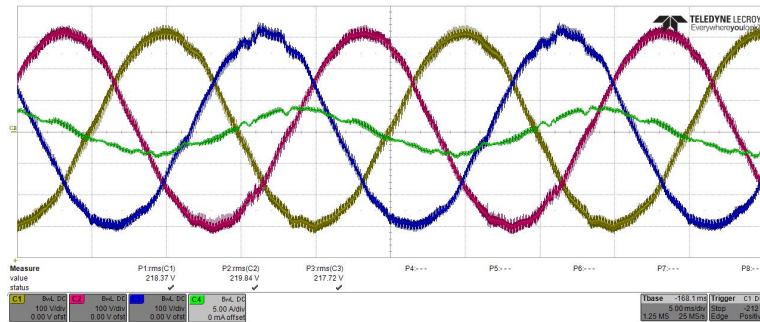
When a grid-current feedback converter is connected to the PCC, and the waveforms of three-phase ST voltage and current (phase A) with different feedforward schemes are shown in Fig. 4.26. In this test, both voltage feedforward schemes can maintain stable operation of the ST-fed grid. Moreover, the power quality of both voltage waveforms are at the same level which can be seen from Fig. 4.25c.

4.5 Summary of the Chapter

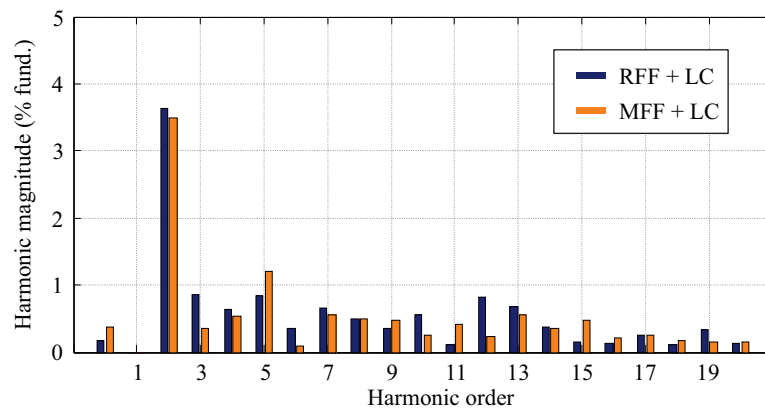
A comprehensive stability assessment of different multiloop voltage control strategies is carried out in this chapter. It is shown that the measured voltage feedforward scheme can provide stable operation under various conditions, while the reference voltage feedforward could lead to instability under some circumstances, especially when converter-current-feedback-controlled grid converters are connected. Nevertheless, comparing the the control gain of the reference voltage feedforward, a higher control gain (e.g., 5 p.u. in the case study) is suggested when the measured voltage feedforward is employed since it could suffer from



(a)



(b)



(c)

Figure 4.25: Experimental results of the three-phase ST output voltage and current (phase A) with different feedforward schemes when a converter-current feedback grid converter is connected (time: 5 ms/div, voltage: 100 V/div, current: 5 A/div): (a) with reference voltage feedforward scheme, (b) with measured voltage feedforward scheme, and (c) voltage spectrum.

harmonic stability issues when the gain is low. For the inner loop, the load- and inductor-current can always maintain stability under various conditions, however the inductor-current encounters stability issues in particular when the grid converters are disable but still connecting to the grid. With these considerations, the multiloop strategy which adopts the measured voltage feedforward and the load- and inductor-current inner loop is an optimal solution to guarantee stable operation of a ST-fed grid. In a practical grid, the resistive component of the distribution network benefits stable operation and therefore sufficient line length and proper line type can largely avoid harmonic instability in a ST-fed LV grid. Case studies in a CIGRÉ benchmark grid and experimental results in a laboratory-size ST-fed grid further

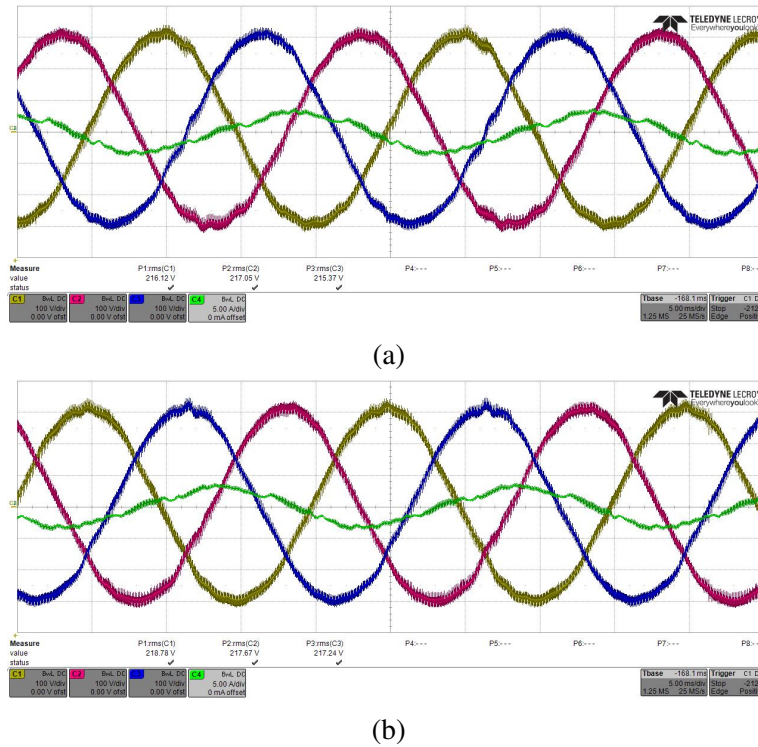


Figure 4.26: Experimental results of the three-phase ST output voltage and current (phase A) with different feedforward schemes when a grid-current feedback grid converter is connected (time: 5 ms/div, voltage: 100 V/div, current: 5 A/div): (a) with reference voltage feedforward scheme and (b) with measured voltage feedforward scheme.

verify the effectiveness of the optimal solution as well as the analysis. Moreover, the case studies and results show that the power quality of this optimal solution is comparable to the other multiloop strategies under various conditions. Furthermore, the grid-current feedback grid converter is recommended to be used in a ST-fed grid, which is less likely suffering from the stability issues in such grid comparing to its counterpart converter-current feedback grid converter.

The study of the interactions between the ST and the LV grid starts from this chapter. Since the first target of the ST LV converter, is to find an optimal control solution which maintains stable operation, this chapter mainly investigates the control interactions, while it is also shown that the resonances of the LV grid are potentially hazardous for stability, for instance, when the grid converters are shut down. In addition to resonances, it is known that the grid synchronization could incur stability issues in distribution grids. The problems and the solutions of resonances and synchronization in a ST-fed grid deserve further investigation. In this context, the stability issues related to these two aspects are studied in Chapter 5 and Chapter 6, respectively.

5 Analysis and Stabilization of Smart Transformer-fed Grid

In addition to the control interactions, the resonances introduced by the output filters of the grid converters compromise the system stability, where its impacts on the ST LV converter are highlighted in Fig. 5.1. This chapter starts with the problem formulation of resonances in both conventional distribution grid and the ST-fed grid. Based on the discovered critical regions, this chapter aims at reshaping the equivalent impedance of the ST LV converter within certain regions and therefore stabilizing the issues in the LV grid. To address the issue of time-varying resonances, online impedance measurement is achieved by means of ST LV converter and it provides real-time grid information for the stabilization methods.

5.1 New Challenges in LV Grid With Stability Concerns

The penetration of DERs is growing rapidly in distribution grids and microgrids. Being affected by the control dynamics and switching techniques, the stability problems arise which can be studied by small-signal analysis [60, 61]. In the context, the stability of an electric grid dominated by the grid inverters have drawn wide attentions, particularly focusing on the topics including system modeling [62], control and filter design [63], stability assessment [55].

One important aspect determining the stability of grid converters is the ratio of grid impedance to converter impedance [62, 52]. Once the converter impedance is fixed, the variation of grid impedance would incur stability issues and lead to the performance degradation of the overall grid. With this consideration, in a conventional distribution grid, one possibility is to appropriately design the control of grid converter or reshape the converter impedance in the critical regions, ensuring the grid converter can adapt to a certain range of grid impedance variation [64, 65, 66]. On the other hand, the newly proposed ST concept provides another possibility to mitigate the stability issues of the grid converters [14]. One scenario is to adapt the dynamic properties of the ST in order to interact with the grid converters of DERs. Like the active dampers [67], which can reshape the equivalent grid impedance to the paralleled grid converters at same PCC, the idea is to directly reshape the grid impedance by means of the ST that is connected to the LV ac grid in series, aiming at modifying the relationship between grid impedance and converter impedance so that the ST can facilitate the stabilization of all local grid converters as well as the whole LV grid. Compared to the traditional decentralized stabilization solutions, the reshaping of the ST output impedance is expected to be an indispensable service provided to all the available DERs and grid-converter-interfaced loads with "plug-and-play" functionality. It can avoid advanced control or sensors being implemented locally, and therefore reduces the computation burden and cost of the DERs and EV charging stations. Rather than designing a robust local control system, the ST can rapidly adjust the grid profiles to meet the evolving and unpredictable requirements from utility and local customers.

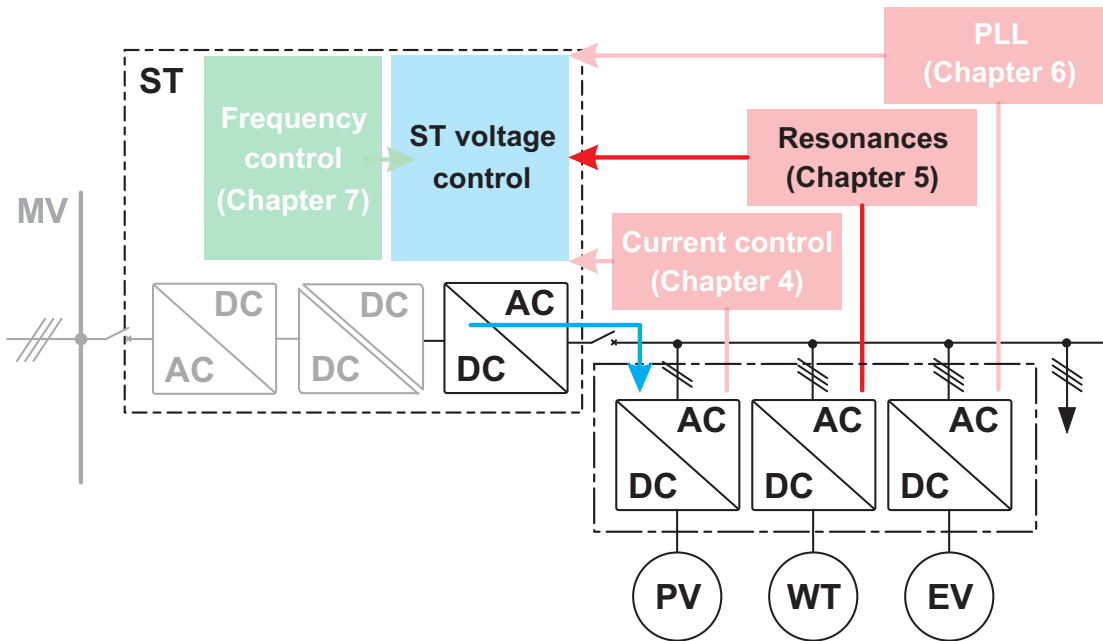


Figure 5.1: Research focus of Chapter 5: interactions between ST and filter resonances of grid converters.

Moreover, the grid features like resonances are not fixed in an actual grid. The activation/deactivation and connection/disconnection of the renewable energy system can drastically change the resonance profile of the grid. In particular, the resonance profiles of a PV power station during the daytime and night are very different [35]. Therefore, the stability conditions of the LV grid are presenting time-varying characteristic accordingly. Conventionally, either the local control for the grid converter or the control system for the active damper can hardly obtain the full map of the grid resonances in real time. Thanks to the series connection, the ST is able to online identify the resonances in the LV grid with the assist of a resonance identification algorithm. The identified resonances information can be easily converted to the frequency-domain transfer functions by using model approximation methods, which makes online stability margin estimation to be reality. The information, for instance, resonant frequency, estimated phase margin, allows the ST to well stabilize the LV grid under various circumstances and improves the robustness of the ST-fed grid.

In general, the objective of this chapter is to propose a centralized stabilization and identification scheme by means of the ST LV converter to address instability caused by grid-converter-interfaced DERs as well as loads, especially the resonance issues. Knowing that the active damping method is efficient in dealing with resonances, it is also considered in the ST stabilization application. To study the effectiveness of the schemes in an extended grid, tests under a CIGRÉ benchmark grid by using a real time digital simulator (RTDS) system and a laboratory ST-fed grid have been carried out. It is known that the flexible alternating current transmission system (FACTS) is one of the most efficient alternatives in transmission system against power system problems [68], one of the main purposes of this study is to prove that using a ST in power grids makes it possible to facilitate system operation in MV/LV distribution grid.

5.2 Stability Issues in LV Distribution Grids with Integration of Grid-Converter-based Devices

The stability issues could emerge in both traditional power transformer-fed and ST-fed grid with the increasing of power electronics interfaces. Nevertheless, the representation and the stabilization methods are quite different according to the different grid features. In this subsection, the stability issues of the two different grids will be illustrated and compared.

5.2.1 Stability Issue of a Traditional Transformer-fed Grid

In a traditional transformer-fed grid, the grid-converter-based devices are controlled as a constant power/current source and the grid can be represented by a Thévenin circuit (see Fig. 5.2a). The grid converter is connected to the PCC through an output filter, and a synchronization and a power/current controller are necessary to regulate the output power/current of the system. As found in Chapter 4, the GCF-controlled grid converter offers more stable operating condition in the ST-fed grid. To investigate the influence of the grid impedance on the grid converter, a schematic diagram of a GCF-controlled grid converter with an *LCL* filter considering the grid impedance is shown in Fig. 5.2b. The grid impedance Z_g (highlighted by the red block) is coupled to the closed-loop system, where G_{cc} is the transfer function of the current controller, G_d represents a one-and-half-sample computational and PWM delay, $G_{L1f} = 1/L_{f1}s$, $G_{L2f} = 1/L_{f2}s$, $G_{cff} = 1/C_{ff}s$ are the admittance of the converter-side inductor and the grid-side inductor, and the impedance of the capacitor, of the *LCL* filter, respectively. Based on Fig. 5.2b, the open-loop transfer function is

$$G_{op,der}(s) = G_{cc}(s)G_d(s)G_{cff}(s)G_{L1f}(s)G_{L2f}(s) \cdot [G_{cff}(s)(G_{L1f}(s) + G_{L2f}(s)) + 1 + G_{L2f}(s)Z_g(s)(1 + G_{cff}(s)G_{cff}(s))]^{-1}. \quad (5.1)$$

In practical cases, Z_g would vary in a certain range depending on the grid configuration in terms of cable length, power transformer parameter, and loads as well as "plug-and-play" devices [69]. Thus the stability margin of (5.1) would change. An example of the stability of grid converter under different grid impedance conditions is studied and the corresponding Bode diagram is shown in Fig. 5.3. In this case, a PI controller is employed as the current controller, an *LCL* output filter with the parameters of $L_{f1} = 5.03$ mH, $L_{f2} = 0.5$ mH, and $C_{ff} = 10$ μ F is used, and two different grid impedance are considered. Initially, the current control system considering $Z_g = 0.00025 \cdot s + 0.15$ (X/R ratio is 0.5) is designed with a phase margin of 49.5 deg (red curve in Fig. 5.3). When the grid impedance changes, the stability of the control system can not always be guaranteed. From the Bode diagram, it is seen that a -180° crossing occurs at the neighborhood of the resonant frequency where the magnitude is positive, when a different grid impedance is considered, for example, X/R ratio is 5, shown by the blue curve in Fig. 5.3. As a result, the stability of a grid-connected converter cannot always be guaranteed in a traditional transformer-fed grid even it is designed with an acceptable stability margin. To address this issue, advanced control algorithms for grid-interfaced

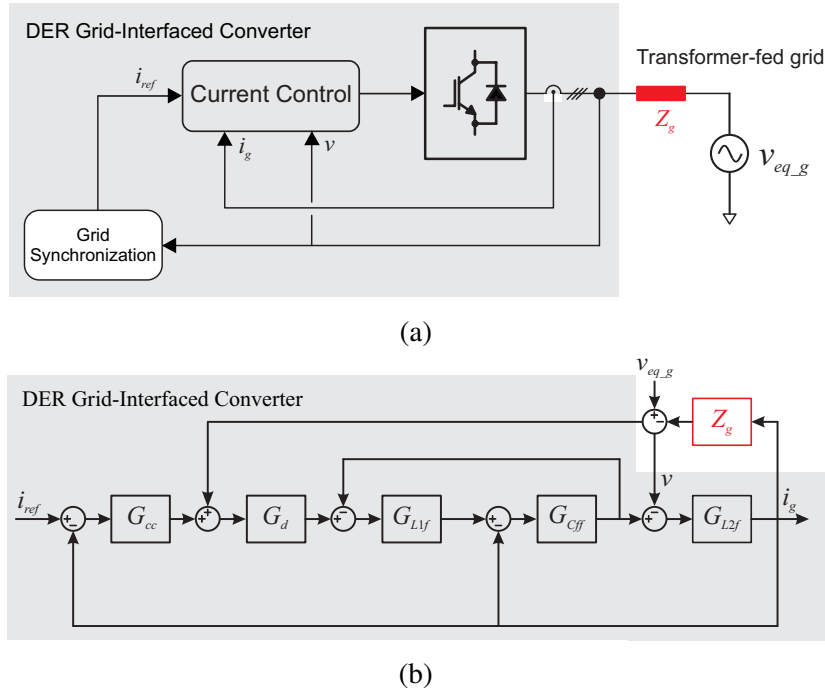


Figure 5.2: Grid integration of a DER inverter in a traditional transformer-fed grid: (a) system configuration, and (b) schematic diagram of a current-controlled grid inverter.

converters have been proposed in literature, aiming at better adapting to various grid conditions. The mathematical expressions of the interaction between the DER impedance and the grid impedance was firstly presented in [64], giving clear guidelines of inverter impedance shaping in certain frequency range. Further work pointed out that by using active/passive damping methods [65], the grid inverter impedance can be optimized, largely avoiding instability. Moreover, adaptive control is another strong candidate to shape online the inverter impedance based on the real conditions of the grid impedance. For example, in [66], an adaptive control strategy based on online grid impedance measurement is able to improve the system stability and adapt to variable feeder impedance. The passivity-based control of the grid inverters is another promising way to evaluate the system stability and offer general guidelines to properly shape the inverter impedance [70, 71].

5.2.2 Stability Analysis of a ST-fed Grid

Since the main purpose is to study the stability issue of LV grid, the other two stages of the ST are not taken into account thanks to the decoupling characteristic. To avoid instability caused by the control interactions, the optimum voltage control strategy proposed in Chapter 4 is used for the ST LV converter. To simplify the analysis and control design, the LV dc-link voltage is assumed to be constant.

In Chapter 4, it is found that the combination of the MFF and the LC multiloop control strategy is the optimal solution for the ST-fed grid. As a result, a multiloop voltage control strategy with the MFF and the LC (as shown in Fig. 5.4) is employed for the following

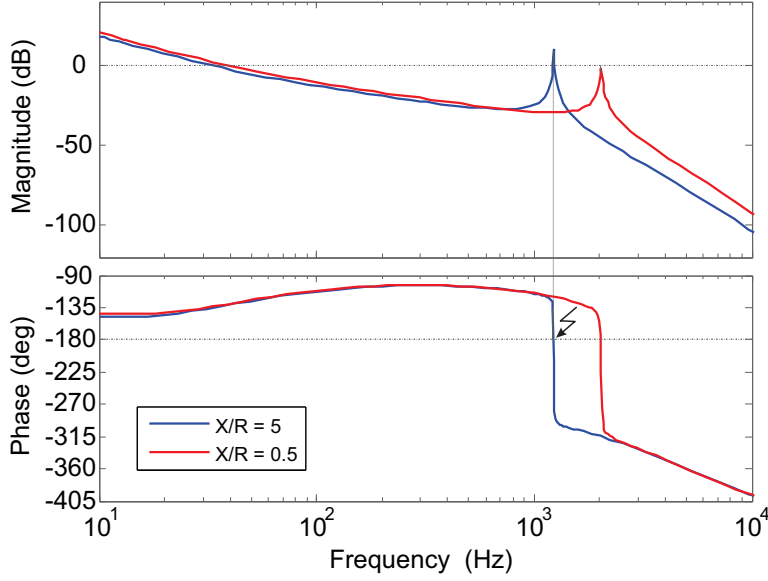


Figure 5.3: Open-loop bode diagrams for DER inverter connected to a grid with different grid impedance.

analysis, in which an LC -type filter is utilized as the output filter, L_f and C_f are the inductance and the capacitance of the LC filter, G_v and $G_{in,v}$ are the transfer functions of the voltage outer loop and the current inner loop controllers. Here, PI controllers are used for both loops. To consider the effects of the LV grid, the equivalent admittance of the LV grid Y_{eq} has been coupled in the closed-loop block diagram. Considering the coupling effect of Y_{eq} , the open-loop transfer function of ST LV converter can be obtained based on its one-line diagram:

$$G_{op}(s) = \frac{G_d G_{o,v} G_{i,i}}{L_f C_f s^2 + (L_f Y_{eq} + G_d G_{i,i} C_f) s + 1 - G_d} \quad (5.2)$$

where $G_{o,v}$ and $G_{i,i}$ are the transfer functions of the voltage outer-loop controller and the current inner-loop controller.

To facilitate the analysis in the following, Y_{eq} is split into three parts: the equivalent admittance of grid-converter-based DERs $Y_{eq,DER}$, the equivalent admittance of grid-converter-based active loads $Y_{eq,AL}$, and the equivalent admittance of passive loads $Y_{eq,PL}$. If a Norton model is taken into account, the equivalent current source of the DER would be opposite to that of the active load, while the equivalent admittances of both devices would be identical, if same control and system parameters are used. Based on the impedance-based modeling theory [55], the equivalent admittance of the grid converter with the considered current control can be obtained by

$$\begin{aligned} Y_{eq,DER}(s) &= Y_{eq,AL}(s) = \frac{i_g(s)}{v(s)} \\ &= \frac{L_{f1} C_{ff} s^2 + R_d C_{ff} s + 1}{L_{f1} L_{f2} C_{ff} s^3 + R_d C_{ff} (L_{f1} + L_{f2}) s^2 + (L_{f1} + L_{f2} + G_d G_{cc} R_d C_{ff}) s + G_d G_{cc}}. \end{aligned} \quad (5.3)$$

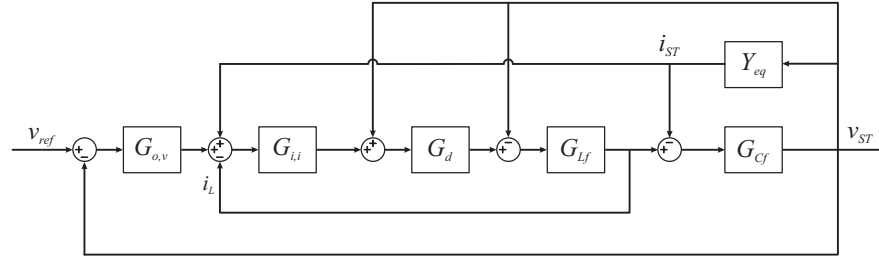


Figure 5.4: Schematic diagram of voltage control of the ST LV converter.

Table 5.1: System Parameters

Symbol	Quantity	Value
L_f	filter inductance of ST	5.03 mH
C_f	filter capacitance of ST	10 μ F
L_{f1}	inverter-side filter inductance of grid converter	5.03 mH
C_{ff}	filter capacitance of grid converter	10 μ F
L_{f2}	grid-side filter inductance of grid converter	0.5 mH
R_d	damping resistor of grid converter	2 Ω
$Y_{eq,PL}$	equivalent admittance of passive load	0.179 - j0.059 S
$k_{p,o}$	proportional gain of ST outer loop	1.25
$k_{i,o}$	integral gain of ST outer loop	10
$k_{p,i}$	proportional gain of ST inner loop	2.25
k_{pc}	proportional gain of current control of grid converter	15
k_{ic}	integral gain of current control of grid converter	50

To investigate the stability issues regarding the integration of grid converters, two scenarios are studied in this section: in the first case study, a heavy passive load and 10 grid-converter-based devices are connected to the PCC, and in the second case study, a light passive load and 10 grid-converter-based devices are connected to the PCC. The system parameters used in the stability analysis are listed in Table 5.1. For the sake of simplicity, the control and system parameters of all the grid-converter-based devices are identical. The equivalent admittance of the heavy passive load equals to $Y_{eq,PL}$ in Table 5.1 and the equivalent admittance of the light one is 10 % of $Y_{eq,PL}$.

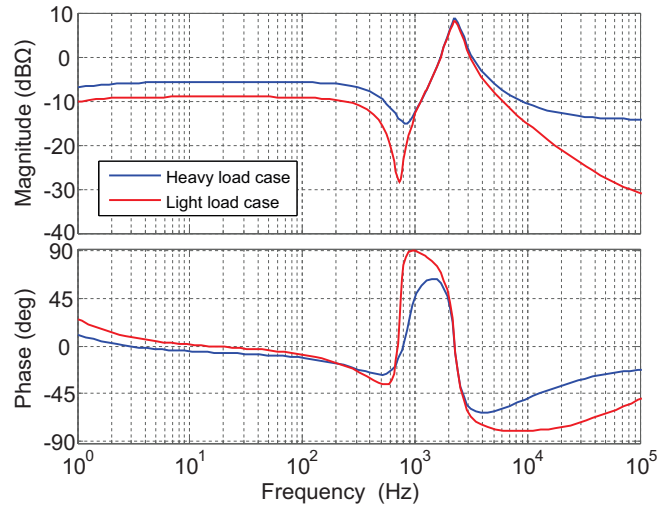
With the consideration of both load and grid converters, the profiles of Y_{eq} of both scenarios are shown in Fig. 5.5a. It can be seen that one positive and one antiresonance peaks have been introduced by the grid converters and the negative resonance peak can be damped by increasing the passive load nearby (heavy load case). Substituting Y_{eq} to (5.2), the open-loop transfer function of ST LV control considering the effects of grid-converter-based devices as well as passive loads can be obtained and the open-loop Bode diagrams (red curves) are shown in Fig. 5.5b and Fig. 5.5c for the two different scenarios. In both Bode diagrams, the open-loop Bode diagrams of the voltage control without grid converters or passive loads connection are shown by the blue curves for comparison. From the open-loop Bode diagrams,

it is seen that Y_{eq} introduces two resonances to the open-loop Bode diagrams of the voltage control considering grid converters. The antiresonance of Y_{eq} becomes a resonance in the low-order harmonic frequency range (e.g., several hundreds hertz), while the resonance of Y_{eq} becomes an antiresonance in the medium frequency range (e.g., several thousands hertz). From the point of view of voltage control, the resonance in the medium frequency range introduced by the grid-converter-based devices is not critical due to its negative magnitudes. However, for the one in the low-order harmonic frequency range, as the magnitude could be positive (e.g., Fig. 5.5c, light load case), the instability would occur because the phase is dramatically changed by the introduced resonance. Seen in Fig. 5.5c, a -180° phase crossing occurs at the neighborhood of the resonant frequency where the magnitude is positive, indicating the system is unstable. Since the critical point appears in the range of low-order harmonic frequencies, the unstable behaviors would be represented by oscillation and low-order harmonic distortion.

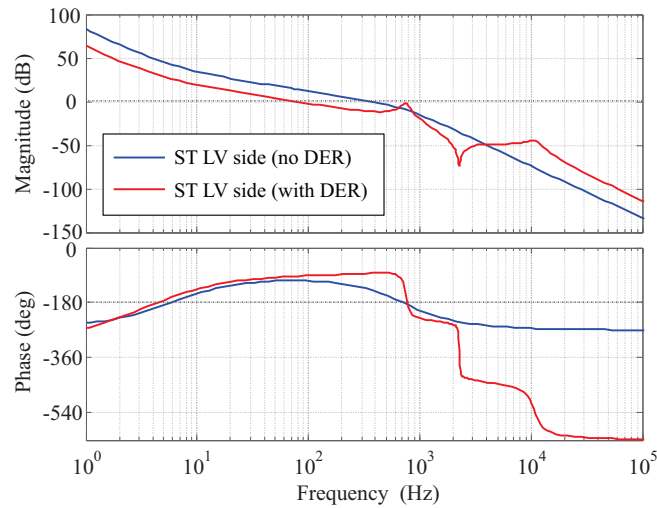
From Fig. 5.5b, it can be observed that the stability of the ST LV converter is mainly determined by the voltage control bandwidth under heavy passive load condition. On the other hand, seen from Fig. 5.5c, the stability of the ST LV converter is affected by the low-order harmonic frequency resonance introduced by grid-converter-based devices during light passive load condition. When increasing the penetration of grid converters, it is known that the magnitude of $Y_{eq,DER}/Y_{eq,AL}$ as well as Y_{eq} increases. Under this circumstance, it can be expected that the bandwidth of ST voltage control considering the effects of Y_{eq} will reduce under the heavy passive load condition, which leads to the decreasing of the phase margin. Under the light passive load condition, since the negative resonance peak at low-order harmonic frequency increases, it results in a lower positive resonance peak of the ST voltage control, especially when the resonance peak reduces below 0 dB, it is interesting to see that the phase margin would turn from negative to positive, namely, the phase margin increases when increasing the connected grid converters under light passive load condition.

To better demonstrate the phenomena, the root loci of the ST LV converter and its control when grid converters increases from 1 % to 100 % of the overall hosting capacity, are shown in Fig. 5.6. In Fig. 5.6a, the heavy passive load case is studied and it can be seen that two dominant poles are gradually moving towards the imaginary axis when increasing the grid converters. The light passive load case is studied and its root locus is shown in Fig. 5.6b and the zoomed figure of its low-frequency range is presented on the right side. It can be seen that the worst case happens when only one grid converter is connected to the grid, where the a pair of conjugate poles locate at the right half plane. By increasing grid converters, the two dominant poles shift from the right half plane to the left half plane, indicating the overall system becomes stable.

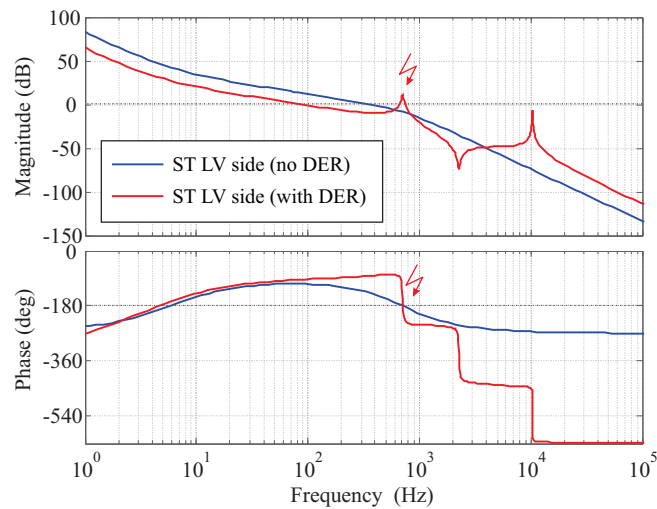
Within the context, the critical case happens when passive loads and few grid converters connect to the grid. To solve the potential stability issue, an adaptive voltage control including stabilization method and resonance identification will be proposed and designed in the followings.



(a)



(b)



(c)

Figure 5.5: Open-loop bode diagram of the LV ST-fed microgrid and load profiles: (a) load profiles, (b) open-loop bode diagram of ST LV control considering grid-connected DERs and heavy load, and (c) open-loop bode diagram of ST LV control considering grid-connected DERs and light load.

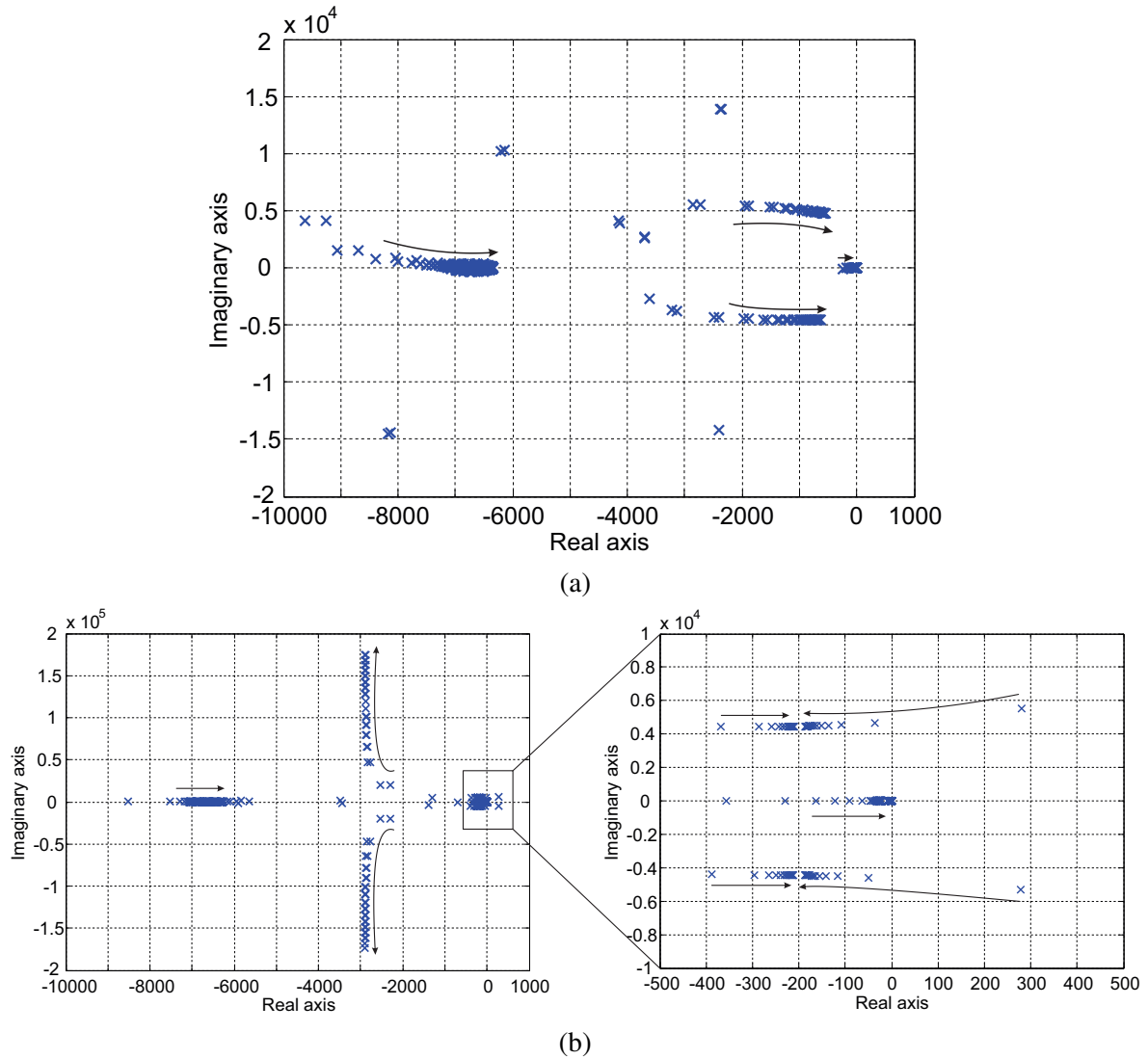


Figure 5.6: Root loci of the ST LV ST-fed microgrid with different load/DER connection: (a) heavy load case and (b) light load case.

5.3 Grid Impedance Reshaping Capability

One distinguished feature of ST is to reshape its output impedance and therefore accordingly modify the equivalent impedance of the ST-fed grid. As soon as the stability issues are detected, the ST impedance will be reshaped by means of voltage control, while the grid impedance Z_g are being changed as well. According to (5.1), the changing of Z_g leads to the alteration of stability margin of the grid-converter-based devices, which in fact offers a possibility to stabilize the DER inverters connected to the grid.

Filter-based active damping is usually used to stabilize single grid converter with *LCL*-type filter [72]. It can reshape the converter output impedance within certain frequency range and up to the Nyquist frequency. In this regard, the filter-based active damping methods are considered for the ST LV converter, aiming at adapting the ST output impedance in certain frequency band and therefore addressing the above-mentioned resonance issues in LV grid.

From the analysis of Chapter 5.2, it is known that the stability issues are subject to low-order

harmonics. To identify the issues, a discrete Fourier transform (DFT) can be adopted and easily implemented into the voltage control shown in Fig. 5.7. In case the harmonic contents of the load current exceed the threshold i_h , the proposed active damping methods will be switched on. The detailed schematics of active damping methods are given and discussed in the following.

5.3.1 Filter-based Active Damping

From the Bode diagrams of Fig. 5.5, the critical point appears in the low-order harmonic range, which leads to harmonic instability. A practical technique to address the resonance- or harmonic-related stability issues is to use the filter-based active damping methods [72]. Compared to the multiloop-based active damping [34], the filter-based methods preserve the closed-loop bandwidth so that the control performance can be maintained. With these considerations, low-pass filter (LPF) and lead element filter (LEF)-based active damping methods are proposed and designed in the following scenarios. Both methods can damp the resonance peak and modify the magnitude and phase of certain frequency band so that they are able to mitigate the critical points shown in Fig. 5.5c. In addition, considering robustness, LPF and LEF are not sensitive to the variation of resonant frequency and therefore they are tolerant to the mismatch between the actual and the measured resonant frequency in practical case. To well tune the filter parameters, an estimator of the resonant frequency of the LV grid by means of frequency sweeping (e.g. [36, 23]) is needed for ST. As shown in Fig. 5.7a and Fig. 5.7b, the ST LV side converter is able to excite the resonance of LV grid by generating harmonic voltage perturbations within all frequency range. The detected resonant frequency is adopted by the LPF and the LEF for the parameters tuning.

A LPF attenuates the magnitude and introduces a phase delay in a frequency band above its cutoff frequency. These two features can be beneficial to shape the ST equivalent impedance in the band around the resonant frequencies of ST converter and grid converter. Fig. 5.7a shows the schematic diagram of the ST voltage control with the LPF-based active damping. Once the harmonic stability or the resonance is detected by the DFT, namely, the harmonic contents of i_{oh} exceeds the threshold at the interested frequencies, the measured voltage feedforward with a LPF will be implemented. Based on the schematic diagram, the ST equivalent impedance is given by

$$Z_{eqST,LPF}(s) = \frac{Z_{cff}(s)}{Z_{cff}(s)Y_{Lff}(s)[1 + G_d(s)(G_{o,v}(s) - G_{LPF}(s))] + 1} \quad (5.4)$$

and the open-loop transfer function of the ST LV converter with the effects of the LV grid can be written by

$$G_{op,LPF}(s) = \frac{G_d G_{o,v} G_{i,i}}{L_f C_f s^2 + (L_f Y_{eq} + G_d G_{i,i} C_f) s + 1 - G_d G_{LPF}}. \quad (5.5)$$

and the transfer function as well as the Bode diagram (show in Fig. 5.8a) of the overall system including both ST LV converter and grid converter can be obtained by combining (5.3) and

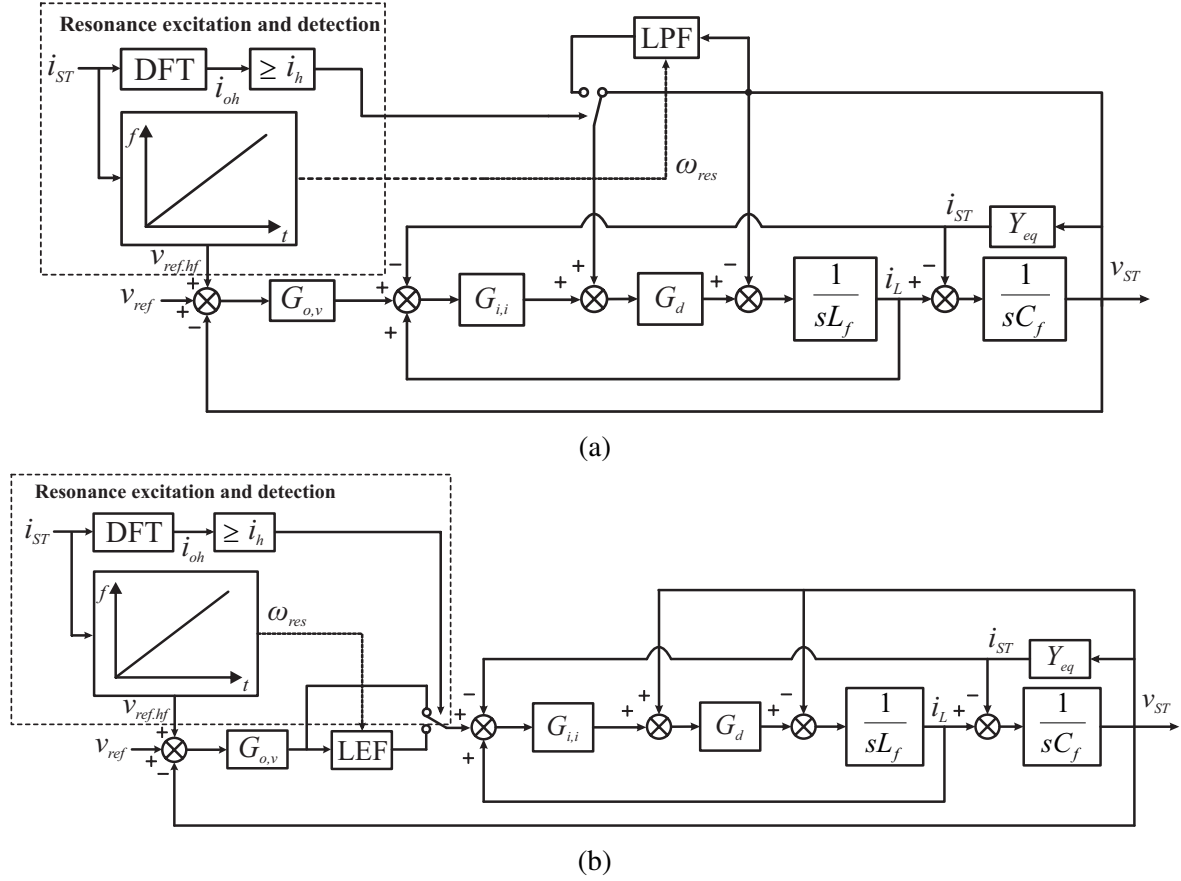


Figure 5.7: Schematic Diagram of the ST voltage control utilizes different active damping methods: (a) low-pass filter-based active damping and (b) lead element filter-based active damping.

(5.5). Here, a second-order LPF is adopted, the transfer function of which is given by

$$G_{LPF}(s) = \frac{\omega_c^2}{s^2 + 2D_{LPF}\omega_c s + \omega_c^2} \quad (5.6)$$

where ω_c is the cutoff frequency and $D_{LPF} = 1/\sqrt{2}$ is used in the study. Assuming the resonant frequency of the LV grid ω_{res} is known, $\omega_c = 0.75\omega_{res}$ is chosen in this case. It is observed in Fig. 5.8a that the LPF-based active damping is able to introduce a phase delay in the low-frequency range and attenuate the resonance peak of the overall system (the peak at 3350 Hz). As a result, the -180° crossing in the low-frequency range is shifted outside the frequency band with a magnitude above 0 dB and the resonance peak is damped with a negative magnitude (blue curve). A stable operation is achieved in this case (minimum phase margin is 63.5°). The impedance properties of the ST LV side converter are shown in Fig. 5.9a, in which the original properties are well maintained within the entire Nyquist frequency. Thus, the LPF-based active damping method can hold the characteristics of the original ST voltage control system, and this is especially beneficial for the fundamental voltage control and low-order harmonic elimination.

A LEF introduces a phase lead in a certain frequency band. By using the LEF-based active damping, the impedance properties of ST in the phase-lead-compensation frequency band

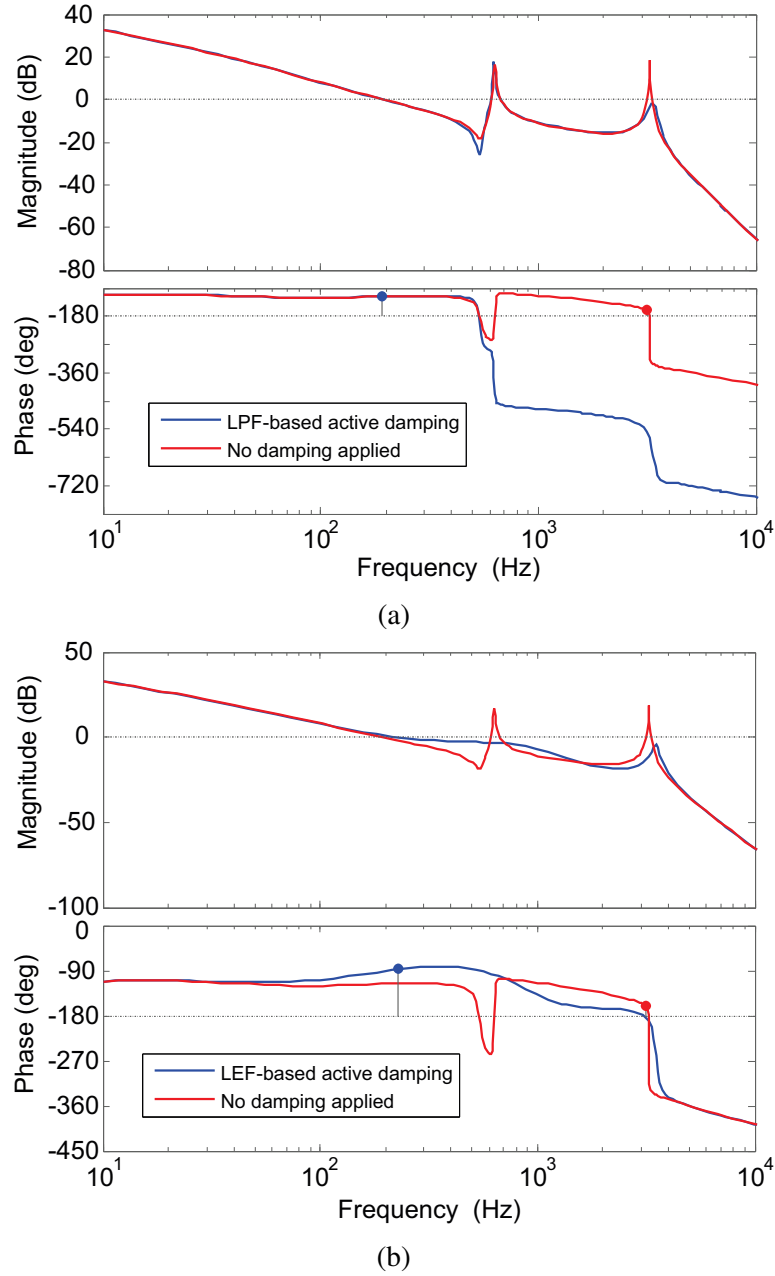


Figure 5.8: Bode diagrams of the grid-connected inverter of DER considering the effects of the grid impedance (ST output impedance): (a) a LPF-based active damping is applied to the ST and (b) a LEF-based active damping is applied to the ST.

can be reshaped. The schematic diagram of the ST voltage control with the LEF-based active damping is depicted in Fig. 5.7b. As soon as the harmonic stability or the resonance is detected, a LEF will be plugged into the voltage control forward channel. Based on Fig. 5.7b, the equivalent ST output impedance is given by

$$Z_{eqST,LEF}(s) = \frac{Z_{cff}(s)}{Z_{cff}(s)Y_{Lff}(s)(1 + G_d(s)G_{o,v}(s)G_{LEF}(s) - G_d) + 1} \quad (5.7)$$

and the open-loop transfer function of the ST LV converter with the effects of the LV grid

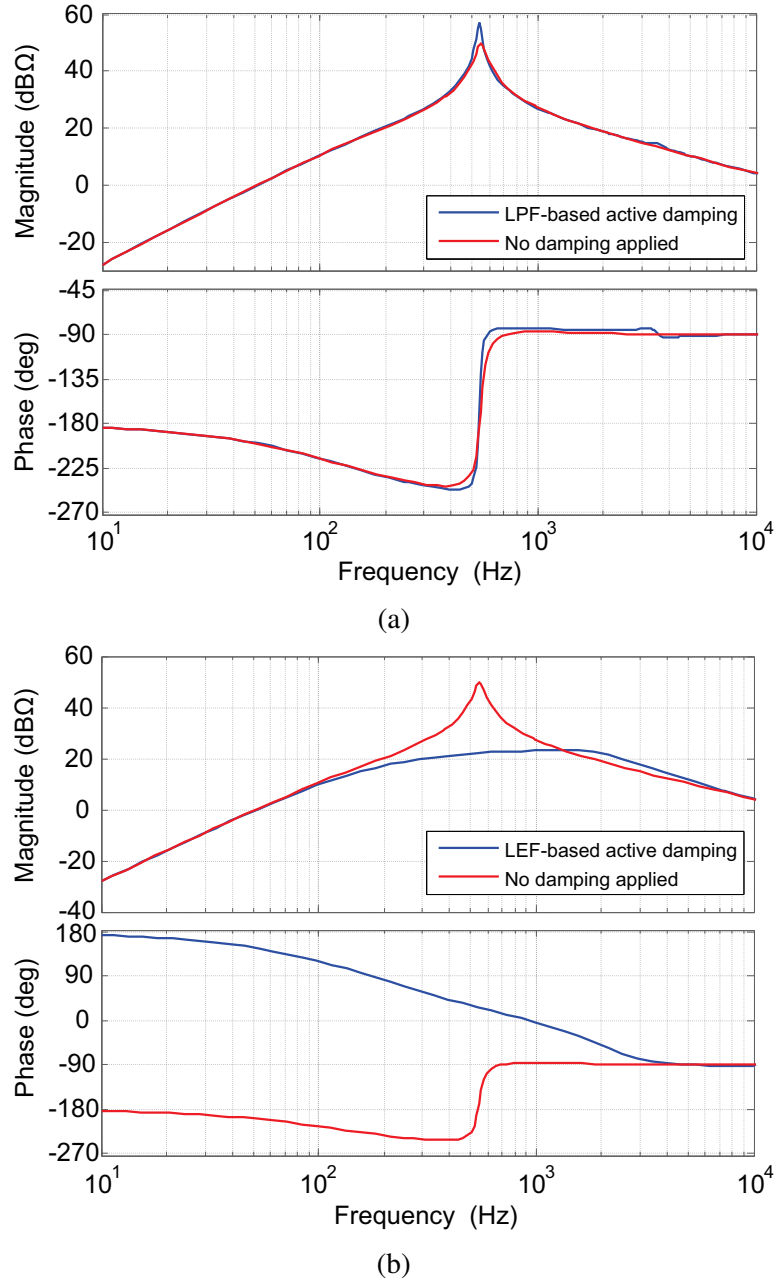


Figure 5.9: Properties of the ST output impedance when: (a) a LPF-based active damping is applied to the ST and (b) a LEF-based active damping is applied to the ST.

can be written by

$$G_{Op,LEF}(s) = \frac{G_d G_{o,v} G_{LEF} G_{i,i}}{L_f C_f s^2 + (L_f Y_{eq} + G_d G_{i,i} C_f) s + 1 - G_d}. \quad (5.8)$$

The transfer function of the overall system can be obtained by substituting (5.3) into (5.8), and its Bode diagram is shown in Fig. 5.8b. Here, the transfer function of LEF is given by

$$G_{LEF}(s) = \frac{1/\omega_f s + 1}{\alpha/\omega_f s + 1} \quad (5.9)$$

where ω_f and α determine the phase-lead-compensation frequency band and the phase-

lead-compensation angle, respectively. A relation $\alpha = \tan(\frac{\pi}{4} - \frac{\phi_{max}}{4})$ holds, $\phi_{max} = 30^\circ$. $\omega_f = 0.55\omega_{res}$ is chosen in this case. It can be seen in Fig. 5.8b that the LEF-based active damping changes the phases of the phase-lead-compensation band and damps the resonance peaks. Due to the phase change, it causes the phase response crossing -180° away from the critical frequency range and stabilizes the overall system (minimum phase margin is 87.4°). The impedance properties shown in Fig. 5.9b shows that the LEF-based active damping can damp the resonance of the LV grid and maintain the control characteristics except the phase-lead-compensation band.

5.3.2 Design Criteria

The active damping control is usually adopted to suppress the resonance and improve the stability margin of grid-interfaced converters. Design criteria have been given to achieve these targets [72, 73]. Nevertheless, the active damping methods being implemented in the ST LV inverter aims at a different target. Instead of stabilizing one local grid converter itself, the main purpose is to stabilize all the grid-converter-based devices in the LV grid by means of ST LV converter. As a result, the stability of the LV grid as well as the grid-converter-based devices is the basic criterion. In addition, there are other demands being taken into consideration, for example the bandwidth and control accuracy of the ST. In general, the influence of the active damping on the ST control is another main concern because a stiff ST voltage is the key factor of the ST-fed grid operation. Therefore, the parameters of the active damping (e.g., ω_c and ω_f) are tuned considering two criteria: 1) the parameters are effective enough to stabilize the LV grid as well as the grid-converter-based devices; 2) the original control properties of the ST voltage control in terms of fundamental steady-state error, dynamic performance, and harmonic elimination should fulfill the grid requirements and should not be affected by the "plug-in" active damping methods. To avoid the impacts of other instability factors, a pre-design of the voltage control of the ST LV converter and the current control of the grid converter was carried out, ensuring phase margins between 45° and 60° .

The multiloop voltage control employs the LC as the current inner loop scheme. The choice of the inner-loop gain is a typical tradeoff between the stability requirement of LV grid and the control accuracy of ST LV converter. With the increasing of the inner-loop gain, the equivalent impedance of the low-frequency range increases accordingly, which will amplify the disturbances and harmonics [34]. The pole-zero map of the overall system with the effects of grid-converter-based devices is shown in Fig. 5.10a, where the inner-loop gain increases from 0.1 p.u. to 7.5 p.u.. It can be seen that a pair of unstable poles are moved from the right-half plane to the left, proofing that the increasing of the inner-loop gain can improve the stability of the overall system. Nevertheless, if one observes the pole-zero map of the ST LV converter itself (shown in Fig. 5.10b), it can be seen that the control bandwidth increases while the damping ratio decreases by increasing inner-loop gain. Therefore, it can be concluded that a higher inner-loop gain results in a more stable LV grid but compromises the control performance in terms of low-frequency disturbances and harmonics rejection. In a

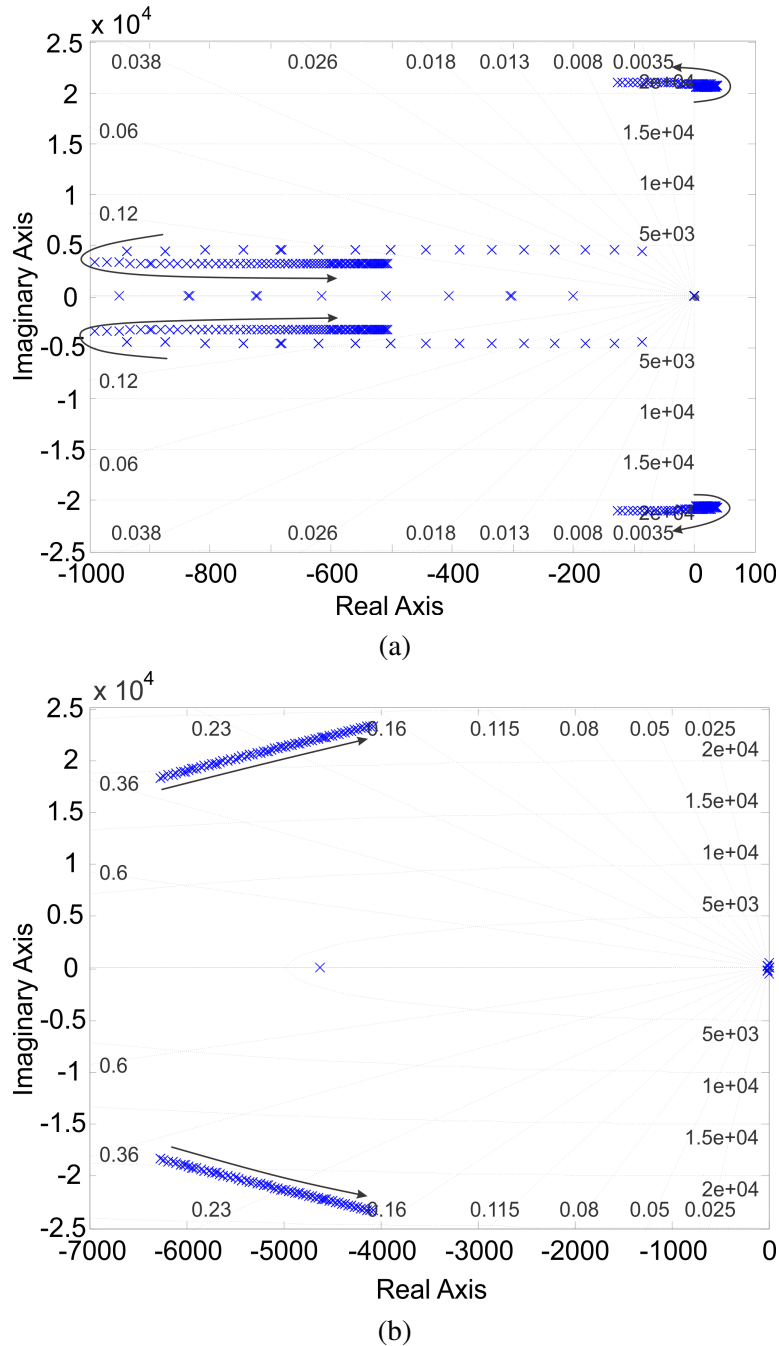


Figure 5.10: Root locus when increasing inner-loop gain of the ST voltage control: (a) overall system including ST LV converter and grid converter and (b) closed-loop ST voltage control.

practical ST-fed grid, the primary consideration for the inner-loop gain is to guarantee good voltage waveform that can meet the requirements of the grid codes so that it should be limited. The stability could be further improved by the filter-based active damping methods.

The LPF-based active damping changes the equivalent ST output impedance in a limited way. Especially in the low-frequency range, both the magnitude and phase response of the impedance remain the same as the one without damping. A pole-zero map of the overall system considering both the ST LV converter and the connected grid converter is presented

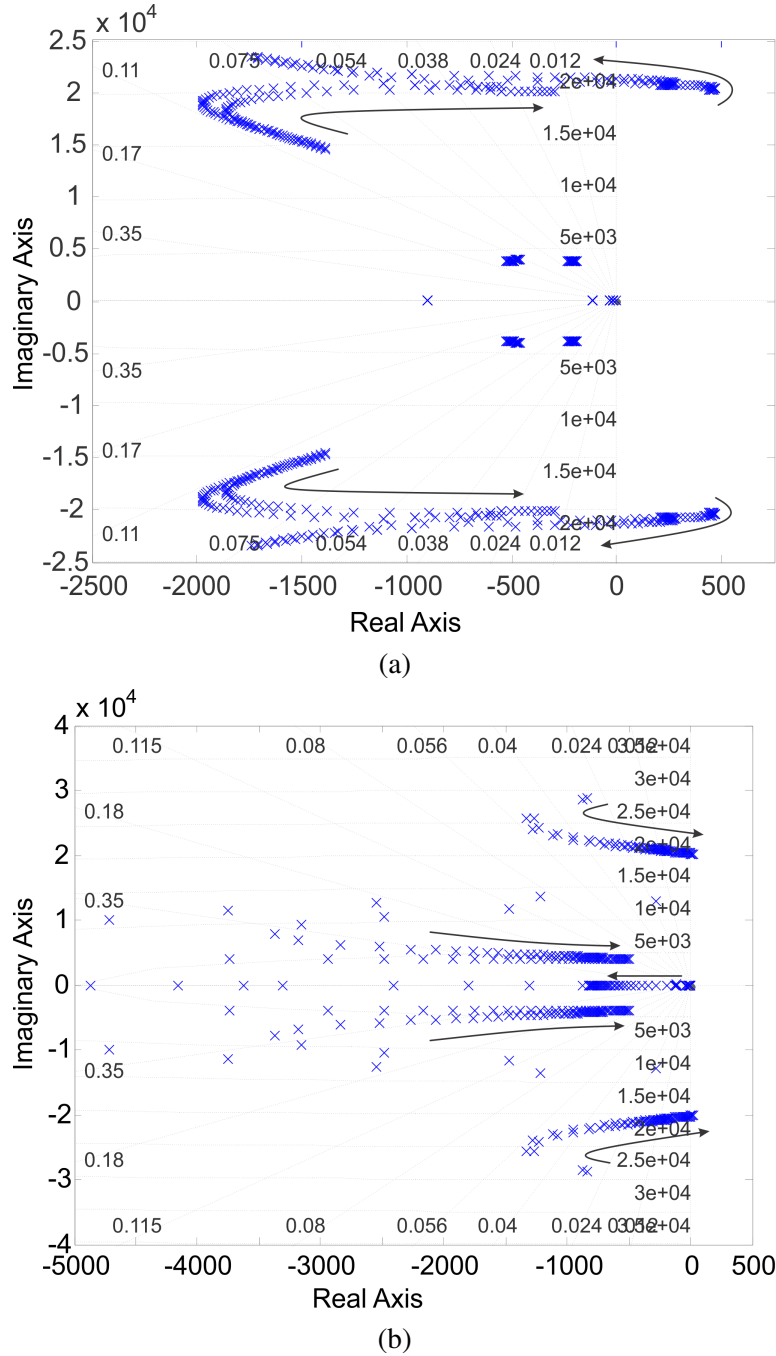
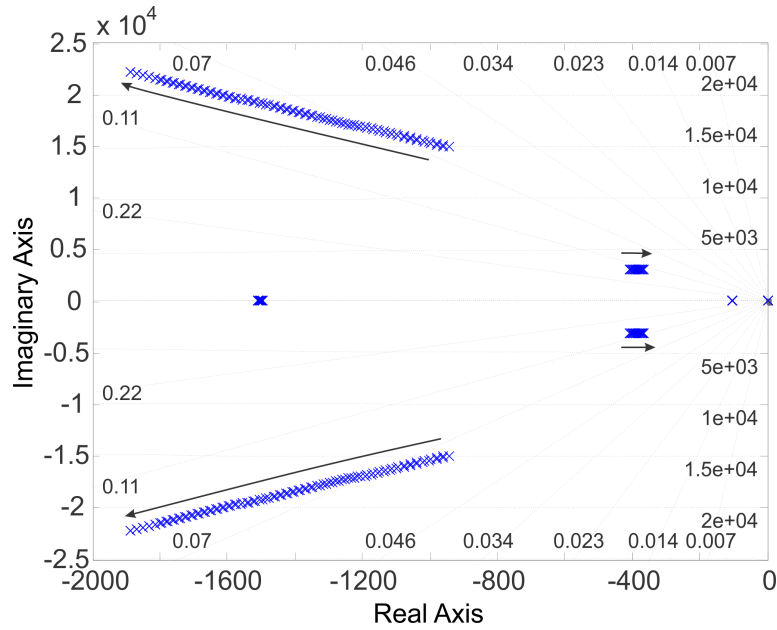
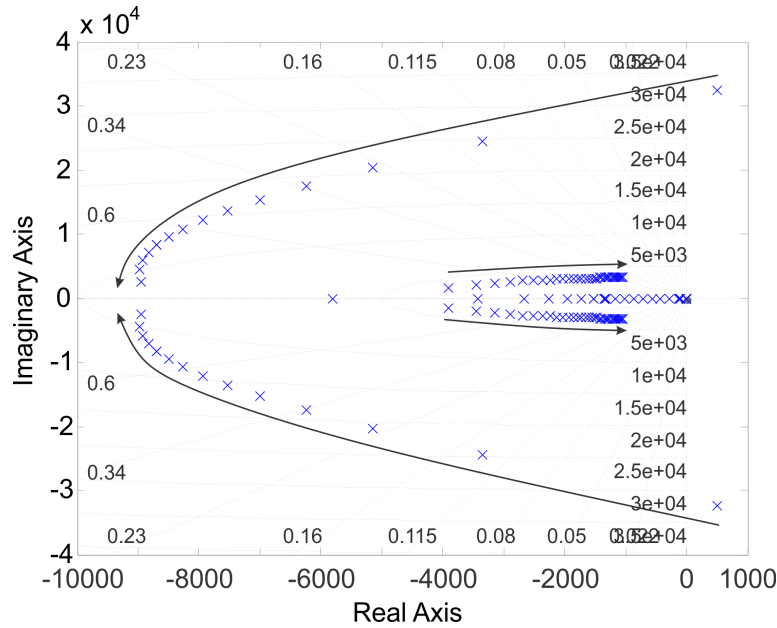


Figure 5.11: Root locus of the overall system when different active damping methods are applied to the ST: (a) low-pass filter-based active damping increasing ω_c and (b) lead element filter-based active damping increasing ω_f .

in Fig. 5.11a, in which the cutoff frequency ω_c changes from $0.65\omega_{res}$ to $0.95\omega_{res}$. It is seen that two pairs of unstable poles move from the right-half plane to the left, while another two pairs of stable poles are shifted towards the imaginary axis, when ω_c increases. From the pole-zero map of the voltage control of the ST LV converter using LPF-based active damping, shown in Fig. 5.12a, it can be seen that the control bandwidth of the ST increases when ω_c increases, indicating a higher ω_c offers the ST better voltage dynamics. In summary, the stability requirement of the LV grid as well as the grid-converter-based devices is the main index for the tuning of ω_c . All the dominant poles of the overall system must be in the left-



(a)



(b)

Figure 5.12: Root locus of the ST voltage control when different active damping methods are applied: (a) low-pass filter-based active damping increasing ω_c and (b) lead element filter-based active damping increasing ω_f .

half plane away from the imaginary axis. From the pole-zero maps, ω_c of $[0.75\omega_{res}, 0.9\omega_{res}]$ is preferred to be the optimal range. The optimal range of the cutoff frequency can be used in conjunction with the resonant frequency obtained from the resonance estimator, enabling the adaptive feature to the variation of LV grid.

The LEF-based active damping changes the magnitude and phase of the equivalent ST output impedance within the phase-lead-compensation frequency band. To mitigate the impact on the low-frequency range (usually up to 750 Hz), the phase-lead-compensation frequency ω_f should be higher than this range. Nevertheless, a higher ω_f could lead to instability of the LV

grid and the connected grid converters, seen from the pole-zero map shown in Fig. 5.11b. In this map, two pairs of poles move towards the imaginary axis till the right-half plane, when ω_f increases from $0.25\omega_{res}$ to $0.5\omega_{res}$. Meanwhile, from the pole-zero map of the voltage control of the ST LV converter using LEF-based active damping which shown in Fig. 5.12b, the control bandwidth, damping factor, and stability margin of the ST voltage control system reduce significantly when ω_f is increasing. With these considerations, provided ω_f is higher than the frequency of interested in the low-frequency range, the lowest ω_f would be expected to provide good ST control performance and stabilization effect. From the pole-zero maps and the requirements of the application, ω_f of $[0.35\omega_{res}, 0.45\omega_{res}]$ is chosen to be the optimal range, and can be used together with the resonant frequency obtained from the resonance estimator.

5.3.3 Resonance Identification and Stability Margin Estimation in a ST-fed Grid

In an actual grid, the profiles of equivalent admittance (including DERs and loads) vary, which could shift resonant frequency. Due to an erroneous frequency, a deviation between ω_f/ω_c of the filter-based active damping and the actual resonant frequency would occur. As seen from the pole-zero map in the previous section, if ω_f/ω_c is not chosen within the optimal range which is related to the resonant frequency, the stability of the overall system and the voltage control performance of the ST LV converter would be compromised. To deal with this problem, a resonance identification method is proposed as presented in Fig. 5.7a and Fig. 5.7b and the detected resonant frequency is utilized for the LEF/LPF parameters online tuning. In this way, a resonant frequency adaptive voltage control strategy can be achieved for the ST-fed LV grid.

Since the main target is to identify the positive resonance in the low-order harmonic frequency, a mono-frequency excitation ranging from 150 Hz to 1500 Hz is implemented together with the voltage control. Taking Fig. 5.7b as an example, the mono-frequency voltage signal $v_{ref.hf}$ at corresponding frequency f_n is added to the voltage reference, where f_n is provided by a frequency sweep with required frequency resolution, a fixed signal amplitude V_h is used. In practical operation, the percentage of V_h over nominal voltage must be higher than the overall accuracy of the sensors so that the generated voltage would not be overwhelmed by the noise and measurement errors. Meanwhile, the upper limit of V_h must be marginally lower than the harmonic limitations at different harmonic frequencies as recommended by the grid codes. In our test, LEM LV 25-P voltage sensors are employed for the ST and the overall accuracy of the sensors is $\pm 0.8\%$. With these considerations, the range of $[3\%, 4.5\%]$ nominal voltage is recommended for V_h during the resonance identification. The harmonic current content of i_{ST} excited by the harmonic voltage can then be extracted by means of DFT or a notch filter, using the fundamental frequency as its notch frequency. Since the harmonic current at resonant frequency is usually far higher than the measurement error, the impacts of noise or error are not as critical as that of voltage measurement and the harmonic content can be accurately detected. As soon as the rms value of the harmonic

current content increases dramatically and exceeds the threshold i_h , it indicates that the harmonic current has been excited by the positive resonance. The frequency sweep will stop and the value of f_n will be considered as the resonant frequency for the filter parameters tuning. The frequency sweep procedure will be repeatedly carried on in order to obtain the grid characteristics in real time.

During ST-fed grid startup, the power from the substation is firstly used to energize some feeders with a majority of passive loads. In the very beginning, the ST LV side voltage would not reach the nominal value (e.g., 230 V) but a relative low value for instance below 180 V so that all the grid-converter-based DERs cannot connect to the grid. The grid voltage will increase gradually to the nominal value for a while and meanwhile the frequency sweep will be carried out to obtain the grid characteristics and provide initial parameters to the phase compensation. Key distributed sources and active loads including grid-converter-based DERs and EV charging stations will connect to the grid when it is stable. Rest of the DERs will connect to the grid in batches and the filter parameters will be online modified depending on the real-time grid characteristics.

In addition to the resonant frequency, the real time stability margin is also important to the stabilization and useful to the grid operation. An example of the LEF-based active damping is given here with the Bode diagrams of the overall voltage control with/without the LEF as well as different ϕ_{max} are shown in Fig. 5.13. Before the LEF plugged in (green curve), it is seen that the a -180° phase crossing occurs at the resonance and the phase margin is negative (minimum phase margin $PM = -7.8^\circ$). By means of the LEF, the -180° phase crossing no longer appears when the magnitude is positive, and the phase margin turns from negative to positive and keep increasing when ϕ_{max} increases. When ϕ_{max} is 25° , the minimum phase margin is 12.5° ; when ϕ_{max} is 35° , the minimum phase margin reaches 29.7° . Obviously, to obtain the stability margin of the LV grid as one did in theoretical analysis would be very useful, not only benefits the stable operation of the grid but also facilitates the parameter design of the stabilization methods. This can be achieved with the aid of the grid characteristics estimation in frequency domain.

During the resonance identification, Y_{eq} in time-domain can be easily obtained based on the measured voltage/current. To well estimate the stability condition, the stability analysis given in Chapter 5.2 needs to be carried out, and Y_{eq} in frequency-domain should be translated by the obtained data. One intuitive way is to use the vector fitting (VF) method, which is one of the most popular tools for identification of linear systems in the frequency domain [74]. The main idea is to approximate a frequency response $v_f(s)$ with a rational function:

$$v_f(s) = \sum_{m=1}^N \frac{r_m}{s - a_m} + d + es \quad (5.10)$$

where N is the approximation order that determines the accuracy, d and e are optional for the rational function. The poles of $v_f(s)$ can be identified by solving the linear problem in the

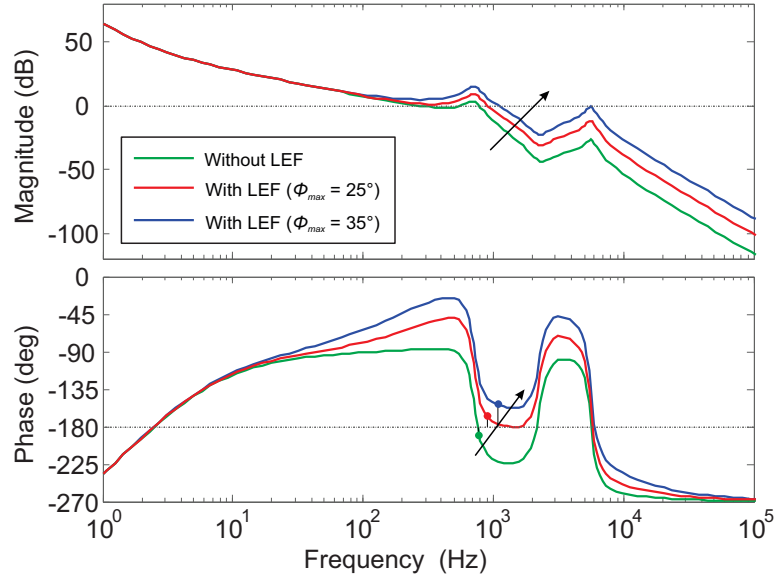


Figure 5.13: Open-loop bode plots of ST LV control with lead-element filter using different ϕ_{max} .

least-square way as followings

$$\begin{aligned}
 v_f(s)\sigma(s) &= p(s) \\
 \sigma(s) &= \sum_{m=1}^N \frac{\tilde{r}_m}{s - q_m} + 1 \\
 p(s) &= \sum_{m=1}^N \frac{r_m}{s - q_m} + d + es
 \end{aligned} \tag{5.11}$$

where $\sigma(s)$ and $p(s)$ are a scalar and a vector, respectively, and $\{q_m\}$ is a set of initial poles. By applying an iterative procedure, $\{q_m\}$ are being replaced by the new poles $\{a_m\}$. After that, the residues of (5.10) can be calculated by solving the linear problem with known poles, which leads to the approximated transfer function.

An example is given to show the effectiveness of the grid characteristics estimation. The comparison between the actual data and the estimated frequency response which uses the VF method is presented in Fig. 5.14. Here, the frequency response of the data (blue curves) is obtained from an actual German grid through mono-frequency sweeping, while the transfer function (TF) of the grid impedance is estimated based on the data by using the VF method and its frequency response is shown by the red dotted curves. To obtain a high precision, the approximated order is 200. It can be seen that the magnitude and phase curves are almost overlapping, showing that the accuracy of the estimated transfer function is high enough to demonstrate the features of the original data in frequency domain.

Furthermore, the grid-converter-based DERs and loads can be either three-phase systems (e.g. wind power system) or single-phase systems (e.g. photovoltaic) in an actual grid. As a result, unbalanced power generation and loading conditions have to be taken into account. Though unbalanced loads and DERs introduce unbalanced current, the bandwidth of the

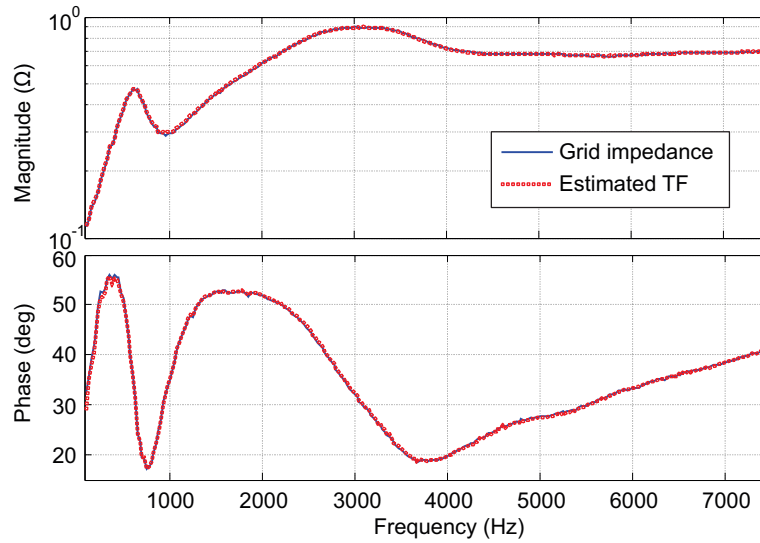


Figure 5.14: Comparisons between actual data from a German grid and the estimated frequency response by using the VF.

ST voltage controller is normally far beyond the fundamental frequency and therefore the ST LV converter can maintain symmetric voltage waveforms. Nevertheless, the equivalent admittance Y_{eq} used in the open-loop block diagram (shown in Fig. 5.4) would be different from one phase to another, which might lead to dissimilar stability conditions on different phases. For instance, the open-loop characteristics of one phase could be quite flat (no obvious resonance) due to relatively heavy passive loads, whereas other phases could have the stability issues because of high penetration of grid converters and light passive loads. Thanks to the three-phase four wire system, the three-phase voltage control subsystems can be decoupled regarding control design as well as stability analysis, which allows different phase-lead compensations to be implemented on every phases through the LEFs. Indeed, it would complicate the implementation and further increase the computational burdens. The design criteria can be easily extended from single-phase analysis (for symmetric system) to three-phase analysis (for asymmetric system).

5.4 Robustness and Sensitivity Analysis

In previous sections, the control and system parameters of grid-converter-based devices are assumed to be identical for simplicity. Nevertheless, in an actual grid, the parameters would be different even from the same manufacturer. In this regard, the sensitivity of the proposed control strategy to the variation of grid converters' parameters (including *LCL* filter parameters, current control parameters, and number of grid converters) will be evaluated in the following. Design guidelines for control and system parameters of grid converters can be derived from the sensitivity analysis.

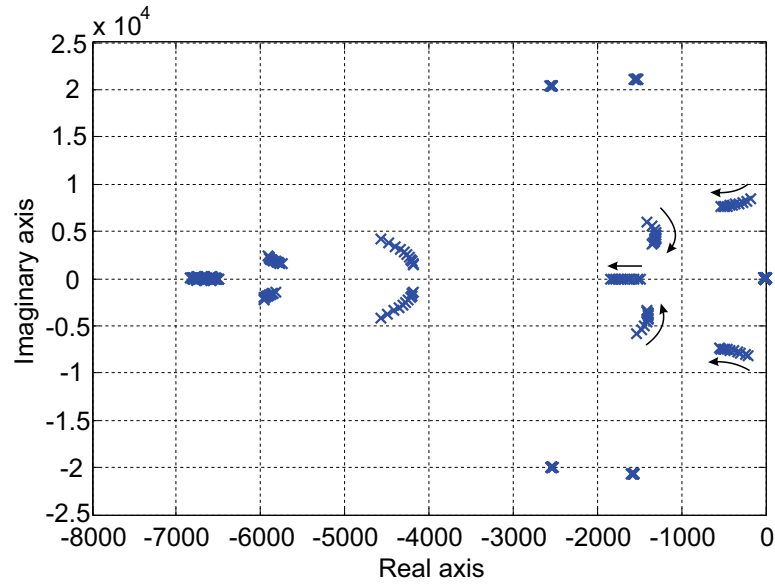
The root loci of the overall system shown in Fig. 5.15 and Fig. 5.16 are used to evaluate the sensitivity of the voltage control with the LEF-based active damping to the variation of grid converters parameters. In the following case studies, a robust voltage control system of ST

is provided with the parameters of $\omega_f = 0.45\omega_{res}$ and $\phi_{max} = 40^\circ$ based on the robust control design section. From Fig. 5.15a to Fig. 5.16a, the variation of the grid converter *LCL* filter parameters has been studied, where the values of those parameters vary from 50 % to 150 % of their nominal values. It is obviously seen that the proposed voltage control strategy is not sensitive to the variation of the converter-side inductance and the filter capacitance. For the variation of the grid-side inductance, though the poles in the medium-frequency range shift within a wide range, the dominant poles remain still. From the stability point of view, the voltage control with the LEF-based active damping is not sensitive to the variation of the grid converter's *LCL* filter.

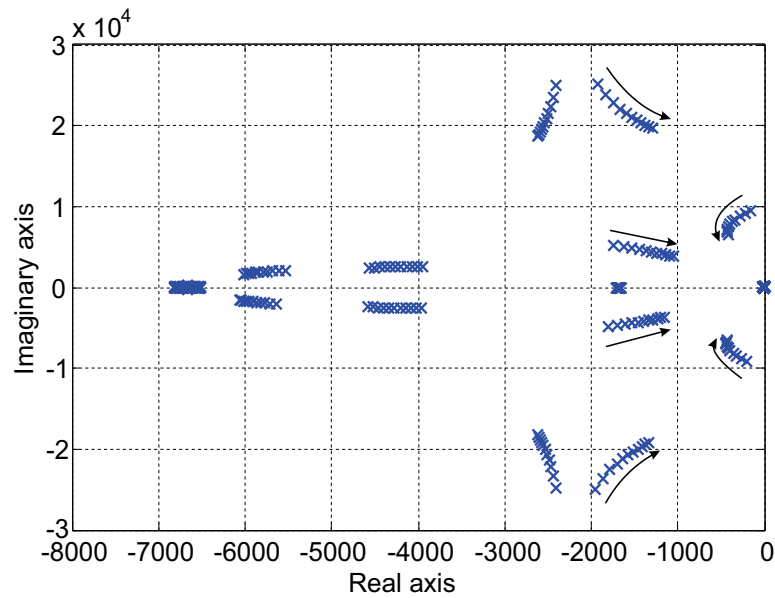
Fig. 5.16b illustrates the root locus of the overall system when the the PI parameter (proportional gain k_{pc}) of current control of grid converter changes from 10 % to 200 % of its nominal value. Obviously, a larger proportional gain of grid converter is likely to incur instability. Under this circumstance, a larger ϕ_{max} could be provided in case of the poles in the medium-frequency range have sufficient phase margin. In Fig. 5.17, the root locus of the overall system with the increasing of grid converters is presented and the penetration level of grid converters increases from 1 % to 100 % of hosting capacity. The area of the dominant poles are zoomed and shown on the right side of the figure. It can be seen that all dominant poles locates at the left half plane and the real pole are moving towards the imaginary axis with the increasing of grid converters. Compared to the root locus of Fig. 5.6b, it is shown that the stability margin of the overall system has been largely improved by the LEF-based active damping method.

The sensitivity of the voltage control with the LPF-based active damping to the variation of grid converters parameters is studied as well. The root loci of the overall system are presented in Fig. 5.18 and Fig. 5.19. In the case studies, a robust voltage control system with the LPF is designed with the parameters of $\omega_c = 0.9\omega_{res}$ based on the robust control design section. From Fig. 5.18a to Fig. 5.19a, the variation of the grid converter *LCL* filter parameters has been carried out, where the values of those parameters vary from 50 % to 150 % of its nominal value. Different from the case studies of the LEF, the LPF-based active damping is more sensitive to the parameter variations, especially when the converter-side inductance and capacitance of the *LCL* filter are low (i.e., [50 %, 80 %] of their nominal values), a pair of conjugate poles would locate on the right half plane. From the stability point of view, the voltage control with the LPF-based active damping is not sensitive to the variation of the *LCL* filter above the nominal values and therefore is recommended to be used in a grid with low frequency resonances.

In Fig. 5.19b, the root locus of the overall system with the increasing of grid converters is presented and the penetration level of grid converters increases from 1 % to 100 % of hosting capacity. It can be seen that all dominant poles locates at the left half plane and the real pole are moving towards the imaginary axis with the increasing of grid converters. Similar to the case studies of the LEF, it is shown that the stability margin of the overall system has been largely improved by the LPF-based active damping method compared to the root locus of Fig. 5.6b.



(a)

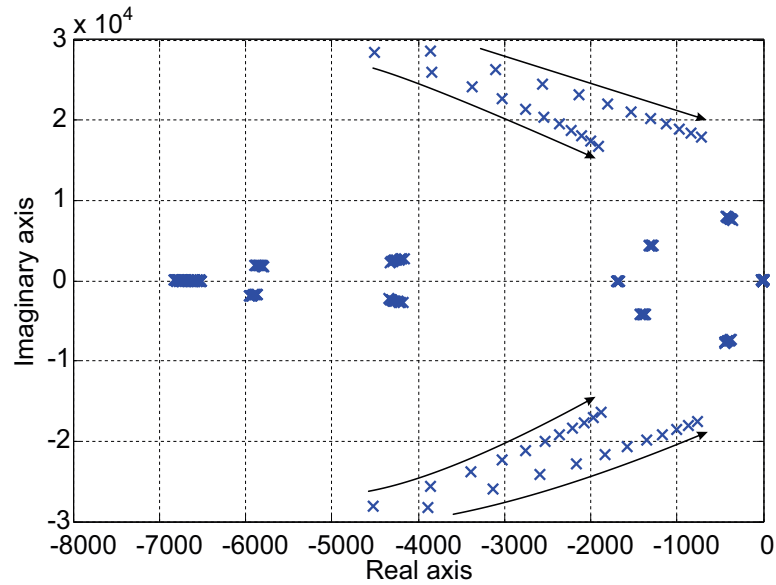


(b)

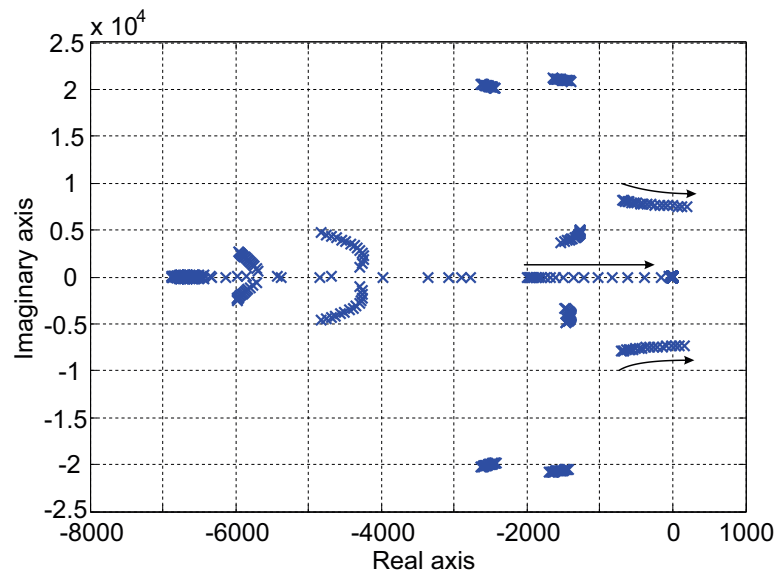
Figure 5.15: Root locus of the ST LV side converter using the LEF-based active damping when varying parameters of connected grid converters: (a) converter-side inductance L_{f1} and (b) filter capacitance C_{ff} .

5.5 Simulation and Experimental Results

To better study the stability issues of a ST-fed grid, a simplified ST-fed power system consisting of two commercial inverters and linear load has been developed in the laboratory (shown in Fig. 6.19). The validity of the proposed active damping methods has been experimentally verified by the setup. Furthermore, a CIGRÉ 18-Bus benchmark grid (shown in Fig. 4.19) has been implemented in a RTDS simulator, with the ST being the voltage supply and two DERs as well as local loads being connected to the LV grid, to show the effectiveness of the proposed methods in an extended distribution grid.



(a)



(b)

Figure 5.16: Root locus of the ST LV side converter using the LEF-based active damping when varying parameters of connected grid converters: (a) grid-side inductance L_{f2} and (b) proportional gain of PI.

5.5.1 Experimental Results

To validate the effectiveness of the proposed methods, a ST-fed grid is tested in the experimental setup. The system configuration of Fig. 5.20 is taken, the current control scheme of Fig. 5.2b and the voltage control with the proposed active damping methods of Fig. 5.4 are implemented in the DER grid converter and the ST LV side converter, respectively. Two Danfoss FC302 inverters are used: one for the ST LV side converter, and the other one for the grid-interfaced converter of DER. A dSPACE 1006 is used to achieve the voltage/current control strategies as well as the proposed stabilization solutions in real-time. The system parameters are listed in Table 5.1. PI controllers are employed for both the current control

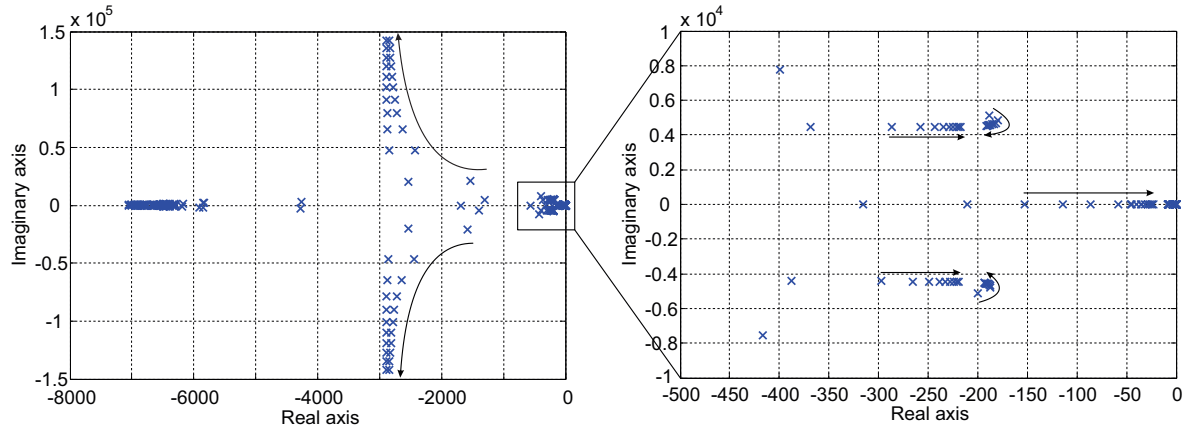


Figure 5.17: Root locus of the ST LV side converter using the LEF-based active damping when varying numbers of connected grid-converter-based devices.

of DER converter and the voltage control of ST LV converter. A predesign of both voltage control and current control are carried out to make sure the stability margins of the DER grid converter (standalone) and the ST LV converter (without DER converter being connected) are between 45° and 60° .

Two case studies are carried out to test the effectiveness of the active damping-based stabilization solutions and the resonance estimation method. Firstly, when the harmonic instability happens, the proposed active damping-based stabilization solutions are plugged in to stabilize the LV grid. From Fig. 5.21a, it is shown that both the ST LV side voltage and the DER output current are unstable and highly distorted at the very beginning. At 0 s, the LPF-based active damping method of Fig. 5.7a is activated in the ST. It can be seen that both the ST voltage and the DER current are effectively stabilized and both waveforms recover their nominal states with good power quality in very short term. The stabilization effect can also be achieved by the LEF-based active damping method of Fig. 5.7b. In Fig. 5.22a, the LEF-based active damping method is activated in the ST at 0 s, both the ST LV side voltage and the DER current are immediately stabilized and quickly recover to their nominal states. The zoomed figures of the harmonic instability condition and the stable condition are shown at the left side and the right side, respectively.

Secondly, the proposed resonance identification method is verified in the laboratory ST-fed grid. Once the overall system is stabilized, the resonance identification is performed to obtain the accurate resonant frequency for parameter tuning and stability margin estimation. The mono-frequency sweeping varies from 150 Hz to 2000 Hz with 50 Hz frequency resolution, and the waterfall FFT plot of the ST voltage is presented in Fig. 5.23a. The highlighted dots can be observed at every 50 Hz from the voltage spectrum. The waterfall FFT plot of the ST output current is presented in Fig. 5.23b, in which the harmonic contents in the low-order harmonic frequency range have been excited and highlighted in the spectrum. The detailed identification procedure of the resonant frequency are shown in Fig. 5.24a. It can be seen that the harmonic content of the ST output current exceeds the threshold at around 400 Hz as well as 450 Hz and then drops drastically, according to the FFT waterfall diagram (shown in Fig. 5.24b). Therefore, the resonant frequency of 425 Hz (average value of 400 Hz and

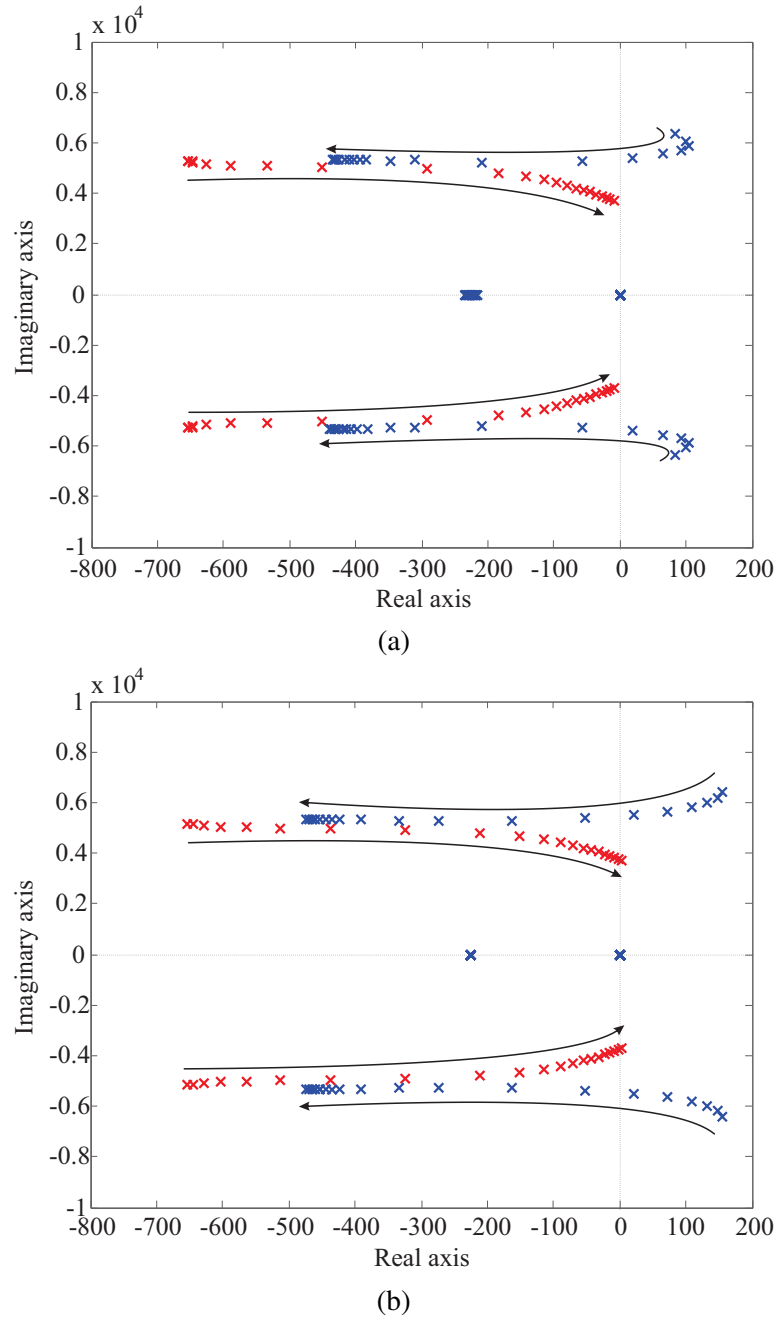
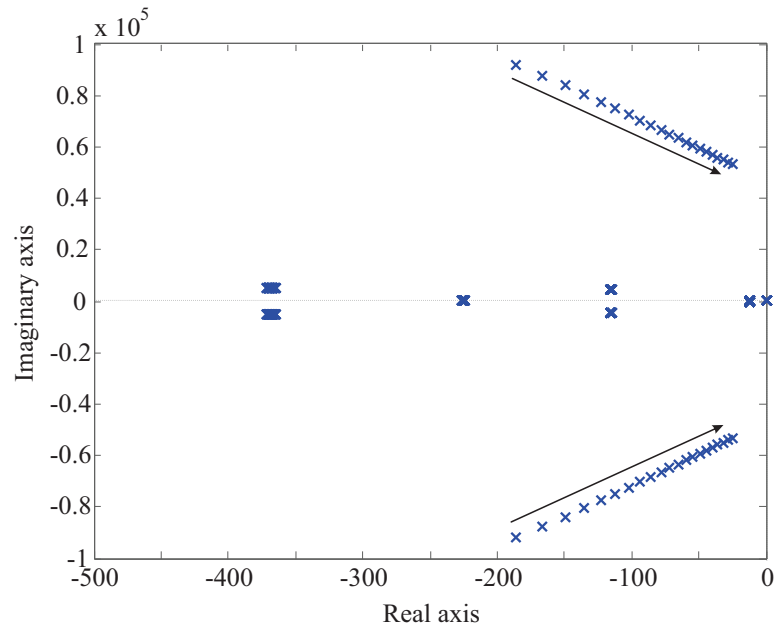


Figure 5.18: Root locus of the ST LV side converter using the LPF-based active damping when varying parameters of connected grid converters: (a) converter-side inductance L_{f1} and (b) filter capacitance C_{ff} .

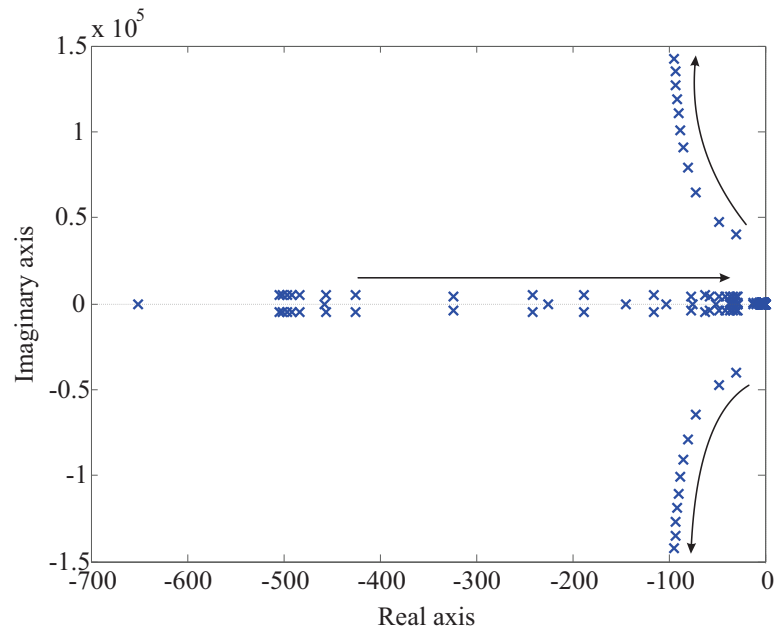
450 Hz) is estimated which is identical to that shown in Fig. 5.24a and thus it is accurate enough for the parameter tuning of the filter-based active damping methods.

5.5.2 Benchmark Grid Evaluation in RTDS

To verify the effectiveness of the proposed method in an extended grid, a CIGRÉ 18-Bus benchmark grid (shown in Fig. 4.19) is employed and simulated in RSCAD, the RTDS software. The cable configuration including cable types and lengths of the benchmark grid are



(a)



(b)

Figure 5.19: Root locus of the ST LV side converter using the LPF-based active damping when varying parameters of connected grid converters: (a) grid-side inductance L_{f2} and (b) number of grid converters.

presented in Table 4.3 and Table 4.4. The LV side of ST is connected to Bus R01, being the voltage source of the benchmark grid. Two grid inverter interfaced DERs are connected to the Buses of R16 and R18, and their nominal power ratings are 25.68 kVA and 17.98 kVA, respectively. To meet the modern grid codes, the reactive power injection of DER is considered, and the power factor (PF) of both grid-interfaced converters is 0.95 in this study. The control strategies mentioned in Chapter 5.3 have been used in the case study. Note that the stability margins of the ST (without DER being connected) and the DERs (standalone) are designed to be between 45° and 60° . Several constant power loads are connected to the

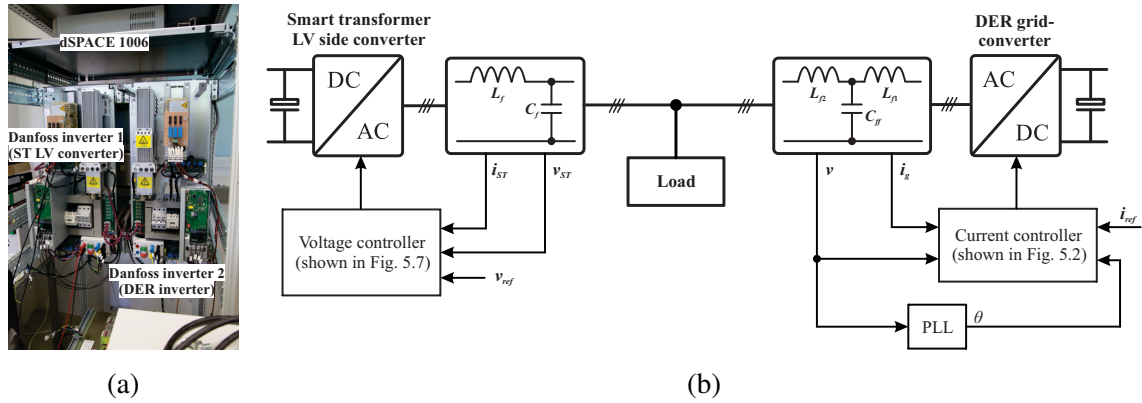


Figure 5.20: Laboratory setup: (a) photo and (b) configuration and control schematics.

Buses of R11, R15, and R16, and their power ratings are 50 kVA, 5 kVA, and 5 kVA, with PF equals to 0.99.

The harmonic instability happens when the two grid converter interfaced DERs connected to the grid. The instability is featured by low-order harmonic distortion of voltage and current (shown in Fig. 5.25). At 0.175 s, the filter-based active damping of Fig. 5.7a is implemented in the ST control, which turns out the harmonic distortions as well as oscillations of both voltage and current are phased out in about two cycles (less than 50 ms). The results show that the proposed active damping methods can stabilize the benchmark grid under various conditions, in particular the ancillary services (like reactive power compensation) are offered by the local DERs.

5.6 Summary of the Chapter

In this chapter, the stability issues of grid-converter-based devices with *LCL*-type filters in a ST-fed grid are studied and active damping-based methods are proposed to address the issues and being seamlessly implemented in the ST LV converter for stabilization of the LV grid. According to the stability analysis, it can be seen that the increasing of the grid-converter-based devices could incur instability when the connected passive loads are heavy in the grid. When light passive loads are connected to the LV grid, it can be seen that the worst case regarding stability happens when very limited grid-converter-based devices are utilized. Under both circumstances, resonance peaks in the low-order harmonic frequency range appear, which compromises the stability and power quality of the LV grid, representing with voltage/current distortion and oscillation.

Since the system stability is determined by the impedance ratio of grid impedance and grid converter impedance, techniques proposed in the literature are usually modifying the grid converter impedance to improve system stability, while this chapter offers another possibility that one can online reshape the grid impedance by means of ST LV converter with stability concerns. Two filter-based active damping stabilization methods are proposed, aiming at reshaping the equivalent grid impedance and therefore improving the stability margin of the

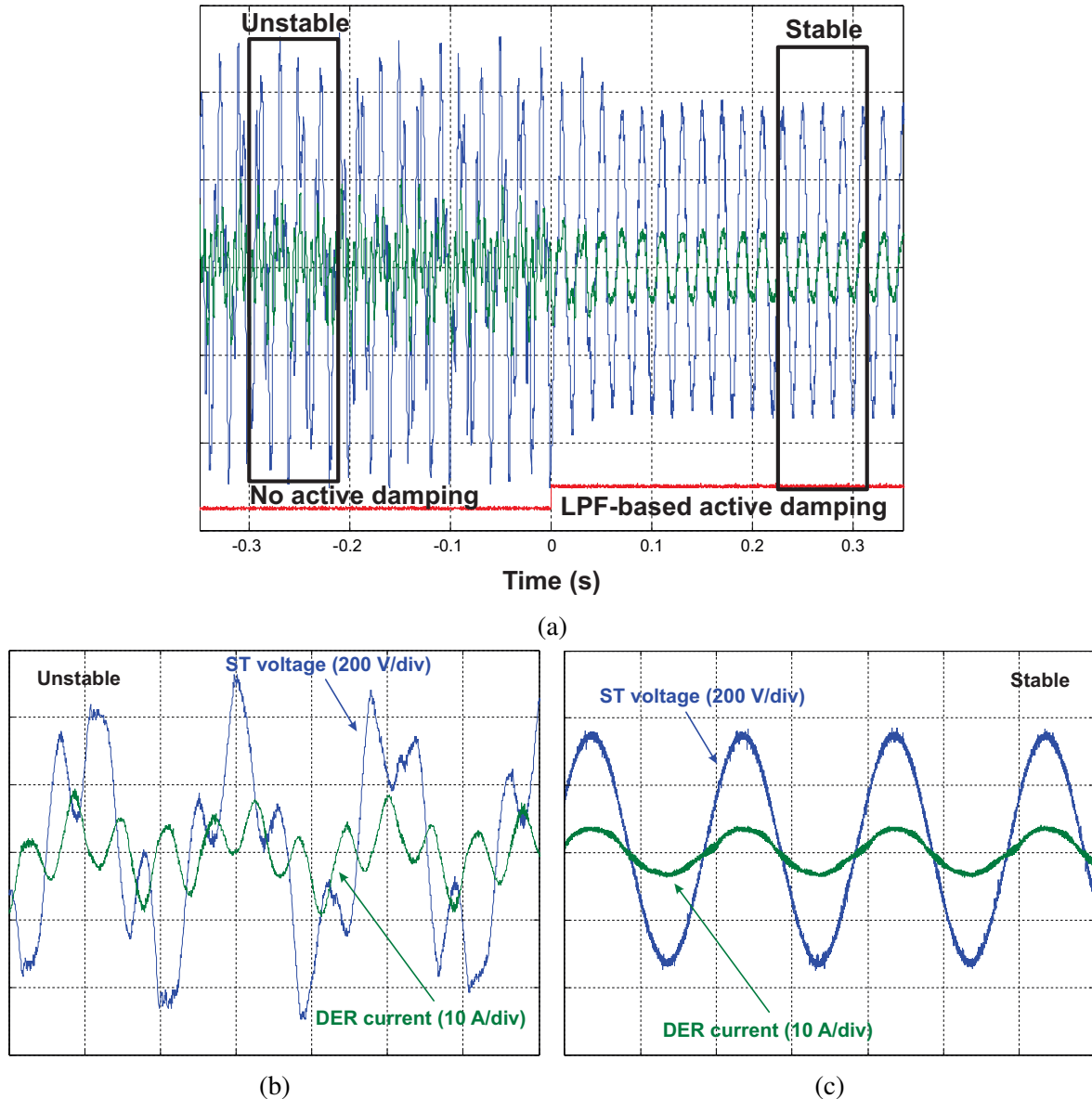


Figure 5.21: Experimental waveforms of ST LV side voltage and DER current with/without LPF-based active damping under the harmonic instability condition: (a) overview of stabilization effect, (b) zoomed waveforms without LPF-based active damping, and (c) zoomed waveforms with LPF-based active damping.

overall system. Both the LEF- and the LPF-based active damping methods only modify the grid impedance as well as the grid features in the critical region and therefore preserve the preferred control features of the voltage control strategy of the ST LV converter in the rest region. From the sensitive analysis, both methods can maintain stability when varying LV grid parameters, for instance, the overall system can have sufficient stability margin when the number of the grid-converter-based devices increases up to 100% of the hosting capacity. In particular, the LEF-based active damping is insensitive to the variation of the *LCL* filter parameters of the grid converters, which is one superior feature for the practical grid implementation, where the filter parameters could be recognizably different due to various manufacturers. The online resonance identification provides the resonance profile of the LV grid, which gives double check for the parameter tuning of the filter-based active damping

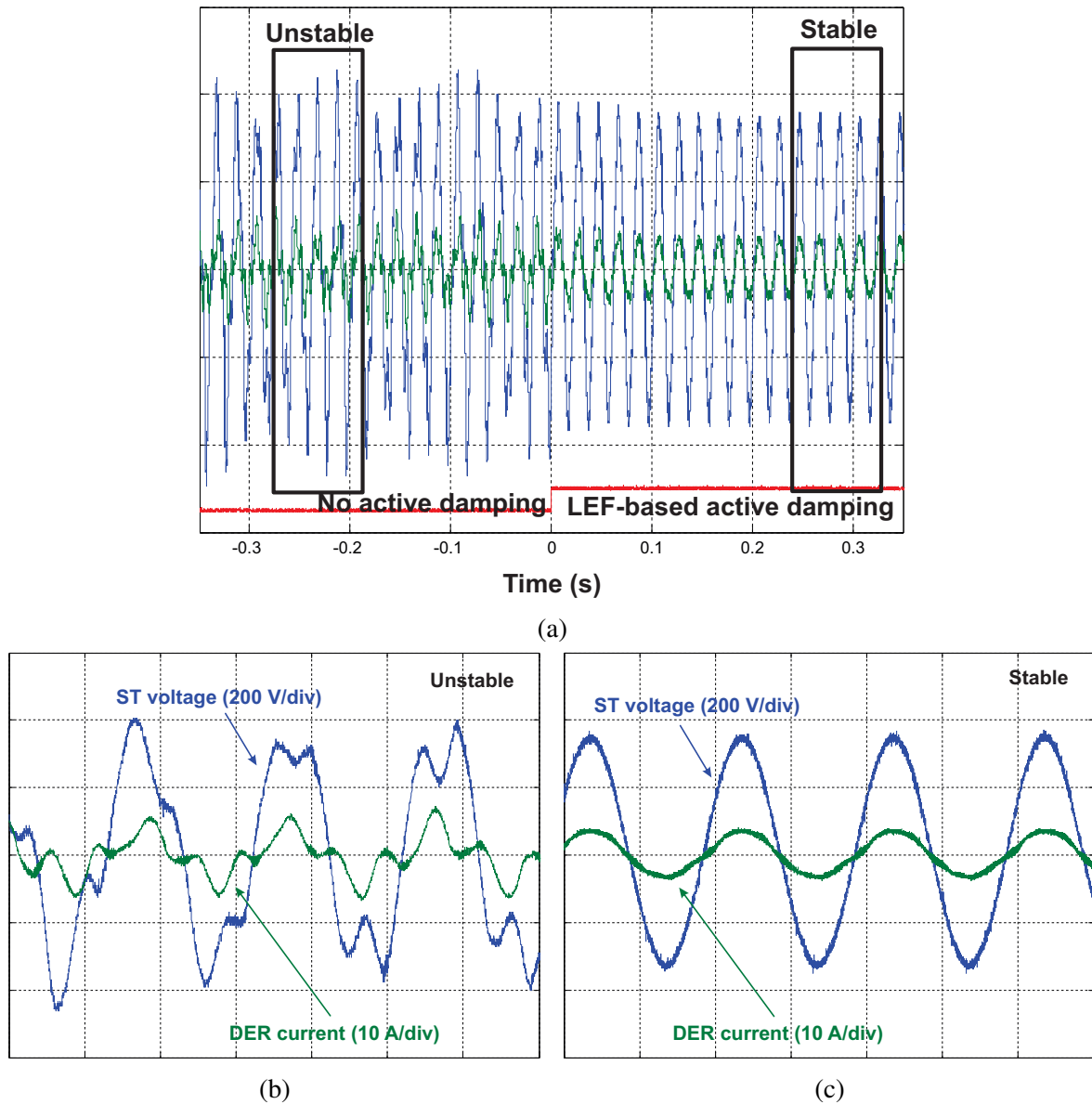
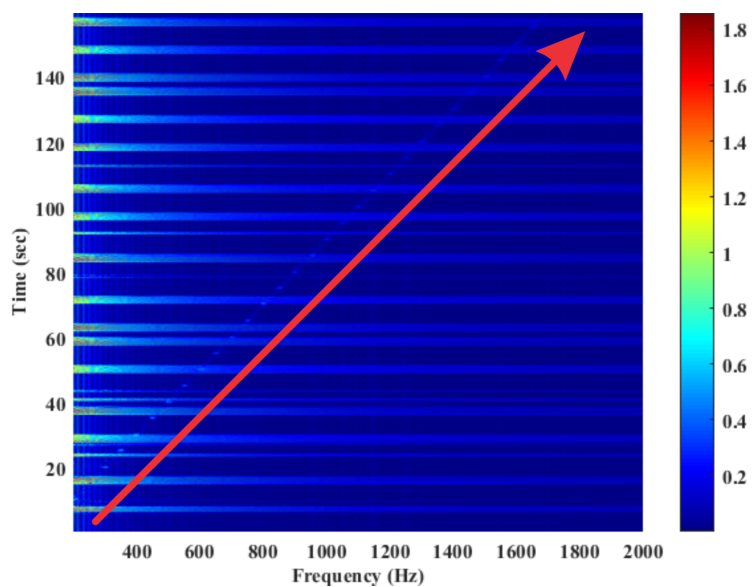


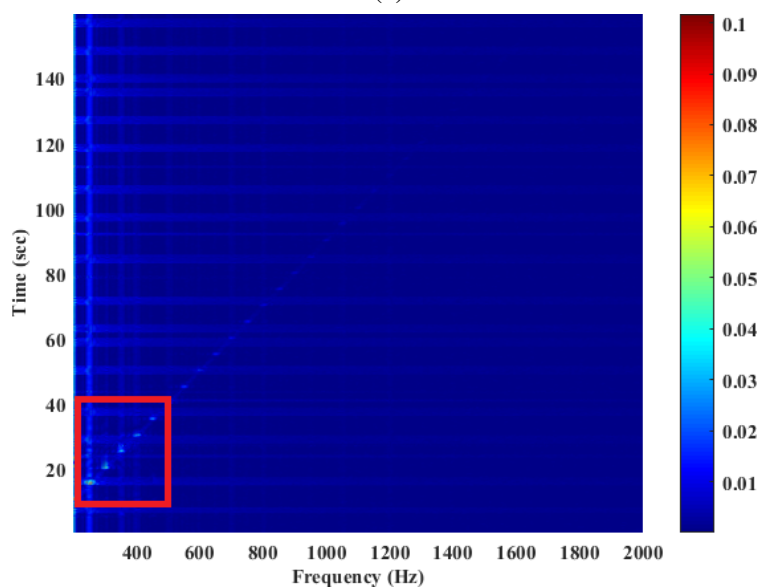
Figure 5.22: Experimental waveforms of ST LV side voltage and DER current with/without LEF-based active damping under the harmonic instability condition: (a) overview of stabilization effect, (b) zoomed waveforms without LEF-based active damping, and (c) zoomed waveforms with LEF-based active damping.

methods. This avoids the stabilization being compromised due to the variations of the LV grid, like "plug-and-play" grid converters, load shedding, and furthermore offers possibility to online assess the stability condition. With the aid of vector fitting, the ST is able to online estimate the resonance profile in the frequency domain as well so that makes the online stability margin estimation reality.

Comprehensive design criteria for the active damping stabilization methods are given in the chapter, considering the voltage control performance and stability of the LV grid. Case studies in RTDS and experimental results both verify the effectiveness of the proposed methods in dealing with resonance and instability issues in an extended grid.

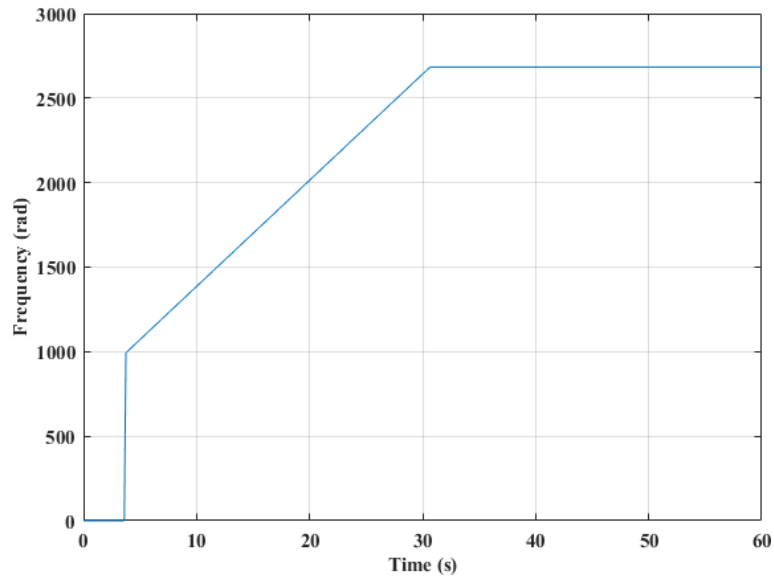


(a)

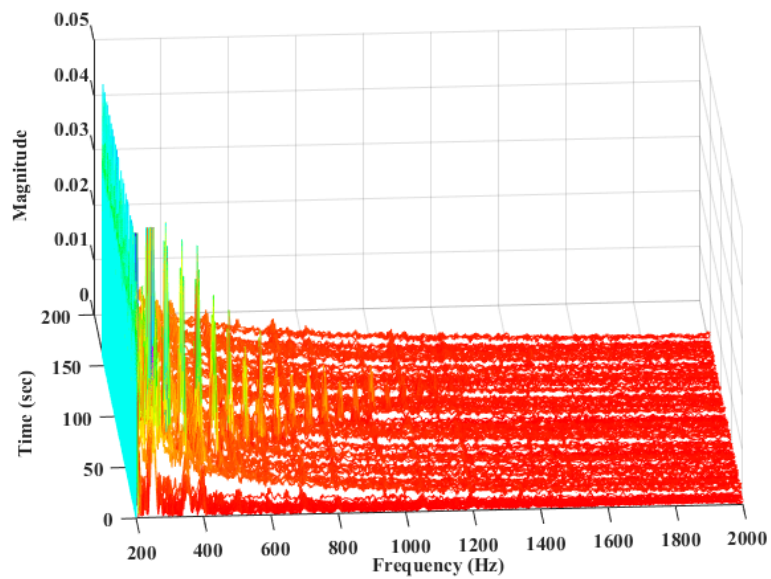


(b)

Figure 5.23: Waterfall FFT plots during the frequency sweeping: (a) ST voltage and (b) ST output current.



(a)



(b)

Figure 5.24: Experimental waveforms of frequency sweep: (a) identification of the resonant frequency and (b) waterfall diagram of the ST output current during frequency sweeping.

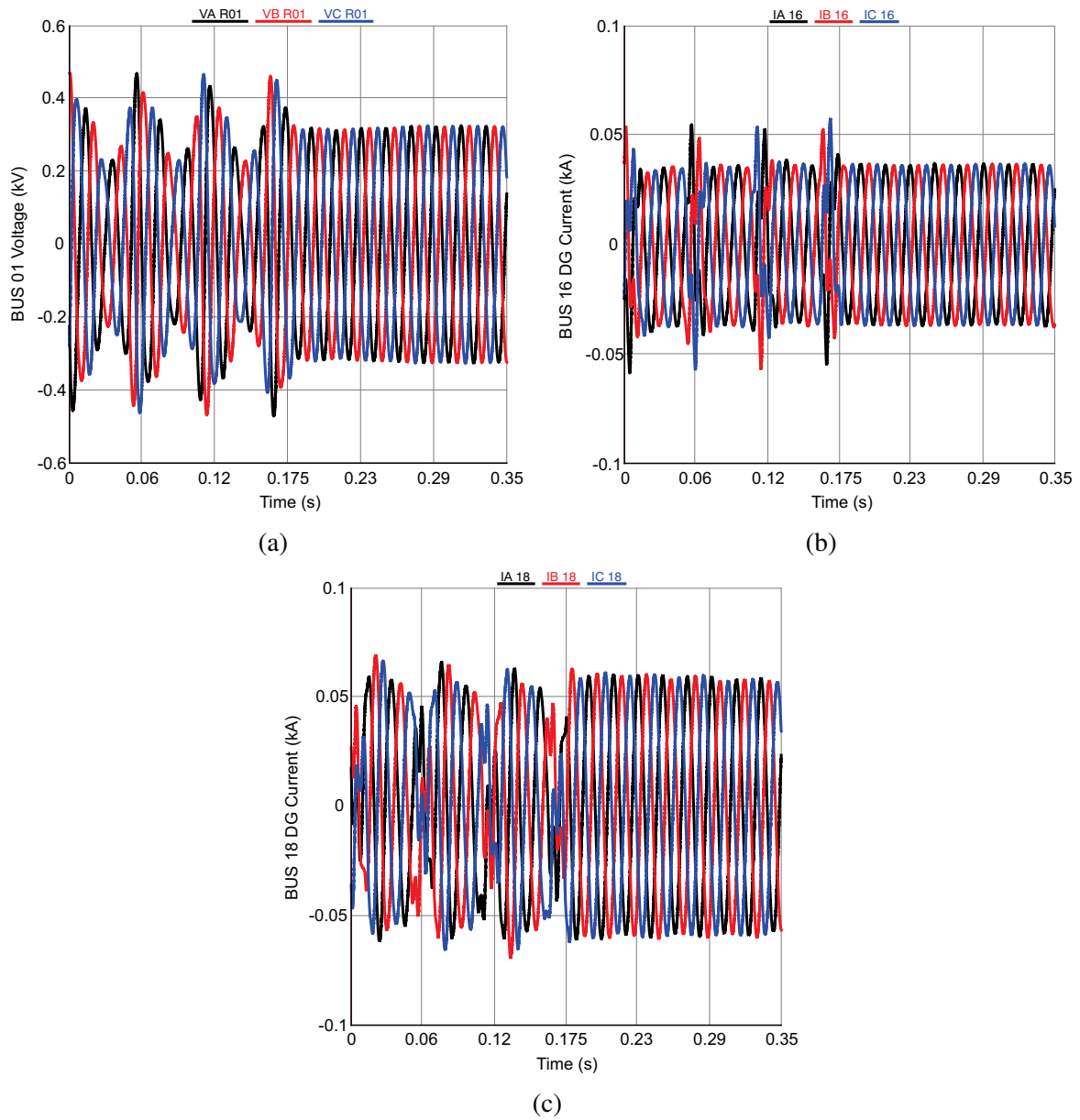


Figure 5.25: RTDS results of a ST-fed grid with/without filter-based active damping under harmonic instability condition: (a) Bus R01 voltage, (b) current injection at Bus R16, and (c) current injection at Bus R18.

6 Influences of Grid Synchronization on Smart Transformer-fed Grid

Different from synchronous generators, which have a synchronization mechanism to the grid that is naturally smoothed by their inertia, grid converters do not inherently preserve their phase shift as well as phase sequencing during grid-connected operation. Most of grid converters have to be equipped with PLL-based synchronization [75, 76]. Apart from control dynamics and filter resonances, grid synchronization is another key factor that challenges the stability of the grid converter and the stable operation of the distribution grid, where its influences on the ST LV converter are highlighted in Fig. 6.1. This chapter presents a full model of the grid converter considering the effects of the PLL and proposes stability criterion based on the full model, which is able to deal with the stability issues under both small- and large-phase perturbations. The stability issue related to the PLL in a ST-fed grid is discussed and a stabilization method has been proposed to address the issue.

6.1 Stability Issues Associated With PLL

When the penetration level of grid converters is low, the influence of PLL behaviors on the grid may be negligible compared to the inertia response of the other devices. However, under some circumstances, ignoring the effects of grid synchronization would result in misjudging the grid characteristics and stability. One scenario is high penetration level of grid converters in a distribution grid, it could have recognizably different voltage stability conditions when the PLL bandwidths (BW) are different. In [77], a CIGRÉ distribution grid with high penetration grid converters with different PLL BWs has been studied, it is shown that the wide utilization of low BW PLLs in a distribution grid could incur voltage collapse. In addition, inertialess hybrid grids (e.g., microgrids) become more and more common in modern power systems, which are dominated by power electronics interfaces. One promising paradigm is the ST-fed grid and it can be found that the effects of the grid synchronization determine the frequency and harmonic stability. In [78], the stability of the ST-fed grid during frequency regulation has been investigated and it is shown that the low BW PLL for the grid converter could lead to severe frequency and power oscillations during grid frequency variation. With these considerations, the effects of the PLL-based synchronization have to be included in the stability analysis when the DER penetration is high or the grid inertia is low.

The previous research efforts in this topic are mainly focusing on the modeling and stability analysis of single grid converter in a weak grid. One method to accurately deal with grid converters and its synchronization is to use impedance-based models, which are derived from the small-signal modeling techniques [79]. In [64], the input admittance by introducing the effects of PLL has been investigated and shows that the high BW PLL enhances the negative real part of the converter admittance which could compromise the system stability. The developed admittance/impedance-based model of grid converter can well describe not only the physical impedance (e.g., output filters) but also the control system as well as the grid

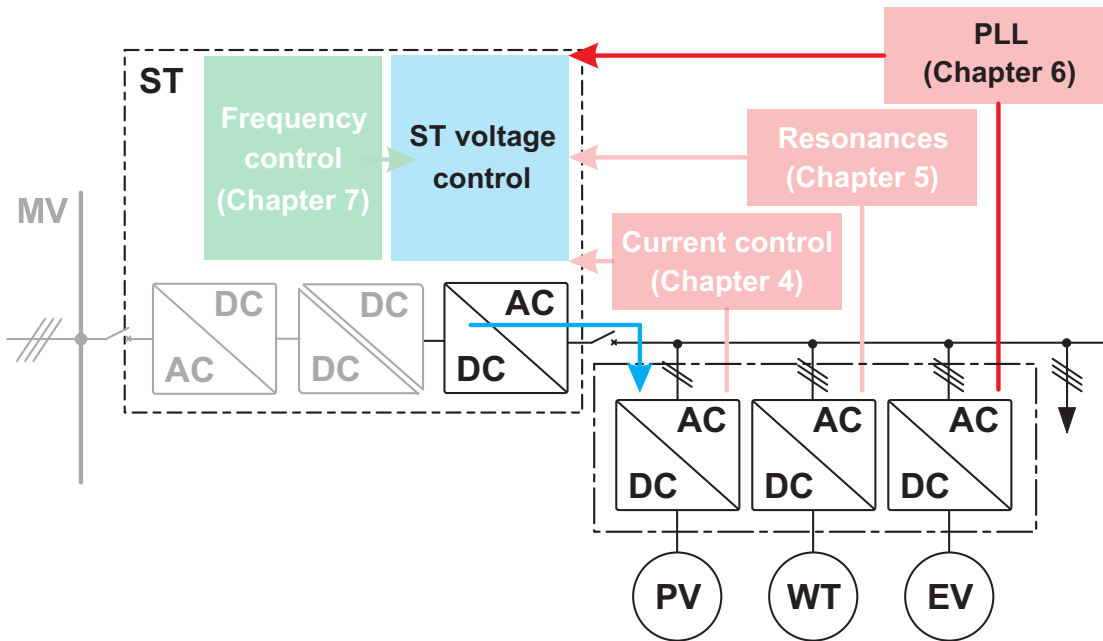


Figure 6.1: Research focus of Chapter 6: interactions between ST and grid synchronization of grid converters.

synchronization [55]. In [38] and [80], impedance models including the effect of the PLL are developed in the synchronous reference frame and the stationary frame, respectively. The motivations of those small-signal models are to investigate the static behaviors and to assess the static stability, assuming the phase deviation between grid and PLL is insignificant. Considering the coupling effects under different frames, the small-signal impedance models in these work has been further extended to the matrix form instead of transfer function form. Therefore, generalized Nyquist criterion has been applied to the impedance matrix of grid converter that considers control and PLL in the synchronous frame to assess system stability [38]. The analysis and results reveal that the negative incremental qq resistance plays an important role on system stability. The interaction between grid synchronization and weak grid has also been studied with similar methodology in [81], showing even a small increment of PLL BW in a weak grid could compromise the stability of the overall grid.

All of the above-mentioned models are used for the static stability analysis and therefore one of the assumptions is the grid phase perturbation is pretty small. However, in an actual grid, large phase perturbation happens as well, for example, phase jumps due to grid faults of distribution grids, frequency variation in a ST-fed grid. Under these conditions, the models in the literature may not be accurate enough for analysis. To address this issue, a more accurate small-signal model of grid converter considering the synchronization is presented in this chapter which is able to describe system behaviors during both small and large phase perturbations. Stability criterion based on the proposed model is given for stability analysis during different phase perturbations.

On the other hand, as seen in Chapter 5, the ST-fed grid offers a promising possibility to adapt its output impedance and then stabilize the LV grid. One consideration is that whether this method is efficient for the issues caused by the PLLs. To explore the potential, this chapter

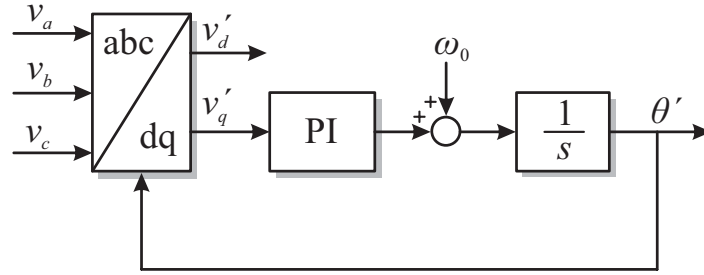


Figure 6.2: Schematic diagram of a synchronous reference frame PLL.

analyzes the interactions between the ST LV converter and the PLL of one grid converter. Based on the analysis, a stabilization method is proposed to address the issues. Simulation and experimental results are given to validate the effectiveness of the proposed method.

6.2 Quasistationary Behaviors of Synchronization

The most extended grid synchronization technique used in three-phase power converters is the PLL based on the synchronous reference frame (SRF-PLL) [82]. The schematic diagram of a typical SRF-PLL is shown in Fig. 6.2, in which the three-phase voltage vector is transformed from the abc frame to the dq frame by the Park's transformation and the phase angle θ' is controlled by a feedback loop that regulates the q component to zero. Once the PLL is locked, assuming the PI controller is well tuned, the phase displacement $\Delta\theta'$ (between the actual phase and the detected phase) is zero in the steady state. When a phase perturbation occurs, for instance, phase jump, frequency variation, the phase displacement during the transient would be asymptotically approaching zero as shown in Fig. 6.3 provided the PLL is asymptotically stable. In this case study, an actual phase jump $\Delta\theta = \pi/18$ of the grid voltage happens at 1 s. Considering the inherent response of PLL, the phase displacement seen from the PLL will be a time-variant value and is indicated by $\Delta\theta'(t)$ in Fig. 6.3a. Being a second-order system, it is expected that $\Delta\theta'(t)$ exhibits oscillatory behaviors after a disturbance. From the point of view of synchronous frame, as shown in Fig. 6.3b, the synchronous reference frame of the PLL (d_{PLL}/q_{PLL}) is asymptotically pursuing towards the synchronous frame of the actual grid voltage (d_{grid}/q_{grid}) in an oscillatory manner. In a current-controlled grid converter, assuming the bandwidth of the current controller is far higher than the bandwidth of PLL (e.g., ten-time higher), namely the transient of current control loop is negligible under the circumstance, the converter current can be regarded to be following the PLL-oriented reference frame all the time. It is conjectured that the converter current mapped in the synchronous frame of the actual grid voltage is oscillatory, which leads to the oscillated characteristics of the equivalent admittance of the grid converter during disturbances. In a electric grid with high penetration of grid converters or an inertia-less grid, the oscillatory behaviors cause by quasistationary synchronization would be critical and can compromise the stability and resilience of grids.

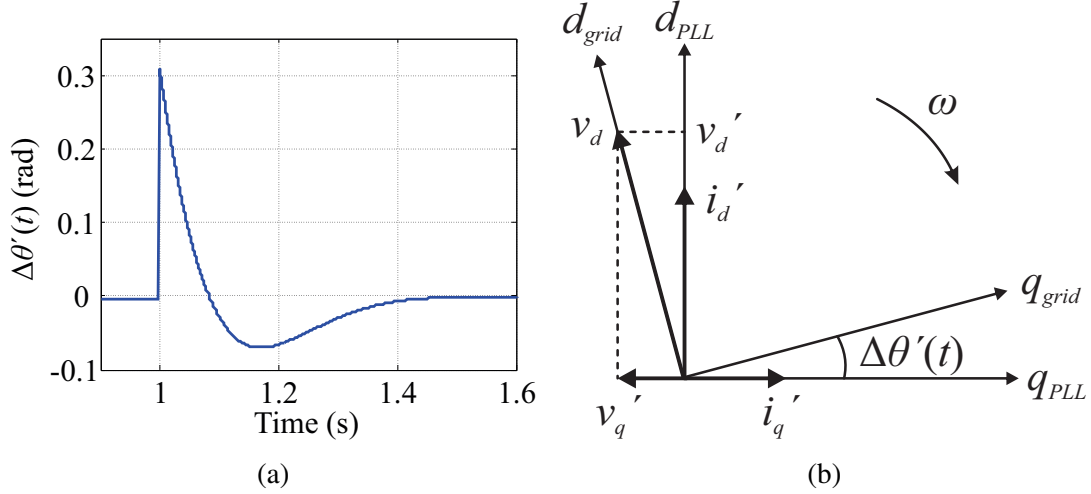


Figure 6.3: Quasistationary behavior of SRF-PLL during phase perturbation: (a) phase displacement $\Delta\theta$ and (b) phasor diagram of grid voltage and converter current.

6.2.1 Conventional Small-signal Model of SRF-PLL

Noting that the Park transform of the PLL holds nonlinearity, to linearize the nonlinear elements which are affected by the PLL, the transfer matrix can be split up into two parts:

$$\mathbf{T}(\theta') = \begin{bmatrix} \cos\Delta\theta' & \sin\Delta\theta' \\ -\sin\Delta\theta' & \cos\Delta\theta' \end{bmatrix} \mathbf{T}(\theta_0) \quad (6.1)$$

where $\theta' = \theta_0 + \Delta\theta'$, here $\theta_0 = \omega_0 t$ represents the actual phase angle of the grid voltage.

By using the transform, the d and q components of the grid voltage: v_d' and v_q' can be calculated by

$$\begin{bmatrix} v_d' \\ v_q' \end{bmatrix} = \begin{bmatrix} \cos\Delta\theta' & \sin\Delta\theta' \\ -\sin\Delta\theta' & \cos\Delta\theta' \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \approx \begin{bmatrix} 1 & \Delta\theta' \\ -\Delta\theta' & 1 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (6.2)$$

where v_d and v_q are the d and q components by applying $\mathbf{T}(\theta_0)$, namely, the actual d and q components of the grid voltage.

If the actual voltages in the dq frame: $v_d = V_d + \Delta v_d$ and $v_q = V_q + \Delta v_q$, the small-signal equations of the Park transform (6.2) can be written by

$$\begin{bmatrix} \Delta v_d' \\ \Delta v_q' \end{bmatrix} = \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \begin{bmatrix} V_q \\ -V_d \end{bmatrix} \Delta\theta' \quad (6.3)$$

where V_d , V_q and Δv_d , Δv_q are the dc quantities and the small-signal perturbation signals of the actual voltage, respectively, while $\Delta v_d'$ and $\Delta v_q'$ are the perturbation signals of the voltage translated by the transform.

According to the PLL schematic shown in Fig. 6.2, one can have the response from $\Delta v_q'$ to $\Delta\theta'$ is the $H_{PLL}(t)$, which in frequency domain can be translated to the open-loop transfer

function of the PLL. Combining $H_{PLL}(t)$ and (6.3) and then translating it to the frequency domain by using the Laplace transform, yields

$$\begin{bmatrix} \Delta v'_d(s) \\ \Delta v'_q(s) \end{bmatrix} = \begin{bmatrix} 1 & V_q G_{PLL,op}(s) \\ 0 & 1 - V_d G_{PLL,op}(s) \end{bmatrix} \begin{bmatrix} \Delta v_d(s) \\ \Delta v_q(s) \end{bmatrix}. \quad (6.4)$$

Here $G_{PLL,op}$ can be defined by

$$G_{PLL,op}(s) = \frac{\Theta'(s)}{V_q(s)} = \frac{H_{PLL}(s)}{1 + V_d \cdot H_{PLL}(s)} \quad (6.5)$$

which is the open-loop q component transfer function of the PLL. Noting that $\Delta v_q = \Delta\theta \cdot V_d$, the closed-loop q component transfer function of the PLL is given by

$$G_{PLL,cl}(s) = \frac{\Theta'(s)}{\Theta(s)} = \frac{V_d \cdot H_{PLL}(s)}{1 + V_d \cdot H_{PLL}(s)} \quad (6.6)$$

where $\Delta\theta$ is the actual phase perturbation of grid voltage.

6.2.2 Higher-order Model of SRF-PLL on Large-signal Perturbation

It is worth noting that, for the conventional small-signal approximation methodologies, only first-order approximation terms would be employed by the linearization as shown in (6.2) and it can well describe the system behaviors when the phase perturbation is less than $\pm 7^\circ$ [83]. However, larger phase perturbation could occur during grid faults, for example, the grid codes in Northern Europe require renewable energies to withstand sudden phase jumps of up to $\pm 30^\circ$ and frequency variation between 47.5 Hz-51.5 Hz [84, 85]. With this consideration, the higher-order approximation terms should be included according to the small-signal approximation of basic trigonometric functions [83], for instance to consider the second-order approximation in (6.2) ensures the model accuracy (i.e., less than 1% error) up to $\pm 38^\circ$ phase jump and therefore will satisfy most of realistic cases in power system. As a result, v'_d and v'_q during large phase perturbation can be written by

$$\begin{bmatrix} v'_d \\ v'_q \end{bmatrix} = \begin{bmatrix} \cos\Delta\theta' & \sin\Delta\theta' \\ -\sin\Delta\theta' & \cos\Delta\theta' \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \approx \begin{bmatrix} \frac{2-\Delta\theta'^2}{2} & \Delta\theta' \\ -\Delta\theta' & \frac{2-\Delta\theta'^2}{2} \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix}. \quad (6.7)$$

The small-signal equation of the Park transform (6.7) with second-order approximation can be obtained by

$$\begin{bmatrix} \Delta v'_d \\ \Delta v'_q \end{bmatrix} = \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \begin{bmatrix} V_q \\ -V_d \end{bmatrix} \Delta\theta' + \begin{bmatrix} -\frac{1}{2}V_d \\ -\frac{1}{2}V_q \end{bmatrix} \Delta\theta'^2 \quad (6.8)$$

Similarly, the small-signal equation of the transform with second-order approximation for

the converter current can be derived by

$$\begin{bmatrix} \Delta i'_d \\ \Delta i'_q \end{bmatrix} = \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} + \begin{bmatrix} I_q \\ -I_d \end{bmatrix} \Delta \theta' + \begin{bmatrix} -\frac{1}{2}I_d \\ -\frac{1}{2}I_q \end{bmatrix} \Delta \theta'^2 \quad (6.9)$$

where $[\Delta i_d, \Delta i_q]^T$ are the perturbations of the actual converter current, $[\Delta i'_d, \Delta i'_q]^T$ are the perturbations of the converter current seen by the transform, I_d and I_q are the amplitudes of d and q components of converter current.

6.2.3 Modeling of PLL-synchronized Grid Converter

The system configuration as well as the control schematics of a grid converter is shown in Fig. 6.4. In the literature, both the current-controlled and the power-controlled grid converters essentially regulate the three-phase converter current $[i_a, i_b, i_c]^T$ [82]. Therefore, a current-controlled converter with single current loop in the synchronous frame (shown in Fig. 6.4b) is considered in this chapter for the sake of analysis simplicity. Given the three-phase PCC voltage $[v_a, v_b, v_c]^T$, the average model of the converter in abc frame is

$$L_{f1} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = G_d \begin{bmatrix} v_{ra} \\ v_{rb} \\ v_{rc} \end{bmatrix} - \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (6.10)$$

where L_{f1} is the output filter of the grid converter, $[v_{ra}, v_{rb}, v_{rc}]^T$ are the reference voltage of the grid converter, and G_d represents the computation and PWM delay. The three-phase converter current and the PCC voltage are measured and sampled through analog-to-digital converters (ADCs) and passed into the controller. Using an ideal transform (with actual phase angle of the grid voltage: θ_0), the dq frame average model in s -domain is given by

$$\begin{bmatrix} L_{f1}s & -\omega L_{f1} \\ \omega L_{f1} & L_{f1}s \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} G_d & 0 \\ 0 & G_d \end{bmatrix} \begin{bmatrix} v_{rd} \\ v_{rq} \end{bmatrix} - \begin{bmatrix} v_d \\ v_q \end{bmatrix}. \quad (6.11)$$

Noting that all of the d and q components in (6.11) are obtained by applying $\mathbf{T}(\theta_0)$, namely all these components are directly oriented with the actual PCC voltage, and thus do not rely on the PLL.

According to the control scheme shown in Fig. 6.4b, the perturbation equation of current control can be written by

$$\begin{bmatrix} \Delta v'_{rd} \\ \Delta v'_{rq} \end{bmatrix} = - \begin{bmatrix} G_{cc} & 0 \\ 0 & G_{cc} \end{bmatrix} \begin{bmatrix} \Delta i'_d \\ \Delta i'_q \end{bmatrix} + \begin{bmatrix} G_{cc} & 0 \\ 0 & G_{cc} \end{bmatrix} \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} \Delta v'_d \\ \Delta v'_q \end{bmatrix} \quad (6.12)$$

where $[\Delta i_{refd}, \Delta i_{refq}]^T$ are the perturbations of the current references in dq frame, $[\Delta v'_{rd}, \Delta v'_{rq}]^T$ are the perturbations of the reference voltage in dq frame, and G_{cc} is the transfer function of

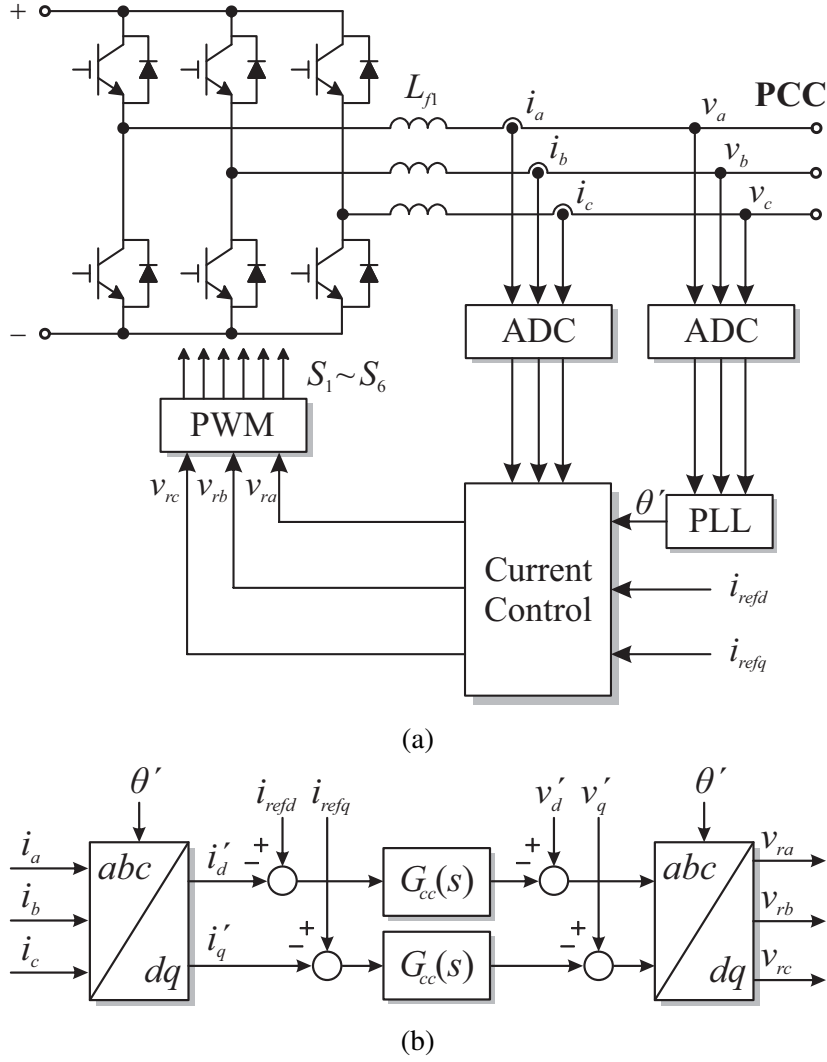


Figure 6.4: A three-phase grid converter: (a) system configuration and (b) control scheme in the synchronous frame.

the current controller. It is worth noting that all of the d and q components in (6.12) are obtained by applying $\mathbf{T}(\theta')$, which indicates the influences of synchronization are coupled.

To decouple the PLL effects, the procedures with small-angle approximation can be applied to the variables which correspond to the (inverse) transform. For the voltage/current transform, the small-signal expressions with second-order approximation are given by (6.8) and (6.9), where the second-order terms have been included. For the reference voltage inverse transform, namely $[\Delta v_{rd}, \Delta v_{rq}]^T$, it can be derived as following:

$$\begin{bmatrix} \Delta v_{rd} \\ \Delta v_{rq} \end{bmatrix} = \begin{bmatrix} \Delta v'_{rd} \\ \Delta v'_{rq} \end{bmatrix} + \begin{bmatrix} -V'_{rq} \\ V'_{rd} \end{bmatrix} \Delta \theta' + \begin{bmatrix} -\frac{1}{2}V'_{rd} \\ -\frac{1}{2}V'_{rq} \end{bmatrix} \Delta \theta'^2 \quad (6.13)$$

where V'_{rd} and V'_{rq} are the amplitudes of d and q components of $[v'_{rd}, v'_{rq}]^T$.

By substituting (6.8), (6.9) and (6.13) into (6.11), one can get the full higher accurate model

of the grid converter:

$$\begin{aligned} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} &= \mathbf{I}(s) \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \mathbf{Y}(s) \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \begin{bmatrix} \Theta_{d1} \\ \Theta_{q1} \end{bmatrix} \Delta \theta' + \begin{bmatrix} \Theta_{d2} \\ \Theta_{q2} \end{bmatrix} (\Delta \theta')^2 \\ &= \begin{bmatrix} I_{dd} & I_{dq} \\ I_{qd} & I_{qq} \end{bmatrix} \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} Y_{dd} & Y_{dq} \\ Y_{qd} & Y_{qq} \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \begin{bmatrix} \Theta_{d1} \\ \Theta_{q1} \end{bmatrix} \Delta \theta' + \begin{bmatrix} \Theta_{d2} \\ \Theta_{q2} \end{bmatrix} (\Delta \theta')^2 \end{aligned} \quad (6.14)$$

where

$$\begin{aligned} Y_{dd} = Y_{qq} &= \frac{(1 - G_d)(G_{cc}G_d + L_{f1}s)}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2}, Y_{dq} = -Y_{qd} = \frac{(1 - G_d)L_{f1}\omega}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2} \\ I_{dd} = I_{qq} &= \frac{G_{cc}G_d(G_{cc}G_d + L_{f1}s)}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2}, I_{dq} = -I_{qd} = \frac{G_{cc}G_dL_{f1}\omega}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2} \\ \Theta_{d1} &= \frac{G_d(G_{cc} + L_{f1}s + L_{f1}\omega)}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2} \cdot (V_q - V'_{rq} - I_q G_{cc}) \\ \Theta_{q1} &= \frac{G_d(G_{cc} + L_{f1}s - L_{f1}\omega)}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2} \cdot (-V_d + V'_{rd} + I_d G_{cc}) \\ \Theta_{d2} &= \frac{G_d(G_{cc} + L_{f1}s + L_{f1}\omega)}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2} \cdot \left(-\frac{V_d}{2} - \frac{V'_{rd}}{2} - \frac{I_d}{2} G_{cc}\right) \\ \Theta_{q2} &= \frac{G_d(G_{cc} + L_{f1}s - L_{f1}\omega)}{(G_{cc}G_d + L_{f1}s)^2 + L_{f1}^2\omega^2} \cdot \left(-\frac{V_q}{2} - \frac{V'_{rq}}{2} - \frac{I_q}{2} G_{cc}\right). \end{aligned} \quad (6.15)$$

6.3 Stability Criterion of Grid Converter During Phase Perturbation

This section starts with the model evaluation of PLL-synchronized grid converter and explains the components of the proposed model of (6.14). Both conventional small-signal and higher accurate models can be derived from the proposed model depending on the orders of θ' . The impedance-based stability criterion of grid converters considering synchronization effects in proposed based on the proposed model.

6.3.1 Model Evaluation

From the model of (6.14), it can be seen that three sets of terms are included in a current-controlled grid converter. First, $\mathbf{I}(s)$ represents the nature of the current control, which is essentially the closed-loop transfer function matrix of the current control system. Second, $\mathbf{Y}(s)$ represents the impacts of the grid voltage on the converter current, which can be interpreted as the equivalent admittance matrix of the grid converter. Last but not least, the $\Delta \theta'$ -related terms have the features of synchronization represented. The combination of the first two terms are actually equivalent to the impedance-based model used in literature [55],

while the effects of synchronization are ignored. The Bode diagrams of these two terms of the model are shown in Fig. 6.5a, by using the system parameters listed in Table 6.1. The non-diagonal elements of $\mathbf{I}(s)$ and $\mathbf{Y}(s)$ are not shown in this figure since the magnitudes of these elements are much lower than those of the diagonal elements, indicating the effects of the non-diagonal elements are negligible. It can be seen that the current controller (which is a PI controller) used in this paper can achieve zero steady-state error within its bandwidth (3160 Hz), while the grid voltage disturbances have very limited influence within the bandwidth according to the admittance characteristics.

When the effects of grid synchronization are considered, the $\Delta\theta'$ -related terms have to be taken into account. For conventional small-signal analysis, the first-order perturbation terms are used and therefore the model of (6.14) can be rewritten by

$$\begin{aligned} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} &= \begin{bmatrix} I_{dd} & I_{dq} \\ I_{qd} & I_{qq} \end{bmatrix} \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} Y_{dd} & Y_{dq} \\ Y_{qd} & Y_{qq} \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \begin{bmatrix} \Theta_{d1} \\ \Theta_{q1} \end{bmatrix} \Delta\theta' \\ &= \begin{bmatrix} I_{dd} & I_{dq} \\ I_{qd} & I_{qq} \end{bmatrix} \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} Y_{dd}^{\theta 1} & Y_{dq}^{\theta 1} \\ Y_{qd}^{\theta 1} & Y_{qq}^{\theta 1} \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \end{aligned} \quad (6.16)$$

where

$$\begin{aligned} Y_{dd}^{\theta 1} &= Y_{dd}, Y_{qd}^{\theta 1} = Y_{qd}, \\ Y_{dq}^{\theta 1} &= Y_{dq} + \Theta_{d1} G_{PLL,op}, \\ Y_{qq}^{\theta 1} &= Y_{qq} + \Theta_{q1} G_{PLL,op}. \end{aligned} \quad (6.17)$$

It can be seen that the first-order perturbation terms contribute to the equivalent admittance matrix. Assuming the grid converter operates at unity power factor (i.e., $i_q = 0$), it is expected that the effects of PLL on the d components of the equivalent admittance are negligible according to (6.17), while the q components of the equivalent admittance are modified when the PLL being taken into account. Comparisons of Bode plots of Y_{qq} (without the effects of PLL) and $Y_{qq}^{\theta 1}$ (with the effects of PLL) are presented in Fig. 6.5b. It can be observed that both the magnitude and the phase of Y_{qq} in the low-frequency range have been significantly modified when the PLL effects are included. Furthermore, different PLL bandwidth from 20 Hz to 200 Hz (i.e., BW_{PLL}/BW_{cc} from 0.006 to 0.06, BW_{PLL} and BW_{cc} are the bandwidths of the PLL and the current control) studied and the Bode plots of $Y_{qq}^{\theta 1}$ are shown in the figure as well. It is shown that the characteristics of $Y_{qq}^{\theta 1}$ in the low-frequency range can be further altered when different PLL BW being applied.

For analysis during large phase perturbation, the second-order perturbation terms are necessary for linearization procedure. As a result, the full higher accurate model of (6.14) will be used for the characteristic evaluation and stability analysis in the followings. As a result, the full model of (6.14) will be used for the characteristic evaluation and stability analysis in the followings. With the consideration of second-order approximation, the proposed model of

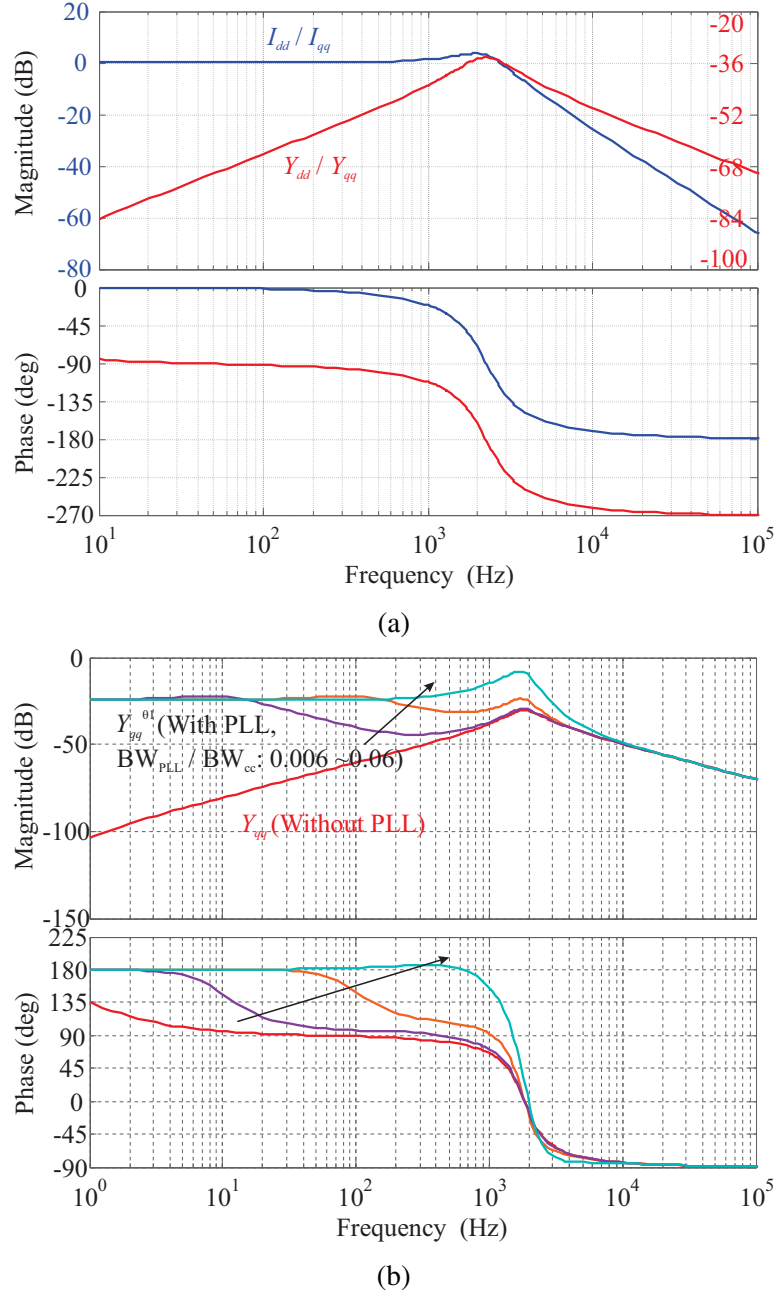


Figure 6.5: Bode plots of grid converter represented by small-signal model: (a) without the effects of PLL and (b) with the consideration of PLL.

(6.14) can be rewritten by

$$\begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} = \begin{bmatrix} I_{dd} & I_{dq} \\ I_{qd} & I_{qq} \end{bmatrix} \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} Y_{dd}^{\theta 1} & Y_{dq}^{\theta 1} \\ Y_{qd}^{\theta 1} & Y_{qq}^{\theta 1} \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \begin{bmatrix} \Theta_{d2} \\ \Theta_{q2} \end{bmatrix} (\Delta \theta')^2. \quad (6.18)$$

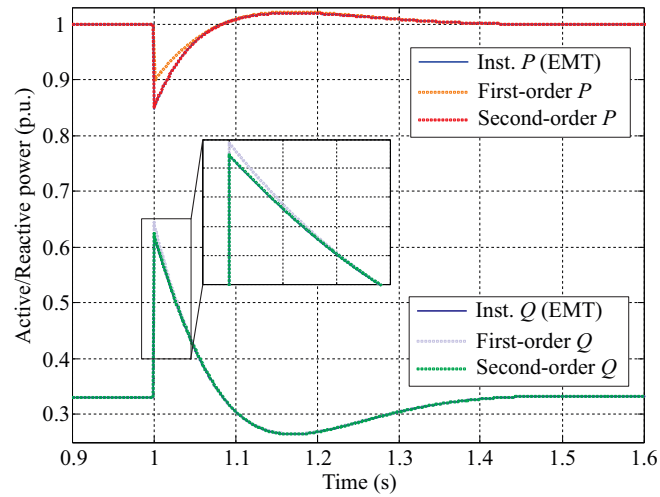
First of all, a comparison of the responses of (6.16) with only the first-order terms and (6.18) with the second-order terms are shown in Fig. 6.6 with the parameters of Table 6.1. Here, two different phase jumps ($\pi/18$ and $\pi/6$) are used in the case studies (Fig. 6.6a and Fig. 6.6b). The phase jumps happen at $t = 1$ s, and the injection of active and reactive power in steady-state are 1 p.u. and 0.33 p.u. (power factor (PF) is 0.95), respectively. To evaluate the model

Table 6.1: System Parameters

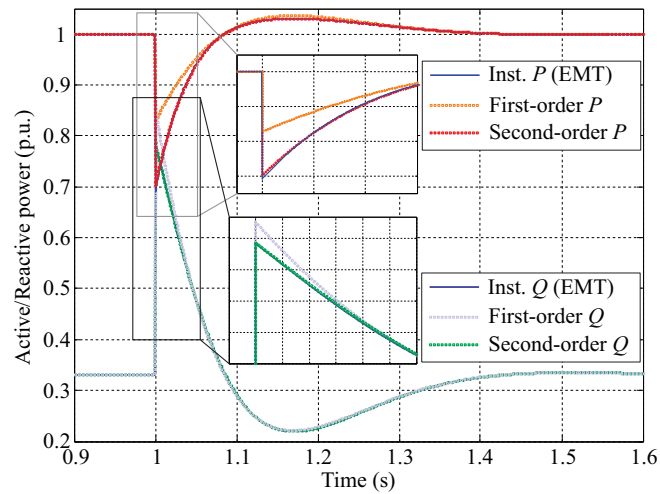
Symbol	Quantity	Value
L_{f1}	Output filter of grid converter	5 mH
T_s	sampling frequency	10 kHz
k_{pc}	proportional gain of current control	15
k_{ic}	integral gain of current control	250
k_{pptl}	proportional gain of PLL	18.4
k_{iptl}	integral gain of PLL	169.3

accuracy, the simulation waveforms done by the MATLAB/Simulink are provided in the figures. In the simulation, the grid inverter and its output filter is implemented by using the PLECS toolbox, and the control system as well as PLL is done by the Simulink. Both the models with the first-order and the second-order terms are developed by the basic Simulink blocks such as square and summation as well as transfer functions. The responses of the models are obtained by using the ode3 (Bogacki-Shampine) Solver with fixed step. Obviously, the responses of the more accurate model with the second-order terms are completely overlapping with the simulation waveforms in both cases, showing high accuracy, while the response of the conventional small-signal model with the first-order terms do not, which have noticeable mismatches in both case studies, especially when the phase jump is considerable (e.g. $\pi/6$, seen from Fig. 6.6b). The percentage of the model mismatch during different phase perturbations can be evaluated and is shown in Fig. 6.6c, where the mismatches of the first-order model and the second-order model are represented by the blue and the red curves, respectively. It can be seen that the conventional small-signal model with the first-order terms has much higher mismatch than the model with the second-order terms. The confidence region is highlighted where the model mismatch in this region is lower or equal to 5 % mismatch. It can be observed that the conventional small-signal model with the first-order terms presents higher than 5 % mismatch when the phase perturbation is larger than 18° ($\pi/10$) (out of the confidence region), while the mismatch of the model with the second-order terms is lower than 1 % in the entire whole phase perturbation range. Under this circumstance, the proposed more accurate model must be considered for obtaining accuracy dynamic responses and stability assessment.

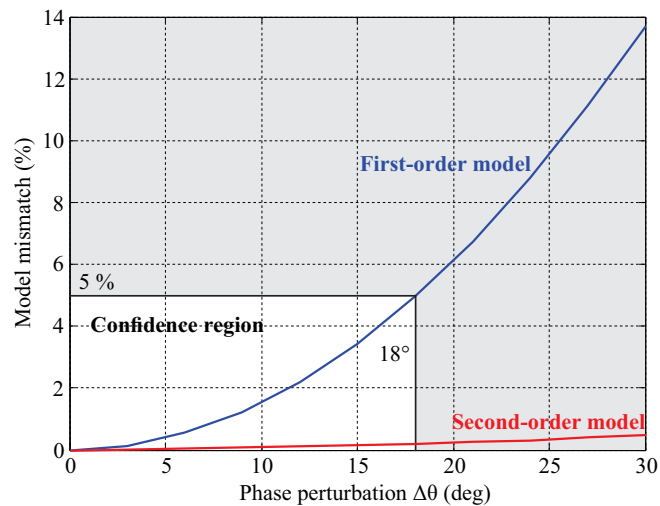
The accuracy of the proposed model during steady-state in frequency domain has been studied as well. By applying small phase perturbations at different frequencies to the grid angle, the model and simulation responses of the d - and q -axis currents can be obtained under frequency domain in the forms of spectrum. Under the circumstance, the mismatches of the conventional small-signal model and the proposed model would be identical, since the influences of the second-order terms are mainly on transients. Due to the filtering effect of the PLL PI controller, the phase perturbations beyond certain frequency (e.g., 350 Hz) have very limit effects on the system responses. In this evaluation, the phase perturbation at each frequency is 1 % of the phase angle of the grid voltage, and the frequency of the phase pertur-



(a)

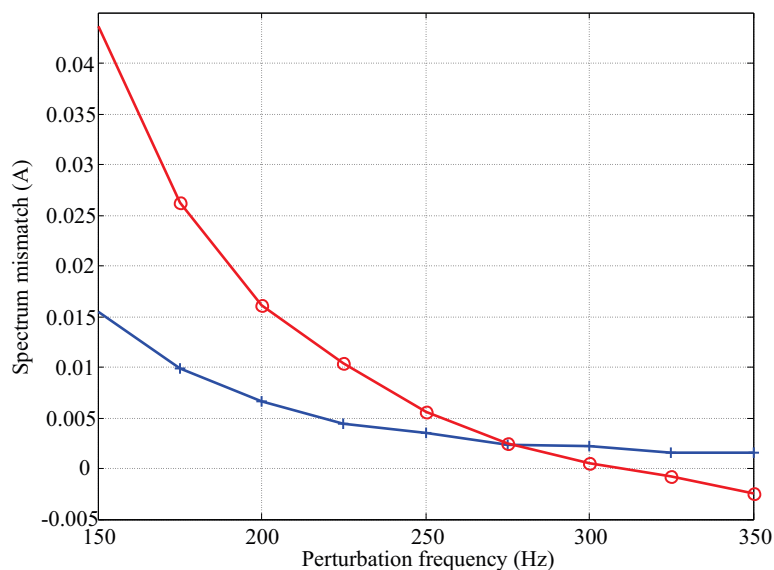


(b)

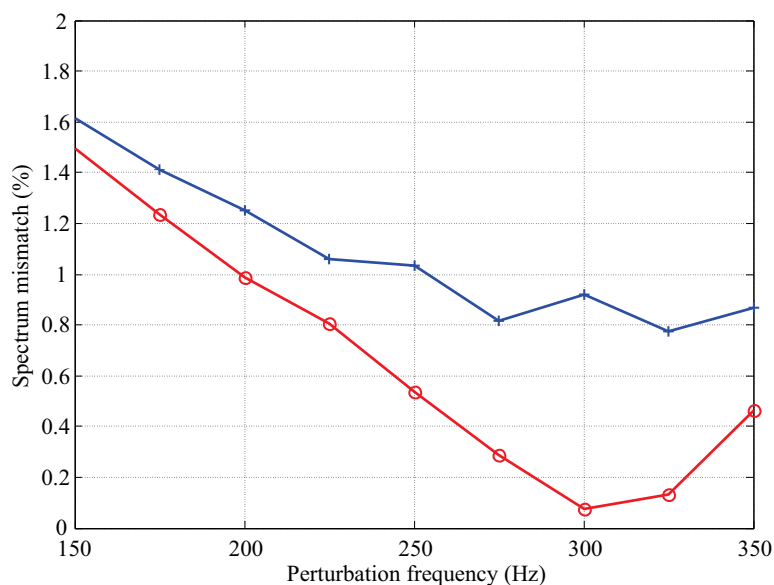


(c)

Figure 6.6: Model evaluations during phase perturbations: (a) active/reactive power curves with $\pi/18$ phase jump, (b) mismatches of first-order (blue curve) and second-order (red curve) small-signal models considering the PLL, and (c) active/reactive power curves with $\pi/6$ phase jump.



(a)



(b)

Figure 6.7: Spectrum mismatch in steady-state under different perturbation frequencies (blue - d -axis current, red - q -axis current): (a) mismatch values and (b) mismatch percentages.

bation is sweeping from 150 Hz to 350 Hz with 25 Hz step. The values and the percentages of spectrum mismatch (between model and simulation) are presented in Fig. 6.7a and Fig. 6.7b, respectively. The percentage of spectrum mismatch at each frequency is the mismatch value divided by the actual harmonic content at that frequency obtained from simulation. It can be seen that the values of spectrum mismatch within the frequency range are decreasing when the frequency increases. Nevertheless, it is worth noting that the harmonic contents excited by the perturbations are drastically decreasing because of the system attenuation. As a result, variations of the mismatch percentages can be observed in Fig. 6.7b when frequency exceeds 250 Hz. In general, spectrum mismatch within the sweeping frequency range is less than 2%, indicating an accurate estimation in frequency domain.

For stability assessment during large phase perturbation, the model of (6.18) has been taken into account. From comparisons, it is seen that (6.18) can well represent the characteristics of grid converter during phase jump, up to $\pm 38^\circ$ according to trigonometric basics. Nevertheless, due to the existence of the second-order terms, the transient behaviors during large phase jump was not included in the admittance matrix. In this regard, Taylor series linearization is utilized to the second-order terms within the valid phase region (i.e., $\pm 38^\circ$) to obtain a more accurate admittance matrix for stability assessment.

The second-order $\Delta\theta'$ -related term, provided the phase perturbation ($\Delta\theta_p$) is known, can be written at each operating point within the valid range by

$$\begin{aligned} \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} &\approx \begin{bmatrix} I_{dd} & I_{dq} \\ I_{qd} & I_{qq} \end{bmatrix} \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} Y_{dd}^{\theta 1} & Y_{dq}^{\theta 1} \\ Y_{qd}^{\theta 1} & Y_{qq}^{\theta 1} \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} + \begin{bmatrix} \Theta_{d2} \\ \Theta_{q2} \end{bmatrix} [\Delta\theta_p^2 + 2\Delta\theta_p(\Delta\theta' - \Delta\theta_p)] \\ &\approx \begin{bmatrix} I_{dd} & I_{dq} \\ I_{qd} & I_{qq} \end{bmatrix} \begin{bmatrix} \Delta i_{refd} \\ \Delta i_{refq} \end{bmatrix} + \begin{bmatrix} Y_{dd}^{\theta 2} & Y_{dq}^{\theta 2} \\ Y_{qd}^{\theta 2} & Y_{qq}^{\theta 2} \end{bmatrix} \begin{bmatrix} \Delta v_d \\ \Delta v_q \end{bmatrix} \end{aligned} \quad (6.19)$$

where

$$\begin{aligned} Y_{dd}^{\theta 2} &= Y_{dd}^{\theta 1}, Y_{qd}^{\theta 2} = Y_{qd}^{\theta 1}, \\ Y_{dq}^{\theta 2} &= Y_{dq}^{\theta 1} + 2\Delta\theta_p \Theta_{d2} G_{PLL,op}, \\ Y_{qq}^{\theta 2} &= Y_{qq}^{\theta 1} + 2\Delta\theta_p \Theta_{q2} G_{PLL,op}. \end{aligned} \quad (6.20)$$

6.3.2 Impedance-based Theory for Stability Analysis

The stability issues related to the synchronization can be analyzed by applying Nyquist stability criterion to the impedance ratio between grid impedance and grid converter impedance. For static stability analysis, the conventional small-signal model of (6.16) can be used for the stability assessment. Indeed, the stability analysis methodologies presented in the literature offer the possibility to well assess the system stability with the effects of synchronization. Nevertheless, all the above-mentioned methodologies rely on the small-signal impedance/admittance models and therefore are eligible for static stability analysis, for instance, harmonic stability assessment during steady state. When large phase perturbations happen, the proposed model including the second-order of the $\Delta\theta'$ -related terms of (6.20) have to be employed for characteristic evaluation and stability analysis.

In order to assess the system stability, the impedance-based stability analysis can be used and the impedance ratio between the grid impedance and the grid converter admittance can be defined by

$$\mathbf{L} = \mathbf{Z}_g \cdot \mathbf{Y}^{\theta 2} = \mathbf{Z}_g \cdot \begin{bmatrix} Y_{dd}^{\theta 2} & Y_{dq}^{\theta 2} \\ Y_{qd}^{\theta 2} & Y_{qq}^{\theta 2} \end{bmatrix} \quad (6.21)$$

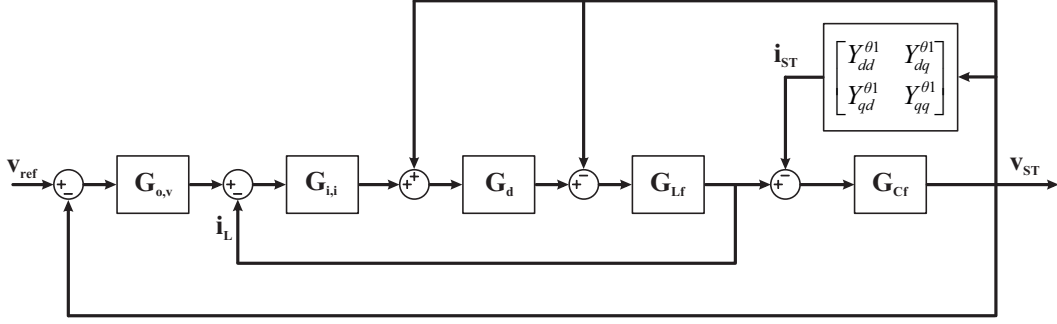


Figure 6.8: One line block diagram of ST LV control with the effects of LV grid.

where \mathbf{Z}_g is the grid impedance matrix. Applying generalized Nyquist criterion to the impedance ratio of (6.21), stability of the grid converter during large phase perturbation can be assessed, depending on whether the system characteristic loci encircles the critical point $(-1, j0)$.

6.4 Stability Analysis of ST-fed Grid Considering Synchronization

This section studies the stability issue of a ST-fed grid when considering the effects of PLL. The multiloop control scheme of ST shown in Fig. 4.6 with the measured voltage feedforward and the inductor-current feedback is used for ST LV control and its one line block diagram is shown in Fig. 6.8, where $\mathbf{G}_{o,v}$ and $\mathbf{G}_{i,i}$ indicate the transfer function matrices of the PI controllers of the outer- and the inner-loop in the dq frame, \mathbf{G}_d represents transfer function matrix of the computation and PWM delay. Considering the effects of the LV grid, the equivalent admittance matrix of the LV grid \mathbf{Y}_{eq} including various loads and grid converters is coupled in the block diagram. To better reveal the synchronization effects, a simplification has been made that only one grid converter is connecting to the ST LV converter, namely \mathbf{Y}_{eq} equals to $\mathbf{Y}^{\theta 1}$ given by (6.17).

Based on the one line diagram, one can get the expression of the open-loop transfer function matrix of the ST LV control as followings:

$$\mathbf{G}_{op} = \mathbf{G}_d \mathbf{G}_{o,v} \mathbf{G}_{i,i} \mathbf{G}_{Lf} \cdot [\mathbf{G}_{Lf} (\mathbf{I} - \mathbf{G}_d) + \mathbf{Y}_{eq} + \mathbf{G}_{Cf}^{-1} + \mathbf{G}_{Lf} \mathbf{G}_d \mathbf{G}_{i,i} (\mathbf{Y}_{eq} + \mathbf{G}_{Cf}^{-1})]^{-1}. \quad (6.22)$$

6.4.1 Impacts of PLL-based Synchronization on ST LV Converter

To investigate the stability issue regarding the impacts of grid synchronization, generalized Nyquist criterion can be applied to the ST open-loop transfer function matrix of (6.22). The system parameters used in the stability analysis are listed in Table 5.1. By changing the bandwidth of PLL, the influences and stability conditions are studied in the followings.

The system characteristic loci of \mathbf{G}_{op} are shown in Fig. 6.9. In this case study, PLLs with two different BWs (i.e., 20 Hz and 200 Hz) are applied to the grid converter. Seen from the Nyquist plots, it is obviously seen that the PLL has minor impact on one of the system

characteristic loci (λ_1), where the characteristic loci with different PLL BWs are almost overlapping in Fig. 6.9a. Both characteristic loci have no encirclement of the critical point $(-1, j0)$. On the other hand, it is seen that the PLL has strong effects on another of the system characteristic loci (λ_2) as shown in Fig. 6.9b. When a PLL with 20 Hz BW is used, as plotted by the blue curve, the Nyquist plot has no encirclement of $(-1, j0)$ showing the system is stable. However, when a faster PLL with 200 Hz BW is utilized, the Nyquist plot illustrated by the green curve has two clockwise encirclement of $(-1, j0)$, indicating the system presents an unstable behavior. As a result, it can be concluded that a higher bandwidth PLL could lead the ST-fed grid to unstable conditions, which is similar to the stability analysis reported in the conventional distribution grid.

As reported in [38], the increasing of PLL BW destabilizes the system due to the negative incremental resistor qq -axis impedance. To better reveal the PLL effects on ST-fed grid, the characteristics of the qq -axis of \mathbf{G}_{op} (i.e., $G_{op,qq}$) are studied. The root locus of the dominant poles of the $G_{op,qq}$ closed-loop transfer function is presented in Fig. 6.10, where the PLL bandwidth increases from 20 Hz to 200 Hz. It can be seen that a pair of conjugate poles gradually shift from the left half plane to the right half plane when increasing the PLL bandwidth, leading an unstable condition. Due to the poles locating at the high-frequency range, it is expected that the unstable behavior would be represented by the high-frequency distortion and oscillation.

6.4.2 Virtual-impedance-based Stabilization Method

As pointed out in the previous chapter, one of the indispensable services of ST is to reshape its output impedance to stabilize the LV grid, addressing the issues caused by the local DERs. With appropriate voltage control strategy, the ST LV converter is able to stabilize an unstable LV grid due to the PLLs of grid converters. From Fig. 6.10, the qq -axis subsystem does not have enough damping ratio when a high bandwidth PLL is applied. With this consideration, one intuitive way is to enhance the damping of the subsystem by using virtual impedance.

To achieve the target, a voltage control with the virtual impedance technique has been proposed and the schematic diagram is shown in Fig. 6.11, where a virtual resistor R_v is implemented in the q -axis controller of the ST voltage control. For the d -axis controller, since PLL has limited influence, it can remain the same as that of Fig. 6.8. With this configuration, the main features of the ST voltage control can be preserved while the feature of the q -related axis (i.e., dq - and qq -axis) would be altered in order to improve the stability. To show the effectiveness, the Nyquist plots of the system characteristic loci considering the stabilization method are investigated. One of the system characteristic loci (λ_1) is still insensitive and therefore the Nyquist plot resembles the one depicted in Fig. 6.9a, which does not encircle the critical point. Nevertheless, for another system characteristic loci (λ_2), the introduced virtual resistance could alter the encirclement of $(-1, j0)$ and thereby change the stability conditions. As shown in Fig. 6.12, where 200 Hz BW PLL is used, the Nyquist plot (green curve) has two clockwise encirclement of $(-1, j0)$ when the virtual impedance is not utilized.

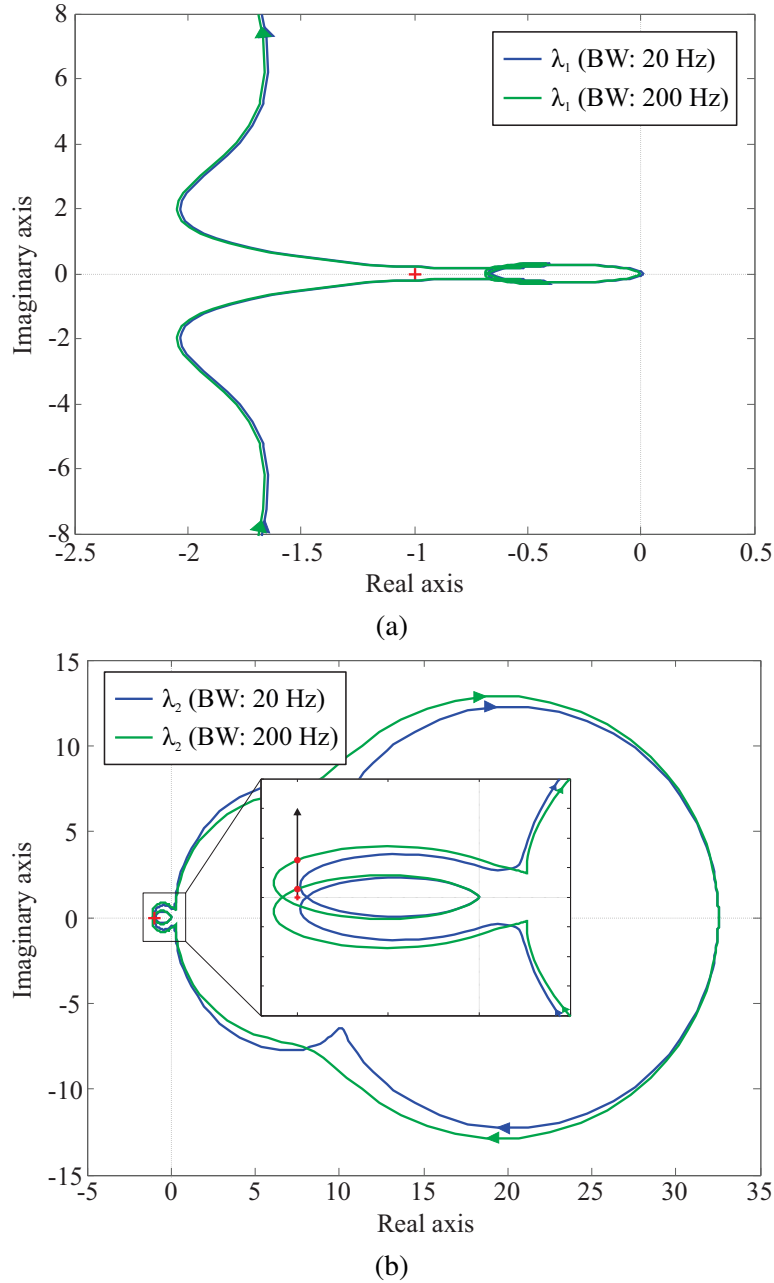


Figure 6.9: Stability analysis of characteristic loci of \mathbf{G}_{op} considering the effects of PLLs: (a) Nyquist plots of λ_1 when different bandwidth PLLs are applied and (b) Nyquist plots of λ_2 when different bandwidth PLLs are applied.

Then, a $2\ \Omega$ virtual resistor being plugged in, the Nyquist plot of λ_2 (magenta curve) has no encirclement of the critical point any more, showing a stable system has been achieved.

To well tune the virtual resistance, the root locus of the $G_{op,qq}$ closed-loop transfer function is presented in Fig. 6.13a, where the virtual resistance increases from 0.2 p.u. to 2 p.u. (base value is $2\ \Omega$). It is seen that the pair of conjugate poles move from the right half plane to the left half plane with the increasing of the virtual resistance, indicating the virtual impedance improves the stability and enhances the damping ratio of the system. A zoomed figure of the rectangular area of Fig. 6.13a is also presented in Fig. 6.13b. It can be observed that some of the dominate poles locating at the low-frequency range shift towards the imaginary

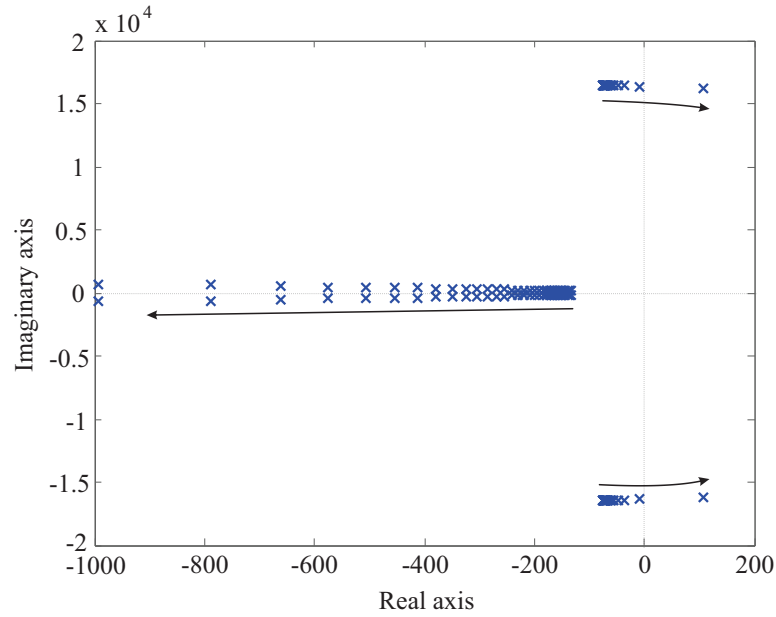


Figure 6.10: Root locus of qq -axis closed-loop transfer function when varying the PLL bandwidth.

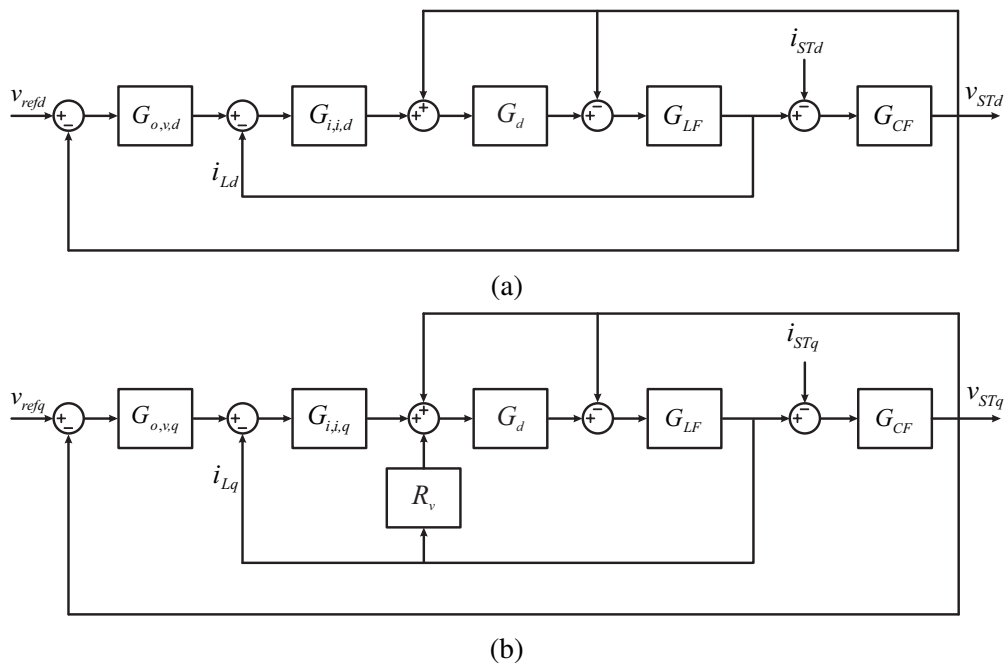


Figure 6.11: One line block diagram of the proposed voltage control of grid-forming converter for stabilization: (a) d-axis and (b) q-axis.

axis when a larger virtual resistance is used, meaning the minimum phase margin of the system is reducing. As a result, a trade-off must be made considering the characteristics of all dominant poles. With the aid of the Robust Control Toolbox™ of MATLAB/Simulink, R_d of [0.75 p.u., 1.3 p.u.] is recommended to obtain a minimum phase margin of 30° .

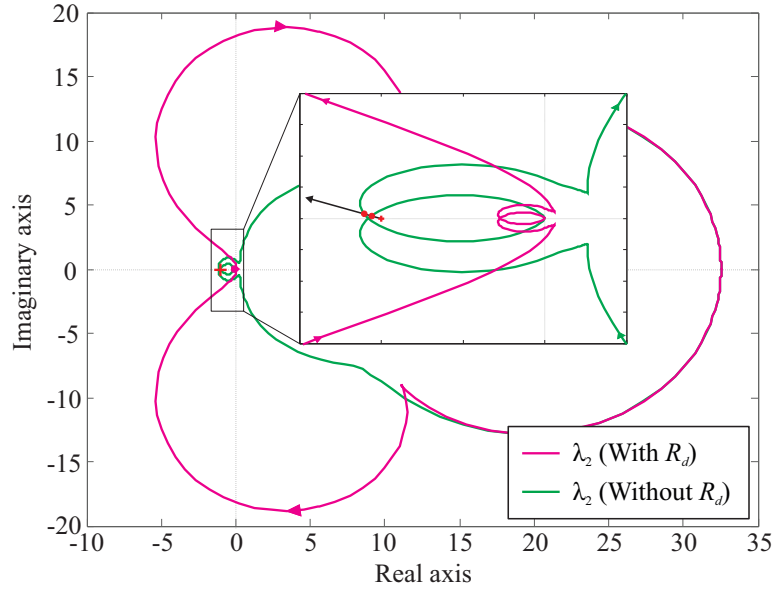


Figure 6.12: Nyquist plots of λ_2 with/without virtual resistance.

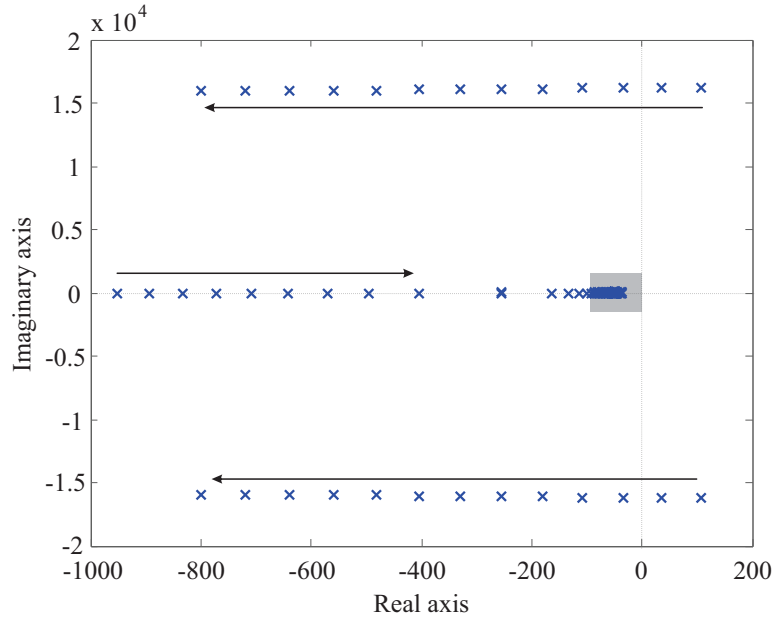
6.5 Simulation and Experimental Results

6.5.1 Case Study and Simulation Results

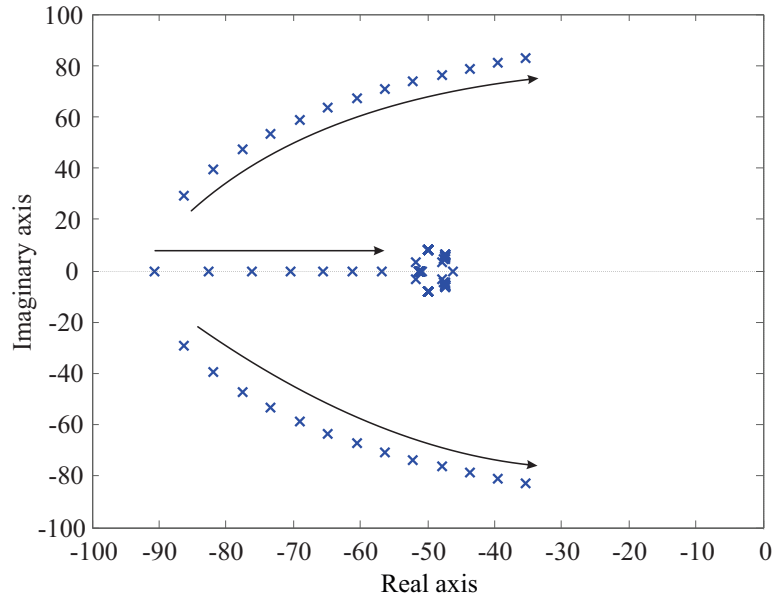
Two case studies are firstly carried out to evaluate the characteristics as well as accuracy of the proposed model. In the first scenario, delta control is employed by the grid converter, i.e. producing less power than what is available in order to have the possibility of providing an indirect reserve (0.75 p.u. in this scenario). The active and reactive power generation P_2 and Q_2 with delta control during large phase perturbation have been studied and shown in Fig. 6.14a. For comparison, the active and reactive power curves P_1 and Q_1 at nominal level (PF = 1, $P_1 = 1$ p.u.) are illustrated in the figure as well. Both the simulation results (solid curves) and the dynamic responses of the proposed model (dotted curves) are presented in the figure. It can be seen that the changing of active power injection would not only affect the undershoot of active power itself but also the overshoot of reactive power during phase jump. In this scenario, the responses of the proposed model are completely overlapping with the simulation results, showing the high accuracy of the proposed model during transients.

In the second scenario, reactive power compensation is used by the grid converter as an ancillary service, where the PF is 0.95 and the corresponding power curves P_2 and Q_2 with this service are given in Fig. 6.14b. Likewise, the active and reactive power curves P_1 and Q_1 at nominal level (PF = 1, $P_1 = 1$ p.u.) are illustrated for comparisons. Both the simulation results (solid curves) and the dynamic responses of the proposed model (dotted curves) are presented in the figure. It can be observed that the reactive power compensation can affect the undershoot of active power and the the responses of the proposed model well follow the simulation results.

Then, the stability of the grid converter during phase perturbation is studied by simulations. In the following simulations, the grid converter is operated at unity power factor and the



(a)



(b)

Figure 6.13: Stabilization of a ST-fed grid by using virtual resistor: (a) Nyquist plots of the ST voltage control system in q-axis with/without the virtual resistor, (b) pole map when tuning the virtual resistance, and (c) zoomed area of the pole map.

system parameters listed in Table 6.1 are used in the tests. To test the effectiveness of the proposed more accurate model as well as the proposed stability criterion, the grid inverter is connected to a conventional distribution grid where grid impedance in series with three-phase voltage source is used as an equivalence. The grid impedance used in the case studies is purely inductive, so that

$$\mathbf{Z}_g = \begin{bmatrix} L_g s & -L_g \omega \\ L_g \omega & L_g s \end{bmatrix} \quad (6.23)$$

where L_g is the grid inductance, which is 1.5 mH. A phase jump of $\pi/6$ is triggered from the

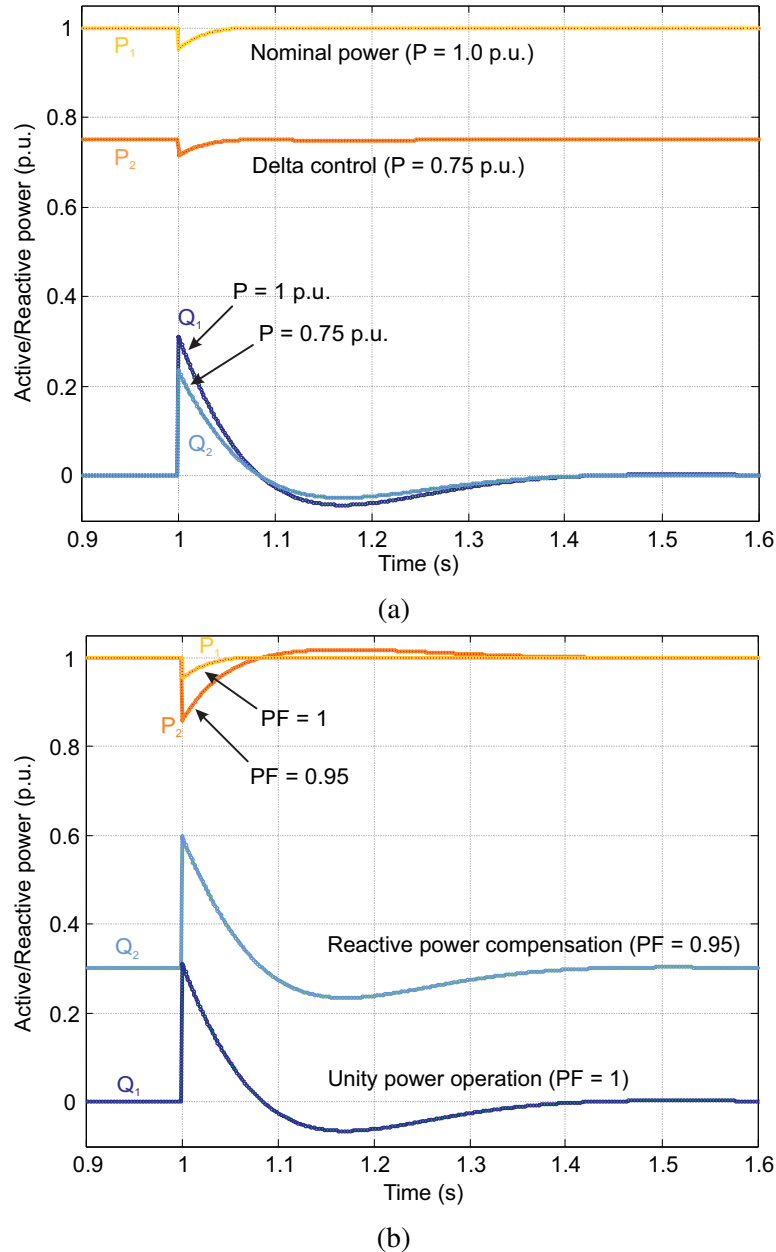


Figure 6.14: Evaluation of models with different scenarios during phase perturbation (solid lines: simulation waveforms, dotted lines: model responses): (a) delta control and (b) reactive power compensation.

grid side at $t = 0.5$ s and two case studies where the grid inverter uses different PLL BW are simulated.

First, a fast PLL (i.e., BW = 200 Hz) is utilized, the grid phase angle and inverter current waveforms before and after the phase jump are shown in Fig. 6.15a. It can be seen that the grid inverter is stable before the phase jump happens. However, the harmonic instability occurs represented by the harmonic oscillations in the inverter current after the phase jump happens. Then, a slow PLL (i.e., BW = 20 Hz) is utilized, the grid phase angle and inverter current waveforms before and after the phase jump are shown in Fig. 6.15b. Ignoring the current dynamics during the phase jump, the grid inverter is able to maintain stability entire the whole stage. The simulation results indicate that the grid inverter employing fast PLL is

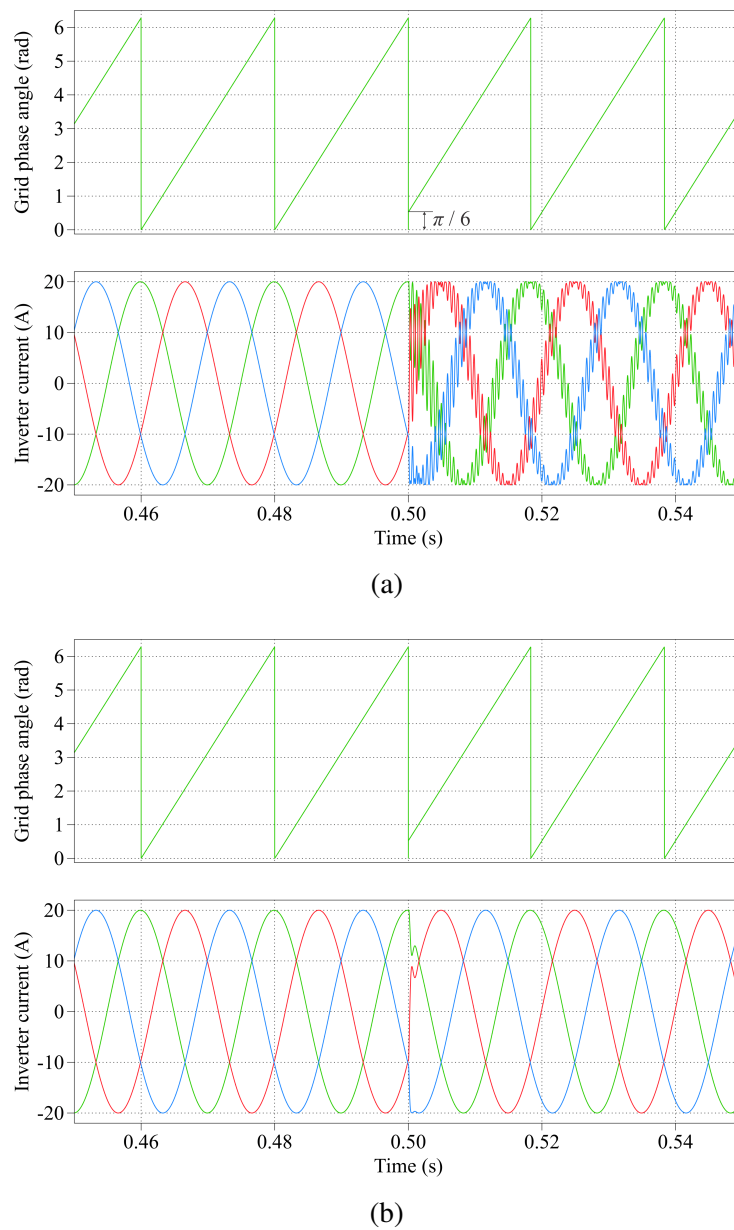


Figure 6.15: Simulation results of grid phase angle and inverter current during large phase jump: (a) with fast PLL, BW = 200 Hz and (b) with slow PLL, BW = 20 Hz.

more likely to suffer from stability issue during large phase perturbation.

The stability conditions of both cases are studied by using the proposed model of (6.18) and generalized Nyquist criterion. When the fast PLL (i.e., BW = 200 Hz) is used, the Nyquist plots of the system characteristic loci with the proposed model are shown in Fig. 6.16a. One of the system characteristic loci (λ_2) encircles the critical point $(-1, j0)$, which indicates the system is unstable during the phase jump. According to the harmonic stability classification [86], the instability in this case study is incurred by the higher PLL BW and therefore can be classified as the sideband harmonic instability. This type of harmonic instability would result in sideband oscillations [86, 87], which is consistent with the simulation results shown in Fig. 6.15a. When the slow PLL (i.e., BW = 20 Hz) is used, the Nyquist plots of the system

Table 6.2: Stability Boundary Versus PLL Bandwidth and Grid Phase Jump

PLL BW Phase jump	180 Hz	182.5 Hz	185 Hz	187.5 Hz	190 Hz	192.5 Hz	195 Hz
5 deg ($\pi/36$)	Stable	Stable	Stable	Stable	Stable	Unstable	Unstable
10 deg ($\pi/18$)	Stable	Stable	Stable	Unstable	Unstable	Unstable	Unstable
15 deg ($\pi/12$)	Stable	Stable	Unstable	Unstable	Unstable	Unstable	Unstable
20 deg ($\pi/9$)	Stable	Stable	Unstable	Unstable	Unstable	Unstable	Unstable
25 deg ($5\pi/36$)	Stable	Stable	Unstable	Unstable	Unstable	Unstable	Unstable
30 deg ($\pi/6$)	Stable	Unstable	Unstable	Unstable	Unstable	Unstable	Unstable

characteristic loci with the proposed model are shown in Fig. 6.16b. None of the system characteristic loci encircles the critical point, indicating system remains stable during the phase jump and the analysis is consistent with the simulation results shown in Fig. 6.15b. On the other hand, if the second-order terms are ignored, namely, the conventional small-signal model is taken for stability analysis, the Nyquist plots of the system characteristic loci for the fast and slow PLL case studies are shown in Fig. 6.17a and Fig. 6.17b, respectively. When the fast PLL is used, from Fig. 6.17a, it can be observed that none of the system characteristic loci encircles the critical point, indicating the system is stable while the fact is not. When the slow PLL is used, from Fig. 6.17b, none of the system characteristic loci encircles the critical point, indicating the system is stable, like the prediction of Fig. 6.16b as well as the simulation result. In this regard, it is shown that the stability analysis based on the conventional small-signal model can not accurately assess the stability condition during large phase perturbation. Especially when the actual system is unstable, the conventional small-signal model could misjudge the system stability.

The stability boundary versus the variations of PLL BW and phase jump of grid voltage is shown in Table 6.2, where the green region is the stable region, the red region indicates the system is unstable. It can be seen that the system stability is determined by both the PLL BW and the grid phase perturbation. With the increasing of the BW and phase jump, the system is less likely to be stable when a phase perturbation occurs. In this case study, the system can maintain stability up to 30° phase perturbation when the PLL BW is lower than 180 Hz.

The effects of PLL on the stability of ST-fed grid are validated and the proposed stabilization method is tested here as well. In Fig. 6.18a, the system is initially stable where the PLL BW is 20 Hz. At $t = 0.5$ s, the BW of the PLL jumps from 20 Hz to 200 Hz, it can be seen that both the ST voltage and current begin to oscillate when a higher BW is applied. The effectiveness of the proposed stabilization method is shown in Fig. 6.18b, where still the 200 Hz BW PLL is utilized. The virtual impedance of 2Ω has been implemented in the beginning and been plugged out since $t = 1$ s. It is seen that the system can maintain stability even a high BW PLL is used when the virtual impedance has been plugged in, while it turns to be unstable as soon as the virtual impedance being removed.

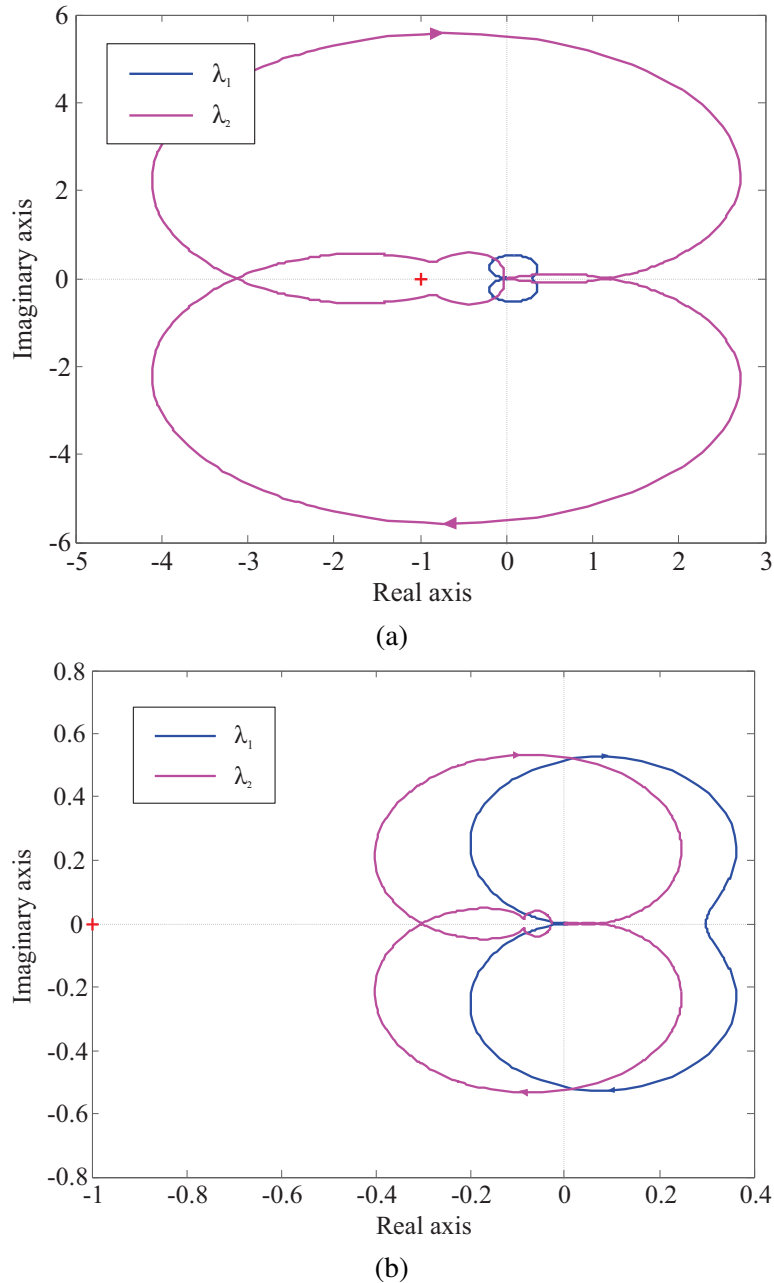


Figure 6.16: Nyquist plots of system characteristic loci when a large phase perturbation occurs: (a) fast PLL case assessed by the second-order model, corresponding to results of Fig. 6.15a and (b) slow PLL case assessed by the second-order model, corresponding to results of Fig. 6.15b.

6.5.2 Experimental Validations

To better validate the model accuracy, an experimental setup consisting of two commercial inverters has been developed in the laboratory. The system configuration is presented in Fig. 6.19b: two Danfoss FC302 inverters are used, one for the grid emulator and the other for the grid-tied inverter. Firstly, to evaluate the proposed higher accurate model and the proposed stability criterion, an open-loop voltage control scheme is adopted for the grid emulator to avoid the control interactions between two inverters, the closed-loop current control scheme of Fig. 6.4b is implemented in the grid-tied inverter. A dSPACE 1006 is used to

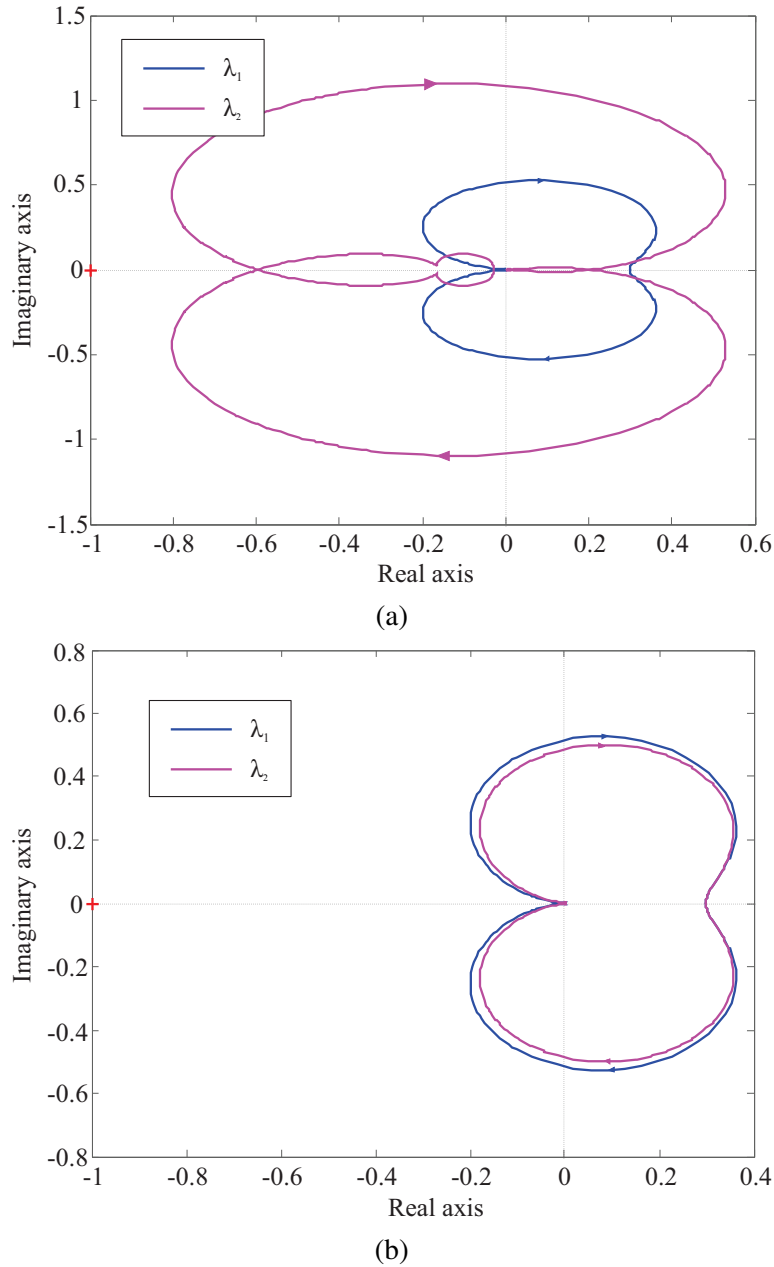
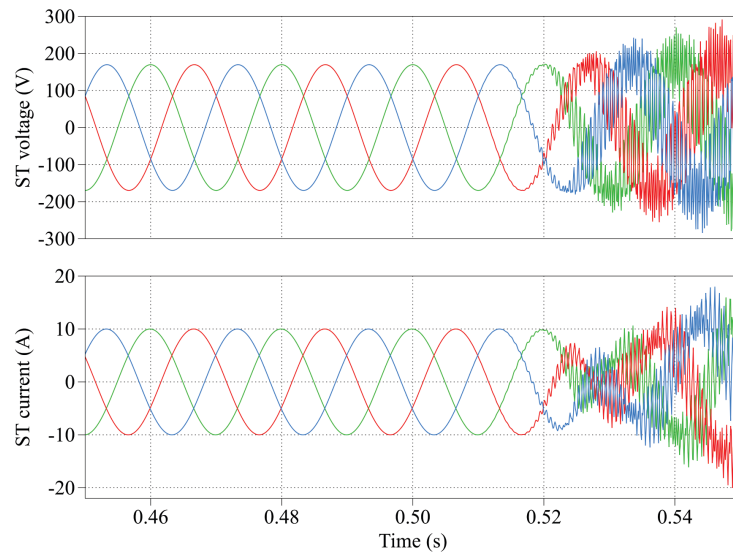


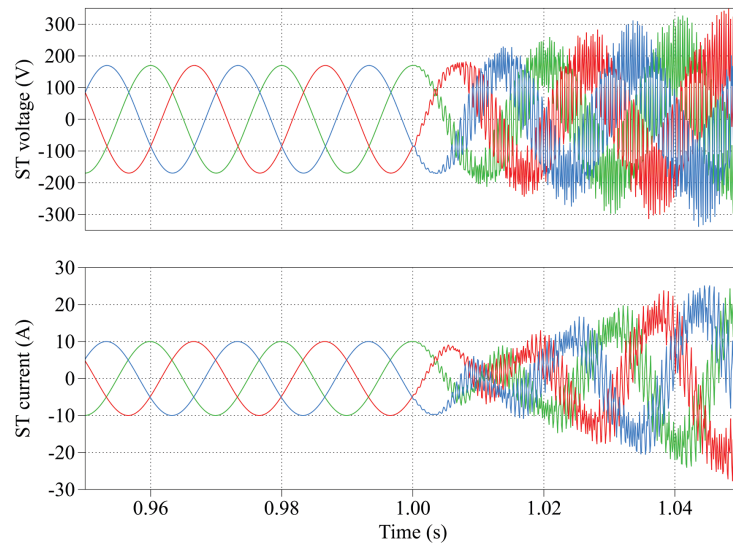
Figure 6.17: Nyquist plots of system characteristic loci when a large phase perturbation occurs: (a) fast PLL case assessed by the conventional small-signal model and (b) slow PLL case assessed by the conventional small-signal model.

achieve the control strategies as well as signal processing in real-time. The system parameters listed in Table 6.1 are used in the experimental tests.

In the experimental test, the grid inverter is operated at its nominal level ($\text{PF} = 1$, $P_1 = 1$ p.u.). Two phase jumps: $\pi/18$ and $\pi/6$, are triggered by the grid emulator at $t = 1$ s. The experimental waveforms and the model responses under the two phase jumps are shown in Fig. 6.20 and Fig. 6.21, respectively. In Fig. 6.20a and Fig. 6.21a, the three-phase PCC voltage waveforms before and after the phase jumps are presented. It can be seen that the voltage amplitudes before and after the phase jumps are identical, avoiding the influences of the forward gain of V_d on the model validation. The d/q components of inverter current mapped by the



(a)



(b)

Figure 6.18: Simulation results of ST voltage and current under different conditions: (a) PLL bandwidth jump, from 20 Hz to 200 Hz and (b) with/without the virtual resistor.

synchronous frame and the active/reactive power generation with a phase jump of $\pi/18$ are evaluated in Fig. 6.20b and Fig. 6.20c. The responses of the proposed model (red curves) and the conventional small-signal model (green curves) are compared with the experimental results (blue curves). Noting that, the current and power curves oscillations are utterly different from the oscillations seen in Fig. 6.15a. The oscillations here are due to the harmonic contents as well as ripples after the Park transform or the power calculation, whose frequencies are relatively low, and in practical they can be easily removed by low-pass filters. It is shown that, for both active/reactive power generation and the d/q current components, the responses of the proposed model can well follow the experimental waveforms, while the responses of the conventional small-signal model can not (in particular the responses of the d -component of current and the active power), indicating the proposed model can better describe the static

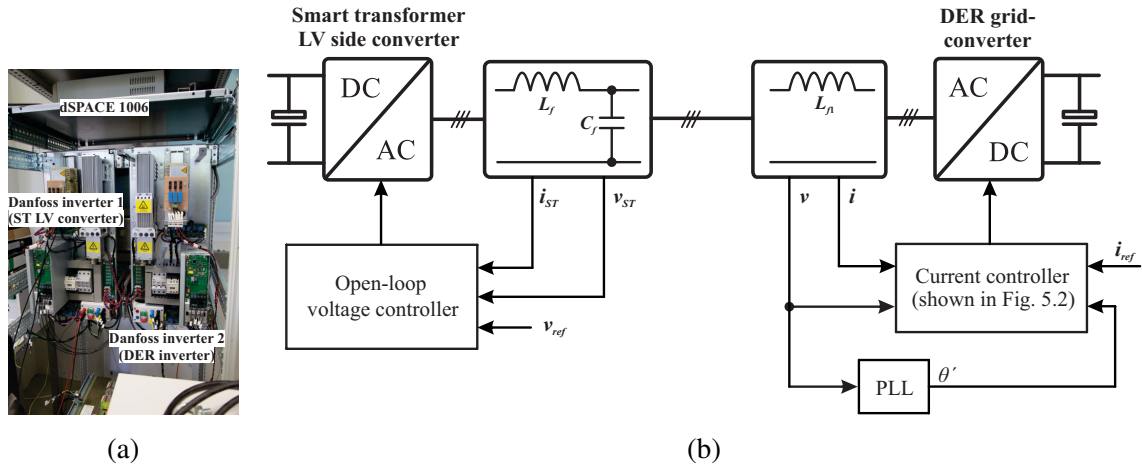
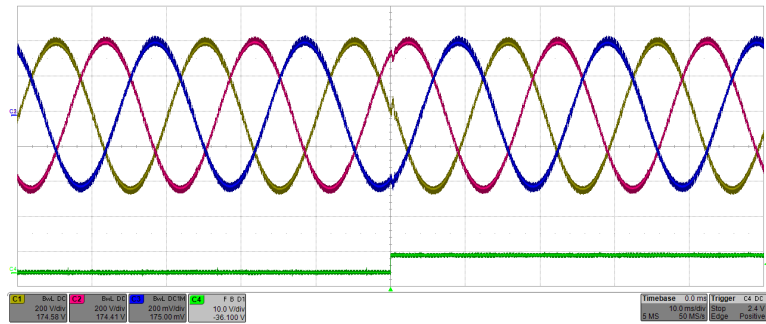


Figure 6.19: Laboratory setup: (a) photo and (b) configuration and control schematics.

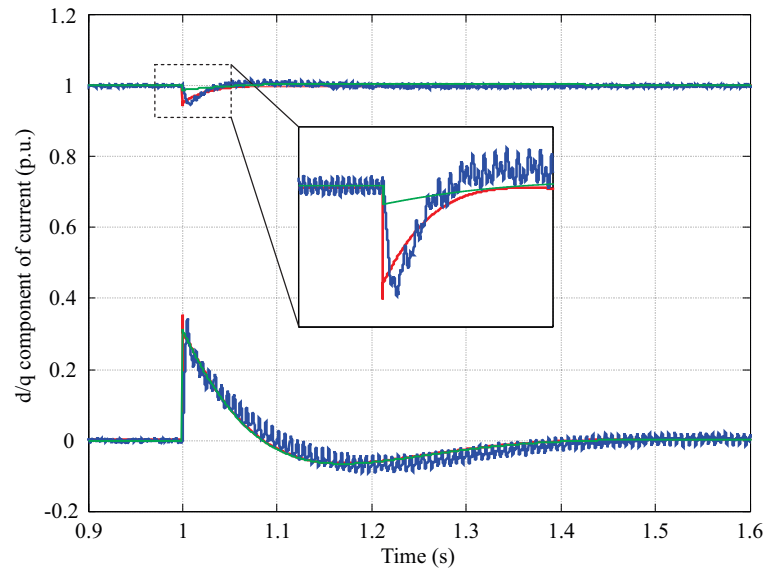
and dynamic behaviors of a grid inverter. With a phase jump of $\pi/6$, the d/q components of inverter current mapped by the synchronous frame and the active/reactive power generation are evaluated in Fig. 6.21b and Fig. 6.21c. Likewise, the responses of the proposed model can follow the experimental waveforms, but the conventional small-signal model can not.

The two case studies shown in simulation subsection are tested by the experimental setup and the results are shown in Fig. 6.22. To well indicate the phase perturbation, the phase jump signal is shown in the figures with green curves. A fast PLL (i.e., BW = 200 Hz) is used in the first case study and a phase jump of $\pi/6$ happens during the unity power grid-connected operation. From Fig. 6.22a, the grid inverter is stable initially where the three-phase inverter current is balanced and sinusoidal. After the phase jump happens, the system turns to be unstable and the inverter current starts to oscillate, which fits the simulation results and the stability analysis. In the second case study, a slow PLL (i.e., BW = 20 Hz) is used for the grid inverter and a phase jump of $\pi/6$ happens during the normal operation. From Fig. 6.22b, it can be seen that the current of the grid inverter can maintain stable before and after the phase jump, except one cycle of transients. The results of the second case study fit with the previous simulation results and stability analysis as well. The zoomed current waveforms of the two case studies in steady-state after the phase jump are shown in Fig. 6.23, which further reveal the current behaviors using different PLL BWs.

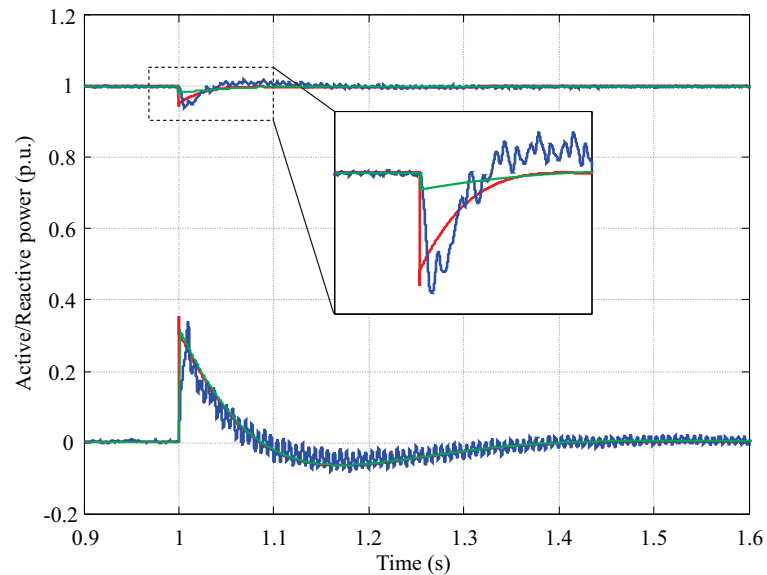
Secondly, the impacts of PLL BW on the stability of ST-fed grid are tested and the proposed stabilization method is verified. The proposed voltage control of Fig. 6.11 is employed for the ST LV converter, implementing in the dSPACE. Fig. 6.24a shows the experimental results when the bandwidth of PLL changes. In the beginning, the ST-fed grid is running under stable conditions according to the waveforms of the PCC voltage, the DER current, and the PLL phase angle. At the moment (that indicated by the dashed line), the bandwidth of the PLL increases from 20 Hz to 150 Hz; the PCC voltage, the DER current and the PLL phase angle start to oscillate, showing the overall grid becomes unstable. In order to stabilize the grid, a virtual resistor (4Ω) has been plugged into the q-axis controller at the dashed line of Fig. 6.24b. The green curve represents the signal of turn on/off the virtual resistor: low level - off, high level - on. Seen from Fig. 6.24b, all the waveforms including the PCC voltage,



(a)

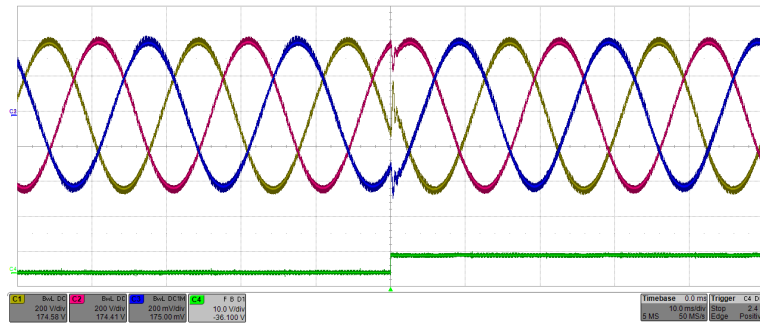


(b)

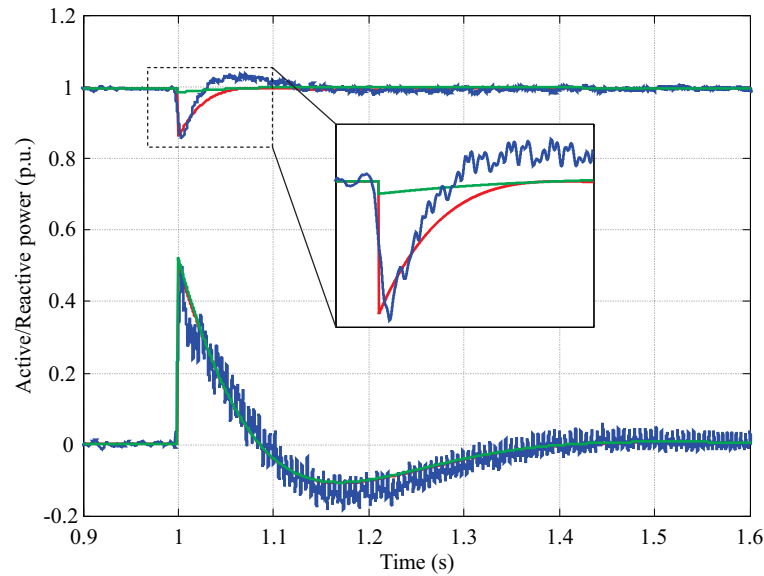


(c)

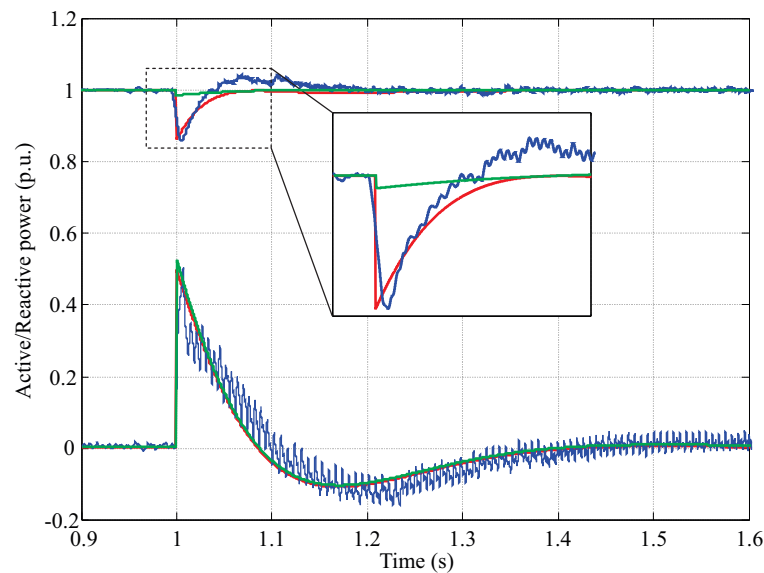
Figure 6.20: Comparisons among responses of the proposed model (red), conventional small-signal model (green), and experimental results (blue) with a phase jump of $\pi/18$: (a) three-phase PCC voltage during perturbation (time: 10 ms/div, voltage: 200 V/div), (b) d and q components of inverter current mapped in the synchronous frame of grid, and (c) active and reactive power of inverter.



(a)



(b)



(c)

Figure 6.21: Comparisons among responses of the proposed model (red), conventional small-signal model (green), and experimental results (blue) with a phase jump of $\pi/6$: (a) three-phase PCC voltage during perturbation (time: 10 ms/div, voltage: 200 V/div), (b) d and q components of inverter current mapped in the synchronous frame of grid, and (c) active and reactive power of inverter.

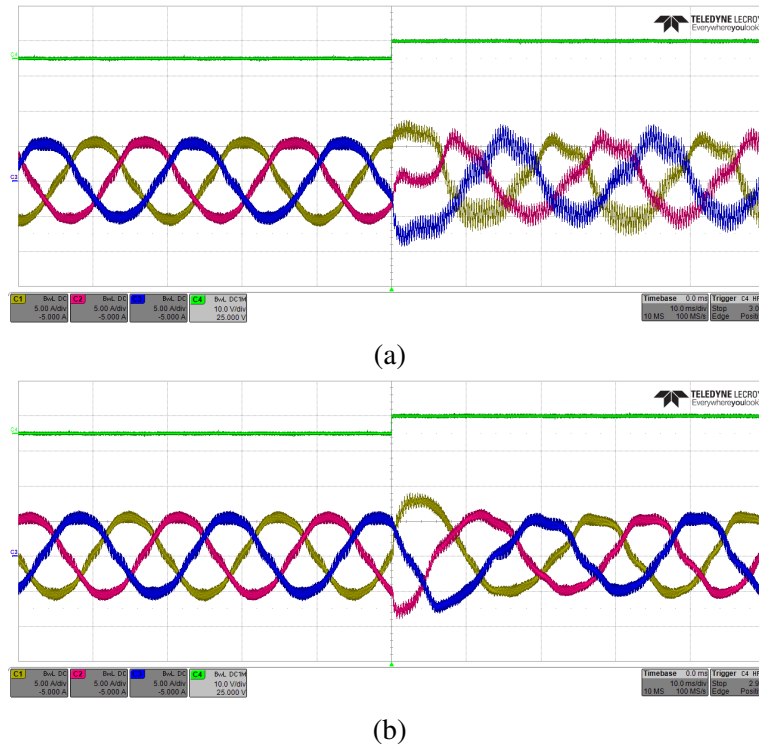


Figure 6.22: Experimental results of inverter current before and after phase jump (time: 10 ms/div, three-phase current: 5 A/div, green curves: low level - before phase jump, high level - after phase jump): (a) PLL BW 200 Hz and (b) PLL BW 20 Hz.

the DER current, and the PLL phase angle gradually stop oscillation after the virtual resistor being turned on, showing that the overall grid becomes stable.

6.6 Summary of the Chapter

This chapter studies the modeling of the PLL-synchronized grid converter and the effects of PLL-based synchronization on the system stability, in particular on the stability of a ST-fed grid. Different from the models in the literature, the proposed model is able to well describe the system features both in steady state and transient in terms of phase perturbation. In particular, the proposed model can accurately represent the characteristics of the grid converter during phase perturbation up to 38° with 1 % model mismatch, while the conventional small-signal model can only reach 7° with 1 % model mismatch or 15° with 5 % mismatch. Based on the proposed model, impedance-based stability criterion can be easily derived and used to assess the stability conditions of either conventional distribution grid or ST-fed grid, with high penetration of PLL-synchronized grid converters. The Nyquist analysis and results show the limitation of the conventional model as well as stability criterion, and verify the effectiveness of the proposed model and criterion in terms of accurate assessment, when a large phase perturbation happens.

Likewise conventional distribution grid, higher BW PLL is more likely to incur harmonic instability in a ST-fed grid, due to the insufficient damping ratio in the qq -axis. Fortunately,

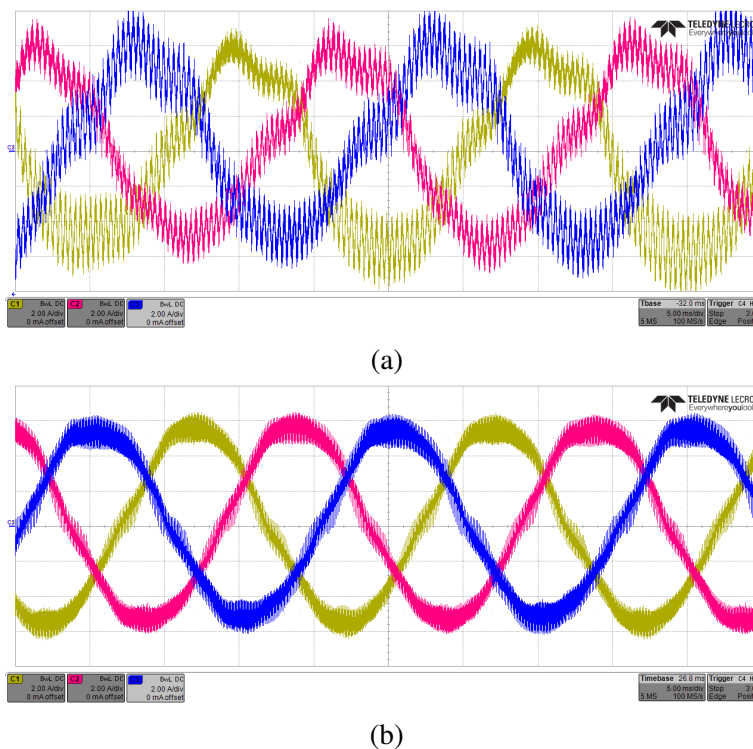
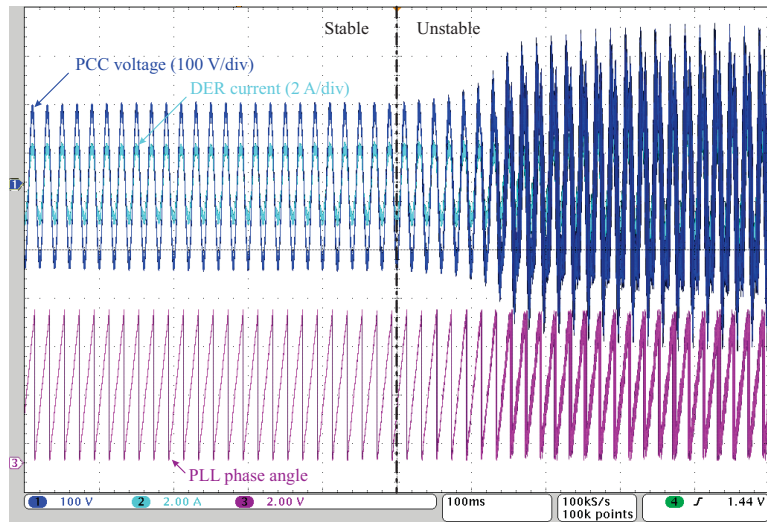
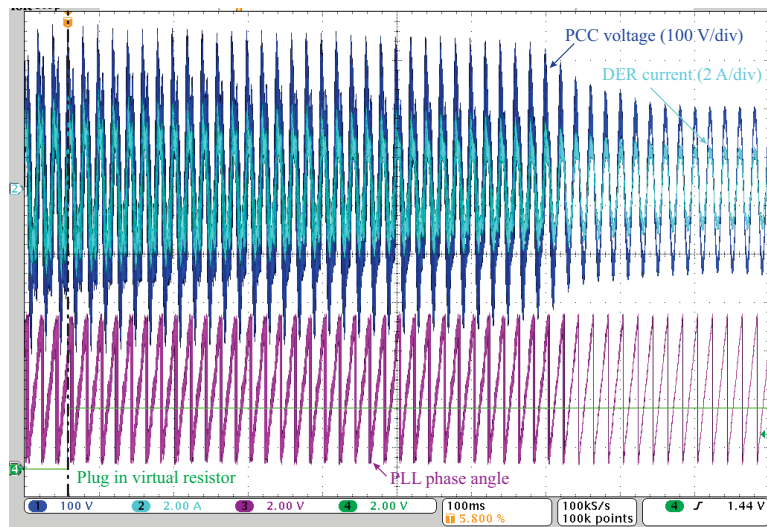


Figure 6.23: Zoomed experimental results of inverter current in their steady-state after phase jump (time: 5 ms/div, three-phase current: 2 A/div): (a) PLL BW 200 Hz and (b) PLL BW 20 Hz.

the instability caused by the local grid converters can be alleviated by using proper voltage control in ST. Under this circumstance, a stabilization method based on the virtual impedance is proposed and can be seamlessly implemented in the voltage control of ST LV converter, which can effectively address the stability issues caused by the synchronization of local converters. Simulation and experimental results are given to verify the effectiveness of the analysis as well as the stabilization method.

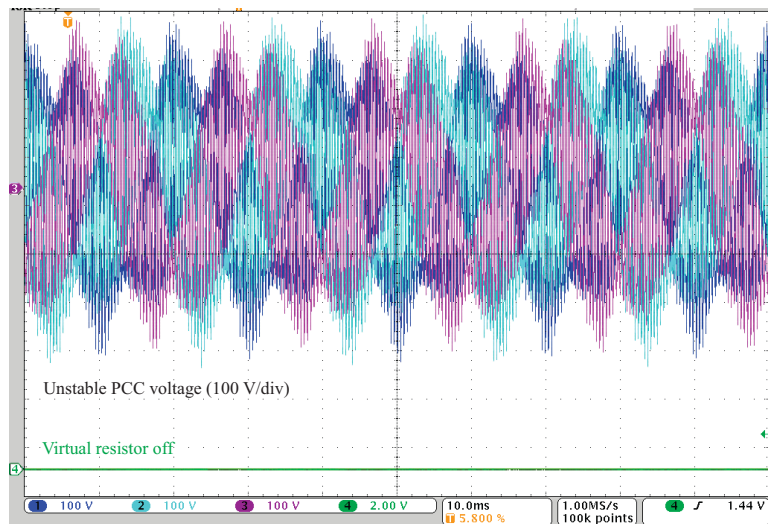


(a)

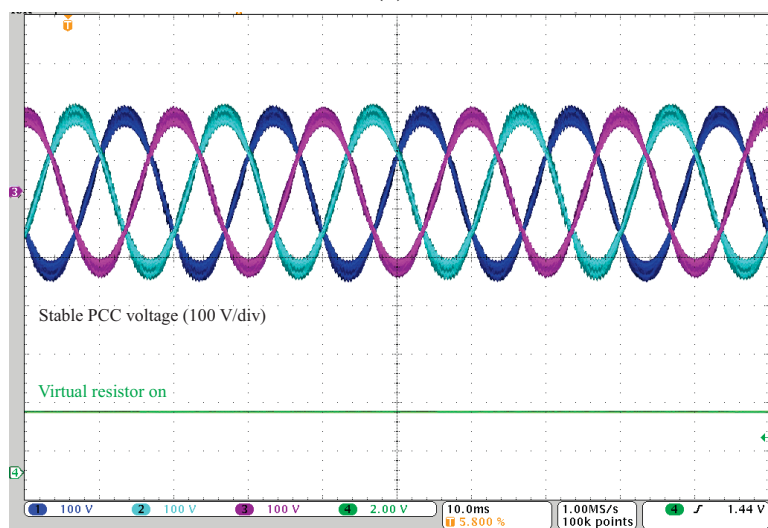


(b)

Figure 6.24: Experimental waveforms of the PCC voltage (blue), the DER current (aqua-marine), and the PLL phase angle (magenta) under different conditions (100 ms/div): (a) increasing of the PLL bandwidth and (b) plug in the virtual resistor.



(a)



(b)

Figure 6.25: Experimental waveforms of the zoomed three-phase PCC voltage (10 ms/div): (a) unstable case (without virtual resistor) and (b) stable case (with virtual resistor).

7 Frequency Adaptive Control of Smart Transformer-fed Grid

On the basis of stable operation, a ST-fed grid provides ancillary services to utilities and end customers, improving the hosting capacity and further exploring grid potential. Frequency control is the promising solution to achieve the grid service which deals with the overload and reverse power flow issues caused by the high penetration of DERs. However, the frequency control challenges the control performance of the ST voltage control as highlighted in Fig. 7.1. This chapter starts with the control issues during overload and reverse power flow in a ST-fed grid and then the solution of frequency adaptive control is proposed, along with detailed control architecture in grid level and a frequency adaptive control strategy - FORC - in the device level.

7.1 Control Challenges During Overload and Reverse Power Flow

As mentioned previously, ancillary services can be provided by means of the ST LV converter to address the grid issues, like overload and reverse power flow. Thanks to the dc-link capacitors, the MV and LV grids are decoupled by the ST from the voltage and frequency point of view. One of the possible scenarios is to adapt the LV frequency in order to interact with the frequency-dependent DERs and loads in distribution grids [24]. The idea is to modify the power sharing between ST and DERs by means of the ST frequency control with two goals: 1) the current flow through the ST can be limited so that overload can be avoided [88]; 2) the reverse power flowing of the distribution grid can be avoided [24].

Similar ideas have been applied for energy saving purposes, such as the conservation voltage reduction (CVR) method [89]. Unlike the proposed scenario for ST, the CVR is applied in steady state and not during transients, and the current value is not controlled during the voltage variation. A possible solution to solve the conventional transformer overload is given in [90]: the transformer tap changer and the implementation of P/V droop controller in the DER has been used to modify the voltage and following the power injection of DER in a microgrid. Nevertheless, no extensive research has been performed until now regarding the overload control and reverse power flow issue of the ST-fed grid or SST LV side.

One of the main challenges of frequency control is to regulate ST voltage and DER current waveforms under variable frequencies. The design of the controller of a power converter in traditional distribution grid/microgrid usually assumes signals with specific fundamental frequency (e.g., 50/60 Hz signal) and offers good voltage/current control performance as well as harmonic elimination under nominal frequency condition [91]. In case of grid with variable frequencies, for example in a ST-fed distribution grid, some of the conventional control strategies as well as design criteria may lead to performance degradation. There are several conventional frequency-adaptive control strategies including: hysteresis control [92], deadbeat control [93], PI control and PR control with frequency adaptivity [94], which could independently maintain their performance of grid frequency to some extent. Nevertheless,

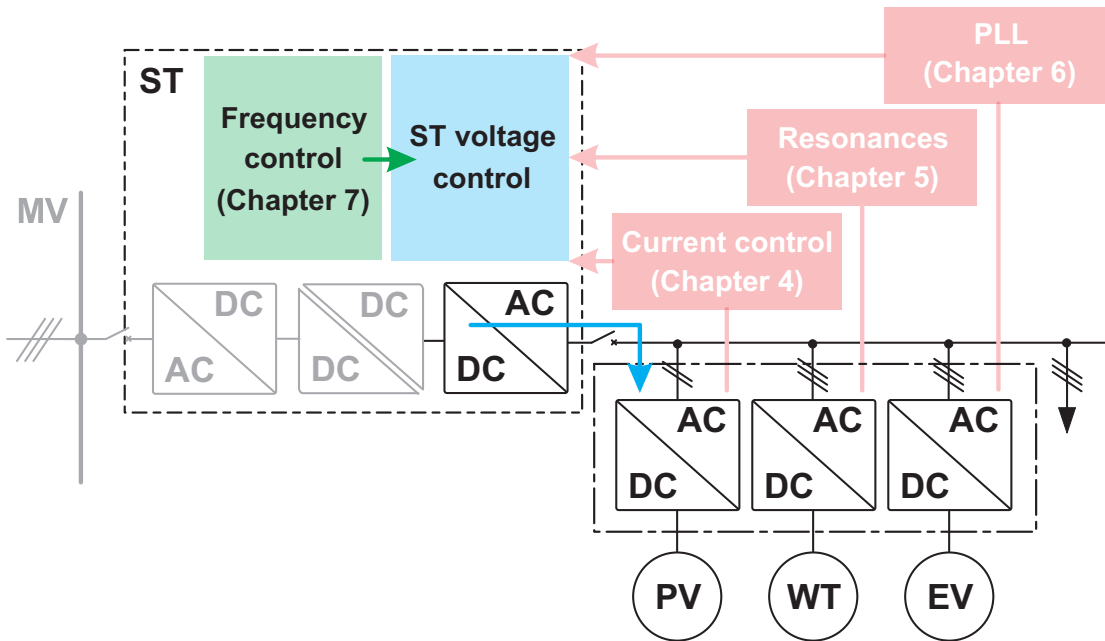


Figure 7.1: Research focus of Chapter 7: impacts of frequency control on the ST voltage control.

these methods have drawbacks: the hysteresis control can suffer from high switching stress or inaccurate harmonic elimination due to its nonlinear nature; the deadbeat control is sensitive to the accuracy of system parameters; both PI and PR with frequency adaptivity can well handle the fundamental frequency signals but may not perform optimally in case of high harmonic content. Multiple resonant controllers with frequency adaptivity can indeed achieve good tracking ability at selective harmonic frequencies, however it is computational heavy and complex to tune. Based on the internal model principle (IMP), repetitive control offers a simple way to achieve zero steady-state error tracking of any periodic signal with a known period due to the introduction of high gains at interested harmonic frequencies [95], but the conventional repetitive control (CRC) with fixed sampling rate is sensitive to the frequency variation from the harmonic control point of view. In the context, a simple and compact structure frequency adaptive FORC scheme has been proposed [96], derived from the IMP and able to provide high control performance with arbitrary frequency. Several case studies on FORC-controlled systems have been proposed in literature for different applications, such as programmable AC power supply [96], grid-connected power converter [97], and active noise cancellation [98].

In this application, a FORC plus PI along with fast frequency detection scheme is proposed and has been implemented in both ST and DERs to achieve a frequency-adaptive distribution grid. Equipped with the proposed scheme, the ST-fed distribution grid is able to modify online the generator production and load consumption by changing LV grid frequency, while maintaining good voltage/current waveforms under variable frequency condition. Moreover, this chapter proposes a comprehensive design of the frequency-adaptive control systems for ST-fed grid, and investigates on stability issues that may arise in certain operative conditions. To study the effects of synchronization on the system stability, a complete analysis consider-

ing the FORC and the PLL is given. Experimental results have been provided to validate the control strategies experimentally, using commercial converters as power-electronics components of the system.

7.2 Frequency Adaptive ST-fed Distribution Grid

Differently from the traditional transformer-fed grids, a ST-fed distribution grid offers advanced control capability and ancillary services to the overall system. The ST can modify the frequency of LV grid within the allowed limits of the local grid codes and interact with the droop controlled-DERs as well as frequency-dependent loads (e.g., induction motors). By changing the frequency, the injected/consumed power of generators/loads can be varied. The typical power/frequency characteristics of DER and loads in a distribution grid are shown in Fig. 7.2, in which the DER and loads characteristics are represented by the red and blue curves, respectively. It is seen that the power electronics-interfaced DER with droop control reproduces the $P - f$ droop behavior of synchronous generators used in conventional power system [99].

The ST can deploy a frequency control to modify the power sharing in the distribution grid, demanding a variation of the power set-points of local DERs. As presented in [91], the grid converters of DERs can be classified as: grid-feeding power converter and grid-supporting power converter. The latter one has the main task to supply the local load imposing the voltage, and can absolve complementary tasks, like grid support services. Among these, the DG power control by means of frequency variation is present. A droop curve allows the DER to output a given amount of power to the grid for regulatory purposes. In the case of a load increase and current exceeding the ST security limit, the frequency control decreases the frequency in the LV grid. The droop controllers of DERs correspondingly react to the frequency variation and increase the active power generation (assuming the DERs operates at unity power factor), while the frequency-dependent load demand decreases following its $P-f$ characteristic. On the other hand, when the generation of DERs is higher than the load demand and the storage rating, the frequency control increases the LV side frequency to allow the reduction of DERs production and the increase of load consumption. As an example of the proposed method, in Fig. 7.2 the distribution grid has its initial equilibrium at point A. When a change from curve 1 to curve 2 in the electric demand occurs (point $A \rightarrow B$), with a power increase of ΔP_0 , the frequency control decreases the frequency from ω_1 to ω_2 . Finally, the system reaches a new equilibrium point (i.e., point C) and an eventual overload of the ST can be avoided. Within this context, the frequency-adaptive ST-fed distribution grid shows two main advantages: 1) can mitigate overloading issue; 2) can reduce the power rating of controllable load and storage systems.

The simplified system configuration of a ST-fed distribution grid with frequency control is given in Fig. 7.3, which is composed of 1) the LV side ST and its voltage controller, and 2) the DER and its current controller. Z_f, Z_{ff} are the output filters of ST LV side, and DER, Z_l and Z_{ll} are the equivalent line impedances. Droop controllers based on power-frequency curves

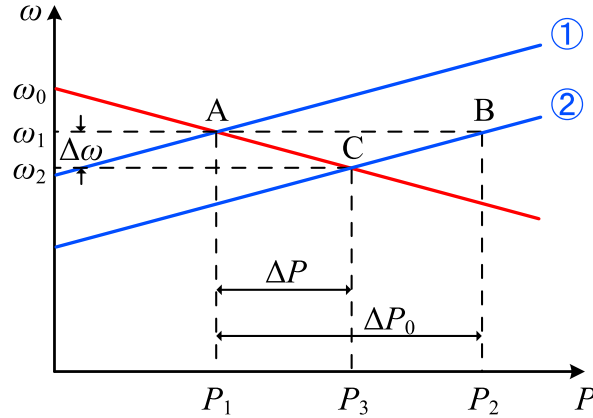


Figure 7.2: Typical steady-state power-frequency curves of DER (red curve) and loads (blue curves).

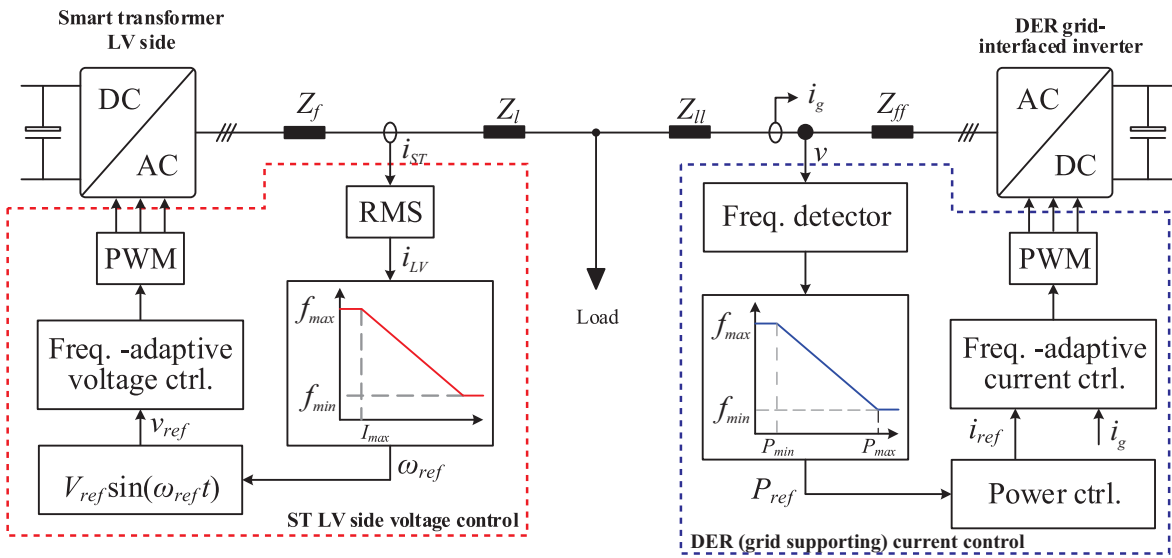


Figure 7.3: Schematic diagram of a frequency-adaptive ST-fed distribution grid.

have been employed in both the ST LV side voltage control and the DER power/current control: for the ST voltage control, the droop control provides the frequency set-point for the grid according to the ST output power; for the DER power/current control, the droop control determines the DER active power set-point according to the grid frequency.

To better illustrate the scheme, an overloading scenario is given as an example shown in Fig. 7.4. During the normal operation, namely i_{ST} within the safe range, the LV grid frequency is kept constant at the nominal value (e.g., 50 Hz). When the load increases, i_{ST} increases as well, and the frequency of LV side voltage is modified according to the droop curve, with a frequency range from 49 Hz to 50 Hz in this scenario. As shown in Fig. 7.4a, the frequency controller is activated as soon as the rms value of i_{ST} exceeds the security limit, namely 80 % of the maximum current limit. If the size of the controllable DER is not sufficient or the frequency droop hits the minimum frequency limit (e.g., 49 Hz), the current rises until it reaches 90 % of the maximum limit then activates the voltage droop. In this example, the ST decreases the voltage amplitude to keep the current within the allowable range. In case the current reaches the maximum current limit, despite the overload action,

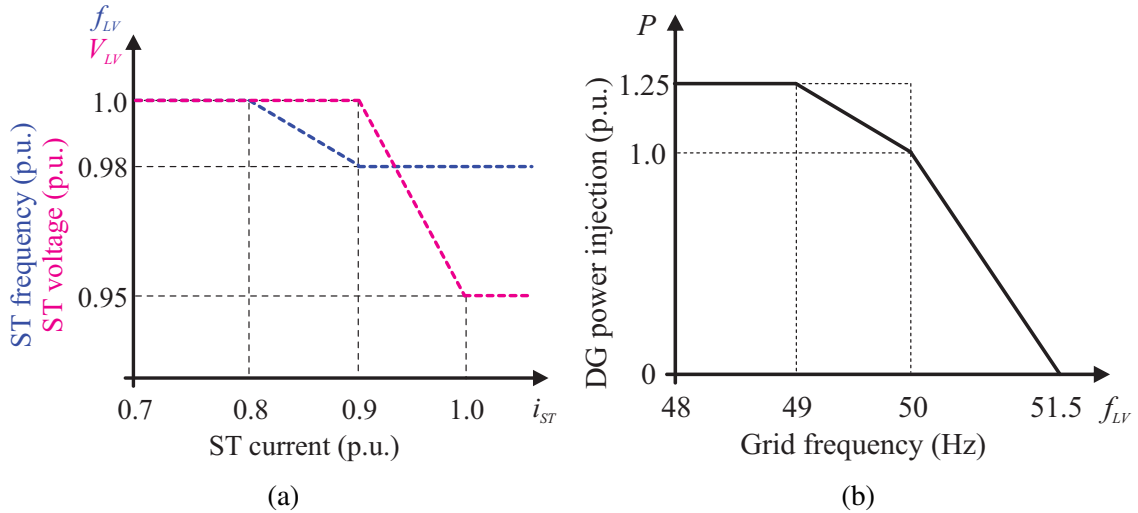


Figure 7.4: Droop controllers for overloading scenario: (a) ST droop curves and (b) DER droop curve.

the system resorts to load shedding in the LV grid. As soon as the ST current decreases, the voltage droop at first, followed by the frequency droop, deactivate. During recovering stage, a rate limit should be implemented in the voltage droop in order to avoid disruptive interaction with the frequency droop. If the voltage droop is too fast in recovering the grid voltage, the frequency may oscillate, destabilizing the overall system.

In the DER side, a droop controller is implemented as shown in Fig. 7.4b. The grid-interfaced converter decreases its power generation until shut down in the case of the upper frequency limit (e.g., 51.5 Hz) and increases its power injection up to 125 % of the nominal power in the case of frequency decrease (49 Hz). With the equipment of such droop controller, the grid-interfaced converter can interact with the ST under frequency variation signals. The frequency variation is detected by a frequency detection device. Two possible alternatives can be adopted to achieve fast frequency detection: 1) fast PLL (e.g., SOGI-PLL), whose dynamic response is much faster than the maximum rate of grid frequency [100]; 2) real-time communication (e.g. powerline carrier communication) between ST and DERs [101]. Once the frequency is detected, the DER varies the power generation following the P - f droop curve till reaching a new equilibrium point.

7.3 Frequency Adaptive Control Strategy

Compared to the conventional frequency adaptive control, the FORC derived from the IMP-based control is able to achieve zero steady-state error tracking of any periodic signal with a known period. In this section, a simple frequency-adaptive control adopting PI and FORC in the $\alpha\beta$ frame is proposed. A preview of the frequency-adaptive FORC is presented in Chapter 7.3.1. The detailed design of the frequency-adaptive controllers for both the ST voltage control and DER current control is given in Chapter 7.3.2.

7.3.1 Frequency Adaptive FORC

The IMP-based control schemes, for instance, CRC, have been well developed for power converters because of their zero steady-state error tracking ability [102]. Including the internal model of a generic periodic signal, the CRC can accurately track or suppress any periodic input or disturbance. A typical closed-loop digital control system with a plug-in CRC for a power converter is shown in Fig. 7.5a, where $R(z^{-1})$ is the reference input, $Y(z^{-1})$ is the system output, $E(z^{-1})$ is the control error, $D(z^{-1})$ represents the disturbance; $G_c(z^{-1})$ is the transfer function of the original feedback controller, $G_d(z^{-1})$ is the $1.5T_s$ (sampling time) delay of the computation and PWM, and $G_f(z^{-1})$ is the transfer function of the output filter. A CRC can be plugged into the feedforward channel and its transfer function is given by [95]

$$G_{rc}(z^{-1}) = \frac{U_r(z^{-1})}{E(z^{-1})} = k_{rc} \frac{z^{-N} Q(z^{-1}) G_{lf}(z^{-1})}{1 - z^{-N} Q(z^{-1})} \quad (7.1)$$

where k_{rc} is the gain of CRC, $G_{lf}(z^{-1})$ is the phase leading element which stabilizes the overall system, $Q(z^{-1}) = a_1 z + a_0 + a_1 z^{-1}$ with $2a_1 + a_0 = 1$ is the low-pass filter which improves the system robustness, $N = f_s/f \in \mathbf{N}$ with f_s and f being the sampling frequency and the fundamental frequency, is the so-called CRC order. It is worthy noting that the poles of CRC are exactly located at $2m\pi f$, with $m \in \mathbf{N}$. Therefore, the magnitudes of CRC at frequencies of $2m\pi f$ approach infinite if $Q(z^{-1}) = 1$, which allows the CRC to provide zero steady-state tracking error of dc, fundamental component and all harmonic components below the Nyquist frequency.

Nevertheless, in a frequency-adaptive ST-fed distribution grid, the frequency of LV side can be modified within a certain range. With a fixed sampling rate, the RC order N would often be a fractional value during frequency changes. A fractional order indicates that a fractional delay (FD) appears and it cannot be directly implemented in a digital controller. To address this issue, one solution is to use variable sampling rate while it will significantly increase the real-time implementation complexity [103]. On the other hand, the FORC scheme with a fixed sampling rate has been proposed. The fractional order N can be split into a integer order N_i and a small fractional order F , where $N = N_i + F$. The main idea of FORC is to approximate the potential FD z^{-F} by using the FD design methods [104]. Among these methods, the Lagrange interpolation-based FD design only needs a small number of sums and multiplications and at the same time can provide high approximation accuracy [105]. The FD can be well approximated by a Lagrange interpolation polynomial finite impulse response (FIR) filter as follows:

$$z^{-F} \approx \sum_n^{k=0} A_k z^{-k} \quad (7.2)$$

where $k \in \mathbf{N}$, the Lagrange coefficients A_k of (7.2) are given by

$$A_k = \prod_{\substack{i=0 \\ i \neq k}}^n \frac{F-i}{k-i}. \quad (7.3)$$

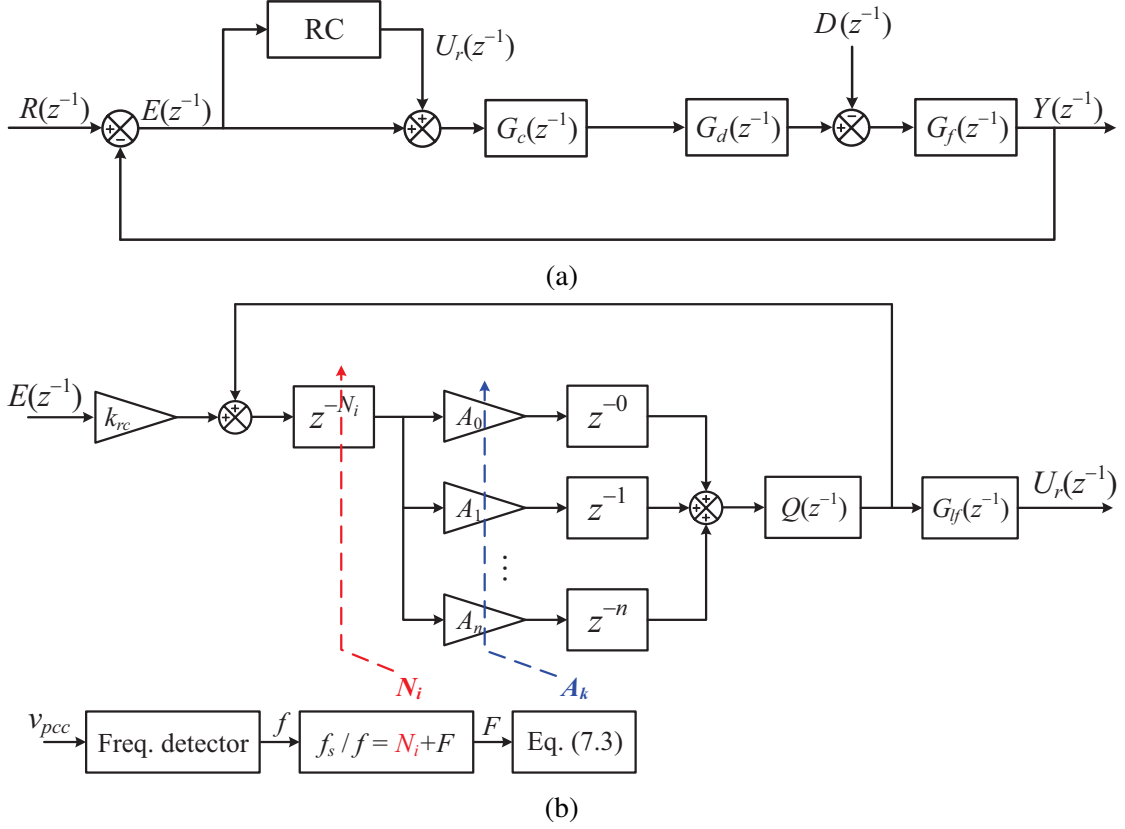


Figure 7.5: Block diagrams of a plug-in RC system: (a) overall system and (b) frequency-adaptive FORC.

Substituting (7.2) into (7.1), the frequency-adaptive FORC will be obtained as

$$G_{forc}(z^{-1}) = \frac{z^{-N_i} \sum_{k=0}^n A_k z^{-k} Q(z^{-1})}{1 - z^{-N_i} \sum_{k=0}^n A_k z^{-k} Q(z^{-1})} G_{lf}(z^{-1}). \quad (7.4)$$

The detailed FORC block diagram of (7.4) is presented in Fig. 7.5b. It is shown that two time scales have been utilized in the control system: 1) the changing rate of delay orders (N_i and F) is highly dependent on the dynamic response of frequency detector; 2) the update rate of A_k depends on the sampling frequency. In a distribution grid application, the changing rates of both the N_i and F are much slower than the sampling rate. In each sampling interval, the detected frequency as well as N_i and F can be regarded as constant values.

According to the properties of the Lagrange Interpolation polynomial, there is always an approximation remainder between the theoretical FD and the polynomial. The remainder term of FD can be written as follows

$$R_n = z^{-F} - \sum_{k=0}^n A_k z^{-k} = \frac{\xi^{-F-n} \prod_{i=0}^{n-1} (-F-i)}{(n+1)!} \prod_{i=0}^n (-F-i) \quad (7.5)$$

where $\xi \in [T_k, T_{k+1}]$ with T_k and T_{k+1} being the k th and $k+1$ th sampling intervals, respectively. Fig. 7.6 shows the magnitude responses of the Lagrange interpolation based FD filter of (7.2) with the degree $n=1$ and $n=3$ for various fraction F from 0 to 0.9. The FD filter of

(7.2) with degree $n = 3$ give an excellent approximation of FD z^{-F} at low frequencies within bandwidth of 75 % Nyquist frequency, whereas the bandwidth of 50 % Nyquist frequency for the FD filter of degree $n = 1$. Within its passband of the FD filter of (7.2), the magnitude response of the proposed FORC is close to one. Thus the proposed FORC can exactly track fractional period signals.

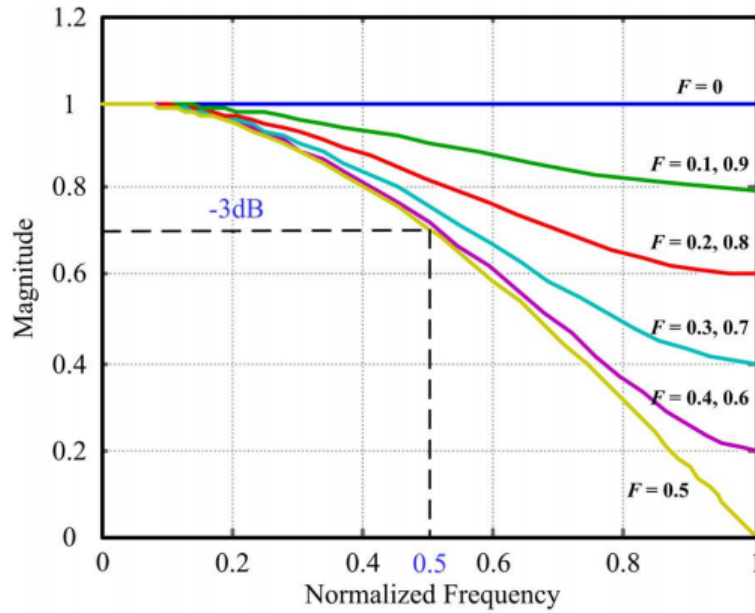
Fig. 7.7a compares the magnitude responses of Lagrange Interpolation-based FD with different polynomial degrees. It confirms that better approximation accuracy can be achieved with the increase of the polynomial degree n . When the degree $n \geq 3$, the approximated FIR filter can achieve excellent approximation towards the FD z^{-F} within the Nyquist frequency. Further increasing of the approximation degree can hardly improve accuracy within the Nyquist frequency but increase the computation burden. To evaluate the tracking ability, the approximation remainder norms of FORC with different sampling frequencies are analyzed as shown in Fig. 7.7b and also compared with those of CRC. When the fundamental frequency varies in a certain range, the remainder norms of CRC change drastically and some of them are relatively high, indicating the tracking error could not be eliminated under variable frequency condition. However, the norms of FORC always remain in a lower level at the neighborhood of fundamental frequency. In addition, the averaging norm at the frequency neighborhood will decrease when the sampling frequency increases. It can be concluded that a higher sampling frequency should be employed to reduce the RMS value of tracking error of FORC or CRC.

The FORC scheme provides a general approach to track or eliminate of any periodic signal with an arbitrary fundamental frequency and fixed sampling frequency. It is evident that the transfer function of (7.4) becomes a conventional repetitive control as (7.1) in the case of an integral order ($F = 0$). Moreover, Lagrange interpolation is one of the easiest ways to design a FD filter to approximate a given FD. The coefficient of (7.3) for the FD filter only consumes a small number of sums and multiplications for a fast online update of A_k . Therefore, Lagrange interpolation-based FIR FD filter not only can be easily implemented in real time applications but can also offer high approximation accuracy in most cases. The FIR FD filter-based FORC can offer an attractive method for the real time control of high switching frequency converters.

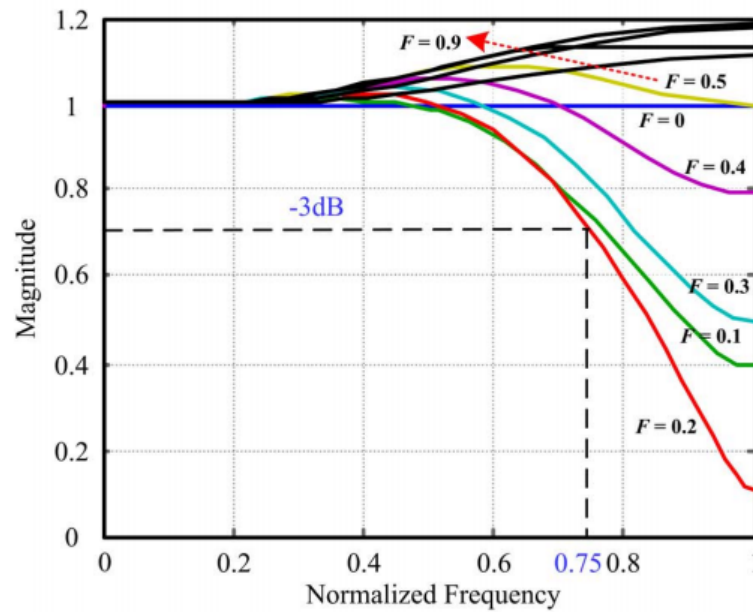
7.3.2 Frequency Adaptive Control Design for ST-fed Grid

As can be seen in Fig. 7.3, frequency-adaptive control strategy has been implemented in both the ST LV voltage and the DER current control to achieve high performance under variable frequency condition. Fig. 7.8 depicts the simplified block diagrams of the ST LV side voltage control scheme and the DER current control scheme in the stationary frame.

The PI-plus-FORC control strategy has been utilized for both control systems to ensure frequency adaptability. It is known that the PI controller under $\alpha\beta$ frame is independent from frequency variation. Using proper gains, the PI-controlled system can offer high stability



(a)



(b)

Figure 7.6: Magnitude response of Lagrange Interpolation-based FD with: (a) first degree and (b) third degree.

margin and good transient response. The plug-in FORC controller improves steady-state performance and guarantees zero steady-state error under variable frequency condition.

For the ST LV side voltage control, to alleviate the LC resonance and limit the overcurrent, an inductance current control loop has been used as the inner loop. A proportional gain is employed as the inner loop control since it can effectively increase the damping ratio and limit the current during overcurrent conditions [34]. The PI-plus-FORC control has been applied to the outer voltage loop to meet error-tracking requirements with specific bandwidth. A voltage feed-forward compensation is used to improve the transient response of the

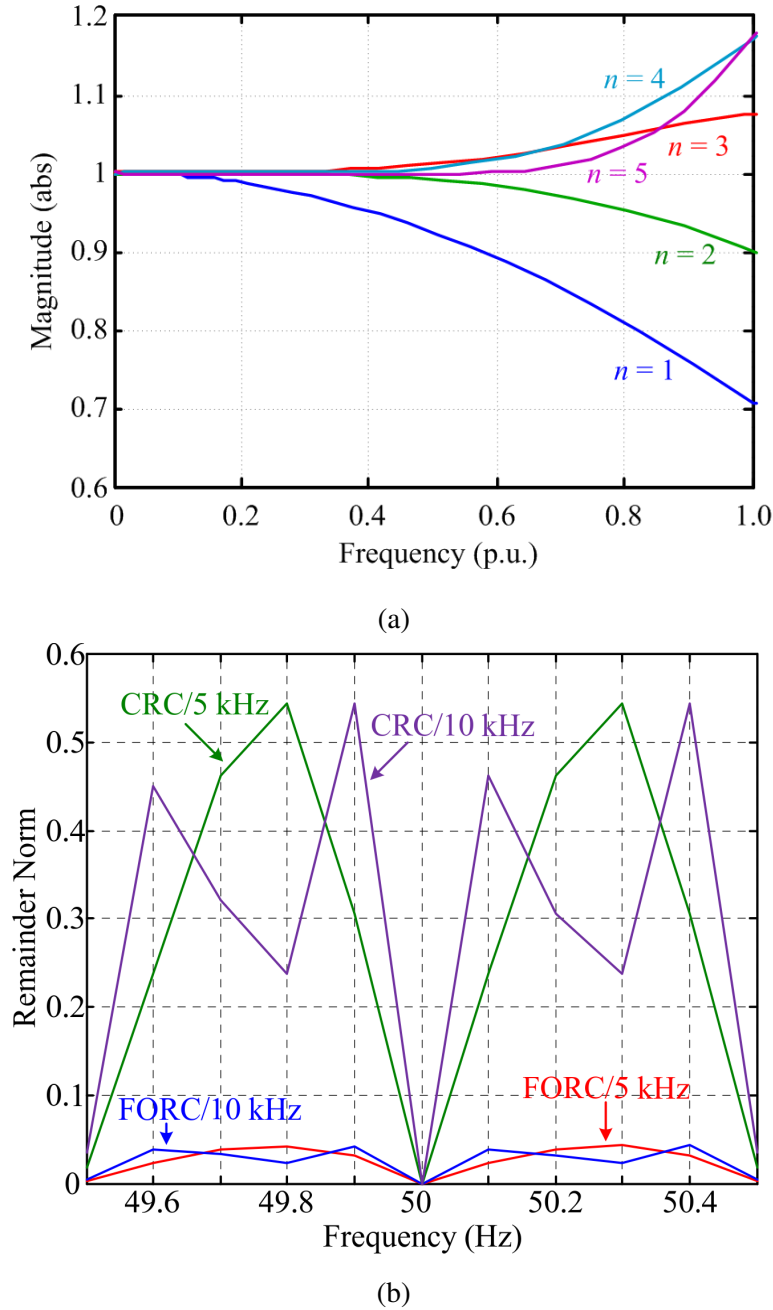


Figure 7.7: Performance evaluation: (a) magnitude response of Lagrange Interpolation-based FD with different degree and (b) comparisons of remainder norm between CRC and FORC under different sampling frequencies.

overall system. The selection of control bandwidth BW_{st} refers to $BW_{st} < f_s/10$, where f_s is the sampling frequency. Meanwhile, the necessary attenuation at the neighborhood of the LC cut-off frequency should be achieved to damp the filter resonance. Without the FORC, the PI controller decides the control bandwidth as well as phase margin of the overall system. The phase margin is selected between 45° and 60° according to the usual design rules. The gains of the PI controller for ST voltage control can be determined based on the above-mentioned rules. The open-loop Bode diagrams are presented in Fig. 7.9a using the system parameters listed in Table 7.1. The blue plot represents the open-loop frequency response of the control system without FORC. By using the control parameters of Table 7.1, the bandwidth is

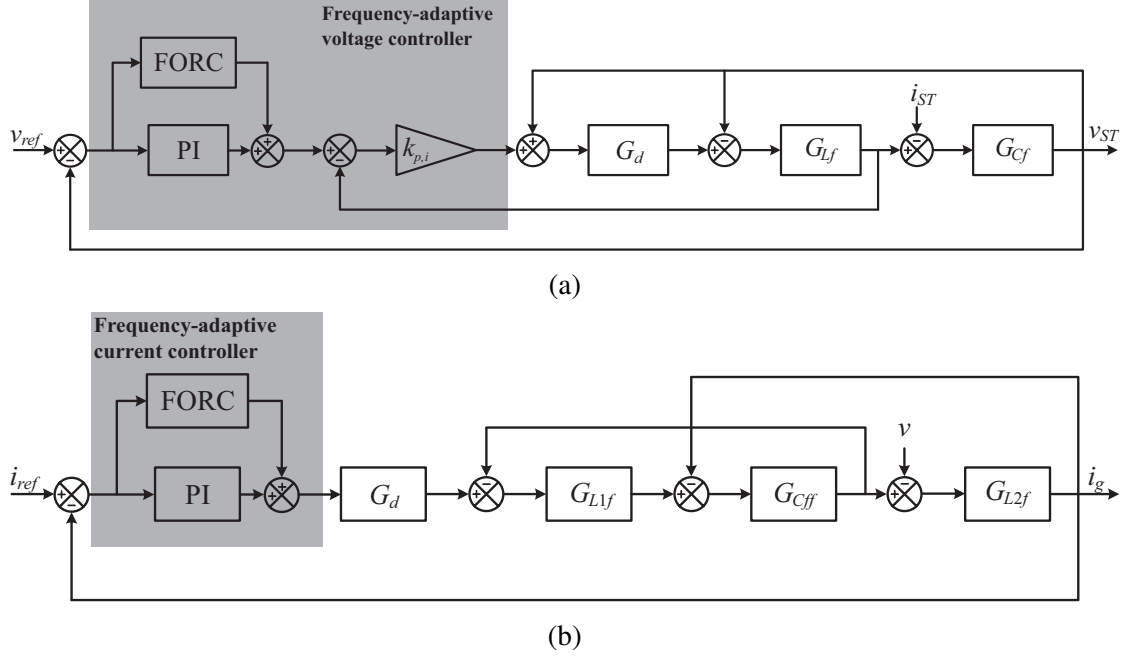


Figure 7.8: Block diagrams of frequency-adaptive voltage/current control systems: (a) ST LV side voltage control and (b) DER current control.

Table 7.1: System Parameters of ST LV Converter

Symbol	Quantity	Value
v_{ST}	Voltage of ST LV converter	230 V (RMS)
L_f	inductance of LC filter	2.4 mH
C_f	capacitance of LC filter	8 μ F
T_s	sampling frequency	10 kHz
$k_{p,o}$	proportional gain of PI	5e-3
$k_{i,o}$	integral gain of PI	0.25
$k_{p,i}$	gain of inner loop	10
k_{rc}	gain of FORC controller	0.1

267 Hz and the phase margin is 47° . The frequency response of the control with plugged-in FORC is shown by the red plot, where large magnitudes and zero phase shifts at interested frequencies have been introduced.

For the DER current control, a passive damping resistor has been employed to alleviate the LCL resonance and the PI-plus-FORC is adopted to deal with the variable frequency current. The design of the PI controller follows the same procedure of voltage control design for the ST LV side inverter. Because of the lack of inner loop, a higher bandwidth between $f_s/5$ and $f_s/3$ can be selected for PI controller to better reject the grid disturbance and the low-order harmonics. The recommended phase margin is still between 45° and 60° . As a result, the gains of PI controller for DER current control can be designed based on these two rules and listed in Table 7.2. A 1220 Hz bandwidth and 45° phase margin system can be obtained.

Table 7.2: System Parameters of DER Grid Converter

Symbol	Quantity	Value
i_g	DER nominal current	7.5 A (RMS)
L_{f1}	inverter-side inductance of <i>LCL</i> filter	2.4 mH
C_{ff}	capacitance of <i>LCL</i> filter	1 μ F
R_d	damping resistance of <i>LCL</i> filter	2 Ω
L_{f2}	grid-side inductance of <i>LCL</i> filter	0.5 mH
T_s	sampling frequency	10 kHz
k_{pc}	proportional gain of PI	2.5
k_{ic}	integral gain of PI	300
k_{rc}	gain of FORC controller	0.1

The open-loop Bode diagrams with/without FORC are shown in Fig. 7.9b. It is seen that the designed PI-plus-FORC current control introduces attenuation at medium/high frequency range and large magnitudes at the frequencies of interest, ensuring low grid current THD.

7.4 Stability Analysis

7.4.1 FORC Stability Conditions

The generic stability conditions of a FORC-controlled system have been given in literature [96]. Before the FORC is added to the system of Fig. 7.5a, the transfer function of the basic closed-loop system is

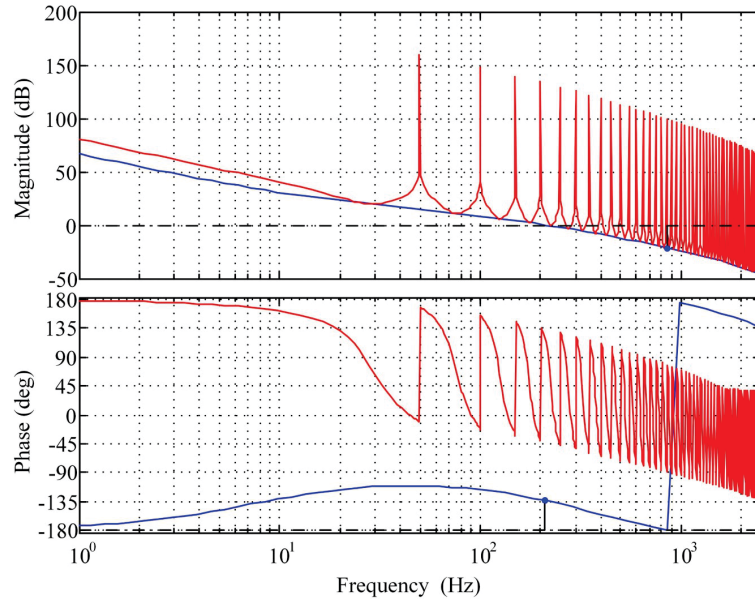
$$H(z^{-1}) = \frac{Y(z^{-1})}{R(z^{-1})} = \frac{G_c(z^{-1})G_d(z^{-1})G_f(z^{-1})}{1 + G_c(z^{-1})G_d(z^{-1})G_f(z^{-1})}. \quad (7.6)$$

Let the open-loop transfer function $G_{ops}(z^{-1}) = G_c(z^{-1})G_d(z^{-1})G_f(z^{-1})$. When the FORC is plugged in, the error transfer function of the overall system becomes:

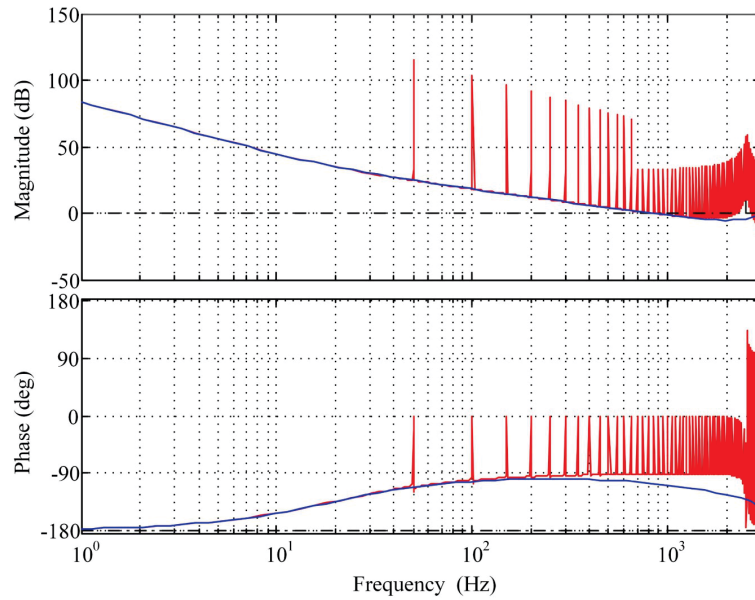
$$G_e(z^{-1}) = \frac{E(z^{-1})}{R(z^{-1}) - D(z^{-1})} = \frac{(1 - z^{-N_i} \sum_{k=0}^n A_k z^{-k})(1 + G_{ops}(z^{-1}))^{-1}}{1 - z^{-N_i} \sum_{k=0}^n A_k z^{-k} Q(z^{-1})(1 - k_{rc} G_{lf}(z^{-1})H(z^{-1}))}. \quad (7.7)$$

Based on the error transfer function of (7.7), two generic stability conditions can be obtained. A FORC-controlled system is asymptotically stable if the following two conditions hold: 1) the roots of $1 + G_{ops}(z^{-1}) = 0$ are inside the unity circle; 2) the roots of $1 - z^{-N_i} \sum_{k=0}^n A_k z^{-k} Q(z^{-1})(1 - k_{rc} G_{lf}(z^{-1})H(z^{-1})) = 0$ are inside the unity circle.

$$\left| 1 - k_{rc} G_{lf}(z^{-1})H(z^{-1}) \right| < \left| Q(z^{-1}) \sum_{k=0}^n A_k z^{-k} \right|^{-1}. \quad (7.8)$$



(a)



(b)

Figure 7.9: Bode diagrams of frequency-adaptive voltage/current control systems: (a) ST LV side voltage control and (b) DER current control.

It is worth noticing that the magnitudes of the Lagrange interpolation polynomial are always less than or close to 1 (abs) within the Nyquist frequency. The inequality of (7.8) can be simplified in practical case study:

$$\begin{aligned}
 |1 - k_{rc}G_{lf}(z^{-1})H(z^{-1})| &< |Q(z^{-1})|^{-1} \left| \sum_{k=0}^n A_k z^{-k} \right|^{-1} \\
 &< |Q(z^{-1})|^{-1}.
 \end{aligned} \tag{7.9}$$

Then, (7.9) yields

$$0 < k_{rc} < \frac{1 + |Q(z^{-1})|}{|Q(z^{-1})| |G_{lf}(z^{-1})H(z^{-1})|}. \quad (7.10)$$

If (7.10) is satisfied and provided the basic closed-loop system $H(z^{-1})$ is asymptotically stable, a stable FORC-controlled system can be achieved.

From (7.9), it is observed that the gain of FORC controller would be restricted by the norm of the low-pass filter. As indicated in [27] that the Lagrange interpolation polynomial behaves like a low-pass filter when lower degree ($n \leq 3$) is used. With this consideration, the low-pass filter $Q(z^{-1})$ can be removed while the stability conditions can still be fulfilled. For instance, if the cut-off frequency of the proposed polynomial FD filter is less than that of $Q(z^{-1})$, (7.9) turns out to be

$$\begin{aligned} |1 - k_{rc}G_{lf}(z^{-1})H(z^{-1})| &< |Q(z^{-1})|^{-1} \left| \sum_{k=0}^n A_k z^{-k} \right|^{-1} \\ &< \left| \sum_{k=0}^n A_k z^{-k} \right|^{-1}. \end{aligned} \quad (7.11)$$

indicating $Q(z^{-1})$ can be omitted while the stability conditions are still fulfilled with the pre-designed k_{rc} . In some practical cases, it can save the design of the low-pass filter for the system and avoid additional phase shift which is introduced by the low-pass filter.

7.4.2 System Stability Considering the Synchronization

The impact of synchronization on the stability of FORC-controlled system has seldom been considered. However, as pointed out by [64], the utilization of synchronization (e.g. SOGI-PLL) in current-controlled inverter could lead to stability issues especially in a weak grid. As a result, the characteristics of PLL must be taken into account for the stability of the control of the DER inverter.

The schematic diagram of Fig. 7.5a in each frame can be updated and is shown in Fig. 7.10, where a PLL is considered: the input signal I_{ref} is the amplitude of the current reference. Considering that the proportional gain k_{pc} of the PI controller mainly determines the stability margin, the root loci of the DER inverter control with the variation of k_{pc} are shown in Fig. 7.11. In Fig. 7.11a, the root locus of the original current feedback system in the gray box of Fig. 7.5a is plotted, while the root locus of the overall system (considering the synchronization in the blue dash box) is plotted in Fig. 7.11b. It is observed that the control system considering PLL introduces additional poles in the low-frequency range, which lead to a smaller gain range, compared to the original current feedback system. As a result, the effects of the synchronization are likely to compromise the system stability. With this consideration, the closed-loop transfer function $H(z^{-1})$ has to be reconsidered, since an asymptotically stable system should be achieved before the FORC is plugged in. In the system of Fig. 7.10,

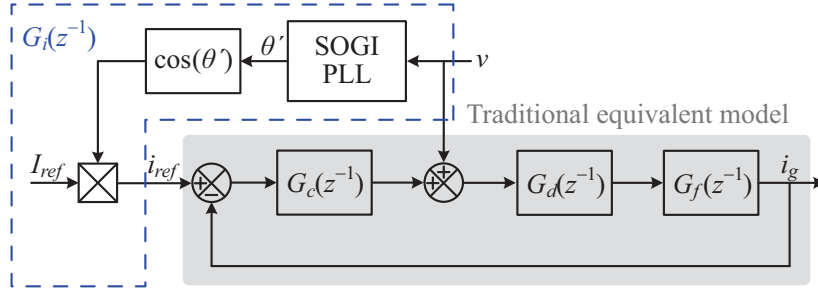


Figure 7.10: Simplified block diagram of a grid-interfaced inverter for DER.

$H(z^{-1})$ can be updated by

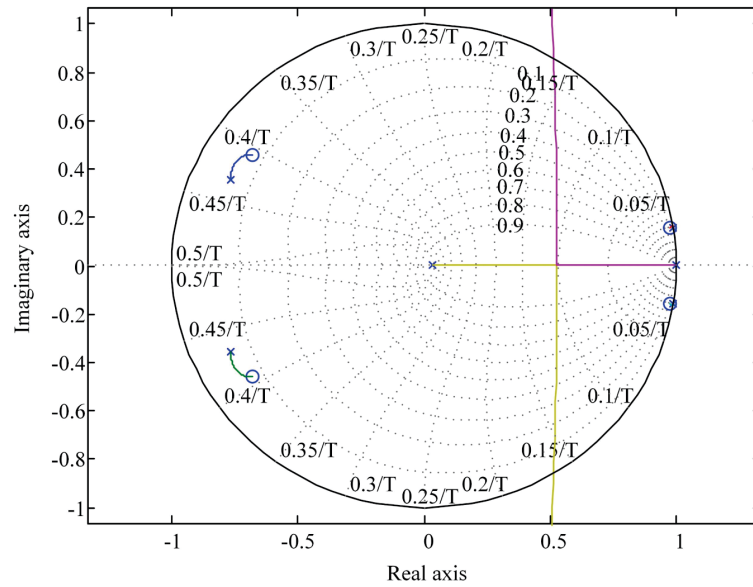
$$H(z^{-1}) = \frac{G_i(z^{-1})G_{ops}(z^{-1}) - G_d(z^{-1})G_f(z^{-1})}{1 + G_{op}(z^{-1})} \quad (7.12)$$

where $G_i(z^{-1})$ is the transfer function of PLL as well as current reference generator, and thus the stability condition should be evaluated by using the updated $H(z^{-1})$ that considers the synchronization. Accordingly, the range of the k_{rc} would be limited depending on the characteristics of PLL.

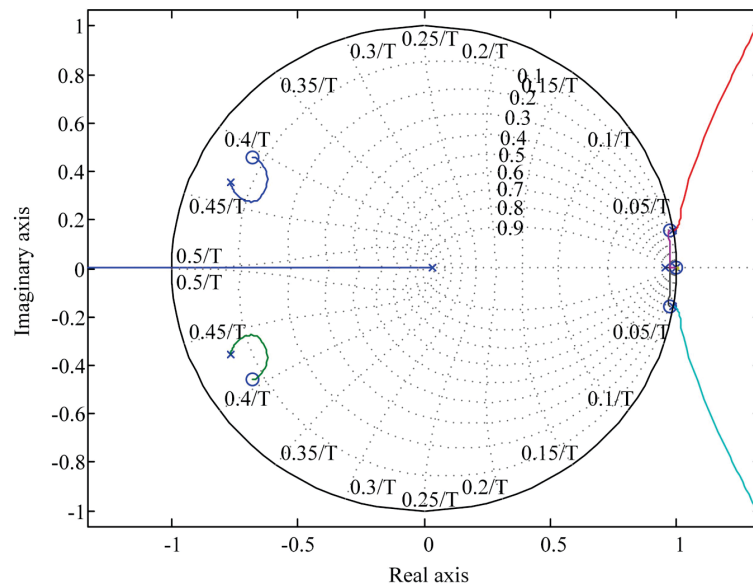
On the other hand, the participation of the frequency-adaptive control of local DERs requires updating online the frequency, which ensuring the accuracy of the Lagrange coefficients. Nevertheless, the intrinsic delay of frequency detection of PLL (the delay between the actual frequency and the detected frequency) has an influence on the FORC-controlled system. The frequency delay is dependent on the dynamic response of PLL (e.g. rising time and settling time). For analysis simplicity, a N_2 steps delay z^{-N_2} has been employed to represent the frequency delay, so that the transfer function of the Lagrange interpolation polynomial FIR becomes

$$Y_f(z^{-1}) = z^{-N_2} \sum_{k=0}^n A_k(z^{-1})z^{-k}. \quad (7.13)$$

Substituting (7.13) into (7.8), it is seen that the form of the second condition remains the same. This indicates that the FORC-controlled system is not sensitive to the frequency delay as long as the first stability condition is fulfilled. For a slow PLL with longer settling time, if the control system is stable before the FORC is plugged in, the delay of frequency can barely jeopardize the system stability after FORC is applied. However, the control accuracy does rely on the accuracy of the frequency detection. The delay of frequency can shift the large magnitudes away from the actual frequencies of interested and thus deteriorate the control performance. As a result, synchronization with the capabilities of real-time measurement and frequency adaptivity is crucial to the performance of the frequency-adaptive distribution grid. A set of frequency-adaptive synchronization algorithms were proposed in the literature [106], allowing the grid-interfaced converters to fast and accurately detect the phase sequencing under variable frequency condition. In the frequency control scenarios, a combination between these frequency-adaptive synchronization and the FORC could be a promising candidate that provides higher power quality and reduced power oscillation.



(a)



(b)

Figure 7.11: Root locus of the overall system when k_{pc} changes: (a) with only current feedback control and (b) considering the PLL.

7.5 Simulation and Experimental Results

7.5.1 Simulation Results

To validate the proposed frequency-adaptive control strategy, it has been simulated in a ST-fed distribution grid of Fig. 7.3 in MATLAB/Simulink with PLECS toolbox. Two case studies are investigated in the following section: the frequency-based overloading scenario [88] and the frequency-based reverse power flow scenario [24]. The system parameters listed in Table 7.1 and Table 7.2 have been utilized for the simulations. In both case studies, the frequency range of the ST-fed distribution grid is defined as 49 Hz-51 Hz.

In the overloading scenario, the security limit of ST LV current is 25 A (rms). The DER is assumed to operate at unity PF with 17 kW nominal power. Initially, the overall system operates at 50 Hz, the power rating of the DER is 12.8 kW at the nominal frequency, a 15.9 kVA (PF = 0.9) linear load and a 6.1 kVA nonlinear load are connected to the grid. At $t = 0.8$ s, the load increases from 22 kVA to 32.6 kVA. As soon as the current of ST LV side exceeds the security limit, the frequency-based overloading control of ST is activated. As shown in Fig. 7.12a, when the load increases at $t = 0.8$ s, the ST LV side current increases as well and activates the frequency control. The ST current decreases till below the security limit and reaches its new equilibrium by means of the frequency control. The voltage amplitude remains constant and it regains the nominal value in less than one cycle after the application of the frequency change. The DER behavior during the frequency control is shown in Fig. 7.12b. A SOGI-PLL is utilized as the synchronization element, and a comparison between the detected frequency and the ST frequency set-point is presented, showing a fast and accurately tracking of the frequency with a delay inferior to two cycles (40 ms). Following the frequency change, the DER proportionally increases its power generation according to the given P - f droop curve. A new power equilibrium is established and the frequency holds the line of 49.5 Hz.

In the reverse power flow scenario, the overall load consumption is 32.6 kVA and the DER is operated initially at the nominal power. At $t = 0.8$ s, the load demand decreases from 32.6 kVA to 16.7 kVA. As a result, a reverse power flow occurs shown in Fig. 7.12c, the frequency-based reverse power flow control of ST is activated. The ST LV side frequency increases until the power flow direction is changed and a new equilibrium is reached. The voltage amplitude remains constant and it regains the nominal value in less than one cycle after the frequency change. The DER behavior during the frequency control is shown in Fig. 7.12d. The frequency detected by the SOGI-PLL can well follow the ST frequency change. Following the frequency change, the DER proportionally decreases its power generation according to the given P - f droop curve. A new power equilibrium is established and the frequency holds the line of 50.5 Hz.

The effectiveness of the proposed frequency-adaptive control strategy is verified in both scenarios as follows. Comparisons of ST voltage control and DER current control by using CRC and FORC schemes during the frequency control are presented in Fig. 7.13 and Fig. 7.14. In the overloading scenario (Fig. 7.13), it is seen that both the ST LV side voltage and the DER output current are well controlled by using FORC-based frequency-adaptive control, providing satisfactory performance even during the frequency control, while the CRC-controlled systems present considerable control errors when frequency deviates from the nominal value, leading to worse voltage and current waveforms. Similarly, in the reverse power flow scenario (Fig. 7.14), the FORC-based frequency-adaptive control offers better accuracy compared to the CRC-based control in terms of waveform and control error. Generally speaking, the FORC-based control is adaptive to the frequency variation, whereas the CRC-based control is not.

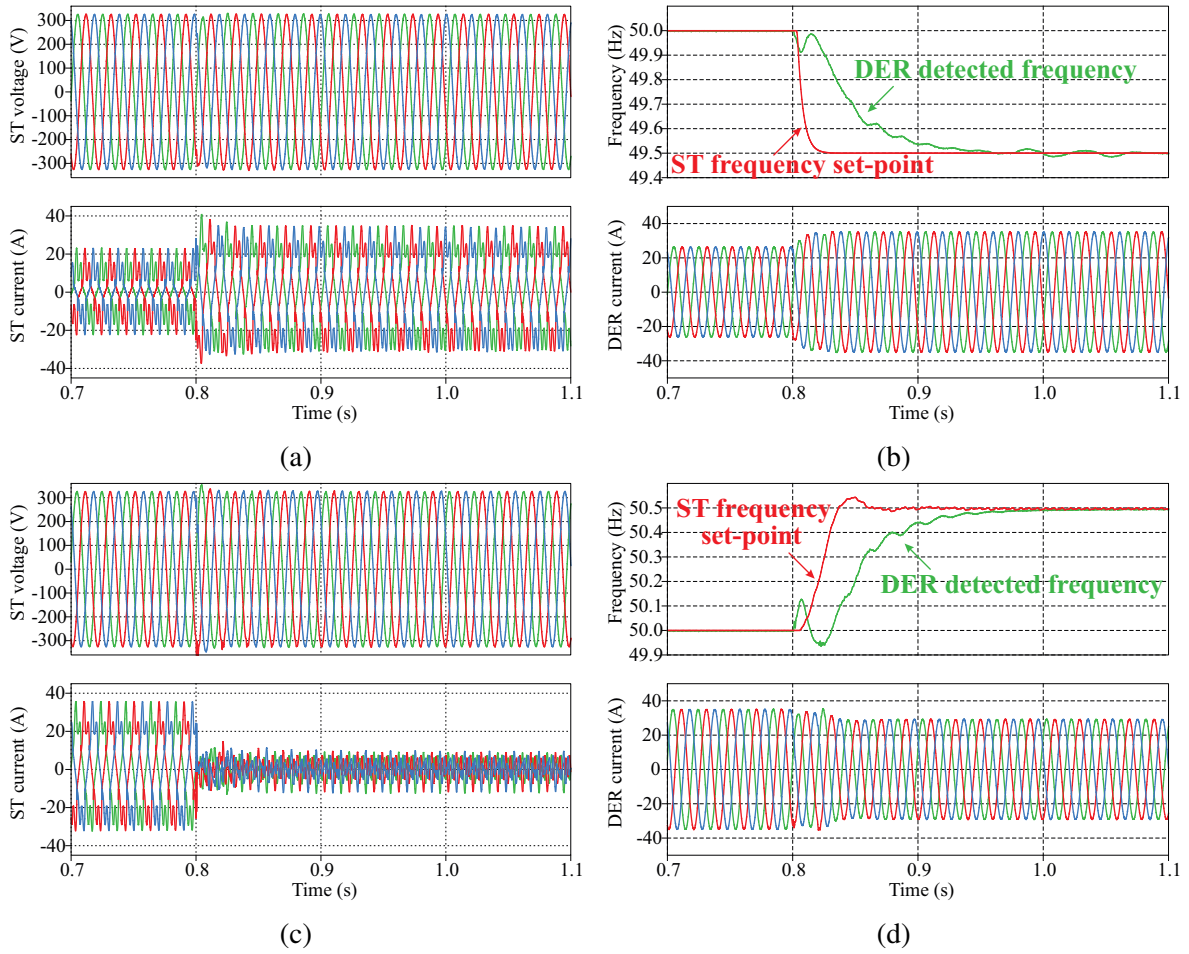


Figure 7.12: Performance evaluation of frequency-adaptive ST-fed grid under two scenarios (overloading, reverse power flow): (a) ST voltage (top) and current (bottom) under overloading scenario, (b) DER detected frequency (top green), ST frequency set-point (top red) and DER output current (bottom) under overloading scenario, (c) ST voltage (top) and current (bottom) under reverse power flow scenario, and (d) DER detected frequency (top green), ST frequency set-point (top red) and DER output current (bottom) under reverse power flow scenario.

7.5.2 Experimental Results

In the following section, the effectiveness of the frequency-adaptive control in a ST-fed grid has been experimentally validated. The experimental setup with two Danfoss FC-302 inverters have been used, one for the LV side inverter of ST, another for the grid-interfaced inverter of DER: a dSPACE 1006 has been utilized to control both inverters. The system configuration of the experimental setup is same to that of Fig. 7.3. A 3.75 kW linear load and 1.12 kVA nonlinear load have been connected into the grid. The detailed parameters of the overall system are listed in Table 7.3. The system parameters listed in Table 7.1 and Table 7.2 are used for the control systems and the output filters of both inverters.

First of all, the overloading scenario shown by the example in Chapter 7.2 has been experimentally verified with the setup. The maximum current limit has been set to 6 A and the thresholds of the frequency and voltage droop controllers have been set to 80% and 90%,

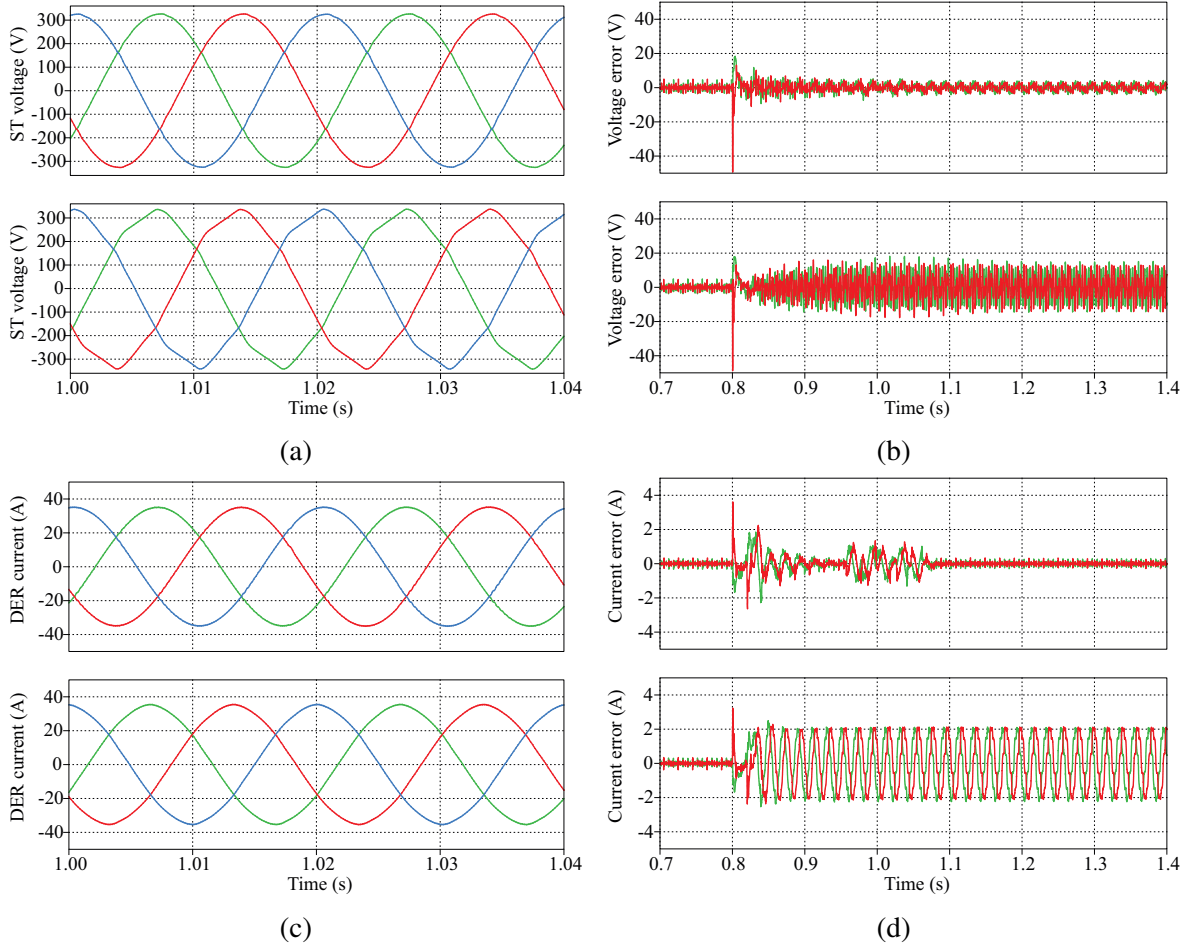


Figure 7.13: Performance comparisons of two different control strategies (FORC, CRC) under overloading scenario: (a) zoomed ST voltages at 49.5 Hz by using FORC (top) and CRC (bottom), (b) voltage control errors by using FORC (top) and using CRC (bottom), (c) zoomed DER currents at 49.5 Hz by using FORC (top) and CRC (bottom), and (d) current control errors by using FORC (top) and using CRC (bottom).

Table 7.3: Setup Parameters of Frequency Adaptive ST-fed Grid

Symbol	Quantity	Value
v_{LVDC}	dc-link voltage of ST LV converter	650 V
v_n	rated voltage of LV converter	3×380 V (RMS)
S_n	rated power of LV converter	4 kW

respectively. The voltage ramp limiter has been set equal to 0.2 V/s. The variable resistor has been operated from 28Ω to 21Ω for about 20 s. The experimental waveforms during the overloading control is shown in Fig. 7.15. As soon as the ST current exceeds the 4.8 A threshold, the frequency droop control is activated and it decreases the frequency from 50 Hz to 49 Hz. When the current increases above 5.4 A the voltage is decreased, limiting the ST overload to 5.6 A, with a further margin for load increase. The voltage drops from 220 V

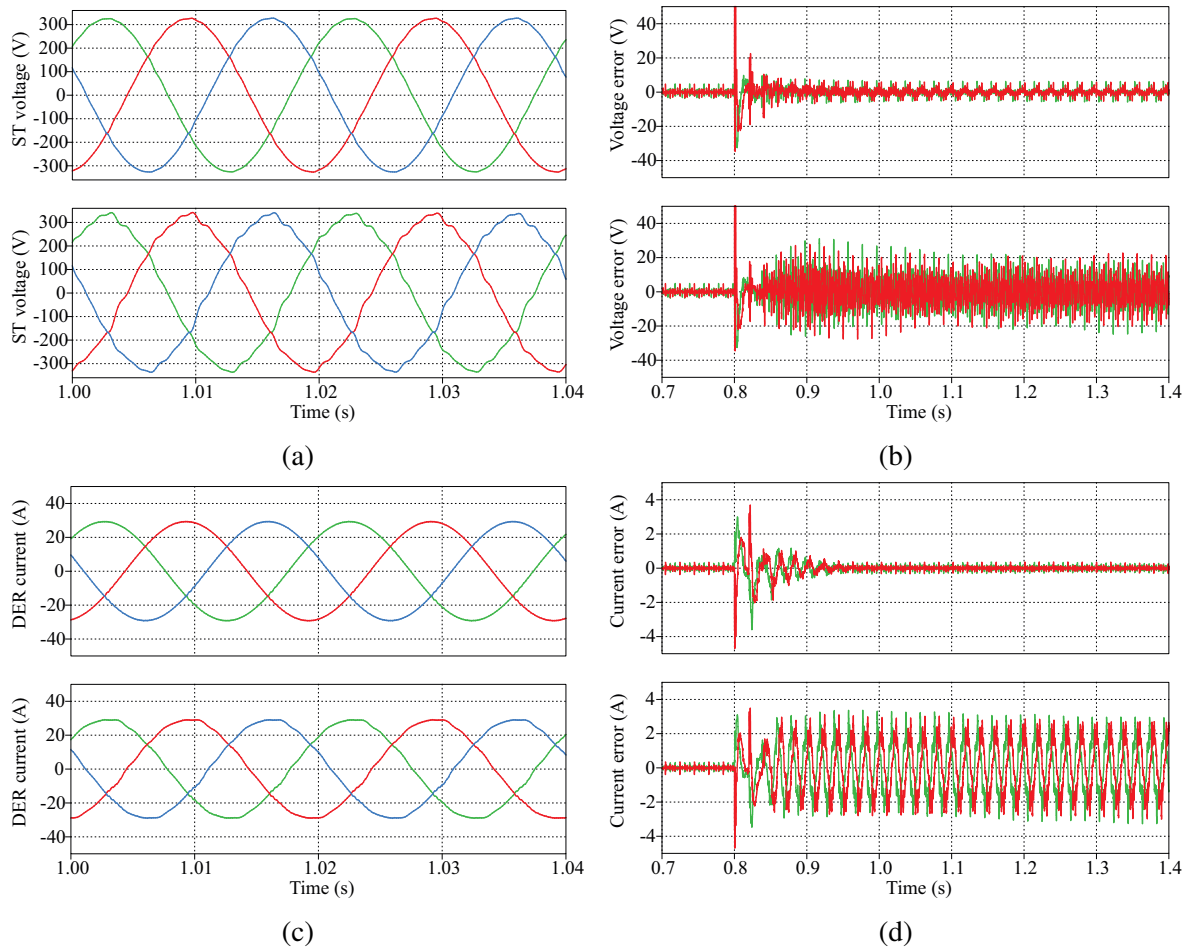


Figure 7.14: Performance comparisons of two different control strategies (FORC, CRC) under reverse power flow scenario: (a) zoomed ST voltages at 50.5 Hz by using FORC (top) and CRC (bottom), (b) voltage control errors by using FORC (top) and using CRC (bottom), (c) zoomed DER currents at 50.5 Hz by using FORC (top) and CRC (bottom), and (d) current control errors by using FORC (top) and using CRC (bottom).

to 215.5 V during the steady state condition. As soon as the variable resistance increases, the ST current decreases and the voltage and frequency are slowly restored to the nominal value.

A better understanding of the overload scenario can be obtained looking at the three-phase voltage and current waveforms Fig. 7.16. The distribution grid initially works under nominal condition (50 Hz), with the above-mentioned linear load. Then, the nonlinear load connects to the ST-fed grid, leading to a higher loading. The frequency control is activated when the ST current exceeds its security limit. In order to alleviate the overloading issue, the frequency gradually decreases from 50 Hz to 49.6 Hz so that the DER production increases and the load consumption decreases. A new power balance is eventually reached at 49.6 Hz. The ST LV side voltage waveform and its frequency set-point during frequency control are shown in Fig. 7.16a. The DER output current and the detected frequency during frequency control are shown in Fig. 7.16b. It is shown that the voltage amplitude stays constant and the power quality is ensured during both the steady-state and the transient stage. The current amplitude

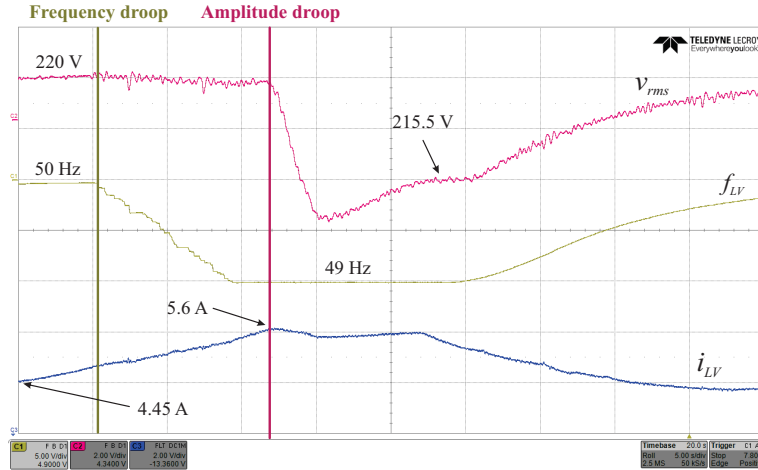


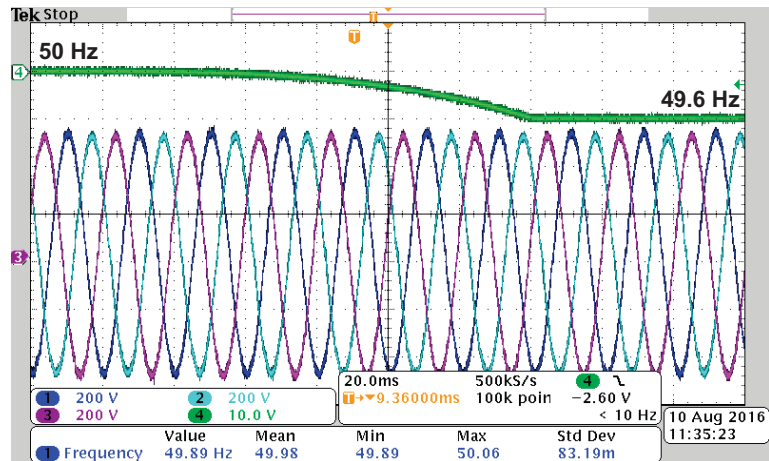
Figure 7.15: Experimental waveforms during overloading control: magenta curve - ST rms voltage, yellow curve - LV grid frequency, and blue curve - ST rms current.

Table 7.4: Performance Comparison of CRC- and FORC-Controlled Systems

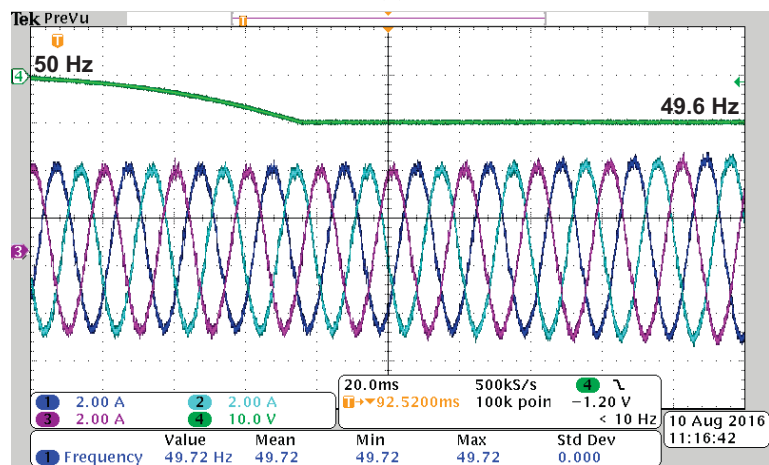
Control	Frequency	Voltage	Current	THD _V	THD _I
CRC	50 Hz	0.987 p.u.	0.987 p.u.	2.90 %	3.76 %
	49.8 Hz	0.967 p.u.	0.938 p.u.	6.54 %	6.97 %
	49.6 Hz	0.959 p.u.	0.917 p.u.	7.21 %	8.36 %
FORC	49.8 Hz	0.981 p.u.	0.975 p.u.	3.12 %	4.21 %
	49.6 Hz	0.979 p.u.	0.958 p.u.	3.35 %	4.69 %

linearly increases according to the droop curve of the DER. To guarantee accurate frequency detection, the SOGI-PLL has been adopted in the DER for grid synchronization. The comparison between the ST frequency set-point and the detected frequency via SOGI-PLL is shown in Fig. 7.16c. It is seen that the frequency detected by the PLL can timely follow the ST frequency with less than 10 ms delay, offering good performance during frequency control stage.

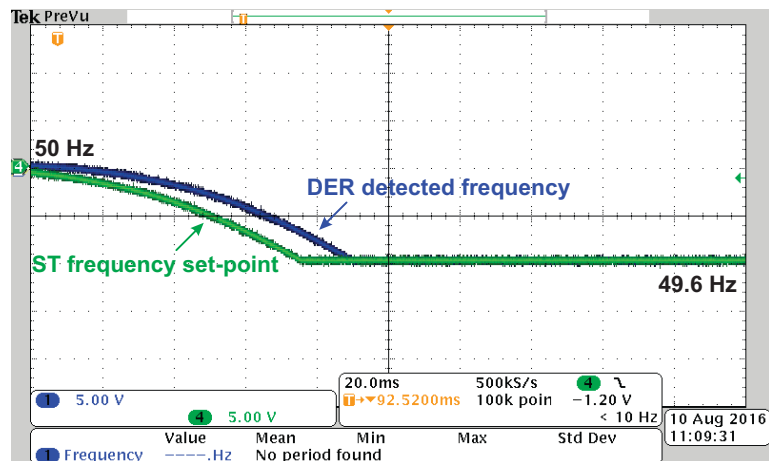
Following, the zoomed voltage and current waveforms in a ST-fed grid during frequency control stage by using different control strategies are compared. In Fig. 7.17a and Fig. 7.18a, the CRC scheme has been employed for both the ST voltage control and the DER current control. It is seen that both the ST LV side voltage and DER output current are distorted during frequency control (e.g., 49.7 Hz). When the proposed FORC-based voltage and current control are used, the ST LV side voltage and DER output current are shown in Fig. 7.17b and Fig. 7.18b, with less harmonic distortion. More details of the performance comparison have been listed in Table 7.4. The case study shows that CRC is sensitive to grid frequency variation in terms of THD and amplitude, whereas FORC is not. By using the proposed frequency-adaptive control, the ST-fed distribution grid can provide satisfactory performance in terms of control accuracy and power quality.



(a)

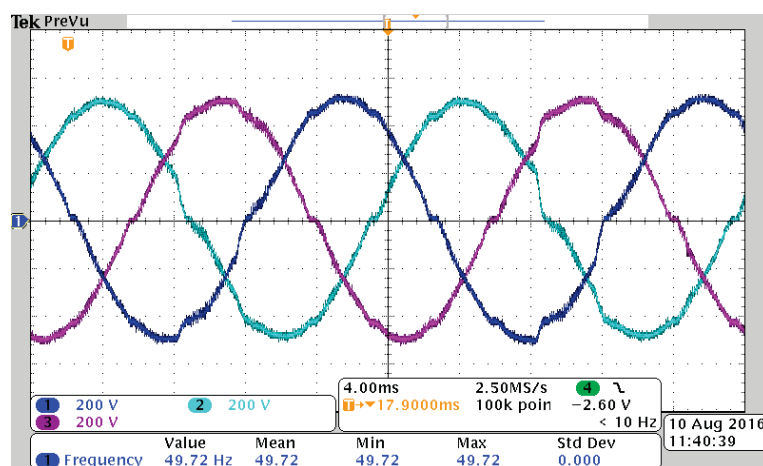


(b)

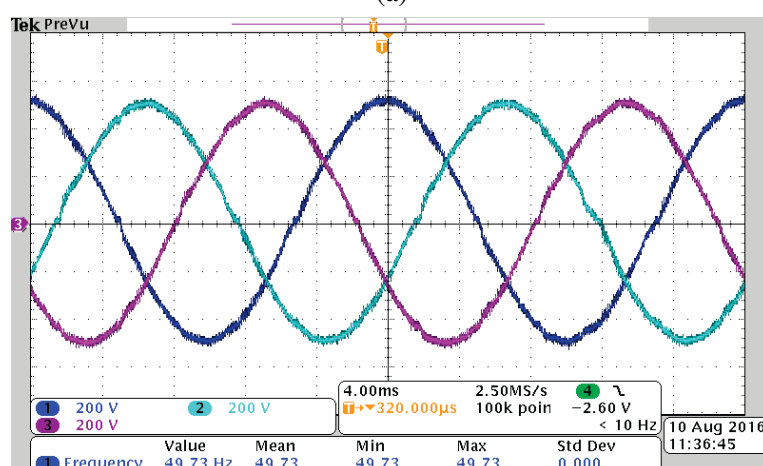


(c)

Figure 7.16: Voltage and current waveforms of a ST-fed distribution grid during overloading condition (time: 20 ms/div, voltage: 200 V/div, current: 2 A/div): (a) ST LV side frequency (top green) and ST LV side voltage (bottom), (b) DER detected frequency (top green) and DER output current (bottom), and (c) ST frequency set-point (green) and DER detected frequency (blue).



(a)



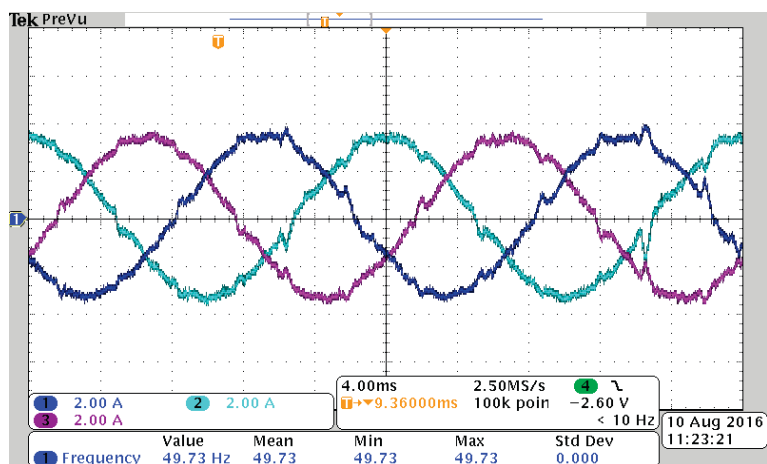
(b)

Figure 7.17: Comparison of ST LV side voltages with different control strategies during overloading condition ((time: 20 ms/div, voltage: 200 V/div): (a) CRC-controlled ST LV side voltage and (b) FORC-controlled ST LV side voltage.

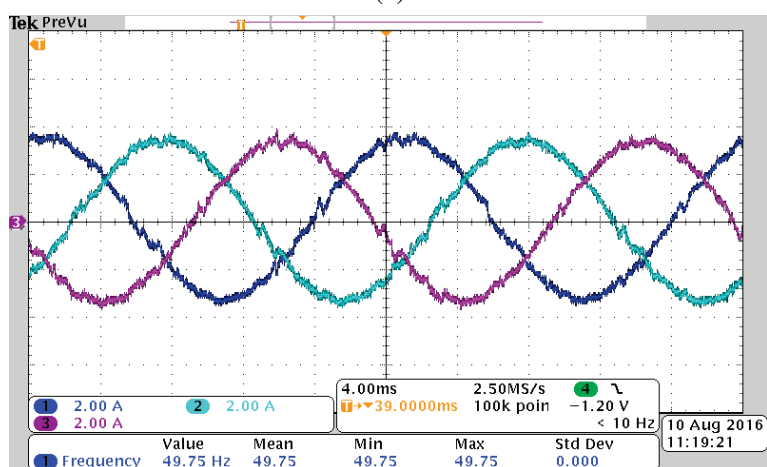
7.6 Summary of the Chapter

This chapter proposes a frequency-adaptive ST-fed distribution grid to address the overload and reverse power flow issues. In the proposed scenarios, the ST has the capability to modify its LV side frequency with the purposes of achieving power sharing among different DERs and establishing power balance between production and consumption of LV grid. In this way, the overload and reverse power flow issues can be largely avoided by decreasing or increasing the LV frequency. The frequency variation should comply with the local grid codes and the power sharing capability relies on the power rating of the grid-supporting converters (e.g., storage systems) in the grid.

Different from the existing control schemes for microgrids, the proposed FORC scheme ensures better performance of the ST and the DERs with droop control during frequency variations. From the control point of view, the FORC has advantages in terms of high control accuracy, easy implementation, and good robustness. It is seen that the FORC is insensitive to the delay of synchronization and communication, which is convenient for a semi-centralized



(a)



(b)

Figure 7.18: Comparison of DER currents with different control strategies during overloading condition ((time: 20 ms/div, current: 2 A/div): (a) CRC-controlled DER current and (b) FORC-controlled DER current.

control structure. Experimental results and case studies further confirms the power sharing capability of the proposed frequency adaptive ST-fed grid and the effectiveness of the FORC-based control under variable frequency condition.

8 Summary, conclusion and future research

8.1 Summary and conclusion

The contemporary electric grid is experiencing significant changes in terms of energy generation and transmission. Due to the emerging of renewables, the share of electricity production in the distribution grid is gradually shift from concentrated power plants through transmission line to DERs installed locally. From the power loss point of view, the wide installation of DERs can largely reduce the power transfer through the transmission line and thus decrease the losses. Nevertheless, new challenges are coming along with the DERs and the fast booming EV market, because of their intermittent energy production feature, utilization of grid-interfaced power converters, and unexpected spread as well as power injection during grid planning. The challenges rise the grid issues including control interactions, grid resonance, decreased system inertia, and power quality violation, and so on. Though solutions have been proposed to address these issues, they are usually targeting specific issues and each of them requires a specific algorithm, control structure, and infrastructure.

To address the grid issues, the ST-fed LV grid concept has been introduced in this thesis. The ST is a solid-state transformer adopted as intelligent substation with control and communication functionalities. It can provide better controllability of grids and meanwhile exploit potentials of the grids. To well understand the concept as well as advantages, a ST-fed grid paradigm is presented in Chapter 2, where the conventional power transformer is replaced by a three-stage ST. Ancillary services are provided to different utilities and customers by ST. For each ancillary service, it requires corresponding control strategies and grid synchronization schemes. The detailed control and synchronization requirements are presented in this chapter.

Detailed control strategies of each ST stage are illustrated in Chapter 3. In particular, the design and analysis of the current control of the MV converter and the voltage control of the LV converter are discussed. In addition to the basic voltage control, advanced control strategies or measures are required to deal with the issues in LV grid, but control challenges are coming with them. This thesis concentrates on four different control challenges: control interaction and harmonic instability, resonance damping and identification, modeling and stability of grid converter considering PLL, and harmonic control strategy for grid frequency variation. The solutions to these challenges by means of the ST LV converter are proposed in Chapter 4 to 7.

To cope with expected harmonic instability problem, the stability conditions of LV grid when using different voltage control strategies have been studied in Chapter 4. Considering the features of a distribution grid, both passive loads and grid-converter-based devices under various conditions are taken into account. The analysis and results show that the multiloop voltage control with the measured voltage feedforward and the load- and inductor-current inner loop is an optimal solution to guarantee stable operation of a ST-fed grid. When using grid-converter-based devices, grid converter using the grid current feedback is recommended

since it is less likely suffering from the harmonic stability in such grid. It is worth noting that the resistive component of the distribution network can benefit the stable operation and thus the line length and type selection are important. For instance, a case study in this chapter shows that using UG-02 cable in the CIGRÉ benchmark grid can avoid the harmonic instability comparing to other cables, under same distance to the ST LV converter.

In order to alleviate the LV grid resonances caused by the high-order filters of grid converter, active damping methods and online resonance identification have been developed for the ST LV converter in Chapter 5. Unlike the conventional active damping, the idea is to directly reshape the grid impedance/resonance by means of the ST which is connected to the whole LV grid in series. Two filter-based active damping: LEF- and LPF-based active damping, are both robust and not sensitive to the parameter uncertainties, which can bear up to $\pm 50\%$ system parameter variation. Both of the active damping methods not only effectively damp the grid resonances but also improve the stability margin of the overall system. Especially when using the LEF-based active damping, it implies a direct connection between the system stability margin and the compensation angle of the LEF: up to 45° phase margin improvement could be achieved. Online resonance identification implemented in the ST further strengthens the resonance alleviation capability and ensures the stable operation of the grid under various condition. By using the vector fitting method, the time-domain data obtained from the resonance identification can be translated to the transfer function in the frequency-domain. This allows the ST to carry out stability analysis in real time.

In Chapter 6, another important factor, synchronization of grid converter with the stability concern, is investigated. The existing research from the literature focuses on the static stability caused by the grid synchronization in the distribution grid with conventional power transformer. To assess the stability during transients, for example, large phase jump due to grid fault, a more accurate model of PLL-synchronized grid converter is developed in this chapter. The model can accurately represent the behaviors of a grid converter during phase jump up to 38° , comparing to 7° of the conventional model. The model is compatible to the impedance-based stability criterion and therefore extends the criterion to the phase jump case. Like the case in conventional grid, a higher BW PLL is more likely to incur instability. To achieve stable operation in a ST-fed grid, a virtual impedance-based stabilization method is proposed for the ST LV converter. In this way, the ST can prevent the instability caused by the synchronization.

Since the ST LV converter independently controls the voltage waveform, it gives the possibility to vary the voltage amplitude and frequency to interact with the grid-supporting devices to limit reverse power flow and transformer overload. With this consideration, the frequency adaptive ST-fed grid paradigm is proposed in Chapter 7. When reverse power flow happens, the LV grid frequency increases and the grid-supporting devices with droop controllers absorb the surplus power (e.g., BESS) or reduce the power generation (e.g., grid-supporting DER). When transformer overload happens, the grid frequency decreases and the grid-supporting devices increase power production, reducing the power demand from the grid. To deal with the control performance degradation during frequency variation, a fre-

quency adaptive control strategy: FORC, is proposed, and is able to maintain good control performance at arbitrary frequency. The FORC only consumes a small number of sums and multiplications, and can be easily plug into a multiloop voltage controller given in Chapter 4.

8.2 Research contribution

Contributions for the stability analysis of ST voltage control strategies

- Model and methodology were developed, where the stability conditions of the ST-fed LV grid using different voltage control strategies can be evaluated
- Stability and power quality evaluation were made for all multiloop voltage control strategies considering features of ST-fed grid
- Stability condition was assessed when different control strategies utilized for local DERs
- A superior multiloop voltage control was found and practical consideration was given to offer stable operation of the ST-fed LV grid

Contributions for the resonance damping of ST-fed grid

- A comprehensive analysis of ST-fed LV grid with consideration of filter resonances, passive loads and line impedance was made
- Critical points of the ST-fed grid due to resonances were identified under various operation conditions
- Filter-based active damping stabilization methods were proposed to damp resonances
- Parameter design criteria and robustness analysis were given to adapt to grid variations
- A real time LV grid impedance estimation for online analysis as well as online stabilization was designed

Contributions in the field of stability issues caused by synchronization

- For static analysis, an impedance-based model using the small-signal technique was developed
- For dynamic analysis, small-signal technique with large-angle approximation was used and an impedance-based model for the case of large phase perturbation was developed
- The developed models were used for assessing stability of both conventional distribution grid and ST-fed grid
- A stabilization method based on virtual impedance by means of ST LV converter was proposed to address the stability issue caused by grid synchronization

Contributions for the frequency adaptive ST-fed grid

-
- A frequency adaptive ST-fed grid was developed to address overload and reverse power flow issue
 - A frequency adaptive control strategy: FORC was proposed for controlling fundamental signal and eliminating harmonics, during variable frequency condition
 - Control design of the FORC-based ST voltage control and DER current control were given
 - Stability analysis of FORC-based system was presented and the impacts of synchronization/communication delay on the FORC were discussed

8.3 Future research

For ensuring stable operation and high performance of ST-fed grid, the model of the system, stability analysis methodology, resonance damping, and harmonic elimination are of major importance. This work has illustrated the modeling of the LV ST-fed grid, stability assessment of voltage control, resonance issues and damping methods, modeling and stability issues related to grid synchronization, and harmonic control for grid frequency variation.

In the author's opinion, the current challenges and remaining issues that the future research must address are:

- The model of the ST LV converter as well as the LV grid components has been developed. However, it is worth noting that the effects of the dc grids have been ignored in the analysis with the decoupling assumption. It has been seen that the impacts of dc grid are possibly minor in the HVDC application under most circumstances, but they could deteriorate the system stability especially harmonic stability when the penetration level of dc grid components is considerable. For ST-fed grid, when MVDC system and large amount of storage systems connected to the MV and LV dc buses, the impacts of the dc grids can no longer be neglected. In this regard, full model including both ac and dc grid components as well as their controls must be developed. Stability analysis with consideration of the full model should be carried out to firstly identify the new critical points introduced by the dc grids and then solutions must be given to guarantee the stable operation of the overall grid.
- Different voltage control strategies have been evaluated in terms of stability and power quality. However, this thesis considers the voltage control performance for the normal operation, namely the voltage control evaluations for the ST providing ancillary services have been neglected. With this consideration, performance evaluation and stability assessment of different voltage control strategies for various ancillary services should be studied. For instance, performance and stability during frequency variation and two phases operation due to a fault. Analysis must be developed to carefully evaluate the performance and assess the stability conditions when carrying out different ancillary services.
- Harmonic stability is one specific stability problem due to the interactions of control dynamics and filter resonances of the power converters. In addition, there are various types of stability problems seen in conventional power systems, with comprehensive definitions and classification [107]. When interconnecting with ST-fed grids, different forms of system instability could evolve in terms of their fundamental causes and manifestations. A comprehensive study has to be carried out in order to clearly understand the causes and phenomenons of different types of instability when the ST-fed grid is taken into account, and the relation to the design and operation is required which can be a possible guideline for the control design and scenario planning of such systems.
- It has been shown that communication techniques are widely used in the operation of ST-fed grid. In the thesis, it has been discussed only the communication requirements

for various scenarios and ancillary services. Further studies have to derive standard model of a ST-fed grid considering the communication effects like delay, data loss, and jitter. Stability analysis considering the communication uncertainties should be carried out to study the impacts of communication on the component level and the whole system level.

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10 Attachment

10.1 Publications related to this thesis

- J1 M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa and Z. X. Zou, "The smart transformer: impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46-58, Summer 2016.
- J2 G. Buticchi, G. De Carne, D. Barater, Z. Zou, and M. Liserre. "Analysis of the frequency-based control of a master/slave micro-grid." *IET Renewable Power Generation*, vol. 10, no. 10, pp. 1570-1576, 2016.
- J3 G. De Carne, Z. Zou, G. Buticchi, M. Liserre and C. Vournas, "Overload control in smart transformer-fed grid," *Applied Science*, vol. 7, no. 2, pp. 208, 2017.
- J4 Z. X. Zou, G. De Carne, G. Buticchi and M. Liserre, "Smart transformer-fed variable frequency distribution grid," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 749-759, Jan. 2018.
- J5 Z. X. Zou, G. Buticchi and M. Liserre, "Analysis and stabilization of a smart transformer-fed grid," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1325-1335, Feb. 2018.
- J6 G. De Carne, G. Buticchi, Z. Zou and M. Liserre, "Reverse power flow control in a ST-fed distribution grid," *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 3811-3819, July 2018.
- J7 Z. X. Zou, F. Hahn, G. Buticchi, S. Gunter and M. Liserre, "Interleaved operation of two neutral-point clamped inverters with reduced circulating current," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10122-10134, Dec. 2018.
- J8 Z. X. Zou, G. Buticchi and M. Liserre, "Grid identification and adaptive voltage control in a smart transformer-fed grid," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2327-2338, March 2019.
- J9 Z. Zou, R. Rosso and M. Liserre, "Modeling of the phase detector of a synchronous-reference-frame phase-locked loop based on second-order approximation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, in press.
- J10 Z. Zou and M. Liserre, "Modeling phase-locked loop-based synchronization in grid-interfaced converters," *IEEE Transactions on Energy Conversion*, in press.
- K1 Z. Zou, M. Liserre, Z. Wang, M. Cheng and S. Fan, "Resonance damping in a smart transformer-based microgrid," *Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Yokohama, 2015, pp. 956-964.
- K2 Z. Zou, G. De Carne, G. Buticchi and M. Liserre, "Frequency adaptive control of a smart transformer-fed distribution grid," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 3493-3499.

- K3 G. De Carne, Z. Zou, G. Buticchi and M. Liserre, "Variable frequency voltage control in a ST-fed grid by means of a Fractional-Order Repetitive Control," IEEE International Symposium on Industrial Electronics (ISIE), Santa Clara, CA, 2016, pp. 1230-1235.
- K4 Z. X. Zou, G. Buticchi and M. Liserre, "Control and communication in the smart transformer-fed grid," 2016 IEEE 21st International Conference on Emerging Technologies and Factory Automation (ETFA), Berlin, 2016, pp. 1-9.
- K5 Z. Zou, G. Buticchi, M. Liserre, A. M. Kettner and M. Paolone, "Voltage stability analysis using a complete model of grid-connected voltage-source converters," IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.
- K6 C. Kumar, Z. Zou and M. Liserre, "Smart transformer-based hybrid grid loads support in partial disconnection of MV/HV power system," IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.
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- K8 Z. Zou et al., "Interleaved operation of parallel neutral-point clamped inverters with reduced circulating current," IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 5254-5261.
- K9 Z. Zou, F. Hahn, G. Buticchi, M. Andresen and M. Liserre, "Optimized modulation in parallel neutral-point clamped inverters for circulating current reduction: A space vector analysis," Annual Conference of the IEEE Industrial Electronics Society (IECON), Beijing, 2017, pp. 7824-7830.
- K10 R. Rosso, G. Buticchi, M. Liserre, Z. Zou and S. Engelken, "Stability analysis of synchronization of parallel power converters," Annual Conference of the IEEE Industrial Electronics Society (IECON), Beijing, 2017, pp. 440-445.
- K11 Z. Zou and M. Liserre, "Study of phase-locked-loop-based synchronization of grid inverter during large phase jump," IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 7128-7134.
- K12 R. Zhu, Z. Zou and M. Liserre, "High power quality voltage control of smart transformer-fed distribution grid," Annual Conference of the IEEE Industrial Electronics Society (IECON), Washington, D.C., 2018, pp. 5547-5552.
- K13 R. Rosso, S. Engelken, Z. Zou, V. Willich and M. Liserre, "Parameter sensitivity analysis of SPC-based control under different grid conditions," Annual Conference of the IEEE Industrial Electronics Society (IECON), Washington, D.C., 2018, pp. 2404-2409.

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- K14 F. Cecati, M. Andresen, R. Zhu, Z. Zou and M. Liserre, "Robustness analysis of voltage control strategies of smart transformer," Annual Conference of the IEEE Industrial Electronics Society (IECON), Washington, D.C., 2018, pp. 5566-5573.

10.2 Curriculum Vitae

Name:

Zhi-Xiang Zou

Date of birth:

30.06.1985

Place of birth:

Wuxi, Jiangsu

Nationality:

Chinese

Education:

2003 - 2007: School of Electrical Engineering at the Southeast University, Nanjing, Jiangsu, China (Bachelor of Science)

2009 - 2014: School of Electrical Engineering at the Southeast University, Nanjing, Jiangsu, China (Doctor of Philosophy)

Work experience:

2007 - 2009: Engineer at the State Grid Electric Power Research Institute, Nanjing, Jiangsu, China

Since 2014: Scientific staff member at the Chair of Power Electronics at Christian-Albrechts-Universität zu Kiel