

# Modular Power Converters for Smart Transformer Architectures

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Levy Ferreira Costa

Kiel, 14.06.2018



*For Nathércia*



*"Se você vier me perguntar por onde andei  
No tempo em que você sonhava  
De olhos abertos lhe direi  
Amigo, eu me desesperava."*

Belchior



*“The greatest scientific discovery was the discovery of ignorance.”*

Yuval Noah Harari



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# Contents

<b>Kurzfassung</b>	<b>xix</b>
<b>Abstract</b>	<b>xxi</b>
<b>1 Fundamentals of Power Electronics-Based Transformer</b>	<b>1</b>
1.1 Concepts: From Solid-State Transformer to Smart Transformer . . . . .	6
1.2 Solid-State Transformer and Smart Transformer Architectures Overview . . . . .	9
1.2.1 Traction . . . . .	11
1.2.2 Electric Distribution Grid Application . . . . .	13
1.2.3 Discussion . . . . .	18
1.3 ST Architecture Classification . . . . .	19
1.3.1 Power Conversion Stages . . . . .	19
1.3.2 Modularity . . . . .	20
1.3.3 Modularity Level . . . . .	22
1.4 ST Architecture Selection for Electric Distribution System	23
1.4.1 Heart Project: Highly efficient and reliable Smart Transformer . . . . .	23
1.4.2 Architecture concept selection . . . . .	24
1.4.3 Power Routing Approach for Modular System . . . . .	25
1.5 Goal and Contributions of the Thesis . . . . .	28
1.6 Outline of the Thesis . . . . .	29
<b>2 Smart Transformer: Architectures and Power Converters</b>	<b>33</b>
2.1 ST Architecture concept . . . . .	35
2.2 Power Converter Topology: MV AC-DC Stage . . . . .	36
2.2.1 Modular Multilevel Converter (MMC) . . . . .	38

2.2.2	Cascaded H-Bridge (CHB) . . . . .	39
2.2.3	Comparison and Discussion . . . . .	42
2.3	DC-DC Stage . . . . .	44
2.3.1	Requirements . . . . .	45
2.3.2	Basic Module Topologies . . . . .	46
2.3.3	Three-Phase DAB . . . . .	50
2.3.4	Multiple Active Bridge . . . . .	54
2.3.5	Series Resonant Converter . . . . .	57
2.3.6	Full-Bridge Topology . . . . .	60
2.3.7	Comparison and Discussion . . . . .	61
2.4	LV AC-DC Stage . . . . .	64
2.4.1	2-Level VSI . . . . .	65
2.4.2	3-Level NPC . . . . .	66
2.4.3	Discussion . . . . .	67
2.5	Smart Transformer Architecture . . . . .	68
2.5.1	Trade off: Number of Module / Semiconductor Voltage Rating . . . . .	72
2.5.2	Modulation and operation . . . . .	73
2.5.3	Reliability issues . . . . .	73
2.6	Summary . . . . .	74
<b>3</b>	<b>Series Resonant DC-DC Converter</b>	<b>75</b>
3.1	Topology of the SRC and Operation Modes . . . . .	76
3.1.1	General Theoretical Analysis . . . . .	77
3.1.2	SRC Analysis in DCM operation . . . . .	82
3.2	Reliability Assessment . . . . .	86
3.3	Design of the SRC for ST . . . . .	88
3.3.1	Losses Modeling . . . . .	90
3.3.2	Reliability Analysis . . . . .	94
3.3.3	Tank Circuit Parameter Selection . . . . .	97
3.3.4	High-Frequency Transformer Implementation and Tests . . . . .	97
3.3.5	Power Stage Hardware Implementation . . . . .	99
3.3.6	Experimental Results . . . . .	100
3.4	Fault Tolerance Capability . . . . .	102
3.4.1	Analysis of the HB-SRC . . . . .	104
3.4.2	Proposed Fault Tolerant Converter . . . . .	105
3.4.3	Generalization of the Fault Tolerance Approach . . . . .	111
3.4.4	Fault Tolerant Multilevel SRC and Bidirectional SRC . . . . .	117

3.4.5	Evaluation of the Proposed Fault Tolerance Approach . . . . .	119
3.4.6	Simulation and Experimental Validation of the Fault Tolerance Approach . . . . .	122
<b>4</b>	<b>Active Bridges DC-DC Converter</b>	<b>129</b>
4.1	DAB Converter: Theoretical Analysis . . . . .	130
4.1.1	Modulation Strategy . . . . .	131
4.1.2	Analysis of the DAB using the PSM . . . . .	132
4.2	QAB Converter: Theoretical Analysis . . . . .	138
4.2.1	Analysis of the QAB using the PSM . . . . .	139
4.2.2	Analysis of the QAB with TCM . . . . .	148
4.2.3	Evaluation and Comparison of the Modulation Strategies . . . . .	152
4.3	Evaluation of the MAB converter in ST application . . . . .	158
4.4	Design of the QAB Converter . . . . .	160
4.4.1	Operation Point . . . . .	161
4.4.2	Losses Analysis . . . . .	162
4.4.3	HFT Design . . . . .	167
4.4.4	Final Converter Design . . . . .	169
4.4.5	Power Stage Hardware Implementation . . . . .	172
4.4.6	Experimental Results . . . . .	173
<b>5</b>	<b>Smart Transformer Architecture Design</b>	<b>181</b>
5.1	Trade-off: Number of Modules versus Semiconductor Blocking voltage . . . . .	182
5.2	Cascaded H-Bridge Converter Analysis . . . . .	184
5.2.1	Semiconductors Design . . . . .	185
5.2.2	Capacitor Sizing . . . . .	188
5.3	Optimum Number of Modules . . . . .	188
5.3.1	Power Semiconductors . . . . .	193
5.3.2	Capacitor Bank Sizing . . . . .	194
5.3.3	Cooling System Design . . . . .	197
5.3.4	Auxiliary Components . . . . .	198
5.3.5	Optimum Number of Modules: Cost vs Performance . . . . .	198
5.4	Performance and Economic Analysis of QAB in ST . . . . .	207
5.4.1	Design Consideration of the Units . . . . .	209
5.4.2	HFT Design Considerations . . . . .	211
5.4.3	Comparative Evaluation . . . . .	214
5.4.4	Discussion . . . . .	221

5.5	Control System Description . . . . .	222
5.5.1	MV Stage Control System . . . . .	224
5.5.2	DC-DC Stage Control System . . . . .	225
5.6	Simulation Results . . . . .	228
5.6.1	Steady-State Operation . . . . .	230
5.6.2	Dynamic Operation - Load Variation . . . . .	230
5.6.3	Summary . . . . .	234
<b>6</b>	<b>Smart Transformer Demonstrator</b>	<b>239</b>
6.1	Hardware Description . . . . .	240
6.1.1	Power Platform . . . . .	240
6.1.2	Control Platform . . . . .	245
6.2	Final Assembly and Test Set-up . . . . .	247
6.2.1	Final Assembly . . . . .	247
6.2.2	Test Set-up Description . . . . .	248
6.3	Experimental Results . . . . .	249
6.3.1	Power Routing Application - System's Performance Analysis . . . . .	254
6.4	Conclusion . . . . .	256
<b>7</b>	<b>Conclusion and Outlook</b>	<b>259</b>
7.1	Summary . . . . .	259
7.2	Conclusion . . . . .	260
7.2.1	Power Converters Level . . . . .	261
7.2.2	System Level . . . . .	263
7.2.3	Device Level . . . . .	263
7.2.4	General Conclusions . . . . .	264
	<b>Appendices</b>	<b>267</b>
<b>A</b>	<b>Failure Analysis of the DC-DC Converter: A Survey</b>	<b>269</b>
A.0.1	Methodology of the Study . . . . .	272
A.0.2	Results . . . . .	274
A.1	Improving the Converter's Availability: Solutions . . . . .	276
A.1.1	Oversize components . . . . .	278
A.1.2	Redundancy . . . . .	279
A.1.3	Fault Tolerant Approach . . . . .	281
A.2	Conclusion . . . . .	283
	<b>Nomenclature</b>	<b>285</b>

<b>List of Publications</b>	<b>289</b>
<b>Bibliography</b>	<b>293</b>
<b>Curriculum Vitae</b>	<b>315</b>



# Kurzfassung

Die Integration der dezentralen Energieversorgung und die neuartigen Lasten wie Elektrofahrzeuge, führen zu neuen Anforderungen hinsichtlich der Netzqualität, Zuverlässigkeit und Spannungsregelung im elektrischen Verteilnetz. Ein neuartiger leistungselektronischer Konverter hat sich als eine gute Technologie herausgestellt, um eine Spannungsregulierung bereitzustellen, während die Lasten und die Integration von dezentralen Energieerzeuger effizient verwaltet werden können. Dieses neue Gerät ist der Smart Transformer (ST). Der ST ist ein Leistungselektroniksystem, der wie ein Niederfrequenz-Transformator arbeiten soll, jedoch mit reduziertem Volumen und Gewicht (aufgrund seines Hochfrequenzbetriebs) und mit fortschrittlichem Steuer- und Kommunikationssystem für die Anwendung in Verteilnetzen.

Das ST-Konzept wurde in der Fachliteratur ausführlich diskutiert und viele Architekturen wurden vorgeschlagen. Ein dreistufiges System, bestehend aus Mittelspannungs-AC-DC-Wandler, einem DC-DC-Wandler und einem ausgangsseitigen Wechselrichter stellt die vollständige Entkopplung zwischen einzelnen Stufen sicher. Damit ist es die beste Option für die elektrischen Verteilnetze. Obwohl die Anzahl der Leistungsverarbeitungsstufen definiert ist, ist die Konzeptualisierung und das Design immer noch eine große Herausforderung, da eine grosse Anzahl an Konvertertopologien für jede Stufe verfügbar ist und diese unterschiedlich kombiniert werden können. Diese Arbeit beschreibt die Konzeption und den Entwurf einer ST-Architektur für die Anwendung in elektrischen Verteilnetzen, unter Berücksichtigung der am besten geeigneten Architekturen und Topologien.

Die unterschiedlichen ST-Architekturen werden in Kapitel 1 diskutiert und klassifiziert, wobei die Anzahl der Leistungsverarbeitungsstufen und die Modularität berücksichtigt werden. Aufgrund der Mittel-

spannung bei der Leistungsumwandlung wird der modulare Ansatz verwendet, um die Spannung zwischen den Modulen aufzuteilen, was den Einsatz von Niederspannungskomponenten ermöglicht. Weitere Vorteile des modularen Ansatzes sind: Fehlertoleranz durch Redundanz, Skalierbarkeit in Spannung und Leistung, Möglichkeit zur Verwendung von Niederspannungskomponenten (für bessere Performance und große Auswahl an Komponenten). Die Stromrichter werden in Kapitel 2 diskutiert. Für die Mittelspannungs-Seite wird eine kaskadierte Vollbrücke (CHB) als die aussichtsreichste Topologie identifiziert, während für die DC-DC Stufe der Serien- Resonanzkonverter (SRC) und die Multiple Active Bridge (MAB) gefunden werden. Der DC-DC Wandler ist die komplizierteste Stufe der ST-Architektur, weshalb der SRC und der MAB ein eigenes Kapitel in dieser Arbeit haben. Für die Niederspannungsseite können die wohlbekanntesten Topologien (z.B. 3-Level oder 2-Level Wechselrichter mit Spannungszwischenkreis) verwendet werden, die ausgereift und industriell erprobt sind und daher in dieser Arbeit nicht weiter untersucht werden. Der SRC Konverter ist in Kapitel 3 beschrieben, und ein optimiertes Design zur Verbesserung der Effizienz und Zuverlässigkeit wird vorgestellt. Zusätzlich wird in diesem Kapitel eine fehlertolerante Topologie des SRC vorgestellt. In gleicher Weise beschreibt Kapitel 4 den MAB Konverter und ein optimiertes Design zur Verbesserung der Effizienz und Kosten wird diskutiert. Der MAB Konverter hat einen wichtigen Vorteil gegenüber dem SRC: Die Steuerfähigkeit von Spannung und Strom. Daher wird die ST Architektur mit dem MAB Konverter entwickelt.

Die Untersuchung zur optimalen Anzahl von Modulen der ST Architektur wird in Kapitel 5 durchgeführt. Abschließend werden in Kapitel 6 der Aufbau und die experimentelle Verifizierung eines Demonstrators einer dreiphasigen ST Architektur basierend auf dem CHB und MAB Konverter diskutiert. Der Hardware Prototyp wurde im Labor getestet und die experimentellen Ergebnisse bestätigen die theoretische Analyse.

# Abstract

The large integration of renewable energy sources (RES) and intermittent loads (e.g. electric vehicles) into the utility grid has imposed new challenges to the electric distribution network with respect to the voltage regulation, power quality and reliability. To keep the voltage regulated and improve the power quality of the electric distribution grid, special devices such as online tap changer, STATCOM, etc, have been normally used. In this context, a particular devices based on power electronics converters has emerged as a promising technology to provide voltage regulation, while managing the loads and RES integration efficiently. The device in question is the Smart Transformer (ST). The ST is a power electronics system supposed to replace the traditional low frequency transformer in the electric distribution grid, providing isolation and voltage adaptation. In addition, the ST has an advanced control system, enabling grid support, and operates in high frequency, reducing the volume and weight of the system.

The ST has been widely discussed and many architectures have been proposed. The three stages architecture composed by a Medium Voltage (MV) AC-DC stage, a DC-DC stage and a Low Voltage (LV) DC-AC stage has been demonstrated to be the most compelling configuration, because it ensures better decoupling between the input and output voltage, when compared to other architectures. Even though the number of power processing stages is defined, the conceptualization and design of the architecture are still very challenging, because of the broad options of power converters available for each stage, and how they can be connected. In this context, this thesis investigates the most promising architectures of the ST and power converters that should be used to fulfill the aforementioned requirements.

The ST architectures are discussed and classified in Chapter 1, con-

sidering the number of power processing stages and modularity. Because of the MV level involved on the power conversion, the modular approach is used to share the voltage among the modules, allowing the use of LV devices. Additional advantages of the modular approach are: fault-tolerance through redundancy, scalability in voltage and power, possibility to use low voltage rating devices (providing better performance and broad choice of devices).

The power converters are reviewed and discussed in Chapter 2. For the MV side, the Cascaded H-Bridge converter (CHB) is pointed out as the most promising topology, while for the DC-DC stage the Series Resonant Converter (SRC) and the Multiple Active Bridge (MAB) are highlighted. The DC-DC stage is the most challenging one for implementing the ST architecture, then the SRC and MAB have a dedicated chapter for each of them in this thesis. For the LV stage, the well-established topologies (e.g. 3 level voltage source inverter [VSI] or 2 level VSI) can be used, which are mature technology and, therefore, it is not investigated further in this work. The SRC converter is investigated in Chapter 3, where an optimized design to improve efficiency and reliability is presented. Additionally, a fault tolerant topology of the SRC is also presented in this chapter. The Chapter 4 is dedicated to the study of the MAB converter, in which a multi-objective optimization design focusing on efficiency and cost is carried out. The MAB converter has an important advantage over the SRC with respect to the control voltage. Then, the MAB is highlighted as a promising choice for the DC-DC stage of the ST.

From the system level perspective, studies about the optimum number of modules of the ST architecture are carried out in Chapter 5. In order to test the studied system, a three-phase ST demonstrator was constructed based on the CHB associated to the MAB DC-DC Converter. The prototype was tested, validating the theoretical analysis presented in the thesis.

# Chapter 1

# Fundamentals of Power Electronics-Based Transformer

**A** LONG many years, the electric distribution system has been well established as a passive network, where the electric power generators and loads had their roles well defined. The electric power plants produce the electricity, which is transmitted in high voltage (HV) by the long-distance lines and then distributed in medium voltage (MV) and low voltage (LV) level to the consumers [1–3]. The conventional low frequency transformer (LFT) is responsible to adapt the voltage levels between the transmission and distribution systems and also between two distribution systems with different voltages, as depicted in Fig. 1.1 (a). In the classic passive distribution grid, all electricity are generated by the large power plants, while it is fully consumed by the end users, implying in an unidirectional power flow [1].

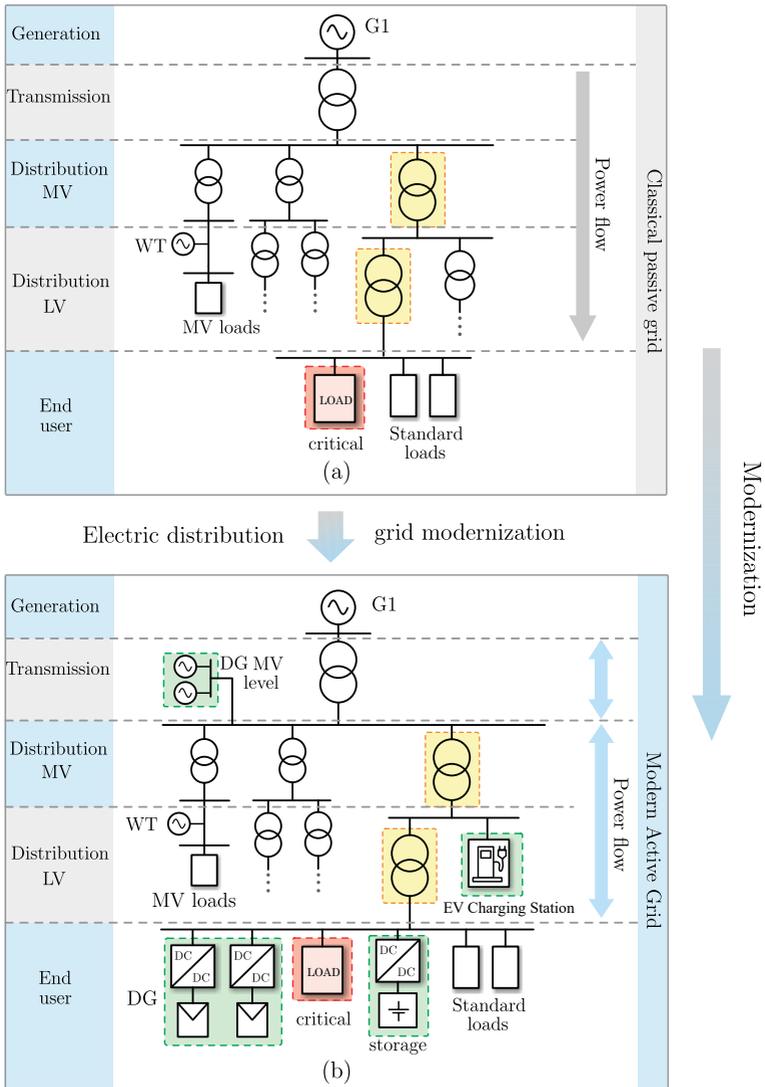
With the evolution of the power electronics and the need to reduce the emission of greenhouse gases, more distributed generator (DG) based on renewable energy sources and more efficient loads have been greatly developed and integrated into the electric distribution network [1–4].

The DG systems (e.g. PV system, wind farms, etc.) are integrated into the grid in different voltage levels, either in LV and MV, and they are typically located close to the loads, reducing transmission line con-

gestion and system losses in some instances [3]. Nevertheless, the large DG penetration can have adverse impacts on the distribution grid reliability and power quality, like flickers generation due to the abrupt variation of produced power by the DG (e.g. when clouds pass by photovoltaic cells), low correlation between the electricity produced and load profiles (especially for wind systems), increase of the distribution line congestion due to dispersed resources if not well managed, etc [5]. Later, storage systems have been incorporated into the grid, in order to storage the exceeded energy produced by the DG and support the grid by improving the electric energy utilization. For instance, the battery storage systems can charge energy from the grid during the off-peak time (low electricity tariff) and discharge into the grid during the peak load demand, shaping the load demand for a flatter profile [5], and finally reducing the distribution line congestion [3,5]. Subsequently, the electric vehicle (EV) technology was greatly developed, which required the installation of charger stations into the distribution grid to fulfill the demand of the EVs [4,6]. From the grid reliability viewpoint, the EV integration has similar features to the storage system integration. However, short charge time has negative impact on the distribution network, like high peak demand and potential to increase congestion at distribution level [5].

The massive penetration of the aforementioned systems into the utility grid changed the infrastructure of the electric distribution network, and now more power electronics system are incorporated into the system. As a result, the power flow is no longer exclusively unidirectional (from the MV lines to the LV lines), but it can be bidirectional [1–4]. It introduced a modern scenario, where the electric distribution system became an active network, as presented in Fig. 1.1 (b). The upgraded system poses new challenges, and the concerns with power quality, reliability and voltage regulation has increased significantly. For instance, deviation of the voltage is not tolerated by the critical loads connected to the grid (e.g. navy, military, data processing facilities), leading to the mandatory use of special devices to regulate the grid voltage in the actual scenario [7,8].

To improve the power quality, voltage regulating devices such as on-load tap changer (OLTC) and/or step voltage regulators (SVRs) have been conventionally adopted, as depicted in Fig. 1.2 (b) [7,9–12]. However, it offers limited voltage regulation and slow dynamic response. Furthermore, the simultaneous response of the OLTC and the DG to

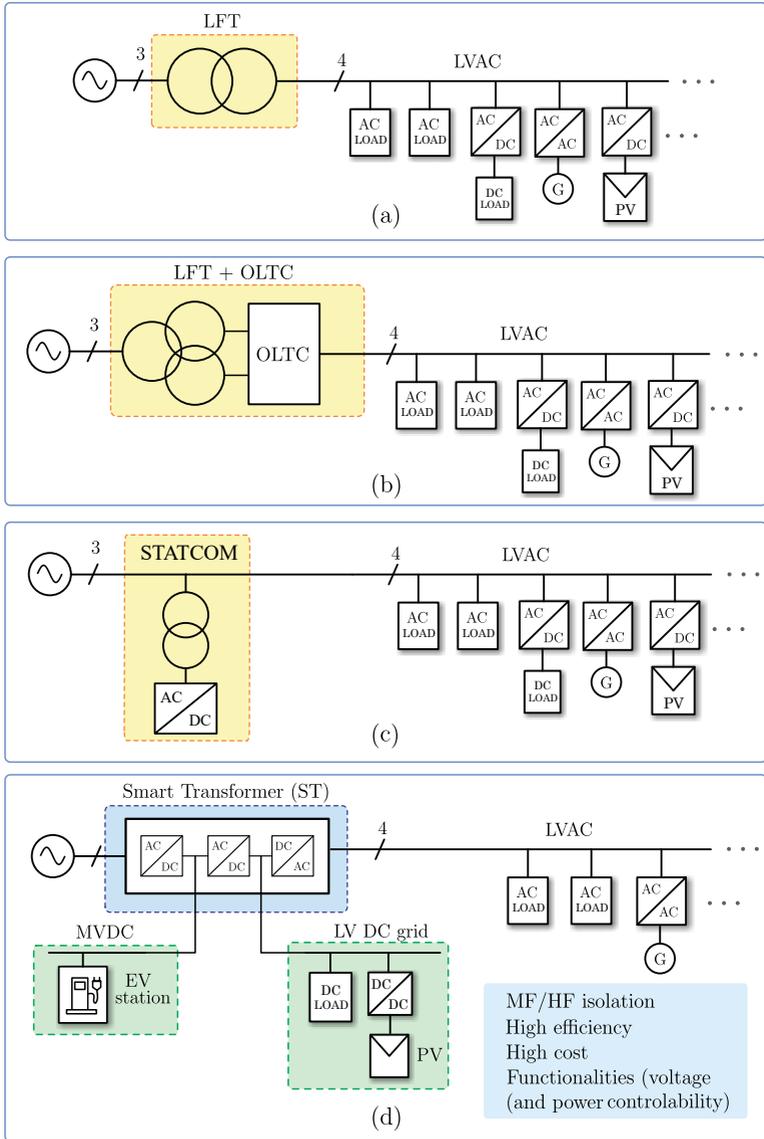


**Fig. 1.1:** Modernization process of the electric distribution system: (a) conventional passive distribution grid and (b) modern active distribution grid, highlighting the emerging sources and loads.

the voltage variation might result in conflicting operations under certain conditions. This may cause unexpected operation of the OLTC, implying in variation of the grid voltage [7]. The power electronics system, mainly the static compensator (STATCOM) as illustrated in Fig. 1.2 (c), plays a very important role to improve the power quality, reliability and voltage regulation. It offers a fast load voltage regulation to the distribution network and compensates the reactive power, improving the power quality. However, it is not widely adopted because of its high cost, considering the limited ancillary services that it can offer to the grid [13, 14].

In spite of the modernization of the electric grid, a crucial power device remained untouched for decades: the transformer. It has been considered the backbones of the electric grid, providing a power conversion with high efficiency (around 98% [8]), and relatively long lifetime (around 20 years [10]). On the other hand, the lack of control of the LFT makes the use of a voltage regulation device mandatory, and the OLTC is the standard solution. It reduces considerably the system reliability, because the OLTC is responsible for 41% of the failures, requiring preventive maintenance regularly [10–12]. Despite the long lifetime of the LFT, the lifetime of the combined system composed by the LFT and the OLTC drops to 2 to 5 years [10–12]. In contrast to that, the modernization of the transformer would offer significant benefits to the grid, because it could provide voltage regulation and improve the power quality, reducing the necessity of additional equipment to keep the system under control. In this circumstance, the concept of solid state transformer (SST) was introduced, which is defined as a power electronics based system supposed to replace the traditional LFT, but adding the advantages of volume and weight reduction and controllability of voltage and current [15–19]. Among these advantages, the possibility to provide ancillary services to the grid by means of the current and voltage control is the key point of the SST and it offers significant contribution to the power quality improvement.

To replace the traditional LFT, the SST needs to provide high efficiency, and reliability with low cost, which is very challenging, because of the considerable amount of power electronics involved in this system. Many researches have been focused on the development of this technology and many architectures have been proposed, focusing mostly on efficiency improvement and volume reduction. The current and voltage controllability, however, has been ignored in many publications and



**Fig. 1.2:** Simplified grid configuration considering voltage regulating devices: (a) standard distribution grid without voltage regulating device, (b) distribution grid regulated by the OLTC, (c) grid based on STATCOM and (d) configuration of the modern grid based on the ST.

most of the proposed SST architectures have limited control, though it is considered one of the most important requirement of this system.

In this regard, a new concept has been proposed: the Smart Transformer [19]. The ST is conceptualized as a SST with advanced control and communication features, with the aim to increase the functionalities, solving many of the grid problems imposed by its modernization. The wide range of new services offered by the ST creates working conditions very different than those of a standard transformer, making it even more difficult to cope with efficiency and reliability requirements. Even more importantly, the possibility to integrate DC networks in different voltage levels, as shown in Fig. 1.2 (d), contributes to the superiority of the ST. Apart from replacing the LFT, the ST provides also multiple ancillary services to the grid, avoiding the need of the additional devices used to support the grid. For that reason, the ST does not aim to compete directly with the LFT in terms of cost, efficiency and size, but it aims to replace (and subsequently compete) with the whole ordinary solution composed by the LFT and the voltage regulating devices.

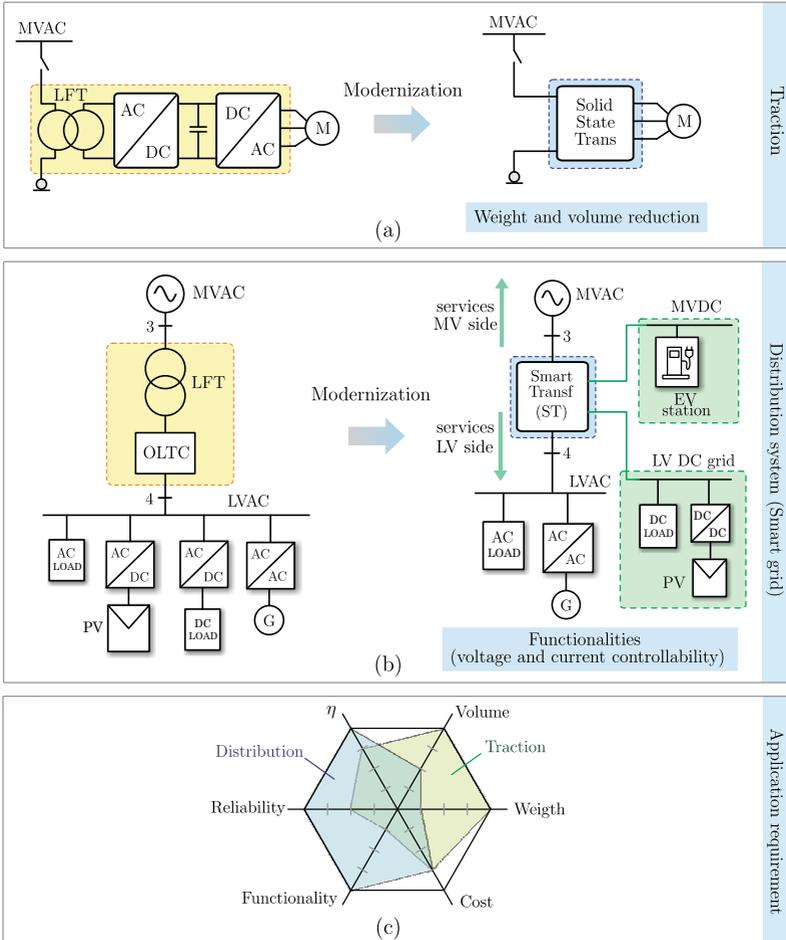
In overall, the ST can help solve system level challenges, but its implementation is a challenge in itself. In this regard, this work investigates the architectures and power converters to implement the ST, with the aim to make this system an enabling technology to solve most of grid problems [19]. General aspects and different concepts used for the ST are discussed next, while the system requirements are presented. Several power electronics converters can be used and combined to conceive a ST architecture and different architectures can be generated. Then, a literature review of the power converters and ST architectures is presented and the most appropriate candidates are analyzed in detail in this work.

## 1.1 Concepts: From Solid-State Transformer to Smart Transformer

The concept of electronic transformer was first introduced by [20] in the end of 1960s, where the main concept would be to adjust the output voltage by using the power electronics, while contributing for the size and volume reduction. In that time, there was no applicability for such apparatus, mainly because of the performance limitation of the available semiconductors on the market.

## 1.1. Concepts: From Solid-State Transformer to Smart Transformer

However, with the advance of the power electronics and semiconductors technology, new faster devices with lower switching energy were developed, enabling faster switching frequency operation. As a result, the volume and size the power converters were considerably reduced, bring advantages for those applications in which the power density is very



**Fig. 1.3:** Application of the Solid State Transformer: (a) Traction, (b) distribution, (c) requirements of the application.

important. At the same time, the classic solution used in traction for the electric locomotive were very heavy, bulky and inefficient, because of the low frequency transformer employed [21]. As power electronics converters were already required in this application to provide suitable DC voltage to the variable speed drive on the locomotive, the power electronics transformer (PET) offered several advantages in this regard. It could provide the suitable controlled and isolated DC voltage in a unique solution, offering yet volume and weight reduction (around 20% - 50%) and efficiency improvement (from 93% to 96%) [19, 21]. Thus, the PET became a reality in traction application. Fig. 1.3 (a) illustrates the conventional solution (state-of-the-art) used on locomotives, as well as the modern solution based on SST. The benefits offered by the SST in traction is limited to hardware (in terms of volume and weight reduction).

Even more importantly than hardware advantages, the SST can offer additional functionality when an appropriate communication and control system are incorporated to it [19]. Then, the potential to use SSTs as the enabling technology for smart grid functionalities in electric distribution becomes very high. This technology has received a lot of attention of the research community (even academia and industry) and it was cited as one of the most emerging technologies by Massachusetts Institute of Technology (MIT) Technology Review in 2010 [15, 16, 22]. The new functionalities in the form of ancillary services to the electric grid are discussed in [19, 23]. Among them, the reverse power flow condition (i.e. electric power flowing from LV to MV), storage integration, management of hybrid grids (DC and AC) and power quality improvement are highlighted. Then, in this application, the SST is not only supposed to replace the conventional LFT, connecting the medium-voltage (MV) grid to the low-voltage (LV) grid, but also to offer DC connectivity and services to both LV and MV grids, as highlighted in Fig. 1.3 (b). In this case, weight and volume advantages have a limited impact, while the efficiency, reliability and functionalities are the primordial requirements. The aforementioned functionalities, enabled by the advanced software communication and control system, make the SST a smart device, leading to the concept of smart transformer (ST).

Fig. 1.3 (c) shows the main requirements of the SST for both described application. While the volume and weight reduction are the most important requirement for traction application, the functionalities, reliability and efficiency play the most important role in electric

distribution grid application. Then the ST and the SST can be conceptualized as:

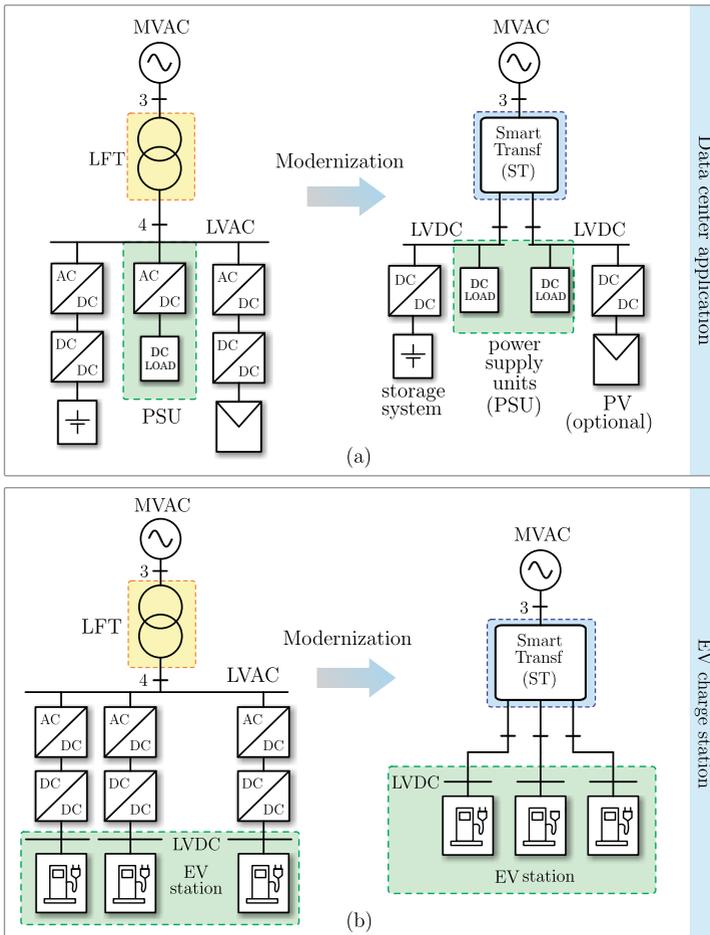
**Solid-State Transformer:** power electronics based system with galvanic isolation in medium or high frequency between the input and output with waveform conditioning capability. It is normally employed to replace the traditional transformer, offering as advantages the volume and weight reduction. Thus, the advantages offered by the SST are related to its power stage.

**Smart Transformer:** power electronics based system with galvanic isolation in medium or high frequency between the input and output with extra control functionalities, obtained through advanced communication and control system. In addition to the hardware advantage, its enhanced control makes the ST an powerful technology able to the provide ancillary services to the distribution grid, solving most of the problems posed by the grid modernization (cf. Section 1.1). This system is a remarkable technology able to fulfill most of the requirements for the implementation of a smart grid, either AC or DC.

Currently, new applications for the SST technology has emerged and data centers and fast charging station for electric vehicles are highlighted, as depicted in Fig. 1.4. In those applications, the SST needs to provide only DC voltage output, because of the load sort, implying in a different concept for the SST. In these cases, the SST is intended to connect the MV AC grid to a DC link, providing galvanic isolation among them, while maintaining the current and voltage control capability. Thus, regardless the concept presented in literature, galvanic isolation in medium or high frequency between the input and output and the output voltage/current control capability is generally mentioned.

## 1.2 Solid-State Transformer and Smart Transformer Architectures Overview

In the last two decades, many different SST and ST architectures have been proposed and discussed in literature for traction and distribution



**Fig. 1.4:** Emerging application of the Solid State Transformer: (a) data center, (b) fast charger station for electric vehicles.

grid applications. The most relevant architectures used in both application are reported next.

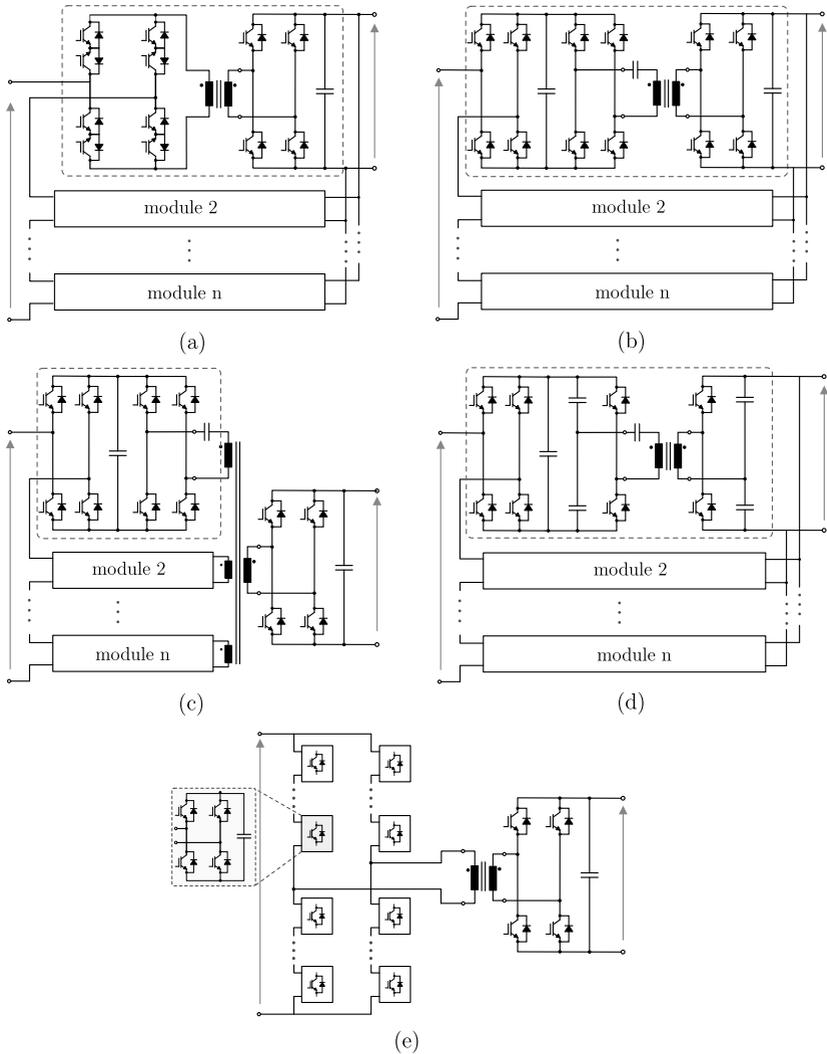
### 1.2.1 Traction

The weight and space saving and the high efficiency expected from the SST could lead to economical advantages to locomotive traction system. This technology has received the attention of the industries and a lot of research were carried out in this regards, focusing on weight, volume and cost reduction. In Europe, the railways are respecified as : single-phase AC lines with 15 kV /  $16^{2/3}$  Hz or 25 kV / 50 Hz [21]. The traditional system (cf. Fig. 1.3 (a)) using the LFT is a heavy (around 2 to 4 kg/kVA) and inefficient solution (around 90% to 92%). In this scenario, various SST have been proposed to improve the system performance, and the most relevant architectures are described as follow.

A SST based on the cycloconverter and using the modular approach was patent by ABB [24,25], that is one of the leader companies in that field. This architecture is depicted in Fig. 1.5 (a) and it uses 16 modules with HV 3.3 kV IGBT, resulting in a total of 192 devices. All of them operate in soft-switching, reducing the switching losses and allowing the use of 400 Hz switching frequency. Experimental results for a 1.8 MW system has demonstrated an efficiency of 94.5%, as well as volume and weight reduction of 20% and 50%, respectively, in respect to the conventional solution based on LFT (cf. Fig. 1.4 (a)).

In contrast to the previous solution, the Bombardier introduced a two-stage SST based on the front-end cascaded H-bridge (CHB) converter associated to an isolated DC-DC converter [26]. The CHB provides an intermediate and constant DC link to the DC-DC converters, as illustrated in Fig. 1.5 (b). This solution reduces the total volume and weight of the system in 30% and 50%, respectively, when compared to the classic solution.

Similarly, a modular system based on the CHB and a DC-DC converter was presented by Alstom in [27, 28]. However, instead to use several DC-DC converters, a single multiwinding medium frequency transformer connected to several bridges in the MV side and to a single H-bridge in the LV side is used, as depicted in Fig. 1.5 (c). Although this approach improves the power density (volume reduction of 55%) and efficiency (94%), the cost increases in 50%, making it infeasible. The high cost is explained by the great number of employed HV



**Fig. 1.5:** Overview of the proposed SST architecture for traction application: (a) modular cycloconverter (ABB, 2006) [24, 25], (b) modular two stage using the CHB (Bombardier, in 2007) [26], (c) modular two stage using a single multiwinding transformer (Alstom, 2007) [27, 28], (d) modular two stage based on the CHB and LLC DC-DC converter (ABB, 2013) [29, 30], (e) modular architecture based on the MMC (Siemens, 2005) [31, 32].

IGBT and the transformer design focus on the size reduction. According to [27], this cost can be reduced, but it will still remain higher than the traditional traction solution.

A new concept of the modular multilevel converter (MMC) was proposed by Glinka and Marquart in [31,32] and applied to traction system, as illustrated in Fig. 1.5 (e). Theoretical investigation has suggested an efficiency of around 97.9% for this approach. The main drawback is the large amount of energy stored in each module of the MMC, but low energy density. It means that the required capacitance in each module is considerable high, increasing then the weight and volume. Consequently, it does not bring significant advantages for the application and it has not being further developed.

The ABB company has presented its new SST in [29,30], which is based on a front-end CHB associated with a resonant DC-DC converter, as shown in Fig. 1.5 (d). The architecture is very similar to that one used by Bombardier [26], but the difference lies on the resonant tank, where a series LLC is used instead the series LC. The solution has presented an efficiency of 96% and weight reduction of 30%, making this one of the most suitable solution presented so far.

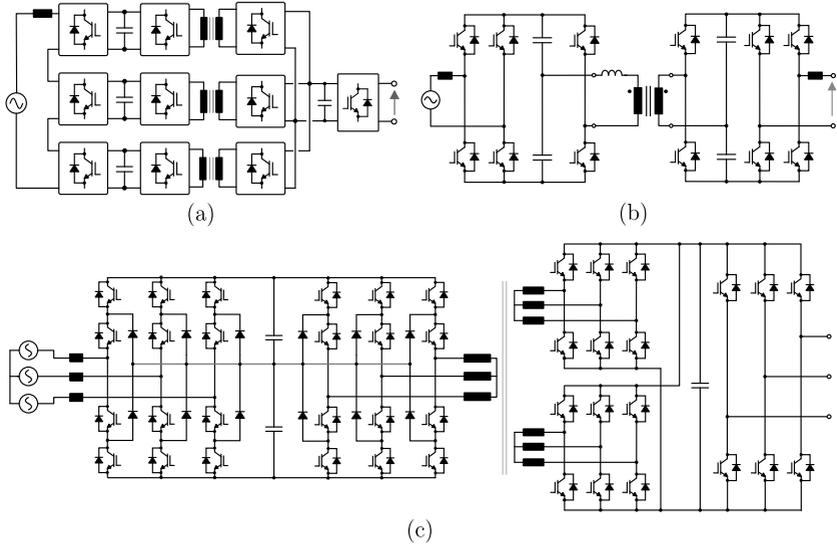
## 1.2.2 Electric Distribution Grid Application

In contrast to the traction, the electric distribution grid application requires different features. The attention must be shifted from volume and weight reduction to efficiency, reliability and functionality improvement. Among the numerous publications, only the most relevant publications are discussed herein.

The FREEDM center was one of the first research groups to give relevant contribution to this field. They proposed a modular architecture using three power conversion stages (i.e. AC-DC / DC-DC / DC-AC stages) and depicted in Fig. 1.6 (a) [16,17,33]. It is the first of three architectures proposed by this group, and then it was named as SST generation 1 (SST-gen1). To implement such structure, the employed converters are: CHB as the MV AC-DC conversion; Dual-Active-Bridge (DAB) as the isolated DC-DC stage; voltage source two-level inverter (VSI) for the LV DC-AC stage. The constant DC link offered by the three stage decouples the LV and MV sides, providing enough degree of freedom to implement the advanced control system required by the ST. Apart from the high efficiency provided by the employed converters,

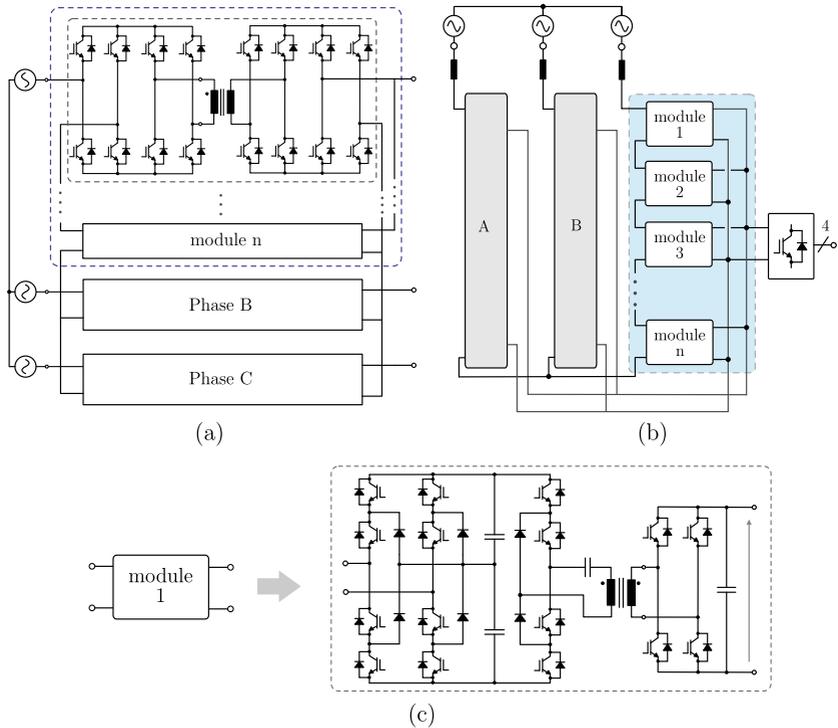
the modular structure allows the used of lower voltage rating devices, benefiting the efficiency and cost. Consequently, it became a standard architecture for ST and many other reports have been published focusing in its control and power management. Although high efficiency is expected, it was not demonstrated in [16].

Similarly, the FREEDM center has also proposed the SST generation 2 (SST-gen2) [34, 35] and 3 (SST-gen3) [36, 37], both based on three-stages, as shown in Fig. 1.6 (b) and (c). Differently from the previous one, the SST-gen2 and SST-gen3 are not modular, then special Silicon Carbide (SiC) semiconductors with high blocking voltage capability were customized for this project, in order to handle the MV involved. The SST-Gen2 is implemented using a 2-level converter on the AC-DC stage, SRC on the DC-DC stage and a 2-level VSI. Customized 15 kV SiC-MOSFETs are utilized in the MV side. A peak efficiency of 95.6% for the whole architecture was experimentally demonstrated,



**Fig. 1.6:** Overview of the proposed SST architecture for electric distribution grid application: (a) Modular architecture (FREEDM/SST-gen1) [16, 17, 33], (b) non-modular based on 10 kV SiC-MOSFETs (FREEDM / SST-gen2) [34, 35], (c) non-modular based on 15 kV SiC-IGBT (FREEDM / SST-gen3) [36].

which is considerably high assuming the number of power stages. The SST-Gen3 employs a 3-level converter for the AC-DC conversion, modified DAB in the DC-DC stage and a 2-level VSI. Likewise, customized 15 kV SiC-IGBTs are used in the MV side. According to the theoretical analysis presented in [36], the architecture is supposed to offer an efficiency of 96.75% for the entire system. However, only partial load has been tested experimentally, showing a peak efficiency of 94.44%. The two last architecture has a constant MVDC link, that can be available for connecting DC loads and sources in MV level. Thus, MVDC connectivity is highlighted as an additional advantage of these last two architectures over the first one.



**Fig. 1.7:** Overview of the proposed SST architecture for electric distribution grid application: (a) Modular architecture using 10 kV SiC-MOSFETs (General Electric) [38], (b) phase modular architecture (ETH) [39].

An advanced ST structure using also customized 10 kV SiC-MOSFETS on the MV side was proposed in [38] and it is depicted in Fig. 1.7 (a). This architecture is implemented by an indirect matrix converter connecting the MV and LV sides. This has caught the attention because of its high efficiency (97% according to [38]). The reason for such high performance is the customized devices employed, that are not commercially available, penalizing the cost. Its main drawback is the lack of the constant DC-link. It means that the LV and MV are not decoupled, limiting the control capability and consequently the services that this architecture can provide to the grid. Moreover, the DC link can not be available for direct connection of DC loads and sources.

A modular three-phase architecture, illustrated in Fig. 1.7 (b), is presented in [39], as the solution called Megalink. Its concept is similar to the one introduced in SST-gen1 by the FREEDM center and they differ by the topology of the basic module. The DC-DC stage is implemented using a SRC converter operating in open-loop. It simplifies the control system, but limits the implementation of extra functionalities. Although high performance is expected, no experimental validation has been presented.

A ST architecture used to connect two different MV grids is described in [40–42]. The architecture is part of the project Uniflex and it focused on the power management between the two grids. Since the hardware concept is the same used in SST-gen1 by the FREEDM center, it is not deeply discussed.

To save cost and increase the efficiency, different architectures based on a single power conversion stage (i.e. direct AC-AC conversion) and double power conversion stage (i.e. indirect matrix converter and an inverter) have been discussed [43–46]. However, these architectures have limited degree-of-freedom for the control implementation, making it infeasible for grid application. Moreover, the advantages in terms of cost and efficiency over the three-stages architecture have not yet been demonstrated. For these reason, these architectures were not considered in this overview.

**Tab. 1.1:** Comparative Analysis of the of the ST and SST Architectures

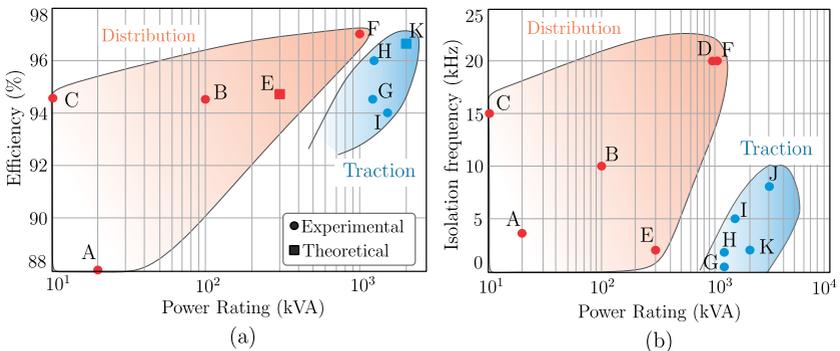
Distribution application						
Name	Project/group	Stages	Concept	DC-Link	Semiconductors	Ref
A	SST-1/FREEDM	3	Modular	LV	Si-IGBT 6.5 kV	[33]
B	SST-2/FREEDM	3	Non-modular	MV/LV	SiC-MOSFET 13 kV	[34, 35]
C	SST-2/FREEDM	3	Non-modular	MV/LV	SiC-IGBT 15 kV	[36, 37]
D	Megalink/ETH	3	Modular	LV	Si-IGBT 1.7 kV	[39]
E	Uniflex/ERC	3	Modular	no	Si-IGBT 1.7 kV	[40–42]
F	GE	2	Modular	no	SiC-MOSFETs 10 kV	[38]
Traction application						
Name	Company	Stages	Concept	Efficiency	Semiconductors	Ref
G	ABB	1	Modular	94.5%	Si-IGBT 3.3 kV	[24, 25]
H	ABB	2	Modular	96.2%	Si-IGBT 6.5 kV	[29, 30]
I	Alstom	2	Partially-modular	94%	Si-IGBT 4.5 kV	[27, 28]
J	Bombardier	2	Modular	96.2%	Si-IGBT 4.5 kV	[26]
K	Siemens	2	Partially-modular	97%	Si-IGBT 3.3 kV	[31, 32]

### 1.2.3 Discussion

The main features of the architectures discussed previously are summarized in Table 1.1. In traction application, the architectures are characterized to use commercialized HV Si-IGBT, two power processing stages, as well as the modular approach. The efficiency for each architecture for traction system is presented in Table 1.1. All of them provide higher efficiency and high power density, when compared to the ordinary solution using the LFT.

The three-stages architecture offers the decoupling between the input and output, besides the availability of at least one DC-link. Consequently, it is the preferable structure for grid application, as seen in Table 1.1. To handle the MV level, two approaches are commonly used: modular with commercial LV devices and non-modular with customized HV devices. Regardless the adopted concept, most of these architectures take advantage of the high performance wide-bandgap SiC devices. They offer lower conduction and switching losses compared to the standard devices and they are very promising in ST application.

Fig. 1.8 (a) shows the efficiency values available in the literature according to power of the system, as denoted in Table 1.1. For distribution system, very few ST demonstrators have presented solid results



**Fig. 1.8:** Performance comparison of the most relevant ST and SST architectures developed by industries and universities: (a) achieved efficiency compared to the power rating, (b) isolation frequency in function of the power rating.

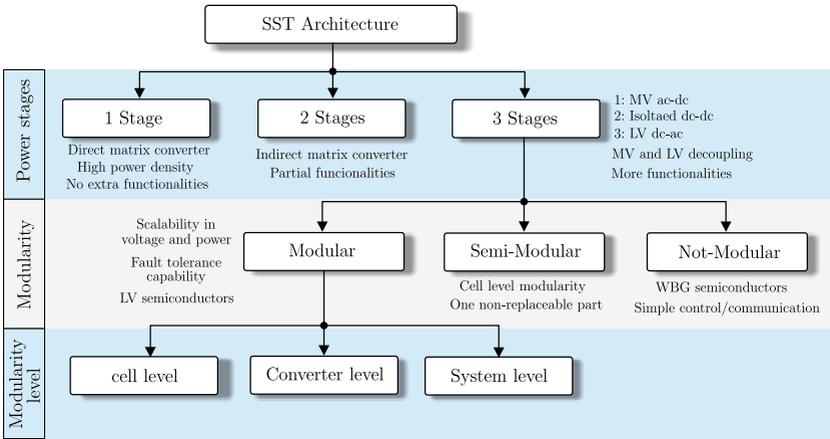
in literature so far. The available data show that the efficiency achieved by this kind of system is around 94.5% to 97%. For traction system, the ST efficiency is in the range of 94.5% to 96%, according to the available data provided experimentally (excluding the theoretical one). Although the ST architectures in distribution use more power stages compared to those used in Traction, their performance is potentially higher, because the utilized wide-bandgap semiconductors that plays a very important role in this regards. Fig. 1.8 (b) shows the isolation frequency for each ST architecture presented in Table 1.1, according to the power level. In traction, the isolation frequency is normally bellow 10 kHz, whereas in distribution system is mostly around 10 kHz to 20 kHz. The limitation of switching frequency in ST for traction is explained by the fact of HV Si-IGBT are normally used to save cost, implying in more switching losses and switching frequency limitation.

## 1.3 ST Architecture Classification

The need to provide high efficiency and high reliability, offering new functionalities has a direct impact on the ST architecture selection. To assist the proper structure selection, Fig. 1.9 provides an overview of the possible architectures.

### 1.3.1 Power Conversion Stages

The most discussed classification is related to the number of power conversion stages, that can be: single-stage, two-stages or three-stages. The single-stage is normally implemented by a direct isolated matrix converter and it is characterized to have high power density, because of the absence of the DC-link capacitors. However, the LV and MV are not decoupled, limiting the control capability. The two-stage topology is usually based on the indirect matrix converter and an inverter. This structure might present up to one constant DC-link, improving the controlability in respect of the single-stage structure. However, the two-stage structure offers limited functionalities. The three-stages is implemented by a MV AC-DC converter, isolated DC-DC converter and a LV inverter. This topology has normally two constant DC-links, in which at least one is available for connectivity. The decoupling between MV and LV sides provides more degree of freedom for the system control, allowing the implementation of the needed functionalities. Hence,



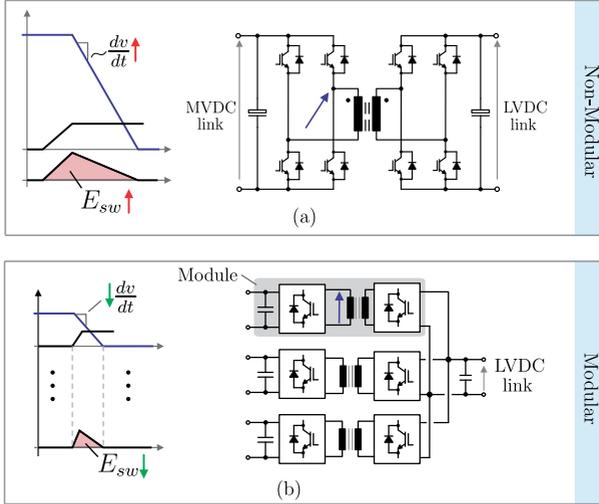
**Fig. 1.9:** Classification of the ST architectures according to the number of power conversions, modularity and modularity level.

this is the preferred architecture for ST implementation.

### 1.3.2 Modularity

The next classification for the ST architecture concerns to the degree of modularity. It can be classified as: modular, non-modular or semi-modular. The non-modular system is based on a single power converter, as exemplified in Fig. 1.10 (a), and usually takes advantage of high voltage wide-bandgap semiconductors [16, 17, 22]. Special devices with high blocking voltage capability, such as 10 kV Silicon Carbide (SiC) MOSFETs or 15 kV SiC IGBTs [34, 36, 37] are needed to handle the MV level in the power converter. Because these devices are not commercially available, but only for research purposes, there is no available products currently using this technology. A standard approach to handle the MV in a non-modular solution and well adopted by the industries is to employ semiconductors connected in series; however, this demands an additional control effort to balance the voltage over the semiconductors.

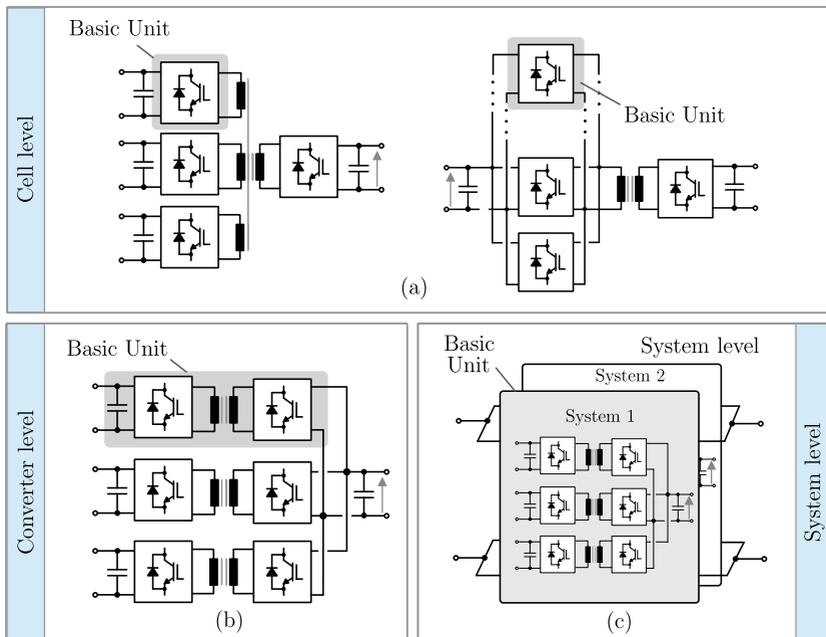
Conversely, the modular approach consists of several basic converters rated for low voltage or low current, which are used as building blocks for the entire system, as depicted in Fig. 1.10 (b). In this solution, the basic building blocks share the voltage on the MV side and the current on the LV side among them, enabling the use of LV rated de-



**Fig. 1.10:** Possible implementation approaches of the ST architecture to handle the MV level involved in the power conversion: (a) non-modular and (b) modular.

vinces. In spite of using more components compared to the non-modular solution, the modular approach is more cost-effective, as demonstrated in [47]. Still, modular architectures bring several advantages to the power and voltage scalability, maintenance, and the implementation of fault-tolerance strategies. In comparison to the non-modular, the modular architectures have reduced electromagnetic interference (EMI) emissions (due to the low  $dv/dt$  and  $di/dt$ , as illustrated in Fig. 1.10 (a) and (b)) and the possibility to use standard LV rating devices that perform well, benefiting both efficiency and cost.

Some features from the modular and non-modular concepts can be combined to form the semi-modular concept, as an alternative for both previous approach. In this case, the architecture is implemented using basic modules sharing the power, similar to the modular approach, but a non-replaceable components processing the total system power is part of the architecture. It can also be called as partially modular approach and an example is presented in Fig. 1.5 (c), where the modules on the primary side divide the power among them, while the HFT and the secondary side bridge processes all the power.



**Fig. 1.11:** Modularization level: (a) cell level, (b) converter level and (c) system level.

### 1.3.3 Modularity Level

The modular approach can be implemented in different level, as shown in Fig. 1.11, and they are classified as: cell level, converter level and system level. The most basic one is the cell level, where the basic unit is the cell used inside the converter, as exemplified in Fig. 1.11 (a). Another example of a cell level modular system is the MMC, that is a single converter using several cells as basic units. The next level is the converter level. In this case, the power converter is the basic unit and they are combined in series and/or parallel to implement the entire system, as shown in Fig. 1.11 (b). This is the most employed modularization level and the input-series output-parallel (ISOP) connection is very popular. Interleaved converter is another example of the converter level modular system, in which several converters are connected in parallel. Finally, the system level is presented in Fig. 1.11 (c). In

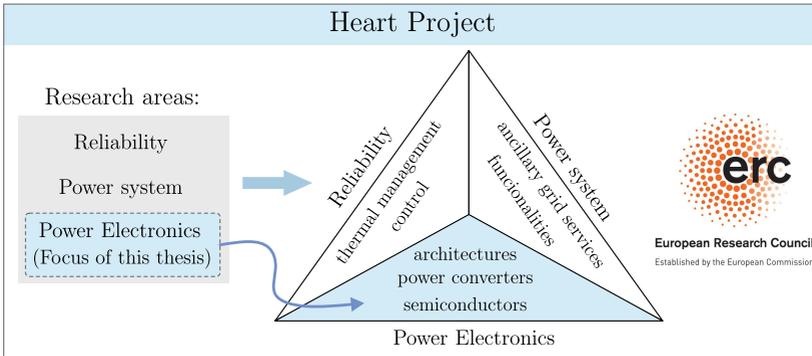
this case, the full system is used as the basic unit. It is very used in application where fault-tolerance or scalability is highly desired. All these levels can be freely combined, resulting in a modular system with multiple levels. In modular ST architectures, the converter level is the most common one, although the cell level can also be used.

## 1.4 ST Architecture Selection for Electric Distribution System

As outlined above, the ST is a fortunate technology and it can offer several benefits to the electric distribution grid. Nevertheless, the amount of power electronics involved in this system and the severe requirements of efficiency, reliability and cost make its design and implementation very arduous.

### 1.4.1 Heart Project: Highly efficient and reliable Smart Transformer

To select the proper ST architecture, certain constraints and requirements must be considered and multidisciplinary research areas are involved, such as: control system, power converter design, electric power system, thermal managements and etc. Then, the architecture must be properly chosen and carefully designed, from the components level until system level. In this context, this thesis deals with the investigation on the power converters and architectures of smart transformers for electric grid application as part of the *Heart Project - Highly efficient and reliable Smart Transformer*, supported by the European Research Council. In the framework of this project, a ST architecture is proposed as an enabling technology for the smart grid implementation and three research areas are highlighted: reliability, power systems and power electronics converters, as presented in Fig. 1.12. The core of the project is to increase the system lifetime by mean of the temperature control, where the operation temperature of the power components has a crucial contribution in this regard. Consequently, thermal management and control are fundamental subjects approached in this project, in order to increase the ST reliability. As an outcome of this research project, the Power Routing (PR) approach has been proposed as a technique to improve the system reliability, by controlling the power



**Fig. 1.12:** multidisciplinary research areas involved in the ST conceptualization and design for the Heart project.

flow according to the component temperature [48]. This technique is explained in detail later. Power system aspects are also investigated in this project, where questions like possible grid services, functionalities, installation, protection and etc are approached. Finally, power electronics aspects needed for the implementation of the system and hardware issues are also studied. In this research topic, the conceptualization of the ST architecture, the power converters used to implement the hardware system and the design are approached. This thesis deals with the last described research topic, where the challenge of making this technology feasible in terms of efficiency, reliability, cost and current/voltage control to provide ancillary services to the grid is the main focus.

As mentioned before, SST and ST concepts differ from each other by their application and consequently their requirements. As this thesis investigates an architecture for electric distribution grid, i.e. a smart transformer, only the term ST will be use in the rest of this work.

### 1.4.2 Architecture concept selection

From the previous overview and the discussion about the ST architecture classification, the basic concept of the ST architecture might be conceived based on the needs. According to the ST classification shown in Fig. 1.9, the first choice concerns the number of power stages. In this case, the three-state architecture is selected, because it guarantees

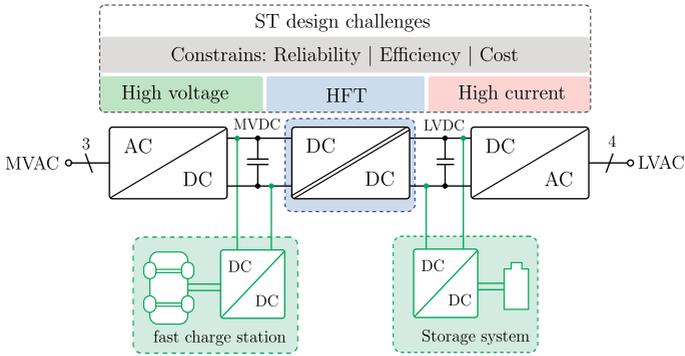
the decoupling between input/output voltages and current, providing more degrees of freedom for the control and for the implementation of functionalities and ancillary grid services. Furthermore, it is possible to provide DC-link connectivity, enabling DC and AC grids integration, as explained before.

The next selection refers to the modularity. Although the non-modular approach might provide advantages in terms of control and communication system, requiring less data exchange, the modular offers more benefits in terms of hardware. The feasibility of using low blocking voltage devices offered by this last approach enables a wide range of semiconductors choice. It provides more degree of freedom during the design and optimization, since more choices are possible. As already cited, modular architectures is also more advantageous in terms of power and voltage scalability, maintenance, and implementation of fault-tolerance strategies, contributing significantly to improve the system's reliability. Later in Chapter 5, a comparative analysis of the modular and non-modular architectures is carried out, demonstrating the economical advantage of the modular approach over the non-modular one. It plays an important role on the decision of using the modular approach. Finally, the modular concept allows the implementation of a technique named Power Routing [48] explained later. For all these reasons, the modular approach is chosen for the ST implementation in this work. Then, Fig. 1.13 shows the simplified block diagram of the ST investigated in this work, as well as the constrains considered for the design. In this figure, both DC links are available for connectivity, but this availability depends on the power converter choice. The power converters used in each is discussed in Chapter 2, where the complete ST architecture investigated in this work is explained in detail.

### 1.4.3 Power Routing Approach for Modular System

The efficiency and reliability are the biggest concerns not only in ST, but also in power electronics converters in general. Many design optimization methods, mainly focusing in efficiency, have been discussed in the literature. These methods normally consider the semiconductor's type, modulation and reactive elements as the main input parameters to maximize the converters efficiency [49–51].

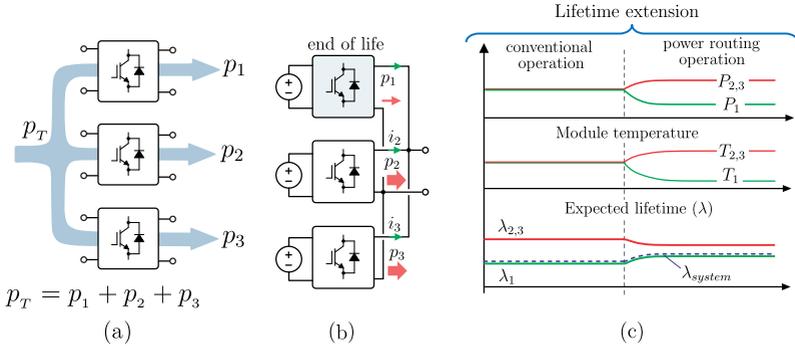
On the other hand, in the system level view, one more aspect can be used to optimize the overall efficiency of the entire system, when the



**Fig. 1.13:** Block diagram of the chosen ST architecture, highlighting the main design constrains: reliability, efficiency and cost.

modular approach is used: the operation point of the individual module with respect to system behavior. Normally, modular system shares equally the power among the modules. However, unequal power sharing can be beneficial for the overall system performance. For instance the phase-shedding can be used to improve the efficiency in light load operation of a modular system, through the technique of activation and deactivation of the modules [52]. This approach is well established in modular parallel converters, usually called multiphase converters [52]. Besides the efficiency, the power routing technique can also be used to postpone the failure (or schedule maintenance), increasing the mean time between failure. The most contributing stress factor to failure rates of the components (IGBTs, MOSFETs and capacitors) are related to the temperature [48], consequently power. Then, using this approach, the temperature is controlled by the means of the power processed by the modules individually, to postpone the failure.

As an example, a system based on three modules is presented in Fig 1.14, where the power processed by the modules 1, 2 and 3 are  $p_1$ ,  $p_2$  and  $p_3$ , respectively. Similarly, the operation temperature (e.g. semiconductor) are  $T_1$ ,  $T_2$  and  $T_3$  for modules 1, 2 and 3, respectively, while the remaining lifetime of each modules is defined by  $\lambda_1$ ,  $\lambda_2$  and  $\lambda_3$ , respectively. The total power is given by  $p_T = p_1 + p_2 + p_3$ . In the conventional operation, the modules process the same amount of power, i.e.  $p_1 = p_2 = p_3$ , in which can be observed in the first moment in the Fig. 1.14. On the other hand, this equality is not true in the power



**Fig. 1.14:** (a) Power routing concept and an application example [in (b) and (c)] to extend the lifetime of a modular system [48].

routing approach [48]. In this example, it is assumed that the remaining lifetime for module 1 is lower than that of the other cells, consequently the entire system will fail when module 1 reaches the end of its life. To postpone the failure by the means of the power routing approach, the power level of module 1 is reduced (resulting in  $p_1 \neq p_2 = p_3$ ), reducing its temperature and increasing the lifetime. It results not only on the improvement of the lifetime of module 1, but also on the entire system, as noticed in Fig. 1.14 (c), once the system is supposed to fail according to the first faulty module (in this case: module 1). Of course, the power processed by modules 2 and 3 increases, as well as their temperatures. Although the expected lifetimes of module 2 and 3 are slightly reduced, the overall system lifetime is improved. Then, the power routing is conceptualized as an optimization technique in which each module processes a specified amount of power with the aim of improving the system's efficiency and reliability [48]. It can be seen as a powerful tool to improve the performance of modular systems. Conversely to the phase-shedding, in the power routing approach, the modules share the power unequally among the cell, while all of them are still activated.

To make it feasible and useful to the system, optimization method must be used to identify the optimum operation point of each module in terms of efficiency and lifetime. Additionally, prognostic method must be used to estimate the operation temperatures of the modules, as well as the remaining lifetime or aging.

This work focus on the ST architecture conceptualization and realization to attend all the requirements for its application and this thesis does not aim to investigate the power routing approach. However, an extra requirement is the feasibility to implement the power routing approach on the selected ST architecture. Consequently, it must be take into account during the selection of the ST architecture. To do so, the architecture must be modular and the power converter should be able to control the power individually. This is one more reason to support the choice of the modular ST architecture.

## 1.5 Goal and Contributions of the Thesis

This thesis aims to investigated the power converters and architecture of smart transformer for electric distribution grid application, with the goal to contribute in this field and make this technology feasible and competitive. The suitable ST architecture is conceived considering as the main constrains: efficiency, reliability, cost, high controlability to implement the grid services and power routing implementation. Still, the power converters used to implement the ST system are chosen and designed in this work. The ST architecture is composed by three power conversion stages and the most challenging one is the DC-DC converter. Thus, this thesis focuses on the DC-DC stage, even though architectures, suitable converters and design methodology for converter level and system level are also addressed. More details of the main contributions of this thesis are presented as follow:

- ▶ **ST Architecture:** literature review of the suitable topologies for smart transformer implementation, and selection of the most suitable concept that can attend all the requirements of the system application. As an additional contribution, the advantages of the modular approach over the non-modular one in terms of cost and losses are demonstrated and the optimum number of modules according to the grid voltage is also derived.
- ▶ **Power Converter Selection:** Power converters suitable to be used in each stage are presented and the most promised are compared. The converter for each stage is discussed, but this thesis focuses on the investigation and contribution to the DC-DC converter topology. Thus, an overview of the most suitable topologies

is presented in detail, where they are compared in terms of efficiency. From the overview, two topologies are highlighted: series resonant converter (SRC) and the multiple active bridge (MAB). They are designed and compared experimentally.

- ▶ **DC-DC Stage Design - Series Resonant Converter:** The selected SRC is designed using an optimization algorithm, in order to improve the efficiency and reliability. As a scientific contribution to the SRC converter design, the lifetime of the capacitor is considered and an optimum parameters selection methodology is proposed considering the trade-off between reliability and efficiency. Additionally, a modified topology of the SRC with fault tolerant capability with minimal additional hardware is proposed and experimentally verified.
- ▶ **DC-DC Stage Design - Multiple Active Bridge:** The optimized design of the MAB converter is carried out considering the trade-off between cost and efficiency. Additionally, the benefits to use SiC-MOSFETs in this application is demonstrated analytically and experimentally. A modulation technique based on the *triangular current modulation* is also proposed as a contribution in this work, as presented in detail in Chapter 4.
- ▶ **ST Architecture Demonstration** Finally, a design procedure of the modular ST architecture is presented and its potential is experimentally evaluated. From the obtained results, a discussion is carried out, where the potential of this technology is evaluated.

This work is developed in the scope of the HEART project, then the results and scientific contributions exposed herein were achieved as consequence of the project assignments and either of direct contributions from the author. In order to clarify the main scientific contribution of the author, Fig. 1.15 shows the structure of this thesis, emphasizing the thesis and project contribution, as well as the main scientific publication related to each topic.

## 1.6 Outline of the Thesis

In order to provide a fundamental understanding of the architecture, power converters and semiconductors selection for the ST implementa-

Heart Project	Thesis contribution
<b>Chapter 2: Smart Transformer: Architecture and Power Converters</b>	
<ul style="list-style-type: none"> <li>• Overview of architectures and power convertes [J1]</li> <li>• Investigation of the power routing approach [J2]</li> </ul>	<ul style="list-style-type: none"> <li>• Critical review of dc-dc converters</li> </ul>
ST Architecture definition	
<b>Chapter 3: Series-Resonant DC-DC Converter</b>	
<ul style="list-style-type: none"> <li>• Design of the SRC as a basic module for the ST</li> </ul>	<ul style="list-style-type: none"> <li>• Optimization of the SRC considering lifetime [J3]</li> <li>• Fault tolerance technique proposal for the SRC [J4]</li> <li>• Generation of a family of FT-SRC [J5]</li> </ul>
<b>Chapter 4: Active Bridge DC-DC Converter</b>	
<ul style="list-style-type: none"> <li>• Design of the QAB as a basic module for the ST</li> </ul>	<ul style="list-style-type: none"> <li>• Optimization of the QAB (cost vs. efficiency) [J6]</li> <li>• Proposal of the TCM for QAB [J7]</li> </ul>
<b>Chapter 5: Smart Transformer Architecture Design</b>	
<ul style="list-style-type: none"> <li>• Design of the CHB for the ST</li> </ul>	<ul style="list-style-type: none"> <li>• Analysis of the optimum number of modules (cost and efficiency)</li> <li>• Comparison of different ST architectures [J8]</li> </ul>
<b>Chapter 6: HEART Demonstrator</b>	
Construction, test and validation of the a ST architecture	

**Fig. 1.15:** Structure of the thesis, emphasizing the thesis and project contributions.

tion, while highlighting the goals and contributions of this work, the content of this thesis is divided in the following.

**Chapter 2** presents an overview of the most suitable topologies of the power converter that can be used to implement each of the three stages of the ST architecture. For the first stage (MV AC-DC stage), the MMC and the CHB are mentioned as the most appropriate converters. Thus they are briefly discussed and compared. Similarly, an overview of the most suitable DC-DC converters is presented and the most suitable topologies for the DC-DC stage is presented. From this investigation, the multiple active bridge (MAB) and the series resonant converter (SRC) are highlighted as the best choice. The suitable

topologies to implement the last stage (LV DC-AC) is also discussed, although it is not the main focus of this work. Finally, two possible architectures are highlighted for further investigation: the first based on the CHB associated to the MAB, whereas the second is based on the CHB associated to the SRC. As the difference lies on the DC-DC stage, the thesis focuses on the analysis of these DC-DC converters.

**Chapter 3** analyzes the SRC converter in detail, where the converter's operation is presented and the performance is evaluated. In this chapter, a fault tolerant SRC topology is proposed and analyzed in detail. The proposed approach is also extended to several topologies of SRC and finally a family of fault tolerant SRC converters are generated and discussed. It is one of the main contributions of this work. The SRC is also designed in detail with the aim to improve the reliability and efficiency of the converter. A design procedure is presented in order to minimize the stresses in the most susceptible components to failure, improving the reliability. Finally, a prototype is designed and experimental results are provided in this chapter.

In **Chapter 4**, the analysis of the MAB converter is presented in detail. The MAB can have several operation modes, according to the power flow and voltage level of each bridge, making its general analysis very extensive. On the other hand, in ST application, the MAB has restricted operation modes with regard to the voltage level, power flow, etc. Then, its analysis is simplified, becoming very similar to the Dual Active Bridge (DAB) converter's analysis. For this reason, the DAB converter is firstly analyzed and the possible modulation strategies is presented. Afterward, the MAB converter is analyzed using the phase-shift modulation (PSM). As an additional contribution, the triangular current modulation (TCM), previously presented for the DAB converter, is extended to the MAB in this work. The analysis of the converter using the TCM is presented in detail and the performance of the converter using TCM and PSM are compared. Finally, multi-objective optimization is applied to the MAB converter, in order to optimize its efficiency and cost. The design is discussed in detail and a prototype built from the design outcomes is shown. Experimental results obtained from the built prototype is presented, in order to validate the high performance of the MAB converter.

Differently from the previous chapter, where the design from the component level up to converter level are carried out, in **Chapter 5** the ST architecture design, from the system level viewpoint, is discussed.

The CHB analysis and design is presented, as well as the optimum number of modules is derived in function of the grid voltage. Furthermore, different ST configuration based on MAB converter are analyzed and compared in terms of cost and performance. Hence, the MAB configuration that provides the best efficiency and cost for the ST architecture is chosen for the implementation of the ST. Finally, ST architecture that provides the best cost-benefits is presented.

A ST architecture prototype is designed in **Chapter 6**, where construction detail are presented. The prototype aims to demonstrate the operation and high performance of the ST architecture presented in Chapter 5, in real scale application. For this reason, the demonstrator is based on a three-phase system, with nominal power of 100 kVA, grid AC voltage of 1.5 kV rms and 800 V for the LVDC link. Experimental results are finally presented to validate its operation.

The conclusion and an outlook on subjects of future research are finally presented in **Chapter 7**.

## Chapter 2

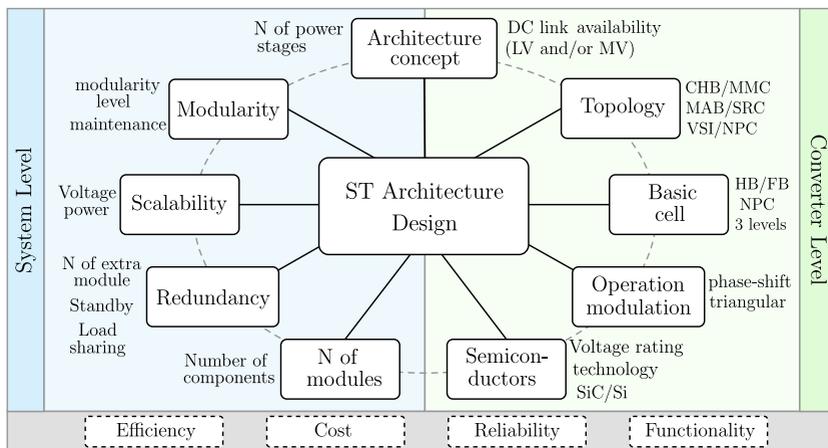
# Smart Transformer: Architectures and Power Converters

**I**N electric distribution system, the ST connects the MV grid to the LV grid providing galvanic isolation in medium or high frequency among them. A typical grid voltage specification and the power level required for the ST is presented in Table 2.1 for different countries. The voltages and power levels involved make the ST architectures design very challenging. Moreover, a numerous options of power converters and parameters that must be chosen make the optimum design an ambitious goal. The typical design procedure of the ST consists in designing the power converter according to the grid specification, restricting its application for a particular country. A ST designed for operating in China can not be installed in the USA, for instance. Consequently, different application places implies in different designs, making this task even more difficult. An alternative to avoid multiple designs is to use the modular approach, in which power and voltage scalability can be employed. It means that the module is supposed to be designed only once and then combined according to the grid specification to realized the whole ST structure. This is one more advantage of the modular approach.

Fig. 2.1 presents an overview of the main ST design parameters. Some of them are directly correlated, such as the number of modules

**Tab. 2.1:** Electric distribution grid specification of different countries

Country	MV grid (kV)	Config	LV grid (V)	Rated power (MVA)	Grid freq (Hz)
Germany	10	3 wires	400	1	50
USA	12.47	4 wires	120	8.6	60
China	10	3 wires	380	2	50
Japan	6.6	3 wires	400	1	60/50
Brazil	13.8	3 wires	380	3	60

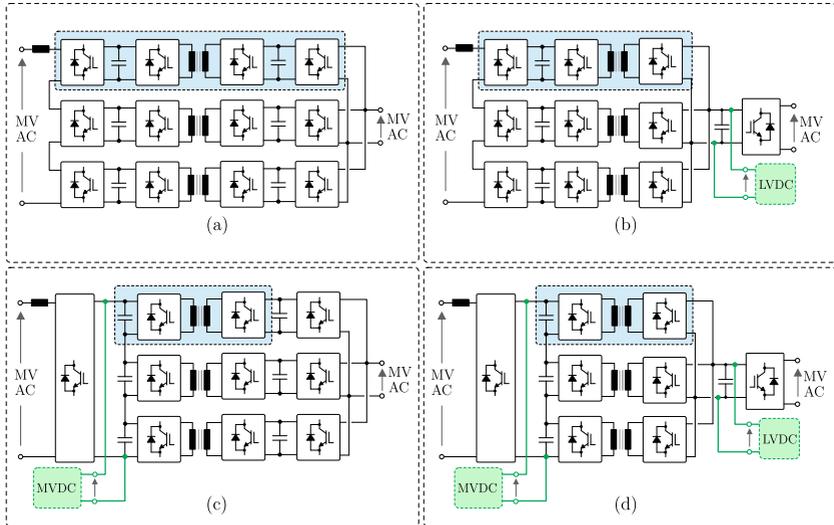

**Fig. 2.1:** Overview of the main ST design parameters from the converter level and system level, as well as the main design requirements.

with the semiconductors voltage rating, the topology choice with the operation/modulation of the converter, etc. Therefore, the trade-off between them must be considered during the design of the ST. In this sense, this chapter presents an overview of the most suitable topologies that can be used to implement each of the three stages of the ST architecture. The architecture concept and power converter are the first choice for designing the complete ST architecture and they are discussed as follow.

## 2.1 ST Architecture concept

The conceptualization of the ST is an important task during its conceive, because it affects and constraints the further design phases. Besides the number of stages and the modularity level, other decisions must be taken, for example the availability of the DC link. In this regard, the modular three-stage architecture has enough degree of freedom to provide one, two or even no connectivity to their DC links. It depends on the configuration of the power converters, as depicted in Fig. 2.2 for a simplified single-phase structure. The availability of one DC link on the LV side (i.e. LVDC link) is the state of the art and the most adopted option, enabling the DC microgrid connection [16, 19, 22].

The configurations without the LVDC link connectivity, as seen in Fig. 2.2 (a) and (c), have distributed DC links on the LV side, instead to have them connected. This strategy does not bring any advantage and for this reason it has not being adopted [19]. The distributed DC



**Fig. 2.2:** Different ST architecture configuration regarding the DC link connectivity for a simplified single-phase structure: (a) without DC link availability, (b) availability of the LVDC link, (c) availability of the MVDC link, (d) availability of both LVDC and MVDC links.

links on the MV side, on the other hand, provides advantages to the DC-DC stage, because the medium voltage can be distributed among the modules. For this reason, this concept has been intensively used [16,19,29,33,47,49,53] and the most adopted structure is that presented in Fig. 2.2 (b).

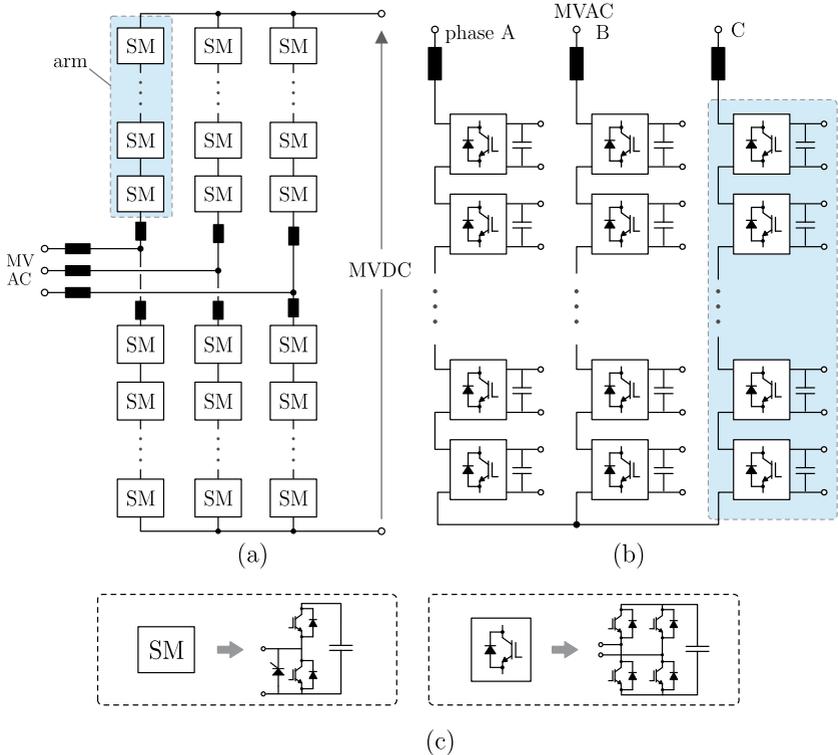
Recently, the availability of the MVDC link has been discussed by the research community, but there is no closed form solution in this regard. The few amount of DC loads applicable for MV level compared to the LV one (which is already well established) makes the MVDC availability still controversial. Nevertheless, new DC load in MV level are emerging, (e.g. fast charger station for EV), supporting research on the architectures with MVDC link. Consequently, the architecture with MVDC link shown in Fig. 2.2 (d) is not well adopted yet, but it is a high potential structure and deserves attention.

Then, two configurations with respect to the DC link connectivity are considered during the power converter topologies choice: the available LVDC link (cf. Fig. 2.2 (e)) and the available LVDC and MVDC links (cf. Fig. 2.2 (d)).

## 2.2 Power Converter Topology: MV AC-DC Stage

The MV side AC-DC converter of the ST should control the active and reactive power absorbed from the grid, as well as regulate the voltage for the next stage, i.e. the DC-DC stage [16,19]. It supports the MV grid providing reactive power when needed. To handle the MV level, multilevel topologies are the most obvious and beneficial choice for implementing the MV stage [56–60]. As the modular approach is adopted, the alternatives are restricted to two power converters: the modular multilevel converter (MMC) [54] and the Cascaded H-Bridge (CHB) [55]. The MMC and CHB topologies are presented in Fig. 2.3 (a) and (b), respectively, as well as the topology of the basic module of each converter. They belong to the same family of converters of Modular Multilevel Cascaded Converter (MMCC), sharing common features, like: reduced filter size, reduced blocking voltage over the semiconductors, modularity, as well as scalability in voltage and power, enabling their application in many places with different grid specifications without major changes in the design of the basic module. In fact, the simi-

larity of these topologies leads to many confusion in the terminology, as described in [61], in which motivated Akagi to propose a classification, as presented in [61]. According to Akagi [61], the topology illustrated in Fig. 2.3 (a) is classified as a double-star chopper-cell (DSCC), because the upper arms are connected in star, as well as the lower arms, consisting in two stars connection. Likewise, the topology illustrated in Fig. 2.3 (b) is named as single-star bridge-cell (SSBC), because its unique start connection of the phases. Although it is a very interesting terminology, they are referred in this work as MMC and CHB for



**Fig. 2.3:** Power converters topologies suitable for the MV stage implementation: (a) Modular Multilevel Converter [54] or Double-Star Chopper-Cell, (b) Cascaded H-Bridge [55] or Single-Star Bridge-Cell and (c) the topology of the basic module used in both converters.

the topologies shown in Fig. 2.3 (a) and (b), respectively, because the well acceptance of this nomenclature. Both converters are described, analyzed briefly and compared in order to choose the most suitable one.

### 2.2.1 Modular Multilevel Converter (MMC)

The MMC converter was introduced by Glinka and Marquart in 2003 [54] as a solution for HV application. Although very few operational MMC converters exist in industry, it is already well established solution for high voltage DC (HVDC) transmission system. The topology is composed by series connection of cells, creating an arm, and two arms are connected through two inductors ( $L_{arm}$ ) to the AC grid, as depicted in Fig. 2.3 (a). Many different topologies for the basic module are possible, but the half-bridge topology is the most utilized. It provides few count parts, as well as few semiconductors on the current path, reducing the conduction losses, when compared to other possible topologies.

An advantage that deserves attention is the availability of the MVDC link, which plays an important role in favor of the MMC application in ST. On the other hand, the main disadvantages are the complex control system and the large amount of required capacitance. Besides to control the three-phase input currents and the total MVDC voltage (as every ordinary front-end converter), the MMC needs to control also the individual voltage of the modules, as well as the circulating current, that is the AC current divided in both arms of one phase. It implies in several voltage and current loops, increasing considerably the complexity of the control system design and implementation. Furthermore, each module of the converter requires large amount of energy stored but low energy density, resulting in large capacitance requirement. In spite of being very worthwhile in HV applications, the MMC feasibility for MV levels is still doubtful and more research in this aspect need to be done.

For the converter design, there are few degrees of freedom during the parameters selection and they are presented in Table 2.2.

The relation between the semiconductor voltage rating and the DC link of the module is shown in (2.1) and the  $V_{MVDC}$ , while the  $V_{MVDC}$  is described in (2.2) and (2.3).

$$V_C = k_u V_{semi} \quad (2.1)$$

**Tab. 2.2:** Design parameters of the MMC

Number of modules per arm	$N_{mod}$
Semiconductors voltage rating	$V_{semi}$
DC link voltage of the module	$V_C$
Semiconductor utilization factor	$k_u$
Total voltage of the MVDC link	$V_{MVDC}$
line to line voltage of the MV grid	$V_{MVAC}$
Modulation index	$m$

$$V_{MVDC} = N_{mod}V_C \quad (2.2)$$

$$V_{MVDC(MMC)} = \frac{\sqrt{2}V_{MVAC}}{m} \quad (2.3)$$

The number of modules can be calculated by

$$N_{mod(MMC)} = \frac{\sqrt{2}V_{MVAC}}{m \cdot k_u \cdot V_{semi}}. \quad (2.4)$$

The capacitance of the modules of the converter can be calculated according to the energy fluctuation of the arm, which is related to the grid frequency ( $f$ ) [62,63]. Then, the required capacitance of the module can be calculated by (2.5), where  $S$  is the apparent power,  $\Delta V_C$  is the capacitor voltage ripple,  $\cos(\phi)$  is the input power factor and  $\omega = 2\pi f$ . More detail about the design of the MMC is presented in [62,63].

$$C_{(MMC)} = \frac{S}{3\omega N_{mod}V_C\Delta V_C} \left( 1 - \left( \frac{m\cos(\phi)}{2} \right)^2 \right)^{2/3} \quad (2.5)$$

### 2.2.2 Cascaded H-Bridge (CHB)

The CHB converter [55] is conceived by several modules connected in series, creating one phase, and the three phases are connected in star, as depicted in Fig. 2.3 (b). It is a well established topology and widely

used in industry in MV applications, [56–60]. The H-bridge is mostly adopted the basic cell, even though other topologies can be employed. [39, 56–60].

Many different strategies can be used to modulated the converter, but the phase-shift has more advantages [56–60, 64] in terms of losses distribution in the semiconductors and AC filter size reduction. Moreover, the operation and control scheme are very simple when this modulation strategy is used. The main disadvantages of the CHB are the lack of a MVDC link for connection of MV loads/sources and the need of isolated sources connected to each module. This last characteristic, however, is not a disadvantage in modular ST application, because the CHB is connected to the DC-DC stage, which is conceived by several isolated DC-DC converter, as explained later.

Similarly to the MMC, the equations (2.1) and (2.2) are also valid for designing the CHB converter. Although this converter does not present a single MVDC link, a virtual MVDC link voltage is defined as the sum of all the capacitor voltage of the modules of one phase and this parameter is calculated by (2.6). This quantity will be used in the comparison between the CHB and MMC in the next section.

$$V_{MVDC(CHB)} = \sqrt{\frac{2}{3}} \frac{V_{MVAC}}{m} \quad (2.6)$$

The  $N_{mod}$  means the number of modules per phase and it is described in terms of the  $V_{MVAC}$ , as

$$N_{mod} = \sqrt{\frac{2}{3}} \frac{V_{MVAC}}{mk_u V_{block}}. \quad (2.7)$$

To design the DC link capacitor of the module, some criteria must be attended. The most severe one refers to the oscillating instantaneous power given by

$$\begin{aligned} p(t) &= v(t) \cdot i(t) = V_{(pk)} \sin(\omega t) \cdot I_{(pk)} \sin(\omega t) \\ p(t) &= \frac{V_{(pk)} I_{(pk)}}{2} [1 - \cos(2\omega t)] \end{aligned} \quad (2.8)$$

where,  $v(t)$  and  $i(t)$  are the instantaneous grid voltage and current, respectively, while  $V_{(pk)}$  and  $I_{(pk)}$  are the grid voltage peak and grid current peak, correspondingly.

**Tab. 2.3:** Main equations for the design of the CHB and MMC converters

Design	MMC	CHB
Module voltage	$V_C = k_u V_{block}$	
MVDC link	$V_{MVDC} = N_{mod} V_C$	
MVDC link	$V_{MVDC} = \frac{\sqrt{2} V_{MVAC}}{m}$	$V_{MVDC} = \sqrt{\frac{2}{3}} \frac{V_{MVAC}}{m}$
N° of modules	$N_{mod} = \frac{\sqrt{2} V_{MVAC}}{m k_u V_{block}}$	$N_{mod} = \sqrt{\frac{2}{3}} \frac{V_{MVAC}}{m k_u V_{block}}$
Capacitance	$C = \frac{S}{3\omega N_{mod} V_C \Delta V_C} \left( 1 - \left( \frac{m \cos(\phi)}{2} \right)^2 \right)^{2/3}$	$C_{min} = \frac{S}{f_s (V_C \Delta V_C - \Delta V_C^2)}$

Thus, using the amount of energy associated with the instantaneous power oscillation, the capacitance is calculated by (2.9) [65, 66].

$$C_{(CHB)} = \frac{S}{f_s (V_C \Delta V_C - \Delta V_C^2)} \quad (2.9)$$

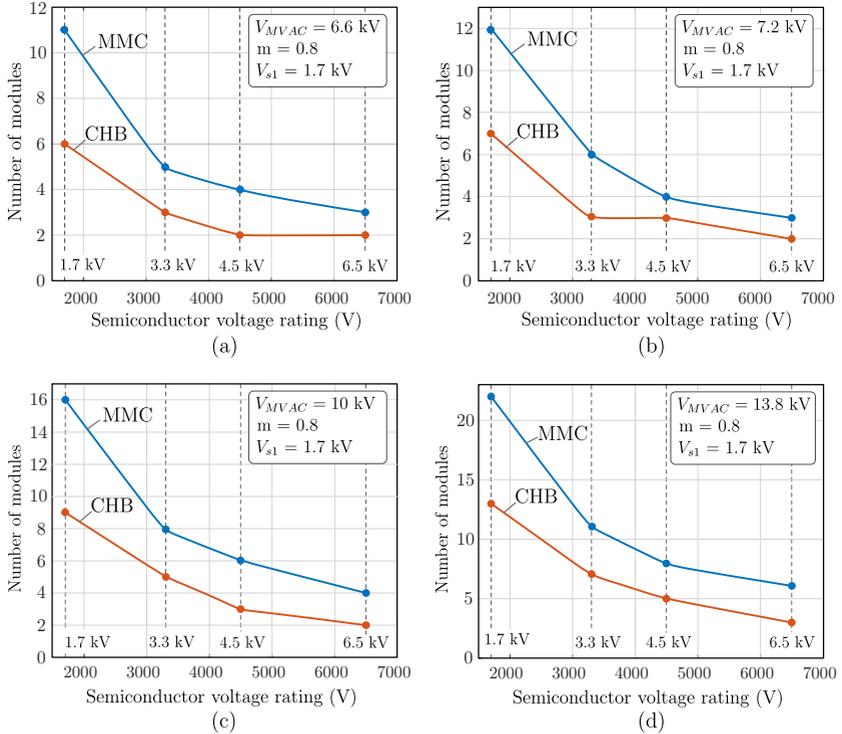
These equations required for the the MMC and CHB design are summarized in Table 2.3.

### 2.2.3 Comparison and Discussion

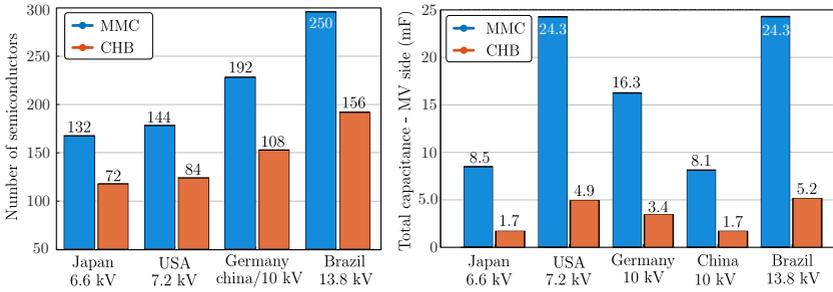
The CHB and MMC have some features in common: modularity, possibility of fault-tolerance implementation, multilevel operation, reduced  $dv/dt$  (EMI) and filter size. The MMC presents the additional advantage of providing the MVDC link for the connection of MV loads/sources, but it is penalized with a very complex control system, bulky filter on the DC side (when compared to the CHB topology), and high cost. For these reasons, it has not been adopted for MV applications yet, but only in HV applications.

To verify which converter is more suitable for the ST implementation, both converters are designed, considering the specification of Table 2.1 and the results are compared in terms of the power devices requirements. For a trustworthy comparison, the same level for the MV grid, as well as the same semiconductor's blocking voltage are assumed for both converters. Different application scenarios for the ST, in terms of grid voltage and power level, are assumed and then the specification presented in Table 2.1 has been used.

The design is realized according to [62, 63, 65, 66], considering a modulation index of  $m = 0.8$  and switching frequency of  $f_s = 5$  kHz. Furthermore, an utilization factor of the semiconductor voltage of  $k_u = 0.65$  is considered, i.e. the maximum voltage over the semiconductor is 65% of its voltage rating. The results are presented in Fig. 2.4 and Fig. 2.5. Fig. 2.4 shows the number of modules required by each topology according to the voltage rating of the chosen semiconductor. The results are plotted for several cases of grid voltage. As can be observed, the CHB converter requires fewer modules compared to the MMC. Consequently, the number of components is also lower. The total number of semiconductors required by each converter is shown in Fig. 2.5 (a), when semiconductors rated for 1.7 kV are used. Regardless the grid voltage, the CHB requires 60% less semiconductors than the MMC.



**Fig. 2.4:** Comparison between the MMC and CHB converters. Required number of modules in function of the selected semiconductor blocking voltage, for different grid voltages: (a) 6.6 kV, (b) 7.2 kV, (c) 10 kV, (d) 13.8 kV.



**Fig. 2.5:** Comparison between the MMC and CHB converters. (a) Number of semiconductors according to the grid voltage application (considering a semiconductor blocking voltage of 1.7 kV), (b) required capacitance according to the grid voltage.

It is important to note that fewer modules does not mean only fewer semiconductor, but also fewer auxiliary components, like gate drive unit, auxiliary power supply and communication/control system. They penalize considerably the cost of the system.

The total required DC link capacitance for both converters are plotted in Fig. 2.5 (b), considering the scenarios shown in Table 2.1. The values presented in this graphic are the total capacitance required per phase. Note that not only the grid voltage changes according to the different scenarios, but also the power level and grid frequency (see Table 2.1). These results show that the total capacitance of the MVDC link can be reduced in approximately 80% when the CHB converter is adopted instead the MMC.

Overall, the CHB presents more advantages than the MMC in terms of: number of modules and semiconductors, required capacitance, as well as control implementation simplicity. For these reasons, the CHB represents the most promising solution and it is selected to implement the MV stage of the ST architecture.

## 2.3 DC-DC Stage

The DC-DC stage is considered the core element of the ST architecture, because it is responsible for connecting the MV side to the LV side, providing galvanic isolation in medium or high frequency among them. In consequence of its strict requirements discussed next, this stage is

the most challenging for the implementation [19,39,48,49,67]. The high voltage and current levels involved in the power conversion make the DC-DC stage responsible for the majority of the system losses; hence it deserves more attention during the design. The requirements and a review of the possible solutions for this stage are discussed next.

### 2.3.1 Requirements

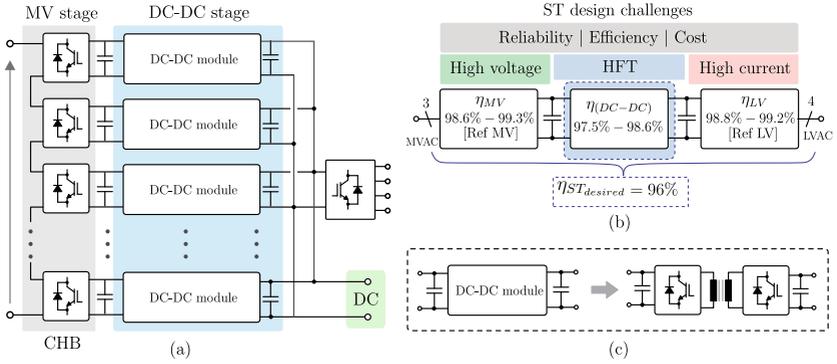
The requirements of the DC-DC stage used in the ST, independently of the adopted approach (modular or non-modular) are summarized as follow.

- ▶ **High voltage capability in the MV side:** Handle voltage level of around 10 kV to 25 kV.
- ▶ **High current in the LV side:** Current level in the range of 100 A to 2000 A is expected, considering the specification shown in Table 2.1.
- ▶ **High voltage isolation:** The medium frequency (MF) or high frequency (HF) transformer employed has an isolation requirement defined by voltage of the MVDC link, i.e. between 10 kV to 15 kV, regardless the solution adopted for this stage.
- ▶ **Decoupling degree between the MV DC side and the LV DC side:** Ability to provide total decoupling between the MVAC grid and the LVAC grid, so that the MV stage and LV stage converters can operate independently from each other. It means that the MV AC-DC stage can operate and provide the required ancillary services to the MV grid (e.g. provide reactive power), without disturb or be disturbed by the LV DC-AC stage operation. The same remark is also valid for the LV DC-AC stage operation. To achieve such decoupling degree, both DC links (MV and LV) must be maintained constant with minimal oscillation voltage (i.e. 5% of the LVDC [19]) and the DC-DC converter should guarantee the voltage regulation.
- ▶ **Control of the power flow:** Ability to control the power flow between the LVDC link and MVDC link and manage the connection of loads of both sides [16,17,22].

- ▶ **Bidirectionality:** many publications agree that the bidirectional power flow capability is required for the DC-DC stage [16–19, 22]. On the other hand, this requirement is questionable, because the reverse power is an exceptional case in distribution system. If economically viable, unidirectional solution could also be accepted. Despite that, bidirectionality is considered as a requirement in this work.
- ▶ **Dc breaker function:** overload and short-circuit protection (working as a DC breaker) of the possible load/source/microgrid connected to the LVDC link [16–19, 22].
- ▶ **High efficiency:** The ST is not only intended to replace the LFT of the distribution system, but also solve problems resulting by the grid modernization [19]. However, high efficiency is expected for the ST, in order to compete with the LFT. The highest efficiencies obtained so far from a SST in traction application is around 95% to 97%, for two processing stages (i.e. AC-DC and DC-DC) [29]. Taking this fact into account, an ambitious efficiency of 96% is defined for the whole ST system, as shown in Fig. 2.6 (b). The MV stage can achieve an efficiency around 98.6% to 99.3% [29, 68], when multilevel converters are used, while the LV stage can offer an efficiency in the range of 98.8% to 99.2% [69–71]. The DC-DC stage should provide an efficiency between 97.5% and 98.6%, so that the entire system achieves the desired efficiency, as shown in Fig. 2. Thus, an efficiency goal over 97.5% can be defined.

### 2.3.2 Basic Module Topologies

From the previous requirements, the high efficiency is the most severe one. The adopted modular approach contributes a lot in favor of performance improvement of the ST, because this approach allows the use of lower voltage rating devices, which perform significantly better than those rated for higher voltage [19]. As described before, this approach consists in several basic modules combined to built the entire architecture, as shown in Fig. 2.6 (a). The basic modules are isolated DC-DC converters, as depicted in Fig. 2.6 (c), and many topology options are available. The topology choice of the basic module plays an important role in the ST design, once the performance of the entire system depends on the efficiency of the individual module. Taking into account



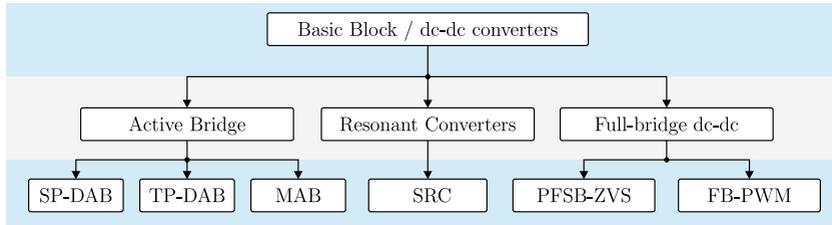
**Fig. 2.6:** (a) Equivalent single phase modular ST architecture adopting the selected CHB, (b) expected efficiency for for the whole system, as well as for each power conversion stage ([Ref MV] = [29, 68], [Ref LV] = [69–71]), (c) implementation of the basic module of the modular DC-DC stage.

the ST specification shown in Table 2.1 and a reasonable number of modules (e.g. 5 to 20), the specification of the DC-DC basic module is in the range shown in Table 2.4. Considering this and the requirements described earlier, an overview of the most suitable topologies for the basic modules is presented as follow.

The most suitable topologies can be classified according to its operation principle, as illustrated in Fig. 2.7, as: active bridge, resonant converter and conventional full bridge DC-DC converter. The converters belonging to the active bridge converter family perform similarly, but each of them has its own peculiarities. Conversely, the converters

**Tab. 2.4:** Specification range of the basic module of the DC-DC stage

Power level	5 to 100 kW
Input voltage	0.6 kV to 1.7 kV
Output Voltage	600 V to 800 V
Isolation Frequency	1 kHz to 40 kHz
Desired efficiency	>97.5%



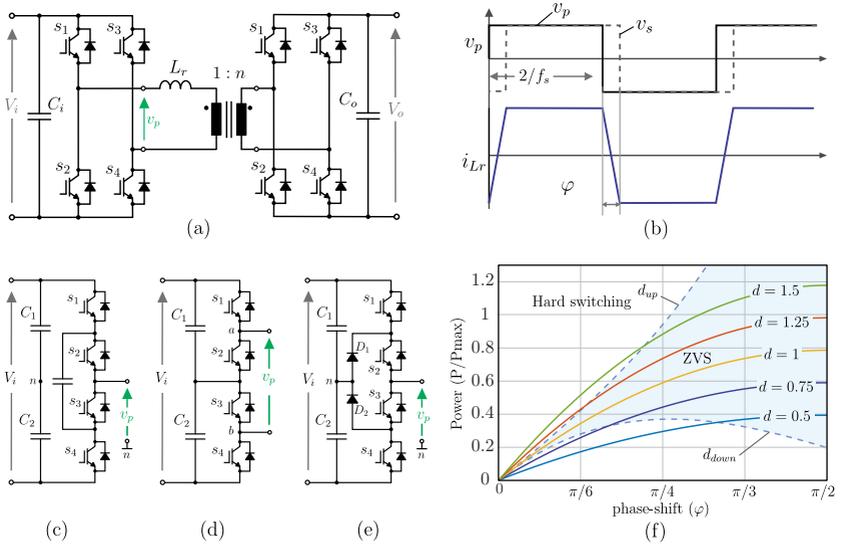
**Fig. 2.7:** Classification of the most suitable DC-DC converters to be used as the basic module of the DC-DC stage. The topologies can be classified in three types: active bridge converters type, resonant converter and full-bridge conventional converters.

belonging to the Full-bridge DC-DC classification operate completely different. All suitable topologies are discussed as follow.

### Dual Active Bridge

The Dual Active Bridge (DAB) converter [72] is composed by two active bridges isolated by a MF/HF transformer, as shown in Fig. 2.8 (a). It has been used in a wide range of voltage (12 V to 5 kV) and power (100 W to 1 MW) [50, 73–78] and it was firstly applied in ST in [33]. To modulate the converter, several strategies have been presented in literature, but the Phase-Shift Modulation (PSM) is the most used one. The main current and voltage waveforms of the DAB using the PSM is shown in Fig. 2.8 (b). The PSM is characterized by zero voltage switching (ZVS) turn-on, but this features depends on the input and output voltages relation and also the load [72]. As the input and output voltage are considered constant in ST application, the converter can be properly designed to work with ZVS for its entire range of operation. Consequently, this scheme offers several advantages for the converter operation. The power is controlled by the phase difference among the bridges and it can be generally described in (2.10), where  $f_s$  is the switching frequency of the converter,  $\varphi$  is the phase shift angle,  $L_r$  is the leakage inductance,  $n$  is the transformer turn ratio and  $v_i$  and  $v_o$  are the input and output voltages, respectively, as shown in Fig. 2.8 (a).

$$P = \frac{V_i V_o}{2\pi f_s L_r n} \varphi \left( 1 - \frac{|\varphi|}{\pi} \right) \quad (2.10)$$



**Fig. 2.8:** Potential converter to be used as the basic cell of the modular ST: (a) DAB topology (b) PSM waveforms. Possible basic cells: (c) flying-capacitor, (d) three-level, (e) NPC. (f) output power of the DAB in function of  $\varphi$ .

$$P = \frac{V_i^2}{2\pi f_s L_r} d\varphi \left(1 - \frac{|\varphi|}{\pi}\right), \quad d = \frac{nv_o}{v_i} \quad (2.11)$$

The inductor current of the DAB is described by (2.12), according to the waveforms presented in Fig. 2.8.

$$i_{L_r}(t) = \begin{cases} \frac{V_i + nV_o}{L_r}t + I(0), & 0 < t < \frac{\varphi}{2\pi f_s} \\ \frac{V_i - nV_o}{L_r} \left(t - \frac{\varphi}{2\pi f_s}\right) + I(0), & \frac{\varphi}{2\pi f_s} < t < \frac{T_s}{2} \end{cases} \quad (2.12)$$

The output power of the converter described by (2.11) is plotted in function of the phase-shift  $\varphi$  in Fig. 2.8, considering different input-output voltage ratio ( $d$ ). In summary, to achieve the ZVS operation, the condition of  $i_{L_r}(0) \leq 0$  and  $i_{L_r}(\varphi) \geq 0$  must be satisfied. Applying these limits in (2.12), the ZVS boundary conditions are obtained

and described in (2.13). Accordingly, the area constrained by (2.13) indicates the soft-switching region of the DAB converter, which is the desired operation region, as highlighted in Fig. 2.8 (f).

$$\begin{cases} d_{ZVS(up)} = 1 - \frac{3\varphi}{2\pi} \\ d_{ZVS(down)} = \frac{1}{1 - \frac{3\varphi}{2\pi}} \end{cases} \quad (2.13)$$

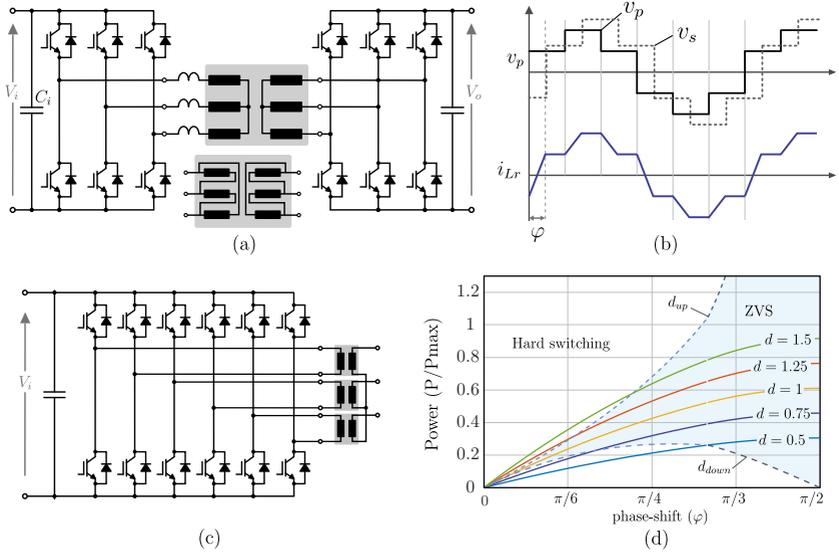
In Fig. 2.8 (f), it is noticed that the DAB converter operates in soft-switching independently from the output power if  $d = 1$ , i.e.  $v_i = nv_o$ . Consequently, the DAB converter can be properly design for operating with soft-switching for the whole load range.

Originally, this converter was proposed using the H-bridge as the active bridge, as shown in Fig. (a). Nevertheless, different topologies (as depicted in Fig. 2.8 (c) to (e)) can be adopted as an active bridge of the DAB, as reported in [73]. Because of its soft-switching operation, high performance is expected, but it depends on the design and the employed semiconductors. In [78], a 4 kW DAB prototype based on 1.2 kV Silicon (Si) IGBT has achieved an efficiency of 97.1%, while an efficiency of 97.5% was reported in [73], for a 6.25 kW prototype based on Silicon-Carbide (SiC) MOSFETs. Similarly, an optimized design of the DAB is presented in [50], where 1.2 kV SiC MOSFETs were employed and an efficiency of 98.2% was obtained.

The most important publications about this converter reporting the obtained efficiency are summarized in Fig. 2.16. As can be noticed, the converter presents an efficiency range around 94.5% to 98.2%.

### 2.3.3 Three-Phase DAB

A three-phase version of the DAB is obtained by adding one more leg to the active bridge (making it a three-phase bridge) and using a three-phase MF/HF transformer, as illustrated in Fig. 2.9 (a) [72]. This converter was firstly described in [72], but intensively investigated in [79–85]. The main advantage of this structure over the classical DAB is the output current ripple reduction, implying in a smaller output capacitor bank. Apart from that, both converters perform similarly, regarding the voltage and current stress on the semiconductors and transformer [72]. The disadvantage is the high number of counterparts



**Fig. 2.9:** (a) Three-Phase DAB converter [72], (b) PSM waveforms, (c) three-phase DAB topology based on six leg on primary side [80], (f) output power in function of  $\varphi$ .

and complex structure of the transformer. In fact, this converter is normally used in high current applications.

The power flow is also controlled by the phase difference between both bridges, as generally described in (2.14) and the ZVS feature is still preserved. The main current and voltages waveforms of the three-phase DAB using the PSM is presented in Fig. 2.9 (b).

$$\left\{ \begin{array}{l} P = \frac{V_i V_o}{2\pi f_s L_r n} \varphi \left( \frac{2}{3} - \frac{\varphi}{2\pi} \right) \quad , \quad \frac{\pi}{3} < \varphi < \frac{2\pi}{3} \\ P = \frac{V_i V_o}{2\pi f_s L_r n} \left( \varphi - \frac{\varphi^2}{\pi} - \frac{|\varphi|}{\pi} \right) \quad , \quad \frac{2\pi}{3} < \varphi < \pi \end{array} \right. \quad (2.14)$$

From the inductor current waveform of the shown in Fig. 2.9 (b) and analyzing the equivalent circuit of the converter for each operation point, the instantaneous inductor current is derived and presented in (2.15).

$$i(t) = \left\{ \begin{array}{ll}
 I(0) + \frac{V_i(1+d)}{3L_r}t, & 0 < t < \frac{\varphi}{2\pi f_s} \\
 I\left(\frac{\varphi}{2\pi f_s}\right) + \frac{V_i(1-d)}{3L_r}\left(t - \frac{\varphi}{2\pi f_s}\right), & \frac{\varphi}{2\pi f_s} < t < \frac{T_s}{6} \\
 I\left(\frac{T_s}{6}\right) + \frac{V_i(2-d)}{3L_r}\left(t - \frac{T_s}{6}\right), & \frac{T_s}{6} < t < \frac{\varphi}{2\pi f_s} + \frac{T_s}{6} \\
 I\left(\frac{\varphi}{2\pi f_s} + \frac{T_s}{6}\right) + \frac{V_i(2-2d)}{3L_r}\left(t - \frac{\varphi}{2\pi f_s} - \frac{T_s}{6}\right), & \frac{\varphi}{2\pi f_s} + \frac{T_s}{6} < t < \frac{T_s}{3} \\
 I\left(\frac{T_s}{3}\right) + \frac{V_i(1-2d)}{3L_r}\left(t - \frac{T_s}{3}\right), & \frac{T_s}{3} < t < \frac{T_s}{3} + \frac{\varphi}{2\pi f_s} \\
 I\left(\frac{\varphi}{2\pi f_s} + \frac{T_s}{3}\right) + \frac{V_i(1-d)}{3L_r}\left(t - \frac{\varphi}{2\pi f_s} - \frac{T_s}{3}\right), & \frac{\varphi}{2\pi f_s} + \frac{T_s}{3} < t < \frac{T_s}{2}
 \end{array} \right. \quad (2.15)$$

Assuming the steady-state condition, the equality  $i(0) = -i(\pi)$  is then satisfied. Solving this equation, the initial condition of the current  $I(0)$  is therefore obtained and described by (2.16).

$$I(0) = \frac{V_i}{3L_r f_s} \left( \frac{d}{3} - d \frac{\varphi}{2\pi} - \frac{1}{3} \right) \quad (2.16)$$

The output power of the converter described by (2.14) is plotted

in function of the phase-shift  $\varphi$  in Fig. 2.9 (d), considering different input-output voltage ratio ( $d$ ). Similarly to the single-phase DAB, the three-phase DAB operates under ZVS if the condition  $i_{Lr}(0) \leq 0$  and  $i_{Lr}(\varphi) \geq 0$  are satisfied. Applying these limits in (2.15), the ZVS boundary conditions are determined by (2.17), for  $0 \leq \varphi \leq \pi/3$ , and (2.18) for  $\pi/3 \leq \varphi \leq \pi/2$ .

$$\begin{cases} d_{ZVS(up)} = 1 - \frac{3\varphi}{2\pi} \\ d_{ZVS(down)} = \frac{1}{1 - \frac{3\varphi}{2\pi}} \end{cases} \quad (2.17)$$

$$\begin{cases} d_{ZVS(up)} = \frac{3}{2} - \frac{3\varphi}{\pi} \\ d_{ZVS(down)} = \frac{1}{\frac{3}{2} - \frac{3\varphi}{\pi}} \end{cases} \quad (2.18)$$

The three-phase DAB operate with ZVS regardless the load if  $d = 1$ . Therefore, if the input and output voltage are constant without significant variation, the converter can be properly designed to operate with soft-switching for the entire range of load, similarly to the single-phase DAB. The design procedure of the converter is reported in [79], where a 8 kW prototype using Si IGBTs was built and an efficiency of 96% was experimentally demonstrated. Different transformers connections have also been investigated [80], but no significant improvement on the efficiency has been experimentally demonstrated. In [85], maximum efficiency of 94.1% and 94.6% were obtained for the Y-Y and Y- $\Delta$  connection of the transformer, respectively. A variant topology using six legs and three single-phase transformers, as presented in Fig. 2.9 (c), is proposed in [80]. In that work, a prototype of 20 kW was developed, reaching an efficiency of 94.7%.

The maximum efficiency reported in literature for this converter was 96%, as can be noticed in Fig. 2.16, assuming the most relevant publications.

### 2.3.4 Multiple Active Bridge

Another variant topology derived from the DAB is obtained by coupling more active bridges to the same high frequency transformer, as depicted in Fig. 2.10 (a). This converter, named as Multiple Active Bridge (MAB), was introduced in [86], where three active bridges were connected to the same transformer. The converter was generalized to multiple bridges connected to a multiwinding transformer in [87] and a version based on four bridges (named as Quadruple Active Bridge (QAB)) was applied in a ST architecture in [88, 89].

This structure has the ability to connect more sources/load with different voltage levels using less converters. When applied to modular ST architecture, the MAB converter offers the advantage of reducing the number of modules and HFT [47], but preserving the same advantages of the DAB converter. The simplified waveforms of the converter is depicted in Fig. 2.10 (b). The power exchange among the bridges can be independently controlled, as illustrated in Fig. 2.10 (c), by the phase difference among the bridges. For instance, considering the circuit shown in Fig. 2.10 (a) where three bridges are used, two equivalent models can be used to analyze the converter: the  $\Delta$ -model (cf. Fig. 2.11 (a)) and the Y-model (cf. Fig. 2.11 (b)).

In the models presented in Fig. 2.11, the voltages and the inductance are reflected to the primary side using the relation shown in (2.19).

$$\begin{cases} V_{1(r)} = V_1 \\ L_{1(eq)} = L_1 \end{cases} \quad \begin{cases} V_{2(r)} = V_2/n_2 \\ L_{2(eq)} = L_2/n_2^2 \end{cases} \quad \begin{cases} V_{3(r)} = V_3/n_3 \\ L_{3(eq)} = L_3/n_3^2 \end{cases} \quad (2.19)$$

The  $\Delta$ -model is more suitable to analyze the power flow among the bridges and it can be directly obtained from the Y-model using the transformation presented in (2.20) and (2.21).

$$L_{12(eq)} = \frac{L_{LK}}{L_{3(eq)}}, \quad L_{13(eq)} = \frac{L_{LK}}{L_{2(eq)}}, \quad L_{23(eq)} = \frac{L_{LK}}{L_{1(eq)}} \quad (2.20)$$

$$L_{LK} = L_{1(eq)}L_{2(eq)} + L_{1(eq)}L_{3(eq)} + L_{2(eq)}L_{3(eq)} \quad (2.21)$$

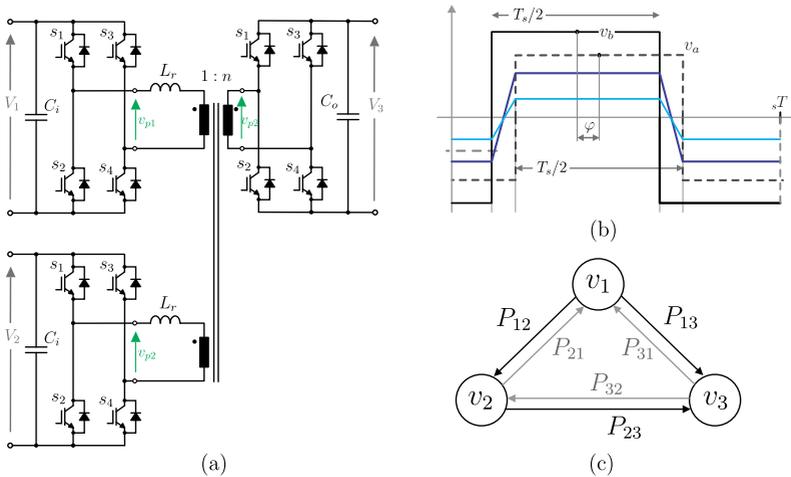
Using the PSM, the power exchanged among two sources, like  $V_1$  and  $V_2$  for instance, is controlled by the phase displacement between

**Tab. 2.5:** Power flow direction of the MAB converter according to the phase-shift angle

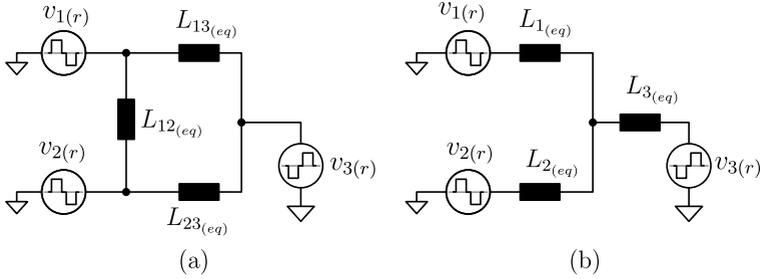
Power flow	Parameters	Control parameter
from $V_1$ to $V_2$	$P_{12}$	$\varphi_1$
from $V_1$ to $V_3$	$P_{13}$	$\varphi_2$
from $V_2$ to $V_3$	$P_{23}$	$\varphi_1 - \varphi_2$

the bridges 1 and 2, defined as  $\varphi_1$ . Consequently, Table 2.5 shows the power flow direction (cf. Fig. 2.10 (c)) according to the phase-shift angle used to control the correspondent power.

The same procedure used to determine the power transference of the DAB converter can be applied to the MAB converter. Therefore, considering the variable shown in Table 2.5, the power transference of the MAB is expressed in (2.22).



**Fig. 2.10:** (a) Topology of the MAB converter [72], (b) PSM waveforms, (c) equivalent circuit highlighting the power flow exchanged among the sources.



**Fig. 2.11:** Equivalent model of the MAB converter based on three bridges: (a)  $\Delta$ -model and (b) Y-model.

$$P_{12} = \frac{V_{1(r)}V_{2(r)}}{2\pi f_s L_{12(eq)}} \varphi_1 \left( 1 - \frac{|\varphi_1|}{\pi} \right)$$

$$P_{13} = \frac{V_{1(r)}V_{3(r)}}{2\pi f_s L_{13(eq)}} \varphi_2 \left( 1 - \frac{|\varphi_2|}{\pi} \right) \quad (2.22)$$

$$P_{23} = \frac{V_{1(r)}V_{3(r)}}{2\pi f_s L_{13(eq)}} (\varphi_2 - \varphi_1) \left( 1 - \frac{|(\varphi_2 - \varphi_1)|}{\pi} \right)$$

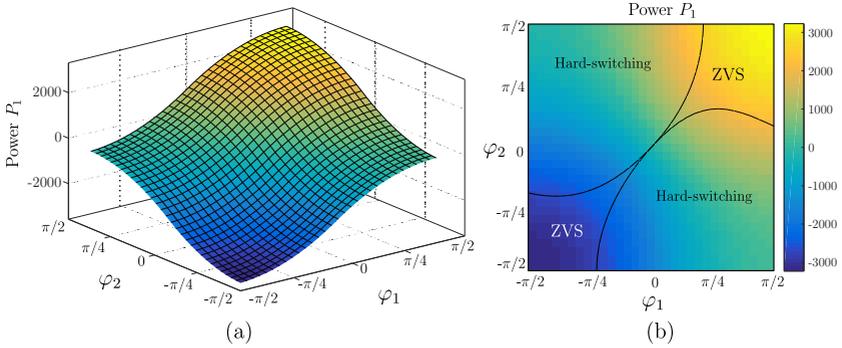
The total power transferred by the voltage source  $V_1$ ,  $V_2$  and  $V_3$  is given by (2.23).

$$P_1 = P_{12} + P_{13}$$

$$P_2 = P_{21} + P_{23} = -P_{12} + P_{23} \quad (2.23)$$

$$P_3 = P_{31} + P_{32} = -P_{23} - P_{13}$$

Note that  $P_1 + P_2 + P_3 = 0$ . As can be observed in (2.23), the power  $P_1$  transferred by the source  $V_1$  depends from the angles  $\varphi_1$  and  $\varphi_2$  and the variation of the power in function of these angles is shown in Fig. 2.12. Similarly to the conventional DAB converter, the MAB can operate with ZVS if some conditions are satisfied. For instance, the bridge 1 related to the source  $V_1$  achieves ZVS if the condition  $i_{L1}(0) \leq 0$  and  $i_{L1}(\varphi_1) \geq 0$  is satisfied, implying in:  $d_{ZVS(up1)} = V_{2(r)}/V_{1(r)} = 1 - 3\varphi_1/(2\pi)$ ,  $d_{ZVS(up2)} = V_{3(r)}/V_{1(r)} = 1 - 3\varphi_2/(2\pi)$ ,  $d_{ZVS(down1)} = 1/d_{ZVS(up1)}$  and  $d_{ZVS(down2)} = 1/d_{ZVS(up2)}$ .



**Fig. 2.12:** Variation of the power  $P_1$  in function of the phase shift-angles  $\varphi_1$  and  $\varphi_2$ .

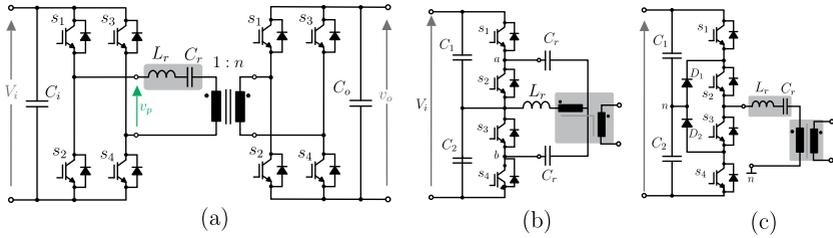
Finally, Fig. 2.12 (b) shows the variation of the power  $P_1$ , emphasizing the region of soft-switching and hard-switching operation, according to the angles.

Although the MAB has been more often discussed in literature recently, most of the publication focuses on the modeling and control strategy of the converter. In fact, very few papers have focused on the design and only [90,91] presented efficiency results obtained experimentally. A maximum efficiency of 92% was reported in [90], while 91.7% was presented in [91]. In both cases, three active bridges were used, as well as standards Si-MOSFETs, to develop the prototype. So far, higher efficiency values have not been reported in literature.

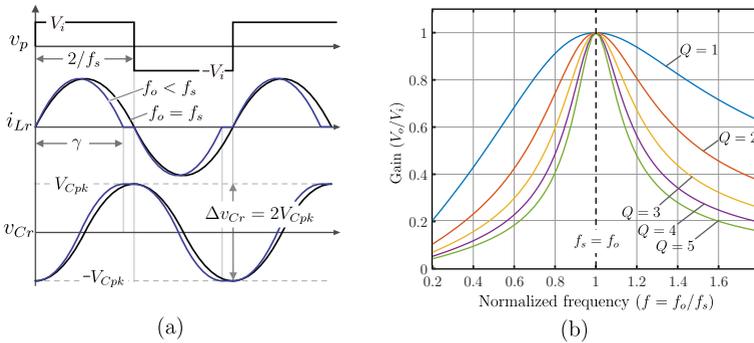
### 2.3.5 Series Resonant Converter

Another candidate to be used as a basic module of the modular ST is the series resonant converter (SRC) and this topology is illustrated in Fig. 2.13 (a). This converter is well-known and it has been very used in a large range of voltage and power application [92–97]. In spite of its similarity to the DAB topology, the SRC operates with sinusoidal current shape on the transformer (as shown in Fig. 2.14 (a)), resulting in a complete different operation.

Analyzing the converter according to [98–100], the input-output voltage relation is obtained and described in (2.24), where  $Q$  is the quality factor,  $\omega_s$  is the angular switching frequency,  $\omega_o$  is the angular resonant



**Fig. 2.13:** (a) Topology of the SRC converter, (b) modified SRC converter using the three level topology in the primary side and (c) using the NPC in the primary side.



**Fig. 2.14:** (a) Main waveforms of the SRC and (b) normalized voltage gain ( $V_o/V_i$ ) of the SRC in function of the normalized operation frequency ( $f_o/f_s$ ), according to the quality factor.

frequency and  $R_o$  is the load resistance. These variables are expressed in (2.25).

$$\frac{V_o}{V_i}(j\omega) = \frac{1}{1 + jQ \left( \frac{\omega_s}{\omega_o} - \frac{\omega_o}{\omega_s} \right)} \quad (2.24)$$

$$\omega_s = 2\pi f_s, \quad \omega_o = \frac{1}{\sqrt{L_r C_r}}, \quad Q = \frac{\omega_o L_r \pi^2}{8R_o} \quad (2.25)$$

Fig. 2.14 (b) shows the normalized voltage gain ( $V_o/V_i$ ) of the SRC in function of the normalized operation frequency ( $f_o/f_s$ ), according to the quality factor. According to this figure, the gain of the SRC varies

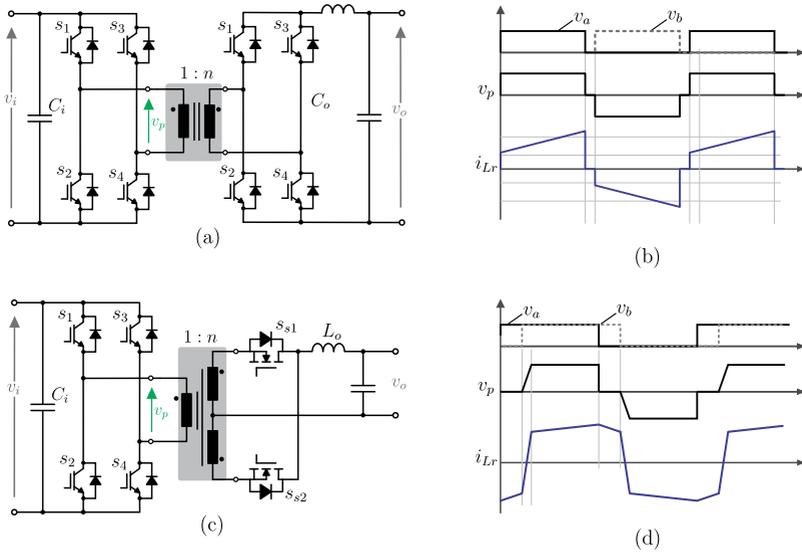
according to the frequency, and usually the switching frequency is used to control the output voltage of the SRC. However, this strategy implies in a complex control system and oversize of the high frequency transformer (HFT), once it must be designed to operate for the minimum frequency.

The most efficient operating point of the SRC is when the converter operates in the discontinuous conduction mode (DCM) with the switching frequency ( $f_s$ ) equal or slightly below the resonance frequency ( $f_o$ ), i.e. with unit gain. In this operation mode, the primary side switches achieve ZVS and the output diodes achieve zero current switching (ZCS) [95]. Moreover, the converter has good transformer utilization and also low EMI emission, due to the smooth current shape (low  $di/dt$ ). In this operation point, the power flow is not directly controlled and the power conversion between input and output is defined by (2.26), where  $n$  is the transformer turn ratio. On the other hand, it is not a disadvantage in ST application, once the system has enough degrees of freedom to control the input voltage by using the front-end rectifier (first stage).

$$V_o = n \cdot V_i \quad (2.26)$$

To optimize the efficiency of the SRC, a computer-aided design approach is proposed in [96], in which a peak efficiency of 97.4% was achieved. In [95], a SRC using Gallium-Nitride (GaN) devices was developed and a maximum efficiency of 98.3% is obtained. Nevertheless, this design was carried out for low power (up to 300 W) and low voltage (up to 400V) applications. A high efficiency SRC is reported in [92] for higher power and voltage level application (5 kW, 600 V). In that paper, SiC MOSFETs are used, presenting a peak efficiency of 97.6%, in which is one of the highest reported in literature, considering the power/voltage level.

Similarly to the DAB, different topologies were used on the SRC, as illustrated in Fig. 2.13 (b) and (c). A modified SRC converter using the bridge presented in Fig. 2.13 (b) was proposed in [97], where a peak efficiency of 98.1% was demonstrated. Similarly, the neutral point clamped (NPC) topology was applied to the SRC (as shown in 2.13 (c)), reaching an efficiency of 97.6%. Therefore, the basic topology used on the SRC does not affect significantly the converters efficiency.



**Fig. 2.15:** (a) Topology of the Full-Bridge PWM converter and (b) main waveform of the FB-PWM converter. (c) Topology of the Phase-Shift Full-Bridge ZVS converter (PSFB-ZVS) and (d) its main waveforms.

### 2.3.6 Full-Bridge Topology

The standard full-bridge converter, Fig. 2.15 (a) and (c), is also a potential topology for the basic module of the ST. This converter is well-known and different operation modes are possible for it. By using the pulse width modulation (PWM) with duty-cycle control ( $D$ ), the converter (named as FB-PWM) behaves as an isolated Buck converter, when transfers power from  $V_i$  to  $V_o$ , or as an isolated Boost converter, in case of reverse power flow, as described in [101]. The main waveforms of the FB-PWM are depicted in Fig. 2.15 (b). In this operation mode, the power conversion between input and output is determined in (2.27) and the converter operates with hard-switching, increasing considerably the losses.

$$\begin{cases} V_o = n \cdot D \cdot V_i & , \text{ Buck mode} \\ V_o = \frac{n}{1-D} \cdot V_i & , \text{ Boost mode} \end{cases} \quad (2.27)$$

In [101], an optimized design of a 1.7 kW FB based on structure shown in Fig. 2.15 (a) and using GaN devices is reported. Due to the characteristic of low switching losses of the employed devices, a very high efficiency of 98.8% was obtained. Furthermore, four MOSFETs were used in parallel, favoring the conduction losses reduction, but penalizing the cost. Still, the converter was designed for low voltage, enabling the use of 600 V rated devices.

Conversely, the converter can operate with phase-shift modulation, where the power transference is controlled by the phase difference between the legs of primary side bridge. Using this modulation, the converter operates with ZVS and it became well-known as phase-shift full bridge ZVS converter (PSFB-ZVS) [102]. Unlike the traditional FB converter, the PSFB-ZVS makes use of the resonant transition during the commutation of the semiconductor to achieve ZVS operation. The transition occurs between the intrinsic capacitor of the semiconductors and the leakage inductance ( $L_r$ ) of the transformer. External capacitors might be used in parallel with the semiconductors to adjust the commutation of the converter. The output voltage of the PSFB-ZVS is determined by (2.28). The disadvantage of this topology is the presence of duty-cycle loss  $\Delta D$ , given by (2.28), which is a load dependent relation. Therefore, the control system needs to compensate the voltage drop in virtue of the duty-cycle loss  $\Delta D$ . Another drawback is the limitation of the soft-switching range.

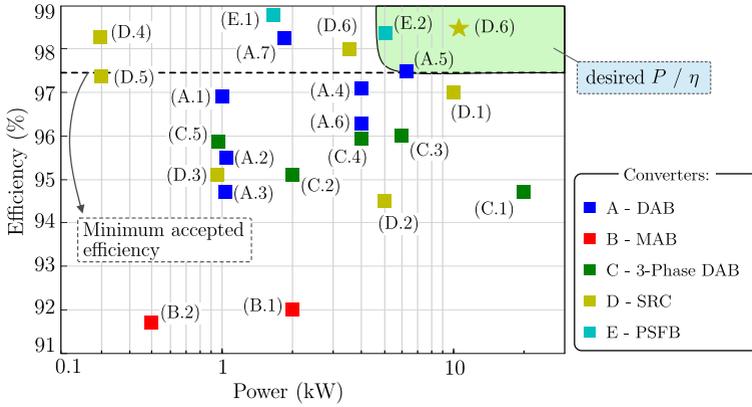
$$V_o = nV_i (D - \Delta D), \quad \Delta D = \frac{4f_s L_r n I_o}{V_i} \quad (2.28)$$

An optimized design of the PSFB-ZVS is presented in [102], where four Si-MOSFETs were used in parallel to reduce the conduction losses. In that work, a maximum efficiency of 98.2% is demonstrated. Therefore, depending on the operation mode of the full-bridge converter, special devices are needed to obtain high efficiency.

As can be seen in Fig. 2.15 (a) and (c), different output rectifiers can be used. A disadvantage of this converter is its input-output asymmetry. It means, that the converter operates differently in case of reverse power flow, regardless the adopted rectifier.

### 2.3.7 Comparison and Discussion

From the literature review, the performance of the converters described previously are compared, in order to recognize the most suitable topol-



**Fig. 2.16:** Efficiency comparison of the possible DC-DC converters candidates to be used as the basic module. (Only the most relevant publication in literature, considering the data obtained experimentally is included in this graphic).

ogy and determine the key parameters for obtaining high efficiency. Thus, the most relevant publications for each topology (only those with experimental values of efficiency) were collected and plotted in the Fig. 2.16. This figure shows the efficiency versus the power level of the converters, where the expected efficiency is highlighted. As can be noticed in this figure, different topologies perform similarly in terms of efficiency. It means that not only the converter choice, but also the topology of the basic cell of the converter, semiconductor technology and design procedure play a key role on the converter's performance. These features are discussed next.

- **Converter Topology:** Only the DAB, SRC and FB converters have presented efficiency over the expected value of 97.5%. On one hand, it suggests that these topologies are the most promises for the basic module. On the other hand, the DAB and SRC topologies presents a wide range of efficiency, It shows that the topology choice plays an important role, but it is not the lone reason that leads to high performance.

Analyzing the FB converter, its high efficiency was demonstrated only for lower power and voltage prototypes [101,102]. To reach such efficiency level, several devices were used in parallel in both

works, reducing the conduction losses, but increasing considerably the cost. This topology has also the disadvantage to be asymmetrical from input-output viewpoint, i.e. it operates differently (with different performance) in case of reserve power flow. Thus, this converter is not a preferable choice for the DC-DC of the ST.

The three phase DAB does not present significant advantages in term of performance, when compared to the conventional DAB. The only advantage is the reduction of the output voltage ripple. Furthermore, this converter has at least four additional semiconductors and a more complex transformer structure, increasing considerably the cost. Thus, it is not considered for the basic module.

From the literature review, the MAB could be directly discharged, because of its poor performance. However, its potential has not been explored so far and indeed there is no publication discussing efficiency. In fact, it operates similarly to the DAB and, then similar efficiency can be expected. In addition to the performance, the cost plays an important role. In [47], the economic advantage of the MAB compared to the DAB was demonstrated, making it a potential converter to be used as a basic module.

- ▶ **Basic Cell:** Although different cells can be used on the DAB converter, their performance do not differ significantly. Actually, the highest efficiency of the DAB was obtained using the classical H-bridge topology [50]. Thus, it is possible to reach high efficiency, regardless the cell used as an active bridge of the DAB. The same observation is valid for the SRC converter, where the highest efficiency was obtained for a modified topology as the basic cell [95].
- ▶ **Semiconductor Technology:** As can be noticed in Fig. 2.16, all the topologies with high efficiency are based on the wideband gap devices, denoting that the semiconductors selection is a key point for improving the converter's performance. The GaN semiconductors are not suitable for ST application, because of its blocking voltage limitation (up to 650 V). On the other hand, SiC semiconductors are commercially available for voltage rating of 1.2 kV and 1.7 kV and this voltage tends to increase even more. Devices

**Tab. 2.6:** Comparative analysis of the basic DC-DC converters

Topology	N° of devices	Switching charact	Symmetry	Output ripple	Control
DAB	8	ZVS	yes	high	active
3P-DAB	12	ZVS	yes	low	active
MAB	12	ZVS	yes	high	active
SRC	8	ZVS/ZCS	yes	medium	open loop
FB-PWM	8	Hard	no	medium	active
FSFB-ZVS	6	ZVS	no	medium	active

with voltage rating of 3.3 kV has already been developed, but they are not yet commercialized [103–105]. SiC semiconductors have a huge potential in ST application, because its suitable voltage and current levels associated to its high performance. As the cost also plays an important role, the standard Si IGBT commercialized with very low price compared to SiC MOSFETs should also be highlighted.

Table 2.6 summarizes the features of each converter discussed before. From the review, the SRC, DAB and MAB can be highlighted as the preferable choices for the basic module of the DC-DC. The DAB and MAB belong to the same family of converters and they perform similarly [47, 86, 87, 90]. The DAB is a particular case of the MAB converter. According to [47], the MAB represents a cost-effective choice compared to the DAB, and then it is selected for further investigation. To verify what is the most suitable solution among the MAB and SRC for the implementation of the DC-DC stage, both topologies must be analyzed in detail. Therefore, the next chapter are dedicated for a deeper investigation of the SRC and the MAB converter.

## 2.4 LV AC-DC Stage

The last stage of the ST is the voltage source inverter (VSI) connected to the LV AC grid and it generates the sinusoidal AC voltage with high quality to the load. The LV stage is the most susceptible one to the LV grid disturbs and its output filter (common mode and differential mode filter) must be carefully designed. The conventional grid voltage level

involved on the power conversion enables the use of mature topologies, which are well established and accepted by academia and industry. Furthermore, standard semiconductor with low blocking voltage (600 V or 1.2 kV, depending on the chosen topology) can be used. It offers a broad choice of devices, benefiting the converter's design and optimization.

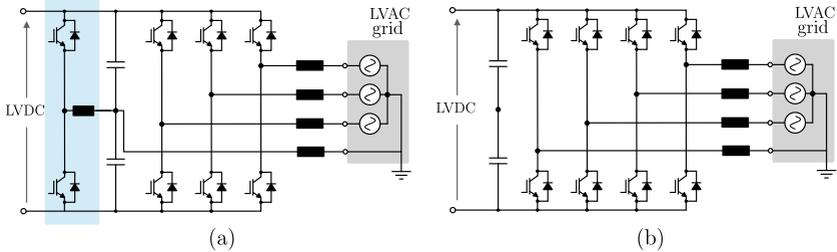
The challenges of this stage are the high current involved and the EMI filter design. Interleaved approach can be used to handle the high current, depending on the power level. Regarding the EMI filter, it must be properly design to avoid disturbance injection in high frequency to the grid.

Its main requirement is the availability of the neutral conductor, once the LV electric distribution grid is based on the Terra-Terra (TT) configuration. Moreover, unbalance and non-linear loads are expected, creating zero sequence current that must be handle by the VSI. A four-wire VSI (with a neutral connection in addition to three-phase connections) are normally used in this case to provide full control over the phase voltages and thereby to ensure good voltage quality. Among the most suitable topologies, the standard two level voltage source inverter (VSI), the three-level neutral point clamped (NPC) and the T-type topologies can be highlighted.

### 2.4.1 2-Level VSI

The topology of the 2-level VSI converter is depicted in Fig. 2.17 and it is considered a very mature technology. Its popularity in different application, such as AC motor drivers, wind and photovoltaic system, many research have been carried out, and many modulation, control strategies and optimization methods have been proposed.

To provide the fourth wire connection, there are two common methods: use split capacitors on the DC link with the neutral conductor connected to the middle-point of the DC link, as shown in Fig. 2.17 (a) [106, 107] or to use a four legs VSI, where the fourth leg is connected to the neutral conductor, as depicted in Fig. 2.17 (b) [69] [108, 109]. The first method is simpler and uses fewer semiconductors. In this case, the VSI operates as three single phase half bridge inverters. Hence, the utilization of the DC link (defined as the peak phase voltage magnitude relative to the LVDC link voltage) is limited. Another drawback is the large zero sequence current produced by unbalanced and nonlinear loads connected to the grid, implying in voltage deviation on the split



**Fig. 2.17:** Topologies of the 2-Level four wires VSI converter: (a) VSI with split capacitors on the DC link with the neutral conductor connected to the middle-point of the DC link, (b) four legs VSI.

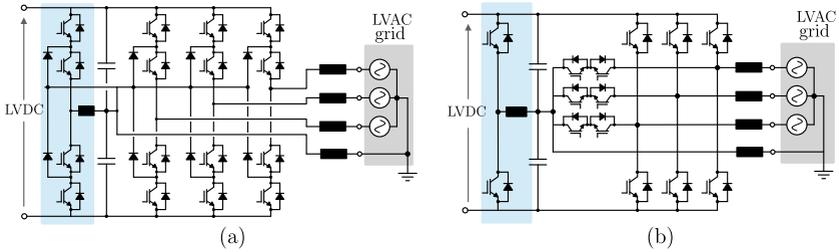
capacitors. It can be attenuated, when large capacitors are used, but increasing the cost. Conversely, the four legs VSI, does not suffer from the unbalance voltage problem, since the fourth legs can manage the zero sequence current. It presents a line-voltage peak equal to half the total DC link voltage, implying in 15% more utilization of the DC link compared to the split capacitor solution [107, 108].

The split capacitor approach is naturally configured for providing the DC link connectivity, since most of the discussed DC grids are based on the bipolar configure (i.e. positive, neutral and negative DC lines). To overcome the aforementioned problem of the split capacitor VSI, a balance circuit can be incorporated to the system as highlighted in Fig. 2.17 (a) and described in [107]. The extra circuit guarantees the capacitor voltage balancing, by the means of the neutral current control, and improves the DC link utilization. In addition, it offer advantages in terms of common mode voltage control, consequently EMI reduction, and management of the DC link voltage.

The high performance of this converter have been demonstrated [71], where an efficiency of 99.3% is mentioned.

### 2.4.2 3-Level NPC

The 3-level NPC, also known as diode clamped converter, was proposed in [110] and it became well accepted by the industry, mainly in AC drivers [64]. Its topology is illustrated in Fig. 2.18. Because its multilevel operation, the output filter size is reduced, as well as the EMI filter. [59, 64]. In contrast to the 2-level, the semiconductors



**Fig. 2.18:** Topology of the 3-Level four wires VSI: (a) neutral point clamped (NPC), (b) T-type VSI.

blocking voltage of the NPC is half of the DC link voltage. Thus, 600 V semiconductor can be used in this topology, benefiting considerably the efficiency. In [69], an optimum design of a NPC for a LV wind system is presented and an efficiency of approximately 99% is described, attesting the high performance of this converter. Its configuration with split capacitor on the DC link allows this topology to provide the fourth wire connection without the requirement of the additional balance circuit. However, the extra leg improves the performance in terms of EMI and energy management of the DC link [111]. Its main drawback is the large amount of power devices compared to the 2-level VSI and the unequal losses distribution on the semiconductor.

An alternative to the diode clamped converter is the T-type 3-level converter, which circuit is shown in Fig. 2.18 (b). Similarly to the standard NPC, the T-type generates a three levels output voltage, reducing the output filter and the EMI filter. It also enables the connection of the neutral wire to the middle-point of its DC link and an extra leg is also considered. On the other hand, this converter presents 16 semiconductors (twice more than the 2-level VSI) and 8 of them are submitted the total DC link voltage, while the others are submitted to half of the DC link voltage. Consequently, semiconductor rated for 1.2 kV are required. Despite this drawback, high performance can be obtained with this topology as described, where an efficiency of 99.2% is presented.

### 2.4.3 Discussion

Many researches have been carried out for the three mentioned topologies and their high performance have already been demonstrated. Re-

**Tab. 2.7:** Characteristics of the two level and three level four wires VSI

Topology	Number of components	Semiconductor voltage	AC peak voltage
Split-capacitor 2-level VSI	8	$V_{dc}$	$(\sqrt{3}/2) V_{dc}$
Four-legs 2-level VSI	8	$V_{dc}$	$V_{dc}$
3-Level standard NPC	24	$V_{dc}/2$	$V_{dc}$
3-Level T-type	16	$V_{dc}/2$	$V_{dc}$

Regardless the adopted topology, the LV stage can reach efficiency around 99% [69–71]. The only characteristic that deserves to be pointed out is the needed of the fourth leg to improve the management of the zero sequence current and voltage control. Table 2.7 presents a brief comparison among the described VSI topologies, in terms of number of semiconductors, semiconductor blocking voltage and maximum AC peak voltage in function of the DC link voltage ( $V_{dc}$ ). Finally, any of these three described converters can be chosen in this work. Thus the conventional VSI with split capacitor is highlighted, because of the reduced number of components. The available design methodology and modulation strategies presented in literature can be successfully used for the LV stage design and it does not deserve further investigation. Thus, this stage is not the focus of this work and then no further analysis is needed.

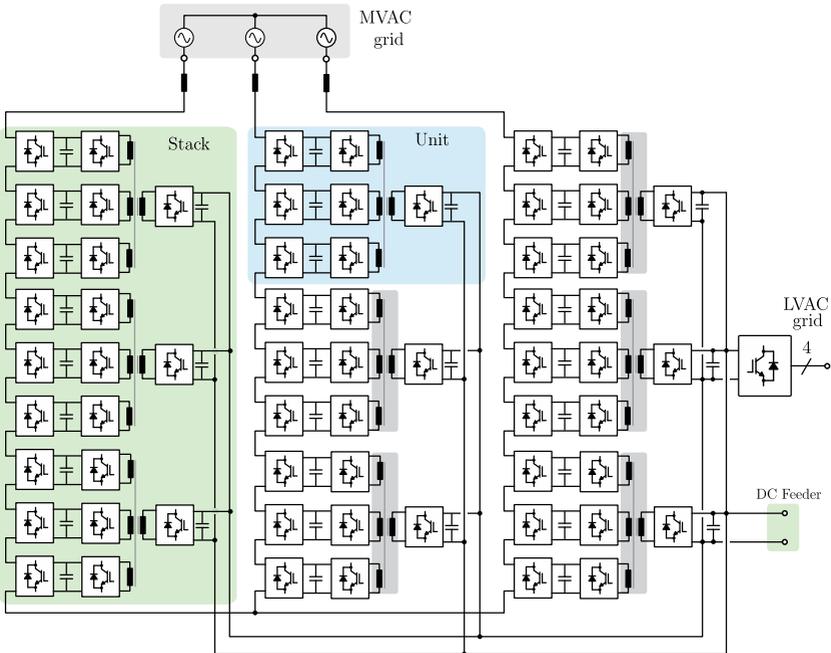
## 2.5 Smart Transformer Architecture

From the topology review and discussion, two suitable ST architectures are finally defined for further investigation and their complete structure are illustrated in Fig. 2.19 and Fig. 2.20. Both architectures use the CHB converter to implement the MV stage and the conventional four wires VSI to implement the LV stage. The architectures differ from each other by the adopted solution of the DC-DC stage, where two strategies are used: MAB-based solution (architecture 1) and SRC-based solution (architecture 2).

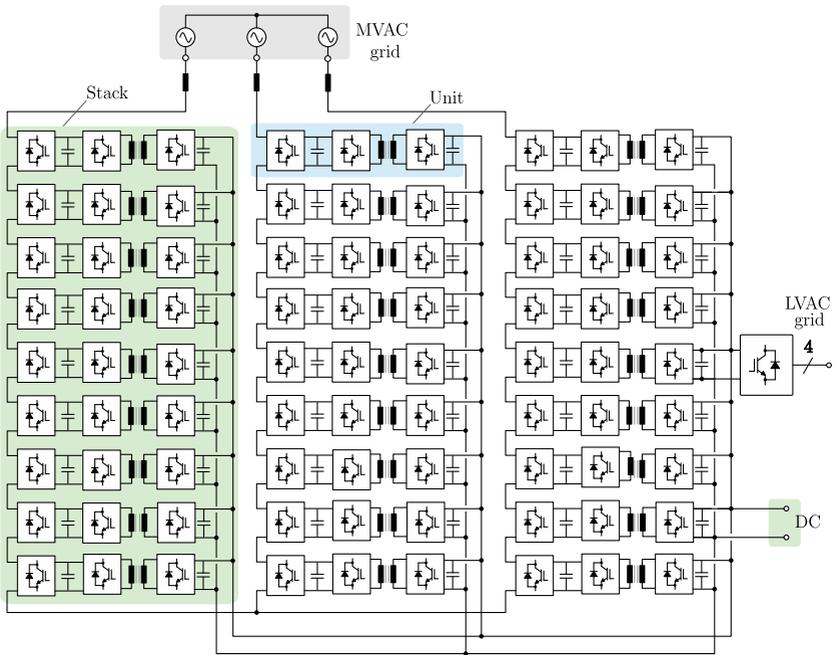
The architecture 1 employs the MAB converter, where four active bridges are used (i.e. QAB converter) and configured as shown in Fig. 2.19. Three bridges are connected to the MV side and one to the LV

side, but different configurations are possible, as described in detailed in chapters 4 and 5. This architecture presents higher performance in terms of control, compared to the other one, because the MAB can control power flow and voltage if necessary. The complete analysis and design of the MAB converter are presented in Chapter 4.

The SRC is adopted in architecture 2, because its high efficiency already demonstrated in literature. The idea is to investigate its potential and the benefits that it can bring to the ST application. Then, the optimum design of this converter is described in Chapter 3 of this thesis. Unlike the MAB converter, the SRC operates in open loop (without control). On one hand, it might be advantageous for SST for traction, because the control system can be simplified. On the other hand, it might be a problem in ST, because the requirement of high performance control system might not be achieved in virtue of its con-



**Fig. 2.19:** Selected modular ST architecture 1: CHB associated to the QAB DC-DC converter.



**Fig. 2.20:** Selected modular ST architecture 2: CHB associated to the SRC DC-DC converter.

trol limitation. Adopting the SRC, the power flow and voltages must be controlled by the MV stage and/or LV stage.

Fig. 2.21 and Fig. 2.22 shows the basic units used to build the modular architectures 1 and 2, respectively. The basic unit is defined as the part that can be combined for conceiving the entire ST system. Once designed, they can be combined to compose the entire architectures, according to the grid specification (voltage and power levels).

Both architectures operate similarly from the perspective of the MV stage and the LV stage. However, they perform different from the viewpoint of the DC-DC stage and indeed different outcomes in terms of efficiency, cost, reliability and capability to provide ancillary services can be expected. The architecture 1 tends to perform better with respect to the cost and capability to provide ancillary services, whereas the second with respect to the efficiency. A qualitative comparison of these two architectures is shown in Fig. 2.23 considering the ST requirements. In

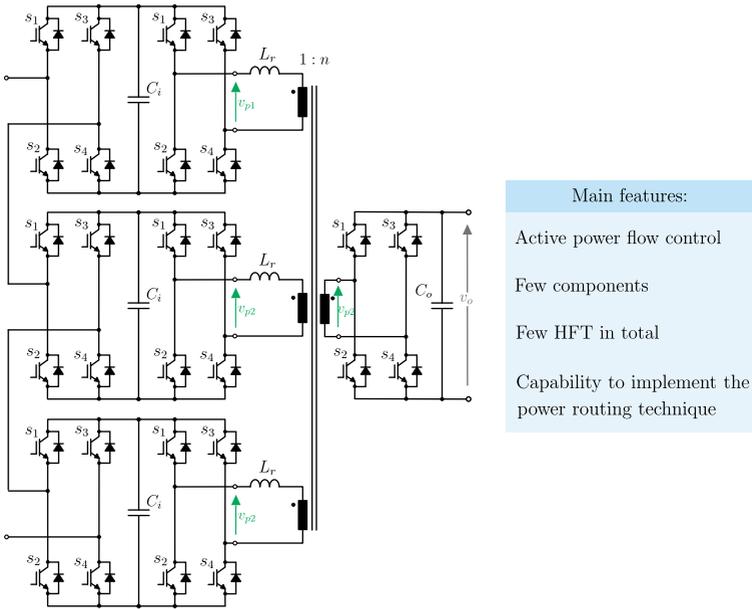


Fig. 2.21: Basic unit of the architecture 1 selected for further investigation.

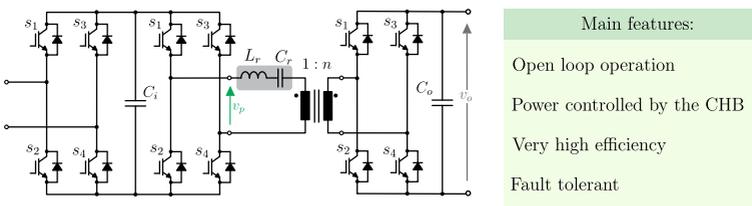
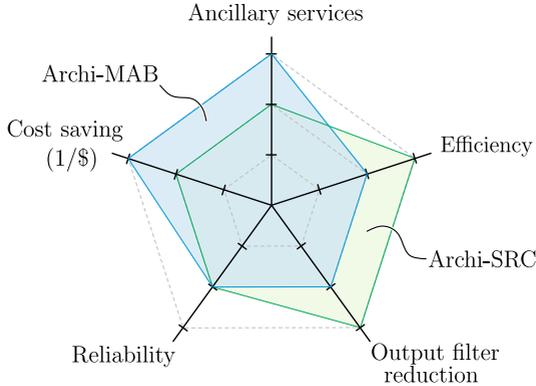


Fig. 2.22: Basic unit of the architecture 2 selected for further investigation.



**Fig. 2.23:** Qualitative comparison of the architectures, considering the ST specifications.

this context, this thesis focus on the DC-DC stage of the ST, where both topologies are analyzed and designed in detail. Each of them has one dedicated chapter of this thesis. The Chapter 3 analyzes the SRC converter, while Chapter 4 studies the MAB converter.

Still, some design parameters presented in Fig. 2.1 needs to be defined, such as semiconductors voltage rating, semiconductor technology choice, optimum number of module, and operation and modulation of the selected converters. All these question will be addressed in the next chapters of this thesis, considering the performance and cost of the ST architecture.

### 2.5.1 Trade off: Number of Module / Semiconductor Voltage Rating

The selection of number of modules or semiconductor voltage rating is one degree of freedom during the ST design. Once one is selected, the other is automatically determined. The fault tolerance capability, number of components, complexity, and the nominal power of the modules are also constrained by number of modules selection. Of course, all these parameters play an important role in the cost, reliability, efficiency, and system complexity. The number of modules is selected from the MV side viewpoint. If a large number of modules is selected, the semiconductor blocking voltage of the MV side is reduced, but the to-

tal number of parts (including the auxiliary power supply, drivers, and communication) and system complexity increase considerably. Consequently, deep investigation is required to guide the correct selection of the number of modules. This topic is analyzed in detail in Chapter 5 of this thesis.

## 2.5.2 Modulation and operation

Many modulation techniques and operation modes can be used for each converter, providing broad options. To define them, the converter's performance, losses distribution, filter size and control requirements must be taken into account.

For the CHB converter, several modulation techniques have been proposed [56–60], but the PSM has presented superior performance and it is used in this work, as discussed further.

The SRC operates in open loop and its operation mode is basically defined to reach the highest possible efficiency. Then, the DCM operation is defined for the SRC, as presented later.

Despite the modulation of the DAB converter has been exhaustively addressed by many researchers, few modulation techniques have been studied for the QAB. Therefore, the triangular current modulation (TCM) strategy already applied for DAB is extended for the QAB converter in this work. The converter's performance is evaluated when the TCM and also the conventional PSM are utilized.

## 2.5.3 Reliability issues

The reliability is addressed through fault tolerant approach and the power routing approach described before. Architecture 1 based on MAB allows the implementation of the power routing approach, as described in [112]. However, the power routing implementation and demonstration is not the focus of this work and then it will not be discussed herein. It is only important to mention that the architecture allows the implementation of such technique. The architecture 2, on the other hand, has limitation regarding the power routing approach implementation. Then, its reliability is improved by the means of the fault tolerance approach. As a result of this studies, a fault tolerant topology of the SRC is proposed and described in detail in Chapter 3. Finally, both architectures can provide high reliability using two different techniques.

## 2.6 Summary

The ST architecture design is not a trivial task, because the numerous options of configurations, power converters and parameters that must be defined. Among the several options, the three-stage modular architectures is presented as the most advantageous one for the ST implementation, because its superior performance in terms of control, fault tolerance capability, scalability, DC link connectivity, etc. This architecture can provide connection to the MVDC link and/or LVDC link, but the availability of the a single LVDC link is more usual.

An overview of the most suitable power electronics converters to implement each stage of the ST was presented and compared. For the MV stage, two converters are highlighted: MMC and CHB. Although the MMC has the advantage to provide accessibility to the MVDC link, the CHB is more advantageous regarding the number of components, capacitance requirement and simplicity. Hence, it is the preferred candidate for the MV stage implementation. Similarly, several options of DC-DC converters are available to be used as the basic module of the modular DC-DC stage. Among them, the MAB and SRC are highlighted as the most suitable options. Consequently, both are selected for further investigation in this work. Finally, the LV stage can be realized based on the conventional 2-level VSI or the 3-level VSI, that can be NPC or T-Type. They are well-established topologies, adopted in different applications and they can be considered mature technology. Then, know-how and experience obtained in this converter from other applications can be used during the design of the LV stage of the ST. As described, regardless the chosen topology, high performance (over 99%) can be obtained. The main requirement for this stage is the fourth wire connection.

After the overview, two ST architecture are defined for further investigation in this work and they differs by the adopted DC-DC stage. Both architectures uses the CHB in the MV stage and the 2-level VSI in the LV stage. Two different strategies are used in the DC-DC stage: MAB-based solution (architecture 1) and SRC-based (architecture 2) solution. While the architecture 1 presents higher current/voltage control capability, the second one is a simple solution in terms of control, but very efficient. Then, both of them are analyzed in detail in the next chapter, considering efficiency, reliability and cost as the main constrains.

## Chapter 3

# Series Resonant DC-DC Converter

**T**HE series resonant DC-DC converter (SRC) is one of the promising converters to be used in the DC-DC stage of the ST, because of its high efficiency, as discussed in Chapter 2. The high performance of such converter have been demonstrated in [49, 97]. Not only the high efficiency, but also the ability to operate in open loop with a well regulated output voltage have motivated its application in SST for electric railway systems [29, 30]. The open loop feature simplifies the control structure of the whole system, which is greatly valuable in this application.

The electric distribution network application, on the other hand, poses additional requirements related to the control system for the ST architecture, because of the desired ancillary services. One of these services that deserves attention is the decoupling between the LVDC link and MVDC link, because it might influence directly the operation of the DC-DC converter. It means that perturbation on the LVDC link should not be translated to the MVDC link and vice-versa. This feature might be difficult to achieve when the SRC is adopted, because the control limitation of that converter. Nevertheless, high performance of the SRC is an appealing reason to adopt that even in ST for distribution grid. In this context, this chapter investigates the SRC converter, where the topology is analyzed and designed, with the aim to achieve the highest possible efficiency. To do so, a computer-aided design is implemented to optimize the converter's efficiency and it will be explained in detail.

Besides the efficiency, the robustness is also an important feature and deserves to be taken into considering during the design of the SRC. Additionally, a fault tolerant technique suitable for the SRC is proposed and a family of the fault tolerant SRC is presented.

### 3.1 Topology of the SRC and Operation Modes

The topology of the SRC is presented in Fig. 3.1, where it is composed by a full-bridge converter on the primary and secondary sides, connected through a tank circuit and a transformer. The tank circuit is composed by a resonant capacitor ( $C_r$ ) connected in series to the resonant inductor ( $L_r$ ). The SRC has different operation modes, according to the load and to the relation between the switching frequency ( $f_s$ ) and resonance frequency ( $f_o$ ). The resonance frequency depends only on the pair  $L_r$  and  $C_r$  and it is defined by equation (3.1).

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (3.1)$$

With respect to the load, the SRC can operate in the continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Regarding the switching frequency, it can operate below the resonant frequency, equal to the resonant frequency and above the resonant frequency [99]. The waveforms of the SRC operating at DCM is depicted in Fig. 3.2, assuming the resonant frequency equal, below and above

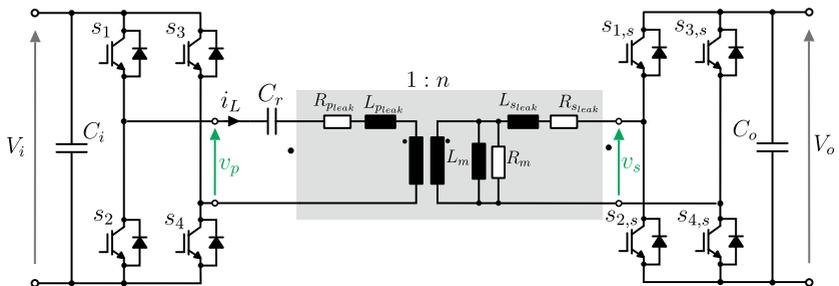
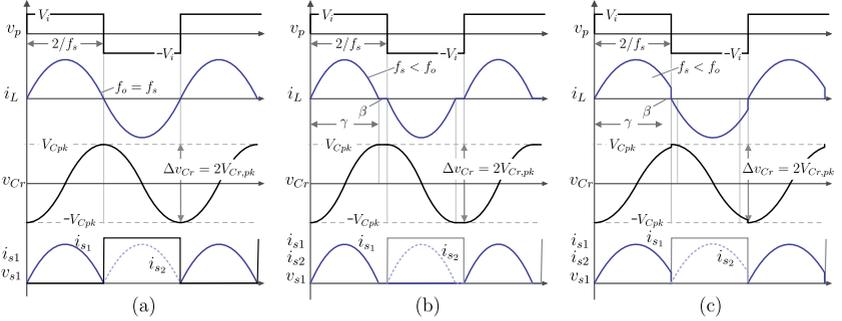
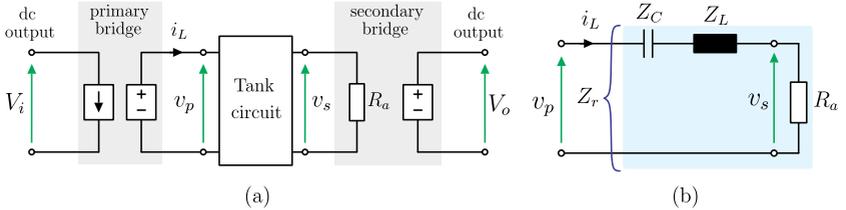


Fig. 3.1: Topology of the series resonant DC-DC converter.



**Fig. 3.2:** Main waveforms of the SRC, i.e. primary side AC voltage ( $v_p$ ), resonant inductor current ( $i_L$ ), voltage over the resonant capacitor ( $v_{cr}$ ) and current and voltage of the primary side semiconductors ( $i_{s1}$ ,  $i_{s2}$ ,  $v_{s1}$ ), considering different operation modes: (a) switching frequency equal to the resonant frequency  $f_s = f_o$  (b)  $f_s < f_o$  and (c)  $f_s > f_o$ .



**Fig. 3.3:** Equivalent circuit of the SRC: (a) complete circuit replacing the controlled switches for equivalent models, (b) equivalence of the tank circuit.

the switching frequency. In this figure, the semiconductor's current and voltage ( $i_{s1}$  and  $v_{s1}$ ) are also illustrated.

### 3.1.1 General Theoretical Analysis

The SRC converter is analyzed according to [98–100] and using the sinusoidal approximation [99]. This approach provides a simple equivalent circuit, because the harmonics of the switching frequency are neglected and only the fundamental component of the tank circuit waveforms are taken into consideration. It means that all waveforms of the tank circuit are considered sinusoidal and. Thus, standard AC circuit analysis can be applied. The relevant parameters used in this analysis are defined in

**Tab. 3.1:** Main parameters used on the analysis of the SRC

Parameter	definition
Angular switching frequency	$\omega_s = 2\pi f_s$
Angular resonant frequency	$\omega_o = 2\pi f_o$
Relative angular frequency	$\omega = \omega_s / \omega_s$
Resonant frequency	$f_o = \frac{1}{2\pi\sqrt{L_r C_r}}$
Quality factor	$Q = \frac{2\pi f_o L_r}{R_a} = \frac{1}{2\pi f_o C_r R_a}$

Table 3.1. The equivalent circuit of the SRC is shown in Fig. 3.3 [99], where the active switches (either primary and secondary side) are modeled as controlled current and voltage sources. In this circuit,  $R_a$  is the equivalent AC load resistance from the viewpoint of the tank circuit. The voltage  $v_p$  is a square wave with magnitude and frequency given by  $V_i$  and  $f_s$ , respectively, as shown in Fig. 3.2 and Fig. 3.4 (a). Hence, the Fourier series can be used to express the voltage  $v_p$ , as described by equation (3.2) and its fundamental component is determined by (3.3).

$$v_p = \frac{4V_i}{\pi} \sum_{m=0}^{\infty} \frac{1}{2m+1} \sin[(2m+1)2\pi f_s t] \quad (3.2)$$

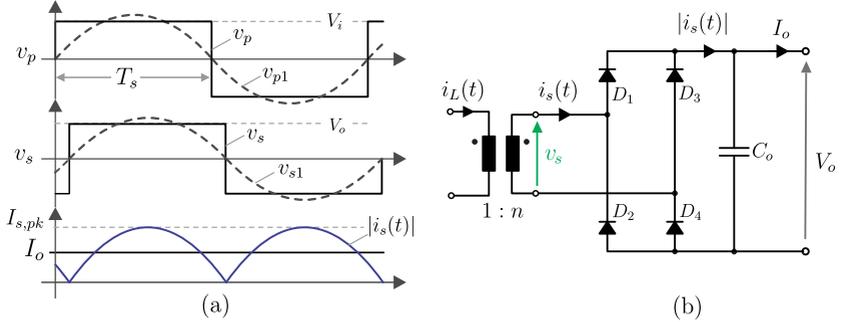
$$v_{p1} = \frac{4V_i}{\pi} \sin(2\pi f_s t) \quad (3.3)$$

The rms value of the fundamental component is calculated by (3.4).

$$V_{p1(rms)} = \frac{2\sqrt{2}}{\pi} V_i \quad (3.4)$$

Similarly, the secondary voltage  $v_s$  is a square wave with magnitude  $V_o$  and frequency  $f_s$ , as shown in Fig. 3.4 (a), and its fundamental component can be determined using the Fourier series, resulting in (3.5).

Thus, the rms value of the secondary voltage is given by (3.6).



**Fig. 3.4:** Equivalent circuit of the SRC: (a) complete circuit replacing the controlled switches for equivalent models, (b) equivalence of the tank circuit.

$$v_{s1} = \frac{4V_o}{\pi} \sin(2\pi f_s t) \quad (3.5)$$

$$V_{s1(rms)} = \frac{2\sqrt{2}}{\pi} V_o \quad (3.6)$$

Although the bidirectional topology of the SRC is presented in Fig. 3.1, the unidirectional version<sup>1</sup> can be used for the fundamental analysis without loss of generality. The following analysis is carried out to determine the equivalent AC resistance  $R_a$  of the equivalent circuit shown in Fig. 3.3.

The current on the secondary side is filtered by the capacitor  $C_o$  and its mean value is equal to the constant output current  $I_o$ , leading to equation (3.7). The waveform on the secondary side is illustrated in Fig. 3.4 (a).

$$I_o = i_{s(avg)} = \frac{2}{T_s} \int_0^{T_s} I_{s,pk} \sin(\omega_o t) dt = \frac{4I_{s,pk}}{\pi} \quad (3.7)$$

The output current  $I_o$  can be expressed as a function of the rms value of secondary current  $I_{s(rms)}$  and vice versa. Reflecting the current of the secondary side to the primary side, the rms current on the inductor is obtained in function of  $I_o$ , as described in (3.9).

<sup>1</sup>The switches on the secondary side bridge are replaced by diodes in the unidirectional version (cf. Fig. 3.4)

$$I_o = \frac{4\sqrt{2}}{\pi} I_{s(rms)} \quad (3.8)$$

$$I_{L(rms)} = \frac{n\pi}{4\sqrt{2}} I_o \quad (3.9)$$

The resistance  $R_a$  can be calculated using the rms current and voltage over this component, as shown in equation (3.10.)

$$R_a = \frac{V_{s(rms)}}{nI_{L(rms)}} = \frac{8}{\pi^2} \frac{R_o}{n^2} \quad (3.10)$$

The equivalent input impedance of the resonant tank circuit, depicted in Fig. 3.3 (b), is calculated by (3.11) and (3.12), in function of the  $L_r$  and  $C_r$ .

$$Z_r = R_a + j \left( \omega_s L_r - \frac{1}{\omega_s C_r} \right) = |Z_r| \angle \phi \quad (3.11)$$

$$\phi = \tan^{-1} \left( \frac{\omega_s L_r - \frac{1}{\omega_s C_r}}{R_a} \right) \quad (3.12)$$

These quantities are rewritten in terms of the quality factor  $Q$ , defined in Table 3.1, as

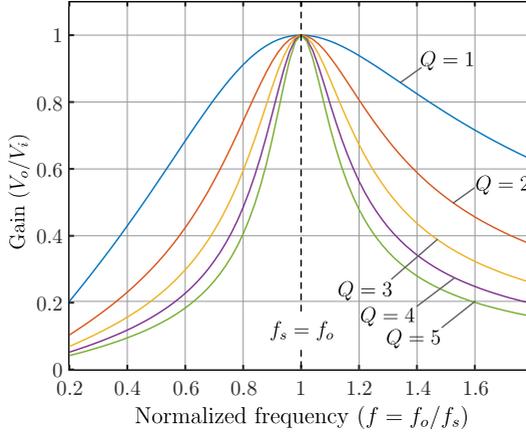
$$Z_r = R_a \left[ 1 + jQ \left( \omega - \frac{1}{\omega} \right) \right] \quad (3.13)$$

$$|Z_r| = R_a \sqrt{1 + Q^2 \left( \omega - \frac{1}{\omega} \right)^2} \quad (3.14)$$

$$\phi = \tan^{-1} \left[ Q \left( \omega - \frac{1}{\omega} \right) \right]. \quad (3.15)$$

The current on the tank circuit ( $i_L$ ) is the tank voltage  $v_{p1}$  divided by the input impedance of the tank circuit, as presented in (3.16).

$$i_L = \frac{V_{s,rms}}{|Z_r| \angle \phi} = \frac{V_i}{R_a \sqrt{1 + Q^2 \left( \omega - \frac{1}{\omega} \right)^2}} \angle (-\phi) \quad (3.16)$$



**Fig. 3.5:** Graphic of the normalized voltage gain ( $V_o/V_i$ ) of the SRC in function of the normalized operation frequency ( $f_o/f_s$ ), according to the quality factor.

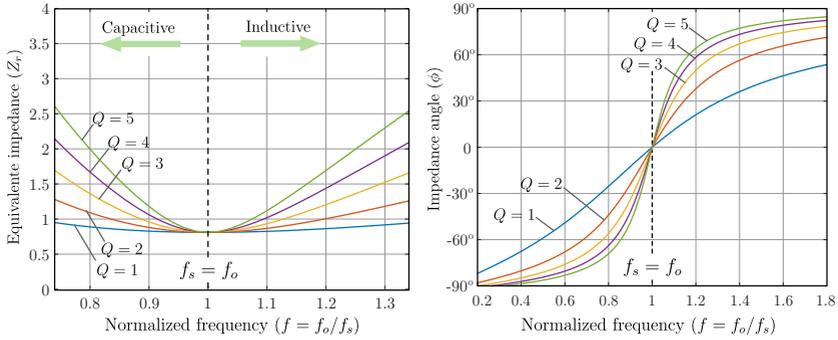
Finally, the output voltage in function of the relative frequency  $\omega$  and the quality factor  $Q$  is calculated by

$$|v_o| = |i_L| R_a = \frac{V_i}{\sqrt{1 + Q^2 \left( \omega - \frac{1}{\omega} \right)^2}} \quad (3.17)$$

The converter's gain ( $v_o/v_i$ ) in function of the relative frequency for several quality factor is plotted in Fig. 3.5. The maximum gain and, consequently, the maximum power transference are obtained at the resonance frequency. This is the preferred operation point of the SRC. Note that the common method to control the output voltage is varying the switching frequency, according to this graphics. On the other hand, this method implies in poor utilization of the HFT<sup>2</sup> and then it is not suitable for ST application, in which the power level is relatively high.

Similarly, the magnitude and displacement angle of the input impedance of the tank circuit are plotted in Fig. 3.6 (a) and (b), respectively. When the SRC operates below the resonance frequency ( $f_s < f_r$ ), the

<sup>2</sup>Using variable switching frequency, the transformer must be designed for the lower switching frequency, penalizing in the volume of the component.



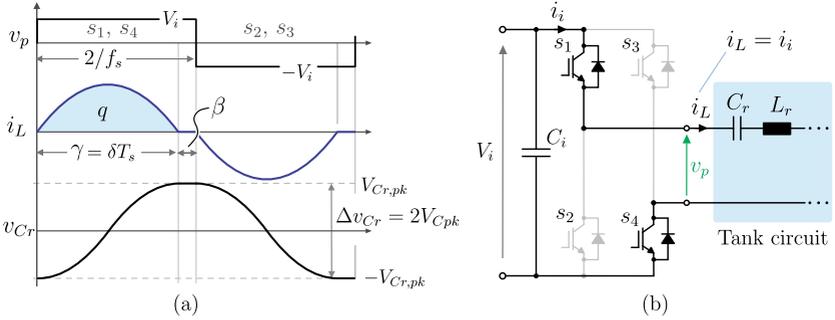
**Fig. 3.6:** Equivalent tank circuit impedance ( $Z_r$ ) in function of the normalized operation frequency ( $f_o/f_s$ ), according to the quality factor: (a) magnitude and (b) displacement angle.

impedance seen by the primary side bridge is capacitive. In this mode, the converter (primary side bridge) operates in ZCS. In contrast to that, when the converter operates above the resonance frequency ( $f_s > f_r$ ), the impedance seen by the primary side bridge is inductive, and the primary side bridge switches at ZVS. For operation at the resonance frequency ( $f_s = f_r$ ), the input impedance of the tank circuit is resistive.

### 3.1.2 SRC Analysis in DCM operation

The most efficient operating point of the SRC is when it operates in DCM with the switching frequency equal or slightly below the resonance frequency. In this operation mode, the primary side semiconductors achieve ZVS and the output switches (secondary side) achieve ZCS. As additional advantages, the converter has good utilization of the transformer and low EMI emission, due to the smooth current shape (low  $di/dt$ ). Therefore, this is the desired operation mode for the converter. Thus, the analysis of the converter operating in its maximum efficiency point is presented next, where the constraints for operating at this point is presented and the equations required for designing the components are derived.

To operate at half-cycle DCM, the parameters of the converter must satisfy the conditions presented in Table 3.2 [99]. The parameter  $\gamma$  is defined as the angular length of half of the resonant period, given in



**Fig. 3.7:** Waveforms of the SRC operating in DCM and the operation of the primary side circuit during the first half resonant period.

radians, and  $\beta$  is defined as the complement of  $\gamma$ , i.e.  $\gamma + \beta = \pi$ . Then,  $\beta$  represents the zero time of the resonant current  $i_L$ , as depicted in Fig. 3.7.

The relation between the amount of charge stored in the capacitor ( $\Delta q$ ) and its voltage ( $v_{Cr}$ ) is given by (3.18). During the period  $0 < t < \delta T_s$  (where  $T_s$  is the switching period), the capacitor voltage starts from  $-V_{Cr,pk}$  and reaches  $V_{Cr,pk}$  (see Fig. 3.7), thus  $\Delta v_{Cr} = 2V_{Cr,pk}$ . Likewise, the charge that flows through the capacitor during this period is defined as  $q$ , as shown in Fig. 3.7. This relation is described in (3.19).

$$\Delta q = C_r \Delta v_C \quad (3.18)$$

$$q = 2 \cdot C_r \cdot V_{Cr,pk} \quad (3.19)$$

The current on the resonant tank, responsible to charge and discharge the capacitor  $C_r$ , is the input current, as illustrated in Fig. 3.7 (b). The instantaneous average value of the input current ( $i_i$ ) is calculated by (3.20). As highlighted in this equation, the integral of the current during the time interval 0 to  $T_s/2$  is the charge accumulated in the capacitor, as depicted in Fig. 3.7. Thus, the relation presented in (3.21) is derived.

$$I_i = \langle i_i(t) \rangle_{T_s} = \frac{2}{T_s} \underbrace{\int_0^{T_s/2} i_i(t) dt}_q \quad (3.20)$$

**Tab. 3.2:** Required condition for the DCM operation of the SRC

Parameter	Condition
Angular length of one half resonant period	$\gamma = \frac{\omega_0}{2f_s} < \pi$
Switching frequency	$f_s < f_0$
Output current	$I_o < 8f_s C_r V_o$

$$I_i = 2f_s q \quad (3.21)$$

Replacing (3.21) in (3.19), the equation (3.22) is obtained, and it can be rearranged to obtain the peak voltage on the capacitor in function of the switching frequency, capacitance value and the load (represented in this equation by the input current  $I_i$ ), as presented in (3.23).

$$\frac{I_i}{2f_s q} = 2 \cdot C_r \cdot V_{Cpk} \quad (3.22)$$

$$V_{Cpk} = \frac{I_i}{8f_s C_r} \quad (3.23)$$

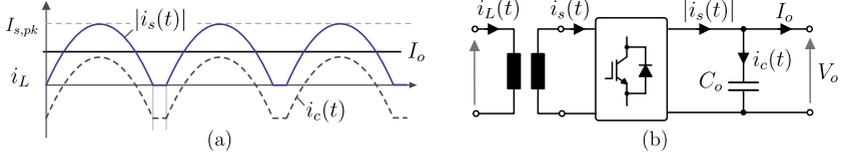
Considering the transformer turn ratio  $n$ , the output voltage of the converter is given by (3.24).

$$V_o = nV_i \quad (3.24)$$

To compute the current stresses on the semiconductors, the peak current on the primary and secondary sides of the transformer are required and they are derived as follow. Analyzing the output circuit of the SRC and using the current waveform illustrated in Fig. 3.8, the output average current can be calculated by

$$I_o = \frac{2}{T_s} \int_0^{\delta T_s} I_{s,pk} \sin(\omega_o t) dt = \frac{4\delta I_{s,pk}}{\pi} = \frac{2I_{s,pk}}{\gamma}. \quad (3.25)$$

Consequently, the peak current on secondary and primary sides of the transformer are calculated by (3.26) and (3.27), respectively.



**Fig. 3.8:** (a) Current waveforms of the output circuit of the SRC converter, i.e. rectifier current on the secondary side ( $|i_s(t)|$ ) and output average current ( $I_o$ ), (b) equivalent circuit of the SRC.

$$I_{s,pk} = \frac{P_o}{4f_s V_o \sqrt{L_r C_r}} \quad (3.26)$$

$$I_{L,pk} = \frac{nP_o}{4f_s V_o \sqrt{L_r C_r}} \quad (3.27)$$

Applying the concept of average current and using the waveforms shown in Fig. 3.2 (b), the average current on the semiconductors are determined and presented in (3.28).

$$I_{s1(avg)} = \frac{1}{T_s} \int_0^{\delta T_s} I_{L,pk} \sin(\omega_o t) dt = \frac{2\delta I_{L,pk}}{\pi} = \frac{I_{L,pk}}{\gamma} \quad (3.28)$$

Replacing (3.26) and (3.27) in (3.28), the average current of the semiconductors of the primary and secondary sides are derived and shown in (3.29) and (3.30), respectively.

$$I_{s1(avg)} = 2I_{L,pk} f_s \sqrt{L_r C_r} = \frac{nP_o}{V_o} \quad (3.29)$$

$$I_{s1_s(avg)} = 2I_{s,pk} f_s \sqrt{L_r C_r} = \frac{P_o}{V_o} \quad (3.30)$$

Finally, the rms current on the semiconductors are calculated based on the waveforms shown in Fig. 3.2 (b), resulting in

$$I_{s1(rms)} = \sqrt{\frac{1}{T_s} \int_0^{\delta T_s} [I_{L,pk} \sin(\omega_o t)]^2 dt} = I_{L,pk} \sqrt{\frac{\delta}{2}} = I_{L,pk} \sqrt{\frac{\pi}{4\gamma}}. \quad (3.31)$$

Thus, the rms current on the primary and secondary sides semiconductors are calculated by (3.32) and (3.33), respectively.

$$I_{s1(rms)} = \frac{I_{L,pk}}{2} \sqrt{2f_s \sqrt{L_r C_r}} = \frac{nP_o}{8V_o} \sqrt{\frac{2\pi}{f_s \sqrt{L_r C_r}}} \quad (3.32)$$

$$I_{s1s(rms)} = \frac{P_o}{8V_o} \sqrt{\frac{2\pi}{f_s \sqrt{L_r C_r}}} \quad (3.33)$$

The rms current on the resonant inductor (i.e. primary side of the transformer) and secondary side of the transformer are calculated by (3.34) and (3.35).

$$I_{L(rms)} = \frac{nP_o}{4V_o} \sqrt{\frac{\pi}{f_s \sqrt{L_r C_r}}} \quad (3.34)$$

$$I_{S(rms)} = \frac{P_o}{4V_o} \sqrt{\frac{\pi}{f_s \sqrt{L_r C_r}}} \quad (3.35)$$

The rms current on the output filter capacitor is then computed by (3.36).

$$I_{C_o(rms)} = \frac{P_o}{V_o} \sqrt{\frac{\pi}{16f_s \sqrt{L_r C_r}} - 1} \quad (3.36)$$

Despite the average current values on the semiconductors are not dependent on the tank circuit parameters ( $L_r$ ,  $C_r$ ), the rms currents in all components are. It means that the selection of these parameters plays an important role on the converter's performance and it needs to be carefully calculated. Further discussion in this sense is presented during the converter's design.

## 3.2 Reliability Assessment

Recently, most of the research carried out on the DC-DC converter field has paid much attention to the efficiency improvement and many optimization methods have been discussed in literature. In addition to the high efficiency feature, the continuity of operation is of paramount importance and then a highly reliable system with a long lifetime is required [48]. Although the reliability is considered even more important

than the efficiency in ST application, issues related to the DC-DC reliability have not been deeply investigated. Currently, very few papers have addressed reliability improvement of DC-DC converters by using fault tolerance approach [113, 114] and the lifetime extension approach for DC-DC converters has not yet been discussed on the literature. The DC-DC stage of the ST is not only supposed to be efficient, but also very robust. Then, both characteristics are carefully analyzed and a design procedure for the SRC considering them is presented later.

To achieve high reliability, the most susceptible devices (those most likely to fail) are evaluated through the Failure Mode and Effect Analysis (FMEA) approach and its application to the SRC converter is presented in Table 3.3. In this table, the most faulty devices are presented, as well as the failure mode and the cause of the fault. Indeed, recognize the devices most likely to fail allows to anticipate some methods (either or the design, topology variation, etc) to avoid the failure. Nevertheless, this information is not usually accessible in literature and only few industries reports [115, 116] are available. In addition to the available reports [115, 116], a survey about failure analysis and fragile devices of the SRC was carried out taking into account the vast knowledge of the universities and the practical experience of industries, with the aim to collect relevant information in this regards and subsequently draw a solid conclusion. The description and detail of the survey study is presented in the Appendix A of this thesis. Both studies agree that the most vulnerable device on the SRC is the primary side semiconductor, usually implemented using MOSFETs [115, 116]. In the second place is the resonant capacitors ( $C_r$ ). To improve the robustness of the converter and consequently the ST reliability, the failure causes on these two components are analyzed with the aim to propose methodologies to avoid or postpone the fault.

► **Primary side semiconductor failure:**

Independently from the mechanism, there are two possible failures types for the semiconductor: open-circuit (OC) or short-circuit (SC). According to [117, 118], the reasons that implies in OC failure are: bond-wire lift off or rupture and failure on the gate drive. Meanwhile, the SC failure might be a result of an overvoltage, static or dynamic latch up, second breakdown or energy shock. For voltage source converter, which is the case of the SRC, the OC fault is not tragic, since the power flow is naturally interrupted. Instead, the SC fault is catastrophic, because

**Tab. 3.3:** Failure Mode and Effects Analysis of the SRC

Faulty device	Failure mode	Failure cause
Semiconductor devices	short-circuit	current stress overvoltage Load SC
Resonant capacitor ( $C_r$ )	open-circuit	current stress overvoltage/start-up overload/SC

of the uncontrolled short current, implying in destructive damage to the power converter. In addition, the SC failure type is mostly likely to happen in real application than the OC failure.

As can be observed in Table 3.3, the fault on the switches leads to a short-circuit (SC) state of this device, regardless the reason, according to [116]. To avoid such problem, a fault tolerance scheme for the SRC is proposed and described in detail in Section 4. The proposed method guarantees the operation continuity of the SRC after the failure (either OC or SC) of primary side semiconductor, contributing significantly for the reliability improvement.

► **Resonant capacitor failure:**

The resonant capacitor is listed as the second most susceptible device to failure. The reasons for that are the start-up conditions (leading to an overvoltage), and also the current stress caused by the load variation (as short-circuit or overload). Normally, most of the failures lead to an OC condition [119]. In order to postpone as much as possible the capacitor failure, its lifetime model is evaluated, in order to implement a reliability-based design.

### 3.3 Design of the SRC for ST

The SRC is expected to reach high efficiency, as aforementioned, and this section focus on the design to achieve such target. Apart from the efficiency, the robustness is also a very important constrain, as described in section 3.2. In this regards, the optimum design of the proposed SRC is presented, focusing on the efficiency and reliability improvement.

**Tab. 3.4:** Specification of the SRC

Input voltage	Output Voltage	Nominal Power	Frequency
800 V	700 V	10 kW	20 kHz

The SRC reliability is improved by means of the lifetime-oriented design for the resonant capacitor, which is the second most susceptible device. This postpones the capacitor's failure, increasing the converter's availability. To improve the efficiency, the losses modeling is realized for all components with the aim to identify those parameters that deteriorate the efficiency of the converter. Moreover, a computer-aided design is implemented to assist the design parameters choice.

Using the modular approach, the basic module can be designed only once and combined to reach the ST specification. Consequently, the specification presented in Table 3.4 is chosen for the SRC design. The voltage level enables the use of semiconductors rated for 1.2 kV in both primary and secondary sides, implying in a wide variety of device choice. It benefits both efficiency and cost.

Generally, the converter is designed to operate at the resonant frequency ( $f_s = f_o$ ) or slightly bellow [49], reaching then the maximum efficiency point. To do so, the pair  $L_r$  and  $C_r$  have to satisfy the condition imposed by (3.1). Thus, there is one degree of freedom to select one of these parameters, while the other is chosen consequently. Nevertheless, the selection of the pair  $L_r$  and  $C_r$  has an impact on the current and voltage effort on the resonant capacitor, influencing its lifetime. Therefore, the selection of  $L_r$  and  $C_r$  plays an important role not only on the converter's efficiency, but also on the components lifetime. This aspect will be discussed in the next sections.

As the converter operates with soft-switching, high switching frequency can be chosen, leading to the reduction of the passive components. However, the HFT requires high voltage isolation, as determined by the application [19], and this sets an upper limit to the operating frequency. In fact, since primary and secondary windings must be spatially separated, proximity effect would increase copper losses. Moreover, given a constant probability of partial discharge, a higher switching frequency translates into more partial discharge events, with detrimental effects on the transformer lifetime. For these reasons, 20

kHz is selected, as shown in Table 3.4.

### 3.3.1 Losses Modeling

The losses in the main components are carefully computed in function of the main converter parameters, with the aim of properly selecting these parameter, minimizing the losses.

#### Semiconductors

The standard IGBT are the usual employed semiconductor for the power and voltage levels of the SRC. Nevertheless, one of the basic premises of this research is to assess the impact of different technology of semiconductors on the converter's performance. Consequently, the pure Si IGBT and SiC MOSFETs are considered on the design of the SRC. SiC MOSFETs with the voltage class of 1.2 kV are characterized by a very low switching energy and a very low  $R_{DS(on)}$ . Its high performance has penalty in cost.

For the primary side, the losses are computed considering the SiC-MOSFETs and Si-IGBT presented in Table 3.5. The conduction losses of the primary side MOSFETs can be calculated by (3.37), where the on-resistance ( $R_{DS(on)}$ ) is a function of the drain-source current ( $i_{dc}$ ), junction temperature ( $T_J$ ) and gate voltage ( $V_{gs}$ ). Assuming a constant junction temperature of  $100^\circ C$  and a constant gate voltage of 15 V, the equation is simplified to (3.38). Using the rms current on the semiconductors, previously calculated in (3.32), the semiconductors losses are then determined by (3.38). As can be observed, the conduction losses are highly depends on the tank circuit components ( $L_r$  and  $C_r$ ).

$$P_{prim(cond)} = \frac{1}{T} \int_0^T R_{ds(on)}(i_{ds}(t), T_J, V_{gs}) \cdot i_{ds}^2(t) dt \quad (3.37)$$

$$P_{S_1(cond)} = R_{ds(on)} \cdot I_{S_1(rms)}^2 = R_{ds(on)} \cdot \left( \frac{nP_o}{8V_o} \sqrt{\frac{2\pi}{f_s \sqrt{L_r C_r}}} \right)^2 \quad (3.38)$$

For the secondary side, bidirectional switches need to be used, because of the bidirectional power flow requirement of the converter. Nonetheless, the converter operates most often transferring the power

**Tab. 3.5:** Specification of the semiconductors considered in the design

MOSFET - MV side					
Type	Reference	V	I	$R_{ds(on)}$ (@150 C)	$E_{off}$
SiC	C2M0040120D	1.2 kV	40 A	84m $\Omega$	0.3 mJ
SiC	C2M0025120D	1.2 kV	90 A	43m $\Omega$	0.3 mJ
IGBT - LV side					
Type	Reference	V	I	$V_{CE(on)}$ (@150 C)	$E_{off}$
Si	IHW40N120R3	1.2 kV	80 A	2.4V	3.1 mJ
Diode - LV side					
Type	Reference	V	I	$V_{F(on)}$ (@25 C)	$Q_C$
SiC	C4D20120D	1.2 kV	16,5 A	3V	52 nC
SiC	C4D40120D	1.2 kV	40 A	3V	130 nC

from MV to LV side, making the use of SiC-MOSFETs even in the secondary side not economically justifiable. Then, IGBTs in parallel with high performance SiC diodes are therefore the most suitable choice. In this circumstances, the IGBTs operate only in reverse power flow case, which is very rare to happen. Then, the converter's efficiency is not compromised, even if low cost IGBT are selected. The diodes considered for SRC design are presented in Table 3.5. The conduction losses of the secondary side diodes can be calculated in function of the current and devices parameters by (3.39). Similarly as for the MOSFET, the diodes conduction losses are highly dependent on  $L_r$  and  $C_r$ . The influence on  $L_r$  and  $C_r$  is discussed in section V.

$$P_{sec(cond)} = \frac{1}{T} \int_0^T V_F(i_F(t), T_J) \cdot i_F(t) dt \quad (3.39)$$

$$\begin{aligned} P_{D_1(cond)} &= V_F \cdot I_{D_1(avg)} + R_F \cdot I_{D_1(rms)}^2 \\ &= V_F \cdot \left( \frac{P_o}{2V_o} \right) + R_{ds(on)} \cdot \left( \frac{P_o}{8V_o} \sqrt{\frac{2\pi}{f_s \sqrt{L_r C_r}}} \right)^2 \end{aligned} \quad (3.40)$$

As the converter operates under soft-switching condition with ZVS and ZCS on the primary side and ZCS on the secondary, the switching losses can be neglected.

### Output Filter Capacitor

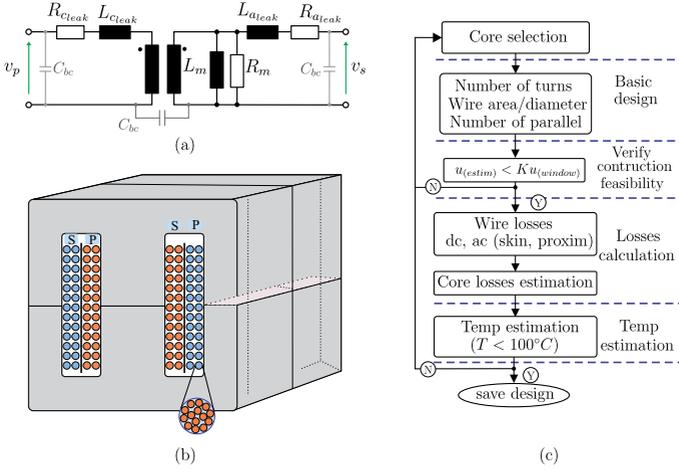
For the dc link capacitor, the aluminum electrolytic capacitor from EPCOS (*long-life* series), with 1000  $\mu F$  capacitance and voltage rating of 450 V is used. This type of capacitor is chosen because of its high energy storage density, compared to other types. The capacitor has an equivalent series resistance of  $R_{ESR} = 55 \text{ m}\Omega$ . Because of the voltage rating of the capacitors, two devices need to be connected in series. The losses on this component are calculated according to

$$P_{C_o} = 2 \cdot R_{ESR} \cdot I_{C_o(rms)}^2 = 2 \cdot R_{ESR} \cdot \left( \frac{P_o}{V_o} \sqrt{\frac{\pi}{16f_s \sqrt{L_r C_r}} - 1} \right)^2. \quad (3.41)$$

### Medium-Frequency Transformer Design

In order to optimize the transformer losses, taking into account also the transformer size, a computer-aided design was carried out, and the algorithm flowchart is depicted in Fig. 3.9. The database populated with suitable E-type ferrite cores was created and it is shown in Table 3.6. The core-type construction as shown in Fig. 3.9 is also assumed. The algorithm starts with the smallest core selection, in this case a single E 55/28/21, and then the basic design is performed. In this point, the number of turn of both windings is calculated and the wires are selected. In the next point, the implementation feasibility is verified by comparing the available window area of the selected core with the area required for the design. If the transformer can not be built, a bigger core is selected and the procedure starts again. Otherwise, the algorithm goes to the next point: losses calculation.

For the wire losses, the skin and proximity effect are considered additionally to the DC losses. To avoid the skin effect, litz wire is used. The losses caused by proximity effect are estimated based on [120]. For the core losses, the Steinmetz equation is used, due to the almost pure sinusoidal current waveform [121]. Finally, the temperature is estimated according to [122] under the assumption of natural convection cooling. The design result is summarized in Table 3.7. Discussions about the transformer implementation and experimental verification are presented in the *Subsection 3.3.4*.



**Fig. 3.9:** Electric model of the MFT, showing the parasitic elements. Implementation scheme of the MFT, showing the disposition of the primary and secondary windings in the core. The simplified flowchart of the algorithm used to design the optimized MFT.

**Tab. 3.6:** Specification of the ferrite cores considered in the design

Core	Ferrite Material	Specification	N <sup>o</sup> of parallel cores
E 55/28/21	N87/N97	B66335	up to 3
E 65/32/27	N87	B66387	up to 3
E 70/33/32	N87	B66371	up to 2
E 80/38/20	N87	B66375	1

**Tab. 3.7:** Physical implementation of the transformer

Core	N of turns	wire
2x E 65/32/27	$n_{pri} = 26$	90 x AWG32
	$n_{sec} = 22$	2000 x AWG44

### 3.3.2 Reliability Analysis

The robustness improvement is also the goal of this design procedure. The failure analysis of the SRC presented in Table 3.3 shows that the most susceptible devices to fail are the primary side semiconductor and the resonant capacitor. To postpone the failure provoked by the resonant capacitor, its lifetime model is evaluated in order to verify the parameters that can extend it. It results in a reliability-based design, as presented next.

#### Capacitor Lifetime Analysis

The Metalized Polypropylene Film (MPPF) capacitors from WIMA (MKP10 series) are used to implement the capacitor bank of the tank circuit. The considered capacitors are: 150 nF, 330 nF, 680 nF, all rated for 400  $V_{ac}$  / 650  $V_{dc}$ . According to [123], the lifetime model for this kind of capacitor is given by (3.42), where  $L_o$  is the expected lifetime tested by the manufacturer,  $V_{Cr}$  and  $V_o$  are the capacitor voltage at use condition and test condition, respectively.  $T$  and  $T_o$  are the temperature at use condition and test condition, respectively, in Kelvin.  $K_B$  is the Boltzmanns constant (8.62105 eV/K),  $E_a$  is the activation energy, and  $n$  is the voltage stress exponent and these last constants depends on the manufacturer [123]. As can be noticed in (3.42), the capacitors lifetime ( $L$ ) does not depend only on the capacitor voltage ( $V_{Cpk}$ ), but also from the rms inductor current ( $i_{L(rms)}$ ), which is directly related to the operation temperature. Since both parameters  $V_{Cr}$  and  $i_{L(rms)}$  can be rewritten in terms of  $L_r$  and  $C_r$ , as demonstrated in equations (3.43) and (3.44), then the capacitor lifetime depends on  $L_r$  and  $C_r$ , as shown in (3.45).

$$L = L_o \cdot \left( \frac{V_{Cr}}{V_o} \right)^{-n} \cdot e \left[ \left( \frac{E_a}{K_b} \right) \cdot \left( \frac{1}{T(i_{L(rms)}, i_{L(os)})} - \frac{1}{T_o} \right) \right] \quad (3.42)$$

$$V_{Cr}(C_r) = \frac{I_i}{8f_s C_r} \quad (3.43)$$

$$i_{L(rms)}(L_r, C_r) = \frac{nP_o}{4V_o} \sqrt{\frac{\pi}{f_s \sqrt{L_r C_r}}} \quad (3.44)$$

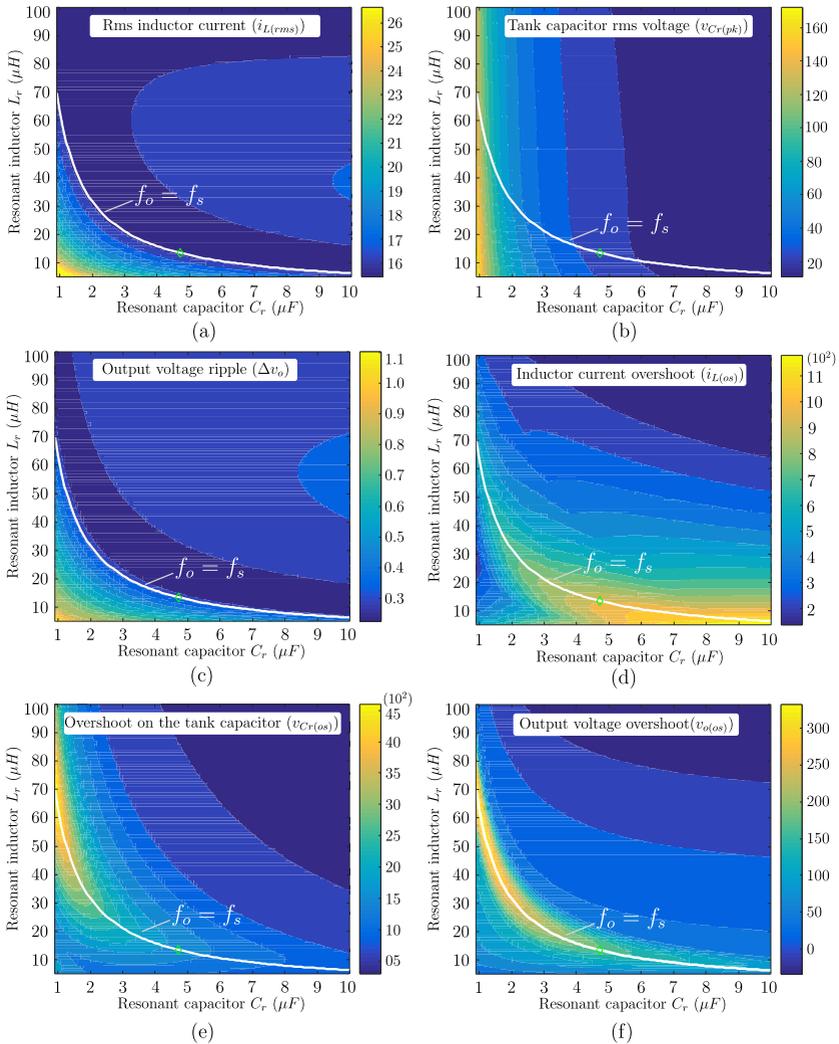
$$L(V, T) \sim L(i_{L(rms)}, i_{L(os)}, V_{Cpk}) \sim L(L_r, C_r) \quad (3.45)$$

In this context, the influence of the  $L_r$  and  $C_r$  pair selection on the capacitor lifetime is evaluated. To do so, the main parameters that have influence on the lifetime capacitor, i.e. the rms inductor current, capacitor voltage and output voltage ripple are analyzed in function of  $L_r$  and  $C_r$ , resulting in the graphics plotted in Fig. 3.10.

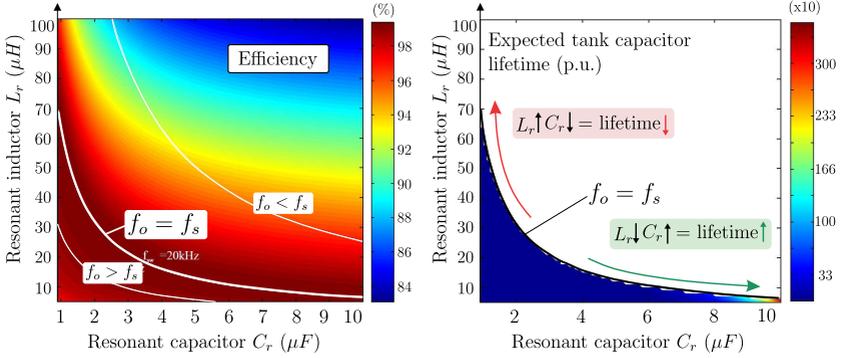
Although the output voltage ripple and output voltage overshoot have no effect on the capacitor lifetime, they are analyzed, because these parameters are very important for the converter and they also depend from  $L_r$  and  $C_r$ . To plot these graphics, two operation conditions were considered:

1. Normal condition: steady-state operation, shown in Fig. 3.10 (a) to (c);
2. Abnormal condition: start-up and load variation, depicted in Fig. 3.10 (d) to (f).

Furthermore, the resonant frequency ( $f_o$ ) was kept constant and the operation point of  $f_o = f_s$  is highlighted in those plots. For normal operation and assuming a constant resonant frequency, it is noticed that the  $L_r$  and  $C_r$  does not affect the rms current on the inductor (see Fig. 3.10 (a)) and output voltage ripple (see Fig. 3.10 (c)). Nevertheless, the rms voltage on the capacitor (see Fig. 3.10 (b)) is minimized if the  $C_r$  value is the biggest possible. Under abnormal operation, if a small  $L_r$  and big  $C_r$  are chosen, the output voltage overshoot (represented in Fig. 3.10 (f)) and tank capacitor voltage overshoot (see Fig. 3.10 (e)) are minimized, whereas the inductor current overshoot is maximized (see Fig. 3.10 (d)), influencing negatively the capacitor lifetime. On the other hand, if a big  $L_r$  and small  $C_r$  are chosen, the inductor current overshoot is minimized, whereas the output voltage overshoot and the tank capacitor voltage overshoot are maximized, also influencing negatively the capacitor lifetime. Hence, to verify quantitatively the influence of  $L_r$  and  $C_r$  on the capacitor lifetime, all these graphics are combined and a capacitor lifetime model based in  $L_r$  and  $C_r$  is obtained, as plotted in Fig. 3.11 (b). Similarly, the efficiency curve of the SRC in function of the  $L_r$  and  $C_r$  also plotted in Fig. 3.11 (a), by using the losses equations described previously.



**Fig. 3.10:** Current and voltage stresses (during normal and abnormal condition) on the main components of the SRC in function of  $L_r$  and  $C_r$ . For normal operation (steady-state): (a) rms current on the resonant inductor ( $I_{L(rms)}$ ), (b) rms voltage on the resonant capacitor, (c) output voltage ripple. For abnormal operation: (d) current overshoot on the resonant inductor, (e) voltage overshoot on the resonant inductor, (f) output voltage overshoot.



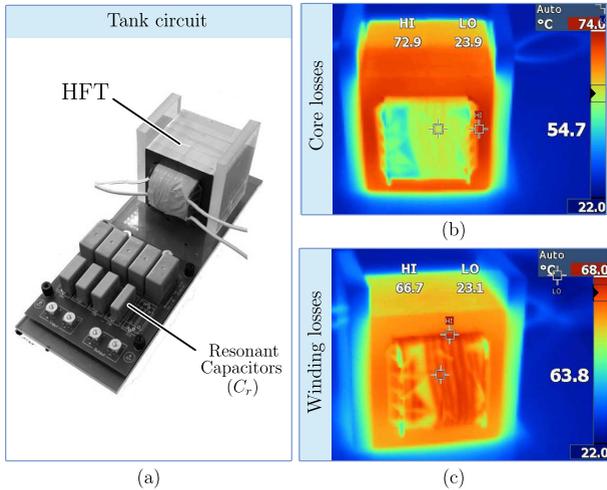
**Fig. 3.11:** Graphic analysis of the SRC efficiency (a) and resonant capacitor lifetime (reliability) (b) in terms of the  $L_r$  and  $C_r$ .

### 3.3.3 Tank Circuit Parameter Selection

Analyzing the curves of efficiency and capacitor lifetime presented in Fig. 3.11, it is noticed that the efficiency reaches its maximum value when  $f_o = f_s$ , as expected and already discussed. According to the graphic depicted in Fig. 3.11 (b), the capacitor lifetime is longer for lower values of  $L_r$  and higher values of  $C_r$ . Therefore, to extend as much as possible the capacitor lifetime, the inductance  $L_r$  must be as smaller as possible, while the capacitance  $C_r$  should be as big as possible, keeping  $f_o$  constant. The minimum inductance value possible is constrained by the leakage inductance of the transformer. Therefore, only the leakage inductance of the transformer should be used and no external inductance is added.

### 3.3.4 High-Frequency Transformer Implementation and Tests

The HFT was implemented according to the design presented in *subsection 3.3.1*. As a result from the design, two cores type E65/32/27 from EPCOS/TDK were used in parallel and the physical implementation is described in Table 3.7. The picture of the resonant tank circuit is depicted in Fig. 3.12 (a), where the implemented transformer is observed. The implemented transformer was experimentally evaluated and its main parameters, as well as the core losses and wire losses were



**Fig. 3.12:** Picture of the implemented HFT and the temperature obtained during the open-circuit and short-circuit tests: (b) core losses (open-circuit test) and (c) wire losses (short-circuit)

**Tab. 3.8:** Measured parameters of the MFT

Leakage inductance	$L_{leak} = 13.5\mu H$
Winding resistance (primary and secondary)	$R_{wire} = 86m\Omega$
Magnetizing inductance	$L_m = 7.93mH$
Core Losses	$R_{core} = 309.5k\Omega$
Total Losses	$P_{MFT} = 56.4W$

obtained. The intrinsic parameters of the transformer are shown in Table 3.8.

In order to evaluate more carefully the power dissipated on the transformer, the open-circuit and short-circuit tests were performed according to [124]. From these tests, it is possible to separate the core losses from the wire losses and to obtain the wire losses decomposition in AC and DC losses. The total losses of the MFT are presented in Table 3.8, while the losses distribution is depicted in Fig. 3.18 (b). As can be observed, the wires are responsible for most of the losses (61%), where

22% of this value are the AC losses, due to the proximity effect. The expected AC losses is between 20% and 30% of the total wire losses. Thus, the obtained value is in accordance to the analysis, showing a good implementation of the transformer.

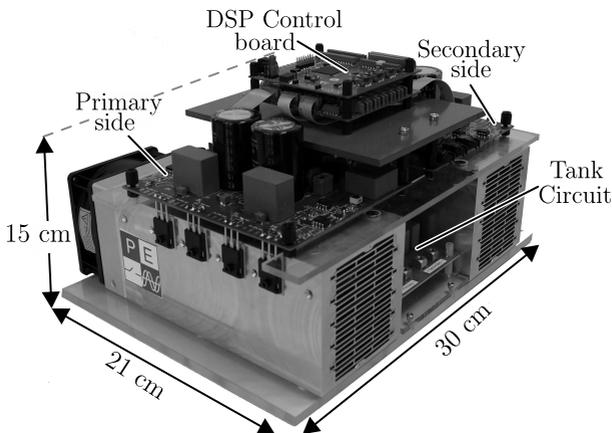
Finally, the temperature were measured in both tests, in order to check the temperature rise due to the core and wire losses individually. The results are presented in Fig. 3.12 (b) and (c) and it is observed that the temperature is well below the maximum of  $100^{\circ}C$ .

### 3.3.5 Power Stage Hardware Implementation

Once the resonant frequency and the transformer leakage inductance are chosen, the resonant capacitance ( $C_r$ ) can be determined. As discussed in Section IV, the resonant inductance should be the transformer leakage inductance, then  $L_r = 13.5 \mu H$ . To select the resonant frequency, the dead-time between the semiconductors of the same leg should be taken into account. Moreover, a resonance frequency slight above the switching should be selected, so that the inductor current can have a small zero-time, allowing the semiconductors to deplete their stored charge. Therefore, assuming a dead-time of  $1 \mu s$ , the resonance frequency of  $f_o = 21.7 kHz$  is selected<sup>3</sup>. To obtain this value, the resonant capacitance should be  $C_r = 4.3 \mu F$ . Thus, the  $C_r$  is implemented by using 9 capacitors of  $330 nF$  and 2 capacitors of  $680 nF$  connected in parallel.

For the semiconductor selection, those devices that provide the minimum conduction losses are selected, since the switching losses are neglected, due to the soft-switching operation of the converter. For the primary side, two SiC-MOSFET were considered during the design (see Table 3.5). The SiC MOSFET C2M0025120D is select to be used on the prototype implementation, because of its lower  $R_{DS(on)}$  and consequently lower power dissipation. For the secondary side, IGBT and a SiC diode are used in parallel as discussed in Section III. The silicon IGBT IHW40N120R3 optimized for lower conduction losses is chosen. For the SiC diode selection, two options are provided in Table 3.5 and they perform similarly from the conduction losses viewpoint. However,

<sup>3</sup>Note that  $T_o < T_s - 2T_{dt}$ , where  $T_o$  is the resonant period and  $T_{dt}$  is the dead-time. Assuming  $T_{dt} = 1 \mu s$  and  $T_s = 20 \mu s$ , then  $f_{o,min} = 20.8 kHz$ . Besides that, a time interval of approximately  $2 \mu s$  is considered as a safety margin to ensure that the converter operates at half-cycle DCM mode. Thus, the  $f_o = 21.7 kHz$ .



**Fig. 3.13:** Implemented 10 kW SRC converter hardware prototype (mechanical dimensions: 300 mm x 210 mm x 150 mm).

the device C4D20120D presents a lower reverse recovery charge, and for that reason it is selected for the prototype implementation.

### 3.3.6 Experimental Results

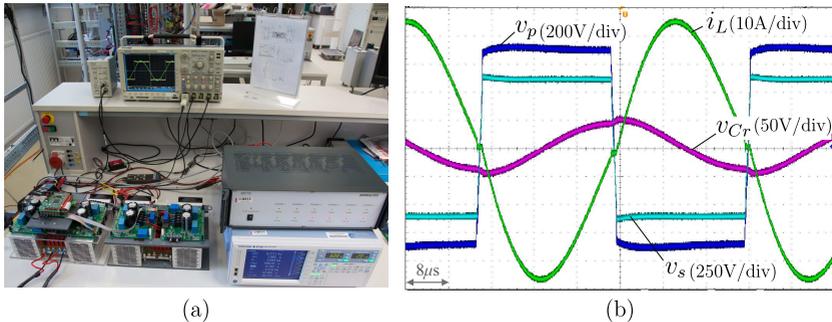
The experimental results were obtained for the converter operating in steady-state, in which the converter was tested with nominal load and voltage. The main waveforms were saved and the thermal behavior of the main components was evaluated by a temperature measurement system. In this test, the converter's performance is analyzed, where the efficiency and losses distribution are discussed.

The main waveforms are shown in Fig. 3.14. In Fig. 3.14 (b), the primary side voltage ( $v_p$ ), the voltage over the resonant capacitor ( $v_{Cr}$ ) and the tank circuit current ( $i_{Lr}$ ) are presented. Fig. 3.15 (a) shows the current and voltage on the primary side semiconductor ( $s_1$ ), where soft-switching operation is verified. As expected, the primary side semiconductors turn on in ZVS and turn off in ZCS. The commutation detail is also depicted in Fig. 3.15 (a). Similarly, the current and voltage on the secondary side diode ( $D_1$ ) are presented in Fig. 3.15 (b), where ZCS operation during turn-on and turn-off is observed. Therefore, these results confirmed that the switching losses can be completely neglected during the design of the converter.

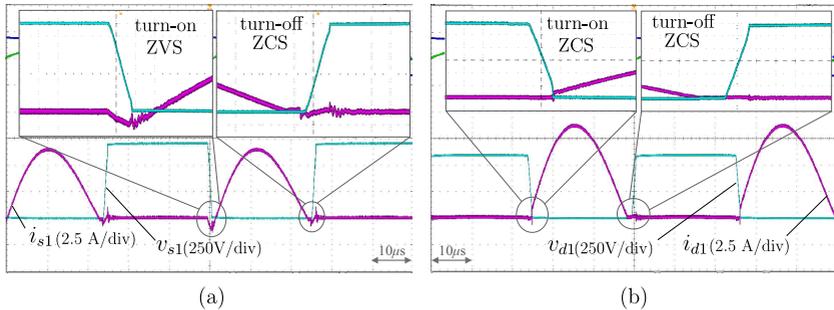
The temperatures of the transformer, as well as the temperature of the semiconductors on the primary side and secondary side are depicted in Fig. 3.16, when the converter is operating at nominal load. As can be noticed, the hotspot on the transformer has an temperature of  $89^{\circ}\text{C}$ , which is below the maximum of  $100^{\circ}\text{C}$  defined by the design.

Finally, the efficiency curve in function of the output power is shown in Fig. 3.17, while the losses distribution is presented in Fig. 3.18. The efficiency curve was obtained experimentally using the high performance power analyzer WT1800 from *Yokogawa* (basic power accuracy of 0.02%). As can be seen, the converter has achieved a peak efficiency of 98.61% at a power level of around 4 kW, while at nominal load the converter has achieved around 98.1% of efficiency. These results confirmed the optimum design of the converter, as well as the high potentiality of the SiC technology in this application.

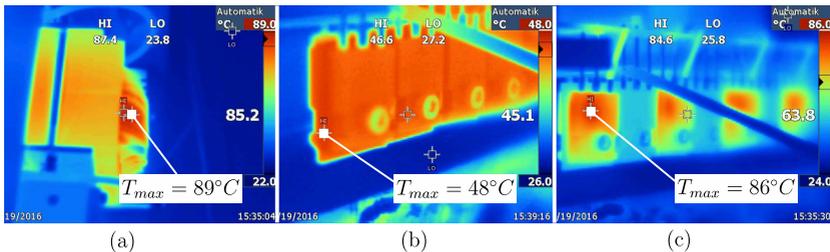
Evaluating the losses distribution depicted in Fig. 3.18, the transformer is responsible for most of the losses, with 39% of the total power dissipated by the converter. Furthermore, the conduction losses of the secondary side semiconductor (around 34% of the total losses) are higher than the primary side ones, that are responsible for 24% of the total power dissipated by the converter. This effect is also noticed in Fig. 3.16, in which higher temperatures are observed in the secondary side devices (around  $86^{\circ}\text{C}$ , see Fig. 3.16(c)) with respected to the primary side semiconductors (see Fig. 3.16 (a)). In spite of having higher rms current, the primary side semiconductor dissipate less power, when



**Fig. 3.14:** Experimental results obtained in steady-state: (a) primary side voltage ( $v_p$ ), voltage over the resonant capacitor ( $v_{Cr}$ ) and tank circuit current ( $i_{Lr}$ ).



**Fig. 3.15:** Commutation of semiconductors: (a) current and voltage on the primary side semiconductor ( $s_1$ ), (c) current and voltage on the secondary side semiconductor ( $d_1$ ).



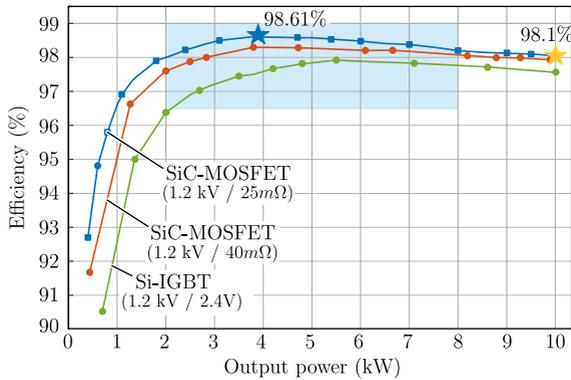
**Fig. 3.16:** Thermal behavior of the main components of the converter operating under nominal condition: (a) HFT (hotspot:  $85.2^\circ\text{C}$ ), (b) primary side semiconductor (SiC-MOSFETs) (hotspot:  $48^\circ\text{C}$ ), (c) secondary side semiconductor (SiC-diodes) (hotspot:  $86^\circ\text{C}$ ).

compared to the secondary side semiconductor. It is explained by the fact that the SiC-MOSFETs presents a very low  $R_{DS(on)}$ , contributing significantly to the conduction losses reduction.

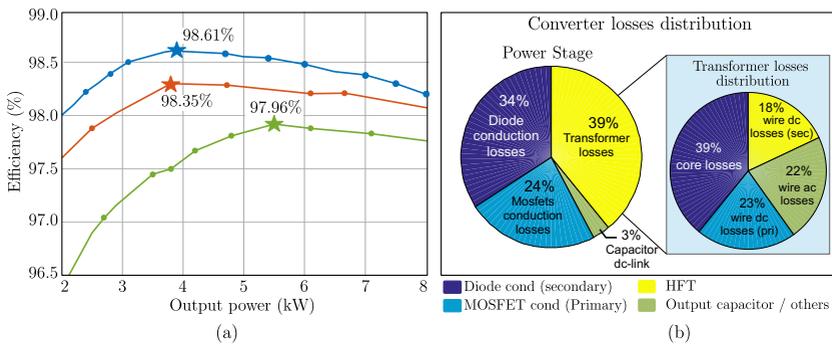
These results demonstrate the high performance of the SRC and validate the optimum design procedure presented in this section.

### 3.4 Fault Tolerance Capability

Reliability and efficiency are subjects that have been intensively mentioned in this chapter, because of their importance in the DC-DC stage.



**Fig. 3.17:** Efficiency curve of the SRC as a function of the output power obtained experimentally, considering the different semiconductors.



**Fig. 3.18:** (a) Detail of the efficiency curve, highlighting the maximum efficiency point for each employed semiconductor. (b) Losses distribution on the main components of the converter and also the losses distribution on the HFT.

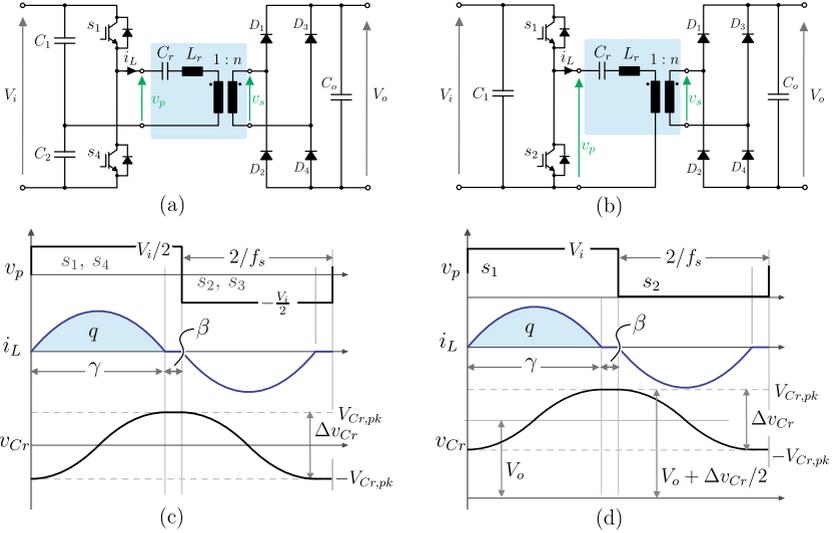
From the reliability assessment of the SRC discussed in Section 3.2, the primary side semiconductor and the resonant capacitor were listed as the most susceptible devices to fail. Therefore, three important issues are highlighted: efficiency of the SRC, lifetime of the resonant capacitor and failure on the primary side semiconductor. In the previous section, a design methodology that optimizes the efficiency of the converter and extends the lifetime of the resonant capacitor was presented

and demonstrated experimentally. This means that two out of the three issues mentioned before were approached in the last section. Thus, only the failure on the primary side semiconductor needs to be addressed, in order to achieve a fully reliable solution. The most suitable method to avoid the interruption of the converter operation due to the failure on the semiconductor is using fault tolerance approach.

The fault tolerance feature contributes unquestionably to increase the availability of system and several fault tolerance methods have been proposed in literature [114, 125–127]. Most of these methods includes a significant amount of extra hardware (such as semiconductors/leg redundancy [114, 125] or series connection of fuses/switches to isolate the fault [125–127]), increasing the cost and compromising the efficiency of the system. As an alternative to the existing methods, this work proposes a fault tolerance solution with minimum of additional hardware and no deterioration on the efficiency of the SRC converter. It uses the advantage of inherent fault tolerant capability of this topology. The idea behind the proposed fault tolerant approach is to reconfigure the Full-Bridge SRC (FB-SRC), depicted in Fig. 3.1, in a Half-Bridge SRC (HB-SRC). Then, for a comprehensive understanding of the proposed method, the HB-SRC is analyzed. Additionally, the unidirectional topology, in which switches on the secondary side are replaced by diodes, is considered at the first moment of the analysis.

### 3.4.1 Analysis of the HB-SRC

The SRC can be also implemented using the Half-Bridge topology (HB-SRC) and two variant circuits of the HB-SRC is shown in Fig. 3.19 (a) and (b). To simplify the analysis, the symmetric HB-SRC shown in Fig. 3.19 (a) will be referred as Sym-HB-SRC, while the asymmetric one will be named as Asym-HB-SRC. They operate similarly to the FB-SRC and the equations (3.18) to (3.22) are still valid. The difference lies on the voltage  $v_p$  synthesized by the primary switches. This can be observed on the waveforms presented in Fig. 3.19 (c) and (d), for the Sym-HB-SRC and Asym-HB-SRC, respectively. As can be noticed, the Sym-HB-SRC creates a rectangular wave voltage  $v_p$  with negative and positive values of  $-V_i/2$  and  $V_i/2$ , whereas the Asym-HB-SRC generates zero and positive values ( $0, V_i$ ). In both cases, the effective  $v_p$  voltage is half of that one generated by the FB-SRC. As a result, the rectified output voltage on the secondary side is given by (3.47),



**Fig. 3.19:** Topology of the Half-Bridge SRC (HB-SRC) and the main waveforms: (a) topology of the symmetric HB-SRC (Sym-HB-SRC), (b) topology of the asymmetric HB-SRC (Asym-HB-SRC), (c) waveforms of the Sym-HB-SRC and (d) waveforms of the Asym-HB-SRC.

which is also half of the output voltage provided by the FB-SRC (see eq. (3.24)), assuming the same parameters ( $V_i$  and  $n$ ). In addition, the voltage  $v_p$  generated by the Asym-HB-SRC has a DC value, which is filtered by the resonant capacitor. It means that this capacitor has an offset given by  $V_i$ , as depicted in Fig. 3.19 (d), and then its peak voltage is determined by (3.46).

$$V_{Cp} = \frac{I_i}{8f_s C_r} + V_i \quad (3.46)$$

$$V_o = \frac{nV_i}{2} \quad (3.47)$$

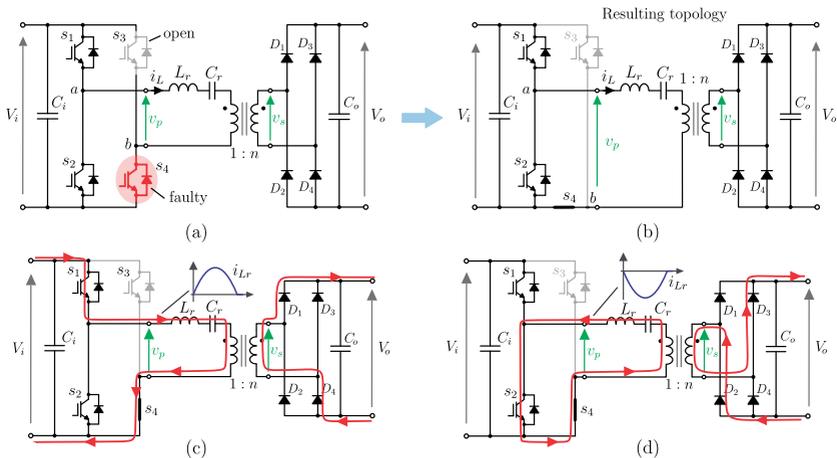
### 3.4.2 Proposed Fault Tolerant Converter

The proposed fault tolerance approach can be used for OC and SC failure and it was previously described in [113]. As the SC failure type

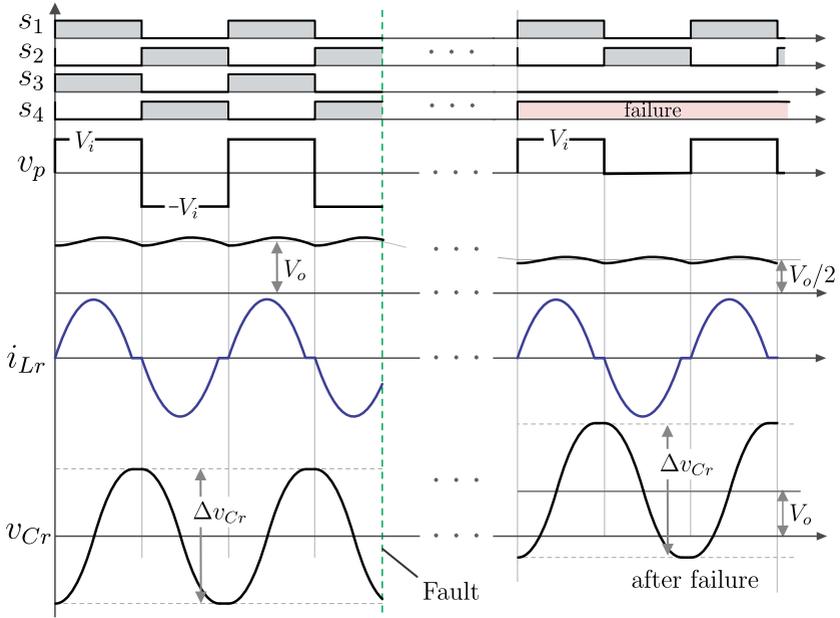
is most likely to happen, then the reconfiguration scheme is described considering the SC fault case.

The proposed reconfiguration scheme for the SRC consists in configuring the FB-SRC in a HB-SRC after the fault, i.e. SC of a semiconductor. Initially, as an example, it is assumed that the switch  $s_4$  is damaged in SC, as seen Fig. 3.20 (a). Hence the switch  $s_3$  must remain open, avoiding short-circuit of the input voltage source. Since the switch  $s_4$  is short-circuited, the point  $b$ , highlighted in Fig. 3.20 (a), is directly connected to the primary side ground and the damaged device is used as a circuit path, resulting in the circuit shown in Fig. 3.20 (b), which is essentially the Asym-HB-SRC. Meanwhile, the healthy leg (composed of  $s_1$  and  $s_2$ ) operates normally. Fig. 3.20 (c) and (d) show the operation states of the SRC after the fault, i.e. after the reconfiguration, where it can be seen the damaged switch  $s_4$  being used as a circuit path. Fig. 3.21 shows the main waveforms of the FB-SRC when a fault happens.

As the HB-SRC provides only half of the output voltage compared to the FB-SRC, the output voltage of the converter after the fault will



**Fig. 3.20:** (a) FB-SRC under faulty condition: SC failure on the semiconductor  $s_4$ , (b) resulting topology after the reconfiguration of the FB-SRC. Operation of the FB-SRC as a Asym-SRC after the reconfiguration. States operation of the SRC after the fault: (a) positive  $i_{Lr}$  current (first state), (b) negative  $i_{Lr}$  current (second state).



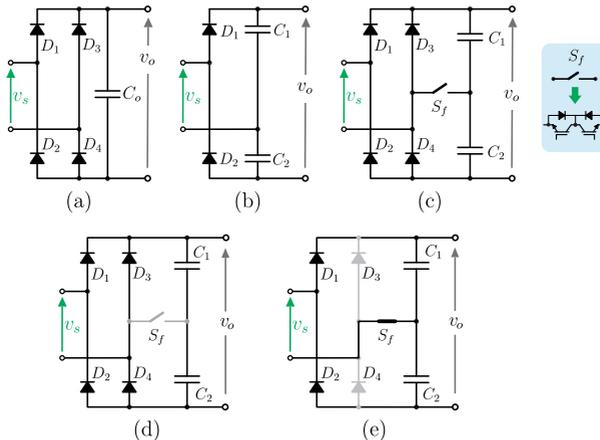
**Fig. 3.21:** Main waveforms (voltages and currents) of the FB-SRC when a fault happens. The waveforms before and after the fault are presented.

be half of its original value, as illustrated in Fig. 3.21, which is not desired. Thereafter, to overcome this problem and keep the output voltage constant after the fault, a modification to the circuit of the secondary side rectifier is proposed and a novel re-configurable rectifier is obtained.

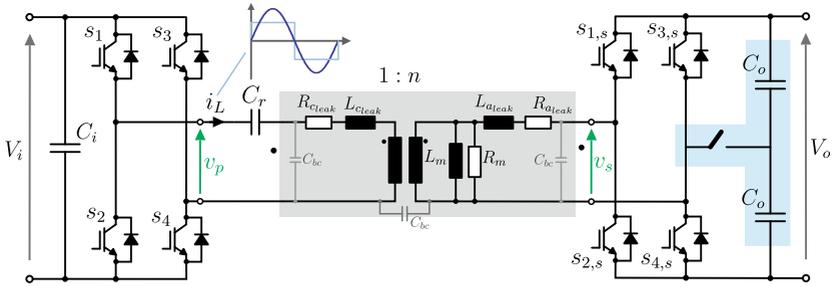
Fig. 3.22 (a) shows the topology of the standard Full-Bridge rectifier (FBR), which is the most used on the secondary side of the SRC [49, 113]. In this configuration, the output is given by:  $v_o = v_{s_{pk}}$ . Fig. 3.22 (b) shows the topology of the voltage-doubler rectifier (VDR). In this configuration, the rectified output voltage is given by:  $v_o = 2v_{s_{pk}}$ . Thus, in order to use the voltage doubler characteristic of the VDR in case of fault of the SRC, keeping its output voltage constant, a re-configurable rectifier circuit presented in Fig. 3.22 (c) is proposed. The proposed rectifier has two split capacitors and an additional switch ( $S_f$ ) that allows to connect one terminal of the secondary winding of the HFT directly to the middle point of the capacitors, becoming a VDR.

The operation in normal and fault conditions is depicted in Fig. 3.22 (d) and (e), respectively. In normal operation, the switch  $S_f$  is open, and the rectifier operates as a standard FBR. In fault case, the switch  $S_f$  is on, and then the leg composed of the diodes  $D_3$  and  $D_4$  is bypassed. The bottom terminal of the secondary winding is connected to the middle point of the capacitors  $C_1$  and  $C_2$ , as depicted in Fig. 3.22 (e). Therefore, the circuit operates as a VDR and the output voltage rises, reaching twice its previous value. Finally, Fig. 3.23 shows the complete circuit of the proposed fault-tolerant series resonant DC-DC converter (FT-SRC).

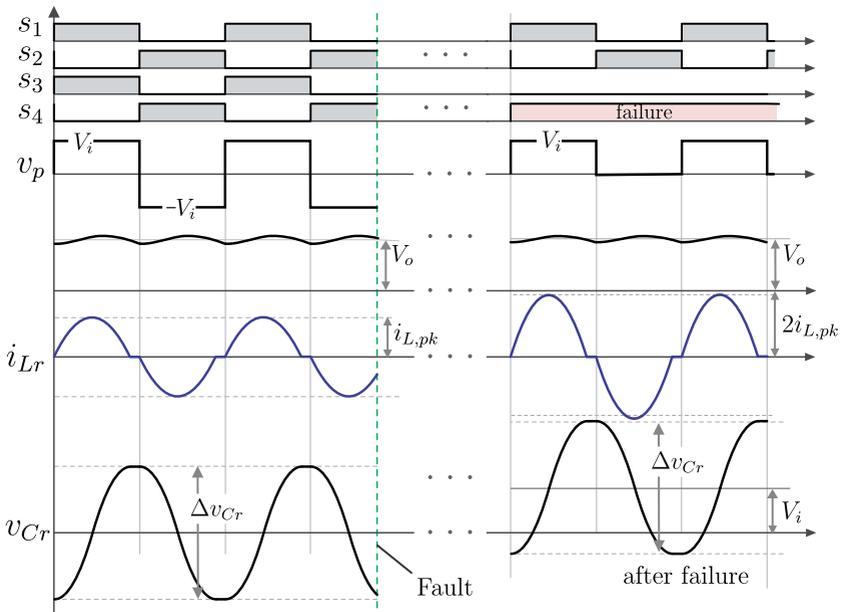
The main waveforms for the proposed FT-SRC before and after a failure are depicted in Fig. 3.24. As can be observed, before the failure (normal operation) the voltages  $v_p$  and  $v_{Cr}$  have an average value equal to zero and the output voltage is given by  $V_o$ . After the failure in the switch  $s_4$  for example, there is the reconfiguration, in which the FB-SRC operates as a Asym-HB-SRC and the switch  $S_f$  is then activated, so that the output stage can operate as the VDR. Consequently, the output voltage will remain at the same value, as desired. The effect of the reconfiguration is only observed on the voltage  $v_{Cr}$ , that has an



**Fig. 3.22:** Possible rectifier topologies and proposed topology: (a) full-bridge rectifier (FBR), (b) voltage-doubler rectifier (VDR), and (c) proposed reconfigurable rectifier. Operation of the proposed rectifier: (d) operation as an FBR and (e) operation as a VDR.



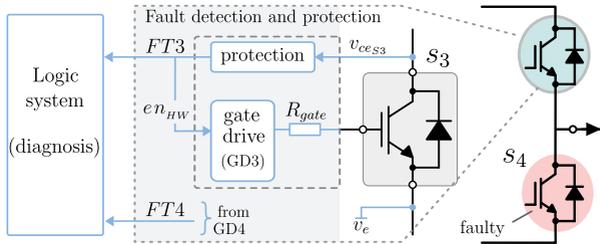
**Fig. 3.23:** Topology of proposed fault-tolerant SRC.



**Fig. 3.24:** Main waveforms (voltages and currents) of the proposed FT-SRC when a fault happens. The waveforms before and after the fault are presented.

expected offset of  $V_i$ , and on the current  $i_{Lr}$ , that must be twice the previous value to process the same amount of power than before.

To detect the fault and identify the faulty semiconductor, a fault



**Fig. 3.25:** Simplified gate-drive block diagram interfaced with the fault detection algorithm.

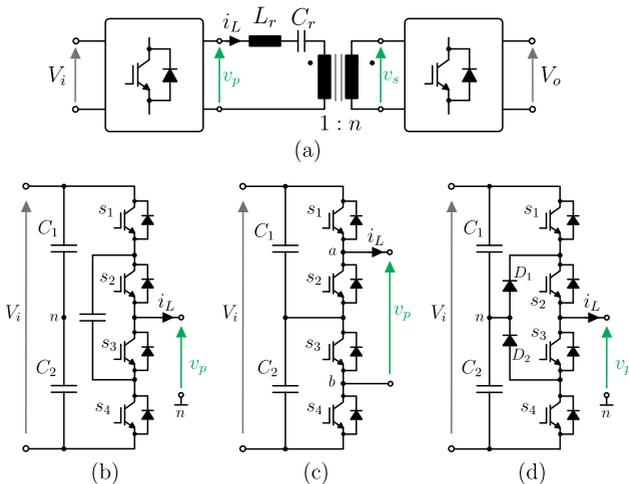
detection and diagnosis method must be implemented. The goal of this section is to propose the reconfiguration scheme for the SRC converter and to propose the FT-SRC, as already mentioned. Hence existing methods can be used to identify the failure in the proposed converter. It is well-known that the IGBT devices can withstand abnormal current during a short period of time, usually around  $10 \mu s$  [118], which is considerably large. Among the various methods that can be applied to this converter, *de-saturation detection method* [128], *protection by gate voltage limiting*, *current mirror method* [128] and *gate voltage sensing* [118] are very suitable. All these methods require the sensing of the device collector voltage and/or current and they are simple to be implemented. Fig. 3.25 shows the protection method based on the *de-saturation detection* interfaced with the logic system used to diagnosis the faulty leg. In case of fault of the switch  $s_4$ , the collector voltage of  $s_3$  ( $v_{ce_{s3}}$ ) increases from the low saturation value to the DC link voltage, while the gate signal is still high. In that case, the protection circuit disables the gate-drive (through the signal  $en_{HW}$ ) and sends a signal ( $FT3$ ) to the diagnosis system, to identify the faulty device. This method needs around  $1\mu s$  to  $5\mu s$  to detect the fault and to react [118], protecting the device. Since the IGBT can withstand a short-circuit current for  $10\mu s$ , the detection method is very suitable for this application.

In case of OC fault, the proposed solution is still valid. Instead of opening the healthy IGBT of the faulty leg, the logic system must close this IGBT. As an example, in case of OC fault of the switch  $s_4$ , the switch  $s_3$  must remain closed, in order to be used as a path of the circuit. Therefore, to extend the proposed solution for OC fault actuation, only the logic system must be adjusted.

### 3.4.3 Generalization of the Fault Tolerance Approach

Besides the FB and HB topologies, the SRC can be conceived using multilevel topologies as the active bridge. More specifically, the multilevel topologies suitable to implement the SRC are: 3-level (3L), Flying Capacitor (FC) and Neutral Point Clamped (NPC), as illustrated in Fig. 3.26. Thus, the proposed fault tolerance approach is extended to the SRC based on multilevel topologies, resulting then in a family of fault tolerant SRC converters. The generated converters were introduced in [129] and they are analyzed as follow.

As a matter of simplification, the SRC based on the 3L, FC and NPC topologies will be named as 3L-SRC, FC-SRC and NPC-SRC, respectively. Despite the capability of the multilevel topologies to operate with 3 level modulation (creating a  $v_p$  voltage with 3 levels), the 2 level modulation is more beneficial for the multilevel SRC, because it combines the advantages of the SRC converter (high efficiency, low EMI emission, etc), with the advantage of the multilevel structure of reducing the voltage effort across the semiconductors. Therefore, the 2



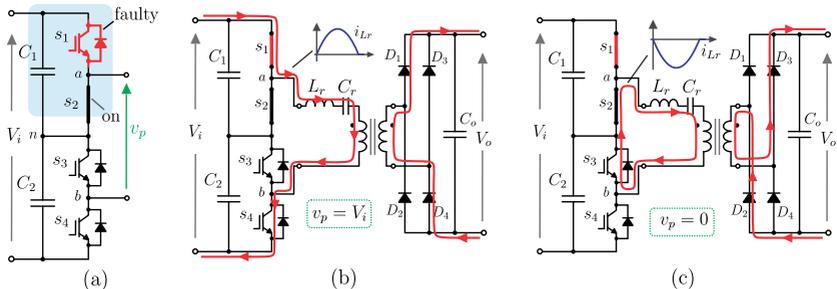
**Fig. 3.26:** (a) Generic topology of the SRC and the possible multilevel topologies used to implement the active bridges of the series-resonant converter: (a) flying-capacitor (FC-SRC), (b) 3-level topology (3L-SRC) and (c) neutral-point-clamped (NPC-SRC).

level modulation is used in the multilevel SRC. These converters present the same voltage and current waveforms of the HB-SRC, when the 2 level modulation is used, because the HB configuration of the multilevel topologies. Note that the FC-SRC and NPC-SRC create an rectangular waveform voltage  $v_p$  with positive and negative values ( $-V_i/2$  and  $V_i/2$ , similarly to the Sym-HB-SRC), while the 3L-SRC generates a rectangular waveform voltage  $v_p$  with positive and zero levels ( $-V_i/2$  and  $V_i/2$ , similarly to the Asym-HB-SRC).

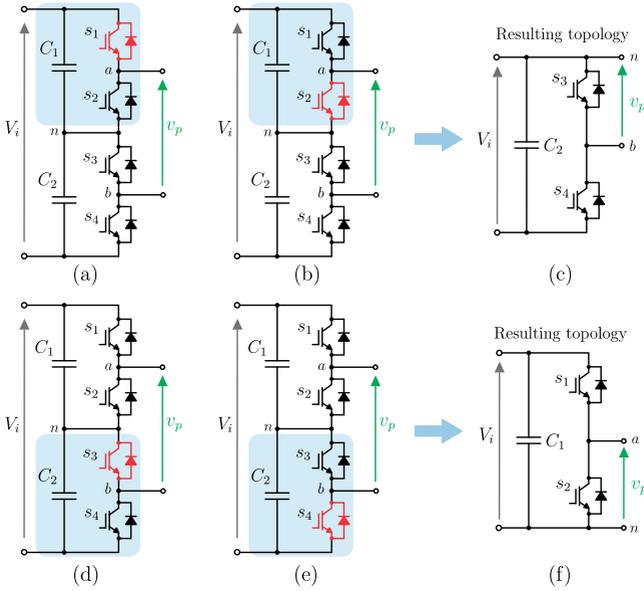
### Analysis of the Fault Tolerant 3L-SRC

As mentioned before, the proposed fault tolerance approach consists in reconfigure the original SRC converter in a HB-SRC, when a fault happens. This concept is then applied for the multilevel SRC and it is firstly explained for the 3L-SRC.

Considering a SC failure on the switch  $s_1$  of the 3L-SRC, as an example. The switch  $s_2$  should stay permanently on, as shown in Fig. 3.27 (a), discharging completely the capacitor  $C_1$ . Then, the part of the circuit composed by  $C_1$ ,  $s_1$  and  $s_2$  and highlighted in Fig. 3.28 (a) is completely by-passed, resulting in the circuit shown in Fig. 3.28 (c). The healthy leg composed of  $s_3$  and  $s_4$  operates normally. As observed, the resulting circuit after the fault (see Fig. 3.28 (c)) is the Asym-HB-SRC topology shown in Fig. 3.19 (b), but with transformer connected to the positive terminal of the input source  $V_i$ , instead of the ground.



**Fig. 3.27:** (a) 3L-SRC under faulty condition: SC failure on the semiconductor  $s_1$ . Operation of the 3L-SRC as a HB-SRC after the reconfiguration and the operation states: (b) positive  $i_{Lr}$  current (first state), (b) negative  $i_{Lr}$  current (second state).



**Fig. 3.28:** Proposed reconfiguration scheme for the 3L-SRC for a faulty case in every device and the resulting circuit after the reconfiguration: (a) fault in  $s_1$ , (b) fault in  $s_2$ , (c) resulting circuit (Asym-HB-SRC) after the reconfiguration in case of fault in  $s_1$  or  $s_2$ , (d) fault in  $s_3$ , (e) fault in  $s_4$ , (f) resulting circuit (Asym-HB-SRC) after the reconfiguration in case of fault  $s_3$  or  $s_4$ .

**Tab. 3.9:** Switching states for the reconfiguration scheme for the 3L-SRC

Faulty Device	$s_1$	$s_2$	$s_3$	$s_4$
$s_1$	SC	ON	switching	switching
$s_2$	ON	SC	switching	switching
$s_3$	switching	switching	SC	ON
$s_4$	switching	switching	ON	SC

The modified connection has no influence on the converter operation.

It is important to note that during the reconfiguration of the 3L-SRC, the capacitor  $C_1$  was discharged by the short-circuit of the switches  $s_1$  and  $s_2$  (see Fig. 3.27 (b)). It means that the short-circuit current flows through the healthy switch  $s_2$ , which can damage this switch, if the magnitude of the short-circuit current is too high. To avoid large short-circuit current and guarantee the safe operation of the proposed method, the energy stored on the capacitor  $C_1$  should be very small. This is an important requirement for the application of the proposed fault tolerant.

Fig. 3.27 (b) and (c) shows the operation states of the 3L-SRC after the reconfiguration. The procedure of reconfiguring the 3L-SRC in case of fault in other switches is presented in Fig. 3.28. Table 3.9 describes the final state for every remaining healthy switch after the failure on each device.

### Analysis of the Fault Tolerant FC-SRC

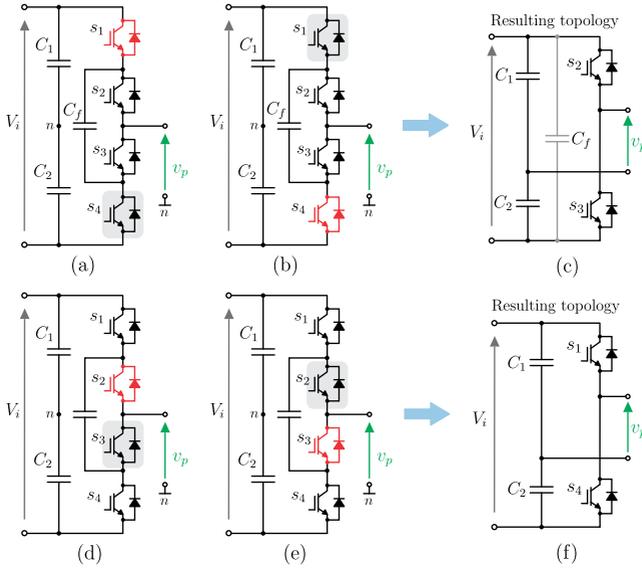
Similarly to the 3L-SRC, the FC-SRC can also take advantage of the proposed fault tolerance method. The reconfiguration procedure is presented in Fig. 3.29, as well as the resulting circuit after the reconfiguration, considering the faulty case in each switch. Considering a faulty on the switch  $s_1$  as an example, the switch  $s_4$  should remaining permanently on for the reconfiguration process. Then, the capacitor  $C_f$  will be charged by the short-circuit current that flows through the components  $C_f$ ,  $s_1$  and  $s_4$ . This process ends when the capacitor  $C_f$  is fully charged with the DC link voltage  $V_i$  (operating in parallel with the array composed by  $C_1$  and  $C_2$ ). To avoid high current<sup>4</sup>, the energy transferred to the capacitor  $C_f$  during the reconfiguration process should be small. In other words, the capacitor  $C_f$  should not be very large.

The switches  $s_2$  and  $s_3$  operate normally and the resulting circuit is shown in Fig. 3.29 (c).

Differently from the FB-SRC and 3L-SRC, the resulting circuit after the reconfiguration of the FC-SRC is the Sym-HB-SRC, shown in Fig. 3.19 (a). As a consequence, the resonant capacitor does not operate

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<sup>4</sup>High currents might cause damage to the healthy devices (like  $s_4$ ), if the reconfiguration process is too long and if the device does not have enough power dissipation capability to keep the temperature within the limits. To avoid that, the energy transferred from the input source to the capacitor  $C_f$  should be small.



**Fig. 3.29:** Proposed reconfiguration scheme for the FC-SRC for a faulty case in every device and the resulting circuit after the reconfiguration: (a) fault in  $s_1$ , (b) fault in  $s_2$ , (c) resulting circuit (Sym-HB-SRC) after the reconfiguration in case of fault in  $s_1$  or  $s_2$ , (d) fault in  $s_3$ , (e) fault in  $s_4$ , (f) resulting circuit (Sym-HB-SRC) after the reconfiguration in case of fault  $s_3$  or  $s_4$ .

**Tab. 3.10:** Switching states for the reconfiguration scheme for the FC-SRC

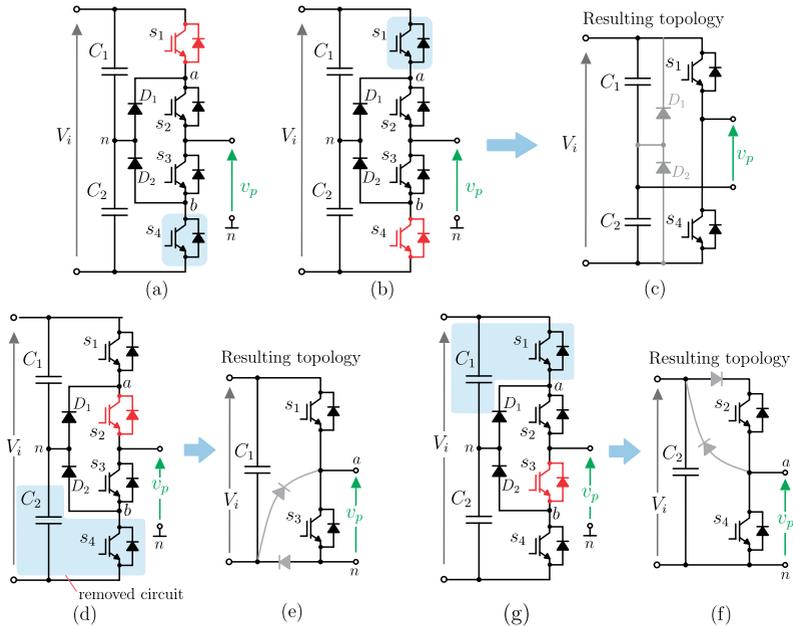
Faulty Device	$s_1$	$s_2$	$s_3$	$s_4$
$s_1$	SC	switching	switching	ON
$s_2$	switching	SC	ON	switching
$s_3$	switching	ON	SC	switching
$s_4$	ON	switching	switching	SC

with the DC offset of  $V_i$  after the fault. Thus, in contrast to the FB-SRC and 3L-SRC, the resonant capacitor of the FC-SRC does not suffer any impact after the reconfiguration.

Table 3.10 describes the final state of each remaining healthy switch after the failure on each device.

### Analysis of the Fault Tolerant NPC-SRC

Finally, the reconfiguration scheme of the NPC-SRC is described. For this converter, there are two possible faults that will result in two different topologies after the reconfiguration: the first case is for a fault in the outer semiconductors, i.e.  $s_1$  and  $s_4$ , whereas the second case is



**Fig. 3.30:** Proposed reconfiguration scheme for the NPC-SRC for a faulty case in every device and the resulting circuit after the reconfiguration: (a) fault in  $s_1$ , (b) fault in  $s_2$ , (c) resulting circuit (Sym-HB-SRC) after the reconfiguration in case of fault in  $s_1$  or  $s_2$ , (d) fault in  $s_3$ , (b) fault in  $s_4$ , (c) resulting circuit (Asym-SRC) after the reconfiguration in case of fault  $s_3$  or  $s_4$ .

**Tab. 3.11:** Switching states for the reconfiguration scheme for the NPC SRC

Faulty Device	$s_1$	$s_2$	$s_3$	$s_4$
$s_1$	SC	switching	switching	OFF
$s_2$	switching	SC	switching	OFF
$s_3$	OFF	switching	SC	switching
$s_4$	OFF	switching	switching	SC

for inner semiconductors  $s_2$  and  $s_3$ . The reconfiguration procedure of the NPC-SRC for both cases are presented in Fig. 3.30, as well as the resulting circuit after the reconfiguration.

Analyzing the first case, a SC fault on the switch  $s_1$  is assumed as an example. Then, the switch  $s_4$  must remain permanently on for the reconfiguration. Consequently, the point  $a$ , highlighted in Fig. 3.30 (a), is connected to the positive terminal of the input DC link  $V_i$ , whereas the point  $b$  (see Fig. 3.30) is connected to the ground, bypassing the clamp diodes  $D_1$  and  $D_2$ . It results in the circuit shown in Fig. 3.30 (c). Meanwhile, the healthy switches  $s_2$  and  $s_3$  operate normally. Similarly to the FC-SRC, the resulting circuit for the first fault case of the NPC-SRC is a Sym-HB-SRC.

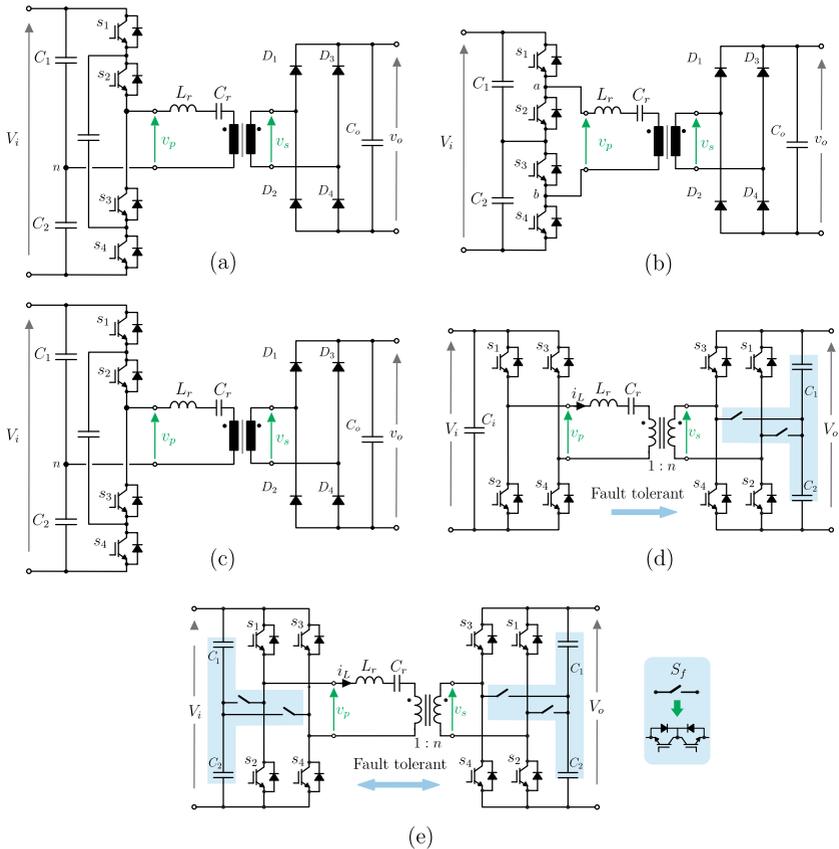
Evaluating the second case, a fault on the switch  $s_2$  is assumed and, as part of the reconfiguration process, the switch  $s_4$  must remain open. Therefore, the part of the circuit composed by the capacitor  $C_2$  and  $s_4$  is removed from the entire network, resulting in the topology shown in Fig. 3.30 (e). Thus, differently from the previous case, the resulting circuit after the reconfiguration is the Asym-HB-SRC. Table 3.11 describes the final state for every remaining healthy switch after the reconfiguration, considering the failure on each device.

### 3.4.4 Fault Tolerant Multilevel SRC and Bidirectional SRC

Considering the reconfiguration process for the multilevel SRC explained in the previous section, a family of fault tolerant multilevel SRC topologies is generated and presented in Fig. 3.31. Differently from the FT-FB-SRC, the fault tolerant multilevel SRC does not require the reconfigurable rectifier in its output stage. Actually, the effective voltage

$v_p$  generated by the multilevel SRC is  $V_i/2$  before and after the fault. As this voltage does not change during the reconfiguration process, the output voltage remains the same after the fault, avoiding the need of the reconfigurable rectifier.

The fault-tolerance capability of the SRC can be easily extended to the bidirectional Full-Bridge topology [130]. In the topology de-



**Fig. 3.31:** Proposed fault-tolerant series resonant DC-DC converter based on the multilevel topologies: (a) fault-tolerant FC-SRC (FT-FC-SRC), (b) fault-tolerant 3L-SRC (FT-3L-SRC), (c) fault-tolerant NPC-SRC (FT-NPC-SRC), (d) and (e) bidirectional FT-FB-SRC.

icted in Fig. 3.31 (d) and (e), the diodes on the secondary side are replaced by active switches, in order to obtain an active bridge. Therefore, the operation is very similar to the unidirectional version, but active switches are used instead of diodes. Similarly to the unidirectional version, in faulty case, the secondary bridge must be reconfigured in a voltage-doubler bridge and, therefore, the reconfigurable bridge is obtained with additional switches as well. Fig. 3.31 (d) shows the proposed fault-tolerant bidirectional series resonant DC-DC converter. Nonetheless, the fault-tolerance capability is obtained only when the power flows from the primary to the secondary side (i.e. from  $V_i$  to  $V_o$ ), where only the secondary bridge is able to reconfigure in a voltage doubler bridge. To obtain a fully fault tolerant converter, either the primary and secondary bridges must be reconfigurable. Therefore, the completely fault-tolerant SRC topology is presented in Fig. 3.31 (e). Although more semiconductors are used, the efficiency is not deteriorated, since the additional switches are only activated in faulty case. Besides that, with the proposed topology, the availability of the topology is highly increased.

### 3.4.5 Evaluation of the Proposed Fault Tolerance Approach

The proposed fault tolerance approach is very advantageous for the SRC, because it is very simple to be implemented and requires few extra components, differently for the existing methods. Furthermore, the technique does not deteriorate the efficiency of the converter, once the extra switch is inserted on the circuit, only in faulty case. On the other hand, the capacitor voltage and the semiconductor's voltage or current might be penalized after the reconfiguration, according to the topology.

To verify the performance of the proposed approach, the voltage and current stresses on the main components before and after the fault for each topology are presented in Table 3.12. In this table, it is considered the same operation condition (in terms of power and voltage) before and after the failure.

For the FT-FB-SRC, the voltage effort on the semiconductor remains the same after the fault, but the current doubles, if the output power remains constant. Hence, the converter must double the current to keep the same power level. Moreover, the voltage over the resonant

capacitor ( $v_{Cr}$ ) will present a DC component, increasing its peak value, while preserving the voltage ripple, as described before. Despite the current stress increases after the fault of the FT-FB-SRC, it is not critical, because the converter does not need to be necessarily overdesigned. The semiconductors and cooling system of the converter are normally designed for the nominal power, but the converter operates most of the time at partial load, implying in a margin to increase the current involved on the power conversion. Additionally, the output power can be limited, avoiding overdesign and overheating of the components.

For the multilevel topologies, the current effort on the semiconductor remains the same after the fault, but the voltage over the devices will double. Consequently, semiconductors must be selected to support twice the DC link voltage. This case is much more critical than the FT-FB-SRC case, because the cost and performance of the semiconductors are directly related to their voltage rating. Higher voltage rating for the semiconductors means higher cost and lower performance<sup>5</sup>.

In summary, to use the proposed fault tolerant technique in the multilevel SRC, semiconductors rated for higher voltage (twice the DC link voltage, instead of the DC link voltage) is required, penalizing the cost and performance of the converter.

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<sup>5</sup>Lower performance means high emitter-collector voltage during on-state ( $V_{CE(ON)}$ ) and higher switching energy

**Tab. 3.12:** Stresses on the main components of the proposed fault tolerant converters before and after the fault

Before the Failure					
Topology	FT-FB-SRC	FT-3L-SRC	FT-FC-SRC	FT-NPC-SRC	FT-NPC-SRC
$V_{S(max)}$	$V_i$	$V_i/2$	$V_i/2$	$V_i/2$	$V_i/2$
$I_{S(rms)}$	$I_{L(pk)}/2$				
$I_{Lr(rms)}$	$I_{L(pk)}/\sqrt{2}$				
$V_{Cr(pk)}$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r} + V_i$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r}$
After the Failure					
Topology	FT-FB-SRC	FT-3L-SRC	FT-FC-SRC	FT-NPC-SRC	FT-NPC-SRC
$V_{S(max)}$	$V_i$	$V_i$	$V_i$	$V_i$	$V_i$
$I_{S(rms)}$	$I_{L(pk)}$	$I_{L(pk)}/2$			
$I_{Lr(rms)}$	$I_{L(pk)}/2$	$I_{L(pk)}/\sqrt{2}$			
$V_{Cr(pk)}$	$\frac{I_o}{8nf_sC_r} + V_i$	$\frac{I_o}{8nf_sC_r} + V_i$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r} + V_i$
Resulting	Assym-HB-SRC		Ssym-HB-SRC		Assym-HB-SRC

### 3.4.6 Simulation and Experimental Validation of the Fault Tolerance Approach

To validate the proposed fault tolerance technique, the fault tolerant SRC converters were evaluated through numerical simulation and experimental tests. Simulation results for the fault tolerant multilevel converters are presented next, as well as experimental results for the FT-FB-SRC topology.

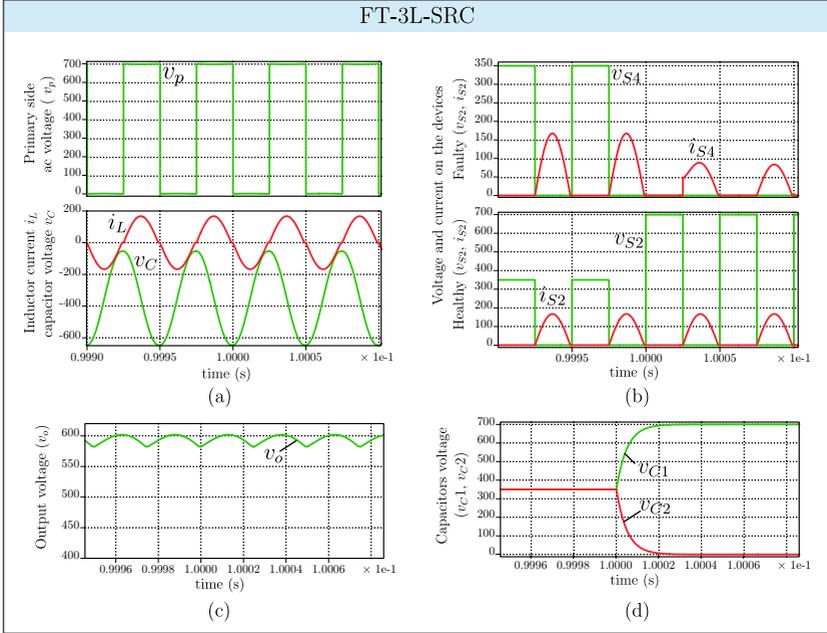
► **Simulation Results:**

To confirm the proposed fault tolerance technique, every multilevel topology was simulated using the MATLAB/Simulink and the PLECS toolbox, considering the parameters presented in Table 3.13. For each case, a fault on the switch  $s_4$  was imposed at moment  $t = 0.1s$  and the main waveforms are summarized in Fig. 3.32 to Fig. 3.34. The results consist in voltage and current on the tank circuit elements [i.e. primary side voltage ( $v_p$ ), capacitor voltage ( $v_C$ ) and inductor current ( $i_L$ )], faulty ( $s_4$ ) and healthy devices ( $s_2$ ), as well as the voltage over the capacitors  $C_1$  ( $v_{C_1}$ ) and  $C_2$  ( $v_{C_2}$ ) and the output voltage ( $v_o$ ). As can be noticed, the tank circuit components ( $v_p$ ,  $v_C$  and  $i_L$ ), as well as the output voltage ( $v_o$ ) are not affected during the fault. On the other hand, the voltage over the semiconductors increases.

For the FT-3L-SRC, the capacitor  $C_2$  is fully discharged, while the capacitor  $C_1$  is charged with the total DC voltage after the fault, as explained before. It can be seen in Fig. 3.32 (d). Similar behavior is observed on the FT-FC-SRC, in which the capacitor  $C_f$  is charged with the full DC link voltage after the reconfiguration process. Thus, it operates in parallel with the array composed by  $C_1$  and  $C_2$ , as observed in Fig. 3.32 (h). For the FT-NPC-SRC, there is no variation on the

**Tab. 3.13:** Specification for the simulation of the multilevel SRC topologies

Power converter specification	
Input voltage	$V_i = 700$ V
Output voltage	$V_o = 600$ V
Nominal output power	$P_o = 10$ kW
Switching frequency	$f_s = 20$ kHz
Transformer turn ratio	$n = 1.45$

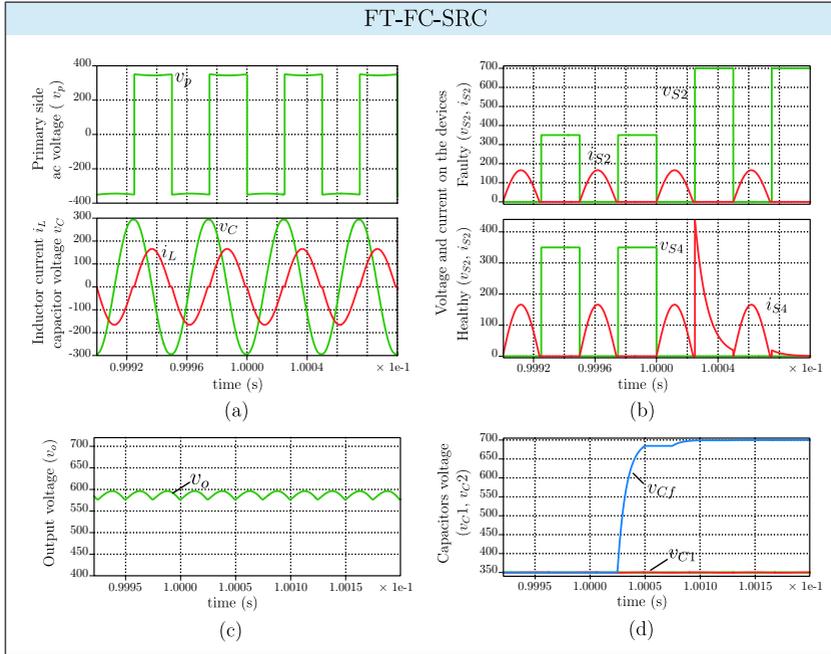


**Fig. 3.32:** Simulation results of the FT-3L-SRC topologies, when a fault occurs in the switch  $s_4$  at moment  $t = 0.1$ s. (a) primary ac side voltage ( $v_p$ ), resonant capacitor voltage ( $v_{cr}$ ), (b) voltage and current on the faulty switch ( $s_4$ ) and on the healthy device ( $s_2$ ), (c) output voltage ( $v_o$ ), (d) voltage over the dc-link capacitors ( $C_1$  and  $C_2$ ).

capacitors voltage, but only the primary side semiconductors. These results demonstrate the effectiveness of the proposed methods and the proposed fault tolerant topologies.

### ► Experimental Results:

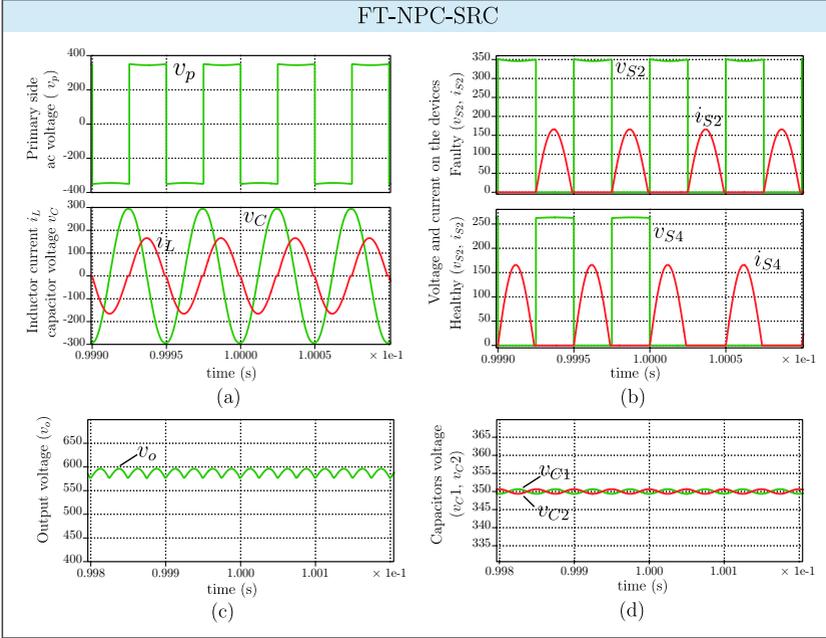
The fault tolerance technique is applied to the FB-SRC and it was tested in laboratory with the aim to evaluate the performance of proposed FT-FB-SRC and to demonstrate the theoretical analysis presented. In this circumstance, a short-circuit on the switch  $s_2$  was emulated. For these tests, the IGBT IHW40N120 (1200V/40A, from *Infineon Technologies AG*) were used on the primary and secondary sides. The results are presented for the converter operating in steady-state



**Fig. 3.33:** Simulation results of the FT-FC-SRC topologies for a fault in the switch  $s_4$  at moment  $t = 0.1s$ . (a) primary ac side voltage ( $v_p$ ), resonant capacitor voltage ( $v_{cr}$ ), (b) voltage and current on the faulty switch ( $s_4$ ) and on the healthy device ( $s_2$ ), (c) output voltage ( $v_o$ ), (d) voltage over the dc-link capacitors ( $C_1$  and  $C_2$ ).

(before and after the fault) and also dynamically during the fault and they are discussed herein. For safety reasons, the dynamic results were obtained for reduced input and output voltages.

Initially, the converter was tested considering only the reconfiguration scheme in the primary bridge, without the reconfigurable rectifier, with the aim to validate the fault tolerant approach and the reconfiguration methodology. The test was performed with input and output voltage of 200 V and 300 V, respectively, and the result for this condition is presented in Fig. 3.35 (a). In this figure, it is observed the dynamic response of the FB-SRC during the fault of the switch  $s_2$ , in which the converter remains operational after the fault, proving its inherent ability to handle the fault. As expected, after the fault, the

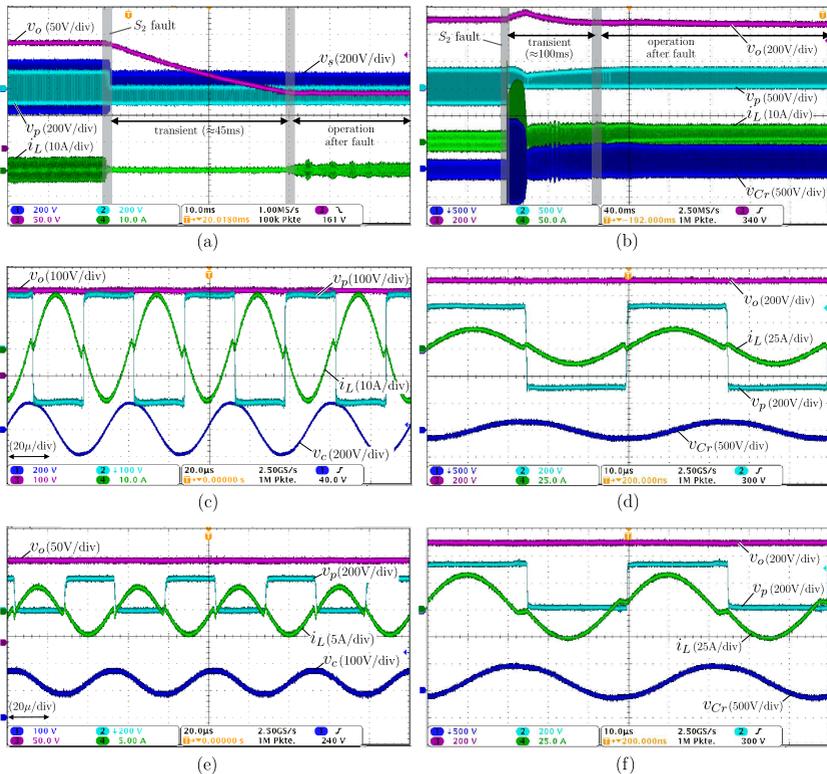


**Fig. 3.34:** Simulation results of the FT-NPC-SRC topologies for a fault in the switch  $s_4$  at moment  $t = 0.1s$ . (a) primary ac side voltage ( $v_p$ ), resonant capacitor voltage ( $v_{cr}$ ), (b) voltage and current on the faulty switch ( $s_4$ ) and on the healthy device ( $s_2$ ), (c) output voltage ( $v_o$ ), (d) voltage over the dc-link capacitors ( $C_1$  and  $C_2$ ).

output voltage drops to half of its value (from 300 V to 150 V) and the capacitor voltage has an offset of  $V_i$ . The inductor current is also reduced, because the test was performed with constant resistance as load.

Subsequently, the prototype was tested including the re-configurable rectifier, in order to validate the operation of the proposed FT-FB-SRC topology. For this test, it was considered an input voltage of 350 V and output voltage of 500 V, and the main results are presented in Fig. 3.35 (b), (d) and (f). The dynamic behavior during the fault on switch  $s_2$  is depicted in Fig. 3.35 (b), showing that the converter remains operational after the failure. Besides that, the converter provides a constant output voltage (500 V) even after the fault, demonstrating

the effectiveness of the proposed rectifier and the converter. As the output voltage remains constant, the amount of processed power is the same before and after the fault. Therefore, the amount of current on the resonant tank is twice after the fault, as previously described. The detailed waveforms before and after the fault can be observed in the Figs. 3.35 (d) and (f), respectively. As can be seen in these figures, the converter behaves as a FB-SRC before the defect and as a Asym-HB-SRC after. Furthermore, the experimental waveforms (Figs. 3.35 (a) and (b)) are in accordance with the theoretical one shown in Fig. 3.21



**Fig. 3.35:** Experimental results of the FB-SRC (without the reconfigurable rectifier on the secondary side) under a fault on the switch  $s_2$ : (a) dynamic behavior of the converter during the fault, (b) steady-state operation before the fault and (c) steady-state operation after the fault.

and Fig. 3.24 .

To summarize, the results have shown that the proposed converter can handle a short-circuit fault in one device and still provide the required output voltage and power, keeping the continuity of operation.

One of the main advantages of the proposed approach is to preserve the converter's performance after the failure, and to demonstrate that, the converter's efficiency was measured before and after the fault. The efficiency test was carried for converter operating at input-output voltage levels of 600 V to 700 V and output power of 3 kW. The efficiency values were obtained experimentally using the high precision power analyzer WT1800 from *Yokogawa*. Before the fault the converter reached an efficiency of 98.25%, whereas it presented 98.1% after the failure. As can be noticed, similar values of efficiency were obtained for both cases. The small deviation between these values is observed, because the current effort after failure on the primary side semiconductor is higher, resulting in higher losses. On the other hand, there is less component on the current path of the secondary side, reducing the losses in this side. These results show an acceptable deviation on the converter's performance. Then, the small influence of the proposed fault tolerant approach on the converter's efficiency is verified

## Summary

Among the suitable DC-DC converters for implementing the modular ST architecture, the SRC is highlighted as a candidate to enable very high performance. In addition to the efficiency, high reliability is extremely desired for ST application. In this context, the SRC has been analyzed, considering the ST specification and requirements, and an optimum design procedure of the SRC to obtain not only high efficiency, but also high reliability was proposed.

The possible operation modes for the converter have been described and the DCM with the switching frequency equal or slightly below the resonance frequency is the most efficient operation point. For designing the converter, the current stresses and losses in the components were carefully modeled, in order to minimize them. Different semiconductors technology, such as Si-IGBT and SiC-MOSFETs, were considered during the design and the converter have been experimentally tested with different semiconductors. As an outcome from this investigation, the most suitable configuration to reach high efficiency is using SiC-MOSFETs on the primary side and parallel connection of SiC Diodes

and IGBT on the secondary side.

To increase the reliability, the two most critical devices were analyzed: the primary side semiconductor and the resonant capacitor. To avoid fault on the switch, a fault-tolerant SRC topology was proposed to be used, instead of the classic one, avoiding the interruption of the system in faulty case. The proposed fault tolerance method consists in reconfiguring the FB-SRC in a HB-SRC, in case of a semiconductor failure, keeping the converter operational. The proposed approach can be applied to the series resonant converter based on full-bridge, three-level, flying capacitor and neutral point clamped topologies, and the reconfiguration methodology for each of them was described. As a result of the reconfiguration, the output voltage is reduced. To overcome this problem a modified rectifier that can be reconfigured in a voltage doubler rectifier, keeping the output voltage constant, was used. Then, a family of SRC with fault capability was generated and presented. The main advantages of the proposed converter are: post-fault operation, simple implementation, reduced number of additional component and no efficiency deterioration. As a drawback, the resonant capacitor must be designed for higher voltage and the current efforts on the healthy devices in failure mode operation are twice than that in normal mode operation.

To improve the reliability of the resonant capacitor, its lifetime model is used and a trade-off between the resonant tank parameters selection was found. As a results, the resonant tank circuit should have a high capacitance value ( $C_r$ ) and small inductance value ( $L_r$ ) (for a given resonant frequency). Following this procedure, the capacitor lifetime is extended. In that case, only the leakage inductance of the transformer should be used as the resonant inductor, and no additional components should be included.

Finally, the description of the implemented prototype was provided, as well as experimental results. The converter was tested under fault condition and its capability to withstand the fault and to remain in operation was demonstrated. Furthermore, the proposed converter has obtained a peak efficiency of 98.61%, proving the validity of the presented design.

## Chapter 4

# Active Bridges DC-DC Converter

**T**HE active bridge DC-DC converters have received much attention in the last years, specially the Dual Active Bridges (DAB), which has been intensively employed in different application, including ST [16–19]. Its choice is justified in many publications by its soft-switching feature and the possibility to control the power easily.

The class of active bridge converter can be divided in three main converters: conventional DAB, three-phase DAB and multiple active bridge (MAB). All of them can operate in soft-switching and use the PSM to control the power. This classification has been already presented in Chapter 2 of this thesis and a brief overview of these converters has been shown.

Among the active bridge converters, the DAB is the simplest one to be implemented, by virtue of using only two single-phase bridges and one conventional single-phase transformer. For this reason, it has been used in ST in many works [16–19]. The three-phase DAB, on the other hand, uses two three-phase bridges (one in each side) connected through a three-phase transformer, increasing the complexity of the transformer and the number of component. The only advantage offered by this converter is the reduction of the output capacitive filter, when compared to the conventional DAB. The limited advantage of this topology does not justify the extra investment in switches and the increase complexity of the transformer. For these reasons, this converter is not investigated

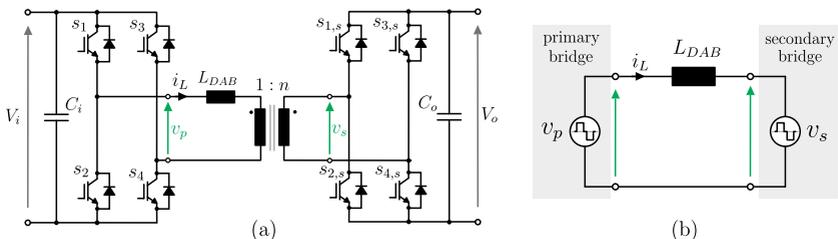
in this work.

The MAB converter is an extension of the DAB, where multiple active bridges are coupled to the same multiwinding transformer. The MAB presents a complicated structure of the transformer, when compared to the DAB, because of the multiwinding arrangement. However, the number of HFT and modules can be reduced, when the MAB is adopted in ST, offering significant advantages in terms of cost [47]. Thus, the MAB converter might be very advantageous economically in ST, which motivates further investigation in this topology.

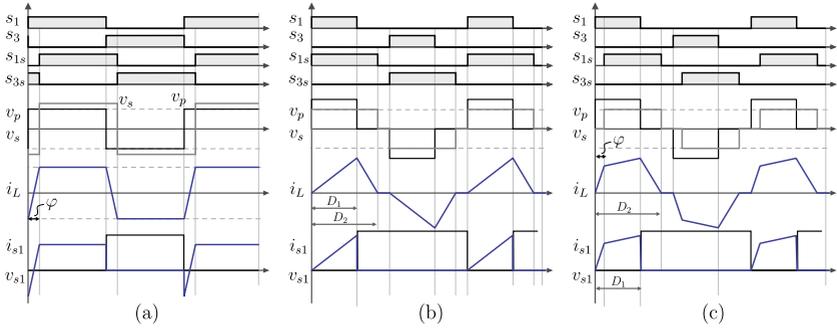
Then, this chapter presents the modulation, operation and analysis of the DAB and MAB converters. As a matter of simplicity, the DAB is analyzed first, where the possible modulation strategies are described and the main equations are derived. Afterward, the analysis of the QAB (a special configuration of the MAB, where four bridges are used) is presented, following the same procedure of the DAB. Then, a multi-objective design taken into account cost and efficiency is carried out for the QAB converter and all the steps of the design algorithm are described.

## 4.1 DAB Converter: Theoretical Analysis

The topology of the DAB converter is presented in Fig. 4.1, where it is composed by two active bridges, connected through the inductance  $L_{DAB}$  and a transformer. Even though the DAB topology is similar to the SRC, its operation is totally different.



**Fig. 4.1:** Topology of the Dual Active Bridge (DAB) DC-DC converter and (b) its equivalent circuit.



**Fig. 4.2:** Main waveforms of the DAB converter considering different modulation strategies: (a) phase-shift modulation (PSM), triangular current modulation (TCM), trapezoidal modulation (TPM).

### 4.1.1 Modulation Strategy

To modulate the DAB, many strategies have been presented [131–136], but the phase-shift modulation (PSM) is the most adopted one. The main waveforms of the DAB using the PSM is depicted in Fig. 4.2 (a). In this scheme, rectangular voltages  $v_p$  and  $v_s$  with 50% duty-cycle, constant switching frequency  $f_s$  and phase-shift of  $\varphi$  are applied to the transformer. The power is controlled by the phase difference between the bridges. The PSM is characterized by ZVS turn-on of the semiconductors, low rms current, symmetrical share of the losses in all switches, high power transfer capability and simplicity of implementation. On the other hand, these advantages are obtained depending on the input-output voltage ratio and also the chosen operation point (nominal phase shift  $\varphi$ ), as explained in Chapter 2.

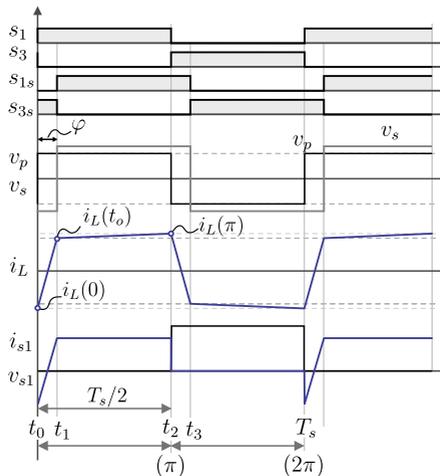
When the input voltage and/or output voltage of the converter deviate significantly from their nominal values (around 20%, according to [72, 134]), the soft-switching operation is normally lost. In this condition, the PSM is not advantageous anymore [134]. To overcome this problem, alternatives modulation strategies have been proposed, like the triangular current mode (TCM) and the trapezoidal modulation (TPM), as shown in Fig. 4.2 (b) and (c), respectively. The TCM imposes a triangular shape current on the transformer, while the TPM generates a trapezoidal current waveform on the transformer, as shown in 4.2 (b) and (c), respectively. Contrary to the PSM, the TCM and

TPM control the duty-cycle for transferring power between the input and output of the converter. These strategies can operate with soft-switching independently from the input and/or output voltage deviation, but with penalty on the peak value of the currents. To transfer the same amount of power, the DAB converter presents higher peak values of currents, when TCM and TPM are adopted in comparison with the PSM, because of the triangular or rectangular shape of the current. It means that the rms value of the currents on the semiconductors and transformers are also expected to be higher, implying in more conduction losses.

In ST application, the input and output voltage are typically constant without large deviation from the nominal value. In this context, the PSM is very advantageous and, therefore the DAB converter is analyzed next using this strategy.

### 4.1.2 Analysis of the DAB using the PSM

For the theoretical analysis of the DAB converter, the equivalent circuit shown in Fig. 4.1 (b) can be used, where the active bridges are replaced by rectangular voltage sources  $v_p$  and  $v_s$ . The waveforms of  $v_p$  and  $v_s$



**Fig. 4.3:** Voltage and current waveforms of the DAB converter operating with PSM.

are shown in Fig. 4.3. Analyzing the equivalent circuit, the inductor current is described by (4.1).

$$i_L(t) = i_L(t_0) + \frac{1}{L} \int_{t_0}^{t_0+T_s} v_L(t) dt \quad (4.1)$$

$$i_L(t) = i_L(t_0) + \frac{1}{L} \int_{t_0}^{t_0+T_s} (v_p - nv_s) dt$$

The average power transferred can be defined by (4.2).

$$P = \frac{1}{T_s} \int_{t_0}^{t_0+T_s} p(t) dt = \frac{2}{T_s} \int_{t_0}^{t_0+T_s/2} v_p(t) i_L(t) dt \quad (4.2)$$

$$P = \frac{2V_i}{T_s} \int_{t_0}^{t_0+T_s/2} i_L(t) dt$$

Considering the current waveform shown in Fig. 4.3, the inductor current can be described by (4.3). In this equation, the initial values are defined by (4.4) and (4.5), respectively.

$$i_L = \begin{cases} i_L(t_0) + \frac{v_p + nv_s}{L} t, & t_0 < t < t_1 \\ i_L(t_1) + \frac{v_p + nv_s}{L} (t - t_1) & t_1 < t < t_0 + \frac{T_s}{2} \end{cases} \quad (4.3)$$

$$i_L(t_0) = -\frac{(V_i - nV_o)\pi - 2nV_o\varphi}{4\pi f_s L} \quad (4.4)$$

$$i_L(t_1) = \frac{(nV_o - V_i)\pi - 2V_i\varphi}{4\pi f_s L} \quad (4.5)$$

Note that  $i_L(t_0) = -i_L(\pi)$  in steady-state condition. Replacing (4.3) in (4.2) and rearranging that, the equation of the power transference of the DAB is obtained, as shown in (4.6) [72].

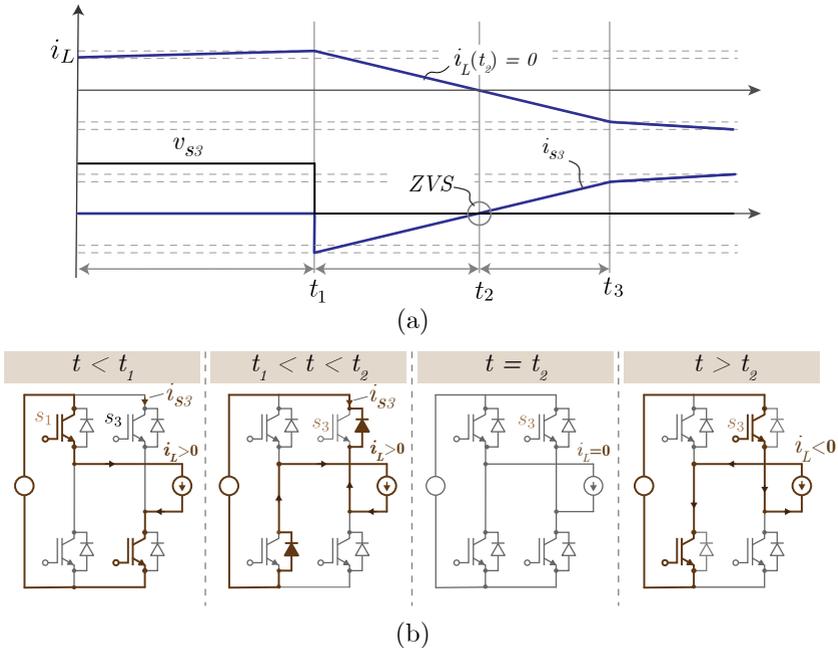
$$P = \frac{V_i V_o}{2\pi f_s L n} \varphi \left( 1 - \frac{|\varphi|}{\pi} \right) \quad (4.6)$$

The input-output voltage relation of the DAB can be defined as  $d$  and given by (4.7). The output power can be rewritten then in terms of this relation, as shown in (4.8).

$$d = \frac{nV_o}{V_i} \quad (4.7)$$

$$P = \frac{V_i^2}{2\pi f_s L_r} d\varphi \left(1 - \frac{|\varphi|}{\pi}\right) \quad (4.8)$$

The ZVS is achieved during the turn-on of the switch when the intrinsic diode of the device is conducting (assuring zero voltage over the device) immediately before the channel starts conducting. To exemplify this operation, the Fig. 4.4 shows the waveforms of the currents ( $i_L$  and  $i_{s3}$ ) and stages during the turn-on of the device  $s_3$ . In the first stage ( $t < t_1$ ), the switch  $s_3$  is off and the current  $i_L$  flows through  $s_1$  and  $s_4$ . Then, the switches  $s_1$  and  $s_4$  turn off at  $t = t_1$  and the current  $i_L$  flows through the intrinsic diodes of the switches  $s_2$  and  $s_3$ ,



**Fig. 4.4:** Simplified analysis of the ZVS commutation of the switch  $s_3$  of the DAB converter: (a) current waveforms of the inductor ( $i_L$ ) and switch  $s_3$  ( $i_{s3}$ ), and (b) topological states of the converter during the commutation.

discharging the inductor  $L_{DAB}$ . During this period, the voltage across the semiconductor  $s_3$  is zero. The second stage ends when the inductor is fully discharged  $i_L = 0$  (at  $t = t_2$ ). Finally, the inductor current becomes negative ( $i_L < 0$ ), and the channel of the device  $s_3$  starts conducting. It happens under zero voltage, as highlighted in Fig. 4.4.

To guarantee this operation, the following conditions must be satisfied:  $i_L(0) \leq 0$  and  $i_L(\varphi) \geq 0$  (c.f. Fig. 4.3). The requirement of  $i_L(\varphi) \geq 0$  ensures the turn-on under ZVS of the switches  $s_1$  and  $s_4$  (see Fig. 4.3), while  $i_L(0) \leq 0$  guarantees the soft-switching of the devices  $s_2$  and  $s_3$ . Applying these limits in the equations (4.4) and (4.5), the ZVS boundary conditions are obtained and described in (4.9). Accordingly, the area constrained by the equation (4.9) indicates the soft-switching region of the DAB converter, which is the desired operation region.

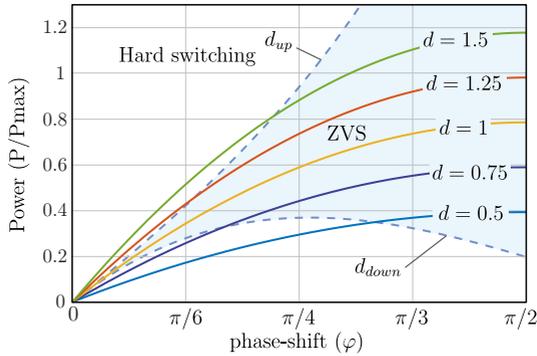
$$\begin{cases} d_{ZVS(up)} = 1 - \frac{3\varphi}{2\pi} \\ d_{ZVS(down)} = \frac{1}{1 - \frac{3\varphi}{2\pi}} \end{cases} \quad (4.9)$$

Fig. 4.5 shows the variation of the normalized power in function of the phase-shift angle for several values of  $d$ , in which the soft-switching boundaries are highlighted. Note that the DAB converter operates in ZVS for the entire range of load if  $d = 1$ , i.e.  $V_i = nV_o$ . Consequently, the DAB converter can be properly design to operate with soft-switching for the whole load range.

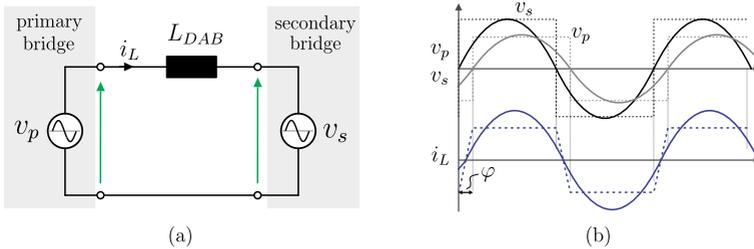
To verify the effect of  $\varphi_{nom}$  on the circulating current of the DAB, the reactive power equation in function of  $\varphi_{nom}$  is derived. To simplify the analysis, the sinusoidal approach is used, where only the fundamental component of the waveforms are considered, as shown in Fig. 4.6. Using the Fourier series and considering only the first harmonic, the fundamental component of the voltages on the primary side and secondary side ( $v_p$  and  $v_s$ ) are described by (4.10) and (4.11), respectively.

$$v_{p1} = \frac{4V_i}{\pi} \sin(\omega t) \quad (4.10)$$

$$v_{s1} = \frac{4V_i}{\pi} \sin(\omega t - \varphi) \quad (4.11)$$



**Fig. 4.5:** Output power of the DAB converter in function of phase-shift angle  $\varphi$ , considering several input-output voltage relation  $d$ .



**Fig. 4.6:** (a) Equivalent circuit and (b) main voltage and current waveforms of the DAB converter considering the fundamental component.

Consequently, the inductor current is given by

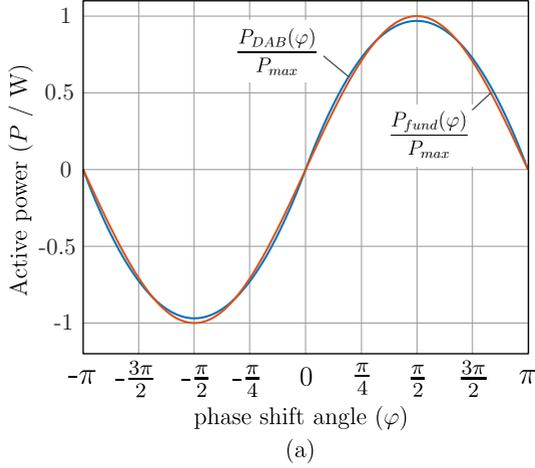
$$i_{L1} = \frac{v_{p1} - v_{s1}}{2\pi f_s L}. \quad (4.12)$$

The total apparent power of the converter is described by

$$S_{DAB} = v_{p1} i_{L1} \quad (4.13)$$

Finally, the active and reactive power of the DAB converter are defined by (4.14) and (4.15), respectively.

$$P_{DAB} = \frac{4V_i V_o}{\pi^3 f_s L} \sin(\varphi) \quad (4.14)$$

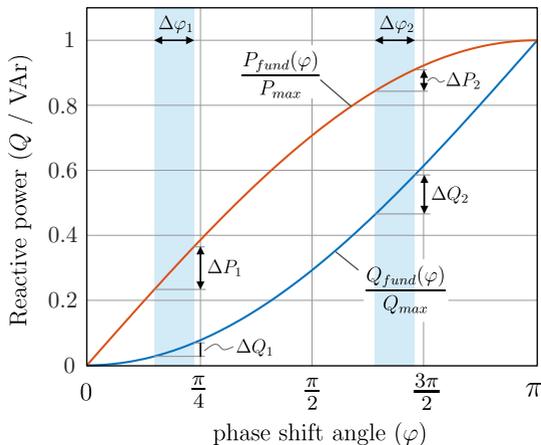


**Fig. 4.7:** Comparison of the normalized power of the DAB converter obtained by the analytical analysis ( $P_{DAB}/P_{max}$ ) and obtained by the fundamental component approach ( $P_{fund}/P_{max}$ ) in function of the phase-shift angle  $\varphi$ .

$$Q_{DAB} = \frac{4V_i V_o}{\pi^3 f_s L} (1 - \cos(\varphi)) \quad (4.15)$$

As can be noticed, using the sinusoidal analysis approach, the equations are simplified, as observed from (4.13) to (4.15). To verify the accuracy of this approach, the active power transferred derived using the accurate method (as shown in equation (4.6)) is compared to that one obtained from the simplified sinusoidal approach. Both equations are plotted in function of the phase-shift angle, as illustrated in Fig. 4.7. From this graphic, a very small deviation between both power curves is observed, validating the simplified approach.

Similarly, Fig. 4.8 shows the variation of the normalized active and reactive power of the DAB converter in function of the phase-shift angle. As can be observed, the active power increases as a sinusoidal function with the phase-shift, while the reactive power increases exponentially. For the phase-shift range of  $0 < \varphi < \pi/4$ , a small increment on the angle  $\Delta\varphi_1$  implies a significant increment on the active power  $\Delta P_1$ , but only a light increment on the reactive power  $\Delta Q_1$  (cf. Fig. 4.8). Conversely, if the same angle increment  $\Delta\varphi_2 = \Delta\varphi_1$  is applied in the

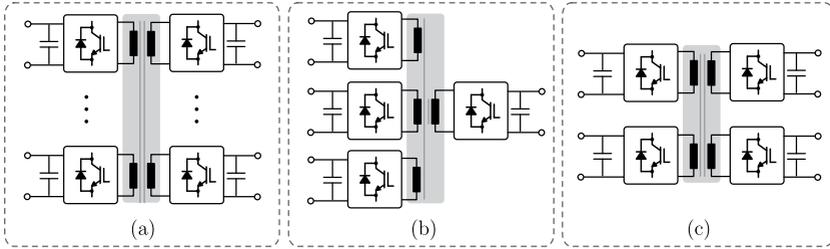


**Fig. 4.8:** Normalized active and reactive ( $Q_{DAB}/Q_{max}$ ) power in function of the phase shift angle.

interval constrained by  $\pi/4 < \varphi < \pi/2$ , the active power increases slightly defined by  $\Delta P_2$ , while the reactive power has a substantial increment of  $\Delta Q_2$ . It is clear in Fig. 4.8 that  $\Delta P_1 > \Delta P_2$  and  $\Delta Q_1 < \Delta Q_2$ , meaning that the first interval ( $0 < \varphi < \pi/4$ ) has more effect on the active, whereas the second one ( $\pi/4 < \varphi < \pi/2$ ) has more effect on the reactive power. Indeed, low reactive power is desired for reducing losses and maximizing the efficiency, which is obtained selecting the nominal phase-shift angle in the range of  $0 < \varphi_{nom} < \pi/4$ .

## 4.2 QAB Converter: Theoretical Analysis

The simplified circuit of the MAB converter is shown in Fig. 4.9 (a), where the multiple bridges are coupled to the same multiwinding HFT. As aforementioned, the QAB converter is a particular case of the MAB, in which four bridges are used and it is analyzed next. The QAB can be configured symmetrically, in which 2 bridges are connected to the input and the other two to the output, as depicted in Fig. 4.9 (c), or asymmetrically, where three bridges are connected to the input and one to the output, as shown in Fig. 4.9 (b). The theoretical analysis of the converter is carried out in detail considering the asymmetrical



**Fig. 4.9:** Possible configuration of the MAB converter: (a) generic topology, (b) asymmetrical configuration and (c) symmetrical configuration of the MAB converter, when four active bridges are used.

configuration and then the results are extended to the symmetrical one.

Regardless the configuration, the bridges can have different voltage levels and they can exchange power among them independently from the others. It means that the QAB can have several operation modes, according to the power flows and voltage level of each bridge, making its general analysis very extensive. In ST application, the QAB has restricted operation modes with regard to the voltage level, power flow, etc. These restrictions simplify considerably the analysis. Therefore, the comprehensive analysis of the QAB is initially presented and later the ST restrictions are taken into account, where the main equations are derived.

To modulate the converter, the strategies presented before for the DAB can be directly adopted to the QAB, i.e. the PSM, TCM and TPM. Nevertheless, only the PSM has been applied to any MAB converter type so far. Taking this into account, the QAB is investigated considering the conventional PSM and the TCM, as a further contribution of this work. Then, the converter's performance using the TCM is evaluated in order to verify the possible advantages that it can bring to the converter.

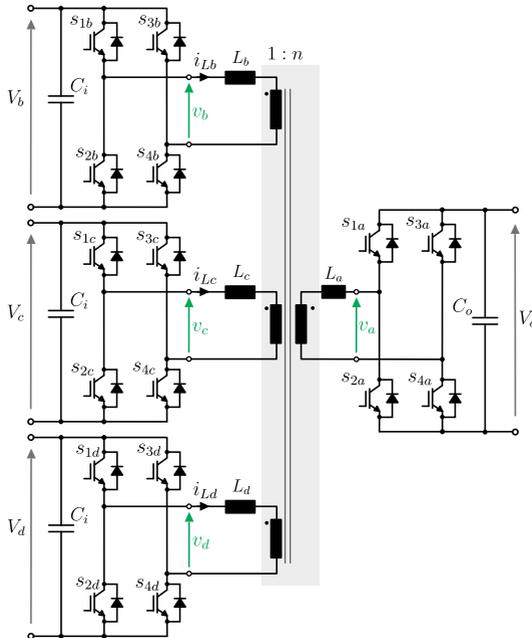
### 4.2.1 Analysis of the QAB using the PSM

The topology of the QAB converter with asymmetrical configuration is depicted in Fig. 4.10, and each bridge is denoted by the letters  $a$ ,  $b$ ,  $c$  and  $d$ . The elements of the bridges have sub-index  $i = \{a, b, c, d\}$  to indicate the bridge the element belongs to.

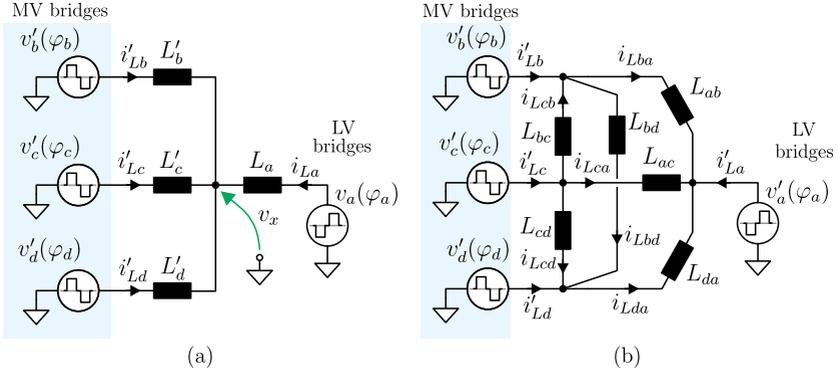
The equivalent circuit of the QAB based on the Y-model and  $\Delta$ -model are shown in Fig. 4.11, in which the bridges are replaced by rectangular voltage sources reflected to the same side ( $v_a, v_b, v_c$  and  $v_d$ ). The parameters of the equivalent circuit (cf. Fig. 4.11) are determined using the original parameters shown in Fig. 4.10 and the transformer turns ratio, as presented in (4.16). In this equation  $n_i$  is the number of turns of the specific bridge  $i$ .

$$v'_i = \frac{v_i}{n_i} \quad i'_i = i_i n_i \quad L'_i = \frac{L_i}{n_i^2} \quad (4.16)$$

Each voltage source is characterized by its phase-shift angle ( $\varphi_i$ ) and the constant voltage of the DC side ( $V_i$ ). It means that bridges  $a, b, c$  and  $d$  have a phase angle defined by  $\varphi_a, \varphi_b, \varphi_c, \varphi_d$ , respectively. In the PSM, the power transference depends basically on the angle difference between the bridges and not on the angle value itself. Thus, a reference



**Fig. 4.10:** Topology of the QAB converter using the asymmetrical configuration.



**Fig. 4.11:** Equivalent model of the QAB converter: (a) Y-model and (b)  $\Delta$ -model.

set point can be established for every bridge, and in this analysis the angle of the LV side bridge is selected as the reference. Hence,  $\varphi_a = 0$ , as shown in Fig. 4.12 (a).

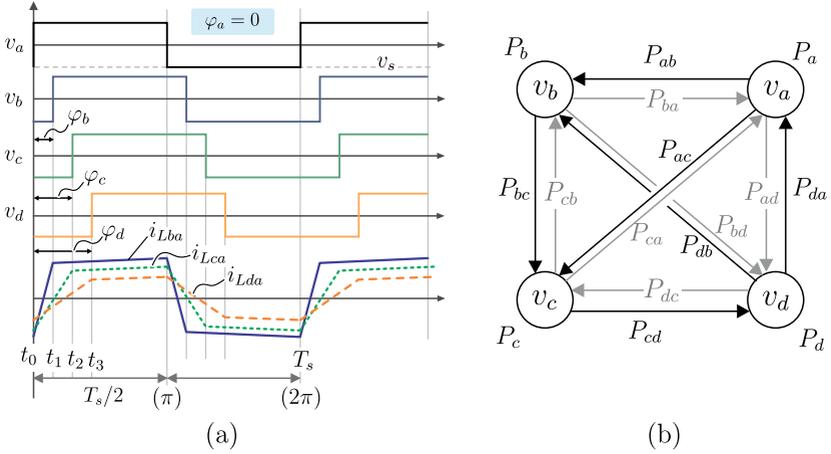
In the Y-model, the voltage at the central point  $v_x$  and the current slope of each inductor are calculated by (4.17) and (4.18), respectively. The inductance  $L'_a$ ,  $L'_b$ ,  $L'_c$  and  $L'_d$  illustrated in the Y-model are obtained directly from real circuit shown in Fig. 4.10, considering also the transformer turns ratio.

$$v_x = \frac{v'_a + v'_b + v'_c + v'_d}{4} \quad (4.17)$$

$$\frac{di'_{Li}}{dt} = \frac{(v'_i - v_x)}{L'_i} \quad (4.18)$$

The  $\Delta$ -model is more suitable for evaluating the power flow, because the bridges are directly connected through an equivalent inductance, as depicted in Fig. 4.11 (b). Hence, the  $\Delta$ -model can be seen as several DAB connected between them. In contrast to the Y-model, where the parameters (e.g. inductance and currents) are obtained directly from the original circuit (cf. Fig. 4.10), the parameters of the  $\Delta$ -model are not obtained straightforward, but they are derived using circuit analysis.

The waveforms of the QAB circuit based on the  $\Delta$ -model is illustrated in Fig. 4.12 (a), while the power flow directions among the bridges are depicted in 4.12 (b). As shown in Fig. 4.12 (a), the current



**Fig. 4.12:** (a) Voltages and currents voltages of the QAB converter using the  $\Delta$ -model and (b) the power flow direction exchanged among the bridges.

flowing between two bridges, for instance bridges  $a$  and  $b$ , is  $i_{Lba}$  and it is controlled by the angle  $\varphi_b$ . Thus, the current and power exchanged between these two bridges ( $i_{Lba}$  and  $P_{ab}$ ) is calculated similarly as a DAB converter. The same approach can be carried out to determine the power and/or current flowing between the bridges  $a$  and  $c$  and then,  $a$  and  $d$ . Finally, the superposition theorem can be used to define the total power and current of the bridge  $a$  ( $P_a$  and  $i_a$ ). In conclusion, the  $\Delta$ -model can be seen as connection of multiples DAB converters.

Using the Kirchhoff's law, the current of the bridges are determined by (4.19).

$$\begin{cases} i'_a = -i_{Lba} - i_{Lca} - i_{Lda} \\ i'_b = i_{Lba} - i_{Lcb} + i_{Lbd} \\ i'_c = i_{Lca} + i_{Lcb} + i_{Lcd} \\ i'_d = i_{Lda} - i_{Lcd} - i_{Lbd} \end{cases} \quad (4.19)$$

The current variation on the inductance  $L_{ab}$  is described by (4.20) and then it is generalized for the other inductances in (4.21), where  $k = \{a, b, c, d\}$ ,  $j = \{a, b, c, d\}$  and  $k \neq j$ .

$$L_{ab} \frac{i_{Lba}}{dt} = v'_{ba} = v'_b - v'_a \quad (4.20)$$

$$L_{jk} \frac{i_{Ljk}}{dt} = v'_{kj} = v'_k - v'_j \quad (4.21)$$

From these equations and using the relation shown in (4.18), the equivalent inductance of the  $\Delta$ -model are obtained and they can be comprehensively determined by (4.22).

$$L_{jk} = L'_j L'_k \left( \frac{1}{L'_a} + \frac{1}{L'_b} + \frac{1}{L'_c} + \frac{1}{L'_d} \right) \quad (4.22)$$

The power exchanged between two bridges is obtained by means of the same approach used for DAB converter. For instance, the power transferred from the bridge  $a$  to the bridges  $b$ ,  $c$  and  $d$  are calculated by (4.23), while the power exchange between the bridges  $b$  and  $c$  is analytically described by (4.24).

$$\begin{cases} P_{ab} = \frac{V_a V_b}{2\pi f_s L_{ab}} \varphi_b \left( 1 - \frac{|\varphi_b|}{\pi} \right) \\ P_{ac} = \frac{V_a V_c}{2\pi f_s L_{ac}} \varphi_c \left( 1 - \frac{|\varphi_c|}{\pi} \right) \\ P_{ad} = \frac{V_a V_d}{2\pi f_s L_{ad}} \varphi_c \left( 1 - \frac{|\varphi_c|}{\pi} \right) \end{cases} \quad (4.23)$$

$$P_{bc} = \frac{V_a V_c}{2\pi f_s L_{bc}} (\varphi_c - \varphi_b) \left( 1 - \frac{|(\varphi_c - \varphi_b)|}{\pi} \right) \quad (4.24)$$

Then, the power exchanged between two generic bridges  $j$  and  $k$  can be determined by (4.25).

$$P_{jk} = \frac{V_k V_j}{2\pi f_s L_{jk} n_{jk}} \varphi_{jk} \left( 1 - \frac{|\varphi_{jk}|}{\pi} \right) \quad (4.25)$$

$$\varphi_{jk} = \varphi_j - \varphi_k, \quad n_{jk} = n_j / n_k$$

The total power processed by an individual bridge is calculated by the sum of power exchanged between the referred bridge and the others, as described by (4.26). This equation is constrained by  $P_a + P_b + P_c + P_d = 0$ .

$$\begin{aligned}
 P_a &= P_{ab} + P_{ac} + P_{ad} \\
 P_b &= P_{ba} + P_{bc} + P_{bd} \\
 P_c &= P_{ca} + P_{cb} + P_{cd} \\
 P_d &= P_{da} + P_{db} + P_{dc}
 \end{aligned} \tag{4.26}$$

The total power depends on all phase-shift angles ( $\varphi_b$ ,  $\varphi_c$  and  $\varphi_d$ ), demonstrating a coupling among them, but it can be simply calculated, as for the DAB converter.

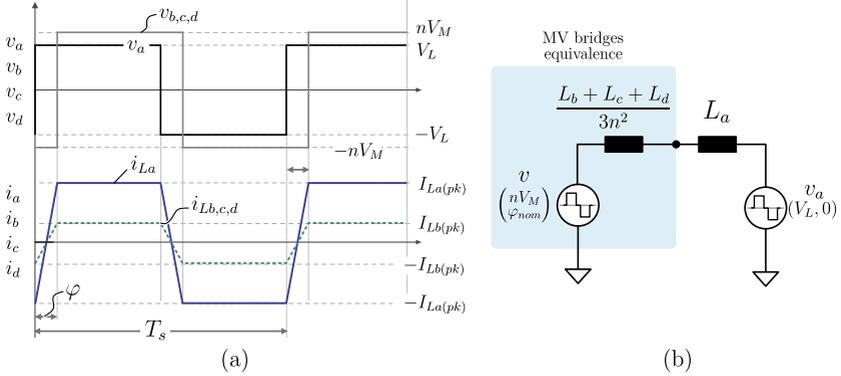
As aforementioned, the ST application poses some restrictions to the operation modes of the QAB with regard to the voltage level and power flow, which simplifies a lot the analysis. The restrictions in questions are:

- ▶ The bridges connected to the MV side have the same voltage  $V_M$ .
- ▶ Power balanced condition is considered, i.e. the MV bridges process the same amount of power.
- ▶ The MV bridges have the same phase-shift angle with respect to the LV grid, defined by:  $\varphi_b = \varphi_c = \varphi_d = \varphi_{nom}$ .
- ▶ The power flow occurs only from the MV side to the LV side or vice versa. There is no power exchanged among the MV cells.
- ▶ The conventional power flow is from MV to LV.
- ▶ The windings connected to the MV bridges have the same number of turns, as well as those connected to the LV bridges. It means that the transformer turn ratio  $n$  is only the relation between the MV windings to the LV windings.
- ▶ The DC link voltage of the MV bridges and LV bridges are defined as  $V_M$  and  $V_L$ , respectively.

Considering these assumptions, the power transferred from the MV side to the LV side is then simplified and determined by (4.27).

$$P_o = \frac{V_M V_L}{2\pi f_s n L_{eq}} \varphi_{nom} \left( 1 - \frac{|\varphi_{nom}|}{\pi} \right) \tag{4.27}$$

In this equation,  $L_{eq}$  is the equivalent inductance seen by the LV side, which is calculated by (4.28).



**Fig. 4.13:** (a) Waveforms of the QAB converter (b) and the equivalent circuit considering the ST operation restrictions.

$$L_{eq} = L_a + \frac{L_b + L_c + L_d}{3n^2} \quad (4.28)$$

Using the nominal power, phase-shift angle and voltage, the required equivalent inductance can be calculated then by (4.29). This can be implemented physically on the MV side and/or LV side, but the relation shown in (4.28) must be satisfied.

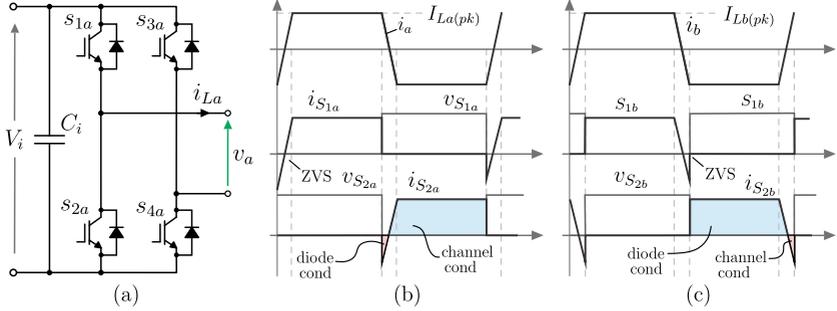
$$L_{eq} = \frac{V_M V_L}{2\pi f_s n P_o} \varphi_{nom} \left( 1 - \frac{|\varphi_{nom}|}{\pi} \right) \quad (4.29)$$

The restrictions dictated by the ST application entail a significant simplification, in such way that the QAB converter performs similarly to the DAB converter, and its equivalent circuit and main waveforms considering these restrictions are shown in Fig. 4.13.

To compute the current stresses on the semiconductors and transformer, the peak current on the LV side inductor ( $I_{L_a(pk)}$ ) and MV side inductor ( $I_{L_b(pk)}$ ) are required, and they can be calculated by (4.30) and (4.31), respectively.

$$I_{L_a(pk)} = \frac{V_L - \sqrt{V_L^2 - 8L_{eq}f_s n V_L I_o}}{4L_{eq}f_s} \quad (4.30)$$

$$I_{L_b(pk)} = \frac{I_{L_a(pk)}}{3n} \quad (4.31)$$



**Fig. 4.14:** (a) Topology of the active bridge and the current and voltage waveforms on the semiconductors of the (b) MV bridge and (c) LV bridge.

Using the concept of average and rms values presented in (4.32) and (4.33), and considering the current waveforms presented in Fig. 4.14 for positive power flow, i.e. from MV to LV side, the current stresses on the semiconductors and transformer are computed.

$$i_{S1a,rms} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{S1a}^2(t) dt} \quad (4.32)$$

$$i_{S1a,avg} = \frac{1}{T_s} \int_0^{T_s} i_{S1a}(t) dt \quad (4.33)$$

The average and rms current on the diodes of the MV bridges in function of the nominal phase-shift angle are calculated by (4.34) and (4.35).

$$i_{D1b(avg)} = \frac{I_{LPK(LV)}}{3n} \frac{\varphi}{8\pi} \quad (4.34)$$

$$i_{D1b(rms)} = \frac{I_{LPK(LV)}}{3n} \sqrt{\frac{\varphi}{12\pi}} \quad (4.35)$$

Likewise, the average and rms current on the channel of the MV side semiconductors are computed by (4.36) and (4.37), in function of the nominal phase-shift angle.

$$i_{S_{1b(avg)}} = \frac{I_{LPK(LV)}}{6n} \left( 1 - \frac{3\varphi}{4\pi} \right) \quad (4.36)$$

$$i_{S_{1b(rms)}} = \frac{I_{LPK(LV)}}{3n} \sqrt{\frac{1}{2} \left( 1 - \frac{5\varphi}{12\pi} \right)} \quad (4.37)$$

Similarly, the average and rms currents on the semiconductor (intrinsic body diode and channel) of the LV side are calculated from equation (4.38) to (4.41).

$$i_{D_{1a(avg)}} = \frac{I_{LPK(LV)}}{2} \left( 1 - \frac{3\varphi}{4\pi} \right) \quad (4.38)$$

$$i_{D_{1a(rms)}} = I_{LPK(LV)} \sqrt{\frac{1}{2} \left( 1 - \frac{5\varphi}{12\pi} \right)} \quad (4.39)$$

$$i_{S_{1a(avg)}} = I_{LPK(LV)} \frac{\varphi}{8\pi} \quad (4.40)$$

$$i_{S_{1a(rms)}} = I_{LPK(LV)} \sqrt{\frac{\varphi}{12\pi}} \quad (4.41)$$

The rms current on the MV side and LV side inductors (and also transformer) are calculated by (4.42) and (4.43), respectively.

$$i_{L_{1a(rms)}} = I_{LPK(LV)} \sqrt{1 - \frac{2\varphi}{3\pi}} \quad (4.42)$$

$$i_{L_{1b(rms)}} = \frac{I_{LPK(LV)}}{3n} \sqrt{1 - \frac{2\varphi}{3\pi}}. \quad (4.43)$$

As observed in these equations, the current stresses in every component are somehow proportional to the  $\varphi$ . Furthermore, when the power flows from the MV to the LV, most of the current flows through the channel of the MV side semiconductors, whereas it flows mostly through the body diode on the LV side. Therefore, it is very important to select a power semiconductor for the LV side with low forward drop voltage for the body diode.

### 4.2.2 Analysis of the QAB with TCM

The TCM was introduced in [134] for the DAB converter and it will be extended to the QAB next, with the aim to evaluate if this strategy can bring some benefits in terms of efficiency to the converter. Differently from the PSM strategy, the TCM uses the duty-cycle to control the power transferred among the bridges. The duty-cycle of the bridges  $a$ ,  $b$ ,  $c$  and  $d$  are defined, respectively, by  $d_a$ ,  $d_b$ ,  $d_c$  and  $d_d$ . Using the TCM, the switches of the MV cells can operate with ZCS and the circulating reactive power on the converter can be reduced. On the other hand, the rms current can increase compared to the PSM, depending on the input-output voltage ratio. This strategy has been intensively investigated for the DAB converter [134–136], and in this work, it is extended to the QAB converter.

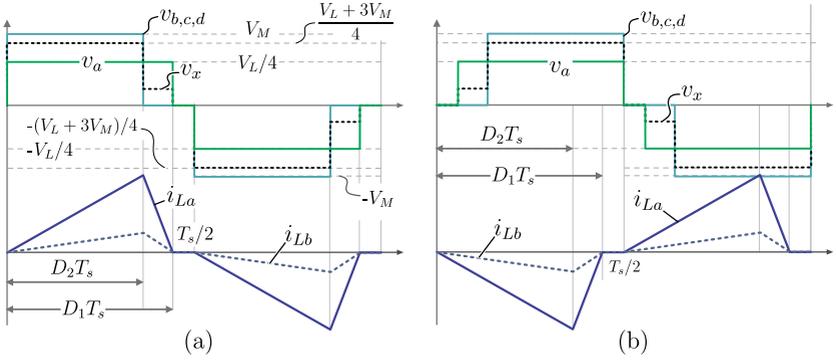
Considering the power balance restriction (i.e.  $P_b = P_c = P_d$ ), the MV bridges perform similarly and their duty-cycle can be considered the same:  $d_b = d_c = d_d = D_2$ . The duty-cycle of the LV bridge is given by  $d_a = D_1$ .

The basic principle of the TCM is to impose a triangular current on the inductors, as shown in Fig. 4.15. To achieve that, the voltages  $v_a$  and  $v_b$  should have the waveforms exactly as depicted in Fig. 4.15 (a). Consequently, in this operation mode, the voltage  $v_x$  (see Fig. 4.11) is defined as

$$v_x = \begin{cases} \frac{nV_L + 3V_M}{4}, & 0 < t < D_2T_s \\ \frac{nV_L}{4}, & D_2T_s < t < D_1T_s \\ 0, & D_1T_s < t < T_s/2 \end{cases} \quad (4.44)$$

As can be seen in Fig. 4.15 (a), the current in the inductor starts from zero and reaches its maximum value  $\Delta i_{Lb}$  during the time period of  $0 < t < D_2T_s$ , where  $T_s$  is the switching period. The current variation during this period, denoted as  $\Delta i_{Lb(0 < t < D_2T_s)}$ , can be calculated using (4.18), where  $v_x$  is given by (4.44), resulting in (4.45). As the currents start from zero, the switches  $s_{1a}$  and  $s_{4a}$  of the LV side and also the switches  $s_{1b,c,d}$  and  $s_{4b,c,d}$  of the MV side turn on at zero current switching (ZCS).

$$\Delta i_{Lb(0 < t < D_2T_s)} = \frac{D_2(V_M - nV_L)}{4Lf} \quad (4.45)$$



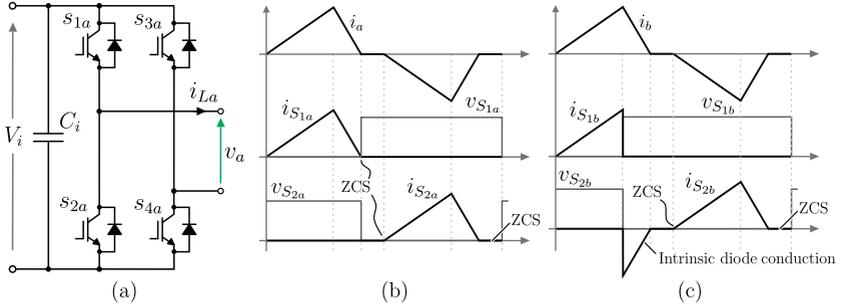
**Fig. 4.15:** Current and voltage waveforms of the QAB converter using the TCM, for (a) positive power flow and (b) negative power flow.

Likewise, during the period  $D_2T_s < t < T_s/2$ , the currents decrease from  $\Delta i_{Lb}$  until reach zero again. In this period, the current variation denoted as  $\Delta i_{Lb(D_2T_s < t < T_s/2)}$  can also be calculated by (4.18), resulting in (4.46). In the moment  $t = D_2T_s$ , the current is zero and the switches  $s_{1,b,c,d}$  turn off at ZCS. It is important to note that the period in zero state should be long enough to deplete all charge accumulated in the IGBT during the conduction state. Thus, this commutation can be critical for rated load operation, where the stored charge is high and the zero time period is small [137]. To achieve ZCS operation regardless the load and input or output voltages levels, the condition  $\Delta i_{Lb(0 < t < D_2T_s)} = \Delta i_{Lb(D_2T_s < t < T_s/2)}$  must be satisfied. As a result, the relation between the duty-cycle  $D_1$  and  $D_2$  is found and presented in (4.47).

$$\Delta i_{Lb(D_2T_s < t < T_s/2)} = \frac{nV_L (D_1 - D_2)}{4Lf_s} \quad (4.46)$$

$$D_2 = \frac{V_L \cdot n}{V_M} D_1 \quad (4.47)$$

The transferred power can be derived analyzing the DC side of the bridge  $b$ :  $P_B = I_b V_M$ . The average current in the bridge  $b$  ( $I_b$ ) is calculated in (4.48). Thus, the power processed by the bridge  $b$  and  $a$  are calculated by (4.49).



**Fig. 4.16:** (a) Topology of the active bridge and the current and voltage waveforms on the semiconductors of the (b) MV bridge and (c) LV bridge.

$$I_b = \frac{2}{T_s} \int_0^{D_2 T_s} i_b(d) dt = \frac{D_2^2 (V_M - nV_L)}{4Lf_s} \quad (4.48)$$

$$P_b = \frac{D_1^2 (V_L n)^2 (V_M - V_L n)}{4Lf_s V_M}$$

$$P_a = \frac{3D_1^2 (V_L n)^2 (V_M - V_L n)}{4Lf_s V_M} \quad (4.49)$$

As observed in (4.49), the duty-cycle of the cell  $a$  ( $D_1$ ) is used to control the power transferred, while the duty-cycle of the MV cells ( $D_2$ ) are used to ensure the ZCS operation.

The current and voltage waveforms on the semiconductors of the MV and LV sides are depicted in Fig. 4.16. As can be noticed in this figure, the LV side devices switch at ZCS during the turn-on and turn-off. On the MV cell, the  $i_{S2b}$  has ZCS during the turn-on and turn-off, while the switch  $i_{S1b}$  has ZCS only during the turn-on. Using the curves presented in Fig. 4.16 and the concept of average and rms values presented in (4.32) and (4.33), the stresses on the semiconductors are obtained.

The rms currents on the MV and LV sides of the transformer in function of the duty-cycle  $D_1$  are calculated by (4.50) and (4.51), respectively.

$$i_{Lb(rms)} = \frac{nV_L (V_M - nV_L)}{12Lf_s V_M} \sqrt{6D_1^3} \quad (4.50)$$

$$i_{La(rms)} = \frac{n^2 V_L (V_M - nV_L)}{4Lf_s V_M} \sqrt{6D_1^3} \quad (4.51)$$

The rms and average currents through the semiconductors of the LV bridge are calculated by (4.52) and (4.53), respectively.

$$i_{S1a(rms)} = \frac{n^2 V_L (V_M - nV_L)}{4Lf_s V_M} \sqrt{3D_1^3} \quad (4.52)$$

$$i_{S1a(avg)} = \frac{3D_1^2 (n^2 V_L) (V_M - nV_L)}{8Lf_s V_M} \quad (4.53)$$

As observed in Fig. 4.16, the MV side semiconductor have unequal power sharing. Then, the rms and average currents through semiconductors  $s_{1b}$  are defined by (4.54) and (4.55).

$$i_{S1b(rms)} = \frac{nV_L (V_M - nV_L)}{12Lf_s V_M} \sqrt{\frac{3D_1^2 nV_L}{V_M}} \quad (4.54)$$

$$i_{S1b(avg)} = \frac{D_1^2 (nV_L)^2 (V_M - nV_L)}{8Lf_s V_M^2} \quad (4.55)$$

Similarly, the current stresses on the MV side semiconductor  $s_{2b}$  are computed by (4.56) and (4.57).

$$i_{S2b(rms)} = \frac{nV_L (V_M - nV_L)}{12Lf_s V_M} \sqrt{3D_1^3} \quad (4.56)$$

$$i_{S2b(avg)} = \frac{D_1^2 (nV_L) (V_M - nV_L)}{8Lf_s V_M} \quad (4.57)$$

From the power equation described by (4.49), the TCM can not be applied when the input and output voltages are equal. In this case, there is no power transference, and it is mathematically expressed in (4.49) by the term  $(V_M - V_L n)$ . Therefore, this modulation is more suitable when the input and output voltage are very different [134].

### 4.2.3 Evaluation and Comparison of the Modulation Strategies

The performance of the QAB converter operating with the TCM and the PSM strategies are compared, in order to verify which modulation strategy is more beneficial for the converter's efficiency. As the power dissipation is directly related to the current stresses on the main components of the converter, then they are calculated using the previous equations and plotted in function of the output power, considering both modulation cases.

To calculate the current stresses, different parameters are required for the TCM and the PSM modulation schemes. In case the same parameters are used (e.g. inductance, transform turn ratio, etc), the output power provided by the converter is higher when PSM is adopted in comparison with the TCM. As an example, considering the same circuit parameters of the QAB converter ( $L_{eq} = 100 \mu H$ ), the power function versus the control parameters for both modulation strategy is plotted in Fig. 4.17. This shows that the maximum power of the QAB is  $P_{max} = 30$  kW when the PSM is used, whereas only  $P_{max} = 3.3$  kW is achieved when the TCM is employed. It means that the PSM has higher power transfer capability. Hence, different parameters of the QAB converter must be used according to the modulation strategy, for comparison purpose.

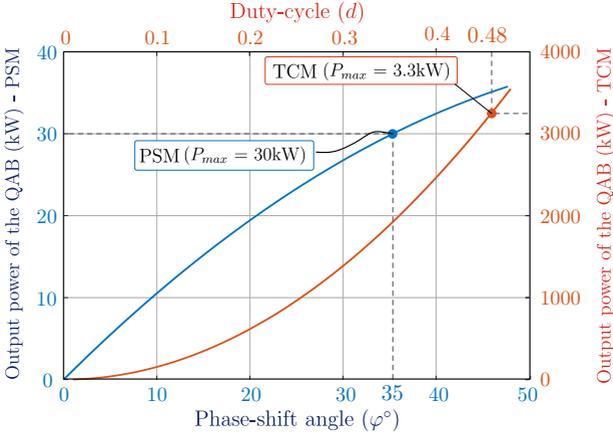
For a trustworthy comparison, the same output power, switching frequency, as well as input and output voltage level are assumed for both modulation, and all these parameters are presented in Table 4.1. To

**Tab. 4.1:** Parameters used for the PSM and TCM comparison

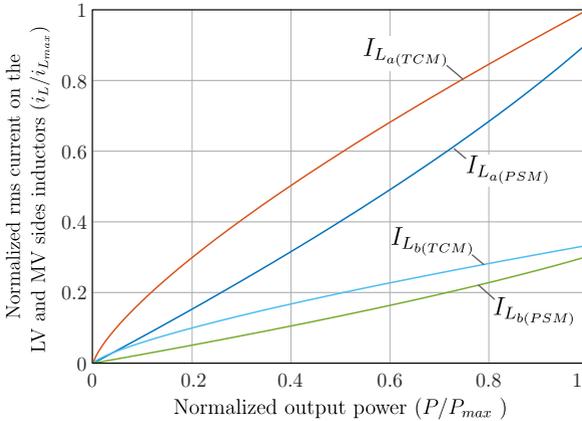
Parameters	PSM	TCM
Output nominal power	$P_a = 30$ kW	
Input voltage	$V_M = 800$ V	
Output voltage	$V_L = 700$ V	
Switching frequency	$f_s = 20$ kHz	
Turn ratio	$n = 1.14$	$n = 2$
Equivalent inductance	$L_{eq} = 100\mu H$	$L_{eq} = 17.8\mu H$
Nominal operation point	$\varphi_{nom} = 45^\circ$	$D_1 = 0.48$

reach the same power level, the equivalent inductance and the transformer turns ratio need to be different, according to the modulation scheme, as shown in Table 4.1. Furthermore, the operation point is also presented for both cases.

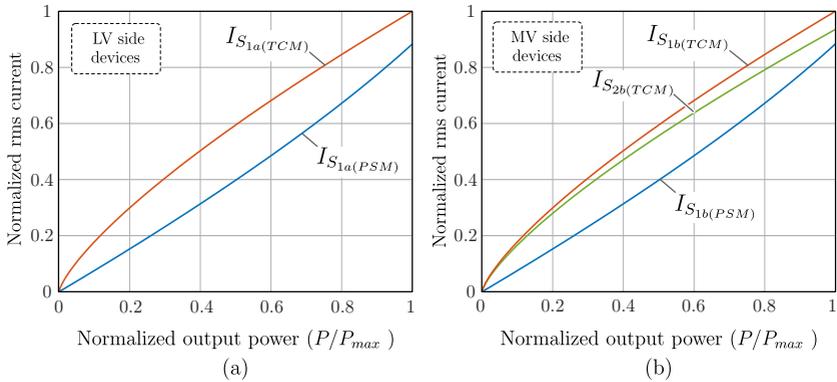
Fig. 4.18 shows the normalized rms current on the MV and LV



**Fig. 4.17:** Output power capability of the QAB converter for different modulation strategy, considering the same circuit parameters.



**Fig. 4.18:** Comparison of the QAB performance for the TCM and PSM strategies: rms current on the MV and LV sides inductors (and transformer).



**Fig. 4.19:** Comparison of the QAB performance for the TCM and PSM strategies: (a) rms current on the LV side semiconductors and (b) rms current on the MV side semiconductors.

side inductors in function of the normalized output power, for both modulation strategies. As can be noticed, the rms currents are smaller when the PSM is used. It means lower losses on the inductor and transformer when the PSM is used, instead of the TCM. The normalized rms current on the MV and LV side semiconductors in function of the normalized output power is plotted in Fig. 4.19, for the QAB converter operating with PSM and TCM. Similarly to the previous case, current stresses on the semiconductors are reduced when the PSM is used.

In contrast to the TCM, the PSM is simpler to implement and the soft-switching feature does not depend on the converter parameters, as the inductance for instance. Furthermore, the current stresses and losses are smaller, implying in higher performance. For constant input and output voltage level, the QAB based on PSM can be properly design to operate with soft-switching and low rms currents, for all operation range of the load. However, when wide variation of the input voltage is expected, the TCM becomes advantageous, because the converter can still operate under soft-switching. In overall, the PSM offers more advantages for the QAB performance in ST application, because of the restriction of constant input and output voltages established by the ST.

## Experimental Evaluation

In spite of the TCM has been successively applied in the DAB converter, it was never used in the MAB converter and it has been extended for the first time to this converter in this PhD Thesis.

Therefore, the QAB converter was simulated and experimentally tested, in order to verify the operation of the converter with the TCM and to validate the theoretical analysis developed in this work. Hence, the results obtained by simulation and experimental tests are compared and discussed next. The converter was simulated using the MATLAB/Simulink and the PLECS toolbox, and subsequently a down scaled prototype of 2.5 kW was built and tested in laboratory. The primary goal of the prototype is to confirm the analytically studied converter capabilities by experimental results. For that reason a reduced scale prototype was used, and the main specifications are presented in Table 4.2.

For the experimental set-up, maximum duty-cycle of  $D_{1max} = 0.45$  was chosen. Using the specification shown in Table 4.2 and the previous equation, the required inductance is calculated. The Fig. 4.20 shows the picture of the implemented prototype, where the power board, control board and also the multi-winding transformer are observed. IGBT modules from *Infineon Technologies* with voltage rating of 1.2 kV were used in all bridges, and the specification is also presented in Table 4.2.

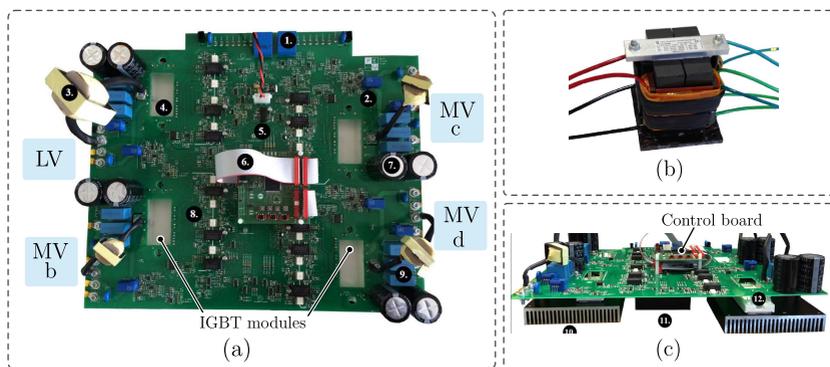
**Tab. 4.2:** Specification of the implemented QAB DC-DC converter prototype

Parameter	Value
Rated Output Power	$P_o = 2.5kW$
LV dc-link ( $V_L$ )	$V_L = 200V$
MV dc-link ( $V_{Mb}, V_{Mc}, V_{Md}$ )	$V_M = 250V$
Switching frequency	$f_s = 20kHz$
Additional external inductance	$L_a = L_b = L_c = L_d = 35\mu H$
Transformer turns ratio	$n = 1 : 1 : 1 : 1$
Output filter capacitor	$C = 500\mu F$
IGBT $S_{1,2,3,4}$	Infineon SIGC32T120R3E IGBT3 (1200V/25A)

Additional inductors of  $35\ \mu\text{H}$  were added to each winding of the transformer, as shown in Fig. 4.20. The transformer is based on a U-shaped ferrite core, and it is depicted in 4.20 (b).

The experimental results consist of relevant voltage and current waveforms for steady-state operation of the QAB converter using the TCM and they are presented in Fig. 4.21 and Fig. 4.22. The Fig. 4.21 (a) and (b) show, respectively, the simulation and experimental results of the voltage and current on the LV side ( $v_a$ ,  $i_{La}$ ) and MV side ( $v_b$ ,  $i_{Lb}$ ) for the converter at light load operation, i.e.  $P_a = 1\text{ kW}$ . As can be observed, the converter operates with soft-switching, low duty-cycle, and very large zero-time of the currents. In this operation condition, the commutation of the semiconductors is not critical, because there is enough time to deplete all charge accumulated in the IGBT during the conduction state before the next commutation.

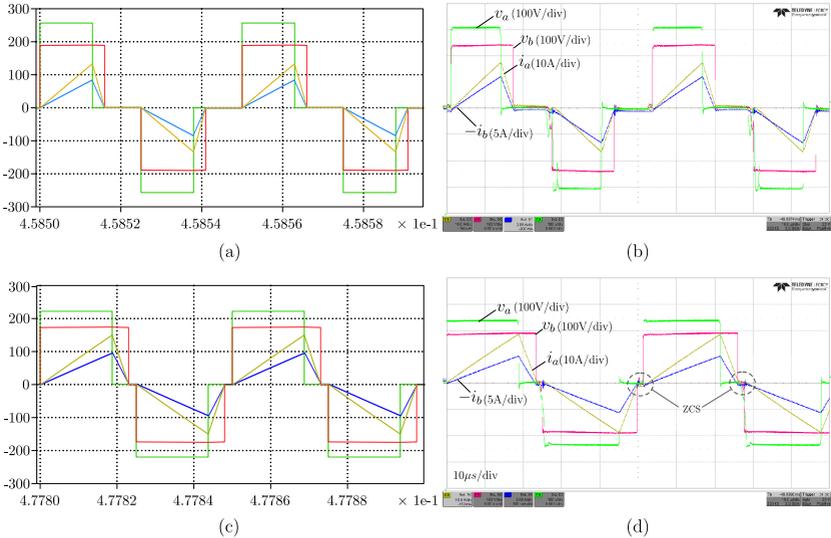
Likewise, the Fig. 4.21 (c) and (d) illustrate the same waveforms obtained by simulation and experimental tests, respectively, considering now the nominal power condition. In this case, the converter operates with an output power around 2.5 kW, divided equally among the MV cells, i.e. balanced condition. As expected, the current and voltage waveforms are very similar to the theoretical waveforms and the ZCS feature can be noticed in the figure. Moreover, the results obtained by simulation and experimentally are analogous, emphasizing the accuracy of such results. The switching details are depicted in Fig. 4.22. Al-



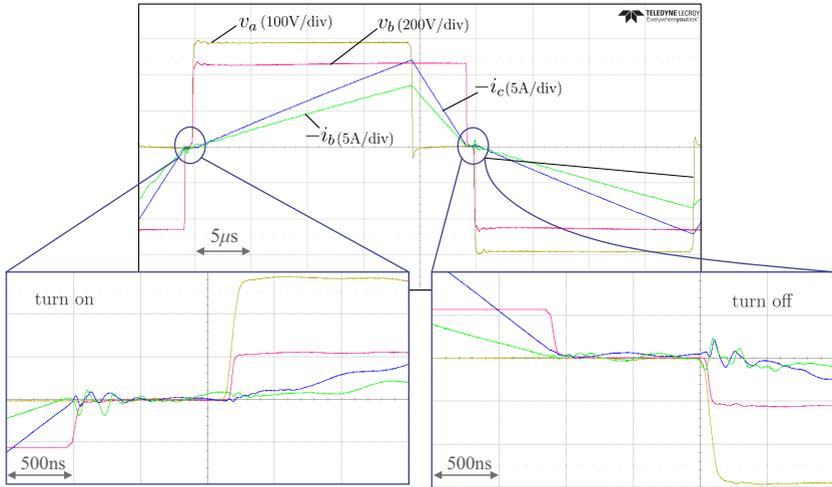
**Fig. 4.20:** Picture of the implemented prototype: (a) top view of the converter prototype. (b) HF multiwinding transformer and (c) front view of the converter.

though the zero-time of the current is very short in the nominal power condition (worst condition), the ZCS operation is still achieved during the turn-on and turn-off of the semiconductor, and it is confirmed in this result.

The waveforms obtained by simulation and experimental tests are very similar to the theoretical waveforms described in this work. Finally, these results demonstrate the operation principle and the analytical equations derived during the theoretical analysis of the QAB using the TCM developed in this work.



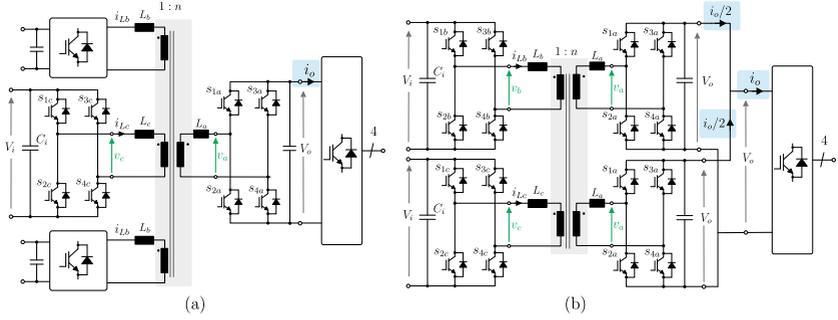
**Fig. 4.21:** Waveforms of the QAB converter obtained by simulation and experimental tests. Voltage and current on the MV side ( $v_b$  and  $i_b$ ) and LV side ( $v_a$  and  $i_a$ ). (a) Simulation and (b) experimental results for light load condition. (c) Simulation and (d) experimental results for high load condition. (Time scale:  $10\mu\text{s}/\text{div}$ ).



**Fig. 4.22:** Experimental results of the QAB converter: detail of the commutation, demonstrating the ZCS condition.

### 4.3 Evaluation of the MAB converter in ST application

The advantages offered by the PSM for the MAB converter was discussed and demonstrated in the previous section, and for this reason it is adopted. Apart from the different modulations, the converter can be configured asymmetrically or symmetrically. Fig. 4.23 shows the QAB converter with both configuration. In section III, the QAB converter configured asymmetrically based on the PSM was analyzed. Nevertheless, the operation principle of the QAB converter is essentially the same, regardless the configuration. Actually, the configuration will play a role on the current stresses on the semiconductors, inductors and transformers. Therefore, using the same approach presented in Section III, the current stresses on the semiconductors and inductors of the converter are generalized and described in equations (4.58) to (4.62). In these equations,  $k$  represents the configuration of the QAB and it is defined in (4.63).



**Fig. 4.23:** Circuit of the QAB converter with (a) asymmetrical and (b) symmetrical configuration.

$$I_{L_{a(pk)}} = \frac{V_L - \sqrt{V_L^2 - 16L_{eq}f_s n V_L I_o / (5 - k)}}{4L_{eq}f_s} \quad (4.58)$$

$$I_{L_{b(pk)}} = \frac{I_{L_{a(pk)}}}{nk} \quad (4.59)$$

$$i_{S_{1b(avg)}} = \frac{I_{L_{a(pk)}}}{2nk} \left( 1 - \frac{3\varphi}{4\pi} \right) \quad (4.60)$$

$$i_{S_{1b(rms)}} = \frac{I_{L_{a(pk)}}}{nk} \sqrt{\frac{1}{2} \left( 1 - \frac{5\varphi}{12\pi} \right)} \quad (4.61)$$

$$i_{L_{1b(rms)}} = \frac{I_{L_{a(pk)}}}{nk} \sqrt{1 - \frac{2\varphi}{3\pi}}. \quad (4.62)$$

$$k = \begin{cases} 1, & \text{symmetric config} \\ 3, & \text{asymmetric config} \end{cases} \quad (4.63)$$

Note that the equations (4.60) to (4.62) describe only the current stresses on the MV side components. The current stresses on the LV side components presented earlier in equations (4.38) to (4.42) are still valid for the symmetrical configuration of the QAB. The difference lies on the current peak value  $I_{L_{a(pk)}}$ , because it is a function of the output current, which changes according to the configuration, as highlighted in (4.23). Then, the peak current  $I_{L_{a(pk)}}$  is generalized in (4.58).

## 4.4 Design of the QAB Converter

Among the main design constrains, the cost and efficiency are the most important ones for the basic module of the ST. In this regard, the optimum design of the QAB converter for improving not only the efficiency, but also the cost, is described.

An approach analogous to that one presented for the SRC is used for designing the QAB converter. Nevertheless, in this case, the efficiency and cost are the optimization parameters, instead of efficiency and reliability. The losses in the main components of the QAB are carefully computed in function of the main converter parameters, with the aim of selecting properly these parameters, minimizing the losses. Moreover, a computer-aided design is implemented to assist the design parameters choice, where an algorithm to calculate the losses and cost is developed, allowing to perform the multi-objective optimization.

Similar specification used for the SRC design is also used to design the QAB converter, and it is shown in Table 4.3. As discussed, the modular approach offers the advantages to choose the specification of the basic module, design it only once and then combine many of them to reach the ST specification. Of course, the specification of the basic cell will play a very important role during the selection of the number of modules used to implement the entire system. It will be discussed in the next chapter, where the optimum number of power unit will be derived. The asymmetrical configuration of the QAB is used, as shown in Fig. 4.23, and more discussion about the QAB configuration on the system implementation is also presented in Chapter 5.

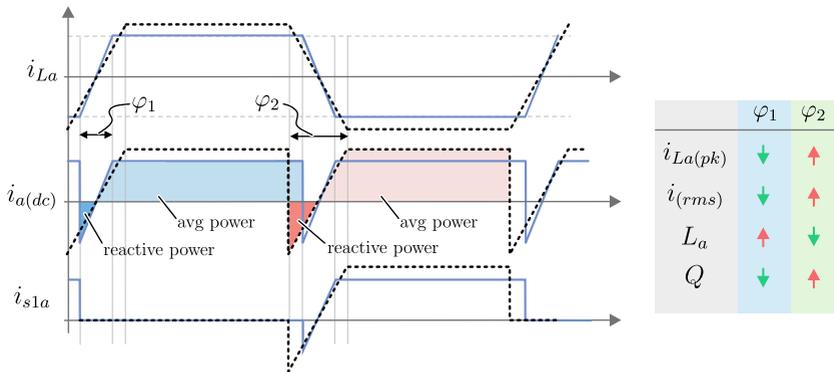
The voltage level presented in Table 4.3 were selected to enable the use of 1.2 kV semiconductors on the primary and secondary sides, implying in a wide variety of device choice and offering more alternatives for the multi-objective design presented herein.

**Tab. 4.3:** Specification of the QAB converter used for the design

Input voltage	Output Voltage	Nominal Power	Isolation frequency
800 V	700 V	20 kW	20 kHz

### 4.4.1 Operation Point

The nominal phase-shift is a crucial parameter during the QAB converter and it plays a very important role on the performance of the QAB converter. The current stresses on the semiconductors and inductors are somehow proportional to the nominal phase-shift angle, as derived before. Then, high angle implies in higher current stresses and therefore losses. Additionally, during the DAB analysis, it was presented that the reactive power increases exponentially with the angle and for  $\varphi > 45^\circ$ , the reactive power rises drastically. This effect can be observed in Fig. 4.24, where the current waveforms of the LV bridge of the QAB is presented for two different phase-shift angle. Both cases has the same output power, i.e. average (avg) power, highlighted in the figure. However, the reactive power increases for higher phase-shift angle ( $\varphi_2$  in this case), as pointed out in this figure. This can be observed on the DC side current ( $i_{a(dc)}$ ), where the circulating current (negative current) is higher for  $\varphi_2$ . The circulating current is defined as the current that flows through the converter, but returns to the input source, instead of being delivered to the load. Furthermore, the peak current through the devices increases according to the angle, as noticed in Fig. 4.24. It has also implications on the current effort and losses on the semiconductors. On the other hand, if large angle is selected, the required inductance is lower. The effect of the phase-shift angle selec-



**Fig. 4.24:** Current waveforms of the QAB converter, considering two different phase shift angle, in order to show the effect on the angle on the circulating (reactive) power and peak current.

tion on the currents, inductance and power is presented in Fig. 4.24 as well.

To verify the effect of nominal angle on the converter's performance, the current efforts on the semiconductors and inductor of both LV and MV sides are plotted in Fig. 4.25. These graphics were plotted using equations (4.30) to (4.43), as well as the specification presented in Table 4.3.

Fig. 4.25 (a) shows the variation of the peak current on the LV and MV side inductors, according to the nominal phase-shift angle, while the Fig. 4.25 (b) shows the variation of the same current as a function of the load for different  $\varphi$ . Similarly, Figs. 4.25 (c) to (e) show the rms and average currents on the semiconductors (intrinsic body diode and channel) and inductors on the LV side and MV side as a function of  $\varphi$ . As expected, high  $\varphi$  implies in higher peak and rms current on these elements and consequently losses. Furthermore, when the power flows from the MV to the LV, most of the current flows through the channel of the MV side semiconductors, whereas it flows mostly through the body diode on the LV side. Therefore, it is very important to select a power semiconductor for the LV side with low forward drop voltage for the body diode.

In overall, high phase shift angle implies in lower required inductance, but in high reactive power and high current efforts on the components [72]. Then, a range between  $30^\circ$  to  $50^\circ$  is desired, and in this work  $\varphi_{nom} = 35^\circ$  is selected.

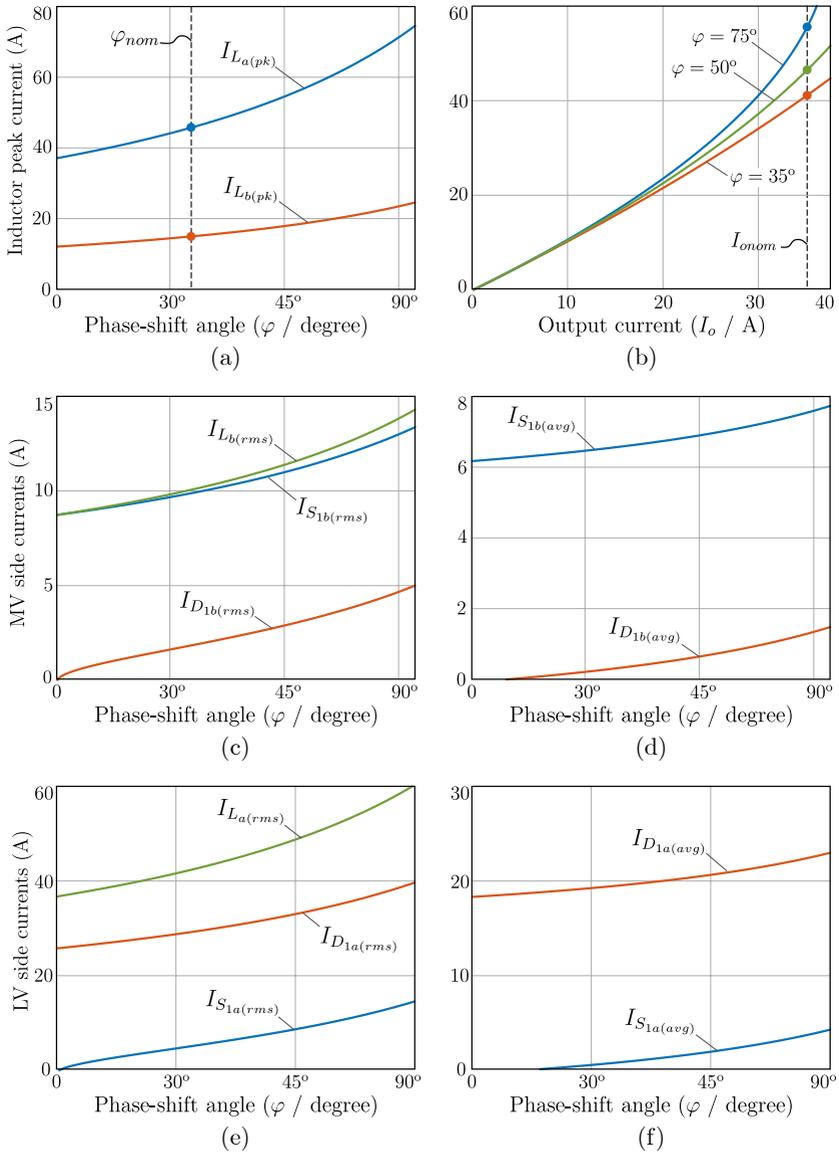
## 4.4.2 Losses Analysis

The losses in all components are analyzed next for the QAB converter.

### Semiconductors

The standard Si-IGBT and SiC-MOSFET with blocking voltage of 1.2 kV are considered for the QAB design. The converter's performance with both semiconductors is compared theoretically and experimentally, in order to verify the possible advantages of these technologies. The semiconductors considered for this design are presented in Table 4.4, and they can be employed in both sides of the QAB converter.

Although the converter is supposed to operate with ZVS, this characteristic is achieved only during the turn-on of the switch. The semiconductors still turn off under hard-switching. Therefore, by using SiC-



**Fig. 4.25:** Current stresses on the QAB converter: (a) and (b) peak current on the LV and MV inductors in function of the nominal phase-shift angle and the output current. (c) Average and (d) rms currents on the MV side. (e) Average and (f) rms currents on the LV side.

MOSFETs, the QAB converter will not only take the advantage of low  $R_{DS(on)}$  of these devices, reducing the conduction losses considerably, but also the low switching energy, reducing the turn-off losses. As can be noticed, three SiC-MOSFET devices and three Si-IGBTs are considered on the design. It results in 36 combinations and then 36 designs iterations.

The conduction losses of the MOSFETs can be generally calculated by (4.64), and simplified to (4.65), assuming constant junction temperature ( $T_J = 100^\circ$ ) and gate voltage ( $V_{gs} = 15V$ ). Similarly, the conduction losses on the IGBT are calculated by (4.66), where  $V_{CE}$  is the collector-emitter voltage, while  $i_C$  is the current that flows on the device. The equation can also be simplified to (4.67), and  $i_C$  becomes the semiconductor current  $I_S$ .

$$P_{MOS(cond)} = \frac{1}{T} \int_0^T R_{ds(on)}(i_{ds}(t), T_J, V_{gs}) \cdot i_{ds}^2(t) dt \quad (4.64)$$

$$P_{MOS(cond)} = R_{ds(on)} \cdot I_{S(rms)}^2 \quad (4.65)$$

$$P_{IGBT(cond)} = \frac{1}{T} \int_0^T V_{CE}(i_C(t), T_J, V_{gs}) \cdot i_f(t) dt \quad (4.66)$$

$$P_{IGBT(cond)} = V_{CE} \cdot I_{S(avg)} + R_f \cdot I_{S(rms)}^2 \quad (4.67)$$

**Tab. 4.4:** Specification of the semiconductors considered in the design

SiC-MOSFET / 1.2 kV					
Name	Reference	I	$R_{ds(on)}(@150C)$	$V_F$	$E_{off}$
SIC-2	C2M0040120D	30 A	84mΩ	3.3 V	0.3 mJ
SIC-2	C2M0040120D	40 A	84mΩ	3.3 V	0.3 mJ
SIC-3	C2M0025120D	90 A	43mΩ	3.3 V	0.3 mJ
Si-IGBT / 1.2 kV					
Name	Reference	I	$V_{CE(on)}(@150C)$	$V_F$	$E_{off}$
IGBT-1	IHW40N120R3	40 A	2.4V	1.3 V	3.1 mJ
IGBT-2	IHW40N120R3	40 A	1.9V	1.3 V	3.1 mJ
IGBT-3	IHW40N120R3	40 A	2.4V	1.3 V	2.03 mJ

The switching losses can be generally calculated by (4.68), where  $N_{sw(on)}$  and  $N_{sw(off)}$  are the number of turn-on and turn-off commutations, respectively, during the time interval  $T_s$ .  $R_g$  is the gate resistance. It is assumed that the power devices switch always with constant voltage, as well as constant junction temperature ( $T_J$ ),  $V_{gs}$  and  $R_g$ . Because of the ZVS operation, the turn-on losses are neglected, and a simplified equation can be written as presented in (4.69). The equation as written in (4.68) is suitable for a computer implementation, because it is already discretized.

$$P_{(sw)} = \frac{1}{T_s} \left( \begin{array}{c} \sum_{n=1}^{N_{sw(on)}} E_{on}(V_{ce}, I_d, T_J, V_{gs}, R_g) + \\ \sum_{n=1}^{N_{sw(off)}} E_{off}(V_{ce}, I_d, T_J, V_{gs}, R_g) \end{array} \right) \quad (4.68)$$

$$P_{(sw)} = \frac{1}{T_s} \left( \sum_{n=1}^{N_{sw(off)}} E_{off}(I_d) \right) = E_{off} \cdot f_s \quad (4.69)$$

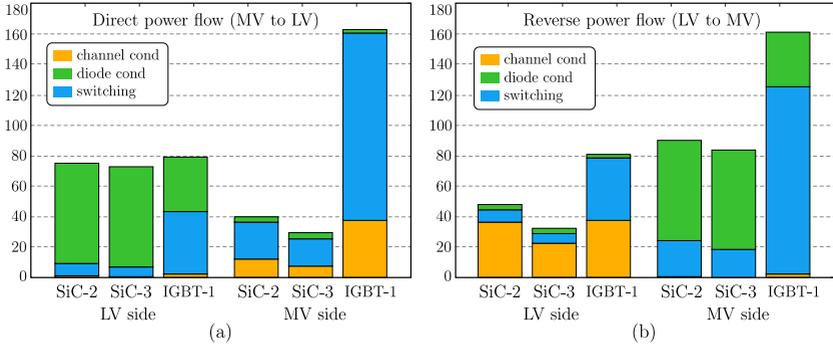
The conduction losses are calculated replacing the equations (4.34) to (4.41) in (4.65) and (4.67), and using the parameters of Table 4.4. Likewise, the switching losses are calculated using the parameters of Tables 4.3 and 4.4 in equation (4.69).

A computer-aided algorithm is used to calculate the semiconductors losses. To verify the losses distribution and performance for different semiconductors technologies, three devices were selected (SiC-2, SiC-3 and IGBT-1), and their losses are calculated for direct (MV to LV) and reverse power flow (LV to MV). The results are illustrated in Fig. 4.26.

Despite of the soft-switching turn-on, the turn-off losses of the QAB are very relevant, mainly when IGBT are employed, because of the high switching energy compared to the SiC-MOSFETs. If SiC-MOSFET is employed in the LV side, and assuming that the gate signal is applied to it<sup>6</sup>, then the current flows through the channel of the MOSFET, instead of flowing through the body diode, because such semiconductor has the ability of conducting reverse current. It provides lower impedance path to the current, reducing the conduction losses. For these reason, the diode losses on the SiC-MOSFETs devices are not relevant in Fig. 4.26.

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<sup>6</sup>Using the PSM, the gate-signal is applied to the switches on the secondary side (LV side, in this case), regardless the semiconductor type and power flow direction.



**Fig. 4.26:** Power dissipation on different semiconductors for the MV and LV side of the QAB converter, for both (direct (a) and reverse (b)) power flow direction.

Note that, the IGBT cannot conduct current in the reverse direction, even when gate signal is applied to it, because it has a bipolar-type structure. Thus, the intrinsic body diode of the IGBT must conduct the current (reverse current) on the LV side.

As expected, the performance of the QAB converter is superior when the SiC-3 (see Table 4.4) is used in both sides, regardless the power flow direction.

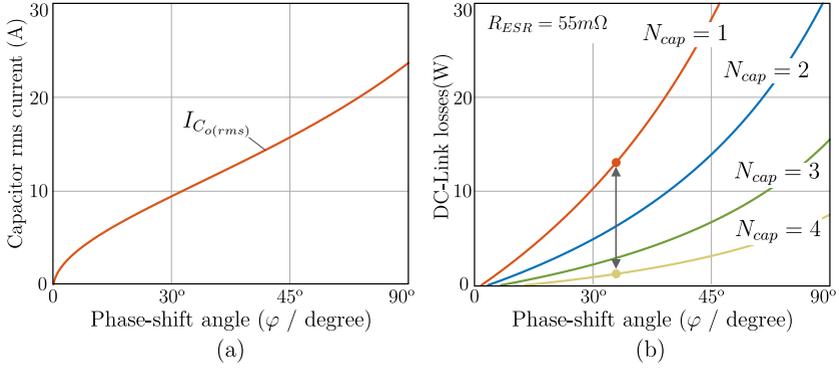
### Output DC Link Capacitor

The rms current through the output capacitor is calculated by (4.70).

$$I_{C_o(rms)} = \sqrt{I_{LPK(LV)}^2 \left(1 - \frac{2\varphi}{3\pi}\right) - \left(\frac{V_L}{R_{load}}\right)^2} \quad (4.70)$$

For the DC link capacitor, the aluminum electrolytic capacitor from EPCOS (*long-life* series), with  $1000\mu F$  capacitance and voltage rating of 450 V is used. This type of capacitor is chosen because of its high energy storage density. The capacitor has an equivalent-series resistance of  $R_{ESR} = 55m\Omega$ . Because of the voltage rating of the capacitors, two devices are connected in series to share the voltage. The losses on this component are calculated according to

$$P_{C_o} = 2 \cdot R_{ESR} \cdot I_{C_o(rms)}^2. \quad (4.71)$$



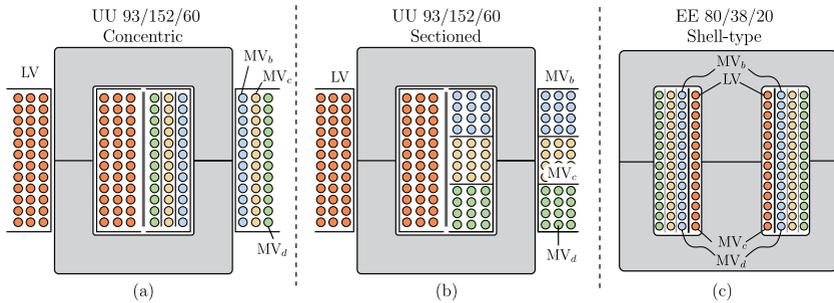
**Fig. 4.27:** (a) Rms current on the output DC link capacitor bank, (b) power dissipated on the DC link capacitors, according to number of parallel capacitors.

The rms current on the output DC link capacitors in function of the designed  $\varphi$ , and also the losses in function of the designed  $\varphi$  for different number of parallel capacitors are illustrated in Fig. 4.27. Parallel capacitors are used, in order to reduce the current effort, losses and also to provide high energy storage on the DC link, guaranteeing the decoupling between both AC sides.

### 4.4.3 HFT Design

To design the HFT, different core shapes and winding construction were considered, as presented in Fig. 4.28. For the U-shape core, two different winding methods were considered and investigated experimentally: concentric and sectioned. In the concentric winding, the MV coils are mounted one over the other (see Fig. 4.28 (a)), whereas in the sectioned, the MV coils are separated, as shown in Fig. 4.28 (b).

An algorithm was developed to assist the HFT design. In this algorithm, the basic design is performed according to [122], where the number of turns is calculated, wires are selected and so on. The feasibility of implementation is verified by the window utilization factor. Then, the core losses, wire losses and temperature rise are estimated. For the wire losses, the skin and proximity effect are considered additionally to the DC losses. To avoid the skin effect, litz wire is used. The losses caused by proximity effect are estimated based on [120]. For the



**Fig. 4.28:** Different HFT implementations: (a) U-shape core with concentric winding, (b) U-shape core with sectioned windings, (c) E-shape core.

**Tab. 4.5:** Transformer specification used for its implementation

parameters	UU93 concentric	UU93 Sectioned	EE-80
Core losses	105 W	85 W	60 W
Wire losses	340 W	98 W	84 W
Leakage inductance (LV)	145 $\mu$ H	140 $\mu$ H	40.7 $\mu$ H
Winding resistance (LV)	0.146 $\Omega$	0.064 $\Omega$	0.08 $\Omega$
Leakage inductance (MV 1)	4.17 $\mu$ H	70.7 $\mu$ H	16.5 $\mu$ H
Winding resistance (MV 1)	0.046 $\Omega$	0.047 $\Omega$	0.072 $\Omega$
Leakage inductance (MV 2)	2.3 $\mu$ H	40.3 $\mu$ H	13.5 $\mu$ H
Winding resistance (MV 2)	0.036 $\Omega$	0.037 $\Omega$	0.059 $\Omega$
Leakage inductance (MV 3)	4.5 $\mu$ H	73.17 $\mu$ H	15 $\mu$ H
Winding resistance (MV 3)	0.049 $\Omega$	0.053 $\Omega$	0.065 $\Omega$
Mag inductance	4.46mH	4.2mH	3.2mH
Implemented HFT			
Core	3 parallel cores - E 80/38/20		
N <sup>o</sup> of turns (LV)	$n_{LV} = 24$		
N <sup>o</sup> of turns (MV)	$n_{MV} = 24$		
wires - (LV)	2000 x AWG44		
wires - (MV)	90 x AWG32		

core losses, the generalized Steinmetz equation [121] is used. Finally, the temperature is estimated according to [122], under the assumption of natural convection cooling.

All the three types of transformers illustrated in Fig. 4.28 were built and tested experimentally, and the main parameters and losses were measured. The results are presented in Table 4.5. Concerning the U-shape core, the sectioned implementation has presented much lower wire losses, because of its lower proximity effect losses compared to the concentric. On the other hand, the sectioned implementation has presented a very high leakage inductance, whereas the concentric is lower. Using the E-shape implementation, it is possible to reach low wire losses and low leakage inductance. However, it is difficult to achieve high isolation voltage between the LV and MV side, as desired by the ST application. Considering these three constrains, the E-shape core is selected to implement the HFT of the QAB converter.

#### 4.4.4 Final Converter Design

In order to find a valuable compromise between efficiency and cost of the QAB converter, a computer-aided based design was used and the flowchart of the developed algorithm is shown in Fig. 4.29. The precise cost estimation is difficult to be obtained, because it is highly dependent on the market parameters, that can change the price over the time, like: distributor, quantity acquired, etc. As a matter of comparison, the cost used in this algorithm for the semiconductors were obtained directly from the devices manufactures, i.e. *Infineon Technology* [138] for the Si-IGBT and *Cree Wolfspeed* for SiC-MOSFET [105]. For the capacitor and transformer cost, the cost were obtained through the well-known distributor Mouser Electronics [139].

The algorithm starts with the basic design of the converter, as shown in Section III, where the converter's parameters are calculated, like: required inductance, phase-shift angle, current efforts, etc. Then, it selects the semiconductors and calculate their losses and cost. At this point, there is an iteration to calculate the losses and cost for all possible combination of semiconductors. The next point is the output capacitance selection, where an iteration is performed to find the proper number of parallel capacitors according to cost and losses. Finally, the HFT is designed, as described in the previous section.

As a result, the theoretical efficiency of the QAB versus its cost

for several designs performed by the algorithm is plotted in Fig. 4.30. Three designs are highlighted in this figure: (1) lowest cost and lowest efficiency; (2) best trade-off between cost and efficiency; (3) highest efficiency and highest cost. The semiconductor selected in each of the pointed-out designs is shown in Fig. 4.30, as well. As can be noticed, the lowest cost and efficiency is obtained when IGBT are employed in both side of the QAB converter. The device SiC-3 provides the best performance, because it has the lowest  $R_{DS(on)}$  (i.e. conduction losses) and switching losses. However, it is the most expensive solution. When SiC-2 is used in the MV and SiC-3 on the LV side of the QAB, the efficiency decreases slightly, but the cost decreases significantly. Therefore, this design presents the best trade-off between cost and efficiency. The losses distribution on the components of the QAB converter for the three highlighted designs are shown in Fig. 4.31. As can be reinforced, even operating with ZVS during the turn-on, the power dissipated during the turn-off is very relevant, when IGBT is used. Therefore, it is very advantageous and recommended to use SiC-MOSFETs.

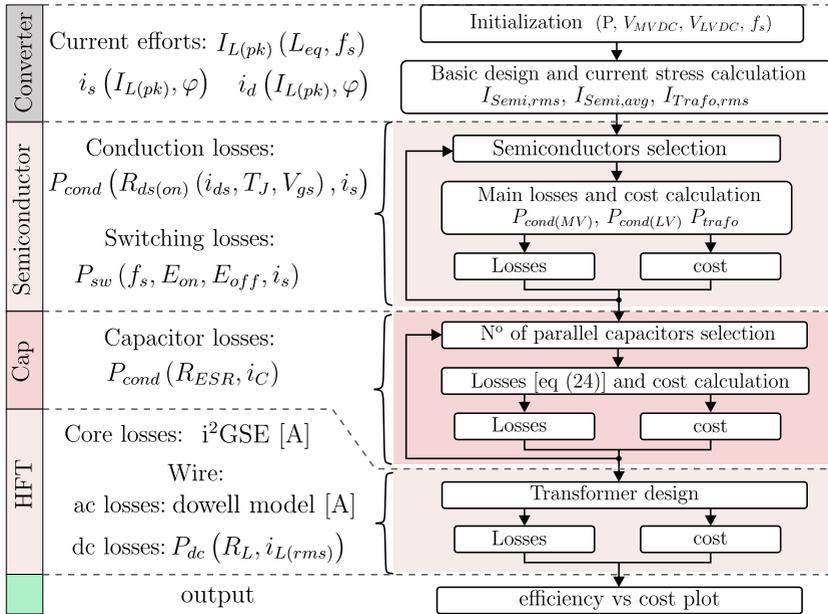
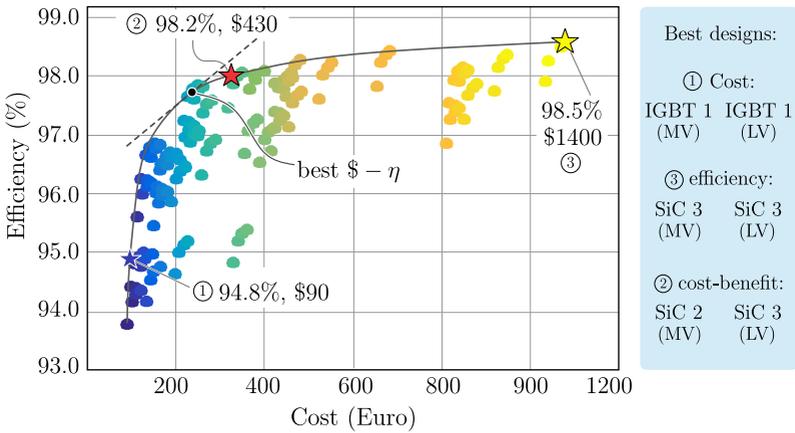
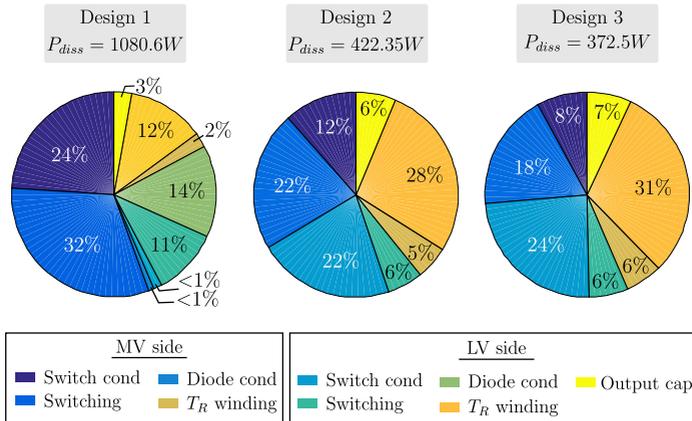


Fig. 4.29: Flowchart of the implemented algorithm used for the QAB design.



**Fig. 4.30:** Results from the multi-objective optimization design algorithm: theoretical efficiency of the QAB versus its cost for different designs.



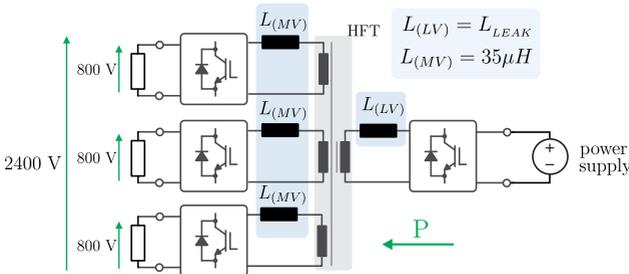
**Fig. 4.31:** Losses distribution on the main devices for the three designs highlighted: (a) lowest cost, (b) best cost-efficiency trade-off, (c) highest efficiency.

### 4.4.5 Power Stage Hardware Implementation

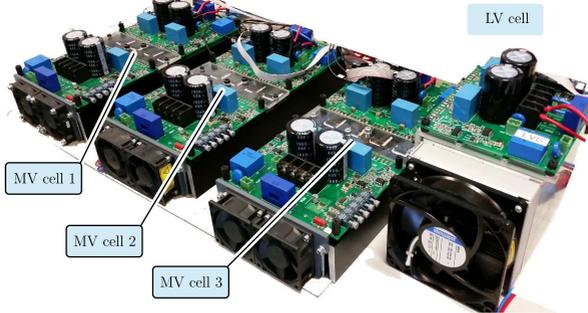
In order to evaluate the converter performance experimentally and verify the validity of the presented design procedure, a prototype was built and tested.

From the previous design methodology, the QAB converter presents the best cost for the design (1) and the best cost-benefits for the design (2), (see Fig. 4.30). Therefore, both combination are used on the construction and test of the prototype, in order to verify the accuracy of the theoretical analysis obtained from the design, as well as to evaluate experimentally the performance of the converter with different semiconductors technologies.

The imperfect construction of the transformer might causes deviation of the leakage inductance values of the MV side windings, i.e.  $L_{b_{leak}} \neq L_{c_{leak}} \neq L_{D_{leak}}$ . To reduce this effect, external inductor should be used on the MV side, resulting in  $L_{(b,c,d)} = L_{(b,c,d)_{leak}} + L_{ext}$ . To reach the desired inductance value of  $75\mu H$  seen by the LV side, three additional inductors of  $35\mu H$  are used in MV side (resulting in  $35\mu H/3 = 11.6\mu H$  seen by the LV side). These additional inductors associated to the leakage inductance of the HFT result in the desired inductance value. Fig. 4.32 shows the block diagram of the schematic used to test the converter. For simplicity's sake, the converter was tested with reverse power flow, where a single DC power supply was used on the LV side and three loads were connected to the MV side. Fig. 4.33 shows the picture of the prototype, where the cells of the CHB associated to the QAB converter are observed, sharing the same cooling system.



**Fig. 4.32:** Scheme of the tested prototype, presenting its connection to the loads and source.



**Fig. 4.33:** Picture of the implemented 20 kW QAB converter hardware prototype

#### 4.4.6 Experimental Results

The experimental results were obtained for the converter operating in steady-state with balanced power, i.e. equal power processed by the MV cells, as well as for unbalanced condition, where the main waveforms were saved. Additionally, the efficiency curve of the QAB is obtained and discussed, when Si-IGBT (design 1) and SiC-MOSFETs (design 2) are used. The results are summarized in Fig. 4.34 to Fig. 4.43.

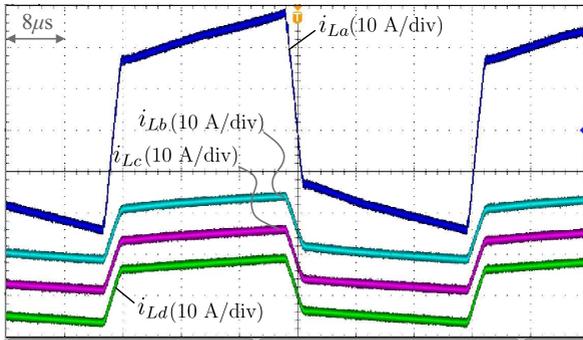
##### ► Power balanced operation

The results were firstly obtained with the converter operating in steady-state, power balance and nominal load condition.

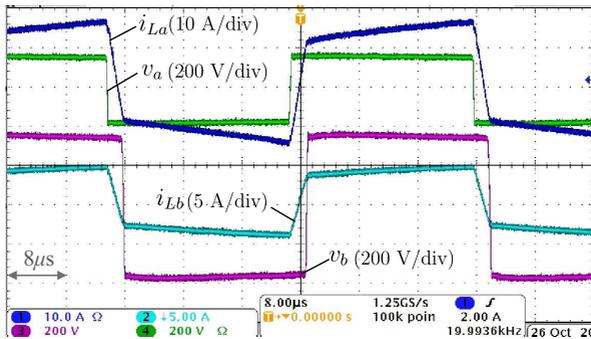
Fig. 4.34 shows the currents on the LV cell ( $i_{La}$ ) and MV cells ( $i_{Lb}$ ,  $i_{Lc}$ ,  $i_{Ld}$ ). In this result, the balanced operation of the QAB converter is noticed, where each MV cell processes the same amount of power.

Similarly, Fig. 4.35 shows voltage and current on the AC side of the MV bridge ( $v_{Lb}$  and  $i_{Lb}$ ) and LV bridge ( $v_{La}$  and  $i_{La}$ ), where the phase shift operation between these bridges is observed. These waveforms are in accordance with the theoretical one shown in Fig. 4.13.

The commutation of the switches for the LV and MV sides are presented from Fig. 4.36 to Fig. 4.39. Fig. 4.36 shows the current and voltage on the LV side semiconductor ( $s_{1a}$ ), where soft-switching operation is verified. The detail of the current and voltage waveforms during the commutation of this switch is illustrated in Fig. 4.37. As expected, the semiconductor turns on in ZVS and turns off under hard-switching.



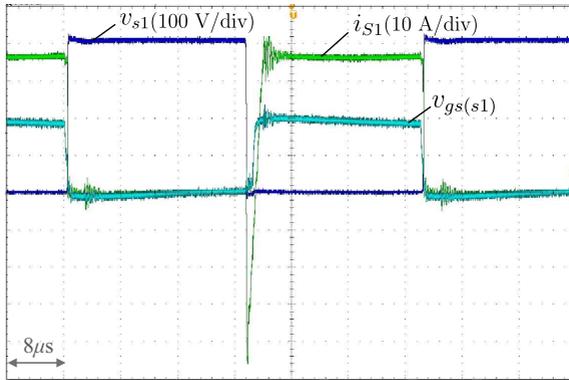
**Fig. 4.34:** Experimental results: inductor current waveforms on the LV side ( $i_{La}$ ) and MV side ( $i_{Lb}$ ,  $i_{Lc}$  and  $i_{Ld}$ ) of the QAB converter.



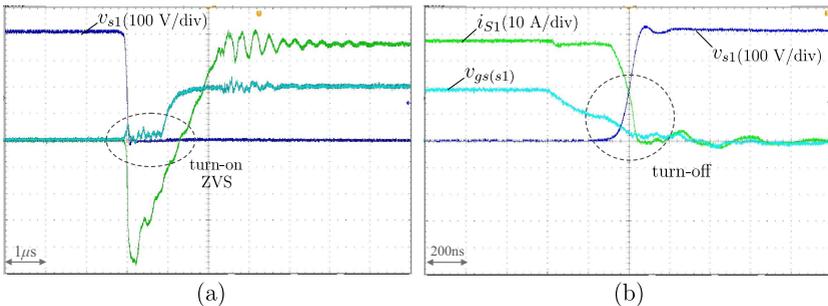
**Fig. 4.35:** Voltage and current waveforms on the LV side ( $v_{La}$ ,  $i_{La}$ ) and MV side of the QAB ( $v_{Lb}$ ,  $i_{Lb}$ ) converter.

However, the constant current imposed by the inductance during the dead-time of the switches discharges the output capacitance of the switch ( $s_{1a}$ ), while charges the capacitance of the respective switch of the leg, (i.e.  $s_{2a}$ ), implying in a commutation losses reduction (almost ZVS operation). This feature is obtained only when SiC-MOSFETs are used. This phenomenon can be seen in Fig. Fig. 4.37 (b).

Likewise, the current and voltage on the MV side semiconductor ( $s_{1b}$ ) are illustrated in Fig. 4.38, while the detail of the current and voltage waveforms are depicted in Fig. 4.39. The same effect described for  $s_{1a}$  is also observed in the MV side switch  $s_{1b}$ .

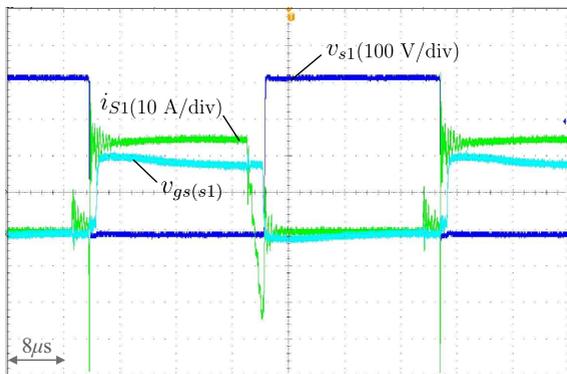


**Fig. 4.36:** Commutation of the LV side semiconductor ( $s_{1a}$ ).

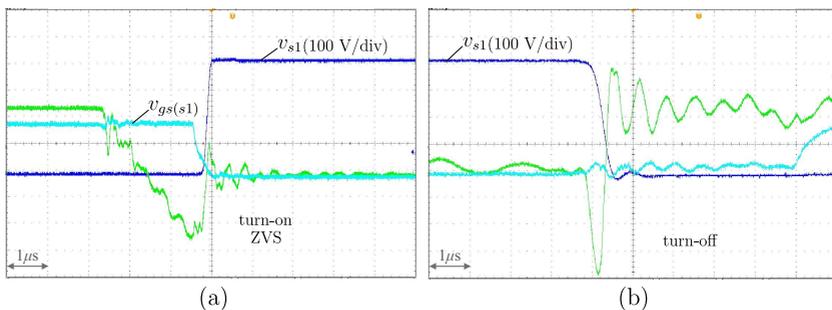


**Fig. 4.37:** Detail of the commutation of the LV side semiconductor ( $s_{1a}$ ): (a) turn on and (b) turn off of the semiconductor.

To verify the soft-switching operation of the QAB converter for different power range, the commutation of the LV side semiconductors were evaluated during the light load operation of the converter. The current and voltage waveforms were saved in this operation condition and this result is illustrated in Fig. 4.40. The detail of the commutation is presented in Fig. 4.41. The total power transferred in this condition is around 2.5 kW, i.e. around 13% of the nominal power. As can be observed in this figure, the soft-switching operation is still achieved in this condition. This result was already expected, since the input and output voltages are constant and the soft-switching should be achieved for the entire range of load.



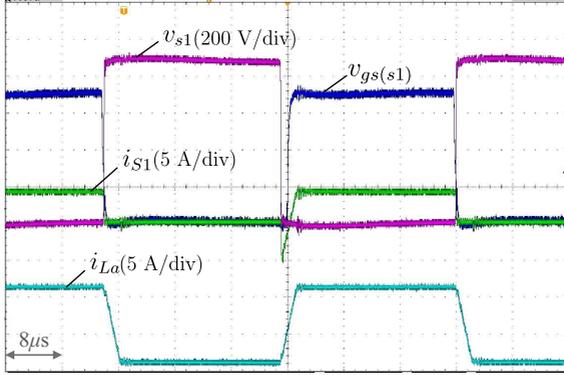
**Fig. 4.38:** Commutation of the MV side semiconductor ( $s_{1b}$ ).



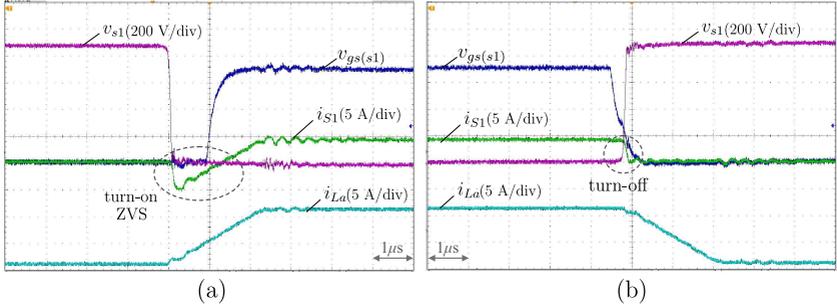
**Fig. 4.39:** Detail of the commutation of the MV side semiconductor ( $s_{1b}$ ): (a) turn on and (b) turn off of the semiconductor.

### ► Efficiency Evaluation

The efficiency curve as a function of the output power is shown in Fig. 4.42. This curve was obtained experimentally using the high precision power analyzer WT1800 from Yokogawa (basic power accuracy of 0.02%). As can be seen, the converter has achieved a peak efficiency of 94.28% at a power level of around 8 kW, when IGBT are used (design 1), while at nominal load the converter has achieved around 93.4% of efficiency. For the design 3 (using SiC-MOSFETs), the converter has achieved a peak efficiency of 97.5% at 8.5 kW of output power, and an efficiency of 97% at nominal load. It is a remarkable result, since the maximum efficiency reported in previous works for this kind of con-



**Fig. 4.40:** Commutation of the LV side semiconductor ( $s_{1a}$ ), considering light load operation of the converter.



**Fig. 4.41:** Detail of the commutation of the LV side semiconductor ( $s_{1a}$ ), considering light load operation of the converter.: (a) turn on and (b) turn off of the semiconductor.

verter was around 92% [86,91]. Consequently, the efficiency presented in this work can be considered the highest obtained so far for the MAB converter. It testifies the high performance of such converter, enabling its application in ST system.

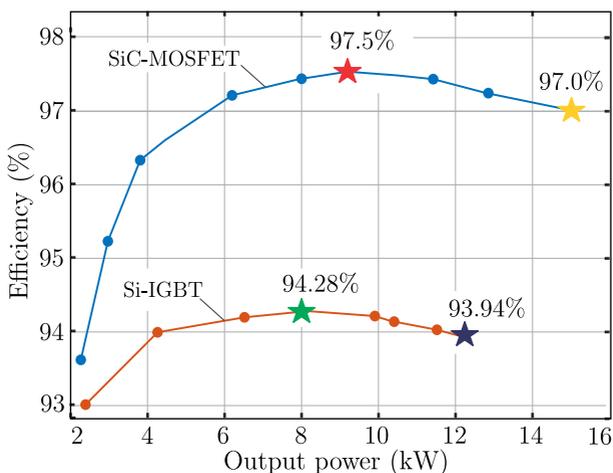
Comparing the semiconductor technologies, the use of SiC-MOSFETs results in a losses reduction of 57% at 8 kW (increasing the efficiency in 3.3%) and a losses reduction of 56.1% at 12 kW (increasing the efficiency in 3%). These results confirmed the optimum design of the converter, as well as the high potential of the SiC technology in this

application.

► **Power unbalanced operation**

As described in Chapter 1 and 2 of this thesis, the HEART project intends to improve the system's lifetime by means of the power routing technique explained in [48]. To so do, the selected ST architectures must allow the implementation of such technique efficiently. According to this technique, the lifetime of a power converter is seriously deteriorated by the high operation temperature, which is related to the power processed by it. It means that reduction of the converter's power level implies in temperature reduction and lifetime extension. Starting from the premises that the temperature can be measured and the age of the individual modules can be estimated through an advanced prognostic system, the control system can then take the decision to reduce or increase the power processed by a specific module, according to its lifetime. As the modular ST architecture is composed by several module, the most aged modules should process less power, while the less aged ones should process more power, in order to maintain the required output power. More detail is described in [48].

To enable the implementation of such technique in the ST, assuming



**Fig. 4.42:** Efficiency curve as a function of the output power of the converter obtained experimentally when SiC and IGBT are used.

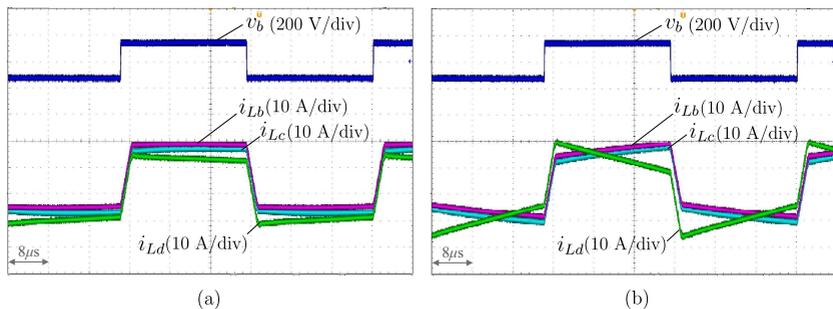
that the QAB is used as the basic cell, the QAB converter must be able to process different amount of power in their MV cells. Consequently, this operation condition is evaluated next.

An unbalanced operation was forced, where the MV bridges were subjected to different power levels. The result is presented in Fig. 4.43, where the voltage on the MV cell ( $v_{Lb}$ ) and three MV cell currents ( $i_{Lb}$ ,  $i_{Lc}$ ,  $i_{Ld}$ ) are presented for balanced (Fig. 4.43 (a)) and unbalanced (Fig. 4.43 (b)) power. As can be noticed, the unbalanced power condition distorts the current shape, but the soft-switching features is not affected.

### Summary

The MAB converter can offer a valuable trade-off between cost and efficiency when used as a basic module of the ST system. Besides cost and efficiency, this converter has enough degree of freedom to control the currents and voltages, contributing to enhance the stability of the overall system. Multiples functionalities can be implemented in the ST if the QAB is used as a basic module with proper control strategies. In this sense, this converter has been analyzed and designed in this chapter.

The MAB can have several operation modes, according to the power flow direction and voltage level of each bridge, making its general analysis very extensive. On the other hand, in ST application, the MAB has restricted operation modes with regard to the voltage level, power



**Fig. 4.43:** Main voltage ( $v_{Lb}$ ) and currents ( $i_{Lb}$ ,  $i_{Lc}$  and  $i_{Ld}$ ) MV side waveforms of the QAB obtained experimentally for: (a) balanced and (b) unbalanced power conditions.

flow, etc. Then, its analysis is simplified and it becomes very similar to the DAB converter's analysis. Then, the DAB converter is analyzed first and the possible modulation strategies are presented. Among them, the PSM and the TCM modulation are highlighted. For this reason, the MAB converter operating with both modulation strategies is analyzed and compared. The TCM was extended to the MAB converter for the first time, as an additional contribution of this work, where the theoretical analysis was presented. Comparing both modulation strategies, the PSM offers more advantages for the MAB used in ST application, because it provides reduced current stresses on the semiconductors, inductors and transformer. In contrast to the TCM, the PSM is also simpler to implement and the soft-switching features does not depend on the converter parameters, as the inductance for instance. For these reason, the PSM should be adopted for QAB converter in ST application.

To design the converter for reaching high efficiency with acceptable cost, a multi-objective optimization algorithm was developed. The losses on the components were modeled and a database with the cost and electric characteristics of each component was created. The algorithm combines these parameters in order to find the optimum point for cost, efficiency and the best trade-off between them. Besides that, SiC-MOSFETs and Si-IGBT were considered on the design of the converter. Using the parameters calculated during the design, a 20 kW prototype was build and tested. The experiments have shown an outstanding efficiency result of 97.5%, which is the highest obtained so far for this kind of converter. It testifies the high performance of such converter, enabling its application in ST system. Furthermore, the effectiveness of the proposed design is demonstrated, since the analytical and experimental efficiency values have a good agreement.

Regarding the converter's performance with different semiconductors technology, it was verified that the SiC-MOSFETs is more advantageous, due to its low energy losses, almost ZVS operation (during the switch turn-off) and the conduction of the reverse current through the channel, instead the diode, reducing the conduction losses. Consequently, the use of SiC-MOSFETs reduced the converter's losses in around 57%, compared to the IGBT. These results demonstrate the feasibility of this technology is such application.

## Chapter 5

# Smart Transformer Architecture Design

**T**HE numerous options of power converters and parameters involved in the ST architecture make its optimum design an ambitious goal. A deep analysis must be carried out from component level, going on through converter level, up to system level. In Chapter 2, the topologies have been discussed and analyzed. Among several options, the CHB is selected for the MV side of the ST, while the MAB and SRC have been highlighted. Beside the topologies choice, analysis and design of the MAB and SRC converters, including their components, have been presented in Chapter 3 and Chapter 4, respectively. In those chapters, the design from the component level up to converter level was carried out, where modulation and operation modes, optimum parameters selection and components selection of the converters have been presented. Therefore, in the current chapter, the ST architecture will be analyzed and discussed from the system level perspective. The analysis and design of the CHB is presented herein and the optimum number of modules is derived. Furthermore, different ST configurations based on MAB converter are analyzed and compared in terms of cost and performance.

## 5.1 Trade-off: Number of Modules versus Semiconductor Blocking voltage

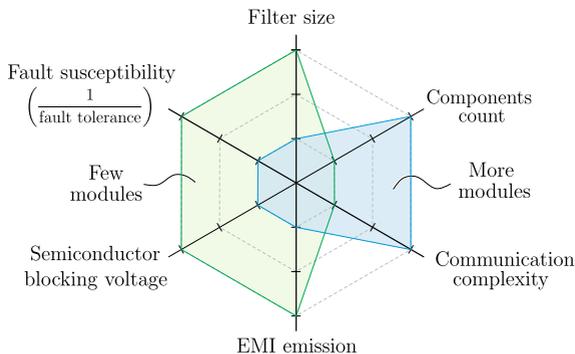
The number of modules or the semiconductor voltage rating of the MV side is one degree of freedom during the ST design. Once one is selected, the other is automatically determined. Nevertheless, this decision has a crucial impact on the system's performance and cost, and therefore the optimum number of modules is still questionable. In the modular approach, the modules share the voltage of the MV side among them, and the voltage over each module and their semiconductors are determined considering the number of modules and the total MVDC link voltage. Indeed, the number of modules is selected from the MV side viewpoint.

Currently, the IGBT devices commercially available have blocking voltage in the range of 1.2 kV to 6.5 kV. Normally, around 60% of the blocking voltage rating of the device can be utilized, to avoid the cosmic-ray induced failures. It means that using this sort of device, the maximum module voltage is 3.9 kV (when 6.5 kV IGBTs are used), demanding at least three modules to share properly the MVDC, in case of grid voltage of 10 kV. The usual ST specification has been presented in Chapter 2, and it is presented again in Table 5.1. Considering the power and voltage levels involved in the power conversion, the resulting current on the MV side is relative low, i.e. around 40 A to 100 A. In fact, IGBT with current rating in the range of 75 A to 150 A can be surely adopted. Nonetheless, most of the HV IGBT commercially available (i.e. those with blocking voltage rating above 1.7 kV) are rated for higher current, implying in over-design, and they are costly. In contrast, the low voltage rating IGBTs (up to 1.7 kV) have lower cost, better performance and provides wide range of options.

Besides the semiconductor blocking voltage, the choice of the number of modules is constrained by fault tolerance capability, the system complexity, the number of components, and the rated power of the modules. All these parameters influence the cost, reliability, efficiency, and system complexity. On one hand, if a large number of modules is selected, lower blocking voltage semiconductors can be used in the MV side and there is more degree of freedom to implement fault tolerance schemes, contributing for increasing the system's availability. Furthermore, in virtue of the larger number of levels, the filter size and EMI emission are reduced. On the other hand, the total number of parts (in-

**Tab. 5.1:** Electric distribution grid specification of different countries

Country	MV grid (kV)	Config	LV grid (V)	Rated power (MVA)	Grid freq (Hz)
Germany	10	3 wires	400	1	50
USA	12.47	4 wires	120	8.6	60
China	10	3 wires	380	2	50
Japan	6.6	3 wires	400	1	60/50
Brazil	13.8	3 wires	380	3	60



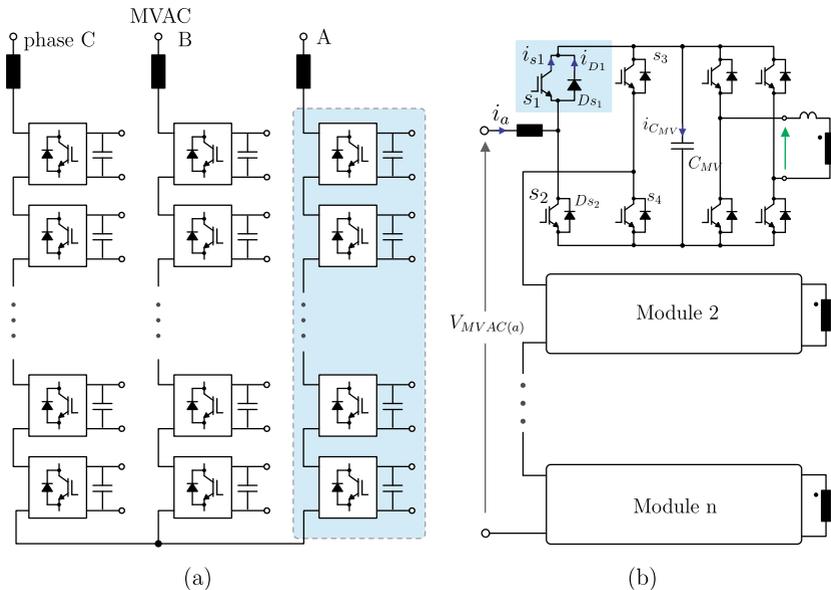
**Fig. 5.1:** Evaluation of the selection of the number of modules on the system's parameters.

cluding the auxiliary power supply, drivers, and communication) and system complexity related to the communication system between the several cells increase considerably. Fig. 5.1 shows how the number of modules affects the main parameters of the ST system.

In order to establish the optimum number of modules, the ST architecture is analyzed and designed from the system level viewpoint, where the losses and cost are computed considering different number of modules. As the selection of the number of modules is carried out from the MV side, the CHB and the DC-DC converter must be analyzed, in order to derive the convenient equations to determine the main components and calculate their losses. The DC-DC converters have been already analyzed in the previous chapter and the CHB is analyzed next.

## 5.2 Cascaded H-Bridge Converter Analysis

The CHB converter is implemented by series connection of the H-bridge cells, as presented in Fig. 5.2. It is responsible for converting the MVAC in DC, that are split among their modules. Hence, there is no single MVDC link in this topology, but several LV DC links connected to the DC-DC converters. In this work, the sum of the individual DC link voltages per phase is defined as the total MVDC link of the CHB, as a matter of nomenclature. Then, the CHB is in charge to control the input current (controlling the active and reactive power exchanged with the grid), the total MVDC link, as well as the individual MVDC link. For the sake of the star connection between the phases, the total MVDC link is calculated considering the line-to-neutral voltage of the grid. It offers advantages, because less modules can be used, for a given semiconductor voltage rating, as discussed later. To modulate the



**Fig. 5.2:** Topology of the three-phase CHB converter and the detail implementation of the module, including the DC-DC converter.

converter, many different strategies can be adopted, but the phase-shift offers more benefits [56–60, 64] with respect to the losses distribution on the semiconductors and AC filter size reduction. Furthermore, the operation and control scheme is very simple when this modulation is employed.

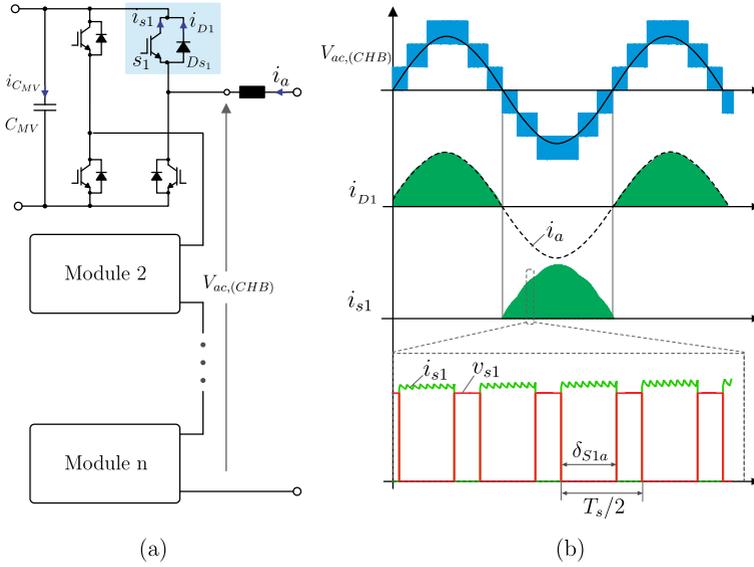
The converter has been investigated and analyzed in previous works [64, 66]. In addition, a brief analysis was presented in Chapter 2, where the requirement to select the capacitors was introduced. Then, the aim of this section is to design the CHB considering the ST specification, and identify and select the optimum parameters to maximize the performance, while reducing cost. Therefore, the existing analysis is used as a basis of this work [64, 66]. For the analysis, it is considered the unit power factor and power flowing from the AC to DC side, as represented in Fig. 5.2 and Fig. 5.3. Consequently, the grid voltage and current are defined by (5.1) and (5.2), respectively. To size the components and compute their losses, the current stress on the main power components are computed in function of the main parameters of the converter. The main waveforms of the converter are depicted in Fig. 5.3, and they are used to calculate the current stresses on the semiconductors.

$$\begin{cases} v_a(t) = V_{a(pk)} \cdot \sin(\omega t) \\ v_b(t) = V_{b(pk)} \cdot \sin(\omega t - 3\pi/2) \\ v_c(t) = V_{c(pk)} \cdot \sin(\omega t + 3\pi/2) \end{cases} \quad (5.1)$$

$$\begin{cases} i_a(t) = I_{a(pk)} \cdot \sin(\omega t) \\ i_b(t) = I_{b(pk)} \cdot \sin(\omega t - 3\pi/2) \\ i_c(t) = I_{c(pk)} \cdot \sin(\omega t + 3\pi/2) \end{cases} \quad (5.2)$$

### 5.2.1 Semiconductors Design

The instantaneous current through the semiconductor  $s_1$  can be calculated by (5.3), where  $\delta_{S1}$  is the switching function of the semiconductor and  $i_a(t)$  is the grid current, as defined in Fig. 5.3. The switching function represents the switching state of the semiconductor, i.e.  $\delta_{S1} = 1$  when the switch is on, and  $\delta_{S1} = 0$ , when the switch is off.



**Fig. 5.3:** (a) Equivalent single phase topology of the CHB used for the analysis and (b) its main waveforms.

$$i_{s1}(t) = \delta_{s1} i_a(t) \quad (5.3)$$

Applying the local average value definition in the switching function during one switching period, the duty-cycle of the semiconductor  $s_1$  is determined and given by  $d_{s1} = \langle \delta_{s1} \rangle_{T_s}$ . The duty-cycle of each leg of the converter is calculated by (5.4), considering the grid period and the three-phase system. In this equation,  $m$  is the modulation index and  $d_0$  is the zero sequence component of the three-phase system.

$$\begin{cases} d_a(t) = m [\sin(\omega t) + d_o] \\ d_b(t) = m [\sin(\omega t - 3\pi/2) + d_o] \\ d_c(t) = m [\sin(\omega t + 3\pi/2) + d_o] \end{cases} \quad (5.4)$$

The average current through the semiconductor  $s_1$  for one grid period is calculated by the mean value definition presented in (5.5), while the rms value is calculate by (5.6).

$$I_{S1(avg)} = \frac{1}{2\pi} \int_0^{2\pi} d_{S1} i_a(t) dt \quad (5.5)$$

$$I_{S1(rms)} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} [d_{S1} i_a(t)]^2 dt} \quad (5.6)$$

In these equations,  $d_{S1}$  represents the duty-cycle of the switch  $s_1$ , but only when the channel is conducting, while  $d_{D1}$  represents the conduction through the diode. Both duty-cycles can be rewritten in terms of duty-cycle of the leg, as presented in (5.7) and (5.8).

$$d_{S1} = \begin{cases} d_a(t) & 0 < \omega t < \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \quad (5.7)$$

$$d_{D1} = \begin{cases} 1 - d_a(t) & 0 < \omega t < \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \quad (5.8)$$

Thus, replacing (5.7) in (5.5) and (5.6), the average and rms values of the current on the switch  $s_1$  are obtained, as presented in (5.9) and (5.10), respectively.

$$I_{S1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} - \frac{m}{8} \right) \quad (5.9)$$

$$I_{S1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} - \frac{m}{3\pi}} \quad (5.10)$$

Similarly, the average and rms current on the diode  $D_1$  are calculated by (5.11) and (5.12), respectively.

$$I_{D1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} + \frac{m}{8} \right) \quad (5.11)$$

$$I_{D1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} + \frac{m}{3\pi}} \quad (5.12)$$

Then, the current stresses on the semiconductors are summarized in Table 5.2, considering unit power factor, and positive and negative power flow cases.

**Tab. 5.2:** Current stresses on the CHB converter

	Direct power flow	Reverse power flow
Channel current		
avg	$I_{S1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} - \frac{m}{8} \right)$	$I_{S1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} - \frac{m}{8} \right)$
rms	$I_{S1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} - \frac{m}{3\pi}}$	$I_{S1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} - \frac{M}{3\pi}}$
Diode current		
avg	$I_{D1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} + \frac{m}{8} \right)$	$I_{D1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} + \frac{m}{8} \right)$
rms	$I_{D1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} + \frac{m}{3\pi}}$	$I_{D1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} + \frac{m}{3\pi}}$

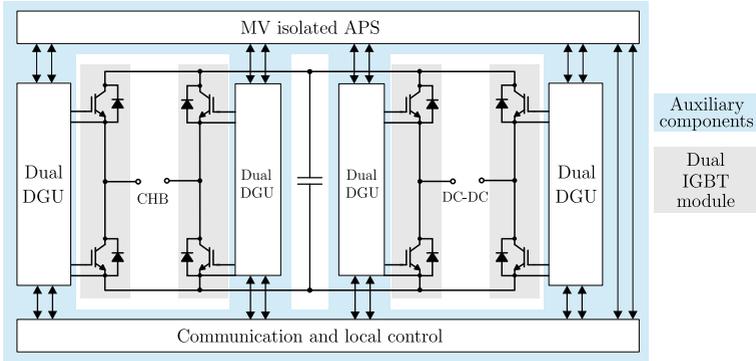
### 5.2.2 Capacitor Sizing

As discussed in Chapter 2, the most severe criteria that must be attended during the capacitor sizing is concern to the oscillating instantaneous power resulted by the sinusoidal voltage and current multiplication, implying in a  $2^{nd}$  order harmonic. Thus, using the amount of energy associated with the instantaneous power oscillation, the capacitance is calculated by (5.13), where  $S$  is the total apparent power of the CHB converter [65, 66].

$$C_{min} = \frac{S}{f_s (V_C \Delta V_C - \Delta V_C^2)} \quad (5.13)$$

## 5.3 Optimum Number of Modules

To define the optimum number of modules per phase of the ST, the system is analyzed from the MV side, where the losses and cost of the components are computed. The MV side module is composed by the CHB cell and the primary side bridge of the DC-DC converter, as shown



**Fig. 5.4:** Implementation of the MV side of the power unit, including the components considered on the cost analysis of the module.

in Fig. 5.2 (b). The implementation of such module is presented in Fig. 5.4, where auxiliary components, like gate driver unit (GDU), auxiliary power supply (APS) and communication and local control unit (CCU) are included. Despite these elements do not contribute to the system losses, they play an important role in the system's cost, mainly when many modules are used. Therefore, 4 dual GDU, 1 CCU and 1 APS, used to feed all the auxiliary peripherals of the module, are considered in each MV module, as illustrated in Fig. 5.4. The module comprises as the main power devices 8 power semiconductors and the capacitor bank, which are responsible for the system losses and the majority of the cost. Thus, their losses are modeled according to the number of modules and their cost are calculated from the system perspective. Finally, a single heatsink for each module is considered<sup>7</sup>, which increases also significantly the cost. For the aforementioned reasons, each of these described items are analyzed and discussed during the selection of the optimum number of modules.

Regardless of the adopted DC-DC converter (either MAB or SRC), the module implementation shown in Fig. 5.4 remains the same, as well as its cost. In this analysis, the MAB converter is used as the DC-DC stage, because of its higher control performance and economic benefits, that will be discussed later in this chapter.

<sup>7</sup>All semiconductors of the MV module (including those from CHB and DC-DC stage) are attached to the same heatsink.

**Tab. 5.3:** IGBT devices considered during the analysis of the optimum number of modules - HV IGBT

6500 V							
PN	I (A)	Cost (\$USD)	$V_{CE(on)}$ (V)	$E_{on/off}$ (mJ)	$t_{d(on)}/t_r$ (ns)	$t_{d(off)}/t_f$ (ns)	$V_f$ (V)
QID6508001	85	689	5.6	460/500	-	-	4.2
4500 V							
PN	I	Cost	$V_{CE(on)}$	$E_{on/off}$	$t_{d(on)}/t_r$	$t_{d(off)}/t_f$	$V_f$
QID4515001	150	740	4	600/450	1500/500	3500/1200	5.6
3300 V							
PN	I	Cost	$V_{CE(on)}$	$E_{on/off}$	$t_{d(on)}/t_r$	$t_{d(off)}/t_f$	$V_f$
QID3310006	100	539	4	250/180	800/160	3200/1300	2.55
QID3310006	200	410	4	335/ 275	800/160	3200/1300	2.55

**Tab. 5.4:** IGBT devices considered during the analysis of the optimum number of modules - LV IGBT

1700 V							
PN	I	Cost	$V_{CE(on)}$	$E_{on/off}$	$t_{d(on)}/t_r$	$t_{d(off)}/t_f$	$V_f$
CM75DY-34A	75	119	2.15	20/34	200/150	550/350	3
CM150DX-34SA	150	147	2.15	26/46	400/100	700/600	2.7
CM200DX-34SA	200	174	2.15	28/56	400/100	700/600	2.7
CM300DX-34SA	200	242	2.15	48/76	500/100	800/600	2.7
1200 V							
PN	I	Cost	$V_{CE(on)}$	$E_{on/off}$	$t_{d(on)}/t_r$	$t_{d(off)}/t_f$	$V_f$
CM75DU-24F	75	98.55	1.9	-	100/50	400/300	3.2
CM100DU-24H	100	99	2.85	-	100/200	300/350	3.2
CM150DY-24A	150	141	2.4	-	130/100	450/350	3.8
CM200DX-24S	200	145	2	30.7/21.5	800/200	600/300	1.7
CM300DX-24S1	300	138	2	26.7/35.7	800/200	600/300	2

**Tab. 5.5:** SiC MOSFETs considered during the analysis of the optimum number of modules

1700 V							
PN	I (A)	Cost (\$USD)	$R_{DS(on)}$ (V)	$E_{on/off}$ (mJ)	$t_{d(on)}/t_r$ (ns)	$t_{d(off)}/t_f$ (ns)	$V_f$ (V)
C2M0045170D	72	76	90	2.1/0.86	65/20	48/18	3.6
1200 V							
PN	I	Cost	$V_{CE(on)}$	$E_{on/off}$	$t_{d(on)}/t_r$	$t_{d(off)}/t_f$	$V_f$
C2M0025120D	90	61	43	1.4/0.3	14/32	29/28	3.1
C2M0040120D	60	29	84	1/0.4	15/52	26/34	3.1
C2M0080120D	40	14.55	208	-	12/18.4	23.3/13.6	3.1

### 5.3.1 Power Semiconductors

The number of modules defines the blocking voltage rating of the semiconductors employed on the MV side and the power device can be selected based on the blocking voltage criteria. Considering an voltage utilization factor of  $k_u = 0.6$ , i.e. 60% utilization of the blocking voltage rating of the IGBT, and a grid voltage of 10 kV, the required semiconductor voltage rating as a function of the number of modules is presented in Fig. 5.5 (a). As can be observed, if commercial devices are employed, three modules or more need to be used. Otherwise, special semiconductors (as those used in [34, 37]) are required, as pointed out in Fig. 5.5 (a). On the other hand, these semiconductors are available only for research purpose, and then they are not considered in this work.

Commercial IGBT are the usual choice for this voltage level. Nevertheless, the SiC MOSFETs have been more and more applied to higher voltage, because of its high performance with reasonable price. These devices are normally rated up to 1.7 kV [105], but its great demand in higher voltage application motivated the development of higher blocking voltage devices. Currently, the *WolfSpeed/CREE* company has developed a 3.3 kV SiC MOSFETs, which is in test phase [103, 105], and it is about to be launched. Consequently, this sort of semiconductors are very suitable for ST application, as demonstrated in chapters 3 and 4, and they are highlighted in Fig. 5.5 (a).

To determine the optimum number of modules, an investigation taking the cost and performance into account is realized. To do so, IGBT from the market leader *Powerex Power Semiconductor/Mitsubishi Power Semiconductors*, as well as SiC MOSFETs from *WolfSpeed/CREE*, also market leader in this segment, are considered. The devices used in this analysis are presented in Table 5.3 and Table 5.5. The precise cost estimation is very difficult to be obtained, because it is highly dependent on the market aspects, that can change the price over the time, like: distributor, quantity acquired, etc. An approach correlating the semiconductor cost with the chip size has been presented in [140, 141]. It is very valid for comparison purpose, although the value does not match the market price. Conversely, the price obtained directly from the manufacture or distributor, would offer a more realistic view of the system cost. Therefore, the last approach is used in this work, where the price of the IGBTs were acquired directly from the manufacture (i.e. *Powerex Power Semiconductor*), while the SiC MOSFETs price were

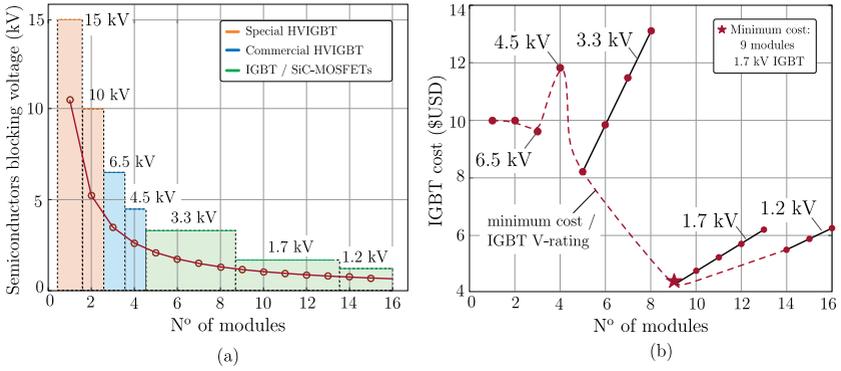
collected from the well-known distributor *Mouser Electronics* (considering 1k pieces). The semiconductors prices are presented from Table 5.3 to Table 5.5. Although the values might differ from those obtained from companies, it is still valid for comparison purpose.

Considering the required semiconductor device for a given number of modules, as show in Fig. 5.5 (a), and using the prices provided in Table 5.3, the total cost of the IGBTs for the whole ST architecture is estimated as a function of the number of modules as a first analysis, and it is shown in Fig. 5.5 (b). The lowest cost is archived when 9 modules are adopted, in which 72 semiconductors with blocking voltage of 1.7 kV are required. Although a significant amount of devices are used, the cost of the 1.7 kV IGBT is considerably low. As a matter of fact, the IGBT cost has a substantial increment according to its voltage rating (considering the same current rating), while it increases slightly according to the current rating (for the same voltage rating). This is presented in Fig. 5.6 (b), where the values from Table 5.3 were used to plot this graphic. Consequently, high voltage IGBTs implies in greater cost. This cost behavior is not established by the technology manufacturing process, but also by the market aspects. The Fig. 5.6 (a) shows the cost of the semiconductors of the ST system in function of the number of modules, when different semiconductors technologies (not only IGBT) are used. Three main cases are plotted in this graphic: IGBT adopted in both MV and LV side, SiC MOSFETs adopted in the LV side and IGBT in the MV side, and finally SiC MOSFETs used in both LV and MV sides. For every case, the minimum cost is obtained for a system comprised by 9 modules.

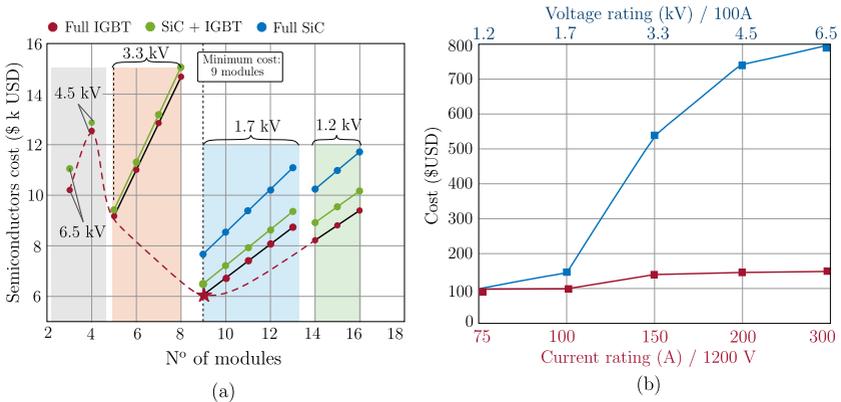
The main equations to determine the components of the CHB converter have been derived in previous section, while the equations of the DC-DC converter have been presented in Chapter 4. Using them, the converters can be designed and their losses estimated. These equations are summarized again in Table 5.7 and Table 5.8.

### 5.3.2 Capacitor Bank Sizing

Similarly to the semiconductors, the capacitor bank is one of the most important elements on the modules and then it must be accurately designed. To define the required capacitance, equation (5.13) is used. To implement the capacitor bank, metalized electrolytic type capacitor or film type capacitor can be used. The first one is usually rated for lower



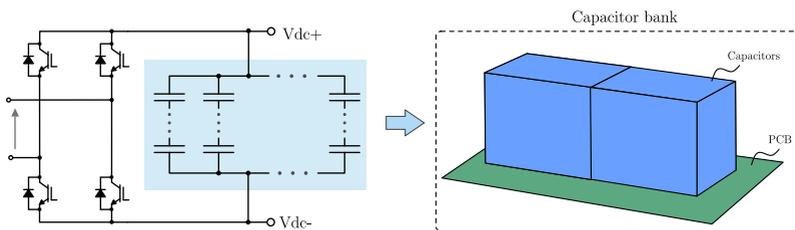
**Fig. 5.5:** (a) Required semiconductor voltage rating in function of the number of modules and (b) estimated cost of the IGBT's for the whole ST architecture in function of the number of module.



**Fig. 5.6:** (a) Estimated cost of the semiconductors (Si-IGBT and SiC-MOSFETs) for the whole ST architecture in function of the number of module and (b) cost variation of the IGBT according to the voltage rating (for a given current rating) and according to the current rating (for the same voltage rating).

**Tab. 5.6:** Capacitors considered for the analysis of the optimum number of modules

Electrolytic				
PN	V	Capacitance ( $\mu F$ )	Cost (\$USD)	$R_{SE}(m\Omega)$
B43520B5108M000	0.45	1000	26.13	15
Film				
B32778J1127K000	1.3	120	69.26	15
B25620B1227K321	1.32	220	50.99	15
B25620B1706K981	1.98	70	45.06	15
B25620B1297K983	1.98	295	109.81	15

**Fig. 5.7:** Implementation of the capacitor bank of the MVDC link: (a) circuit implementation and (b) physical implementation in the circuit.

voltage (up to 600 V) with high capacitance, while the second one has normally high voltage rating (over 1 kV), but low capacitance. Although the electrolytic capacitors have high energy density, its intrinsic resistance is very high, because of its constructive structure. Therefore, to avoid high losses, parallel devices are generally used. Among the possible options, devices from *EPCOS/TDK* were considered, which is one of the biggest company in this sector. The devices used in the analysis are presented in Table 5.6.

Initially, the required capacitance is calculated and each device from Table 5.6 is combined in parallel or series, as shown in Fig. 5.7, until reaching the required voltage and capacitance. After that, the cost and losses of the capacitor bank is calculated. The device that provides the lowest cost is chosen.

### 5.3.3 Cooling System Design

A single cooling system is used per module, where the semiconductors of the CHB and the semiconductors of the primary side of the DC-DC converter are attached to it. The air forced cooling system is used. The required volume of the heatsink is calculated in order to maintain a maximum junction temperature of the semiconductor in  $T_J = 125^\circ C$ , considering an ambient temperature of  $T_a = 50^\circ C$ . Following the procedure described in [142–145], the total thermal resistance between the junction and the heatsink surface is calculated by

$$R_{HS} = \frac{T_J - T_a}{P_{losses}}, \quad (5.14)$$

where  $P_{losses}$  is the total losses of all semiconductors attached to the heatsink. To define the required volume of the heatsink, the Cooling System Performance Index (CSPI) introduced in [142] can be applied. The CSPI characterizes the performance of a given cooling system (or heatsink profile) in terms of power dissipation capability per volume, considering a certain temperature difference. In other words, the CSPI can be understood as a volumetric thermal conductivity and it correlates the volume and the thermal resistance of the heatsink, as presented in (5.15).

$$V_{HS} = \frac{273}{CSPI \cdot R_{HS}} \quad (5.15)$$

This approach is very useful for cost and performance comparison purpose, because assuming a constant CPSI means that the cooling system performance will be the same for every number of module, and only the heatsink volume changes according to the power dissipated in each case. The cooling system cost is directly proportional to the volume, which will change considering the number of modules. As the cost and volume of the heatsink are correlated proportionally, a cooling cost constant  $K_{HS_{cost}}$  [ $USD/dm^3$ ] can be defined as

$$K_{HS_{cost}} = \frac{Cost_{HS}}{V_{HS}} \quad (5.16)$$

Using a constant value of  $K_{HS_{cost}}$  and CSPI regardless the number of module, the performance will then be constant and only the cost will change according to the number of module. As reported in [140,142], for a standard forced air cooling system, the CSPI can be assumed

as  $CSPI = 10 \text{ W}/(Kdm^3)$ . A suitable heatsink profile that can be used on the power module of the ST is the LA V 22 from *Fischer Elektronik* [146]. The cost of such heatsink profile was obtained directly from the manufacturer *Fischer Elektronik*, resulting in a  $K_{HS\text{cost}} = 0.059 [USD/dm^3]$ . Finally, the cooling system is designed for each number of modules using equations (5.14) to (5.16) and considering the value of CSPI and  $K_{HS\text{cost}}$  presented before.

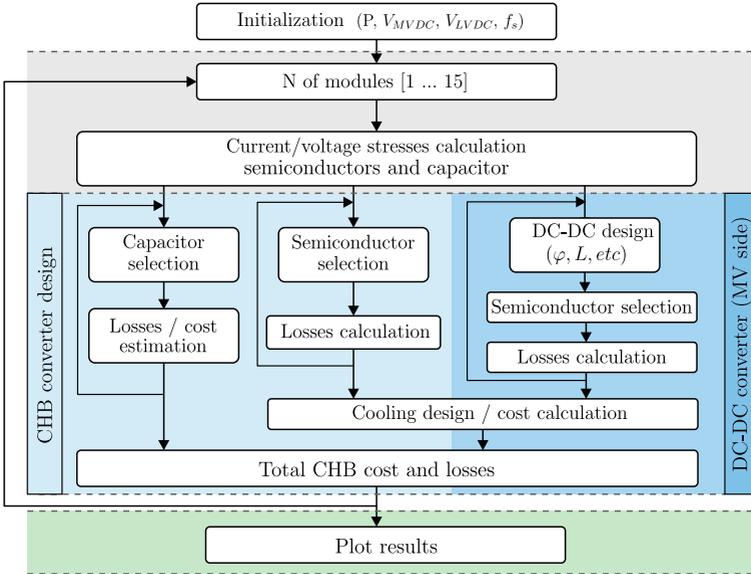
### 5.3.4 Auxiliary Components

The auxiliary components will interfere only on the cost of the system, according to the number of modules. Each module has 4 GDU, 1 APS and 1 CCU, which constant price are considered for them, independently of the voltage specification of the semiconductor or DC link voltage. For the GDU and APS, constant cost of 100 \$ USD is presumed, while 10 \$ USD for the CCU is assumed.

### 5.3.5 Optimum Number of Modules: Cost vs Performance

Taking into account of the aforementioned considerations with respect to the losses and cost calculation, a computer-aided based design is used, where an algorithm to size the components and to calculate their cost and losses was developed. The flowchart of the implemented algorithm is presented in Fig. 5.8, where the specification of the ST system presented in Table 5.1 for Germany is used. Apart from that, a switching frequency of  $f_{s(CHB)} = 5 \text{ kHz}$ , modulation index of  $m = 0.8$  and  $k_u = 0.6$  are considered for the CHB, while switching frequency of  $f_{s(dc)} = 20 \text{ kHz}$  and  $k_u = 0.6$  are assumed for the DC-DC converter.

In this algorithm, the specification of the system is provided, and it starts the design considering the lowest number of module, i.e.  $N_{mod} = 3$ . Then, the capacitor bank is designed, and the losses and cost estimated as presented in subsection 4.2. Likewise, the semiconductors are selected, while their losses and cost are estimated according to the subsection 4.1. Then, the DC-DC converter is designed, and the cost and losses are obtained. Subsequently, the cooling system is calculated according to subsection 4.3. Finally, the total losses and cost of the module are obtained and plotted, considering also the auxiliary components. Thereafter, the procedure is repeated, considering the next



**Fig. 5.8:** Flowchart of the implemented algorithm used to design the ST and estimate the losses and cost according to the number of modules.

number of module (in this case  $N_{mod} = 4$ ), until  $N_{mod} = 15$ . The design was performed considering IGBT and SiC-MOSFETs separated. First, the results obtained for IGBT are discussed and later for the SiC-MOSFETs.

As a result from the design, the cost per module is obtained and plotted as a function of the number of modules, as presented in Fig. 5.9, while the total system cost per phase versus the number of modules is plotted in Fig. 5.10. As expected, modules based on higher blocking voltage rating IGBTs are more expensive than those with lower voltage rating devices, because of the cost of the component. The only exception is detected for the 6.5 kV IGBT, which are cheaper than the 4.5 kV IGBT, mainly because of the current rating (see Table 5.3). Considering the total number of modules per phase depicted in Fig. 5.10, the optimum number with respect to the cost is  $N_{mod} = 9$ , in which 1.7 kV IGBT are used. It is explained by the low cost of the 1.7 kV, besides the reasonable quantity of modules. While the cost variation from 1.2 kV to 1.7 kV IGBT increases only slightly, the cost difference between

1.7 kV and 3.3 kV is large. In addition, many more modules are required when 1.2 KV IGBT are used, increasing the total system cost. Therefore, the minimum cost for the system is obtained when 1.7 kV

**Tab. 5.7:** Equation used for the ST architecture design

DC-DC Design	
Required inductance	$L_{eq} = \frac{V_M V_L}{2\pi f_s n (S/N_{mod})} \varphi_{nom} \left( 1 - \frac{ \varphi_{nom} }{\pi} \right)$
Peak current	$I_{L(pk)} = \frac{V_L - \sqrt{V_L^2 - 8L_{eq} f_s n (S/N_{mod})}}{4kL_{eq} f_s}$
Semiconductors current stresses - DC-DC	
Channel rms current	$I_{S5(avg)} = \frac{I_{L(pk)}}{2n} \left( 1 - \frac{3\varphi}{4\pi} \right)$
Channel avg current	$I_{S5(rms)} = \frac{I_{L(pk)}}{n} \sqrt{\frac{1}{2} \left( 1 - \frac{5\varphi}{12\pi} \right)}$
Diode rms current	$I_{D5(avg)} = \frac{I_{L(pk)}}{n} \frac{\varphi}{8\pi}$
Diode avg current	$I_{D5(rms)} = \frac{I_{L(pk)}}{n} \sqrt{\frac{\varphi}{12\pi}}$
Capacitor Bank	
Minimum capacitance	$C_{min} = \frac{S}{f_s (V_C \Delta V_C - \Delta V_C^2)}$
Semiconductors current stresses - CHB	
Channel rms current	$I_{S1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} - \frac{m}{8} \right)$
Channel avg current	$I_{S1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} - \frac{m}{3\pi}}$
Diode rms current	$I_{D1(avg)} = I_{a(pk)} \left( \frac{1}{2\pi} + \frac{m}{8} \right)$
Diode avg current	$I_{D1(rms)} = I_{a(pk)} \sqrt{\frac{1}{8} + \frac{m}{3\pi}}$

**Tab. 5.8:** Equation used for the ST architecture design and losses calculation

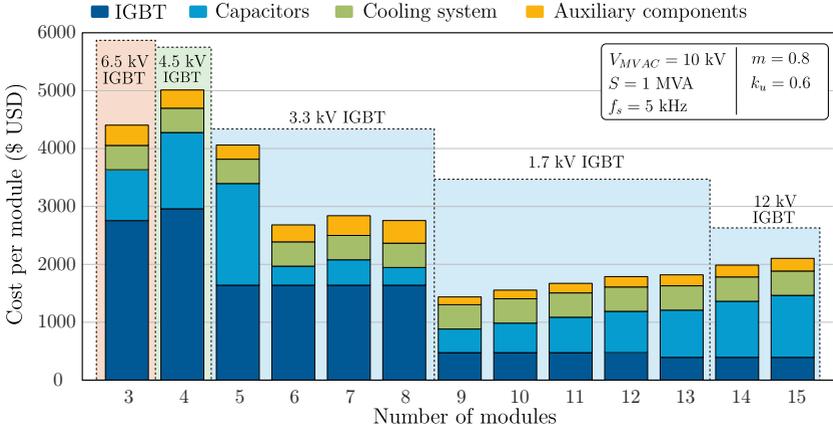
Semiconductors losses	
Cond MOSFETs	$P_{MOS(cond)} = \frac{1}{T} \int_0^T R_{ds(on)}(i_{ds}, T_J, V_{gs}) i_{ds}^2(t) dt$
Cond IGBT	$P_{IGBT(cond)} = \frac{1}{T} \int_0^T V_{CE}(i_C, T_J, V_{gs}) i_f(t) dt$
Switching losses	$P_{(sw)} = \frac{1}{T} \left( \begin{array}{c} \sum_{n=1}^{N_{sw(on)}} E_{on}(V_{ce}, I_d, T_J, V_{gs}, R_g) + \\ \sum_{n=1}^{N_{sw(off)}} E_{off}(V_{ce}, I_d, T_J, V_{gs}, R_g) \end{array} \right)$
Cooling system design	
Thermal resistance	$R_{HS} = \frac{T_J - T_a}{P_{losses}}$
Volume	$V_{HS} = \frac{273}{CSPI \cdot R_{HS}}$
Cost	$Cost_{(HS)} = K_{HS} V_{HS}$

IGBT is used in its highest blocking voltage potential, i.e.  $N_{mod} = 9$ .

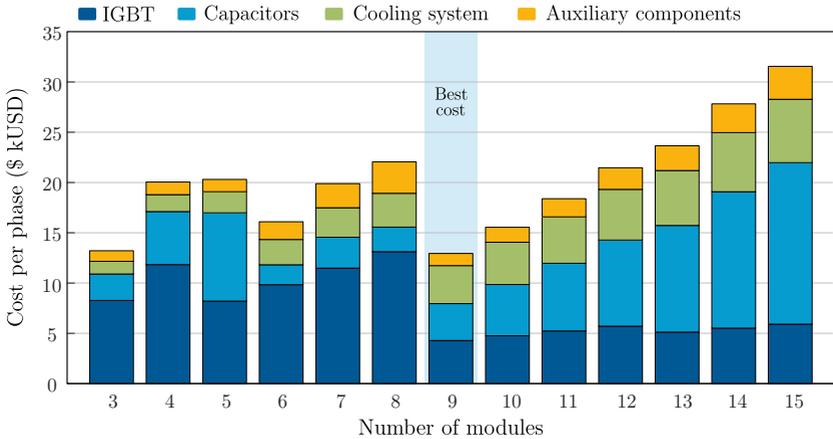
Similarly, the total losses per phase are plotted as a function of number of selected modules, as illustrated in Fig. 5.9. In this graphic, the loss distribution on the DC-DC and MV stages (i.e. the CHB) is also shown. As can be noticed, the minimum losses are obtained when  $N_{mod} = 9$  is adopted. In this case, the high performance of the 1.7 kV semiconductor contributes significantly for losses reduction. It is important to mention that the 1.2 kV IGBT has the best performance in terms of conduction and switching losses. However, when this device is adopted, many modules are required ( $N_{mod} = 14$  and  $N_{mod} = 15$ ), resulting in large amount of components in series, and therefore more losses.

The DC-DC stage is responsible for the majority of the losses, as expected. Analyzing the losses distribution, the majority of the losses is attributed to the semiconductor switching, mainly in the DC-DC stage and when higher blocking voltage IGBT are used. It is explained by the fact that high voltage rating IGBT has very large commutation energy ( $E_{on}$  and  $E_{off}$ ) and they are not supposed to be used for high switch-

ing frequency. However, the DC-DC converter operates with switching frequency of 20 kHz, leading to very high switching losses. In overall, the ST provides the best results with respect to the efficiency and cost

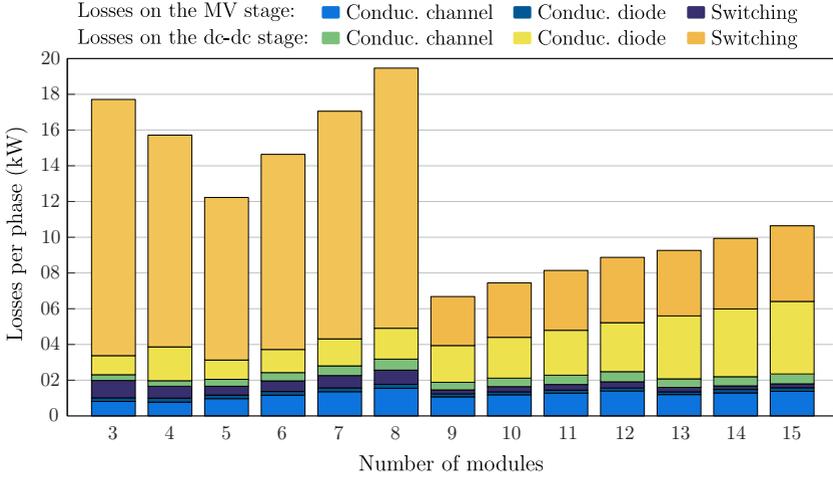


**Fig. 5.9:** Cost of the module (using Si-IGBT) according to the number of modules, highlighting the cost sharing among the components.



**Fig. 5.10:** Total implementation cost of one phase of the ST architecture (using Si-IGBT) according to the number of modules, highlighting the cost sharing among the components.

### 5.3. Optimum Number of Modules



**Fig. 5.11:** Total losses in one phase of the ST system (using Si-IGBT) and the losses distribution on the MV stage and DC-DC stage.

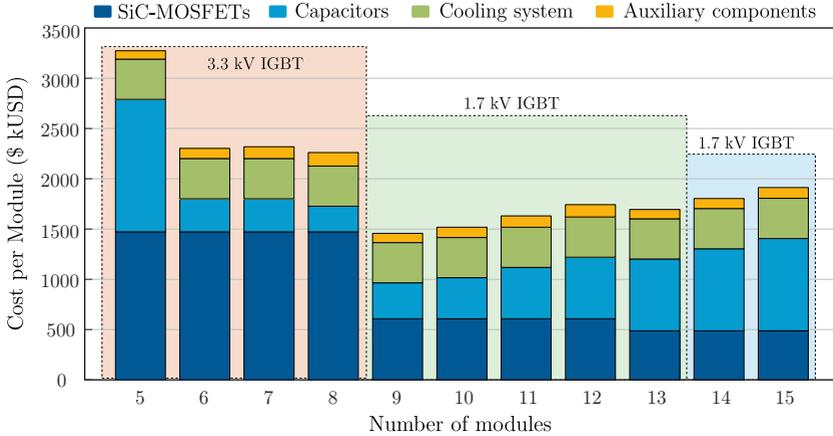
**Tab. 5.9:** Specification of the 3.3 kV SiC MOSFET from *Wolfspeed/CREE*

3300 V					
V (V)	I (A)	Cost (\$USD)	$R_{DS(on)}$ ( $m\Omega$ )	$E_{on/off}$ (mJ)	$V_f$ (V)
3300	40	3.6/A	98	25/4	4

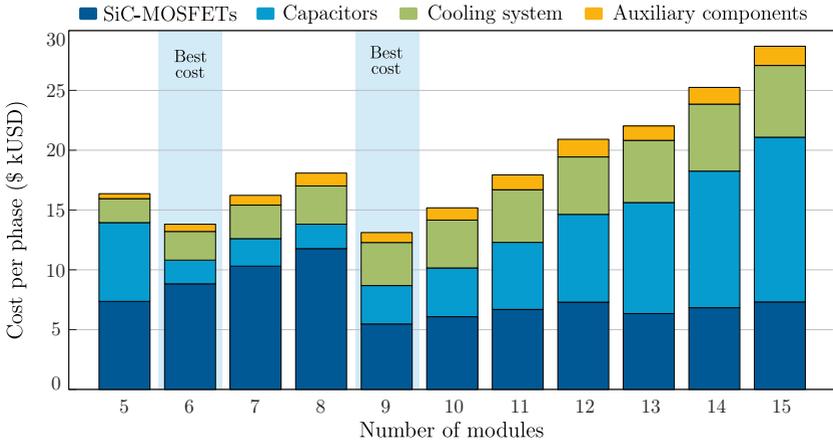
when 9 modules are adopted.

The same study has been carried out considering now SiC-MOSFETs. Devices with breakdown voltage of 1.2 kV and 1.7 kV were considered (see Table 5.5). In addition, the preliminary specification and forecast price provided by the *Wolfspeed/CREE* [103] and shown in Table 5.9, for the 3.3 kV voltage rating SiC-MOSFETs are also considered in this investigation. Consequently, the results are plotted for a minimum number of 5 modules, as presented from Fig. 5.12 to Fig. 5.14. It can be observed in Fig. 5.12 that the cost of the individual module is much higher when 5 modules are used. The reason for that is the high cost of the capacitors, since two capacitors connected in series are required to meet the voltage requirement, and four in parallel to meet the capacitance requirement. Considering the number of modules, the total cost

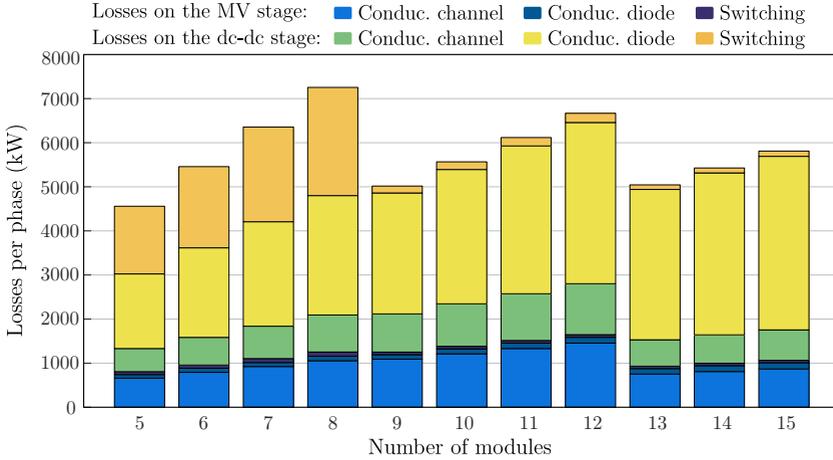
per phase is shown in Fig. 5.13, where the most cost-effective options are achieved for  $N_{mod} = 6$  and  $N_{mod} = 9$ . It is important, however, to highlight that the cost shown for  $N_{mod} = 6$  was calculated considering



**Fig. 5.12:** Cost of the module (using SiC-MOSFETs) according to the number of modules, highlighting the cost sharing among the components.



**Fig. 5.13:** Total implementation cost of one phase of the ST architecture (using SiC-MOSFETs) according to the number of modules, highlighting the cost sharing among the components.



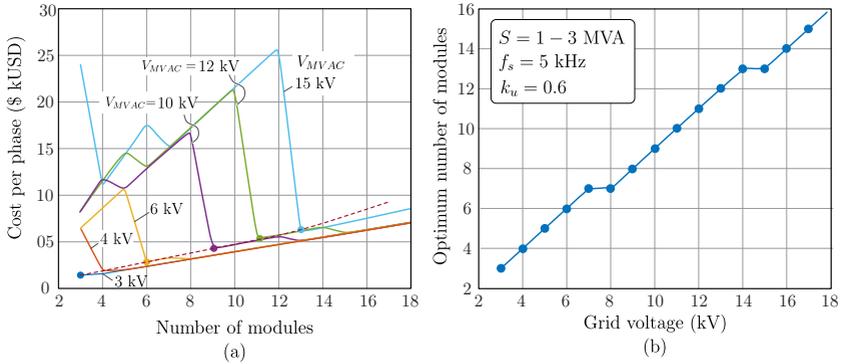
**Fig. 5.14:** Total losses in one phase of the ST system (using SiC-MOSFETs) and the losses distribution on the MV stage and DC-DC stage.

the projected price for the 3.3 kV SiC MOSFETs reported in [103], and not the real one, since the device is not commercially available yet.

From the losses analysis, the best performance is obtained when  $N_{mod} = 9$  and  $N_{mod} = 13$ . Actually, the performance of the SiC MOSFETs of blocking voltage of 1.7 kV and 1.2 kV are similar. For these reason, the results are also very similar. In overall, even adopting SiC-MOSFETs, the system offers the best cost-benefit when  $N_{mod} = 9$ .

Comparing the cost of the ST architecture using IGBT and SiC-MOSFETs, it is noticed that the investment does not differ much. In spite of the fact the SiC devices are more expensive than the IGBTs, the semiconductors cost represents only 35% of the total cost of the module. For this reason, the cost impact is not very significant, when SiC-MOSFETs are used.

Now, comparing the results of losses of the ST architecture using IGBT and SiC-MOSFETs, it is noticed that losses reduce in the range of 25% (when  $N_{mod} = 9$ ) to 58% (when  $N_{mod} = 5$ ) if SiC-MOSFETs are employed, which is a substantial improvement. It is explained by the characteristic of low switching losses of the SiC devices in comparison with the IGBTs. Although the optimum number of modules is currently  $N_{mod} = 9$ , the system provides also satisfactory results when  $N_{mod} = 6$ . It indicates a strong potential of using 3.3 kV SiC-MOSFETs in ST



**Fig. 5.15:** (a) Cost of one phase of the ST in function of the chosen number of modules, considering several grid voltage, (b) optimum number of modules according to the grid voltage.

application. It is important to point out once more that the results for  $N_{mod} = 6$  were obtained with preliminary values and more faithful data are need to confirm such results.

The previous analysis can be generalized taking into account different grid voltages, in order to have a comprehensive case of the optimum number of modules as a function of the grid voltage in which the ST is applied. To simplify, only the semiconductor cost is taking into account, because it is the most expensive device of the module. The results for several grid voltage and power level of 1 MVA ( $k_u = 0.6$ ,  $m = 0.8$ , IGBT semiconductors) is presented in Fig. 5.15. Fig. 5.15 (a) shows the total cost of the semiconductors per phase versus the number of modules for several grid voltages. From this graphic, the optimum number of modules can be expressed in terms of the grid voltage, as presented in (5.17). Consequently, the optimum number of module in terms of the grid voltage is depicted in the Fig. 5.15 (b).

$$N_{mod(opt)} = \begin{cases} V_{grid}(kV), & V_{grid} \leq 7 kV \\ V_{grid}(kV) - 1, & 7 kV < V_{grid} \leq 14 kV \\ V_{grid}(kV) - 2, & 14 kV < V_{grid} \leq 18 kV \end{cases} \quad (5.17)$$

The results presented in Fig. 5.15 (b) is in accordance with those

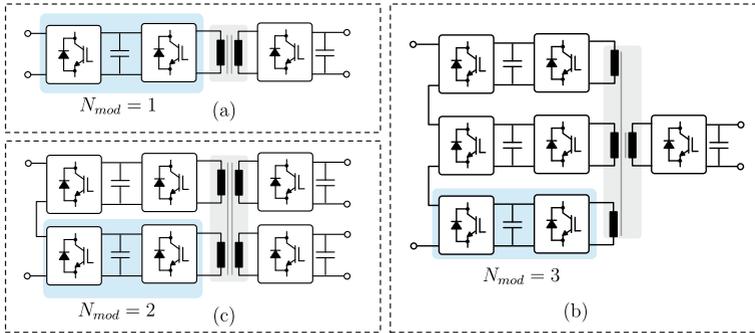
obtained before for grid voltage of 10 kV.

## 5.4 Performance and Economic Analysis of QAB in ST

The QAB converter operates similarly to the DAB, and then similar performance in terms of efficiency can be expected, as demonstrated in chapter 4. On the other hand, there are still some open questions that must be analyzed to justify the QAB converter's suitability in ST application: the economic feasibility and the best configuration. Although the DAB has become the standard solution for the modular ST, its economic feasibility has not been analyzed. In fact, as the QAB and DAB have similar performance, their cost plays the most important role during the choice between them. In this regard, the QAB and DAB are compared in terms of cost, performance, complexity and redundancy cost implementation.

Concerning the configuration, the QAB converter has two degrees of freedom : symmetrical (two inputs and two outputs) or asymmetrical (three input bridges and one output bridge), as shown in Fig. 5.16. Nonetheless, the peculiarities and advantages of those configurations have not yet been evaluated in the literature. Therefore, the comparative analysis is also extended for the different configurations of the QAB converter, where the losses and cost are estimated for each case. As demonstrated in the previous section, the optimum number of modules for the modular ST is  $N_{mod} = 9$ . It means that the number of modules on the MV side (i.e. CHB converter) should be 9, so that the ST achieves the best cost-benefit. The power unit is defined as the DC-DC converter (either LV and MV sides) in combination with the CHB cells in the MV side, as depicted in Fig. 5.16. It means that, depending on the adopted DC-DC converter or the chosen configuration, the number of unit ( $N_{unit}$ ) differs for the number of MV modules ( $N_{mod}$ ).

Fig. 5.16 shows the different units that will be evaluated and compared next, which are based on the DAB converter, symmetric QAB converter and asymmetrical QAB converter. As noticed, the number of MV modules are different in each case, where 1 MV module ( $N_{mod} = 1$ ) is observed for the DAB-based unit, 2 MV modules ( $N_{mod} = 2$ ) are used in the unit based on the QAB with symmetrical configuration, and fi-



**Fig. 5.16:** Power units used as the basic module of the modular ST, pointing out the difference between the number of MV modules ( $N_{mod}$ ) and number of units ( $N_{unit}$ ). (a) Unit based on DAB, (b) unit based on QAB with symmetrical configuration, (c) unit based on QAB with asymmetrical configuration.

nally 3 modules ( $N_{mod} = 3$ ) are observed for the unit based on the QAB with asymmetrical configuration.

Originally,  $N_{mod} = 9$  per phase is adopted for the comparative analysis. It results in 9 units per phase for the system based on the QAB, and 3 units for the system using the asymmetric QAB converter. Consequently, the DC link voltage of the MV modules is 1.13 kV, enabling the use of 1.7 kV blocking voltage IGBT. For the units with the symmetric QAB converter, 5 units should be used, implying in  $N_{mod} = 10$ , in order to provide a lawful comparison. In this case, the DC link voltage of the MV modules is 1.02 kV, allowing still the use of 1.7 kV semiconductors. In order to provide a broad comparison, an additional case is included in the analysis: 3 units based on the symmetric QAB converter. In this case, the power level of each unit will be same of those units based on the asymmetric QAB. On the other hand, the DC link voltage of the MV module will be 1.7 kV, demanding the use of 3.3 kV blocking voltage rating. Finally, four ST architectures will be evaluated and compared: one based on the DAB converter (named as DAB, for now on), one based on asymmetric QAB (called as AQAB) and two based on the symmetric QAB (SQAB). The SQAB is divided in two cases: the first one with 5 units, preserving the DC link voltage of the MV module, called then SQAB-V, and the second case when 3 units are used, preserving the power level of the unit (with respected to the AQAB), named then SQAB-P. Table 5.10 shows the specifications

**Tab. 5.10:** Specification of the Evaluated ST Architectures

ST Architecture	$N_{mod}$	$N_{units}$	$P_{units}$ (kW)	$V_{MVDC}$ (kV)	IGBT voltage rating
DAB	9	9	37.04	1.13	1.7 kV
AQAB	9	3	111.11	1.13	1.7 kV
SQAB-V	10	5	66.66	1.02	1.7 kV
SQAB-P	6	3	111.11	1.7	3.3 kV

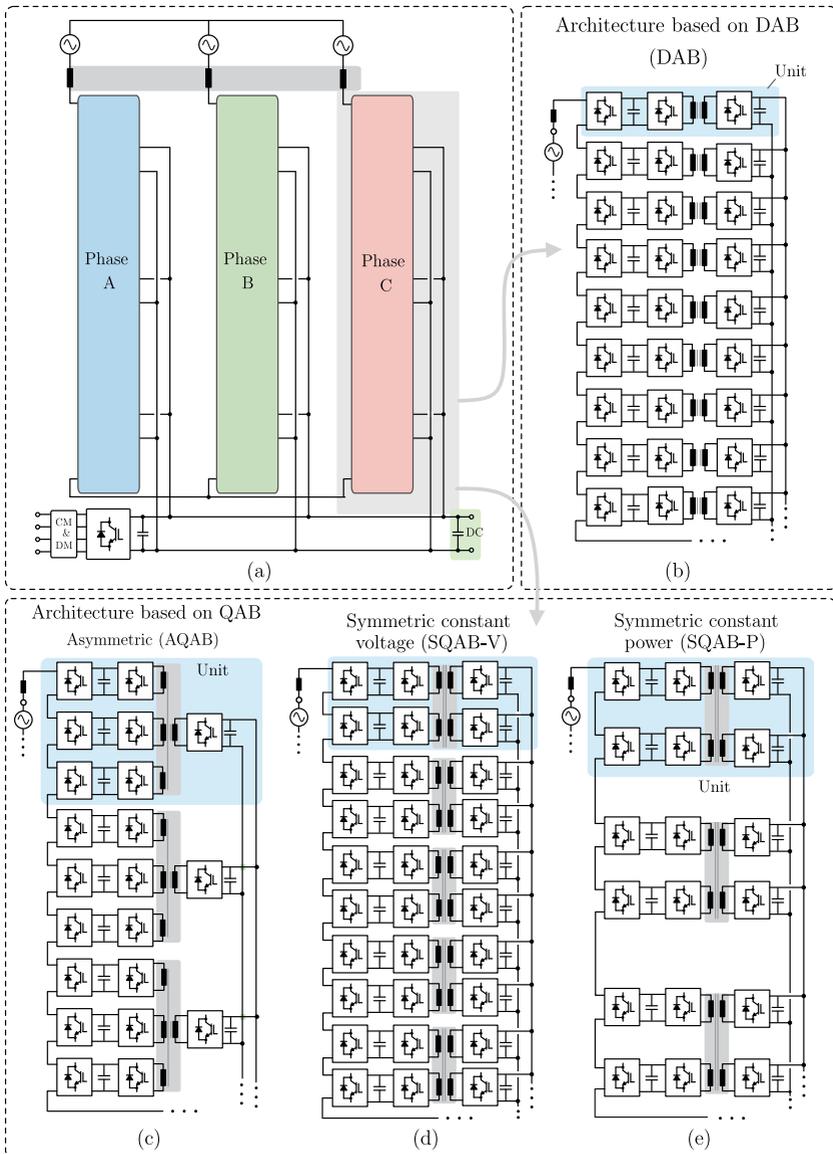
of the evaluated ST architectures, where the power level, voltage level of the DC link and the required voltage rating of the semiconductors are presented. As can be noticed, the AQAB and SQAB-P have the same power level, while the AQAB and SQAB-V have similar voltage level for the DC link. The implementation of each ST architecture considered for investigation is presented in Fig. 5.17.

The main goal of this investigation is to verify the feasibility of the QAB converter in ST application, with respect to the standard solution (the DAB converter) and ascertain which configuration offers more benefits to the ST system.

### 5.4.1 Design Consideration of the Units

Each of the described units are designed taking into account the assumptions and specifications shown in Table 5.11. The losses and efficiency of each ST architecture must be computed for comparison purpose, and then the same design equations and procedure described previously are employed. Hence, a computer-aided based design is used and an algorithm similar to the one depicted in Fig. 5.8 was implemented.

For the DC-DC converter design, the nominal phase shift angle of  $35^\circ$  and switching frequency of 20 kHz were chosen, for the same reasons described in Chapter 4. The current stresses on the IGBT changes according to the architecture and they are calculated for each case. Once they are computed, the semiconductor device is selected and the losses estimated, using the same approach presented in previous section. The equations shown in Table 5.7 are used, regardless the architecture. Differently from the previous section, the transformer and the LV side of the DC-DC converter are considered during the design of the power



**Fig. 5.17:** Smart transformer architectures: (b) DAB: DAB converter as the basic block, (c) AQAB: QAB converter in asymmetrical configuration, (d) SQAB-V: QAB converter in symmetrical configuration, preserving the same voltage level of the MV cells, (e) SQAB-P: QAB converter in symmetrical configuration, preserving the same power level of the asymmetrical configuration.

**Tab. 5.11:** Specification and design consideration of the evaluated ST architectures

System level specification		Converter level specification	
MVAV	10 kV	$\varphi_{nom(QAB/DAB)}$	35°
LVAC	400 V	$f_{s(QAB/DAB)}$	20 kHz
Power	1 MVA	$f_{s(CHB)}$	5 kHz
Grid Frequency	50 Hz	$m_{nom(CHB)}$	0.8
MVDC	10.2 kV	$\Delta V_{dc}$	10%
LVDC	800 V	$T_{a(max)}$	50°C
Country	Germany	$T_{J(max)}$	125°C

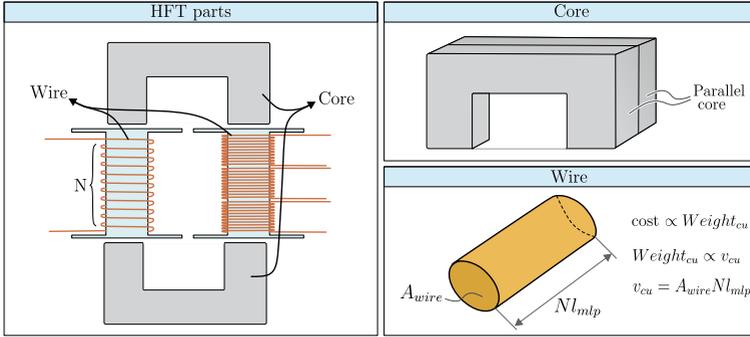
units. As the LVDC is 800 V, those devices shown in Table 5.3 and Table 5.5 with blocking voltage rating of 1200 V are taking into consideration. Further details of the HFT design is presented next.

The design procedure of the CHB (including the current stresses calculation, semiconductor and capacitor selection) is the same, independently the ST architecture. In this case, a nominal modulation index of 0.8 and a switching frequency of 5 kHz are assumed. To select the semiconductors, those devices shown in Table 5.3 and Table 5.5 are used. The cooling system is sized according to the Section 5.4.3 of this document, where the considered temperatures are presented in Table 5.11. For each power unit, auxiliary components (GDU, APC and CCU) were also included in the cost calculation, where the amount of components depends on the unit configuration. For instance, 5 GDU (4 in the MV and 1 in the LV side), 1 APS and 1 CCU are required per unit for the AQAB architecture. Finally, this procedure is carried for each architecture, resulting in 5 different designs.

### 5.4.2 HFT Design Considerations

To design the transformer, a flux density variation of  $\Delta B = 0.3$  T and current density of  $J_{HFT} = 6$  A/mm<sup>2</sup> are considered.

To estimate the total cost of magnetic, the wire and core costs are considered. The cost of the wires used to implement the winding of the transformer is estimated based on the total amount of cooper employed.



**Fig. 5.18:** Part of the HFT considered on the cost computation for the comparison of the different ST architectures.

The basic idea of this approach is to obtain an equation that correlates the copper volume required to implement the winding with the rms current that flows on this coil. This approach is described in detail as follows.

Using the  $i_{rms}$  values through the transformer and a desired current density  $J$ , the necessary wire area  $A_w$  can be calculated as

$$A_w = \frac{i_{rms}}{J}. \quad (5.18)$$

The number of turns for a winding is calculated by (5.19), according to [122],

$$N = \frac{V_{winding}}{4A_c f_s \Delta B} \quad (5.19)$$

where,  $V_{winding}$  is the voltage imposed on the winding,  $A_c$  is the cross section of the selected core,  $f_s$  is the switching frequency and  $\Delta B$  is the magnetic flux variation defined during the design. The required volume of copper is computed by multiplying the area of selected wire by the total length of wire per winding, resulting in

$$v_{cu} = A_{wire}(Nl_{mlp}), \quad (5.20)$$

where  $l_{mlp}$  is the mean length of one turn. Replacing (5.18) and (5.19) in (5.20) the following relation is obtained

**Tab. 5.12:** Considered parameters for the MFT Design

Current density	$J = 3 \text{ A/mm}^2$
Copper density	$d_{cu} = 8.96 \cdot 10^{-3} \text{ g/mm}^3$
Copper Cost	$C_{cu} = 2.96 \cdot 10^{-3} \text{ U\$/g}$
Switching frequency	$f_s = 20 \text{ kHz}$
Mean turn length of wire	$l_{mlp} = 96 \text{ mm}$
Flux density variation	$\Delta B = 0.3$

$$v_{cu} = \frac{V_{winding}}{4A_c f_s \Delta B} \frac{I_{rms}}{J} l_{mlp}. \quad (5.21)$$

As the design parameters  $f_s$ ,  $\Delta B$  and  $J$  are constant and assuming constant core size, then equation (5.21) can be rewritten as

$$v_{cu} = k_1 V_{winding} I_{rms}, \quad (5.22)$$

$$k_1 = \frac{V_{winding}}{4A_c f_s \Delta B} \frac{I_{rms}}{J} l_{mlp}. \quad (5.23)$$

The weight of cooper used is determined using the volume ( $v_{cu}$ ) and the cooper density  $d_{cu} = 8.96 \text{ g/cm}^3$ .

$$W_{cu} = v_{cu} d_{cu} \quad (5.24)$$

Then, replacing (5.22) in (5.24), the equation of the total amount of cooper required is given by (5.25). From this equation, it is noticed that the required cooper is proportional to the power processed by the winding.

$$W_{cu} = k_1 d_{cu} (V_{winding} I_{rms}) \quad (5.25)$$

Finally, the cost required to implemented the winding is calculated using the cooper cost per kg obtained from [147] and also the weight, as defined in (5.26). From this equation, it was demonstrated that the cooper price used is proportional to the power processed by the winding ( $P_{winding}$ ). Considering the same constant dc voltage imposed on the

winding, then the cost became directly proportional to the rms current flowing in the winding.

$$C_{cu} = W_{cu}P_{cu}, \quad (5.26)$$

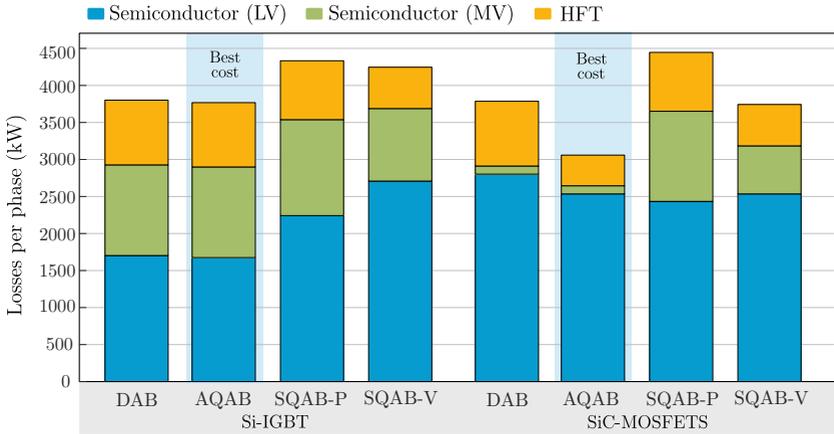
$$C_{cu} \propto P_{winding} \propto I_{rms}. \quad (5.27)$$

Then, using (5.27) and assuming the parameters presented in Table 5.12, the cost of the MFT transformer is obtained for each architecture considered in this work.

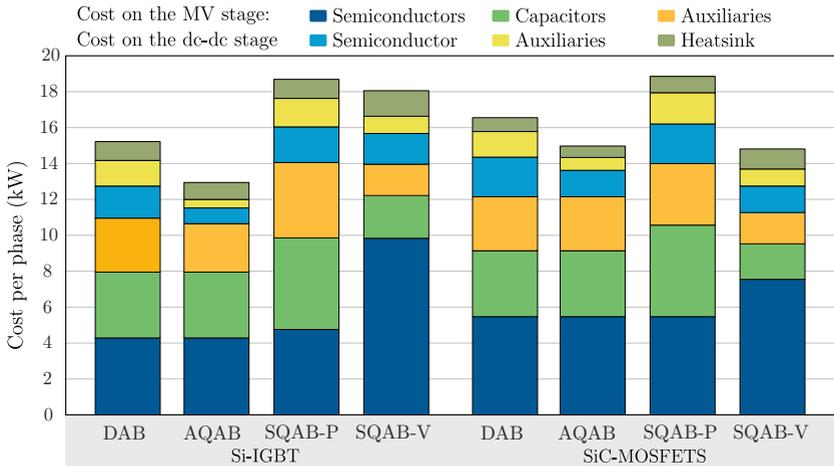
### 5.4.3 Comparative Evaluation

The results from the design described before are summarized in Table 5.13 and in Figs. 5.19 and 5.20. They are divided in two cases, according to the employed semiconductors technology. The first case uses Si-IGBT, whereas the second uses SiC-MOSFETs, and each case is discussed as follows.

The DAB architecture has more power units, but the power level of each unit is the lowest one compared to the other architectures. Analyzing the parameters of the MV side, the current efforts on the semiconductor are the same for all architectures, independently from the configuration. Hence, the current rating of the employed semiconductor is also the same. With respect to the voltage level of the semiconductors, only the SQAB-P requires 3.3 kV devices, while the others require 1.7 kV rated devices. Then, DAB, AQAB and SQAB-V use the same devices on the MV side. In spite of the availability of 3.3 kV IGBT on the market, there is no SiC-MOSFET available yet with this voltage rating, as mentioned before. The previous information provided by [103, 104], including the price estimation, were used to calculate the losses and cost of SQAB-P. Analyzing the LV side, power semiconductors rated for 1.2 kV of blocking voltage are used independently from the architecture.



**Fig. 5.19:** Losses comparison of the investigated ST architectures, considering the Si-IGBT and SiC-MOSFETs devices.



**Fig. 5.20:** Cost comparison of the investigated ST architectures, considering the Si-IGBT and SiC-MOSFETs devices.

**Tab. 5.13:** Comparative Analysis of the Architectures

Basic Information (per Phase)				
	DAB	AQAB	SQAB-V	SQAB-P
N° of units per phase	9	3	5	3
Power level of the unit	37.04 kW	111.11 kW	66.66 kW	111.11 kW
MVDC link	1.13 kV	1.13 kV	1.02 kV	1.7 kV
Semiconductor - MV side				
N° of power devices	36	36	60	36
Si-IGBT	CM75DY-34A	CM75DY-34A	CM75DY-34A	QID3310006
SiC-MOSFET	C2M0045170D	C2M0045170D	C2M0045170D	CREE 3.3 kV
Semiconductor - MV side				
N° of power devices	36	12	20	12
Si-IGBT	CM75DU-24F	CM200DX-24S	CM75DU-24F	CM75DU-24F
SiC-MOSFET	C2M0040120D	C2M0025120D	C2M0040120D	C2M0025120D
Medium-Frequency Transformer				
N° of MFT	9	3	5	3
Equivalent inductance	27.3 $\mu$	187.96 $\mu H$	54.56 $\mu H$	34.54 $\mu H$
Auxiliary Components				
N° of APS	18	12	20	12
N° of GDU	36	24	40	24
N° of CCU	36	24	40	24

### Losses and Cost Comparison

The cost and efficiency are the most important parameters evaluated in this work and they are compared as follows.

From the losses analysis presented in Fig. 5.19, it can be seen that the AQAB presents the best performance, while SQAB-V the worst one, regardless the semiconductor type used. The few number of components and the high performance of the power devices on the LV side of the AQAB played an important role in favor of the AQAB architecture's efficiency. The DAB used as basis of comparison, has presented the second best performance, but only slightly better compared to the SQAB-P. As an overall analysis, it can be noticed that the losses for all architecture are very similar to each other, with a difference of only 10% between the best one and the worst one. Note that this design concerns the specifications provided in Table 5.11. Different grid specification might imply in different results. Still from these results, the application of SiC MOSFETs has improved the performance in terms of efficiency of the architectures DAB, AQAB and SQAB-P, but deteriorated the efficiency of the SQAB-V. Due to the high number of employed modules in this last architecture, the current in the LV side bridge is very small, allowing the use of lower current rating devices, compared to the others. As a result from the design, the SiC MOSFET C2M0040120D (1200V / 60 A) was selected for the SQAB-V, while the device C2M0025120D (1200V / 90 A) was selected for the others architectures, providing lower on resistance and better performance. Of course, the device C2M0025120D can also be used in SQAB-V, improving the performance, but also increasing the cost.

Regarding the cost analysis, the AQAB has also presented the best results, regardless the semiconductor. However, when SiC-MOSFETs are employed, the DAB, AQAB and SQAB-V presented similar cost, with a small difference of 1%. Only the SQAB-P has presented a significant high cost compared to the others, because of the price of the high-voltage device required on the MV side of this architecture. As noticed, the total cost of the semiconductors used on the MV side are always higher than the total cost of the semiconductors used on the LV side, even for those architectures that utilizes the same number of cells on the LV and MV sides. The reason for that is the higher number of semiconductors on the MV side (once the CHB are also included) associated to the higher voltage rating devices (blocking voltage of 1.7 kV and 3.3 kV) compared to the LV side semiconductors.

### **QAB Configurations**

The AQAB architecture is more advantageous in terms of efficiency and cost. The main reason for that is the reduced number of cells and MFT, compared to the SQAB-V, and the possibility of using lower voltage rating devices, compared to the SQAB-P. Although higher current rating devices are required to implement the LV cell of the AQAB (see Table 5.13), the cost of the individual device does not differ much from the cost of the devices required by the other solutions. As SQAB-P requires semiconductors with voltage rating of 3.3 kV on the MV side, only IGBT can be used. Besides, the price of this device is very high, increasing drastically the cost of the system. For that reason, SQAB-P is the most expensive solution, reaching almost twice the cost of the AQAB.

### **Si-IGBT vs. SiC-MOSFETs Comparison**

As expected, the performance of all architectures are improved in terms losses reduction, when SiC MOSFETs are used, demonstrating the superior performance of this semiconductor technology. On the other hand, its price is still very high, when compared to the classic Si-IGBT. Using the results obtained from the AQAB, i.e. the most promising one, the SiC-MOSFET offers around 10% of losses reduction, but the system cost increases in almost 40%. Then, the energy saving throughout the system operation needs to be evaluated economically according to the application, to verify if the additional installation investment of using SiC-MOSFET is economically viable.

### **Further Comparison**

In addition to the cost and efficiency, the architectures can be compared qualitatively in two more categories:

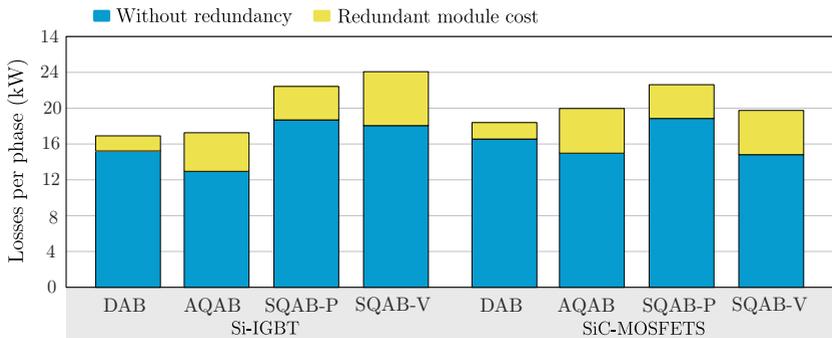
- Redundancy implementation effort:

The fault tolerance scheme is a very important feature for the system, because it increases significantly its availability. This feature is normally obtained by using redundant power units and to implement that, at least one additional power unit needs to be used. The investment for implementing the redundancy scheme depends on the cost of the individual unit and the number of additional

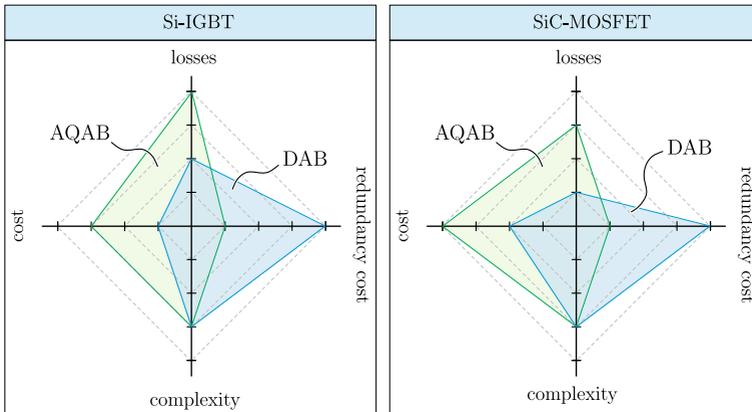
units needed. This investment will be different for each architecture evaluated in this work. Therefore, the cost of redundancy implementation for each architecture is analyzed and compared herein. To to so, it is assumed that the minimum number of additional units is used, i.e. only one extra unit in each architecture. Fig. 5.21 shows the cost of the different architectures without redundancy and also the cost of the redundant unit. As can be noticed, the cost of the extra unit of the DAB is the lowest one, regardless the semiconductor technology used, because of its simplicity. Nevertheless, considering the total cost of the system including the redundant unit, the AQAB is still more advantageous economically, when Si-IGBT is used. When SiC-MOSFETs are used, the DAB presents more advantages. From this comparison, it is important to note that the DAB has advantages for the redundancy scheme implementation because the price of the individual unit the lowest.

► Design Complexity:

The design complexity is very difficult to quantify, then a qualitative discussion is presented. Discussion regarding the QAB design indicates that the architectures based on this converter are more complex than the DAB-based architecture from the control and power stage aspects. The QAB converter requires an additional control loop to equalize the power of the bridges, then the control effort implementation is slightly higher, when compared to



**Fig. 5.21:** Cost comparison of the investigated ST architectures, considering the Si-IGBT and SiC-MOSFETs devices.



**Fig. 5.22:** Qualitative comparison of the standard solution based on DAB converter with the proposed QAB solution, considering the most promised configuration (asymmetric configuration): (a) Si-IGBT, (b) SiC-MOSFETs.

the DAB. From the power stage viewpoint, the complexity of the QAB lays on the multiwinding transformer design, compared to the classical two winding used on the DAB converter. In this aspect, the DAB-based solution is more advantageous than the QAB-based architectures. Nevertheless, some adversities in this sense have been discussed in [88, 89].

### QAB vs. DAB Comparison

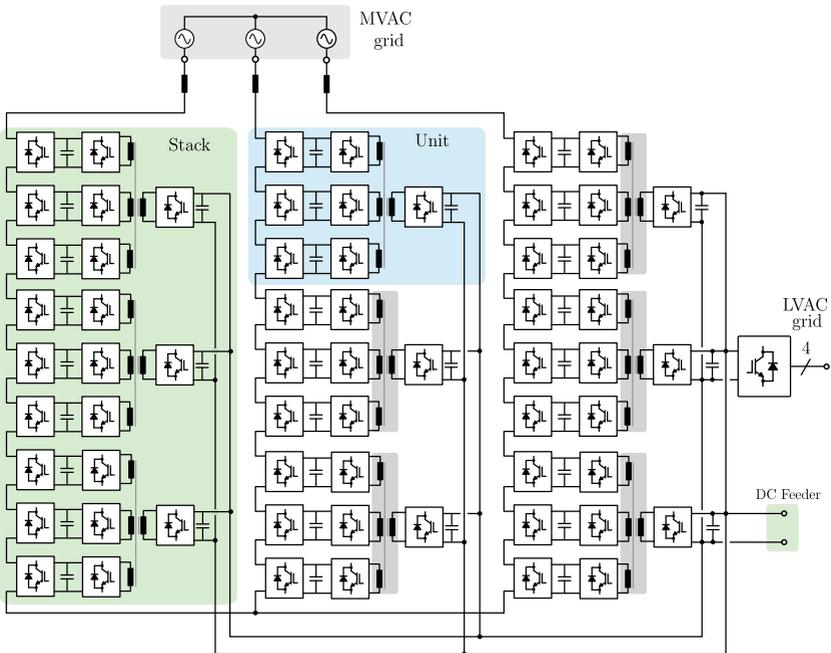
To evaluate the potential of the QAB converter in ST application, the best configuration (AQAB) is individually compared to the standard solution based on DAB, and the results are depicted in Fig. 5.22. In virtue of the fewer number of components (cells and MFT), the QAB solution is more cost effective, as presented in Fig. 5.19 (b). Adopting this solution instead of the DAB, and considering the specification of the Table 5.11, the system cost can be reduced in around 20%, when Si-IGBT are employed.

Regarding the efficiency, both QAB and DAB solutions have presented similar performance, although the first one performs slightly better. As the QAB operates similarly to the DAB converter, when processing balanced power, then similar power dissipation is also ex-

pected. Of course, semiconductors with different electric characteristics are used in the LV cells for both cases, and also the quantity of devices, resulting in different power dissipation between the solutions. Then, QAB converter is presented as an economically viable solution and its potential in ST application has been demonstrated from the results obtained in this work.

#### 5.4.4 Discussion

From the previous analysis, it is observed that different performance and cost for the ST system are expected according to the configuration of the QAB converter. Among them, the asymmetrical configuration consisting in 3 bridges connected to the MV side and one to the LV side (i.e the AQAB) provides more benefits for both cost and efficiency. In comparison to the DAB, the AQAB performs similarly, while pro-



**Fig. 5.23:** ST architecture based on CHB and QAB with the the cost-benefit trade off.

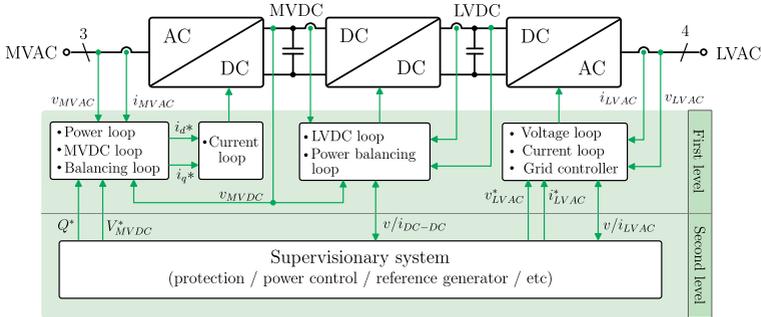


Fig. 5.24: Block diagram of the smart transformer control system.

viding a cheaper solution. Consequently, the AQAB is the best choice. Moreover, it has been demonstrated that  $N_{mod} = 9$  offers the best cost-benefit. Thus, Fig. 5.23 shows the most promise ST architecture and the control system and simulation for this architecture is presented next.

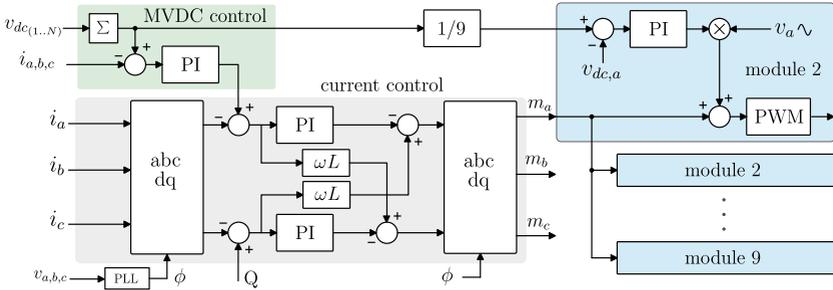
## 5.5 Control System Description

The ST is intended to have an advanced control system, in order to provided the required ancillary services to the grid. Some of the possible and profitable services are summarized in Table 5.14, according to [19, 53]. This table shows also the control loops required to implement the aforementioned services. The simplified block diagram of the control system of the ST is illustrated in Fig. 5.24, where two control levels are observed. The first level refers to the control loops related to the converter control, where the power, current and voltages loops are implemented. The second level is related to the system level control, or supervision system, where it is responsible for taking the decision and generating the references for the first level control. As noticed in Fig. 5.24, the MV stage controls the input current, the total MVDC link, as well as the individual DC link voltage of each module. The active and reactive power exchanged between the MV grid and the ST is controlled by means of the current loop.

The DC-DC stage is responsible to control the LVDC link, providing a well regulated DC voltage for the LV stage. Due to the modular

**Tab. 5.14:** Ancillary Services Provided by the ST to the Grid and Required Control Loops

Ancillary services		
AC-DC MV Stage	DC-DC Stage	DC-AC LV Stage
Voltage Support (Steady State and LVRT)  Reactive power compensation at MV Substation  Power quality improvements  Islanding Control (high DG in LV)	Reverse power (flow control)  Circuit breaker function (current limitation)	Impedance identification  power flow control  ST overload control  Soft load reduction  Damping of harmonics and resonances
Required control loops		
Input current (active and reactive power)  Total MVDC link  Individual MVDC links	LVDC link  Power balance among the modules	LV grid voltage  Grid current



**Fig. 5.25:** Block diagram of the control strategy of the CHB converter [148–151].

characteristics of the ST, each module is intended to process the same amount of power, and then a power balance loop is required. This control loop is also implemented in the DC-DC stage, as seen in Fig. 5.24. Moreover, the DC-DC stage must provide output current limitation, for protecting the loads and sources connected to the LVDC link, like storage system for instance.

The LV stage controls the output voltage, where a sinusoidal voltage waveform with the required amplitude and frequency must be provided, regardless the load characteristic connected to the grid. To provide the extra services described in Table 5.24, such as impedance and load identification, power flow control and damping of harmonics for instance, the current needs to be controlled. Therefore, an output voltage loop and current loop are required, as shown in Fig. 5.24. The system level control (second level), which is intended to take the decisions according to the grid load profile, generates the references for the voltage and current loops.

This thesis emphasizes the study on the MV stage and DC-DC stage, focusing mainly on the DC-DC stage. Then, the control system of these both stages is described and more detail of the DC-DC stage control is discussed.

### 5.5.1 MV Stage Control System

The block diagram of the MV stage control strategy is depicted in Fig. 5.25 and this scheme has been intensively adopted in many other works related to three-phase rectifiers [66, 148–155]. The well-known scheme

based on an outer voltage loop and inner current loop is employed. The current loop is implemented in the  $d$ - $q$  rotating reference frame, where  $i_p$  and  $i_q$  are related, respectively, to the active and reactive power processed by the CHB. The reference used to control the direct current  $i_p$  is generated by the MVDC link voltage loop, while the reference to control the current  $i_q$  is provided directly by the supervision system, as seen in Fig. 5.25. To control the individual DC link voltage of the modules, each module has its own loop. It is a standard strategy, where a voltage loop is used, contributing to the modulation index of the individual modules, to increase or decrease the power processed by it, according to its DC link voltage. More detail of this strategy is given in [66].

### 5.5.2 DC-DC Stage Control System

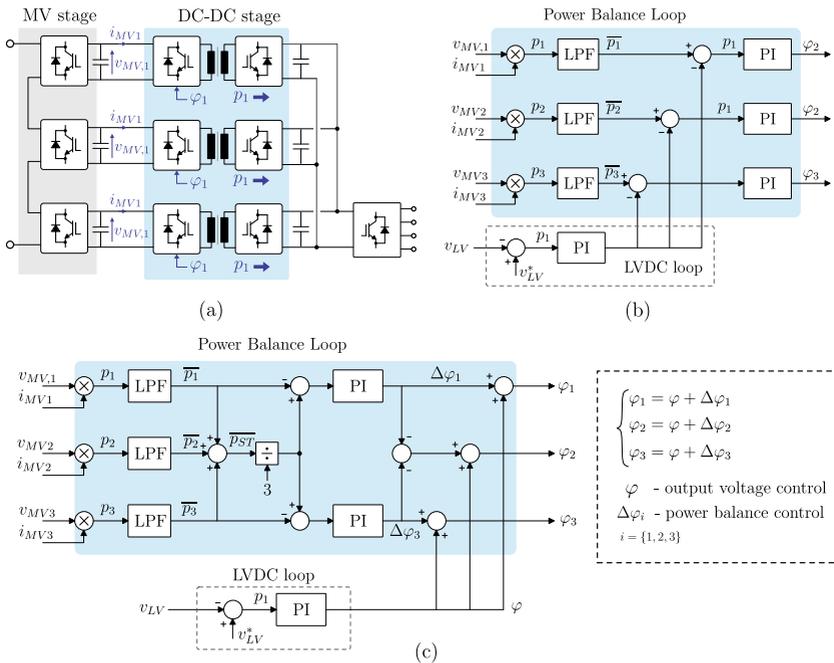
The DC-DC stage controls the LVDC link, by means of the power exchange between the MV side and LV side. By the virtue of the modular characteristics, each module must contribute equally for the LVDC control and then a power balancing loop is required. In fact, the voltage loop defines the amount of power required to guarantee a regulated voltage, and the power balance loop defined the distribution of this power among the modules. Hence, a single voltage loop is used for the whole DC-DC stage, regardless the number of modules. To implement the power balancing loop, two strategies have been highlighted in literature for system using the DAB converter on the DC-DC stage [156–158]. Assuming the system composed by the CHB and the DAB converter, as shown in Fig. 5.26 (a), the two power balancing loop strategies are: the cascaded loops [156], shown in Fig. 5.26 (b), and parallel loops [157] shown in Fig. 5.26 (c).

The cascaded loops technique consists in an outer voltage loop, providing the reference to the power inner loop, as illustrated in Fig. 5.26 (b). It means that each module has its own power loop.

The second technique consists in a common voltage loop, defining the nominal phase-shift angle  $\varphi$  of the DAB converters, which is the same for every module. The power of each module is adjusted by a perturbation  $\Delta\varphi$ , computed individually by each module. Then, in this strategy, the phase-shift of a generic module  $i$  is defined as  $\varphi_i = \varphi + \Delta\varphi_i$ , where  $\varphi$  is responsible to control the output voltage, while  $\Delta\varphi_i$  is responsible to balance the power of module  $i$ .

Both control strategies can be easily adapted to the QAB converter. On the other hand, besides to balance the power shared among the QAB converters, the power of a single QAB must be balanced between its own cells, since the QAB is constituted by three cells connected in the MV side. It means that each MV cell of one QAB must share equally the total power of the QAB converter. To do so, both strategies (with parallel loops and cascaded loops) can be combined, and adapted for the QAB, consisting then in an output voltage loop and two power balance loops: the first one to balance the power among the several QABs, and the second one to balance the power in the QAB among their cells.

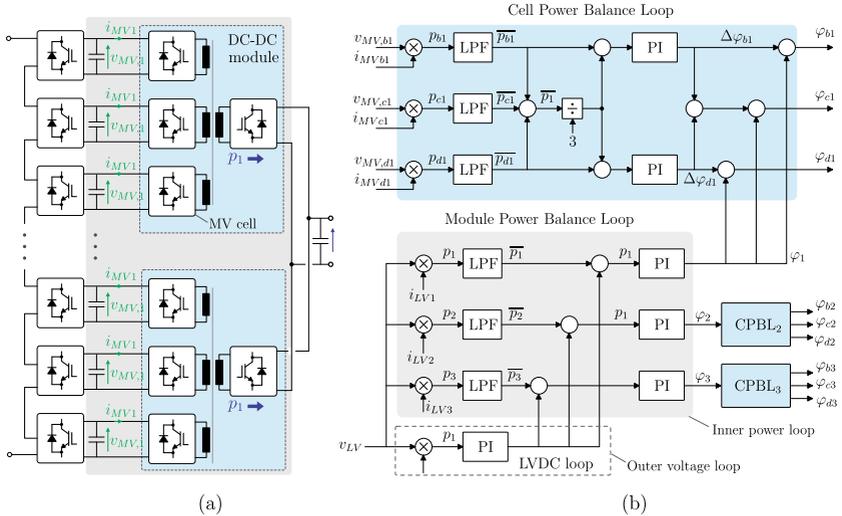
The Fig. 5.27 (a) shows the block diagram of an equivalent single-



**Fig. 5.26:** Control of the DC-DC stage based on the DAB converter: (a) equivalent single-phase ST based on DAB converter, (b) control strategy of the DC-DC stage (based on the DAB) using the cascaded loops [156], and (c) control strategy using parallel loops [157].

phase ST composed by the CHB and the QAB, where the Fig. 5.27 (b) illustrates the block diagram of the control scheme. The control strategy of the QAB consists in an outer voltage loop, providing the power reference to the power inner loop (named as Module Power Balance Loop - MPBL). This power loop controls the power sharing among the modules of the DC-DC stage, i.e. the QAB converters in this case. This control loop works analogous to the cascaded loops technique explained for the DAB. A second power balance loop (Cell Power Balance Loop - CPBL) is used to balance the power sharing by the cells of one QAB. In this case, the parallel loops technique is used, where each QAB has nominal phase-shift angle  $\varphi$ , provided by the MPBL.

The power of each cell of the QAB is adjusted by a perturbation  $\Delta\varphi$ , computed individually. Then, in this strategy, the phase-shift is



**Fig. 5.27:** Control system of the DC-DC stage, considering the QAB converter as the basic unit: (a) equivalent single-phase ST based on QAB converter, (b) control strategy of the dc-dc stage using the cascaded loops to balance the power among the units, and the parallel loops to balance the power among the cells of the same unit.

defined as

$$\begin{cases} \varphi_{b,i} = \varphi_i + \Delta\varphi_{b,i} \\ \varphi_{c,i} = \varphi_i + \Delta\varphi_{c,i} \\ \varphi_{d,i} = \varphi_i + \Delta\varphi_{d,i} \end{cases} \quad (5.28)$$

where  $i$  refers to the generic QAB ( $i = \{1, 2, 3\}$ ) and  $\varphi_{b,i}$ ,  $\varphi_{c,i}$  and  $\varphi_{d,i}$  are the nominal phase shift angles of the cells  $b$ ,  $c$  and  $d$ , respectively of the QAB  $i$ . In this case,  $\varphi_i$  is used to control the total amount of power processed by a QAB module, where  $\Delta\varphi_{b,i}$  is responsible to balance the power of the cell  $b$ .

## 5.6 Simulation Results

To verify the operation of the ST architecture depicted in Fig. 5.23 using the control system previously described, the architecture was designed and simulated. Only the AC-DC and DC-DC stages of the three-phase ST architecture were taken into account during the simulation. The design of the ST was carried out using the grid specification presented in Table 5.15, and the equations discussed in this chapter. Furthermore, the algorithm used for the comparison of the architectures (5.8) was also used to design the converters in this section. Note that the equations used for designing the converters and the entire system were already described, they are not discussed again. Only the outcomes of the design is presented. Table 5.15 presents the parameters and assumptions for the design of each stage, as well as the outcomes of the converter's design. Each phase of the system is composed by three units of 111.11 kW each, implying in nine modules with power capability of 37.04 kW on the MV side. From the design, an expected efficiency of 97.85% was calculated, which is considerably high.

To control the CHB converter, the controllers were designed based on the strategy presented in Fig. 5.25, which three loops are used: output voltage loop, input current loop and balancing voltage loops of the MVDC link of the modules. The current compensator was designed in the  $d$ - $q$  rotating frame according to [64, 159], where a proportional-integral (PI) compensator is used. The voltage controller provides the reference for the current controller, and this compensator is also based on a PI controller. The voltage balancing control uses a simple proportional (P) controller, to compensate the imbalances. To control the

QAB converter, the PI compensator is used in the LVDC loop, the power balance loop between the modules and also the power balance loops among the cells of a single QAB. The LVDC loop presents the higher bandwidth, with a crossover frequency of 2 kHz, while the MPBL has a lower bandwidth, with a crossover frequency of around 150 Hz.

**Tab. 5.15:** Specification and Design Consideration of the Evaluated ST Architectures

System Parameters	
Nominal power	$S_{ST} = 1 \text{ MVA}$
Input voltage	$V_{MVAC} = 10 \text{ kV}$
RMS input current	$I_{a(rms)} = 57.73 \text{ A}$
Output voltage	$V_{LVAC} = 400 \text{ V}$
Total MVDC link	$V_{MVDC} = 10.2 \text{ kV}$
Individual MVDC link	$V_{dc(mod)} = 1.1 \text{ kV}$
LVDC link	$V_{LVDC} = 800 \text{ V}$
Number of modules per phase	$N_{mod} = 9$
Power of the individual module	$P_{mod} = 37.04 \text{ kW}$
MV AC-DC Stage - CHB	
Switching frequency	$f_{s(CHB)} = 5 \text{ kHz}$
Nominal modulation index	$m_{nom(CHB)} = 0.8$
Semiconductor utilization factor	$k_u = 0.65$
Capacitor voltage ripple	$\Delta V_{dc} = 10\%V_{dc(mod)} = 110 \text{ V}$
Required capacitance per module	$C_{mod} = 1.6 \text{ mF}$
Utilized capacitor	$8 \times 295\mu\text{F}$ (B25620B1297K983)
DC-DC Stage - CHB	
Switching frequency	$f_{s(QAB)} = 20 \text{ kHz}$
Nominal phase-shift angle	$\varphi_{nom(QAB)} = 35^\circ$
Required equivalent inductance	$L_{eq} = 203\mu\text{H}$
Transformer turn ratio	$n = 0.4725$
Calculated efficiency	$97.85\%$

The CPBL is the slowest loop, with a crossover frequency of around 30 Hz. The design of the controllers is not described, because it is not the focus of this work.

To verify the system's operation by simulation, the ST and control system were implemented and simulated using the PLECS toolbox of the MATLAB. The results are presented from Fig. 5.28 to Fig. 5.32.

### 5.6.1 Steady-State Operation

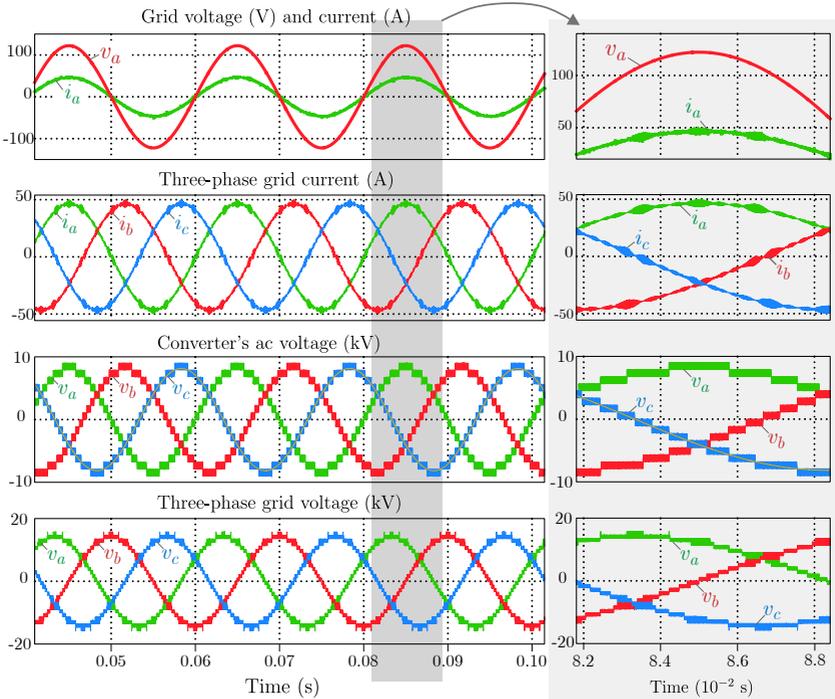
Initially, the designed ST is simulated in steady-state to evaluate the operation. The results are summarized in Fig. 5.28 and Fig. 5.29. As observed in Fig. 5.28, the converter operates with unit power factor, where the grid voltage and current are in phase. The phase-to-ground and line-to-line three-phase voltages are observed in this figure, where multiple levels are observed. The details of the waveforms are also depicted in Fig. 5.28, where a low current ripple, due to the high number of levels are noticed.

The main waveforms of the DC-DC stage is presented in Fig. 5.29, where a regulated output voltage of 800 V is observed. The phase-shift operation is also observed in this figure, where displacement between the primary and secondary voltages are observed. Besides that, equal power level are processed by each bridge, demonstrating the power balancing condition.

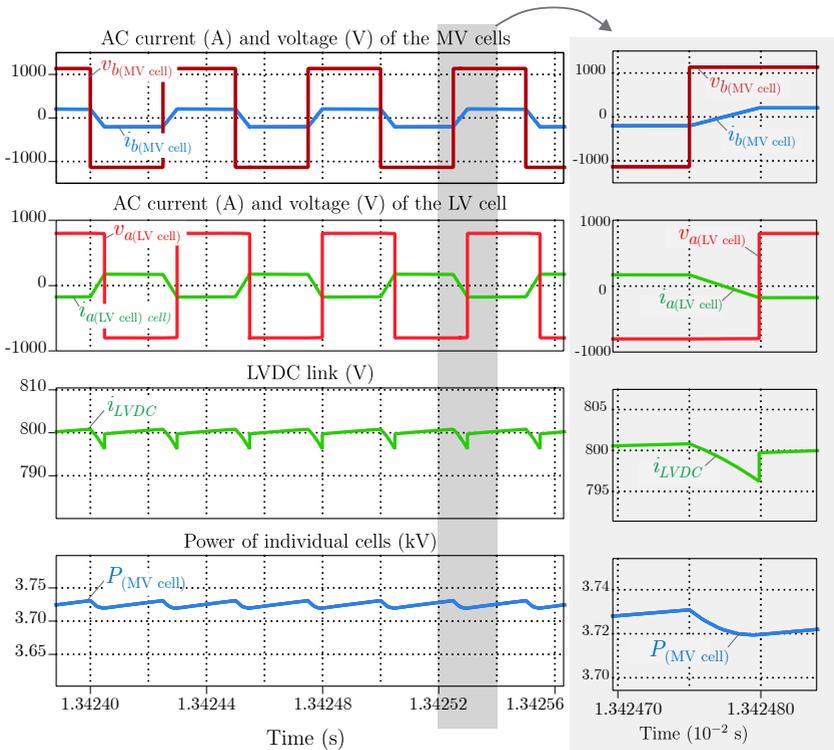
### 5.6.2 Dynamic Operation - Load Variation

#### Load Variation

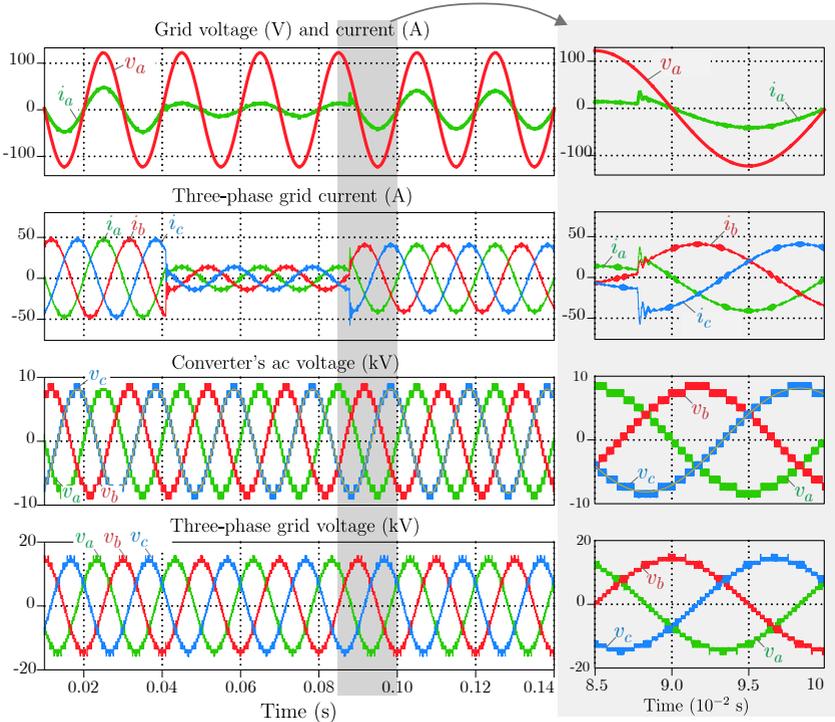
To verify the dynamic operation of the converter, load variation was applied to the system and the dynamic response of the AC side currents and voltages were saved. Although soft variation of the load is expected in field application, the instantaneous load variation was applied to the ST architecture in this simulation, to verify its performance in the worst (and unexpected) case. The results are presented in Fig 5.30. Two load variations over the time are observed in this figure: from full load to 30% of the load, and from 30% to 88% of the load. The detail of the dynamic response is also highlighted in Fig 5.30, during the step-up variation of the load. This result shows a proper operation of the converter under load variation, validating the design of the control system.



**Fig. 5.28:** Simulation results: main waveforms of the three-phase ST architecture operating in state-state.



**Fig. 5.29:** Simulation results: main waveforms of the DC-DC stage of the ST architecture operating in state-state.



**Fig. 5.30:** Simulation results: main waveforms of the MV stage of the ST architecture under load variation.

### **Power Flow Control**

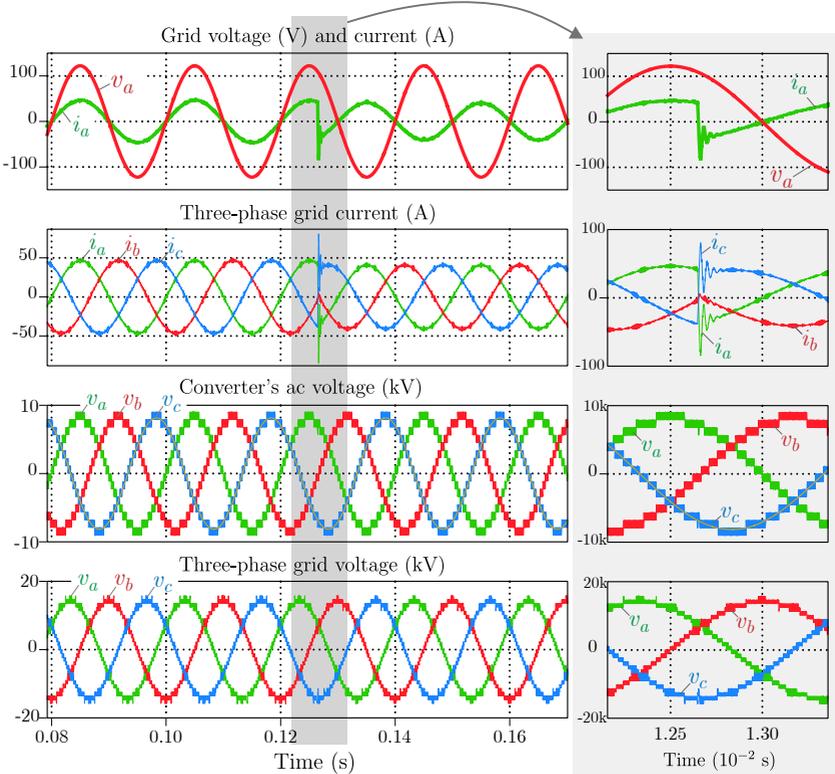
An extreme load variation case was applied to the converter, including the variation of the power flow. In this case, the variation from full load to  $-88\%$  of the load was applied to the converter. The converter operates in the first moment with full direct load (from AC side to DC side), when the load changes suddenly for some reason to  $88\%$  in the reverse direction, injecting power into the grid. The result is presented in Fig. 5.31, and it shows a proper operation of the converter, where the voltages were maintained regulated. This result demonstrates the converter's capability to control the power flow.

### **Reactive Power Compensation on the MV side**

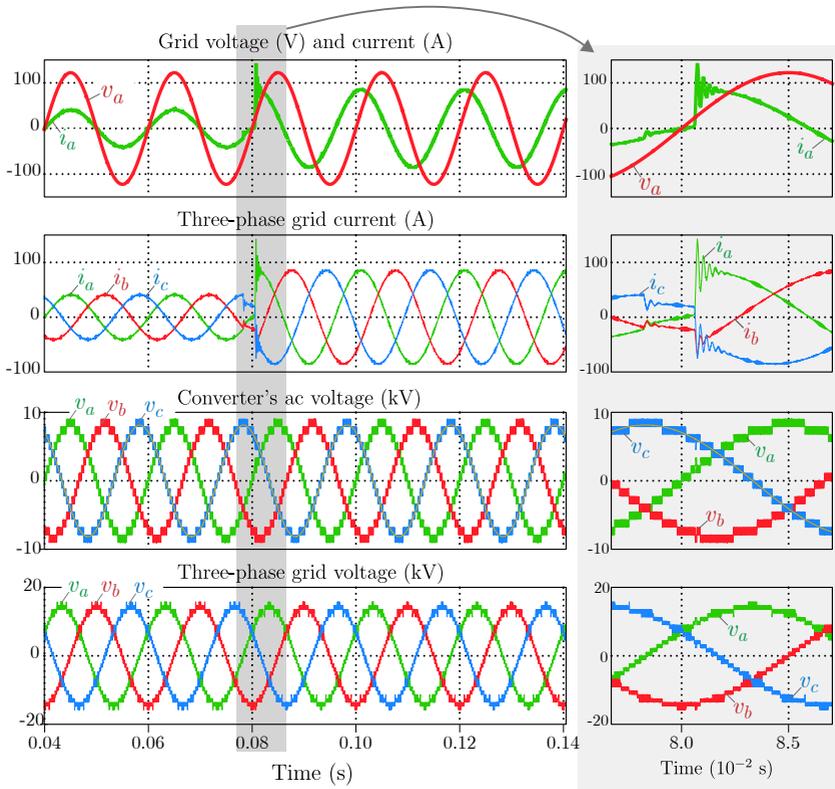
Finally, the reactive power flow compensation functionality was evaluated in simulation, and the result is illustrated in Fig. 5.32. In this case, the converter is initially absorbing only active power from the grid, when suddenly it is requested (for some grid service) to provide 200 kVAR of reactive power, as observed in the Fig. 5.32. In this case, the amount of active power is also reduced, due to the load reduction, keeping the apparent power into the limit of 1 MVA. As observed in Fig. 5.32, the current grid is in advanced with respect to the grid voltage, indicating that inductive reactive power is processed. It shows that the converter operates as expected.

### **5.6.3 Summary**

Not only the converter's design is a challenge for the ST implementation, but also the architecture design by itself. The implementation of the entire system involves different design levels, such as: component level, converter level and system level. In this chapter, the system level design has been carried out and discussed. Initially, the analysis of the CHB was realized, where the modulation was described, and main equations required for its design were derived. Then, the trade-off between cost and performance of the system was analyzed, according to the number of module, with the aim to determine the optimum number of modules. To do so, an algorithm was implemented, and the system was designed with different number of modules: from 5 modules to 15 modules. In each case, the losses and cost of the system were computed and compared. From this investigation, it was noticed that the system



**Fig. 5.31:** Simulation results: main waveforms of the ST architecture when the power flow direction changes from positive (from ac to the dc side) to negative direction (dc to ac side).



**Fig. 5.32:** Simulation results: main waveforms of the ST architecture processing reactive power.

presents the best performance when nine module are employed.

Moreover, different configurations of the QAB converter were described and, consequently, three ST architectures based on these configurations were generated. Besides that, a ST architecture based on the classic DAB was also presented, resulting then in four architectures, named as: DAB-based architecture (used as benchmark), Asymmetrical QAB (AQAB), Symmetrical QAB in voltage (SQAB-V) and Symmetrical QAB in power (SQAB-P). They were then compared in terms of efficiency, cost and complexity, with the aim to determine which one offers the best trade-off between cost and performance. From this investigation, the AQAB architecture presented the best performance in terms of efficiency and cost. Compared to the classic DAB solution, the AQAB offers a cost reduction of around 20%. The efficiency of both solutions are very similar, only a slightly improvement of 5% is obtained in the AQAB. Regarding the potential of SiC-MOSFETs in ST application, this device offers a reduction in losses of around 10%, but it increases the system cost in around 40%. Therefore, to verify the economic feasibility of such device in this application, a study considering the energy saving over time and the installation cost should to be realized.

Finally, the control system is briefly described and simulation results for the system operating in different condition were provided. The simulation results have verified the proper operation of the ST system.



## Chapter 6

# Smart Transformer Demonstrator

**M**ANY challenges faced during the conceptualization and design of the ST have been covered along this work. An overview of the possible architectures and topologies was presented in chapters 1 and 2, where the three-stage architecture based on the CHB has been pointed-out as the most promised one. For implementing the DC-DC stage, two converters have been pointed out: the SRC and the QAB. The SRC was described and analyzed theoretically in chapter 3, in which its high performance and reliability were validated experimentally. Similarly, the QAB converter was studied in chapter 4, where the analysis, design and experimental results were presented. Comparing both DC-DC converters, the QAB offers a broad possibility to control voltage and current and it is the most cost-effective option. Thus, the QAB is the most rational choice.

At this point, the ST architecture is defined: CHB is used on the AC-DC MV stage, and the QAB is used as the basic module of the isolated DC-DC stage. In chapter 5, additional design aspects related to the system level were addressed, like optimum number of modules and the best configuration of the QAB converter. Yet in that chapter, the studies have demonstrated that the optimum number of modules is  $N_{opt} = 9$  for a grid voltage of 10 kV. Consequently, every design aspects have been discussed in previous chapters of this work.

The final step of this work is to verify experimentally the operation

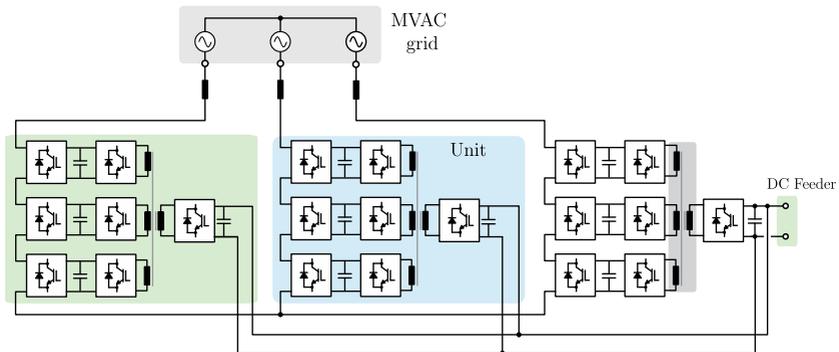
and performance of the entire ST architecture and validate the analysis covered herein. In order to achieve such goal, a prototype of the ST was built and its construction aspects are described in this chapter.

## 6.1 Hardware Description

### 6.1.1 Power Platform

As a matter of fact, 9 modules per phase is the best choice when the system is installed in a grid with voltage level of 10 kV. Nevertheless, the ST demonstrator prototype presented in this chapter is specified for lower voltage for safety reason. Hence, the line-to-line voltage employed is 2.6 kV. According to analysis presented in chapter 5, the optimum number of modules per phase for  $V_{grid} < 7$  kV is determined by:  $N_{mod(opt)} = V_{grid}$ . Thus, 3 modules per phase should be used for providing the best performance in the selected grid voltage of 2.6 kV. Fig. 6.1 illustrates then the ST architecture used for constructing the prototype, while the specification is presented in Table 6.1. As observed in Fig. 6.1, an unit comprises a QAB converter associated with three CHB cells. One unit is used per phase, resulting then in three units for assembling the entire architecture. The topology of the unit is depicted in Fig. 6.2.

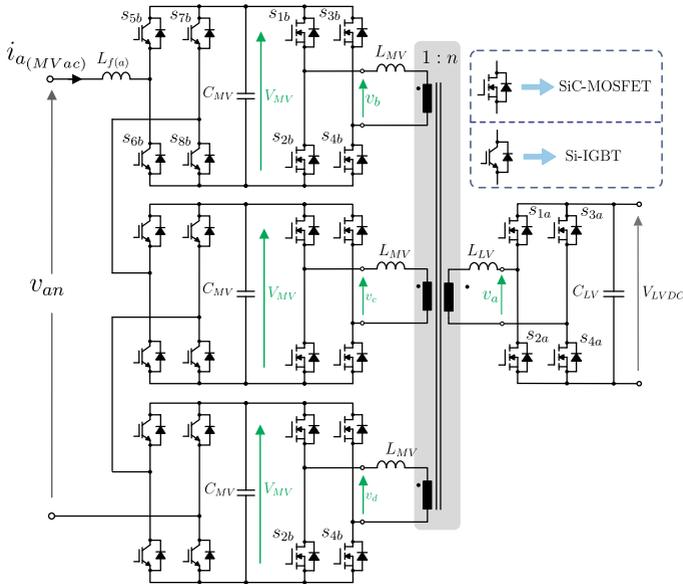
To design the system and to define the components illustrated in



**Fig. 6.1:** Architecture of the three-phase smart transformer selected for implementation and experimental evaluation.

**Tab. 6.1:** Technical specification of the ST demonstrator

<b>System Specification</b>	
System configuration	Three-phase
Total Power	100 kW
Input line-line voltage	2600 V
Input line-neutral voltage	$V_{MVAC} = 1500$ V
Total MVDC link	$V_{MVDC} = 2400$ V
Single medium voltage DC link	$V_{LV} = 800$ V
Low voltage DC link	$V_{MV} = 800$ V
<b>CHB Parameters</b>	
Nominal modulation index	$m = 0.8$
Switching frequency	$f_{s(CHB)} = 10$ kHz
IGBT	IKW40N120T2 Infineon Technology $V_{block} = 1200$ V / $V_{CE} = 1.75$ V
Capacitor bank	$C_{MV} = 1500$ $\mu$ C
Grid line inductor	$L_{ac} = 1$ mH
<b>QAB Parameters</b>	
Transformer turn-ratio	$n = 1 : 1 : 1 : 1$
Switching frequency	$f_{s(QAB)} = 20$ kHz
LV side inductor	$L_{LV} = 75$ $\mu$ H
MV side inductor	$L_{MV} = 75$ $\mu$ H
SiC-MOSFETs (MV side)	C2M0040120D Wolfspeed/CREE $V_{block} = 1200$ V / $R_{DS(on)} = 40$ m $\Omega$
SiC-MOSFETs (LV side)	C2M0025120D Wolfspeed/CREE $V_{block} = 1200$ V / $R_{DS(on)} = 25$ m $\Omega$



**Fig. 6.2:** Circuit of the power unit of the ST architecture, pointing out the semiconductors used in each converter.

Fig. 6.2, the specification presented in Table 6.1 and the equations provided in chapter 5 have been used. Hence, the selected components are summarized in Table 6.1. In order to produce a sinusoidal AC voltage with rms value of 1.5 kV line-to-ground (2.6 kV line-to-line), it is used a total MVDC link of 2.4 kV divided among the 3 modules of the power unit. This results in 800 V for the single MVDC link. Similarly, 800 V is used on the LVDC link. This value allows the use of semiconductors rated for 1.2 kV of blocking voltage.

As specified in Table 6.1, the switching frequency of the CHB is 10 kHz, which leads to an effective frequency of 30 kHz on the AC filter. This frequency leads to low switching losses, while maintains low filter volume. In virtue of the low commutation frequency, IGBTs optimized for reducing the conduction losses can be properly employed and then the device IKW40N120T2 from *Infineon Technology* is adopted. This IGBT is recommended in application up to 10 kHz and it very suitable in this case.

The QAB, on the other hand, has a switching frequency of 20 kHz,

which provides a good trade-off between magnetic elements volume and isolation issues, due to the partial discharge, as discussed in chapters 3 and 4. The SiC-MOSFETs from *Wolfspeed/CREE* were employed in both sides of the converter. The device C2M0040120D, which has a  $R_{DS(on)} = 40 \text{ m}\Omega$ , was used on the MV side, while the device C2M0025120D with  $R_{DS(on)} = 25 \text{ m}\Omega$  was used on the LV side. The semiconductors with lower  $R_{DS(on)}$  was selected for the LV side in order to reduce the conduction losses, once the current level in this side is very high. The inductance and capacitance are also presented in Table 6.1.

The DC link capacitor bank of the MV cells comprises 8 capacitors of  $270 \text{ }\mu\text{C}/500 \text{ V}$  and 4 capacitors of  $1000 \text{ }\mu\text{C}/450 \text{ V}$ . Four capacitors of  $270 \text{ }\mu\text{C}/500 \text{ V}$  and 2 capacitors of  $1000 \text{ }\mu\text{C}/450 \text{ V}$  are connected in parallel, forming an array. Hence, two of these arrays connected in series (to share the 800 V of the individual MVDC link) are used to build the entire DC link capacitor bank. This result in a total capacitance of  $C_{MV} = 1500 \text{ }\mu\text{C}$ .

The required inductance of the QAB converter was split, in order to be implemented in either MV and LV sides. Each side requires an inductance value of  $75 \mu\text{H}$ , which has been physically implemented considering the E-core shape from *TDK/Epcos* and using the parameters presented in Table 6.2. These parameters were obtained from the inductor design, using the procedure already discussed in chapter 4. Similarly, the high frequency multiwinding transformer has been implemented considering the parameters shown in Table 6.3, where a ferrite (N87) material core with *U* shape from *TDK/Epcos* has been adopted. Since the DC voltages on the LV and MV sides are equal, the transformer has a turn ratio of 1:1:1:1. The different winding of the transformers were implemented using the interleaved approach, leading to small leakage inductance. Fig. 6.3 (a) illustrates the picture of the implemented transformer, as well as the inductors (either LV and MV sides) connected to it.

Small current ripple on the MVAC lines is expected and then an AC line inductor is used in each phase, in order to maintain a maximum current ripple on 15% of its nominal value. To achieve this current ripple, an inductance of  $L_{ac} = 1 \text{ mF}$  is required. This value was calculated according to [66], considering the maximum peak current of 30 A and  $m = 0.8$ . The AC line inductors of the CHB were also implemented using two ferrite cores UU93/76/30 connected in parallel, where

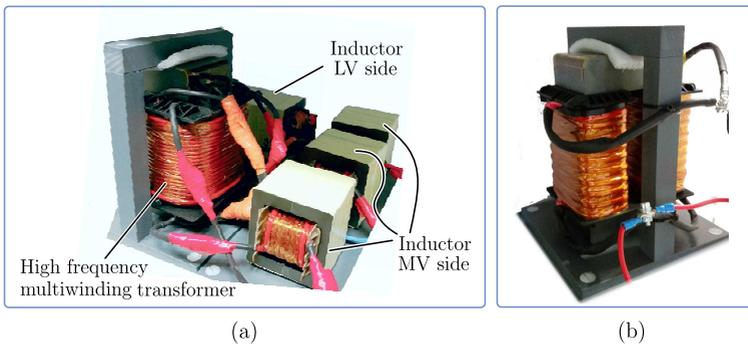
54 turns were required to achieve such inductance. The picture of the

**Tab. 6.2:** Parameters of the inductors used on the QAB converter

	MV side	LV side
Inductance	$L_{MV} = 75 \mu H$	$L_{LV} = 75 \mu H$
Core	2 x EE70/33/32	4 x EE70/33/32
Number of turns	$n_{LMV} = 9$	$n_{LMV} = 9$
Litz-wire	1260 x 0.071 mm	512 x 0.1 mm (3 in parallel)

**Tab. 6.3:** Parameters of the transformer used on the QAB converter

QAB Transformer	
Turns ratio	1:1:1
Core	2 x UU93/76/30
Number of turns of the LV side	$n_{LV} = 21$
Number of turns of the MV side	$n_{MV} = 21$
Litz-wire	512 x 0.1 mm



**Fig. 6.3:** Picture of the magnetic used on the ST demonstrator: (a) high frequency multiwinding transformer and the the inductors of the QAB converter, (b) ac line inductor of the MV stage converter.

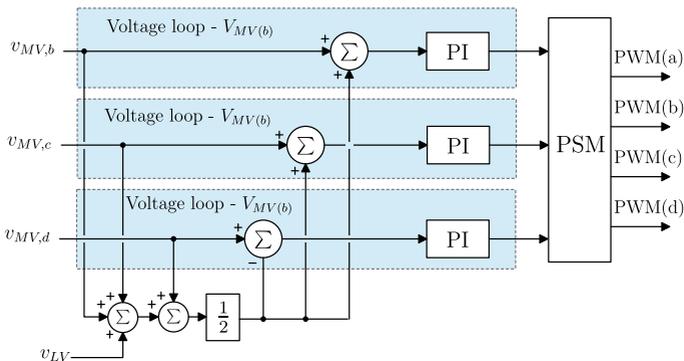
implemented transformer is depicted in 6.3 (b).

As a matter of safety, the tests in the laboratory were carried out with reverse power flow, i.e. power flowing from the LV side to the MV. Consequently, a 800 V DC source was connected, while the resistive loads were used on the MV side.

### 6.1.2 Control Platform

The control stage is based on multiple microcontrollers, where all control loops are implemented in it. Fig. 6.6 shows the scheme of the power and control platforms and the information exchange among them. As observed in this figure, 7 microcontrollers MPC5643L floating point DSP (32-bit CPU, 60 MHz) from *Freescale Semiconductor* were used. In fact, 2 microcontrollers are used per phase: one for controlling the CHB and other for controlling the QAB.

As mentioned before, the control system is not the focus of this work, but it needed to be implemented, in order to make the system operational. The implemented control differs from that scheme presented in chapter 5, because the tests now are realized with reverse power flow, and considering a DC source connected to the LVDC link (avoiding the needed of the LVDC link control, as presented in the previous chapter). Moreover, the prototype uses passive loads, requiring then an additional output voltage loop on the MV side. For these reasons, different control structure needed to be used for testing the prototype. In the new control structure, the QAB controls the individual DC links of the MV



**Fig. 6.4:** Block diagram of the control scheme of the QAB converter.

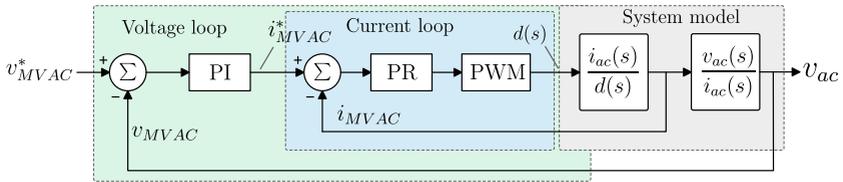


Fig. 6.5: Block diagram of the control scheme of the CHB converter.

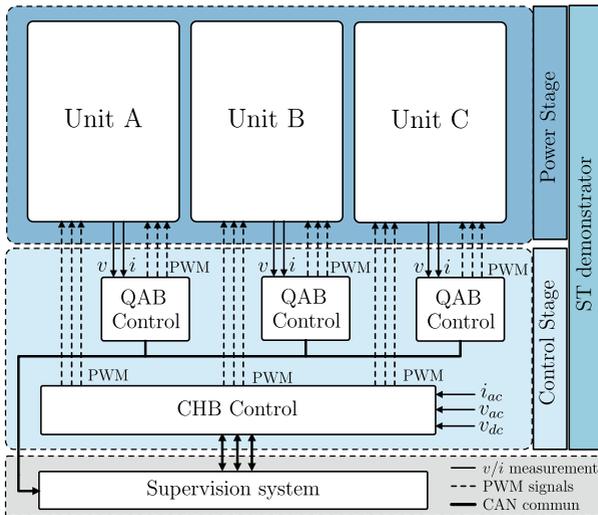


Fig. 6.6: Block diagram of the implemented ST demonstrator, comprising the power and control platforms.

side, while the CHB controls the MV AC current and voltage. The block diagram of the control scheme of the QAB converter and CHB are depicted in Fig. 6.4 and Fig. 6.5, respectively. As observed, the CHB control has two control loops: an outer loop that controls the AC voltage, using an *PI* controller, and a inner current loop, based on a *PR* compensator.

Fig. 6.6 shows the scheme of the power and control platforms, and the interface among them. As mentioned, there is one microcontroller dedicated for each QAB, and one microcontroller for each phase of the CHB converter, resulting in 6 microcontrollers. They communicate among them using the CAN communication bus, as shown in Fig. 6.6.

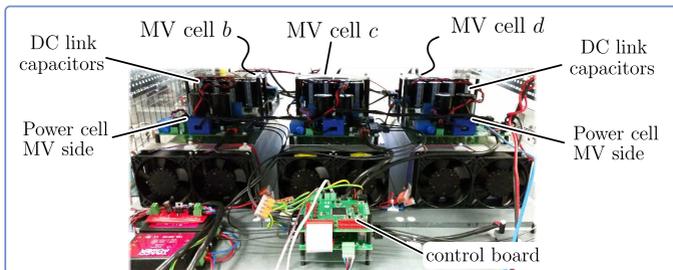
An additional microcontroller is used as supervision for guaranteeing the synchronization among the microcontrollers.

## 6.2 Final Assembly and Test Set-up

The final assembly of ST prototype uses three units, one per phase, and each unit is composed by two separated hardware part: LV side hardware and MV side hardware. The LV side hardware comprises the power converter (LV side cell of the QAB), the capacitor bank of the LVDC link, as well as the magnetic components: AC side inductor (connected to the MV grid), multiwinding transformer and the inductors of the QAB converter. The MV side hardware consists in three cooling system (heatsink and forced air cooling), one of each combination of QAB and CHB cells, as depicted in Fig. 6.7. It means that the QAB and CHB bridges shares the same cooling system. Moreover, the capacitor bank for each of the MV bridges is included in this part.

### 6.2.1 Final Assembly

The final assembly of the three-phase ST demonstrator is illustrated in Fig. 6.8. As noticed, the two parts described before comprises a phase, and each phase are stacked on the power rack. There is an auxiliary power supply and a control platform dedicated for each phase. The control system of each phase communicates through CAN bus with the master controller, which is responsible for the synchronization of the phases.

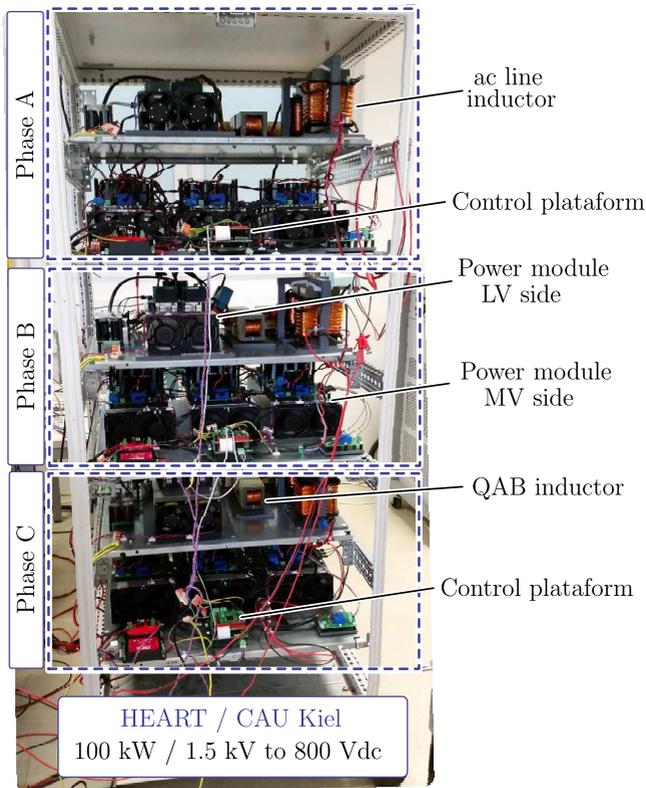


**Fig. 6.7:** Block diagram of the control scheme of the QAB converter.

## 6.2.2 Test Set-up Description

For the experimental evaluation, the ST demonstrator was placed in a safety area with restricted access, enabling the test with high voltage level. The currents and voltages measurements were collected and sent to the accessible area, called as control area, where the measurements equipments were located. The schematic of the test set-up is depicted in Fig. 6.9.

The ST demonstrator was tested with reserve power flow, i.e. the power is transferred from the LV side to the MV side, because this condition provides a safer test case, since a MV grid does not need to be



**Fig. 6.8:** Picture of the implemented ST demonstrator: 100 kW, 1500 Vac to 800 Vdc.

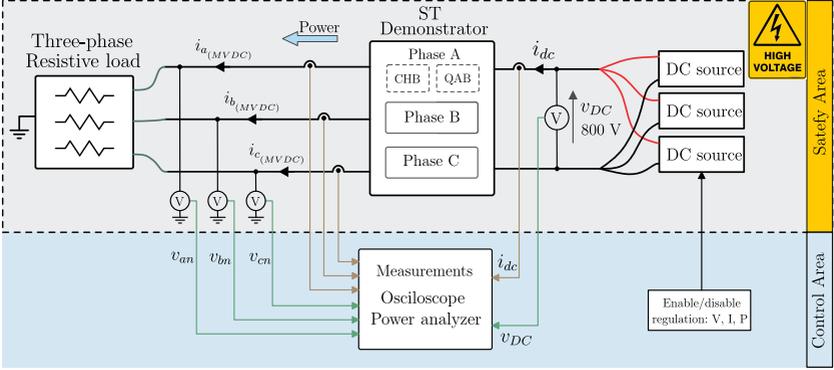


Fig. 6.9: Scheme of the test set-up on laboratory.

connected to the prototype. As observed in Fig. 6.9, three DC sources were connected to the LVDC link, providing the expected 800 V. In the MV side, resistive three-phase load were used. The ST demonstrator, DC source and loads were placed in the test area, while the measurements equipments were placed on the accessible area. Besides that, the DC sources were controlled from the control area, where current and power limitation could be defined and the voltage controlled.

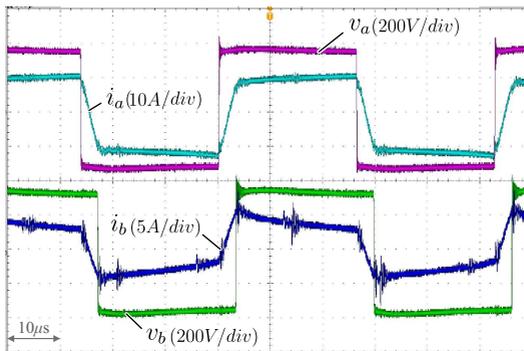
## 6.3 Experimental Results

The experimental results consist in the main current and voltage waveforms of the converter operating in steady-state. As a matter of safety, the prototype was tested with a maximum voltage of 500 V on the LVDC link, resulting in a total MVDC link of 1500 V. In this condition, the system creates an output line-to-neutral voltage of 900 V, implying in a line-to-line voltage of around 1500 V. The main waveforms are presented from Fig. 6.10 to Fig. 6.14.

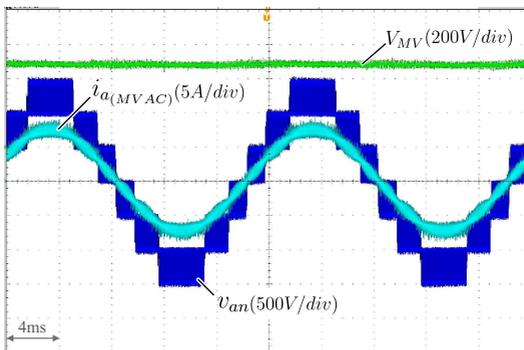
Initially, the operation of one unit is analyzed, where the main waveforms of both stages comprised in one power unit (i.e. the DC-DC stage and MV stage) are obtained. These results are presented in Fig. 6.10 and Fig. 6.11. The Fig. 6.10 shows the result for the QAB converter, where the voltage and current on the AC side of the MV bridge ( $v_b$  and  $i_b$ ) and LV bridge ( $v_a$  and  $i_a$ ) are depicted. From this result, the phase-shift operation is observed. Moreover, the current on the inductor  $L_a$

( $i_a$ ) is negative during the transition of  $v_a$  from negative to positive (see Fig. 6.10), implying in zero voltage over the switches when they turn-on. It indicates the soft-switching operation of the converter, as expected.

Similarly, Fig. 6.11 and Fig. 6.12 show the output AC voltage and current for the system operating with power level of 4 kW and 10 kW, respectively. Fig. 6.11 shows the line-to-ground output voltage



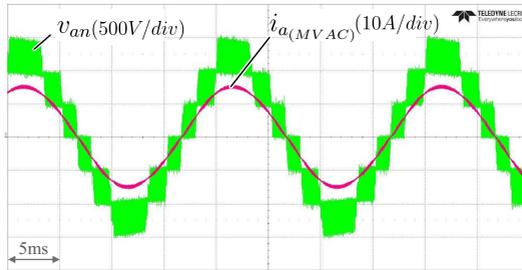
**Fig. 6.10:** Experimental results of the ST demonstrator. Current and voltage waveforms of the dc-dc stage: LV side ( $v_{La}$ ,  $i_{La}$ ) and MV side ( $v_{Lb}$ ,  $i_{Lb}$ ).



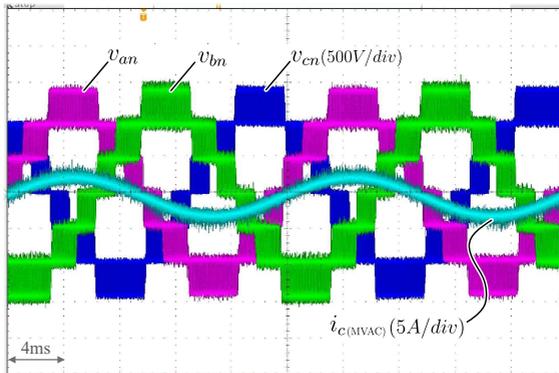
**Fig. 6.11:** Experimental results of the ST demonstrator working with 4 kW of output power: voltage of the individual MVDC link ( $V_{MV}$ ), line-to-neutral output voltage before the inductor filter ( $v_{an}$ ) and the output current ( $i_{aMVAC}$ ).

(before the ac filter) and AC current of the system, i.e. CHB stage, as well as the voltage of a single MVDC link ( $V_{MV}$ ). From these results, the 7-level output voltage with a peak voltage of 1500 V is observed. Furthermore, the sinusoidal current waveform is observed, as well as a regulated DC voltage of  $V_{MV} = 500$  V.

The results of the three-phase system operating in light load, i.e. 9 kW, are depicted in Fig. 6.13 and Fig. 6.14. In Fig. 6.13, the three-phase line-to-ground voltage (unfiltered,  $v_{an}$ ,  $v_{bn}$  and  $v_{cn}$ ) of the ST is depicted, as well as the line current  $i_{c_{MVAC}}$ . Likewise, the three-phase output currents ( $i_{a_{MVAC}}$ ,  $i_{b_{MVAC}}$  and  $i_{c_{MVAC}}$ ), as well as the voltage



**Fig. 6.12:** Experimental results of the ST demonstrator working with 10 kW of output power: line-to-neutral output voltage before the inductor filter ( $v_{an}$ ) and the output current ( $i_{a_{MVAC}}$ ).

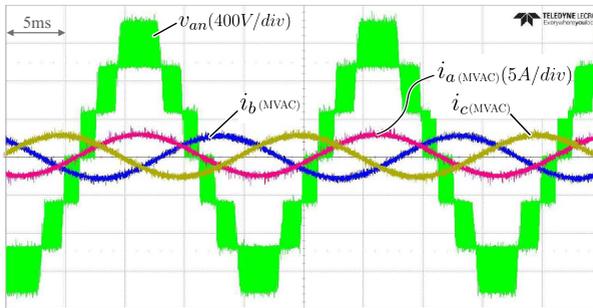


**Fig. 6.13:** Experimental results of the ST demonstrator: three-phase output voltage before the filter ( $v_{an}$ ,  $v_{bn}$  and  $v_{cn}$ ) and the output current ( $i_{c_{MVAC}}$ ).

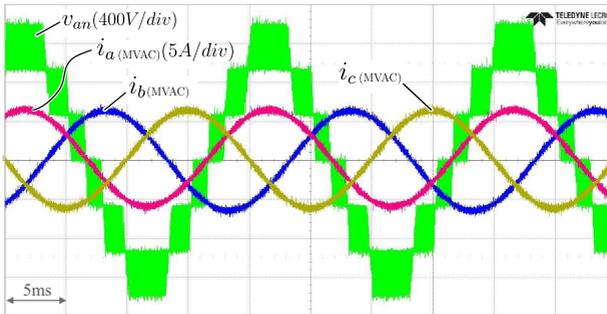
$v_{an}$  are depicted in Fig. 6.14.

Similarly, Fig. 6.15 presents the three-phase output currents ( $i_{a_{MVAC}}$ ,  $i_{b_{MVAC}}$  and  $i_{c_{MVAC}}$ ) and the voltage  $v_{an}$  for the system operating with total power of 25 kW. These results demonstrate the proper operation of the three-phase ST system, as well as a good regulation of the output voltage.

Finally, the efficiency of the entire system was measured using the high performance power analyzer WT1800 from *Yokogawa*, and the efficiency curve as a function of the output power is illustrated in Fig. 6.16. The ST demonstrator was tested with maximum power of 10 kW

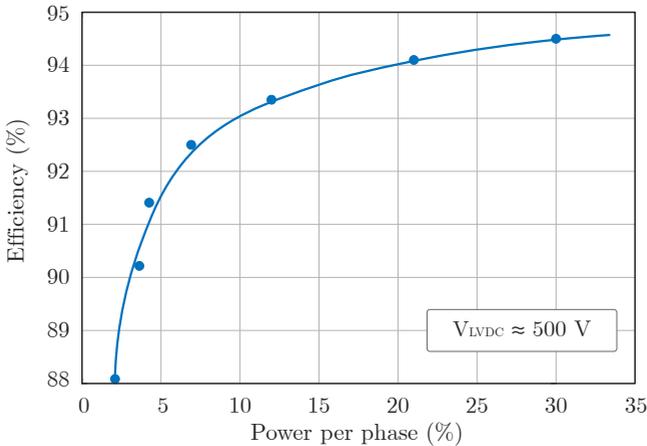


**Fig. 6.14:** Experimental results of the ST demonstrator operating with power level of 9 kW: three-phase output current ( $i_{a_{MVAC}}$ ,  $i_{b_{MVAC}}$ ,  $i_{c_{MVAC}}$ ) and the voltage before the filter ( $v_{an}$ ).



**Fig. 6.15:** Experimental results of the ST demonstrator operating with power level of 30 kW: three-phase output current ( $i_{a_{MVAC}}$ ,  $i_{b_{MVAC}}$ ,  $i_{c_{MVAC}}$ ) and the voltage before the filter ( $v_{an}$ ).

per phase and maximum voltage of 500 V on the LV side, i.e. 1500 V on the MV side, in virtue of the voltage probes limitation. The power analyzer WT1800 can measure voltages up to 1500 V, limiting the system to reach its maximum voltage. The measured efficiency is illustrated in Fig. 6.16 up to 30% of the nominal power (10 kW per phase). As noticed, the ST presents an efficiency of 94.5% for 30% of the nominal power, that is the maximum output power tested. It is a notable result, considering that the system consists in two power processing stages (MV stage and DC-DC stage). Moreover, the results were obtained for 65% of the nominal voltage of the system (i.e. 500 V instead of 800 V), which deteriorates considerably the efficiency, since the semiconductors are not operating at their best performance condition. Hence, operating at nominal voltage, the ST demonstrator is supposed to present better performance. Still analyzing the efficiency curve, it continues to increase for higher output power. In overall, the efficiency obtained so far is quite notable, demonstrating the high performance of the ST architecture.

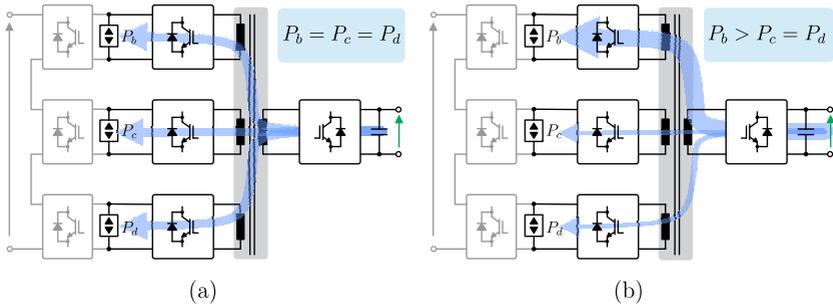


**Fig. 6.16:** Efficiency curve of the ST demonstrator as a function of the output power (in percentage) obtained experimentally.

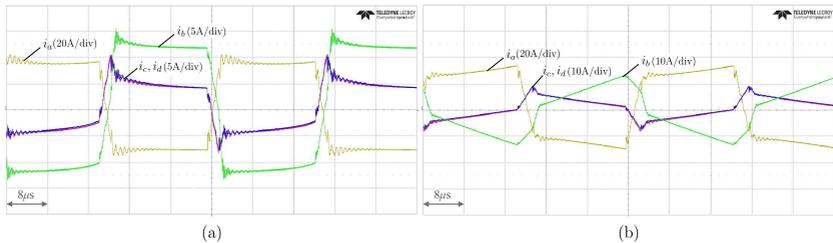
### 6.3.1 Power Routing Application - System's Performance Analysis

An important promises of the HEART project is to improve the system's reliability using the power routing approach [48], as discussed in chapter 1. The ST architecture has been conceptualized in this work considering as one of the requirements the possibility to implement the power routing strategy efficiently. In this sense, the system's performance is evaluated experimentally, considering unbalanced power condition on the QAB, i.e. different power on the cells of the QAB converter.

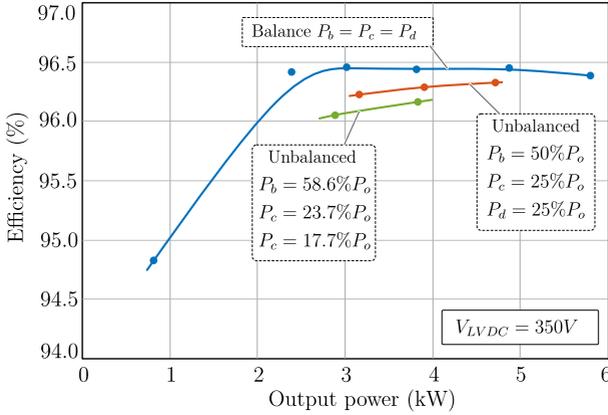
In normal condition, the QAB converter and CHB work with the output power distributed equally among their cells, i.e. balanced condition, as illustrated in Fig. 6.17 (a). When power routing strategy is applied to the ST, the QAB and CHB cells are loaded unequally, as



**Fig. 6.17:** Scheme of the power unit considering: (a) balanced power condition ( $P_b = P_c = P_d$ ) and (b) unbalanced power condition ( $P_b > P_c = P_d$ ).



**Fig. 6.18:** Waveforms of the currents (either MV and LV sides) of the QAB converter operating under unbalanced power condition: (a) output power  $P_o = 3kW$ , (b)  $P_o = 5kW$ .



**Fig. 6.19:** Efficiency curve of the QAB converter as a function of the output power obtained experimentally considering balanced and unbalanced power conditions.

depicted in Fig. 6.17 (b), to improve the lifetime of the overall system. This latest condition has been tested in laboratory, considering the scheme illustrated in Fig. 6.17 (b) (i.e. the CHB was not considered), and the experimental results are presented in Fig. 6.18. The results show the current on the LV bridge ( $i_a$ ) and MV bridges ( $i_b$ ,  $i_c$  and  $i_d$ ) of the QAB converter considering that the bridge  $b$  is processing twice more power than the bridges  $c$  and  $d$ , i.e.  $P_b = 50\%P_o$ ,  $P_c = P_d = 25\%P_o$ , where  $P_o$  is the output power. The Fig. 6.18 (a) shows the current waveforms for the converter operating with output of 3 kW, while in the Fig. 6.18 (b) the converter is working with output power of 5 kW. These results demonstrate the ability of the converter to work under unbalancing power condition, which is required for the power routing implementation.

To verify the effect of the unbalance power processing on the converter's performance, the efficiency curve of the QAB converter was measured considering balanced and unbalanced power and the result is depicted in Fig. 6.19. The tests to obtain the efficiency curve were carried out with input voltage of 350 V on the LVDC link, implying in a total MVDC link of 1050 V. The efficiency has been measured under three operation cases: (1) balanced condition:  $P_b = P_c = P_d = 33\%P_o$ ; (2) unbalanced condition  $P_b = 50\%P_o$ ,  $P_c = P_d = 25\%P_o$ ; (3) total

unbalanced case:  $P_b = 58.6\%P_o$ ,  $P_c = 23.7\%P_o$ ,  $P_d = 17.7\%P_o$ . The three curves are illustrated in Fig. 6.19. For unbalanced cases, only two points were saved for safety reasons. From this result, it can be noticed that the efficiency of the QAB converter is only slightly deteriorated when the power routing strategy is used. The efficiency reduction is explained by the higher rms current on the bridge  $b$ , which increases the conduction losses non-linearly.

Nevertheless, the deterioration is less than 0.5% for the more extreme unbalanced case. Thus, the power routing strategy is worthy of implementation, once the lifetime of the system can be improved, according to [48], considering only a small reduction of the efficiency. Furthermore, the efficiency reduces in 0.5%, only for extreme unbalancing case, which does not happens in real application. In real case, the power imbalance is expected to be smaller than that forced in this work.

## 6.4 Conclusion

The analysis and design of the ST architecture were discussed in previous chapters, considering either the converter level and system level. As a final step, a prototype was built and evaluated experimentally to validate the analysis presented in this work. The detail of the construction and experimental results were then presented in this chapter.

The prototype of the ST is based on the three-phase architecture and it consists in two power processing stages (the MV stage and DC-DC stage), i.e. the LV stage was not considered. One unit composed by the QAB converter and the CHB is used per phase, resulting in a total of three units. The ST demonstrator has a power level of 100 kW, a line-to-line input AC voltage of 2600 V and an output DC voltage of 800 V.

The system has been intensively tested, considering reverse power flow for safety reasons. The laboratory evaluation has shown a proper operation of the smart transformer. A well regulated voltage provided by the QAB, and a sinusoidal voltage and current regulated by the CHB were observed. Furthermore, an efficiency of 94.5% was obtained for 30 % of the total output power (for an LVDC link of 500 V). Additionally, the system is supposed to present even higher efficiency, if 800 V is used on the LVDC link. In overall, the results obtained so far for the ST architecture is quite notable, demonstrating its high performance

and the theoretical analysis presented in previous chapters. Finally, the system has been tested with unbalanced power condition, and the ability to implement the power routing strategy has been demonstrated. This strategy has minor impact on the system's performance.



# Chapter 7

## Conclusion and Outlook

### 7.1 Summary

**T**HE solid state transformer has received a lot of attention in the last decade as a potential technology to replace the traditional LFT, while providing benefits in terms of volume and weight reduction. This feature is achieved in virtue of its high frequency isolation, which reduces drastically the size of the passive components. Therefore, this device was applied initially in electric locomotive, and it has been presented as an efficient and compact solution. Besides the advantages achieved in terms of hardware, the power electronics involved in the SST enables the implementation of an advanced control strategy, allowing the implementation of multiple control loops (e.g. power, voltage and current). In this sense, a new concept was presented: the Smart Transformer (ST). The ST is a SST with high capability to control currents and voltages, managing the power more efficiently. This extra ability makes the ST very suitable for application in electric distribution system, in which power and voltage control is the central requirement.

In this application, the ST can perform as a LFT (replacing it), while providing ancillary services to the grid through its high advanced control platform, improving the overall power quality of the distribution grid.

In this context, this thesis has investigated suitable architectures and power converters for implementing efficiently the smart transformer. To define the most suitable architecture, the requirements for the ST in

distribution grid application were collected and they are listed as: capability to implement a multiloop control (for providing ancillary services to the grid), high efficiency, high reliability, low cost, possibility for providing dc connectivity for dc source/loads. Of course, it is not yet possible to achieve a very high efficiency, with very high reliability and very low cost. Thus, the trade-off between these parameters were evaluated and discussed herein, in order to find the best compromise among them. Thereafter, an extensive literature review was carried out, and the most promises ST architectures concepts and power converters were highlighted.

The ST architecture composed by three power processing stages, i.e. MV stage, DC-DC stage and LV stage, with a constant DC link provides the decoupling between the LV and MV side. Hence the control of the LV side and MV side converters are fully independent from each other, providing more degree of freedom for the control system. To handle the MV level involved in this system, the modular approach is used, where the MV stage and DC-DC stage are based on basic building blocks that share the total voltage. This approach offers the benefits of: fault tolerance through redundancy, scalability in voltage and power, possibility to use low voltage rating devices (providing better performance and broad choice of devices), and the possibility to improve the reliability through the power routing technique [48]. Furthermore, using this approach, the cell once designed can be combined and installed in places with different grid voltage. For instance, Japan has a grid voltage of 6.6 kV, while the grid voltage in USA is 13.8 kV, requiring a specific design of the ST architecture for each of these two places. However, using the modular approach, the basic cell can be designed only once and combined differently to compose the entire system, according to the installation place. In essence, the specification of the ST systems used and Japan and USA are different, but the basic cells used to construct the entire system are the same. This plays an important role during industrialization of the system. For these reasons, the ST architecture is based on three stage modular architecture.

## 7.2 Conclusion

From the research carried out in this thesis, the conclusions can be divided in three parts: power converter level, system level and device level.

## 7.2.1 Power Converters Level

### Topologies Choice:

Regarding the power converters, the most promises topologies were evaluated for each power processing stage. For the MV stage, the CHB and MMC are highlighted as the most suitable topologies. Comparing them, the CHB has more advantages in terms of number of components, capacitance requirement and simplicity. Hence, it is the preferred candidate for implementing the MV stage. Similarly, several DC-DC converters options are available to be used as the basic module of the modular DC-DC stage. Among them, the MAB and SRC are highlighted as the most suitable options, and both were investigated. For the LV stage, well-established topologies (e.g. 3 level VSI or 2 level VSI) can be used, which are mature technology and do not deserve to be investigated. For this reason, the LV stage was not considered in this work.

### DC-DC Series Resonant Converter:

The SRC is pointed out as a candidate to be used as a basic cell to implement the DC-DC stage of the ST, because it is supposed to achieve high efficiency. Nonetheless, not only the efficiency is important, but also the reliability and then both parameters were taking into account during the analysis of the converter. To increase the reliability, the two most critical devices were analyzed: the primary side semiconductor and the resonant capacitor. To avoid fault on the switch, a fault-tolerant SRC topology was proposed to be used instead the classic one, avoiding the interruption of the system in faulty case. The proposed fault tolerance method consist in re-configuring the FB-SRC in a HB-SRC, in case of a semiconductor failure, keeping the converter operational. The main advantages of the proposed converter are: post-fault operation, simple implementation, reduced number of additional component and no efficiency deterioration. As a drawback, the resonant capacitor must be designed for higher voltage and the current effort on the healthy devices in failure mode operation is twice higher than in normal mode operation.

To improve the reliability of the resonant capacitor, its lifetime model is used and the trade-off between the resonant tank parameters selection was found. As a results, the resonant tank circuit should

have the highest capacitance value ( $C_r$ ) and smallest inductance value ( $L_r$ ) possible (for a given resonant frequency). Following this procedure, the capacitor lifetime is extended. In that case, only the leakage inductance of the transformer should be used as the resonant inductor, and no additional component needs to be included.

A multi-objective optimization design (optimizing efficiency and reliability) was carried out, the prototype was built and then evaluated experimentally. The converter was tested under fault condition, demonstrating its high reliable characteristic. Furthermore, the proposed converter has obtained a peak efficiency of 98.61%, validating the presented design.

Nevertheless, the SRC has no control capability, since it operates in open loop. It limits the control possibilities of the overall ST system. This is the main drawback of this topology.

### **Multiple Active Bridge DC-DC Converter:**

The MAB converter offers a valuable trade-off between cost and efficiency when used as a basic module of the modular ST system. Besides cost and efficiency, this converter has enough degree of freedom to control the currents and voltages, contributing to enhance the controllability of the overall system. Regarding the modulation strategy, it has been demonstrated that the PSM provides low current stresses on the semiconductors, inductors and transformer, besides to be simple to implement. Moreover, its soft-switching feature does not depend on the converter parameters, as the inductance for instance.

A multi-objective optimization algorithm (for improving cost and efficiency) was developed for designing the converter, and the performance of the converter was evaluated experimentally when SiC-MOSFETs and Si-IGBT are used. The experiments have shown an outstanding efficiency result of 97.5%, when SiC-MOSFETs were employed, which is the highest obtained so far for this kind of converter. Regarding the converter's performance with different semiconductors technology, it was verified that the SiC-MOSFETs is more advantageous, due to its low energy losses, almost ZVS operation (during the switch turn-off) and the conduction of the reverse current through the channel, instead the diode, reducing the conduction losses. Consequently, the use of SiC-MOSFETs reduced the converter's losses in around 57%, compared to the IGBT. These results demonstrate the feasibility of this technology is such application.

### 7.2.2 System Level

From system level perspective, the optimum number of modules and the best configuration of the QAB converter were investigated taking the cost and performance into account.

With the aim to determine the optimum number of modules, the trade-off between cost and performance of the system was analyzed, according to the number of module. To do so, an algorithm was implemented to compute losses and cost, and the system was designed for different number of modules: from 5 modules to 15 modules. From this investigation, it was noticed that the system presents the best performance when nine module are employed, for a grid voltage of 10 kV.

Different configurations of the QAB converter were described in Chapter 5. Then, three ST architectures based on QAB were defined: Asymmetrical QAB (AQAB), Symmetrical QAB in voltage (SQAB-V) and Symmetrical QAB in power (SQAB-P). Thereafter, they were then compared in terms of efficiency, cost and complexity, with the aim to determine which one is the best solution for ST application. Furthermore, the classic architecture using the DAB was also included in this comparison. The comparison has shown that the AQAB architecture presents the best performance in terms of efficiency and cost. Compared to the conventional DAB solution, the AQAB can reduce the cost of the system in around 20%. The efficiency of both solution are very similar, only a slightly improvement of 5% is obtained in the AQAB.

### 7.2.3 Device Level

The performance of the individual converters and the full system were evaluated, considering Si-IGBT and SiC-MOSFETs.

Considering the most promising ST architecture (i.e. using the AQAB converter in the DC-DC stage and 9 modules per phase), the use of SiC-MOSFETs instead of Si-IGBT offers a losses reduction of around 10%, but it increases the cost of the system in around 40%. Therefore, to verify the economic feasibility of such devices in this application, a study considering the energy saving over time and the installation cost should to be realized.

### 7.2.4 General Conclusions

In overall, some remarks can be highlighted regarding the ST architecture for grid application:

- ▶ The three-stage modular architecture has several advantages for implementing the ST, like: high control possibility, connectivity to the DC link, fault tolerance through redundancy, scalability in voltage and power and possibility to implement the power routing strategy.
- ▶ For the MV stage, the CHB and MMC are the most suitable topologies. Comparing them, the CHB shows superior results over the MMC in terms of number of components, capacitance requirement and simplicity.
- ▶ The SRC DC-DC converter is the first option to be used as a basic cell of the dc-dc stage. The topology of a fault tolerant SRC has been proposed and investigated in detail. The proposed converter presents as main advantages: post-fault operation, simple implementation, reduced number of additional components and no deterioration of the efficiency. The drawbacks are: the resonant capacitor must be designed for higher voltage, and the current effort on the healthy devices in failure mode operation is twice than in normal mode operation. The investigation has shown that the lifetime of the series resonant capacitor ( $C_r$ , which is the second most susceptible device to failure) can be improved, by properly selecting the elements of the tank circuit. In this case, the inductance  $L_r$  must be the lowest possible and the resonant capacitor  $C_r$  must be the biggest possible. An efficiency of 98.61% has been demonstrated experimentally for the SRC in this work, which is a notable result.
- ▶ The QAB converter is the most promising choice for implementing the modular DC-DC stage of the ST, because it has high performance and economic advantages. The asymmetric configuration, where three bridges are connected to the MV side and one to the LV side, is the most economic one, because few devices are used, contributing significantly for cost reduction. Adopting the QAB instead of the DAB in the DC-DC stage, the system's cost can be reduced in 20%. The efficiency of both solutions are very similar, only a slight improvement of 5% is obtained in the AQAB. The

converter allows also the implementation of an advanced control system and the possibility to implement the power routing approach.

- ▶ A prototype of the three-phase ST architecture, comprising the MV stage and DC-DC stage, was built and tested in laboratory. The ST architecture was designed for 100 kW of output power, line-to-line voltage of 2.6 kV and LVDC link of 800 V. The converter was tested up to 10 kW per phase, achieving an efficiency of 94.5%. Additionally, the performance of the QAB converter was tested individually, showing an efficiency of around 96.5%. Furthermore, the QAB was tested for unbalanced power condition. The results has shown a minor deterioration on the efficiency of the converter, i.e. less than 0.5%.

The results of the entire system have validated the operation and the high performance of the ST architecture. Moreover, high efficiency is expected, once the system has been tested with limited voltage (up to 1500V) and limited power (up to 30 kW).



# Appendices



# Appendix A

## Failure Analysis of the DC-DC Converter: A Survey

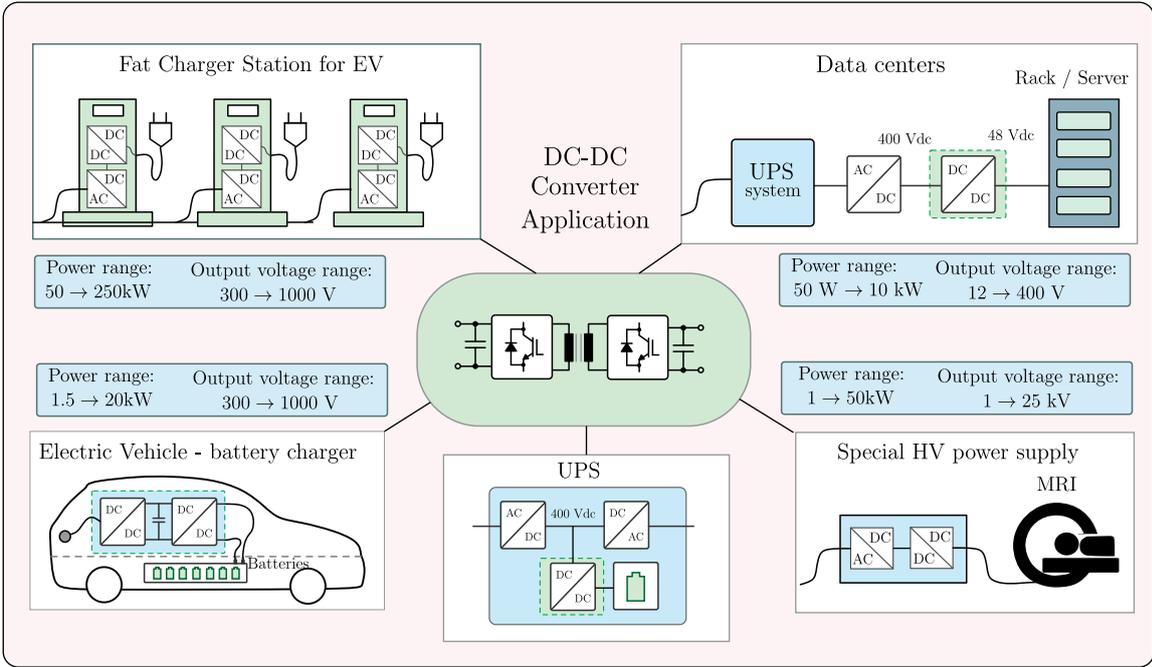
**T**HE rapid evolution of the power electronics and information theory in the last decades enable the arise of new technologies in diverse areas of application, such as electric vehicles (EV), fast charger station, uninterruptible power supply system (UPS), medicine, data processing (and data center) and others. All these applications contain at least one dc-dc converter for adapting the voltage and/or control the power and current transferred between distinguished buses. Fig. A.1 shows examples of the those aforementioned applications, in which the dc-dc converters are highlighted. The Dual-Active-Bridge (DAB) and Series-Resonant Converter (SRC) are the most adopted converter in this application because their characteristics of soft-switching, low EMI and high power density. In industry, the SRC became even more popular and its variant, the LLC converter, has gained more attention. Nowadays, the SRC and LLC are widely adopted in industry in many applications.

In EV, faster charger station and UPS systems the dc-dc converter are mostly used as battery charger, while in data center it is used also to adapt the voltage and supply the server. Thus, each application imposes different requirements in terms of power level, voltage level and control for their dc-dc converters, as pointed out in Fig. A.1. On the

other hand, all these converters have common requirements, independently for the application: (1) high efficiency, (2) high reliability and (3) low production cost. Indeed, the overall cost is the most relevant aspect of the converter from the industry's viewpoint and the reliability and efficiency affect directly the operation cost. The efficiency is directly related to the energy saving in each application, resulting then in low energy cost over the years, while reliable converters reduce the cost of maintenance and warranties. Thus, both features deserve much attention during the converter design.

Over the past years, many researches have been focused on efficiency improvement of dc-dc converters and several design optimization methods and power converter topologies have been discussed [16, 17, 19, 33, 48, 49, 51, 80, 96]. On the other hand, there is a lack of information about the reliability assessment for dc-dc converter. Yet, robustness is considered even more important than the efficiency in many industrial application, because an interruption of the power flow can be very costly. In contrast, very few papers have attempt to improve the converter's reliability by the mean of fault tolerance approach [113, 114].

To improve the robustness and availability of the converter, it is necessary to understand precisely the possible failures and subsequently propose some strategy to avoid or postpone them as much as possible. In this context, this paper aims to identify the most vulnerable devices to failure of the dc-dc converter, considering different application, and how these failures can be avoided. To take advantage of the industry experience and academia knowledge in this field, a survey had been carried out to recognize the most faulty devices and this is discussed in detail in Section II. Thereafter, a review of possible solution proposed in literature to avoid such failures are presented in Section III, in which advantages, drawback and applicability of each of them are discussed.



**Fig. A.1:** Example of different applications of the dc-dc converter, pointing out the usual range of power and voltage in each of these applications.

section Failure Analysis of the DC-DC Converter: A Survey Two different approaches can be used to quantify analytically the reliability of the converter: the statistical approach based on the constant failure rate [160, 161] or the physics-of-failure (PoF) [160, 162–164]. The first method uses the constant failure rate for converter’s components according to the military handbook MIL-HDBK-217F [165], regardless the application or condition that the devices are subjected to. It means that each component of the converter is considered a ‘black-box’ with constant failure rate determined by the military handbook MIL-HDBK-217F and then standard metric (e.g. Mean Time Between Failure [MTBF], Mean Time To Failure [MTTF]) are adopted to quantify how robust the converter is. This approach might lead to inaccuracy results, once all metrics are considered constant, regardless the condition, and no wearout is taken into account. In contrast, the second methodology investigates deeply the possible causes of failures for each device, considering the conditions (voltage, current, temperature, etc.) and the mission profile of the converter. The PoF has a high level of accuracy, but it is paid off by the high effort of modeling and computational implementation. Besides, the results are truthful for this specific converter and application (mission profile). Whereas the first approach is considered outdated, the second one requires too many data and very high computational effort and it is valid a single application case.

This work does not intend to quantify analytically the reliability of the dc-dc converter, but to identify the device most prone to fail in field, considering different applications and conditions. Moreover, only substantial and trustworthy data obtained either from academia and industry were taken into account.

### A.0.1 Methodology of the Study

To collect a meaningful amount of relevant data for this study, a survey was carried out, in which several questions related to the converter failure were conceived and distributed to many industries and universities. To draw a solid conclusion about the reliability of the SRC, information related to the power converter, such as application, voltage/power level, devices used and so on were required. Moreover, questions related to the source authenticity, such as years of experience, affiliation, etc, were also required, in order to ensure the validity of the collected data. (The questions are described in the appendix A).

The headquarter of companies involved on the survey are located in different countries, such as: USA, Canada, Italy, Sweden, Germany, Switzerland, Brazil, China, Tunisia, UK and India. On the other hand, some of them export their product worldwide, e.g. the Huawei Technologies Co., Fulham Inc., Valeo, Powerbox Benelux BV and etc. It means that most of the data obtained from these companies are not related to an unique sample of power converter, but their great experience from several samples. It is an additional advantage for the accuracy of this survey.

Even more importantly, the survey involves companies from different market segments, with large experience and with mature product on market. It reinforces the accuracy of the obtained data. Indeed, 72% of the answers comes from industries with more than 10 years on market. Information related to the experience of the participant of the survey are summarized in Fig. A.2. With respect to the application of the products involved on the survey, they are also summarized in Table A.1 and in Fig. A.2. The survey covers different application products that are characterized in three different power levels: low power (<500 W), medium power (500 W to 5 kW) and high power (>5 kW).

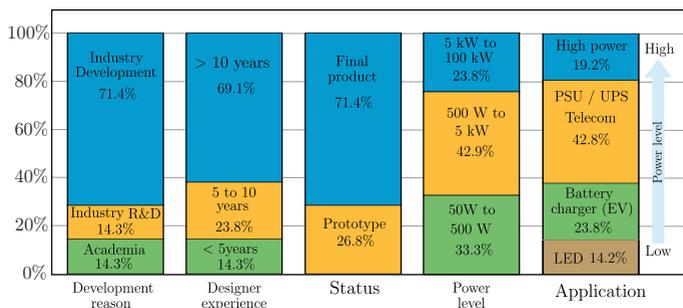
**Tab. A.1:** DC-DC Converter application according to the power level

Companies	Countries
Low power (<500 W)	light emitter diodes (LED)
	Battery Charger
	PSU (auxiliary)
Medium power (500 W to 5 kW)	UPS
	Battery Charger (Automotive)
	Power Supply for Space application
	PSU for motor driver
High power (>5 kW)	Datacenter/Telecom
	Datacenter/Telecom
	Distribution system (microgrid)
	Renewable energy interface
	Welding power supply

## A.0.2 Results

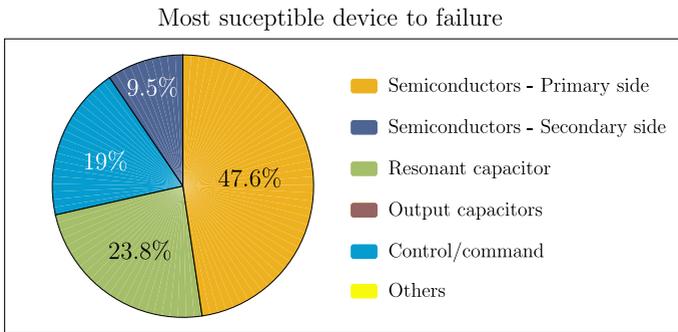
The results of the survey are summarized in Fig. A.3 and Fig. A.4. Fig. A.3 shows the most failure device of the converter. Regardless the application and power level, the primary side semiconductor is listed as the major failure source of the converter, followed by the resonant capacitor. These two devices together are responsible for 72% of the total failure faced on industry for this kind of converter. The fault on the semiconductor of the primary side alone is responsible for almost half of the damage of the converter, and it results mostly in short-circuit of the device, according to the participants. The resonant capacitor, on the other hand, opens the circuit during the fault, avoiding the power to be delivered to the secondary side. The last failure is, at least, not catastrophic, since the circuit is opened, avoiding further damage. Failures on control and command (e.g. gate driver) platform comes in third place followed by failures on semiconductor of the secondary side.

The occurrence of the failure on the SRC converter is presented in Fig. A.4 (a). Note that the converter faults occurs occasionally in 60% of the cases. Only 15% of the products covered in this survey presents failure frequently. In this group of converters, all failure reported are related to the semiconductor on the primary side. Additionally, these converter applied for high power (i.e. 5kW) and they employ IGBT devices on the primary side. The Fig. A.4 (b) shows the type of semiconductor used on the primary side of the converter covered in this survey. Note that most of the products use the Super-Junction MOSFETs (SJ-MOSFETs), because of its high performance with low price.

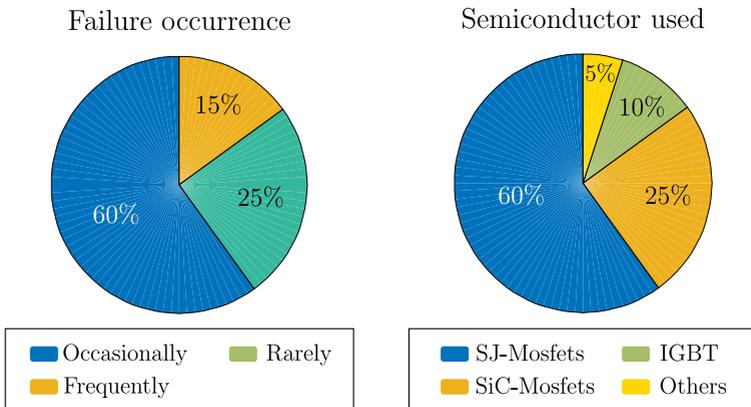


**Fig. A.2:** information related to the participants of the survey (companies and universities) and status, specification and application of the converter.

Moreover, most application uses input voltage up to 900 V, enabling the use of such semiconductor. Note that SiC-MOSFETs have been used 25% of the cases, illustrating a significant increasing of the application of such technology. Note that the SiC-MOSFET has generally better electric characteristics than the SJ-MOSFETs. On the other hand, its higher price is the limiting for using this technology. As the cost is a crucial aspect in industry, most of the companies choose for using SJ-MOSFET instead.



**Fig. A.3:** Result from the survey: most vulnerable device to failure of the SRC/LLC converter.



**Fig. A.4:** Result from the survey: (a) occurrence of the failure and (b) technology of the semiconductors used on the primary side of the converter.

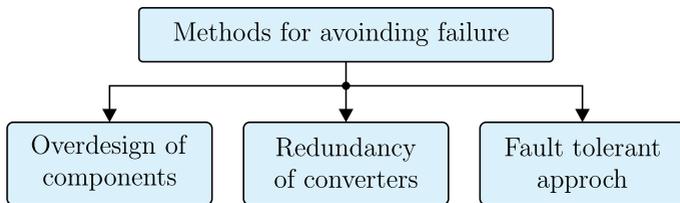
## A.1 Improving the Converter's Availability: Solutions

From the previous analysis, the semiconductors of the primary side and the resonant capacitor have been recognized as the most vulnerable devices to fail.

Most of the events that cause the semiconductors failure are related to the malfunction of the auxiliary circuit (e.g. gate driver, auxiliary power supply, forced cooling system, control system, etc) or unexpected behavior of the load. Those events lead to three main failure cause on the semiconductors: overcurrent (short-circuit current), overvoltage or overtemperature. In fact, bug on the auxiliary circuit or unexpected load behavior are classified as the primary root of failure and they lead to the real failure mechanisms. Fig. A.5 shows the fundamental failure mechanisms and the predominant primary events that leads to such causes. As a matter of facts, the semiconductors might assume two possible states, depending on the failure mechanisms: open-circuit (OC) or short-circuit (SC) [117]. For voltage source converter, which is the case of the SRC/LLC, the OC fault is not catastrophic, since the power transfer will be naturally interrupted. Yet, in some applications, power flow interruption is not tolerable. Instead, the SC fault is the main issue, because it can cause destructive damage to the power converter.

Primary cause	Failure mechanism	Failure mode	Device
Reduced load impedance Converter control error Faulty driver pulses for the switches Human errors (wrong connection, etc.)	Overcurrent Short-circuit current		
Supply voltage error in the driver stage Emitter/source di/dt feedback Overvoltage on the gate Parasitic oscillations in the gate circuit	Overvoltage	Short-circuit	Semiconductor
Supply voltage error in the driver stage Emitter/source di/dt feedback Overvoltage on the gate Parasitic oscillations in the gate circuit	Overtemperature		
Reduced load impedance Converter control error Faulty driver pulses for the switches Human errors (wrong connection, etc.)	Overcurrent Short-circuit current	Open-circuit	Resonant cap
Start-up of the converter Short circuit on the load	Overvoltage		

**Fig. A.5:** Failure mode effect analysis of the SRC/LLC converter.



**Fig. A.6:** Most adopted solution in industry for avoiding failure on the converter.

Even more importantly, the SC failure is not only the most destructive type that should be avoided, but also the most likely to happen in the real application and then it deserves more attention. This can be observed in Fig. A.5, in which the failure mode are related to the failure mechanism and primary cause for each device.

With respect to the capacitor failure, the major primary causes are related to the start-up of the converter and load behavior. Indeed, the start-up leads to overvoltage on the capacitor if soft start-up is not used. Furthermore, suddenly variation on load impedance entails not only to overcurrent on the capacitor, but also over voltage. Normally, most of the failures results in an OC condition [123] and the relation between the primary cause, failure mechanism and failure mode are also shown in Fig. A.5.

Avoiding the failure on those devices might enlarge considerably on the converter's availability. Thus, the most adopted solution in industry and academia for such purpose are presented in Fig. A.6 and discussed next.

### A.1.1 Oversize components

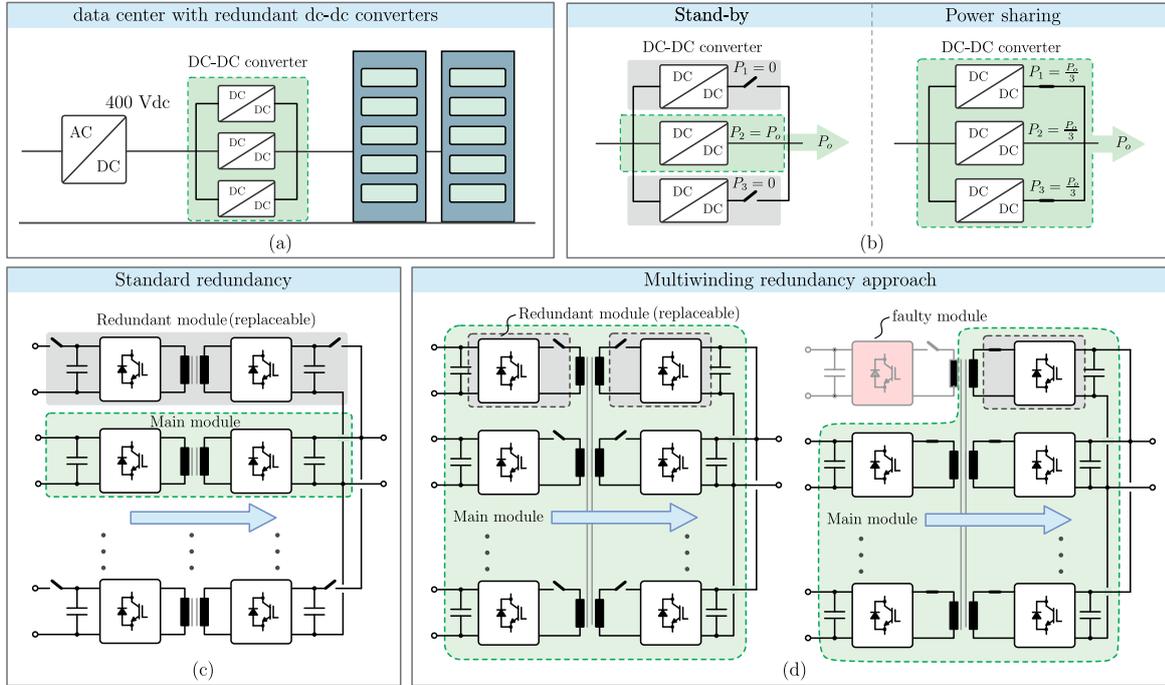
To most simple solution is oversize the most critical components. This is usually adopt in industry, mainly when the failure cause in unknown, though penalizing the cost. In case of LLC or SRC converter, this approach is very suitable for the resonant capacitor. The component regularly fails because overstress of voltage or current, due to the unexpected operation, like overload, short-circuit or start-up. As a results, the damaged capacitor behaves as an open the circuit, interrupting the power flow. Therefore, oversize the capacitor is a simple and relatively cheap solution. Contrarily, oversize the semiconductors is not recom-

mended and very rarely adopted. Indeed, oversize the semiconductors in voltage penalizes greatly the cost and efficiency of the converter, because the price and on resistance or drop voltage during the on-state of the semiconductors is directly related to the voltage rating of the device. Thus, higher voltage rated device means higher cost and higher losses. Oversize the semiconductors in current might not solve the problem, in most case, and then it is not adopted.

### A.1.2 Redundancy

The most adopted solution for increasing the availability of the converter is to use redundant converters. Redundancy has been employed in many applications in which power interruption is not acceptable, such as data center and distribution system (e.g. smart transformer [53]). In this approach, the dc-dc converter is conceived by connecting multiple modules as exemplified in Fig. A.7 (a) for data center application. Once a module fails, the remaining ones are in charge to provide the required power, maintaining the continuity of power flow. There are two kind of redundancy: the stand-by and power sharing, as shown in Fig. A.7 (b). In the stand-by redundancy, the extra converter (or converters) remains inactive in normal operation and it is activated in case of damaging on the main converter. Contrarily, in the power sharing redundancy, all modules operate simultaneously sharing the power among them and when one of them fails, the remaining ones assume the total power. Regardless of the type, the redundancy approach implies in extra cost, because more converters are needed. Thus, it is considered a very expensive solution.

Traditionally, the redundancy approach uses an extra dc-dc converter as a replaceable part of the entire system, as depicted in Fig. A.7 (c). Alternatively, a redundancy approach using a cell of the converter as the replaceable part of the entire system has been reported in [89]. In this case, the dc-dc converter is based on a multiwinding transformer, instead the traditional LLC or SRC, and several cells are coupled to the same high frequency transformer (HFT) as depicted in Fig. A.7 (d). In this approach, all cells of the converter operate simultaneously in normal condition, sharing the power among them. In fault case, only the faulty cell is isolated from the entire system, as exemplified in Fig. A.7 (d).



**Fig. A.7:** Redundancy approach of converter: (a) example of application of redundancy in datacenter application, (b) types of redundancy operation (stand-by or power sharing), (c) standard redundancy scheme of dc-dc converters, (d) alternative redundancy scheme using multiwinding transformer presented in [89].

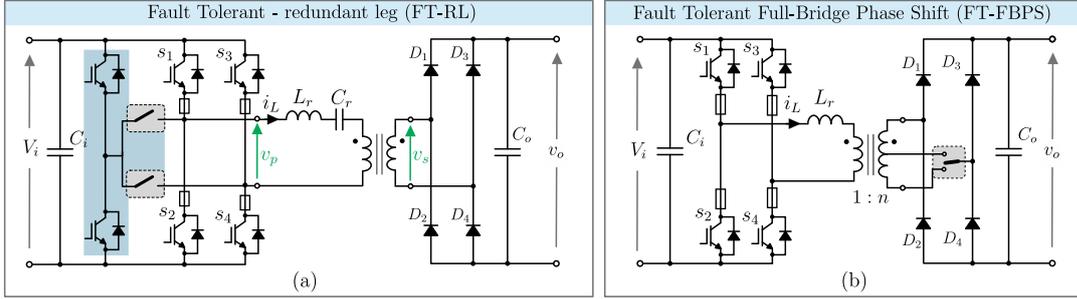
Unlike the traditional redundancy scheme where the faulty converter (composed by two cells and one HFT) is replaced, in the method described in Fig. A.7 (d), only a single cell is replaced. This reduces the maintenance cost.

### A.1.3 Fault Tolerant Approach

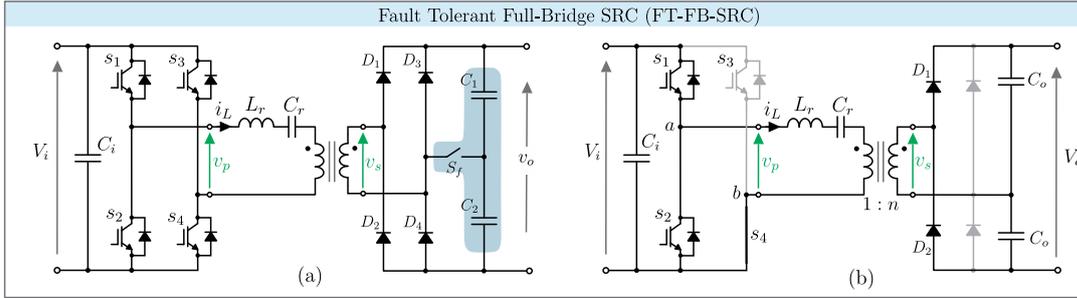
The fault tolerant feature contributes to increase the availability of system and it is a cost-effective solution for such purpose. Several fault tolerance methods have been proposed in literature and most of them include a significant amount of extra hardware, such as semiconductors/leg redundancy [114, 125] or series connection of fuses/switches to isolate the fault [125–127]. Yet, this method is still more cost-effectively than the redundancy approach.

From the existing fault tolerant methods presented in the literature, the use of a redundant leg is the most popular one. It is shown in Fig. A.8 (a) [125]. In this solution, an extra leg is used to replace the damaged leg in case of fault. To isolate the faulty leg, fuses must be connected in series with the semiconductors, opening the circuit for the short-circuit case. Consequently, this solution requires many additional components, increasing considerably the cost. Yet, the fuses used in series with the main devices dissipate power, deteriorating the converter's efficiency. Another fault-tolerance approach was proposed in [127] for the full-bridge phase-shift DC-DC converter, in which it is reconfigured in an asymmetrical half-bridge converter. The proposed topology is illustrated in Fig. A.8 (b), and it is valid only for OC failure. Moreover, this technique also requires fuses in series with the main devices, deteriorating the converter's efficiency. Thus, this method has limited application.

A promising fault tolerant solution with minimum of additional hardware and no impact on converter's efficiency has been proposed in [113]. The modified topology of the SRC with fault tolerance capability, named as Fault Tolerant Full-Bridge SRC (FT-FB-SRC) is shown in Fig. A.9 (a). This topology is resilient to OC or SC, making it a suitable solution for every kind of semiconductor fault of the primary side. The basic idea of this topology is to keep operating the converter after the fault, (i.e. SC or OC of a semiconductor), but as a half-bridge SRC (HB-SRC), instead the full-bridge (FB-SRC), isolating the faulty leg.



**Fig. A.8:** Existing fault tolerant approaches: (a) redundant leg [125], (b) fault tolerant FBPS proposed in [127].



**Fig. A.9:** (a) Fault-Tolerant Full-Bridge SRC proposed in [113] and (b) its operation under fault.

**Tab. A.2:** Evaluation of different fault tolerant approaches

Extra devices	FT-RL	FT-FBPS 2	FT-FB-SRC
Semiconductors	6	4	2
Fuses	6	4	0
Capacitors	0	0	1
Others	-	central tap trafo	-
Applied converters	FB / SRC / LLC	FB	SRC/LLC
Failure type	OC / SC	OC	OC / SC
Efficiency impact	yes	yes	no

In fact, damaged device is used as a circuit path, and the FB-SRC became a HB-SRC, as illustrated in Fig. A.9 (b). After the reconfiguration, the output voltage ( $V_o$ ) drops to half of its value and for this reasons a reconfigurable rectifier is required to keep the output voltage constant, according to [113]. Compared to the previous fault tolerant solution, this one uses only one extra device and no additional fuse.

The Table A.2 shows the comparison of the described existing methods with the proposed one, in terms of components and efficiency impact. As can be noticed, the FT-FB-SRC provides an efficient and low cost solution.

## A.2 Conclusion

This survey has presented failure analysis of the Series Resonant DC-DC converter (SRC) and LLC converter. In this study, a survey involving companies and academia was carried out with the aim to recognize the most vulnerable devices of the converter to failure.

The result from the survey shows that the primary side semiconductors are the most susceptible device of the SRC, and they are responsible for almost half of the failure. The resonant capacitor is listed as the second most susceptible device to failure, causing almost 25% of the converter's failure. These data are valid for different power level application and semiconductors technology used on the primary side. Most companies reported that the failures on the resonant capacitors occurs

normally during the start-up or overload. Both conditions result in overvoltage on the capacitor and subsequently its failure. Oversize the resonant capacitor is normally adopted in industry, but unpredictable behavior of the load still leads to this problem.

The major failure cause, i.e. semiconductors failure, can be overcome using a fault tolerant approach. By doing so, the converter might be resilient to semiconductors failure, remaining in operation. Among the possible methodology, the FT-FB-SRC topology presented in this paper is the most suitable one for such purpose.

# Nomenclature

## Abbreviations

3L	Three Level
3L-SRC	Three Level Series Resonant Converter
AC	Alternating Current
APS	Auxiliary power supply
Asym-HB-SRC	Asymmetric Half Bridge Series Resonant Converter
AVG	Average
CCM	Continuous Conduction Mode
CCU	Communication and local Control Unit
CHB	Cascaded H-bridge
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DG	Distributed Generator
DSCC	Double-Star Chopper-Cell
EV	Electric Vehicle
FB-PWM	Full Bridge converter with Pulse-Width Modulation
FBR	Full Bridge Rectifier
FB-SRC	Full Bridge Series Resonant Converter
FT-SRC	Fault Tolerant Series Resonant Converter
FT-FB-SRC	Fault Tolerant Full Bridge Series Resonant Converter
FC	Flying Capacitor
FC-SRC	Flying Capacitor Series Resonant Converter
FMEA	Failure Mode and Effect Analysis
GaN	Gallium Nitride
GDU	Gate Driver Unit
HB-SRC	Half Bridge Series Resonant Converter
HF	High Frequency
HFT	High Frequency Transformer

## Nomenclature

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HV	High Voltage
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
ISOP	Input-Series Output-Parallel
LFT	Low Frequency Transformer
LV	Low Voltage
MAB	Multiple Active Bridge
MF	Medium Frequency
MIT	Massachusetts Institute of Technology
MMC	Modular Multilevel Converter
MMCC	Modular Multilevel Cascaded Converter
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MPPF	Metalized Polypropylene Film
MV	Medium Voltage
NPC	Neutral Point Clamped
NPC-SRC	Neutral Point Clamped Series Resonant Converter
OC	Open Circuit
OLTC	On-Load Tap Changer
PI	Proportional-Integral
PR	Power Routing
PRA	Power Routing Approach
PSFB	Phase-Shift Full-Bridge
PSFB-ZVS	Phase-Shift Full-Bridge with Zero Voltage Switching
PSM	Phase Shift Modulation
PV	Photovoltaic
PWM	Pulse-Width Modulation
QAB	Quadruple Active Bridge
RMS	Root-Mean-Square
RES	Renewable Energy Sources
SC	Short Circuit
Si	Silicon
Sym-HB-SRC	Symmetric Half Bridge Series Resonant Converter
SiC	Silicon Carbide
SRC	Series Resonant Converter
SSBC	Single-Star Bridge-Cell
SST	Solid State Transformer
ST	Smart Transformer
STATCOM	Static compensator
TCM	Triangular Current Modulation

TPM	Trapezoidal Modulation
TT	Terra-Terra
VDR	Voltage Doubler Rectifier
VSI	Voltage Source Inverter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching



# List of Publications

Different parts of the research findings presented in this dissertation and of other research projects carried out in parallel have been published in international scientific journals, conference proceedings and workshops. The publications published by the author of this thesis developed during the course of the PhD are.

## Journal Papers

1. **L.F. Costa**, G. Buticchi, and M. Liserre, Optimum Design of a Multiple-Active-Bridge DC-DC Converter for Smart Transformer. *IEEE Transactions on Power Electronics*, 2018 (Early Access).
2. **L.F. Costa**, G. Buticchi, and M. Liserre, Comparative Analysis of Multiple Active Bridge Converters Configurations in Modular Smart Transformer. *IEEE Transactions on Industrial Electronics*, 2018 (Early Access).
3. **L.F. Costa**, G. Buticchi, and M. Liserre, A Family of Series-Resonant DC-DC Converter With Fault-Tolerance Capability. *IEEE Transactions on Industry Applications*, 2018.
4. G. Buticchi, D. Barater, **L.F. Costa**, M. Liserre, A PV-Inspired Low-common mode Dual Active Bridge Converter for Aerospace Applications. *IEEE Transactions on Power Electronics*, 2018 (Early Access).
5. G. Buticchi, **L.F. Costa**, D. Barater, M. Liserre and Eugenio Dominguez, A Quadruple Active Bridge Converter for the Storage Integration on the More Electric Aircraft. *IEEE Transactions on Power Electronics*, 2018 (Early Access).

6. **L.F. Costa**, G. Carne, G. Buticchi, and M. Liserre, The Smart Transformer: A Solid-State Transformer Tailored to Provide Ancillary Services to the Distribution Grid. IEEE Power Electronics Magazine, Summer 2017.
7. **L.F. Costa**, G. Buticchi, and M. Liserre, Highly Efficient and Reliable SiC-Based DC–DC Converter for Smart Transformer. IEEE Transactions on Industrial Electronics, 2017.
8. **L.F. Costa**, G. Buticchi, and M. Liserre, A Fault-Tolerant Series-Resonant DC-DC Converter. IEEE Transactions on Power Electronics, Feb 2017.
9. **L.F. Costa**, G. Buticchi, and M. Liserre, Quad-Active-Bridge DC-DC Converter as Cross-Link for Medium-Voltage Modular Inverters, IEEE Transactions on Industry Applications, Feb 2017.
10. G. Buticchi, **L.F. Costa**, and M. Liserre, Improving System Efficiency for the More Electric Aircraft: A Look at DC-DC Converters for the Avionic On-board DC Microgrid. IEEE Industrial Electronics Magazine, Spring 2017.
11. M. Liserre, M. Andresen, **L.F. Costa**, and G. Buticchi, Power Routing in Modular Smart Transformers: Active thermal control through uneven loading of cells. IEEE Industrial Electronics Magazine, Spring 2016.
12. M. Liserre, G. Buticchi, M. Andresen, G. D. Carne, **L.F. Costa**, and Z. X. Zou, The Smart Transformer: Impact on the electric grid and technology challenges. IEEE Industrial Electronics Magazine, Summer 2016.

## Conference Papers

1. L. F. Costa, G. Buticchi and M. Liserre, "Efficiency/Cost Trade-off Design of a Multiple-Active-Bridge Converter for Smart Transformer," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018.
2. G. Buticchi, L. F. Costa, D. Barater and M. Liserre, "A Quadruple Active Bridge Converter as a Storage Interface in the More Electric Aircraft" 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018.

3. Y.J. Ko, A. Chub, L. F. Costa, M. Andressen and M. Liserre, "Smart Transformer Universal Operation" 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018.
4. L. F. Costa, G. Buticchi and M. Liserre, "Highly efficient and reliable DC-DC converter for smart transformer," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 184-190.
5. L. F. Costa, G. Buticchi and M. Liserre, "A family of series-resonant DC-DC converter with fault-tolerant capability," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 3378-3384.
6. L. F. Costa, F. Hoffmann, G. Buticchi and M. Liserre, "Comparative analysis of MAB dc-dc converters configurations in modular smart transformer," 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Florianopolis, 2017, pp. 1-8. (**Best student paper award**)
7. L. F. Costa, G. Buticchi and M. Liserre, "Modular Smart Transformer architectures: An overview and proposal of a interphase architecture," 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Florianopolis, 2017, pp. 1-7.
8. G. Buticchi, L. Costa and M. Liserre, "DC/DC conversion solutions to enable smart-grid behavior in the aircraft electrical power distribution system," IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, 2017, pp. 4369-4374.
9. A. Chub, L. Costa and M. Liserre, "Analysis and design of asymmetric quad-active-bridge converter," IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, 2017, pp. 5367-5372.
10. G. Buticchi, L. Costa and M. Liserre, "A quadruple active bridge electrical power distribution system for the more electric aircraft," 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE), Edinburgh, 2017, pp. 1851-1855.

11. G. Buticchi, L. Costa and M. Liserre, "Resilient multi-bus distribution in more electric aircraft by means of dual active bridges," 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE), Edinburgh, 2017, pp. 1874-1878.
12. L. F. Costa, G. Buticchi and M. Liserre, "Quadruple Active Bridge DC-DC converter as the basic cell of a modular Smart Transformer," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 2449-2456. (**Best presentation award**)
13. L. Costa, G. Buticchi and M. Liserre, "Bidirectional series-resonant DC-DC converter with fault-tolerance capability for smart transformer," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-7.
14. M. Andresen, L. F. Costa, G. Buticchi and M. Liserre, "Smart Transformer reliability and efficiency through modularity," 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, 2016, pp. 3241-3248.
15. G. Buticchi, M. Andresen, L. Costa and M. Liserre, "Modular DC/DC converter structure with multiple power flow paths for smart transformer applications," 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, 2015, pp. 1-9.
16. L. F. Costa, G. Buticchi and M. Liserre, "Comparison of basic power cells for quad-active-bridge DC-DC converter in smart transformer," 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, 2015, pp. 1-10.
17. L. F. Costa, G. Buticchi and M. Liserre, "Quad-active-bridge as cross-link for medium voltage modular inverters," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 645-652.

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# Curriculum Vitae

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## Education

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## Work Experience

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