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Digital Object Identifier (DOI): 10.1109/MIE.2016.2588898

IEEE Industrial Electronics Magazine (Volume:10, Issue:3) Fall 2016 **Power Routing in Modular Smart Transformers: Active Thermal Control Through Uneven Loading of Cells**

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Suggested Citation

M. Liserre, M. Andresen, L. Costa and G. Buticchi, "Power Routing in Modular Smart Transformers: Active Thermal Control Through Uneven Loading of Cells," in IEEE Industrial Electronics Magazine, vol. 10, no. 3, pp. 43-53, Fall 2016.

Power Routing in Modular Smart Transformers: Active Thermal Control Through Uneven Loading of Cells

I. INTRODUCTION

The increase of decentralized energy production challenges the actual distribution grid [1], [2]. In many countries, the generation and the consumption are spatially separated and the energy needs to be transferred over a long distance [3]. This calls for new concepts to transfer the power to the loads without overloading grid feeders and to connect new intelligent loads and storage [4], which are typically making the actual electric grid hybrid (ac and dc) and coupled with other energy networks (multimodal) [5]. In the current configuration, the transformers are passive devices, which do not enable connecting dc systems or interfacing the electric grid with other energy grids. A solution, which provides hybrid and multimodal connectivity and possible control of the power flow, is the Solid State Transformer (SST), which is based on power electronic converters and a medium frequency transformer for galvanic isolation [6]. Unfortunately, the SST has not achieved market breakthrough even in traction and ships, where it offers reduced space requirements and higher efficiency compared to the low frequency transformer [7].

On the contrary, the application of the SST in the distribution system would be justified and its higher cost paid by functionality so that it is more suited to define it Smart Transformer (ST) to highlight these dominant "software" aspects while the main "hardware" requirement is to allow a connection points of hybrid distribution networks among dc and dc distribution. As a consequence, an ST is an SST with available dc-link connectivity (so minimum two-stages) and significant flexibility in managing its ac and dc connection points, which calls for advanced identification and control algorithms [8].

However, this ST has to compete with the traditional transformer not only in the field of functionality, but also in the field of efficiency and reliability. In the field of reliability, the traditional transformer is hard to outperform, because its lifetime is in the range of several decades with low maintenance effort, a target hardly achievable with today's power semiconductor technology. Also the efficiency of the traditional transformer is expected to be higher than that of an SST, especially, in a three-stages architecture [9]. The target of achieving high efficiency while preserving dc connectivity is addressed with a modular design of the ST by using power semiconductors rated for lower voltage and current [8].

In the current design of modular power converter architectures, the power electronic cells forming the converter are usually equally loaded. Activating/deactivating can be applied to increase the efficiency of the system [10], but may lead to higher stress because of the activation and deactivation process [8]. A software-based opportunity to reduce the stress of power converters has been proposed by industry: active thermal control. It has been applied to regulate thermal cycling during high torque and low speed of drives to prevent a failure of the system [11].

Modular architectures can handle cell failures, especially if redundancy is present [12]. However, a series device for the electric grid, like the ST, which can process the full power going to the consumers shall be designed to to have the highest possible availability. HVDC for example requires an availability of 99 % [13]. As a consequence, avoiding failures is one of the main targets of such systems.

Previous studies based on field data about failures in wind and photovoltaic systems did show that the power modules and the capacitors are the components most prone to fail [14]. Different components are subjected to different failure mechanisms that in some cases depend on the processed power and in other do not [15]. It is reasonable that once one cell of a modular architecture fails, independently from which component did fail, the cell is sent to maintenance and replaced. The same cell is repaired and becomes again available on the stock of replacement units (Fig. 1). This means that a modular converter is by nature a system made by differently aged cells.

This work introduces the concept of power routing in modular STs to implement active thermal control through an uneven loading of the cells of the modular architecture. The aim is to avoid or delay as much as possible the failures dependent on the processed power of the cell, shifting the load from the cells, whose components are older, as shown in the Fig. 1.

The article presents the power routing concept and discusses with experimental test results made on three different prototypes (including a 98.35 % peak efficiency SiC-based dc/dc converter) how the power routing can influence the efficiency, since this is typically the most known

Fig. 1: Concept of a repairable system in operation: Commissioning with new cells and different wear out due to different aging, replacement and repair of the cells. The resultant different aging condition of each cell in the system are indicated with gray color.

drawback of active thermal control [16]. At the end, a study case shows how the proposed approach can work in a real system and which could be the actual benefits in terms of minor consumed lifetime of the mostly aged cells.

II. FROM SST TO ST

The concept of a Solid State Transformer (SST) was first introduced in 1968 by McMurray, who proposed a device based on solid-state switches with high-frequency (HF) isolation, which behaved like a traditional transformer. Since then, the SST concept has been refined by new opportunities, offered by new technologies and application requirements. Considering different possible application fields, the SST has high potential to be used in electric distribution, as the enabling technology for smart grid functionality. In this application field, the SST is supposed to replace the standard low frequency transformer (LFT), connecting the medium-voltage (MV) grid to the low-voltage (LV) grid, enabling DC connectivity and offering services to both LV and MV grids. The services requirement, together with the need for control and communication functions make this device a smart SST, leading to a new concept: the Smart Transformer (ST).

Mainly due to the power electronics and semiconductors technology evolution, new ST implementation possibilities have been proposed and classified in literature. Fig. 2 presents an overview

Fig. 2: The classification of the SST architecture according to the number of power conversions and modularity.

of the possible architectures, where the three-stage configuration enables dc-link connectivity and also guarantees input/output decoupling of voltages/currents, providing more degrees of freedom to the system control. Hence, it is the preferred candidate for an ST [8].

The next choice in terms of architecture is the degree of modularity. Modular architectures consist of several cells rated for low voltage or low current, which are used as building blocks for the entire system.

In contrast to this, a non-modular system is based on a single power converter, usually taking advantage of high-voltage wide-bandgap semiconductors [17], [18]. To handle the MV level involved in the power converter, special devices with high voltage capability, such as 10kV SiC Mosfet [18] or 15 kV SiC Mosfet [17], need to be employed. Since these devices are still not available on the market (only for the research purpose), there is no available product using this technology. A standard approach to handle the MV in a non-modular solution, which is used in industrial applications, is to use series connection of semiconductors. However, it demands additional control effort to balance the voltage among the semiconductors.

The non-modular architectures have the advantage of using a small number of semiconductors, drivers, and sensors, as well as a single transformer, leading to a lower number of possibly faulty components. On the other hand, modular architectures bring several advantages to power and voltage scalability, maintenance and the implementation of fault-tolerance strategies [19]. In comparison to the non-modular architecture, the modular one has reduced EMI emission (due to the low dv/dt and di/dt) and the possibility to use standard low voltage rating devices, which present good performance, leading to a highly efficient system [20], [21].

Fig. 3: Three-stage modular architecture of the ST and possible power converters used to implement each of them.

The semi-modular architecture is another concept to consider, where the basic cell is more complex than the modular case. An example of a semi-modular architecture is a structure using multiple active bridges connected to a multi-winding transformer. This kind of architecture has the same advantages of a full modular configuration but requires a lower number of transformers.

Fig. 3 shows the three-stages ST implementation, providing an overview of possible modular topologies that can be used and the possible basic cells for the DC/DC stage.

III. CELLS LOADING IN A MODULAR SYSTEM: IMPACT ON EFFICIENCY AND LIFETIME

The system efficiency is the biggest concern in the design of modular architectures and this parameter is dependent on the single converter efficiency. For the maximization of the efficiency of the single cell, many design optimization methods have been discussed in literature, which consider the semiconductors technology, the modulation or reactive elements as the main input parameters [22]. In a system level view, on the other hand, one more aspect can be used to optimize the overall efficiency of the system: the operation point of the individual cell with respect to the system behavior.

Fig. 4 shows a typical efficiency curve of a system composed of three parallel connected cells ($N = 3$), the efficiency curve of the single cell ($N = 1$) and when two cells ($N = 2$) are operating. As it can be observed in this figure, the efficiency of a single cell in light load is much higher when a single converter is operating instead of all three converters. This shows that, depending on the operation point, deactivating converters can bring benefits to the overall system efficiency. This operation method based on activation or deactivation of cells was introduced in [10], as a solution to improve the system efficiency in light load. Currently, this concept is known as phase-shedding technique and it is commonly used in systems based on interleaved converter (either dc-dc or dc-ac/dc-ac). In the following, to do not create confusion, with the use of "Phase" for multi-phase ac systems "Phase shedding"' is indicated as activation/deactivation method.

Although the concept of unloading cells can bring advantages to the system in terms of efficiency, it might have negative impact on other parameters of the converter or the system. As an example, in a system based on activation/deactivation method operating in light load, a single cell will be active and therefore the output current ripple will be higher (when compared to three operating cells), introducing higher stress in the output capacitors. This example already shows that the process of activating/deactivating cells puts efficiency and power quality coherent stress

Fig. 4: Example of efficiency improvement in light load, when the phase-shedding concept is used.

in contrast. Besides that, the system can operate in a non-optimum efficiency point, if another parameter (e.g. temperature or lifetime) needs to be optimized.

The differences among the proposed approaches are reported in Tab. I.

TABLE I: Comparison of strategies to control the power in modular systems.

In the reliability assessment, it is mandatory to use a physics of failure approach, which takes into account the real operating conditions and the loading of the devices, referred to as mission profile [8]. Applying physics of failure to the power electronics converter led to the finding that power semiconductors and capacitors are among the most fragile components [23]. For these components, the relevant failure mechanisms are known. In power electronic modules, which are commonly used to increase the power density, thermal cycling is affecting the failures [24]. The failure mechanism is caused by cooling down and heating up, which is causing mechanical stress between layers with different coefficients of thermal expansion. For instance, the lifetime of the power semiconductors is given by the manufacturer in the number of cycles with a certain magnitude as shown in Fig. 5 (a). For this reason, the reliability is investigated in terms of thermal stress on the components for different load variations. The lifetime is related to the number of thermal cycles to failure (N_f) with exponential influence of the magnitude ΔT and the average junction temperature during the cycle $(T_{i,mean})$. In particular, the average junction temperature represents the classical approach of thermally activated creep, modeled with the Arrhenius equation based on an activation energy [25]

It needs to be pointed out, that in real applications, the thermal cycles are distributed with different magnitudes and different average junction temperatures, which do not make these power cycling curves directly applicable. In order to overcome this problem, the damage is usually linearly accumulated as expressed with the Palmgreen Miner rule [16].

Based on this knowledge, it is possible to analyze the effect of a thermal design on the lifetime of the system. In general, the design for a high maximum junction temperature is limiting the lifetime, while a design for a very low junction temperature might change the dominant failure

Fig. 5: (a) Relation between thermal swing and cycles to failure [26], (b) effect of unbalanced loading on the power cycling capability of the system, (c) simplified relation between power imbalance and lifetime.

(b)

(a)

mechanism or even let another component fail before. The system design for a maximum junction temperature $\Delta T = 60$ K is shown in Fig. 5 (b) and corresponds to the design for a maximum junction temperature of $T_{j,max} = 90 °C$ under the assumption of an ambient temperature of $T_a = 30 °C$. The design for a lower junction temperature decreases the maximum thermal swing and the average junction temperature during this swing. In order to extend the analysis for modular systems with redundant power paths, a similar design of the modular cells is assumed. Assuming that the losses are mostly related to the processed power, the effect of asymmetrical loading on the lifetime of the system is investigated using the accumulated damage approach, by means of the Palmgreen Miner rule [16]. A reduction of the power in the cell results in lower thermal cycles and thus the detected thermal cycles c_i are shifted in lower stress ranges. An increase in the power instead shifts the cycles c_i to higher stress ranges. This effect is illustrated in Fig. 5 (c). Here, the effect of loading two parallel converters with equal and unequal power is shown. For the equal loading of the converters, both undergo the same thermal swing as it was shown in Fig. 5 (b) and result in similar lifetime consumption. It is demonstrated, that an unbalanced loading with 30% : 70% leads to a significant increase of the lifetime of the lightly loaded cell and a decrease of the highly loaded one. Consequently, this example shows that it is possible to influence the lifetime of the modular system by controlling the power processed

 (c)

by the individual cells. It is important to note that the lifetime also depends on many others components (e.g. capacitors) and their related failure mechanisms. Since the aim of this example is to demonstrate the influence of unequal power sharing of the modules on the system's lifetime, the others failures and their mechanisms are not investigated.

IV. POWER ROUTING

As pointed out in the previous section, activating/deactivating cells in a modular structure is beneficial for efficiency, but detrimental to the reliability of the system. Instead of activating/deactivating cells, routing the power while having all of them active as differentiated in Fig. 6, offers more freedom in the optimization of the conflicting goals to maximize the efficiency and lifetime.

Fig. 7 shows a modular system based on three cells, where p_1 , p_2 and p_3 are the power processed by the cells 1, 2 and 3 respectively. The total power is given by $p_T = p_1 + p_2 + p_3$. In a standard operation scheme, the cells process the same amount of power and therefore $p_1 = p_2 = p_3$. Power routing is the optimization technique where each cell processes a specified amount of power with the aim of improving the system's efficiency and reliability. The result can be $p_1 \neq p_2 \neq p_3$.

The cells can be connected in series, parallel or even a mix of both. In the series connection, the cells share the same current i_T , as illustrated in Fig. 7 (b), but each cell has the degree of freedom to control its output voltage, defined by v_1 , v_2 and v_3 . Since the power of a generic cell k is given by $p_k = v_k i_T$ (where $k = \{1, 2, 3\}$), the power of the individual cell can be controlled by changing the output voltage of the cell. Likewise, in the parallel configuration, the cells share the same voltage v_T , as illustrated in Fig. 7 (c), but each cell has the degree of

Fig. 6: Power routing concepts: (a) activation/deactivation of cells, (b) all cells active with unbalance power transfer.

Fig. 7: Power routing concept and possibilities to implement a modular system: (a) power routing concept in a modular system. (b) Series connection of cells, where the cell voltage is used to control the power (c) parallel connection of the cells, where the current is used to control the power and (d) combintation of parallel and series connected cells.

freedom to control its output current, defined by i_1 , i_2 and i_3 . In that case, the parameter used to control the power of the cells is the current instead of the voltage.

Finally, both previously described connections can be combined in a series/parallel configuration, as depicted in Fig. 7 (d), where the cells share the total voltage and the current of the system. In that configuration, they have the degree of freedom to control the power through the current or the voltage control.

Comparing the configurations, in the series approach, the semiconductors may need to be overrated in term of blocking voltage capability, because one cell will have higher output voltage, and consequently higher dc voltage may be needed. The overrating of the semiconductors blocking voltage leads to a negative impact on the cost and efficiency of the converter, since the semiconductor's price and conduction losses are related to the voltage rating of the device.

As an example, a system based on three cells connected in parallel is shown in Fig 8 (a). In that system, each cell has an expected remaining lifetime defined by λ_1 , λ_2 and λ_3 for the cells 1, 2 and 3, respectively. The remaining lifetime for the cell 1 is lower than the other cells and once the end of life for the cell it is reached, the entire system will fail. Therefore, to extended the expected lifetime of the entire system, it is necessary to increase the lifetime of cell 1. One strategy to increase the lifetime of the power cells is to reduce the operation temperature of the cells, since the temperature and lifetime are directly related [27]. This example is illustrated in Fig. 8 (b), where in the first moment all cells process the same amount of power, resulting in

Fig. 8: Example for the impact of power routing on the lifetime of a modular system: (a) block diagram of a example system highlighting that one cell is close to the end of life, (b) expected lifetime graphic showing the impact of the power routing on the system's lifetime.

similar operation temperature, but the cell 1 has a reduced lifetime. With the power routing, the power processed by the cell 1 (p_1) can be reduced in order to reduce its temperature, as shown in Fig. 8 (b). As a result, the expected lifetime of the cell 1 and, consequently, the lifetime of the entire system is increased. Of course, the power processed by the cells 2 and 3 will increase, as well as the temperature in these cells. Although the expected lifetime of the cell 2 and 3 are slightly reduced, the system lifetime is increased. Thus, this example has shown that it is possible to delay the time to the next failure and therefore improve the availability of the system.

It can be stated that the aim of the power routing is to extend the lifetime of the converter, delaying the maintenance. However, the system should also be protected from random failures, that cannot be predicted by the actual prognostic systems. For this reason, fault tolerant techniques must be implemented [28] and additional hardware should be installed. Different approaches can be pursued, depending on the level at which the redundant components are located (switch, leg, module and system level). It is opinion of the authors that, considering the high level of modularity envisaged for the system, the best approach is to install additional cells (module-level redundancy). In this case, the actual installed power is greater than the rated one, meaning that the power routing can be applied even at full load, when the temperature of the modules and the stress on the semiconductor is higher. Therefore, the redundancy allows at the same time to protect the converter from random failures and to enable the power routing capability at full load.

V. EFFICIENCY IMPACT OF POWER ROUTING

Fig. 9 (b) shows a modular architecture of the ST based on the CHB converter connected to a quadruple-active-bridge (QAB) DC/DC converter. The CHB controls the input power to ensure a high power factor and also provides services, such as reactive power control. Meanwhile, the QAB converter is responsible to ensure the isolation required in this application and to control the LVDC voltage. As it can be observed, the third stage is not considered in Fig. 9 (b), since it is not relevant for the discussion in this section. The behavior of the QAB converter was experimentally evaluated, in order to verify if the uneven loading leads to a reduction of the overall system efficiency. Thus, the system was first evaluated for balanced condition and then for unbalanced power among the cells, with the aim to show the power routing effect on the system efficiency. As a matter of demonstration, the tests were obtained with ac voltage of 230 V, low voltage dc-link of 200 V, and the power level of 1.5 kW. The cooling system is based on natural convection, so that the thermal resistance remained constant regardless the power processed by the modules.

For the CHB, the losses behavior according to the unbalanced power is observed in Fig. 9 (a). Of course, the losses increase for the overloaded cell, while they decrease for the unloaded cell. However, the overall losses remain basically constant, once the variation is only 0.01%, for a unbalanced condition of $\Delta P = 40\%$ (i.e. $P_1 = P_2 = 1.4P$ and $P_3 = 0.2P$). Therefore, the impact of power routing on the CHB converter's efficiency is irrelevant and then it can be used for lifetime optimization without efficiency deterioration. For the QAB converter, the normalized

Fig. 9: Main results of the power routing effect on the ST: (a) impact of the power routing on the losses and efficiency of the CHB converter, (b) basic ST architecture used as an example for the power routing concept application and (c) impact on the QAB converter.

efficiency curve is presented in Fig. 9 (c), for balanced condition and also for unbalanced condition of $P_1 = P_2 = 25\%P$ and $P_3 = 50\%P$. From these results, it can be noticed that the normalized efficiency of the QAB converter is only slightly reduced for high power transfer, while for lower power transfer, the difference in the efficiency is even lower.

As a conclusion, for the structure presented in Fig. 9 (c), the unbalanced power processing approach has not much effect in the overall efficiency of the ST; hence the power routing concept can be applied to maximize reliability without efficiency deterioration. For the maximization of the reliability, a prognostic algorithm must be used, in order to identify the aged cells and consequently reduced the power processed by them, extending their lifetime.

An alternative to the semi-modular architecture is to use a completely modular architecture, in which the QAB converter can be replaced by isolated converters attached to each CHB cell, composing therefore the dc-dc stage. An option already presented in Fig. 3 is to use the seriesresonant converter, that can obtain high efficiency. In order to evaluate the benefits that the seriesresonant converter can bring to the ST in term of efficiency, a dc-dc converter has been optimally designed and its efficiency limit was evaluated. The converter's topology, prototype specification and the picture of the developed prototype are presented in Fig 10. For the semiconductors, Silicon Carbide (SiC) MOSFETs with very low on resistance $(R_{DS(on)})$ have been used. Three converters with parallel connected output ports were tested in the system, as illustrated on the scheme presented in Fig. 3 (b). The efficiency curve obtained experimentally is illustrated in Fig 10 (c). The maximum efficiency is 98.35% at approximately 4kW output power.

Fig. 10: Series-Resonant converter as a basic cell of the ST' dc-dc stage: (a) specification of the developed prototype and the topology, (b) cells configuration, (c) efficiency curve obtained experimentally, highlighting the maximum efficiency of 98.35%, (d) picture of the developed prototype.

For IGBT-based converter, the semiconductors losses show mainly a direct proportionality to the output current and, consequently to the output power of the cell. Hence, the semiconductors losses can be controlled by the cell output power control. Nevertheless, the semiconductors losses on mosfet-based converters are related, but not direct proportional, to the output current of the converter. Since the emerging SiC-Mosfet devices are a promising technology to be used in ST, the relation between their losses and the output current/power is evaluated. Fig. 11 (a) shows the conduction losses of an Si-IGBT and SiC-Mosfet device versus the output current, for the series-resonant converter described before in Fig. 10. As expected, the relation between the Si-IGBT losses and output current is linear (because of its characteristic of constant drop voltage), while the SiC-Mosfet losses are related to the square of the output current (because of its characteristic of constant resistance when conducting). Because of this non-linear relation, the semiconductors losses on the unloaded and overloaded cell differ from each other, when the power routing is used, even if the output power asymmetry of the unloaded/overloaded cell is the same.

To evaluate the impact of the power routing on the SiC-based converter, two dc-dc converters were connected as illustrated in Fig. 10 (b) (but with 2 cell in this case) and they were both simulated and experimentally tested. The used converter is the series-resonant described in the previous section and the picture of the tested set-up is shown in Fig. 11. Simulation results, showing the semiconductors conduction losses, are presented in Fig. 11 (d), while the main waveforms obtained experimentally for balanced and unbalanced condition are shown in Fig. 11 (e). In the beginning of the simulation , both converters share equally the power (operation point: *a*). Then, an unbalanced condition is forced, in which cell 1 is overloaded processing 25% more power (operation point: *b* (for Si-IGBT) and *d* (for SiC)) and cell 2 is unloaded processing 25% less power (operation point: *c* (for Si-IGBT) and *e* (for SiC))). Analyzing these results, it is concluded that for IGBT devices, the additional conduction losses introduced in the cell 1 are equal to the reduced conduction losses of cell 2 ($\Delta P_{cond(cell1)_{(IGBT)}} = \Delta P_{cond(cell2)_{(IGBT)}}$), in which the overall conduction losses of the system are constant. On the other hand, for SiC devices, the conduction losses added to cell 1 are higher than the one saved from the cell 2 $(\Delta P_{cond(cell1)_{(IGBT)}} > \Delta P_{cond(cell2)_{(IGBT)}})$. Consequently, the overall system losses are increased. As a conclusion, the power routing does not affect the system's losses, when Si-IGBT is used in the dc-dc stage. However, for SiC devices, the system's losses are increased when the power routing approach is employed, impacting the overall system's efficiency.

Fig. 11: Power routing effect when IGBT and SiC-Mosfets are used: (a) relation between semiconductors conduction losses and output cell's current when Si-IGBT and SiC device are used and (b) Simulation results showing the effect of power routing on the semiconductors losses. Experimental evaluation: (c) picture of the prototype and main waveforms for balanced (d) and unbalanced (e) condition.

VI. LIFETIME IMPACT OF POWER ROUTING

In order to demonstrate a case for the application of power routing, a study case in the LV stage of the ST is made as shown in Fig. 12. Three converter cells are installed in parallel and a mission profile with high power fluctuation is applied to the converter. Without power routing, the power is split equally among the converter cells. Power routing is applied in the case of different remaining lifetimes in the cells, e.g. a lower remaining lifetime of cell 1. Since power cycling is assumed to be the dominant failure mechanism in this study, it is required to reduce the thermal swing of the power semiconductors. Thus, it is beneficial to operate with constant power in order to reduce the thermal swing, whenever it is possible. The routing capability depends on the number of cells and the mission profile. Here, the constant power is 1/3 of the average output power, corresponding to 60 %. In this case, the unloaded cell 1 needs to reduce its output power as soon as the power is lower than 20 % of the rated power and it needs to increase the power, when the power exceeds 87 % of the rated power. For determining the

Fig. 12: Study case about power routing in the LV stage: Application of power routing for the stress reduction in cell 1 of the system based on a mission profile.

thermal stress, it is required to simulate the junction temperature of the power semiconductors. This is done with the assumption of a converter design for a maximum junction temperature of 90 °C and an ambient temperature of 40 °C. The power variations are assumed to change much slower than the time constants of the cooling path, which enables to neglect the time variance of the thermal impedances. The thermal cycling of the unloaded cell is reduced, while the other two cells suffer from higher thermal stress in comparison to the case without power routing. For a quantification of the effect, rainflow counting is applied and the accumulated damage is derived. As it can be seen, the damage for cell 1 is reduced to one fifth of its prior value, while the stress for cell 2 and 3 is six times bigger. This is due to the exponential relation between damage and temperature variation. The example is intended to show the potential of the method: a small variation of the losses can produce big effects on the stress. The same small variation of the losses causes only minimal variation of the efficiency while the overall losses are only 1 % bigger.

VII. CONCLUSION

Modular smart transformer architectures have several advantages, such as the use of low voltage/current rated devices, fault tolerance capability, low EMI emission and scalability in voltage and power. An additional advantage, which has not been exploited is the possibility to optimize the system operation by routing the power differently among the cells.

This new approach is based on a repairable system with different age of the modular cells. For an extension of the lifetime, the individual cells process different amount of power. Power routing can be used to reduce the average temperature of the aged cells and also the thermal swing on semiconductors, extending their lifetime. In this paper the power routing approach has been successfully demonstrated to have a negligible influence on the efficiency, while allowing to delay significantly wear-out of aged cells.

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