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Frequency-Domain Thermal Modelling and Characterization of Power Semiconductor Devices

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Abstract - The thermal behavior of power electronics devices has being a crucial design consideration because it is closely related to the reliability and also the cost of the converter system. Unfortunately, the widely used thermal models based on lumps of thermal resistances and capacitances have their limits to correctly predict the device temperatures, especially when considering the thermal grease and heat sink attached to the power semiconductor devices. In this paper, frequency-domain approach is applied to the modelling of the thermal dynamics for power devices. The limits of the existing RC lump-based thermal networks are explained from a point of view of frequency domain. Based on the discovery, a more advanced thermal model developed in the frequency domain is proposed, which can be easily established by characterizing the slope variation from the bode diagram of the typically used Foster thermal network. The proposed model can be used to predict not only the internal temperature behaviours of the devices but also the behaviours of heat flowing out of the devices. As a result, more correct estimation of device temperature can be achieved when considering the cooling conditions for the devices.

I. Introduction

Power electronics are being widely used in many important applications of energy conversion system like renewable energy production, motor drives, transportations and power transmission, where the cost of maintenances and failures might be high. Consequently the reliability requirements for power electronics in these systems are getting more critical [1]-[4]. Thermal loading of power semiconductors are especially important, as it is one of the most expensive components and dominant heat sources. It has been demonstrated in [5] that the thermal dynamics under various time scales either inside or outside the power semiconductors could contribute to the quantified damage of the component. As stated in [6]-[12], the fast thermal cycling inside the power devices may cause important fatigues like bond-wire lift-off and cracks/voids in the chip soldering layer, while the slower thermal variations outside the device (i.e. on the

case/baseplate of device or heat sink) will cause important fatigues like cracks on the soldering layer and the thermal grease. As a result the accurate temperatures estimation including the thermal dynamics either inside or outside the power device are critical information not only for the reliability enhancement but also for cost-efficient thermal management of the power converter.

Unfortunately, the thermal stress of the power device is very challenge to model, because it is not only related to the characteristic of the device itself, but also depends a lot on the performance of the attached thermal grease and heat sink. Generally, the thermal behavior for the power devices can be modeled by a series of lumps of thermal resistance R and capacitance C [13]-[17], which together are referred as the thermal impedance Z . According to the connection of RC lumps, they can be grouped into Foster or Cauer type thermal networks, as shown in Fig. 1. The Cauer RC network based on the physical structure of the device is considered to be a relatively correct model to describe the thermal behaviors of power devices. However, an accurate Cauer model is normally hard to use because the internal geometry, materials and effective heat path of device have to be all determined with the help of Finite Element Method (FEM) simulation. On the other hand, the other RC network named Foster type is more popularly used because it is based on the measurement of temperature dynamics of power devices [15], [17], and is independent of the internal structure or material.

One problem with the Foster type thermal network is that its parameters are based on mathematical fitting of the measured/simulated temperature curves, and each of the RC lump in the Foster network represents no physical meaning. Therefore by using this model, only the overall temperature behaviors between the measured points can be guaranteed, provided with a known temperature at the node where heat is flowing out [15]. It has been found that when extending the Foster type thermal network with the thermal models for the thermal grease and heat sink, unrealistic temperature behaviors either inside or outside the power devices will be experienced [13]-[17]. These drawbacks make the Foster type thermal model hard to be utilized for thermal design or lifetime prediction, where the external temperature

and cooling conditions of the power devices need to be carefully characterized.

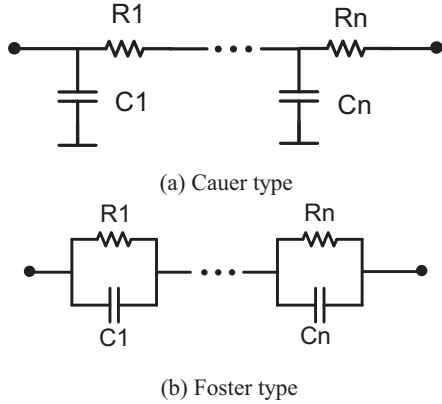


Fig. 1. Commonly used thermal networks for power device based on RC lumps.

In order to improve this problem of Foster thermal network, a mathematical transformation is developed which can convert the Foster network to an equivalent Cauer type with the same number of RC lumps [18], [19]. Although the obvious error of the device temperature when including the cooling conditions seems to be avoided, this mathematical transformation does not regain any physical means of internal structure of power device, and the accuracy of the estimated device temperature still need to be evaluated.

In the last decade, some more advanced modelling techniques have been introduced to improve the prediction of thermal dynamics for power device [19]-[22]. However, they mainly focus on the internal temperature behaviours of the device, and the problems of the existing thermal models when considering the external cooling conditions are not considered or solved.

In this paper, the power loss/heat and temperatures of the power semiconductor devices are considered as signals in the frequency domain, and the corresponding frequency-domain models are first established for several typically used thermal networks. Afterwards the performance and limits of the Foster type and its equivalent Cauer type thermal model are explained from a new point of view. Based on the discovery, a new thermal model is proposed which put more efforts to establish a correct transfer function for the filtering of the power loss, and thereby it can overcome some of the limits in the existing RC thermal networks for the power devices. Finally, some simulation and experimental results are given to validate the accuracy and advantage of the proposal thermal model under both time and frequency domains.

II. Frequency Domain Thermal Modelling and Limits of the Existing Thermal Models Based on RC lumps

A multi-layer Cauer type thermal network for an IGBT module is first defined as a study reference in this paper, as shown in Fig. 2. This Cauer thermal model is extracted from the internal structure and material specifications for a 1700V/100A IGBT module used for wind power application, as shown in Fig. 3 and Table I, a heat spreading angle of 45° is assumed in this case. It can be seen that 7 Cauer type RC lumps are introduced to represent 7 layers of the internal materials of the device as indicated in Fig. 2. In respect to the cooling conditions outside the device, a large thermal resistance is used to represent the thermal behaviour of the thermal grease, and a series of small thermal resistances with large thermal capacitances are used to represent the thermal behaviour of the heat sink. It is assumed that the network in Fig. 2 and the parameters in Table I can correctly reflect the temperature behaviours of the given IGBT module under the given specifications and cooling conditions. Although more detail and complicated modelling techniques such as [21], [22] can be introduced to refine the parameters in Table I, they can be updated depending on the needs of accuracy, but they are not considered in this paper.

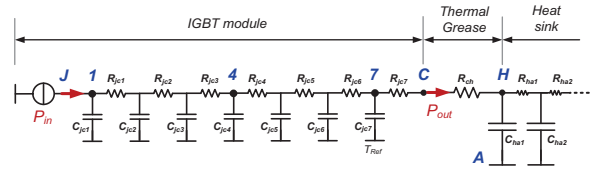


Fig. 2. Cauer type thermal network based on Fig. 3 as reference of study.

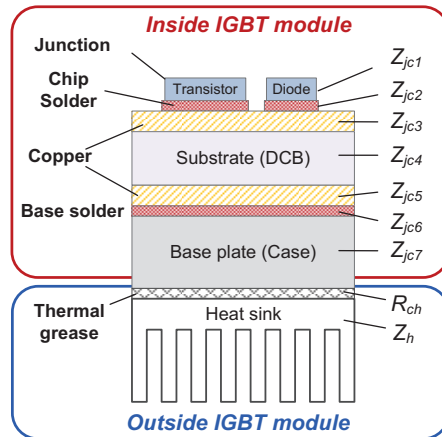


Fig. 3. Construction of an IGBT module as reference for study.

Table I. Parameters for the material, layer and thermal impedance of Fig. 3.

Layers	Thickness (mm)	Density (g/cm ³)	Specific heat (J/kg·°C)	Thermal conductivity (W/m·°C)	Thermal resistance (K/W)	Thermal capacitance (J/K)
Chip (Silicon)	0.3	2.3	790	83.6	0.0194	0.1021
Chip solder	0.05	9.7	260	78	0.0034	0.0179
Copper	0.3	8.9	397	386	0.0040	0.2092
DCB (Al ₂ O ₃)	0.7	3.7	880	18	0.1732	0.5118
Copper	0.3	8.9	397	386	0.0030	0.2732
Base solder	0.1	9.7	260	78	0.0048	0.0517
Base (Copper)	3	8.9	397	386	0.0209	4.0898
Thermal grease	0.021	2.25	NA	0.8	0.0518	NA

Inspired by the typical approach used for the analysis of electrical RC circuits, it is also possible to model the frequency-domain characteristics of the thermal RC networks in order to further understand the thermal behaviors and thermal dynamics of the power device, which will be detailed as follows:

A. Thermal modelling under frequency domain – with Caue network as reference

Normally the power loss P_{in} is injected into the J or 1 node of the Caue type thermal network in Fig. 2, and a series of temperatures and heat flow can be identified in this network. It is noted that the power loss or heat source P_{in} , which is generated in the chips of the IGBT module, can be seen as a disturbance signal; while the corresponding temperatures on each node of the thermal network or different layers of the material can be seen as response signals, so well as for the heat flowing after each node/layer. As a result the gain from the disturbance P_{in} to each of the thermal response under Laplace domain can be analytically solved with the information of R and C parameters.

One group of important relationships between the thermal disturbance and responses, is the gain from input heat P_{in} to the temperature responses on each node of Fig. 2. These gains can be solved by the following functions:

$$Z_{P_{in}T_{X,H}}^{Ref}(s) = \frac{T_X(s) - T_H(s)}{P_{in}} = \begin{cases} 1 / \left(\frac{1}{R_{ch} + R_{jcX}} + s \cdot C_{jcX} \right) & \text{if } X=7 \\ 1 / \left(\frac{1}{Z_{P_{in}T_{X+1,H}}^{Ref}(s) + R_{jcX}} + s \cdot C_{jcX} \right) & \text{if } X=1 \text{ to } 6 \end{cases} \quad (1)$$

where s is the Laplace operator, $Z_{P_{in}T_{X,H}}^{Ref}(s)$ represents the impedance from input loss (P_{in}) to the temperature difference between node X and the heat sink node H ($T_{X,H}$), when the referenced Caue network (Ref) is analyzed. R_{ch} is the thermal resistance of thermal grease, R_{jcX} represents the thermal resistance of each of the 7 layers inside the IGBT module, and C_{jcX} is the thermal capacitance for each layer. The detailed parameters of R_{ch} , C_{jcX} and R_{jcX} can be found from Table I. It is noted that for simplicity of analysis, the heatsink temperature T_H is considered as a reference temperature in the modelling process of this paper, because normally the

thermal capacitance of suitable heat sink is a factor of 100-1000 compared to the internal thermal capacitance of power device, and the temperature on node H is much more stable than the temperatures on nodes 1 to C. However, other reference node such as ambient A can be chosen as the reference temperature, coming with some small deviations in function (1).

Another group of important relationships between the thermal disturbance and responses are the gains from input heat P_{in} to the heat flowing out of each node in Fig. 2. This group of relationships typically is not considered in most of the existing thermal networks, and can be solved as the following functions for the reference Caue model:

$$G_{P_{in}P_{X}}^{Ref}(s) = \begin{cases} \frac{G_{P_{in}P_{X-1}}^{Ref}(s)}{R_{ch} + R_{jcX}} / \left(\frac{1}{R_{ch} + R_{jcX}} + s \cdot C_{jcX} \right) & \text{if } X=7 \\ \frac{G_{P_{in}P_{X-1}}^{Ref}(s)}{G_{P_{in}P_{X+1,H}}^{Ref}(s) + R_{jcX}} / \left(\frac{1}{G_{P_{in}P_{X+1,H}}^{Ref}(s) + R_{jcX}} + s \cdot C_{jcX} \right) & \text{if } X=1 \text{ to } 6 \end{cases} \quad (2)$$

where $G_{P_{in}P_{X}}^{Ref}(s)$ represents the gain from input heat/loss (P_{in}) to the heat flowing out of node X (P_{X}), when the reference Caue network (Ref) is chosen.

Based on (1) and (2), the gain from P_{in} to the temperature difference between junction node J and case node C, as well as the gains from P_{in} to the heat flowing out of the device P_{out} , can be solved as:

$$Z_{P_{in}T_{J,C}}^{Ref}(s) = \frac{T_J(s) - T_C(s)}{P_{in}} = Z_{P_{in}T_{J,H}}^{Ref}(s) - R_{ch} \cdot G_{P_{in}P_7}^{Ref}(s) \quad (3)$$

$$G_{P_{in}P_{out}}^{Ref}(s) = G_{P_{in}P_7}^{Ref}(s) \quad (4)$$

It is noted that $G_{P_{in}T_{J,C}}$ and $G_{P_{in}P_{out}}$ are selected as two of the indicators to benchmark the accuracy of thermal models focused in this paper. As a result the frequency-domain model for the reference 7 layers Caue type thermal network is established.

B. Thermal modelling under frequency domain – Foster network

When applying a step power loss P_{in} to the reference Caue network shown in Fig. 2, the temperature response in node J and node C can be measured and recorded, afterwards the Foster type thermal network and its RC parameters can be extracted by curve-fitting the time-domain temperature responses with the following functions [10]:

$$Z_{jc}^{Foster}(t) = \frac{T_j(t) - T_c(t)}{P_{in}} = \sum_{n=1}^X R_{fn} \cdot (1 - e^{-t/(R_{fn} C_{fn})}) \quad (5)$$

where R_{fn} and C_{fn} represent the mathematically-solved thermal resistance and thermal capacitance for the Foster thermal network, and are connected in the form as indicated in Fig. 4. In (5) X means the number of pairs

for the used R_{fn} and C_{fn} , normally 4 pairs of the Foster RC parameters can achieve an accurate fitting to most of the temperature responses between node J and C for the IGBT module. In this paper the RC parameters are summarized in Table II.

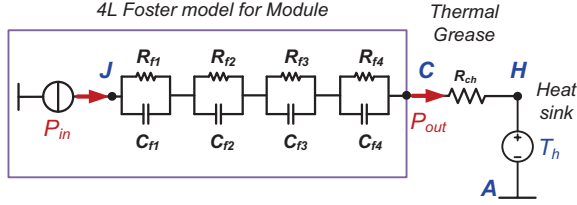


Fig. 4. Foster type 4L thermal network fitted from the referenced Cauer network shown in Fig.2. (J denotes junction node, C, case node, H heat sink node, A ambient node)

Table II. RC parameters of the Foster and equivalent Cauer network in Fig. 4 and Fig. 5.

Foster network		Equivalent Cauer network	
Thermal resistance Rf1-4 (W/K)	Thermal capacitance Cf1-4 (J/K)	Thermal resistance Rec1-4 (W/K)	Thermal capacitance Cec1-4 (J/K)
0.0014	15.646	0.0249	0.1062
0.0188	0.0023	0.1602	0.7285
0.0892	0.4059	0.0422	8.39
0.1191	0.1167	0.0013	11950

The gain from input loss P_{in} to the temperature difference between node X and heat sink, as well as the gain from input loss P_{in} to the heat flow/power loss after each node X can be solved in (6) and (7) respectively for the Foster thermal network as:

$$Z_{P_{in}T_{X-H}}^{\text{Foster}}(s) = \sum_{n=X}^4 \frac{R_{fn}}{R_{fn}C_{fn} \cdot s + 1} + R_{ch} \quad (6)$$

$$G_{P_{in}P_{Xc}}^{\text{Foster}}(s) = 1 \quad (7)$$

Then the two benchmark indicators $Z_{P_{in}T_{jc}}$ and $G_{P_{in}P_{out}}$ for the given 4 layers Foster thermal network can be solved in (8) and (9):

$$Z_{P_{in}T_{jc}}^{\text{Foster}}(s) = \sum_{n=1}^4 \frac{R_{fn}}{R_{fn}C_{fn} \cdot s + 1} \quad (8)$$

$$G_{P_{in}P_{out}}^{\text{Foster}}(s) = 1 \quad (9)$$

C. Thermal modelling in the frequency domain – Equivalent Cauer network [18]

This type of thermal network targets to solve some problems of the Foster type thermal network as mentioned before, and it is often used for the electro-thermal simulation of the power device temperature. By applying the mathematical transformation and boundary conditions shown in [18], the Foster type RC network in Fig. 4 can be converted to an equivalent Cauer type thermal network with the same pair numbers of RC parameters but different values, as shown in Fig. 5 and Table II.

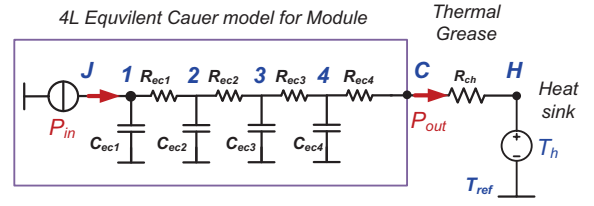


Fig. 5. Equivalent 4L Cauer type thermal network converted from the Foster network shown in Fig.4. (J denotes junction node, C, case node, H heat sink node, A ambient node).

Thereby the frequency domain thermal model for the given 4 layers equivalent Cauer RC network can be established. The gain from input loss P_{in} to the temperature difference between node X and heat sink, as well as the gain from input loss P_{in} to the heat flow/power loss after each node X can be solved in (10) and (11) respectively. The two benchmark indicators $Z_{P_{in}T_{jc}}$ and $G_{P_{in}P_{out}}$ can be solved in (12) and (13):

$$Z_{P_{in}T_{X-H}}^{\text{eqCauer}}(s) = \frac{T_X - T_H}{P_{in}} = \begin{cases} 1 / \left(\frac{1}{R_{ch} + R_{ecX}} + s \cdot C_{ecX} \right) & \text{if } X = 4 \\ 1 / \left(\frac{1}{Z_{P_{in}T_{X+1-H}}^{\text{eqCauer}}(s) + R_{ecX}} + s \cdot C_{ecX} \right) & \text{if } X = 1 \text{ to } 3 \end{cases} \quad (10)$$

$$G_{P_{in}P_{Xc}}^{\text{eqCauer}}(s) = \begin{cases} \frac{G_{P_{in}P_{X+1-H}}^{\text{eqCauer}}(s)}{R_{ch} + R_{ecX}} / \left(\frac{1}{R_{ch} + R_{ecX}} + s \cdot C_{ecX} \right) & \text{if } X = 4 \\ \frac{G_{P_{in}P_{X+1-H}}^{\text{eqCauer}}(s)}{G_{P_{in}P_{X+1-H}}^{\text{eqCauer}}(s) + R_{ecX}} / \left(\frac{1}{G_{P_{in}P_{X+1-H}}^{\text{eqCauer}}(s) + R_{ecX}} + s \cdot C_{ecX} \right) & \text{if } X = 1 \text{ to } 3 \end{cases} \quad (11)$$

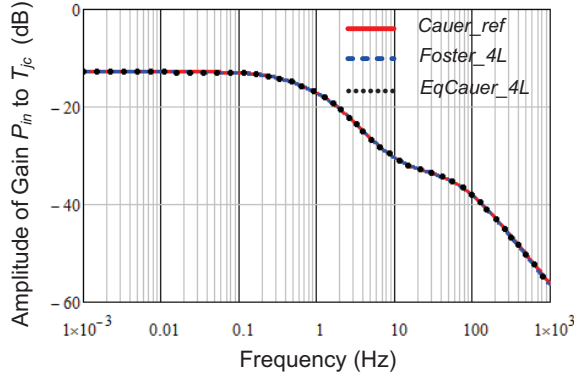
$$Z_{P_{in}T_{jc}}^{\text{eqCauer}}(s) = \frac{T_{j-H} - T_{c-H}}{P_{in}} = Z_{P_{in}T_{j-H}}^{\text{eqCauer}}(s) - R_{ch} \cdot G_{P_{in}P_{j-H}}^{\text{eqCauer}}(s) \quad (12)$$

$$G_{P_{in}P_{out}}^{\text{eqCauer}}(s) = G_{P_{in}P_{c}}^{\text{eqCauer}}(s) \quad (13)$$

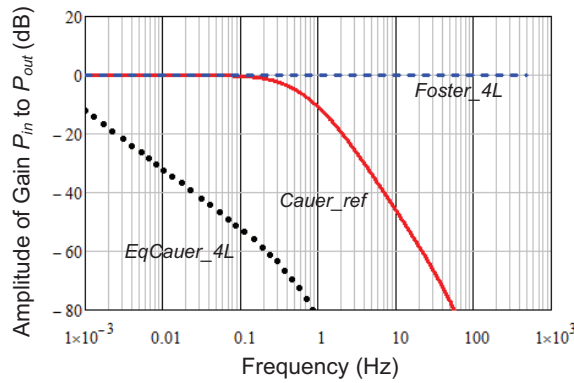
D. Limits of existing thermal models based on RC lumps

With the built frequency-domain models of the three types of thermal networks, the Bode plot of some interesting gains can be compared. One benchmark Bode plot is the gain from loss P_{in} to the temperature

difference between junction and case, which is normally provided by the manufacturer datasheet or measured by the user as an important thermal characteristic of the power device. As it can be seen in Fig. 6 (a), the difference in gains among the three types of thermal models is almost ignorable.



(a) Gains from Pin to Tjc.



(b) Gains from Pin to Pout.

Fig. 6. Bode plot of critical gains in various thermal networks under frequency domain. (Cauer_ref: reference 7 layer Cauer thermal network, Foster_4L: 4 layer Foster type fitting network to the temperature response of Cauer_ref, EqCauer_4L: mathematical transformation from Foster_4L to the equivalent Cauer type).

However, when comparing the Bode plot of the other benchmark gains from P_{in} to the output heat of power device P_{out} , the difference among the three types of thermal models are significant, as shown in Fig. 6 (b): As the correct thermal behavior assumed in this paper, the reference 7 layers Cauer type thermal network (Cauer_ref) behaves like a second-order low pass filter to the input heat P_{in} with bandwidth around 0.5 Hz. The curve-fitted 4 layers Foster type thermal network (Foster_4L) behaves transparently to the frequency components of P_{in} whose disturbances will be immediately seen by the thermal grease and heatsink outside the power device (obviously incorrect in real case). On the contrary the equivalent 4 layers Cauer type

thermal network (eqCauer_4L) transformed from Foster_4L has much lower bandwidth compared to the Cauer_Ref, which means many important disturbances of P_{in} in the real case will be blocked and not seen by the thermal grease and heatsink.

By including a large thermal resistance R_{ch} of the thermal grease to the three thermal networks, the Bode plot of the gains from P_{in} to the junction temperature T_j with different thermal networks are shown in Fig. 7, (with heat sink temperature T_H as the reference temperature) It can be seen that the limits of the Foster_4L and eqCauer_4L thermal network can be more clearly identified: The Foster_4L has a good agreement with the reference Cauer model at lower frequency band, but there is a large error on the high frequency band. On the contrary, the eqCauer_4L has a good agreement with the reference Cauer model at high frequency band, but there is a large error at the low frequency band.

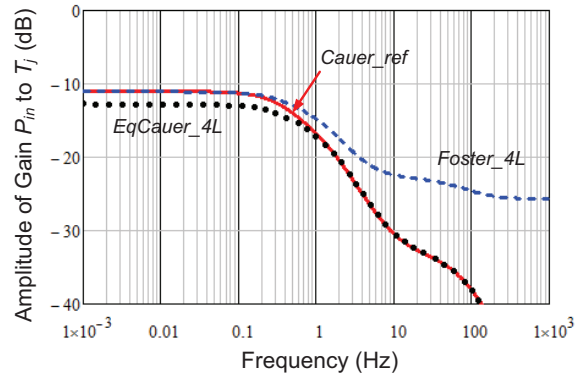


Fig. 7. Bode plot of gains from Pin to Tj in various thermal networks. (Heat sink temperature T_H is used as reference temperature, Cauer_ref: reference 7 layer Cauer type thermal network, Foster_4L: 4 layer Foster type fitting network to the temperature response of Cauer_Ref network, EqCauer_4L: mathematical transformation from Foster_4L to the equivalent Cauer type)

The time domain simulations also agree with the behaviours predicted in the frequency domain, as shown in Fig. 8, where a step power loss P_{in} of 100 W at the time of 1 second is applied to various thermal networks. It can be seen that compared to the Cauer_Ref model, the Foster network has no filtering effect to the injected power loss/heat, which immediately flows through the thermal grease outside the device and result in a large error at the beginning of the thermal transient of the junction temperature T_j ; but the steady-state T_j is more consistent with the Cauer_Ref. The equivalent Cauer type network converted from the Foster type has an over-filtering effect to the injected power loss/heat, and thereby the junction temperature T_j has a large error at the beginning of the thermal transient with the Cauer_Ref.

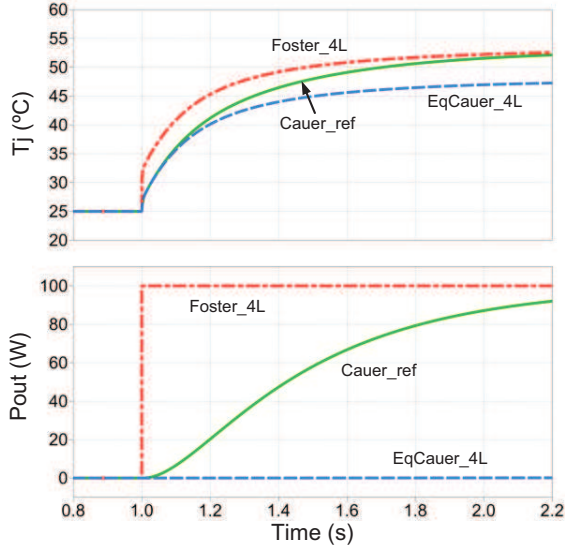


Fig. 8. Time domain simulation of the junction temperature under a step power loss in various thermal networks (100 W loss step at 1 second, $T_H=25^\circ\text{C}$).

As a conclusion, either the Foster or its equivalent Cauer type thermal network has their limits to describe the correct thermal dynamics of the power device. The key to achieve more correct thermal modelling, especially when considering the thermal grease and heat sink, is to create a correct filtering to the power loss – or correct heat gain from P_{in} to P_{out} ($G_{P_{in}P_{out}}$) under the frequency-domain.

III. A New Thermal Model for power device under Frequency Domain

A. Characterization of the heat flowing out of device

In the practice, the Cauer type RC parameters based on the structure and material of the power semiconductor devices is difficult to be accurately accessed; and the correct heat gain from P_{in} to P_{out} is also hard to be directly solved from the commonly used Foster type thermal network. Thereby other approaches have to be investigated in order to find the correct gain from P_{in} to P_{out} .

As illustrated in Fig. 9, by looking at the slopes and corner frequencies of the heat gains $G_{P_{in}P_1}$ to $G_{P_{in}P_7}$, the 7 layers of materials in the reference Cauer network can be generally seen as a series of low-pass filters and can be classified into three dominant groups: the first group consists of layers from chip to the upper copper as shown in Fig. 10, (Node 1 to 4 in Fig. 2), the second group consists of layers from DCB to Base solder (Node 4 to 7), and the third group consists of layer of base plate (Node 7 to C). It is interesting to see that in each group of material layers, the frequency behaviours of heat

gains are very similar to each other. The characteristics (corner frequencies and slope changes) among the three groups of heat gains generally follow the behaviours of three cascaded low-pass filters. As a result, the reference 7 layer Cauer type thermal network for the device can be degraded to 3 cascaded 1st-order low pass filters, as illustrated in Fig. 10, where C_{jc123} , C_{jc456} , C_{jc7} represent the virtual thermal capacitances for each dominant group of layers, and P_{123} , P_{456} , P_7 represent the virtual heat flowing out of each dominant group of layers.

Because the DC gains of the heat transfer function on each node all equal to 0 dB, the key to establish correct gain from input loss P_{in} to output loss of device P_{out} ($G_{P_{in}P_{out}}$), is to identify the three dominant corner-frequencies of the cascade low-pass filter shown in Fig. 9.

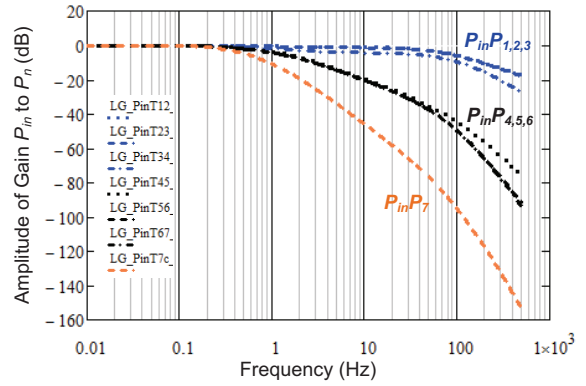


Fig. 9. Bode plot of heat gains in different nodes of the reference 7 layers Cauer network.

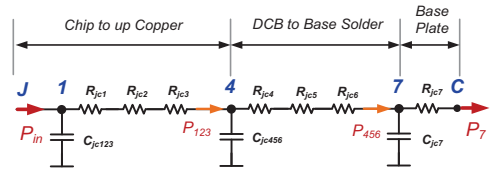


Fig. 10. Transforming of the 7L-Cauer type network to 3 cascaded low pass filter according to the frequency behaviours of Fig. 9.

Based on the simplified thermal network shown in Fig. 10, the benchmark thermal impedance of the power device $Z_{P_{in}T_{jc}}$ can be revised as the sum of three parts:

$$\begin{aligned} Z_{P_{in}T_{jc}}(s) &= Z_{P_{in}T_{14}}(s) + Z_{P_{in}T_{47}}(s) + Z_{P_{in}T_{7c}}(s) \\ &= G_{P_{in}P_{123}}(s) \cdot \sum_{X=1}^3 R_{jcX} + G_{P_{in}P_{456}}(s) \cdot \sum_{X=4}^6 R_{jcX} + G_{P_{in}P_7}(s) \cdot R_{jc7} \end{aligned} \quad (14)$$

By ignoring some of the high frequency band behaviors in the heat gains $G_{P_{in}P_{456}}$, $G_{P_{in}P_7}$, and only considering their first-order low-pass-filter (LPF) behaviors, (14) can be simplified as:

$$\begin{aligned}
Z_{P_{in}T_{jc}}(s) &\approx G_{P_{in}P_{123}}(s) \cdot R_{jc1-3} + G_{P_{123}P_{456}}(s) \cdot R_{jc4-6} + G_{P_{456}P_7}(s) \cdot R_{jc7} \\
&= \frac{1}{\frac{1}{2\pi f_{cr1}} \cdot s + 1} \cdot R_{jc1-3} + \frac{1}{\frac{1}{2\pi f_{cr2}} \cdot s + 1} \cdot R_{jc4-6} + \frac{1}{\frac{1}{2\pi f_{cr3}} \cdot s + 1} \cdot R_{jc7}
\end{aligned} \quad (15)$$

which is equivalent to the form of three-layers Foster thermal network under frequency-domain, and the frequencies f_{crx} on each layer of the Foster network is the same as the corner frequencies in the heat gains.

It can be seen that, the thermal impedance $Z_{P_{in}T_{jc}}$ is inherently correlated with the heat gains of the three dominant groups of material. Therefore it is possible to extract the corner-frequencies of the heat gains from the thermal impedance $Z_{P_{in}T_{jc}}$, which can be more accurately and easily acquired with experimental measurement. Then the key of the question is to determine the correct values of corner frequencies and thermal resistance on each layer of (15), by knowing the behaviours of $Z_{P_{in}T_{jc}}(t)$.

In Fig. 11, the Bode diagram of $Z_{P_{in}T_{jc}}(s)$ and its three components $Z_{P_{in}T_{14}}$, $Z_{P_{in}T_{47}}$, and $Z_{P_{in}T_{7C}}$ are plotted with the slope changing information, several corner-frequencies on $Z_{P_{in}T_{14}}$, $Z_{P_{in}T_{47}}$, and $Z_{P_{in}T_{7C}}$ can be seen. By applying a deviating operator $F(x)$ to the $Z_{P_{in}T_{jc}}(s)$, as illustrated in (16), the slope deviation on the amplitude of the $Z_{P_{in}T_{jc}}(s)$ can be identified, as shown in Fig. 12, in which the turning points (representing several critical frequencies f_1 - f_3) are closely related to the corner frequencies f_{cr1} - f_{cr3} on the three groups of heat gains in Fig. 9.

$$F(x) = \frac{\delta^2}{\delta x^2} 20 \cdot \log_{10}(|Z_{P_{in}T_{jc}}(10^x)|) \quad (16)$$

However, according (15), the critical-frequencies identified from $Z_{P_{in}T_{jc}}$ are slightly different from the corner-frequencies in the heat gains, because the corner-frequencies in the heat gains will be disturbed during the weighted summing up with R_{jcx} to compose $Z_{P_{in}T_{jc}}$.

One solution to this problem is to refit $Z_{P_{in}T_{jc}}(t)$ with a new Foster network, by setting the boundary conditions of fitting algorithm with the numbers and ranges of critical frequencies f_1 - f_3 identified from Fig. 12. As a result the parameters in each layer of (15) can be solved, which includes the information of critical frequencies f_{cr1} - f_{cr3} in the heat gains. It is noted that the number of Foster layers used for refitting depends on the number of critical frequency identified from $Z_{P_{in}T_{jc}}(s)$. In the case of the given IGBT module for case study, three critical frequencies $f_1 = 0.316$ Hz, $f_2 = 1.422$ Hz, and $f_3 = 74.129$ Hz can be identified from $Z_{P_{in}T_{jc}}(s)$ as boundary conditions for fitting, and three frequencies of $f_{cr1} = 0.38$ Hz, $f_{cr2} = 1.36$ Hz, and $f_{cr3} = 70.36$ Hz, can be solved from the fitted Foster network as the corner frequencies for heat gains.

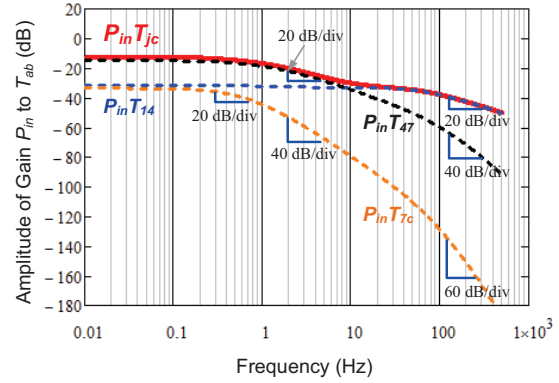


Fig. 11. Bode plot and slope of thermal impedance gains for the reference 7L Cauer type network.

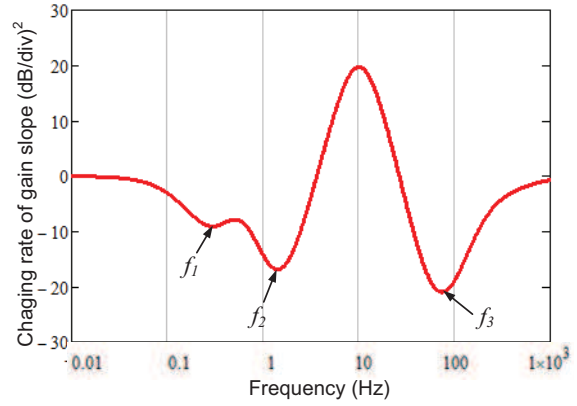


Fig. 12. Identified corner-frequencies from bode plot of $Z_{P_{in}T_{jc}}$ in Fig. 11.

By cascading the three 1-order low-pass filters with the extracted corner frequencies and unity DC gain, the heat transfer function $G_{P_{in}P_{out}}$ for the power device can be recomposed by only the information of the measured Foster type thermal impedance $Z_{P_{in}T_{jc}}$. So the low-pass filter for the power loss can be calculated as:

$$G_{LPF}(s) = \frac{2\pi f_{cr1}}{s + 2\pi f_{cr1}} \cdot \frac{2\pi f_{cr2}}{s + 2\pi f_{cr2}} \cdot \frac{2\pi f_{cr3}}{s + 2\pi f_{cr3}} \quad (17)$$

In Fig. 13, the Bode plot of the heat gains $G_{P_{in}P_{out}}$ by the new methods are shown, and it can be seen that the extracted 3-order Low Pass Filter from the Foster thermal network has almost the same frequency behaviour with the $G_{P_{in}P_{out}}$ in the reference Cauer thermal network. As a comparison, the $G_{P_{in}P_{out}}$ of the Foster thermal network in Fig. 4 is also shown.

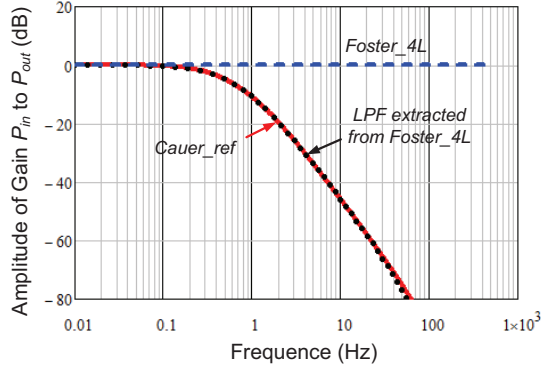


Fig. 13. Bode plot of heat gain $G_{PinPout}$ by different thermal networks.

B. A new thermal model in the frequency domain

As a result, a new thermal model is proposed based on the extracted $G_{PinPout}$. As shown in Fig. 14, the proposed thermal model contains of two paths: The first thermal path is used for the junction temperature estimation inside power device. In this path the datasheet-based or experimentally measured Foster thermal network of power device are used, and only a reference temperature, whose value is determined by the case temperature T_c from the other thermal path, is connected. The second thermal path is used for the temperature estimation outside device. In this path the extracted low pass filter from the Foster thermal network is used to model the loss behaviours flowing out of the device, and the filtered loss can create correct temperature behaviour of thermal grease T_{CH} and heat sink T_{HA} outside the devices.

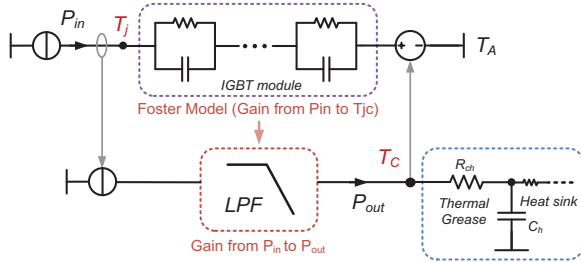


Fig. 14. Proposed thermal model for power device based on frequency domain.

The two benchmark indicators Z_{PinTjC} and $G_{PinPout}$ for the new thermal model can be solved in (18) and (19), and then the gain from P_{in} to junction temperature can be calculated in (20):

$$G_{P_{in}T_{jc}}^{New}(s) = G_{P_{in}T_{jc}}^{Foster}(s) \quad (18)$$

$$G_{P_{in}P_{out}}^{New}(s) = G_{LPF}(s) \quad (19)$$

$$Z_{P_{in}T_j}^{New}(s) = \frac{T_{jc} + T_{ch}}{P_{in}} = Z_{P_{in}T_{jc}}^{Foster}(s) + R_{ch} \cdot G_{LPF}(s) \quad (20)$$

The Bode plot of $Z_{P_{in}T_j}$ and the time-domain simulation on the same conditions of Fig. 8 are implemented on the new thermal model, as shown in Fig. 15, and Fig. 16, respectively. It can be seen that, there are good agreement of the new thermal model with the reference 7 layer Cauer model both in the frequency domain and in the time domain. It is noted that the new thermal model is only based on the information of Foster type thermal network, which is commonly accessed from the datasheet or external measurements of device, and it is independent of the internal materials, structure and heat path information of devices, being a promising advantage.

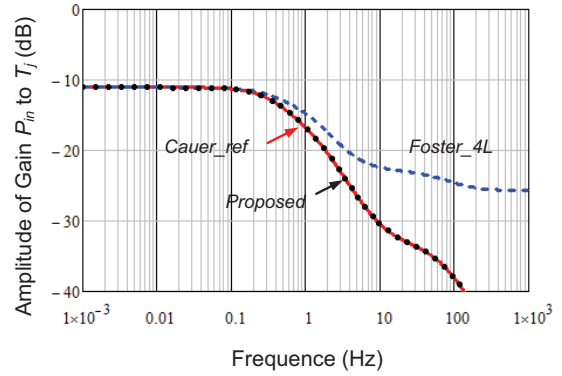


Fig. 15. Bode plot of gains from Pin to Tj in various thermal networks. (T_H is used as a reference temperature)

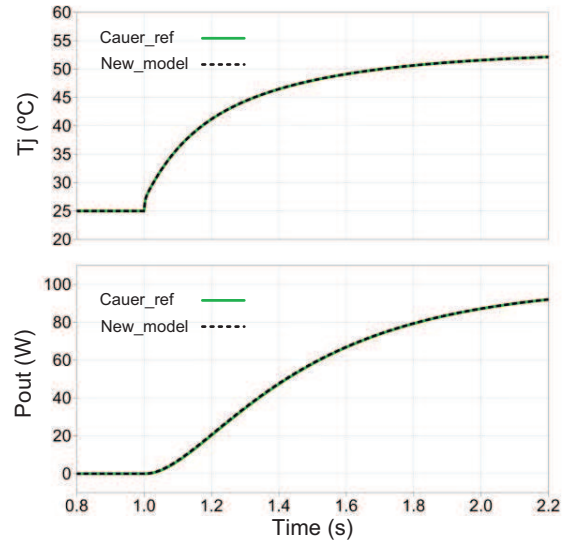
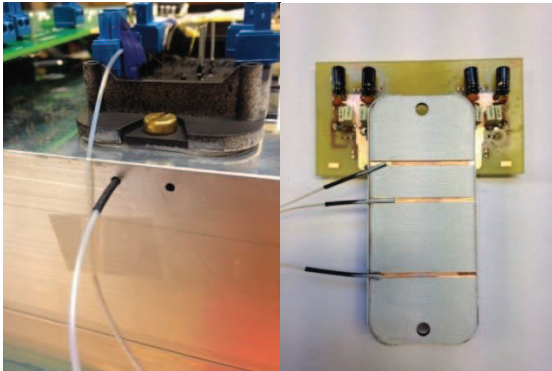


Fig. 16. Time-domain simulation of the thermal dynamics under a step power loss in the proposed thermal network (same conditions of Fig. 8, 100 W loss step at 1 second).

IV. Experimental characterization and validation

A 30A/1200V power Module for PV application is used to validate the performance of the proposal thermal model. A few optical fibers from Opsens for thermal measurements are set to the chips, baseplate, heat sink and the air channel in the heat sink to monitor several critical temperature nodes in the thermal networks, as illustrated in Fig. 17, where a 1 mm depth of gap is curved on the baseplate of module and a 1 mm diameter hole is drilled into the heat sink for the mounting of sensors. The measuring point for the junction node is in the centre of a MOSFET chip and the rest of measured nodes are all allied in the heat path right beneath chip of the module. The optical sensor has a measurement range of $-40\text{ }^{\circ}\text{C}$ to $+250\text{ }^{\circ}\text{C}$ with accuracy of ± 0.3 to $0.8\text{ }^{\circ}\text{C}$, and the response time is limited to 5 ms.

Then the target MOSFET chip is turned off with constant current of 20A and conduction voltage of 1.315 V, which is equivalent to a step power loss of 26.3 W applied to the thermal networks of the power module. The junction temperature T_j , case temperature T_c , heat sink temperature T_h and ambient temperature T_a are recorded in the time span of 15 seconds, as shown in Fig. 18. Because the conduction voltage of device is not constant during the turn-on process, actually the voltage at the instant of turning off is measured, and then a mathematical transformation is applied to the recorded waveforms to make the temperatures rise along with the time.



(a) Sensors attached in the base plate of device.

(b) Sensors attached in the heat sink.

Fig. 17. Experimental setup and sensor locations for the thermal measurements of power device.

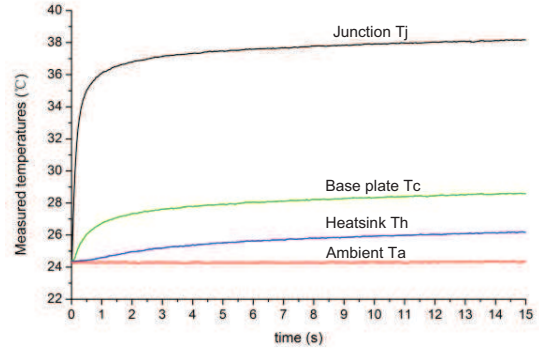


Fig. 18. Measured thermal dynamics under a step power loss of 26.3 W in a IGBT chip.

A. Characterization of thermal behaviours under frequency domain

By initial fitting the measured temperature difference of T_j and T_c with the functions shown in (5), the 4 layer Foster type thermal network for the power module can be established, and the RC parameters are shown in Table III. As a result the frequency-domain thermal impedance $G_{P_{in}T_jc}$ for the measured power module is plotted in Fig. 19.

Table III. Extracted parameters of the Foster and equivalent Cauer network from the experimental results.

Foster network		Equivalent Cauer network	
Thermal resistance Rf1-3 (W/K)	Thermal capacitance Cf1-3 (J/K)	Thermal resistance Rec1-3 (W/K)	Thermal capacitance Cec1-3 (J/K)
0.0219	46.6	0.3466	0.3713
0.2019	0.631	0.01655	60.43
0.1395	0.920	0.000196	661.9

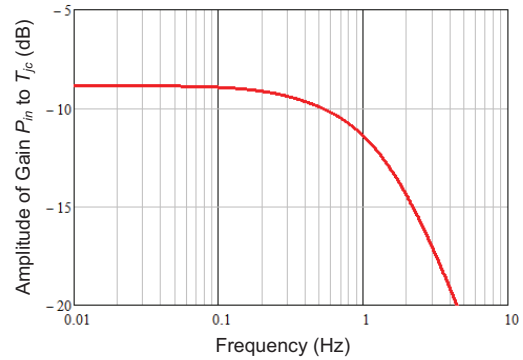


Fig. 19. Bode plot of the measured thermal impedance from P_{in} to T_{jc} ($Z_{P_{in}T_{jc}}$).

By deviating the slope of Z_{PinTjc} , the critical-frequencies on the Z_{PinTjc} can be identified, as shown in Fig. 20. It is noted that only two critical frequencies are seen in the experimental results, because the response time of the sensor is limited at 5 ms, which corresponds to a cut-off frequency around 30 Hz, and this will filter out many high frequency behaviours.

Another important discovery from Fig. 20 is that the critical frequency f_1 is not so significant to be accurately identified; this is mainly because the thermal resistance at this band is much smaller than the one around f_2 , based on the function (14). The solution to this problem is to set only one critical frequency f_2 as boundary condition for the fitting algorithm, with undetermined numbers of RC layers. After refitting $Z_{PinTjc}(s)$, the new foster network should contain one layer (referred as $Z_{f2}(s)$) that represents the corner frequency of f_{cr2} in the heat gain and corresponding thermal resistance. Afterwards the rest of the critical frequencies in $Z_{PinTjc}(s)$ can be more accurately identified by analysing the function of $Z_{PinTjc}(s)-Z_{f2}(s)$, which excludes the behaviours of $Z_{f2}(s)$, as illustrated in Fig. 21.

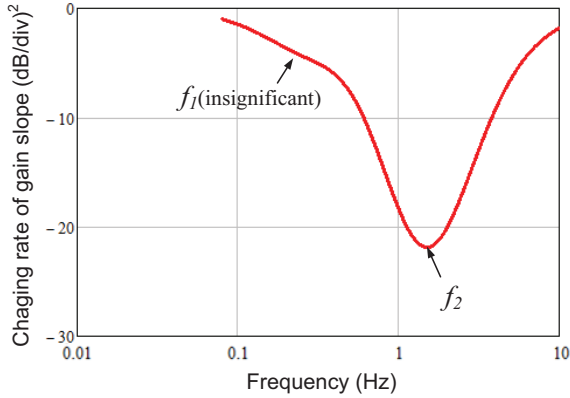


Fig. 20. Identified corner-frequencies from bode plot of Z_{PinTjc} in Fig. 19.

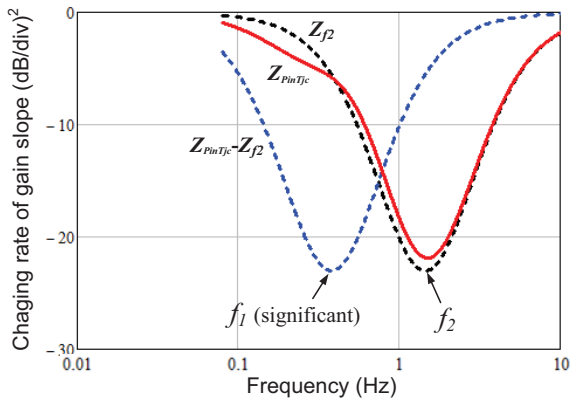


Fig. 21. Extract the insignificant critical frequency f_1 from Fig. 20.

By refitting the frequency behaviours of Z_{PinTjc} with a new Foster thermal network, and setting the boundary conditions of the numbers and ranges of critical frequency f_1 and f_2 to the fitted RC pairs, the corner frequencies for the low pass filter of the power loss can be extracted, in this case $f_{cr1}=0.379$ and $f_{cr2}=1.452$, and the $G_{PinPout}$ of the power module can be plotted in Fig. 22.

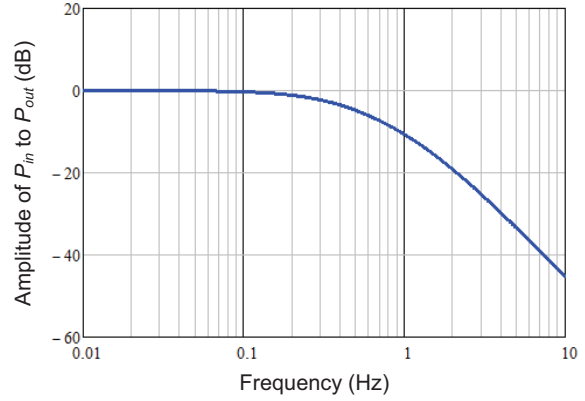


Fig. 22. Extracted heat gain $G_{PinPout}$ from Fig. 21.

As a summary, the flow chart to extract the proposal new thermal model is shown in Fig. 23, where the inputs and outputs of the process are demonstrated.

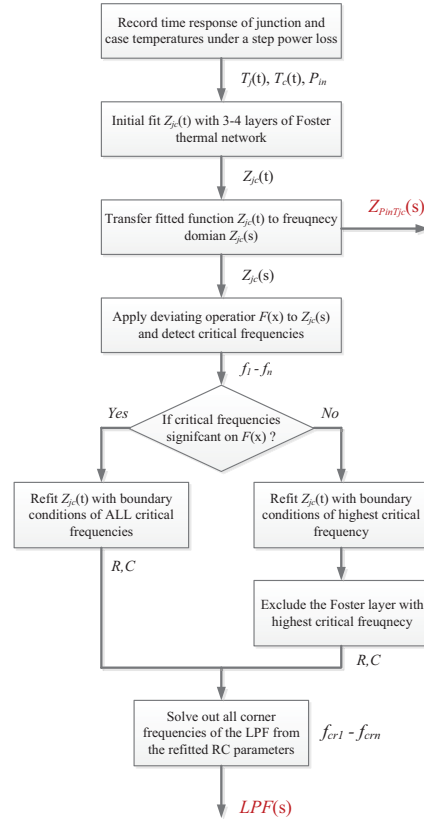
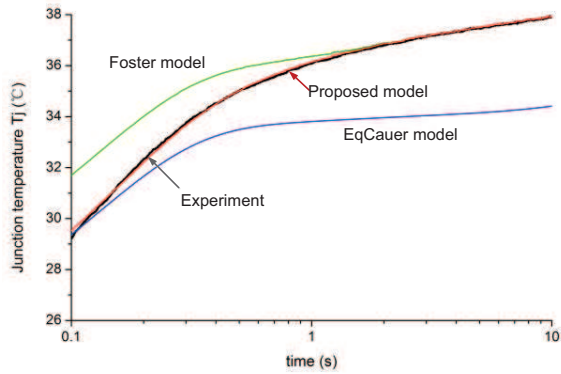


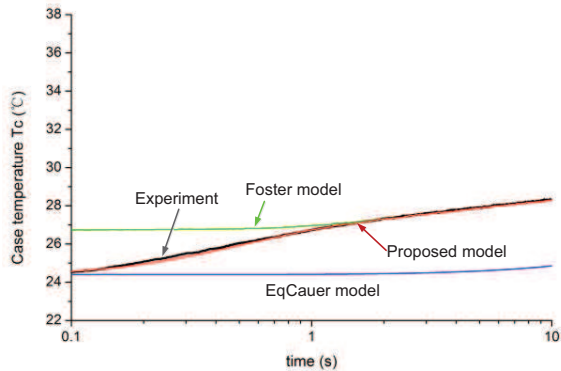
Fig. 23. Flow chart to acquire $Z_{PinTjc}(s)$ and LPF(s) in Fig. 14.

B. Comparison of the thermal models

The experimentally recorded junction temperature T_j and case temperature T_c , as well as the estimated temperatures by using various thermal networks are shown in Fig. 24 (a) and Fig. 24 (b), respectively, where the heat sink temperature by experiment is used as the reference temperature for the models. It is noted that the response time of the temperature sensors is limited to 5 ms, making the step response of thermal dynamics below 0.1 s slower than the actual value, and therefore only the thermal dynamics above 0.1 s is shown and used for the analysis. As it can be seen, the experimental results agree well with the simulations shown in Fig. 8 and Fig. 16: The proposed thermal model can not only correctly reflect the thermal behaviours of the temperatures inside the power device, but also has a good agreement with the thermal behaviours outside the power devices, which is hard to be achieved by the existing Foster and its equivalent Cauer thermal networks.



(a) Junction temperature T_j .



(b) Base plate temperature T_c .

Fig. 24. Comparison of the estimated temperatures of device by various thermal models (the measured T_H is set as reference temperature).

V. Conclusion

Frequency domain modelling is conducted on several typically used thermal networks for power

semiconductor devices. It is found that either the widely used Foster type or its equivalent Cauer type thermal networks have their limits to correctly predict the device temperatures, especially when considering the cooling conditions outside the device. The main reason is due to the incorrect heat behaviour flowing out of the device.

A new thermal model is proposed in this paper, which put more efforts to establish a correct transfer function for the filtering effects of the power loss. It is only based on the information of Foster type thermal network, which is easily accessible from the datasheet or external measurements, and it is independent of the internal materials and structure information of devices. Compared to the existing thermal models, the proposed model can achieve a more correct estimation of device temperature, when considering the cooling conditions.

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