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Analysis of the frequency-based control of a master/slave micro-grid

Giampaolo Buticchi

Giovanni De Carne

Davide Barater

Zhixiang Zou

Marco Liserre

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Analysis of the Frequency-Based Control of a Master/Slave Micro-Grid

Abstract

Renewable energy penetration in the low-voltage grid faces several limitations due to the current grid topology. Master/slave micro-grids could help solving these issues, by offering additional services to the grid, such as the power management of the distributed power energy sources.

In some cases, the power produced by the distributed energy sources exceeds the local consumption of the low-voltage grid. The consequent reverse power flow can be either dangerous (for the medium voltage) or impossible (for a micro-grid with limited storage). The droop characteristic of commercial inverter can be exploited to avoid this behavior. However stability problems can arise due to a low phase-locked-loop (PLL) bandwidth. This paper investigates the stability of this solution depending on the bandwidth of the PLL of the distributed power generation sources.

I. INTRODUCTION

The distributed power generation systems (DPGS) became more and more important over the last few years. Their increasing popularity has been driven by the use of renewable energy sources and the rising costs of the energy distribution, leading to modifications of the electric grid. Among the renewable energy sources employed in this framework, photovoltaic (PV) is receiving a great attention. PV systems can be divided into island-grid (or stand-alone), where the converters supply local loads, and grid-connected, where the power produced by the panels is transferred to the electrical grid.

In general, grid-connected systems have been preferred to stand-alone ones, since the mains can compensate the energy production oscillations due to the variable nature of the PV source. As a consequence a great number of distributed low power sources have been connected to the LV grid in the last years, leading in some case to grid stability problem such as: transformer reverse power flow, voltage rise, unexpected islanding operations, sympathetic tripping, etc. [1], [2].

To partially mitigate these problems, standards have recently imposed to grid-connected inverters to vary their output power in function of the instantaneous value of grid voltage and frequency (CEI-021 [3]). In fact, when in a LV grid the amount of energy from installed distributed sources is comparable to the loads' consumption, particular care must be taken to manage conditions of high imbalance between power generation and energy demand. Therefore, grid-connected systems have to limit their output power to face the cases of low local consumption. For PV systems an example is that of summer months in south European regions, when to an high PV energy production may not correspond an equivalent local demand [4].

This paper investigates the stability of a micro-grid where a frequency control is adopted to manage the power balance [5]–[7]. The basic assumption is that the frequency of the micro-grid can be changed (fully-decentralized micro-grid or smart-transformer micro-grid) to interact with the distributed sources. The novelty of the proposed approach is that standard current-controlled grid-connected converters are used, as opposed to the droop-controlled micro-grid. It is shown that the Phase Locked Loop (PLL) of the distributed energy system affects the stability of the grid.

The paper is organized as follows, Section II is related to the state of art of micro-grid concepts, the Smart Transformer-fed grid concept is explained in section III. In section IV the concept of frequency depending power derating is presented; in section V the stability analysis of the system is addressed. Simulation and experimental verification are shown in section VI. A discussion regarding the required power rating of the master inverter is reported briefly in section VII, and the applications scenario is discussed in section VIII. Section IX draws the conclusions.

II. STATE OF ART OF MICRO-GRID CONCEPTS

The parallel operation of multiple Voltage Source Converters (VSC) was widely investigated by researchers, with the aim to realize Uninterruptible Power Supply (UPS) [8] or self-sustaining micro-grids. In case of micro-grid, the grid stability must be guaranteed by the control strategy of the connected VSCs, that have to cooperate for a smart managing of the distributed energies sources; a feature that is not envisaged by existing grid-connected converters. With respect to a fully-decentralized micro-grid (Fig. 1), the use of Smart Transformer (ST) holds particular interest, as it faces the problem of the existing electronic equipment already present in the LV grid.

The scenario is depicted in Fig. 2. It retains the characteristics of actual distribution grid, where the power distributor still holds the ability to control the grid parameters. The grid-connected VSCs react to the grid parameter variations but still perform their own algorithm, since the grid power management is realized by the ST. Moreover, the ST expands the freedom of the grid's owner, allowing finer controls. From the point of view of the control, these two cases are equivalent. The main difference is represented by the storage capability, since a fully-decentralized micro-grid is very likely to have batteries to guarantee continuous

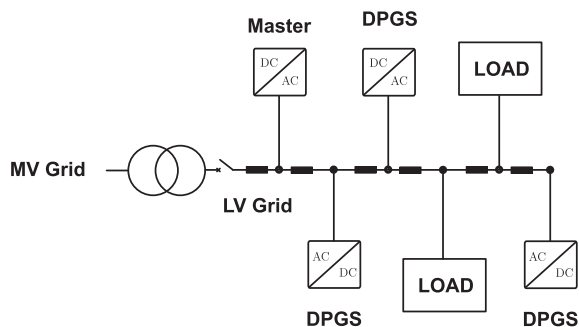


Fig. 1: Fully-decentralized micro-grid integration of DPGS.

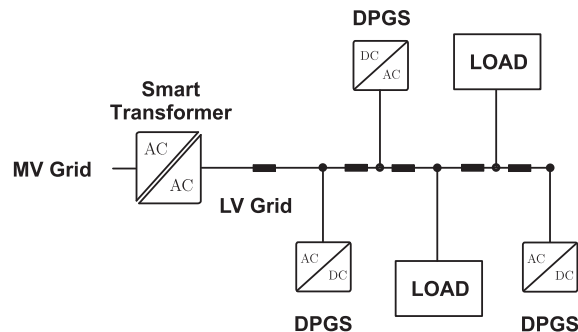


Fig. 2: Semi-decentralized ST-based integration of DPGS.

energy supply. How to optimally control this battery is a research topic [9], [10]. On the other hand, in a Smart Transformer grid the storage is absent or limited.

Several means of synchronization for parallel operation of VSCs were proposed. In [11] each VSC is controlled by a dedicated current loop. The total load current is measured and a separate synchronization and control units generate current set-points for each converter. In [12] each inverter is controlled by three nested feedback loops. The innermost current loop is used to control the output current. Its reference is generated by a voltage controller which ensures that all the inverters output the same voltage. The problem resides in the fact that small discrepancies in the output impedances can generate large differences in the output current of each VSC. For this reason, an additional outer current loop corrects the voltage reference to ensure a balanced current sharing among the VSCs. A similar approach was exploited in [13], while in [14] a supervising controller generates a common analog reference signal for all the parallel converters to attain power sharing and to limit the circulating currents among converters. The above proposals need communication among the different power stages, in order to share and dispatch the various current and voltage set-points.

In [15] the authors propose a Master-Slave approach. A master converter is controlled by an inner current loop and an outer voltage loop that fixes the load voltage. The slave converters implement only the inner current loop. The current sharing between the modules is ensured by the fact that each converter measures the total load current. The slave converters generate the current set point by dividing the total load current by the number of nodes. This architecture operates without communication between the stages, but each converter must measure the load current and needs information about the system topology.

In literature several applications of the droop control, normally used for synchronous generators, are reported for the parallel operation multiple inverters without communication [16], [17]. In [18], the hierarchical control of a decentralized micro grid is analyzed. The power sharing is realized via droop control, while a secondary control acts on the voltage and frequency reference of the droop control to maintain the correct micro-grid operations. A tertiary control is employed to regulate the power flow between the micro-grid and the mains.

It is important to note that, although in the future high-speed communication between the power converters will probably be available, the solution described in this paper could be employed in the transition time, when existing electronic equipment is still connected to the grid and must be integrated in a more flexible grid scenario.

III. THE SMART TRANSFORMER CONCEPT

The Smart Transformer is a three-stage power electronics transformer [19] that adapts the voltage between the MV to the LV grid and provides new services to the distribution grid. Although several topology solutions can be studied for each stage, the control strategies do not differ substantially. The LV side controls symmetrical voltage waveforms with an amplitude and frequency fixed to the reference values independently from the load. The amplitude and shape of the current waveform is determined solely by the load. The DC/DC converter performs two tasks: transforms the voltage from MV to LV and controls the voltage value of the LV DC link, thus keeping the balance between input and output active power. The MV side keeps the MV DC link voltage fixed to the nominal value, exchanging the needed power with the MV grid. The control strategy of the ST is shown in Fig. 3.

The MV converter is controlled with an outer DC voltage loop and an inner AC current loop. The outer loop keeps the DC link voltage to the nominal value, setting the AC active current reference. The inner loop controls the active and reactive currents. The reactive current loop receives the reference value from an external reference to providing required ancillary services to the DSO. The DC/DC regulates the power flow between the two DC stages. The DC/DC controller is composed of a loop that controls the power flow in the LV side in order to keep the LV DC link voltage constant to the nominal value. The reference power is

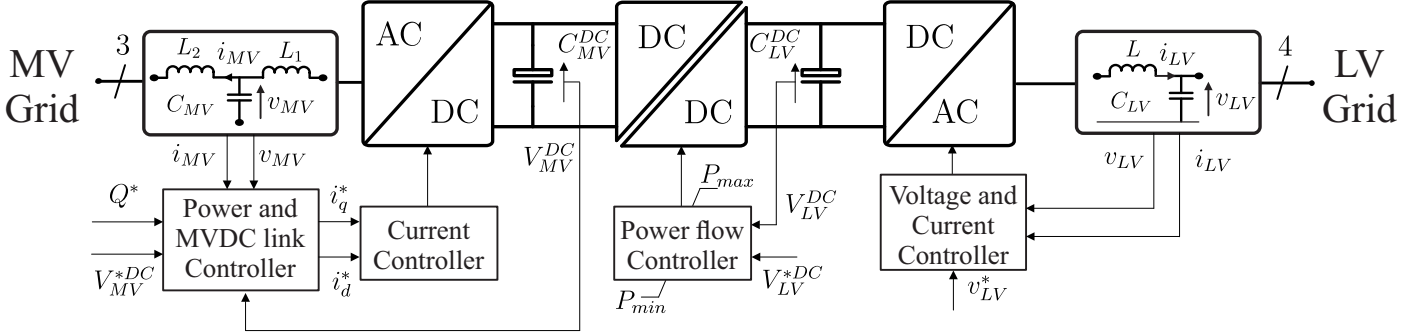


Fig. 3: Smart Transformer control scheme.

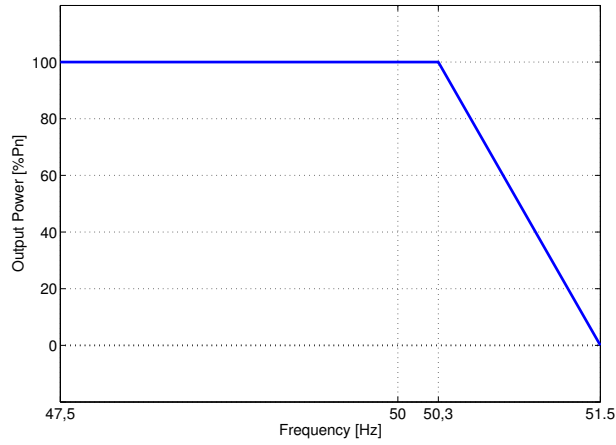


Fig. 4: Derating curve of a grid-connected inverter as a function of the grid frequency.

limited between the P_{max} , determined by the ST sizing, and P_{min} . The LV converter is controlled by means of a voltage and a current control loops, where the AC voltage waveform is kept sinusoidal with a constant amplitude and a frequency dependent on the frequency-based controller.

IV. FREQUENCY-BASED POWER LIMIT

The increasing adoption of renewable energy conversion systems into the LV distribution grid is causing problems with the stability of the grid itself. There have been several cases where the power produced by grid-connected inverters was above the local consumption. In these conditions a reverse power flow occurs in the MV/LV substation with a corresponding increase of the grid voltage amplitude and frequency [20]–[22].

For this reason, recent regulations specify a linear derating characteristic of the power supplied by the converters to the grid as the grid frequency increases. In particular, considering the Italian CEI 0 – 21 [3], at the maximum operating frequency of 51.5 Hz, the grid-connected equipment must inject no active power into the grid (Fig. 4).

In the chosen micro-grid topology, the master inverter generates the grid voltage waveform whereas the grid-connected converters inject current with an almost unitary power factor. A simple H-bridge can be considered for a phase of the master converter without losing generality. If the DC/DC stage of the master converter is programmed to prevent the reverse power flow, an excess of power produced by the grid will cause an increase of the DC Link.

Therefore, an overload condition can be detected by monitoring the DC link voltage. Upon the detection of the overload, the DC/AC inverter increases the frequency of the output voltage, thus reducing the power injected by the grid-connected converters by exploiting their derating curves. Fig. 5 shows the block diagram of the proposed solution.

The master selects the output frequency by following the overload curve, in which a linear variation of the frequency corresponds to an increase of the DC link voltage. The grid-connected converter detects the frequency variation by means of a Phase Locked Loop (PLL) and changes its output power according to the characteristic in Fig 4.

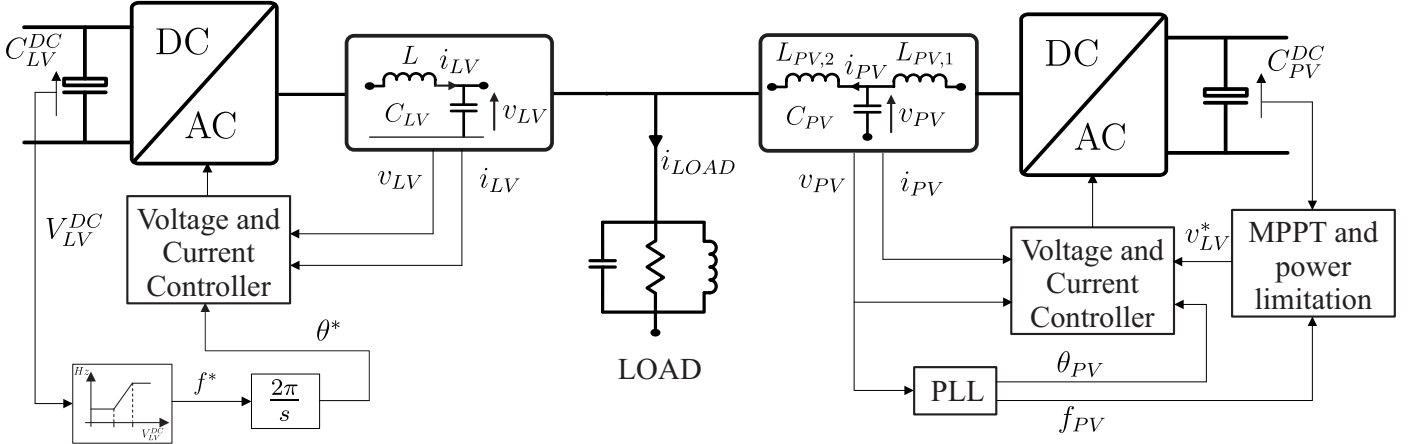


Fig. 5: Block scheme of the control system with the DPGS and master converter.

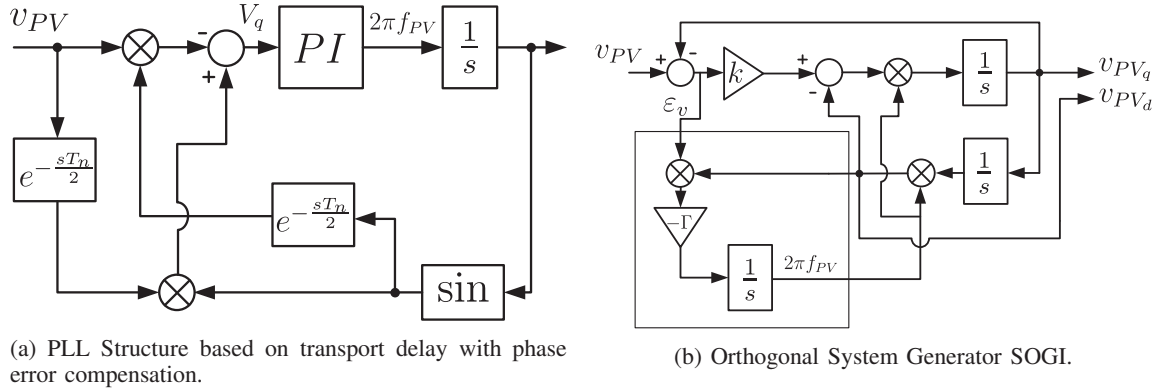


Fig. 6: Structure of the PLLs

V. STABILITY ANALYSIS

In order to analyze the controller requirements for this master-slave application, a simplified model derived from control scheme in Fig. 5 was realized to study the system's dynamics. Fig. 7 shows the block scheme. Multiple converters can be considered, however, for a matter of simplicity, the system considered a single inverter, the one with the slowest dynamic. The analysis will be conducted with only two inverters without losing in generality, because the slowest inverter has the biggest impact on the stability. V_{LV}^{DC0} indicates the threshold value of the ST DC link voltage at which the variation of the frequency begins; K_f is the slope of the frequency variation, whereas f_0 is the nominal frequency of the system, i.e. 50 Hz. The master converter compares the DC voltage measurement V_{LV}^{DC} with the reference V_{LV}^{DC0} . If this difference exceeds a certain threshold (e.g. 10 V) the frequency is increased accordingly in order to interact with the DPGS and reduce their power output. The slope in the frequency change is decided by the gain K_f , that should be designed to output the maximum frequency at the maximum safe value of V_{LV}^{DC} .

The PLL of the DPGS detects the change of frequency according to the coefficients of its Proportional-Integral (PI) regulator. Several PLLs can be implemented, and the topologies considered in this work are reported below. Fig. 6a shows the transport delay PLL with phase error compensation. In fact, the transport delay of T_n works only if T_n is a quarter of the nominal period. Employing the same delay for the calculus of the cosine of the estimated angle allows obtaining zero steady state error in a wide frequency range. This solves the drawback of the traditional transport delay PLL. Fig. 6b shows the Orthogonal System Generator - SOGI. The Frequency Locked Loop (FLL) detects the input signal's frequency and adapts the filter's resonance. The parameter k selects the bandwidth of the filter, and the parameter Γ tunes the bandwidth of the FLL.

Regardless the PLL structure chosen, a small signal approach has been pursued, so that the input of the PLL PI regulator is the phase displacement between the two sinusoidal signals (grid and reference). Upon the detection of the frequency, the

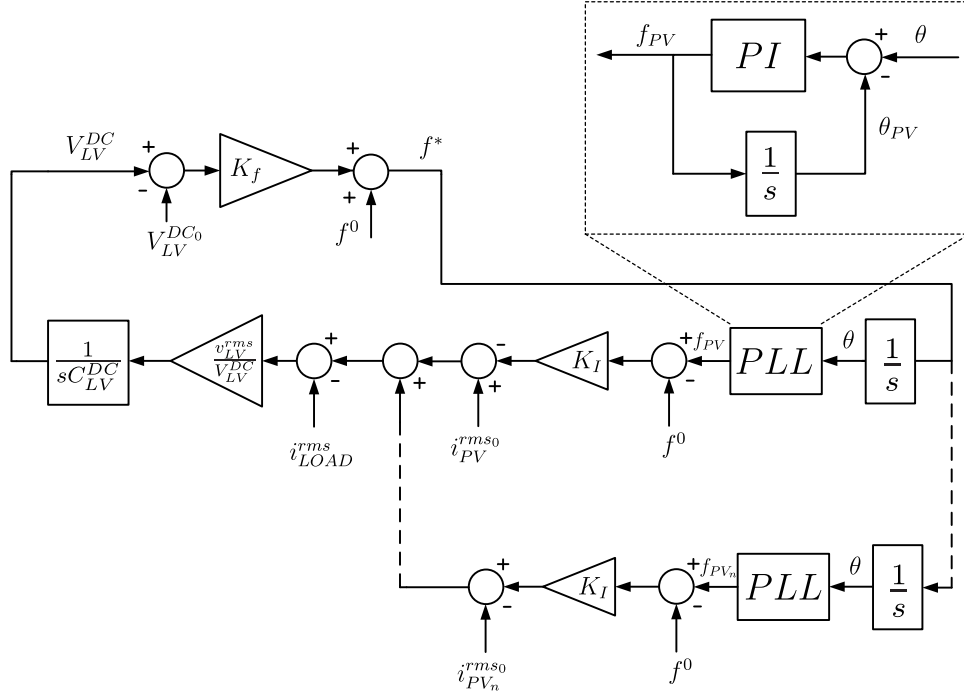


Fig. 7: Simplified block diagram for the stability analysis of the system in Fig. 5.

grid-connected inverter changes its output current following the derating curve, with parameters i_{PV}^{rms0} and slope K_I (Fig. 7). K_I originates from the derating curve, and represents the nominal current over the maximum frequency variation. The current flowing into the DC link of the master converter is the grid-connected current minus the load current with a scale factor equal to the ratio between the V_{LV}^{DC} and the RMS value of v_{LV}^{rms} .

The stability of the system can be addressed considering the feedback system of Fig. 7, where the constants of the PI regulator of the PLL (tuned with 1 Hz bandwidth) are multiplied by a gain k .

The characteristic equations of the system can be written as in (1), therefore the equation used to evaluate the root locus (Fig. 8) is given in (2).

$$A(s) = \frac{K_f K_I v_{LV}^{rms}}{s^2 V_{LV}^{DC} C_{LV}^{DC}} \quad (1)$$

$$1 + A(s) \left[\frac{ksPI(s)}{s + kPI(s)} \right] = 0 \quad (2)$$

A first order Pade approximation for a 10 ms delay was inserted in the loop to account for the low pass filtering usually applied at the output of the PLL. The parameters refer to the derating curve of a 4 kW inverter with $V_{AC} = 220V_{RMS}$. As can be seen, a narrow bandwidth of the PLL (small gain) leads to poles with positive real parts, the critical point is found to be for $K = 1.7$, corresponding to a 3dB bandwidth of 2.5 Hz.

As can be seen from eqn. (1), the constant $\frac{K_f K_I}{C_{LV}^{DC}}$ represents the intrinsic gain of the system that has the PLL frequency as an input and the master converter's angle as an output. The numerator is related to the nominal power of the grid-connected converters and to how fast the frequency is changed in response to a DC link increase. The denominator is related to the temporary storage capability of the master converter. In fact, a bigger DC capacitor tends to stabilize the system, which can work even with slower PLL. The same effect can be achieved by reducing the power of the grid connected converters K_I or reducing the slope of the droop characteristic K_f , allowing bigger voltage swings.

VI. SIMULATION AND EXPERIMENTAL RESULTS

The proposed strategy was simulated using the MATLAB/Simulink environment with the aid of the PLECS toolbox. The control scheme of Fig. 5 was implemented, and Fig. 9(a) shows the power circuit considered for the test. The parameters are listed in TABLE I. The DC/DC converter is modeled as a constant DC source V_{src} with a series diode, that represents a valid

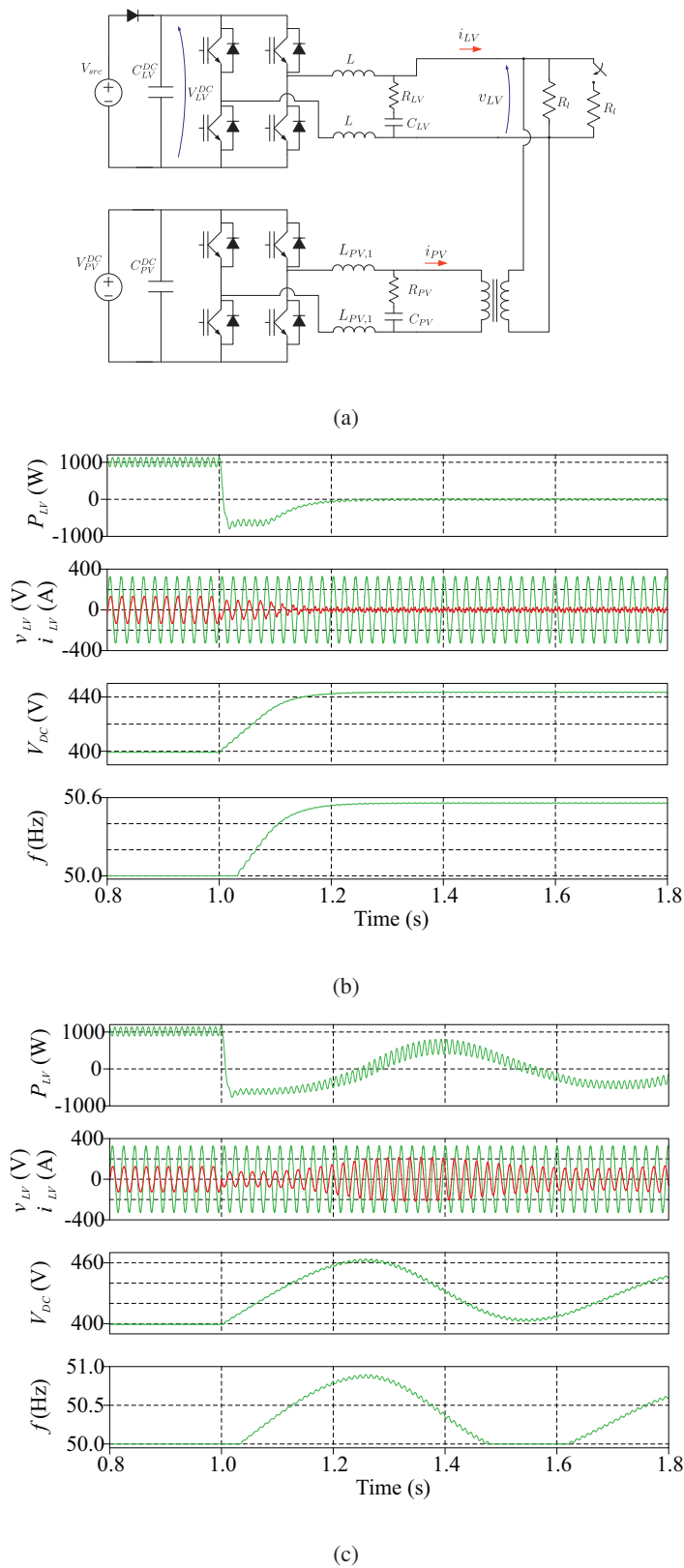
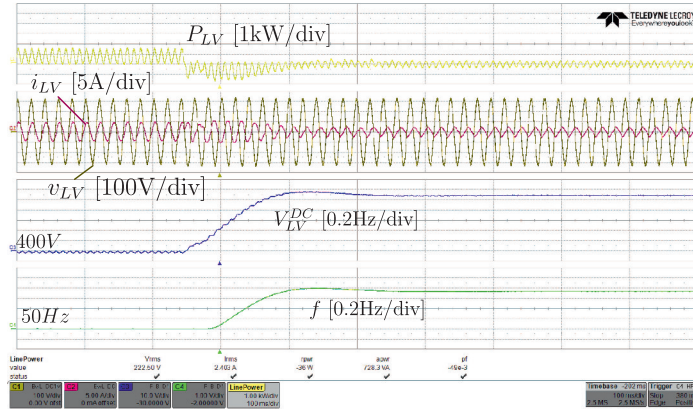
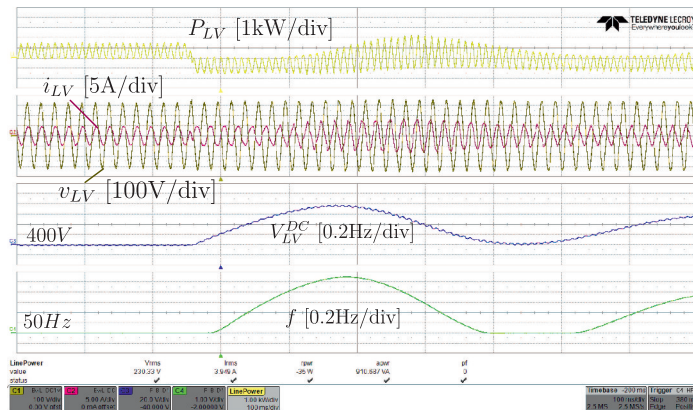


Fig. 9: Simulation results: (a) System under investigation, representing the master converter, a DPVS and a local variable load, (b) system performance (P_{LV} , v_{LV} (green, 200 V/div) and i_{LV} (red, 10 A/div), V_{DC} , and f , from top to bottom) with fast PLL, and (c) with slow PLL.



(a)



(b)

Fig. 10: Experimental waveforms of the overload start transient. (a) PLL tuned with settling time 0.1 s (bandwidth 14 Hz), (b) PLL tuned with settling time 2.5 s (bandwidth 1 Hz).

one shown in Fig. 5 and the parameters are the same used in the simulations.

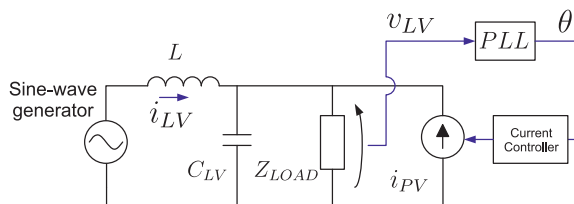
Fig. 10 shows the overload transients in the same conditions of Fig. 9. The results are in agreement with the simulation results, particularly for the transient duration. Small differences in the voltage and frequency level are due to the non-ideality of the transformer (the voltage rises at the point of connection due to the high current injection) that also causes a distorted magnetizing current to appear in I_{LV} .

VII. DISCUSSION ON THE RATED POWER OF THE MASTER CONVERTER

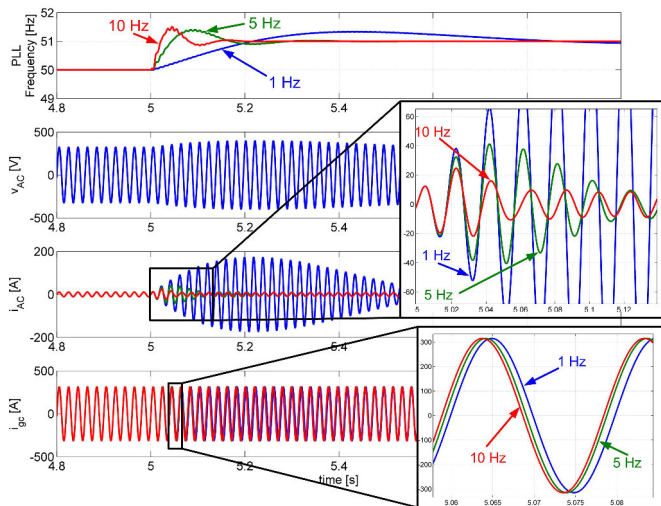
The micro-grid is regulated by only a voltage controlled inverter. For this reason it is worth investigating if the master can still control the frequency when the total power of the current-controlled inverters exceeds its rated power. In order to investigate this matter, the circuit represented by the block scheme of Fig. 11a is analyzed. The master is modeled by an AC source, while the grid-connected converters are modeled as a current-controlled AC source, whose reference angle is given by the same PLL structure of the previous simulations.

The goal of this test is to assess which is the current that the master converter must supply during the transient after a frequency step change.

The local impedance is modeled by resonant load at the nominal frequency, and a step variation of the frequency is realized, so that the master current could be monitored. From extensive simulations, it was shown that the behavior is strictly dependent on the dynamic of the PLL employed by the grid-connected converter. In fact, during a frequency change, the master absorbs active and reactive power, thus shifting the frequency of all the other converter. During the time where the frequencies are out-of sync, the current absorbed by the master converter can present a great amplitude. Instead, if the PLL bandwidth is selected sufficiently high, a small overcurrent is present.



(a) Simplified schematic for the analysis of current requirements.



(b) Effect of different PLL bandwidth on the current rating of the master converter.

Fig. 11: Frequency step change with different PLL bandwidths.

This effect is shown in Fig. 11b, where the effect of the PLL bandwidth on the output of the master's current, i_{LV} is clearly visible. The tuning of the three different PLL was realized with a pole-zero placement, and in each case the phase margin of the control was $\frac{\pi}{4}$. The PLL is realized in the synchronous reference frame and an adaptive transport delay is used for the quadrature system generation. This structure does not allow to achieve high values for the bandwidth. The master converter's rated current is supposed to be 32 A. A grid-connected converter is injecting 320 A (equivalent to 10 grid-connected converters of the same rating of the master one) of active current on a resonant load of 1Ω with a quality factor $Q = 0.3$. At the time $t = 5s$ the master realizes a frequency step from 50 Hz to 51 Hz, where in steady-state conditions the master has an output current of peak amplitude 20 A. If the bandwidth is 1 Hz, the master has to absorb a great share of the grid-connected current during the frequency step, and this performance would be unacceptable for an actual system, as that transient would damage the semiconductor. If the PLL bandwidth is 5 Hz, a small overcurrent (twice the steady-state value) occurs for 100 ms. As a matter of fact this behavior could be already acceptable, as such a transient is unlikely to damage the devices. Instead, if the bandwidth of the PLL is 10 Hz or above, there is almost no overcurrent. Similar results were obtained with a SOGI PLL structure [23], suggesting that the controllability of the system does not depend on the PLL structure but only on its bandwidth.

This behavior can be explained by the fact that the micro-grid described in this paper is different from a droop-controlled micro-grid, where a change in the frequency by a single generator can happen only if this generator rated power is greater than the total power of the other generators. Otherwise, a generator with a little output power cannot cause a marked shift in the frequency. Grid-connected inverters are current controlled, and it is mandatory from international regulations that they disconnect from the grid in the case of island operations. Several anti-islanding algorithms were reported in literature, but the basic fact is that grid-connected inverters are very sensitive to frequency changes. For this reason, if the bandwidth of the PLL is sufficiently high, it is possible for the master to control the frequency of a whole micro-grid, even if the power rating is inferior to the total power of the current-controlled inverters.

Another complication may arise from the active anti-islanding methods that can be employed by commercial inverters in order to reduce the risk of undetected islanding. These methods imply the introduction of determined amounts of disturbance into

the grid (reactive power, zero crossing distortion, phase imbalances) that are normally compensated by the distribution grid. However, in the case of island operations, the master needs to compensate also for this additional power.

VIII. SCENARIO OF APPLICATION OF THE PROPOSED SOLUTION

The proposed frequency control can be adopted in an ST-fed distribution grid with the total power of the micro-grid exceeding the one of the ST under the assumption that the grid-connected inverters PLL has sufficient bandwidth (e.g. 5 Hz) for detecting the frequency changes. In such case it was shown that the frequency can be properly controlled by a VSC that implements a variation of the grid frequency.

Nevertheless, the solution proposed presents also drawbacks. The differences among grid-connected inverters from different manufacturers regarding current control and PLL may deteriorate the frequency control, increasing the current requirements of the master inverter. A simulation was run where multiple grid-connected inverters with different PLL (considering SOGI, Fig. 6b, fixed transport delay, transport delay with phase error compensation, Fig. 6a) structures.

In this case, the bandwidth of the fixed delay PLL must be kept lower than the other structures in order to prevent unacceptable frequency oscillations. As can be seen from Fig. 12, at time $t=5$ s, when the frequency changes from 50 Hz to 51 Hz, the ST must supply a considerable amount of current, rendering impractical the micro-grid realization.

Moreover, the considerations stated above are valid only in case of grid-connected converters featuring a current loop control, such as commercial PV inverters. In term of generality, if droop-controlled generators were connected to the micro-grid, the frequency control mechanism would require that the ST had a power rating similar to the total micro-grid power.

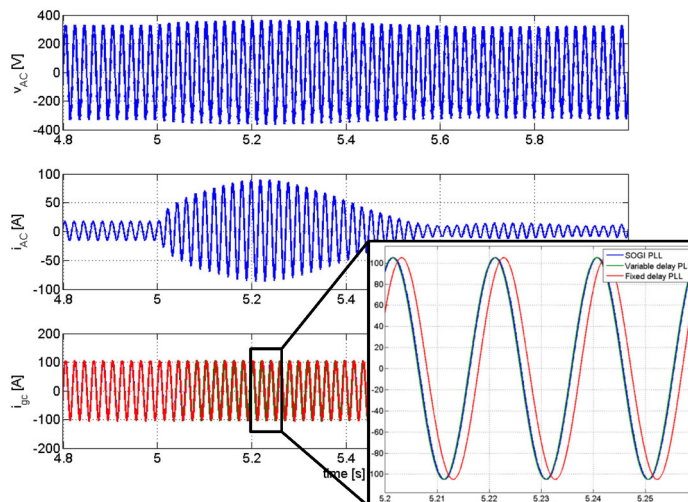


Fig. 12: Simulation results of the master converter with multiple grid-connected converters with different PLLs.

As this paper proposes a master/slave approach, this grid suffers from single point failure. While for fully-decentralized micro-grids this constitutes a serious drawback, in the case of a malfunction of the transformer in a LV distribution, usually the LV grid should be de-energized, and the anti-islanding mechanisms of the DPGS should disconnect all the grid-connected equipment. The case of multiple ST connected to the same LV grid and the fault tolerant operation is reserved for future investigation.

IX. CONCLUSION

In this work a frequency-based master/slave synchronization method is used to implement a LV micro-grid. The proposed mechanism exploits the features of the newest grid-connected converters, which incorporate frequency-depending power derating characteristics.

Imitating this mechanism of the mains a master VSC generates the grid voltage, and several grid-connected inverters transfer active power to the micro-grid. The master increases the output frequency in case of reverse power flow, forcing the grid-connected converters to reduce their output power, thus stabilizing the system.

Experiments highlight that the effectiveness of the proposed solution depends on the ability of the grid-connected inverters to rapidly detect a change of the grid frequency.

Finally, some considerations are given regarding the actual feasibility of this system with commercially available power converters. In fact, if multiple grid-connected converters are present, the total power may exceed the power of the master

converter that is realizing the frequency control. Extensive simulations were performed and the results show that the feasibility of the proposed solutions relies on the PLL bandwidth of the grid-connected inverters.

This scenario is particularly interesting because it does not require to deploy several inverters with custom firmware and it can be applied as well as in a ST-fed distribution grid. Considering that the ST has enough power to modify the frequency regardless the control systems of the DPGSSs, this methodology can be used also with older equipment that do not feature derating characteristics.

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