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# Analysis of the Robustness of Transformerless PV Inverter Topologies to the Choice of Power Devices

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*Abstract*—Transformerless topologies are employed in single-phase PV inverter converters due to their small size and low weight. Avoiding the grid side transformer requires the modulation technique and the basis topology to be accordingly changed in order to mitigate dc current components in the grid side and the leakage current to ground. This paper carries out a sensitivity analysis of selected transformerless topologies. This analysis investigates the impact of parameter variations depending on the choice of the employed semiconductor devices and detects the device for each topology, which affects the most the overall efficiency as well as the topology that is affected the most by parameter variations with respect to the efficiency, leakage current and grid-side dc current component. It is shown that, based on the proposed statistical analysis procedure, the impact of parameter variability can be analyzed with reduced computational burden. An approach for the simplification of the comparison of the analyzed topologies is presented. As a result, relevant information for engineers selecting the most suitable power devices for the implementation of a certain transformerless topology is provided. The proposed analysis also allows to assess the robustness of the topologies' performance to the choice of different components when this selections is driven by other factors, like cost and supply chain management.

*Index Terms*—Inverters, Photovoltaic power systems, Sensitivity.

## I. INTRODUCTION

As a result of the last decade's researching activity on PV inverters, a number of transformerless (TL) topologies for $1\phi$ PV inverters has been developed in order to reduce the size and weight of the commercial equipments while increasing the overall efficiency. However, these topologies have some drawbacks, such as the injection of dc current components at the grid side and a higher number of power devices in comparison to the basic transformer-based topology (H4). The injection of dc currents at the grid side can be avoided by the employment of appropriate control techniques while a higher number of power devices is required in order to reduce leakage currents flowing through the parasitic capacitor of the PV generator by decoupling the grid during the freewheeling

period of the inverter current. TL $1\phi$ PV inverters are commercially available and manufacturers have developed their own inverter series based on transformerless topologies (H5, HERIC, HB-NPC and H6, respectively) [1]. A review of the state-of-the-art in single phase TL topologies is carried out in [2], where a new family of HERIC-based clamping inverters with high efficiency ($\eta_{EU} = 97.0$ %) and low leakage current is presented.

The efficiency, leakage and dc currents, inverter reliability and standards/grid codes accomplishment are key issues to be managed for integration of TL topologies in commercial PV systems. The efficiency of these topologies can be increased by employing SiC devices and/or soft switching, e.g. [3] demonstrates that the efficiency of H6-I topology, at nominal power, can be improved by applying zero-current soft-switching (more than 2 %) and, as presented in [4], through zero-voltage soft-switching (more than 2.5 %). A topology with two power MOSFETS is proposed in [5] to reduce the leakage current. The developed prototype (200 $W$) results in peak leakage currents below 2.5 $mA$ and 96 % efficiencies. The authors of [6] propose a PWM technique for a TL PV cascaded multi-level inverter, by which a minimization of leakage current is achieved compared to the conventional SPWM method with less number of carrier waves and without the need for additional switches. Regarding the leakage current in $3\phi$ TL PV systems, in [7] a modulation strategy for eliminating the leakage current of a four-leg inverter by keeping the common-mode voltage constant is presented. The reduction of the leakage current in a H7 $3\phi$ inverter is also the target in [8]. Moreover, the PV inverter lifetime can be increased by means of a better balance of the power losses in TL topologies [9] and reducing the leakage current without increasing the number of power devices [10]. In [11] a novel 2-D analytical model for the parasitic capacitance of PV systems is presented, allowing for a more precise evaluation of leakage current during the design stage. The low-voltage ride-through (LVRT) capability of $1\phi$ full-bridge and HERIC topologies is evaluated in [12], where it is shown that HERIC is the least suitable topology for PV systems with LVRT capabilities.

Performance comparisons of TL topologies based on the aforementioned parameters and considerations have been carried out in literature. H5, HERIC, NPC and FB-ZVR topologies are analyzed and evaluated experimentally in [13]. The efficiencies of Half-bridge with unipolar switching, HERIC and HBZVR are experimentally compared in [14] at power levels from 500 $W$ to 2800 $W$. The results show that HERIC allows a higher efficiency (95.94 % at 2.8 $kW$). [15] compares

the performance of H5, HERIC, H6, FB-ZVR, HB-NPC and Araujo inverter by means of simulation tests in terms of the European Efficiency, output current THD and leakage current. The HERIC topology reaches a $\eta_{EU} = 98.27$ % while the lowest THD corresponds to H6 and no leakage current is obtained in case of NPC topologies. The behavior of H5, HERIC and H6 topologies is analyzed and compared in terms of power losses in [16], where the proposed H6 topology shows a lower efficiency than HERIC but higher than H5 (the measured European Efficiencies in $1 \ kW$ prototypes for H5, HERIC and H6 are 96.78 %, 97 % and 97.09 %, respectively) and the minimum leakage current corresponds to H5 ($6 \ mA$). Neutral Point Clamped converters are analyzed in [17], where it is shown that the European Efficiency reaches 96.4 %, 96.9 %, and 97.2 % for FB-DCBP, oH5 and PN-NPC topologies, respectively. NPC $1\phi$ PV inverters are also analyzed in [18], where a generalized design principle for NPC circuits is discussed. In [19] the losses of a $1 \ kW$ prototype are compared by means of simulation tests for H5, oH5, H6, HERIC, HBZVR and HBZVR-D and the leakage currents are measured experimentally. The obtained results show that HERIC topology results in a higher efficiency (96.05 %) and the lowest leakage current corresponds to HBZVR-D ($42.7 \ mA$). A $1 \ kW$ prototype is also employed in [20] for comparison purposes of three variants of H6 topology. The results show that leakage currents are in the range $19.6 - 24.5$ $mA_{rms}$ and the range of obtained European Efficiencies is $97.22 - 97.39$ %. In [21] the same authors propose a TL PV topology based on superjunction MOSFETs switches and SiC diodes, which achieves low leakage current and low output distortion, resulting in a maximum experimental efficiency of 98.5 %. An equivalent high-frequency circuit for evaluation of leakage currents in H4, H5, H6, HERIC and Paralleled-Buck is presented and evaluated experimentally in [22]. The obtained results in a $3 \ kW$ setup show that H6 results in the lowest leakage current ($29.4 \ mA$) and the highest efficiency corresponds to paralleled-buck topology ($\eta_{EU} = 97.8$ %) follwed by HERIC ($\eta_{EU} = 97.5$ %). Similar analyses have been carried out in [23] and [24] and, in all cases, the obtained results, both in simulation and experimentally, are valid for the specifically considered power devices selected for simulation purposes or the implementation of prototypes. The variability of IGBT and diode parameters due to the employed technology and the characteristics of the manufacturing process is considered in [25], where a statistical approach for performance evaluation of transformer-based H4 topology is proposed. In [26] the impact of parameter variability on TL PV inverter topologies is first discussed.

The performance results found in literature are normally obtained in optimized conditions, when the researchers chose the right semiconductors to maximize a certain performance index, e.g., the converter efficiency. Researchers and industrial engineers have been looking carefully at each commutation, considering which devices are switching at high frequency and which diodes are forcefully switched off (with reverse recovery losses), as an example. As a matter of fact, different transformerless topologies have their peculiarities. The H6 avoids the reverse conduction in devices on the DC side. This

means that their body diode characteristics do not impact on the overall efficiency, and, therefore, the inverters designer should take a closer look on the parasitic capacitance, since this capacitance is in the common-mode equivalent circuit and should be minimized [27]. The authors of the first H6 paper [28] used different IGBTs for devices of the full bridge and for the DC devices. Other researchers also used MOSFETs [29]. In the H5 topology, since there are devices switching at line frequency, they can be optimized for conduction and may be allowed to show worse performance regarding switching losses.

This approach is, however, not sufficient for a general comparison between the different architectures. This manuscript aims at filling this gap, proposing a methodology to evaluate the robustness of the TL PV inverters. In fact, two cases can be considered: topology optimization or supply chain management optimization. The proposed approach can point out which device in a topology is the most responsible for certain performance index, suggesting the designer where to act to improve the performance. In the case the semiconductors' choice depends on factors other than the performance, and the same devices are always used across a broad range of products, the analysis allows to individuate which topology is the most robust to the semiconductors' parameter uncertainty.

This manuscript proposes the statistical analysis of four TL topologies (H5, H6, HB-NPC and HERIC) in order to determine the switch whose characteristics affect the most the PV inverter efficiency, dc-component of the grid-side current and leakage current, respectively. The proposed analysis provides the PV inverter manufacturers a tool to improve the performance of their products by focusing on the power devices which reduce the overall performance. It is worth mentioning, that the sensitivity is evaluated not with respect to parameter variations within a certain device series of one manufacturer, since theses parameters are very robust, but how much a topology is sensible to the choice of devices available in the market.

The manuscript is organized as follows: the evaluated topologies are described for ideal and theoretical conditions in Section II, the procedure to carry out the sensitivity analysis with respect to parameter variability is given in Section III, sections IV and V provide the obtained simulation results and the conclusions, respectively.

## II. EVALUATED TL TOPOLOGIES

The $1\phi$ TL topologies analyzed in this work are shown in Fig. 1, where the employed subsystem for generation of the gate signals is also depicted. The H5 topology (Fig. 1 (a)) consists of a full-bridge with one additional switch in the dc-link which enables the decoupling of the PV inverter from the grid during the freewheeling period of the current [15]. The current contains a switching ripple which is equal to the switching frequency resulting in high filtering effort. However, due to the fact that the voltage across the filter is unipolar, low core losses can be expected. Another advantage of the H5 topology can be found in the low leakage current. This is because the voltage to ground $V_{PE}$ is sinusoidal with grid frequency component.
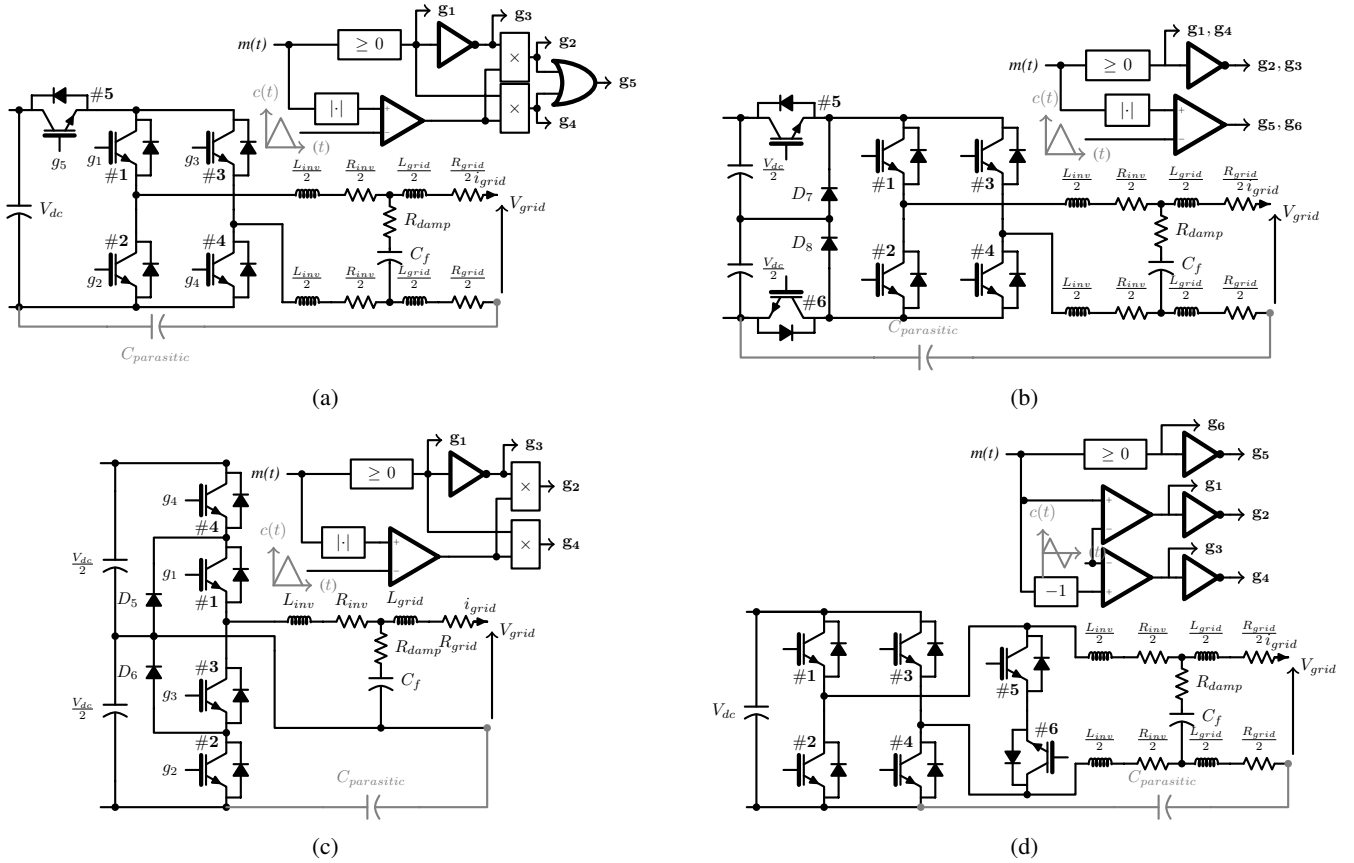
Fig. 1: Transformerless topologies and the applied gate signals considered in the present analysis: (a) H5 topology, (b) H6 topology, (c) HB-NPC topology, (d) HERIC topology.

The H6 topology, also known as Full-Bridge Inverter with DC Bypass (FB-DCBP), is shown in Fig. 1 (b). This topology consists of a full-bridge with two extra switches, #5 and #6, in the dc-link and two clamping diodes ($D_7$ and $D_8$) which are connected at the midpoint of the dc-link capacitance [1]. As in the case of H5, here again the voltage across the output filter is unipolar and $V_{PE}$ has only a grid frequency component, resulting in low core losses and a low leakage current, respectively.

In contrast to H5 and H6 the HB-NPC topology (*Half Bridge - Neutral Point Clamped*) is not based on the full bridge concept. As it can be seen in Fig. 1 (c) the HB-NPC is a half-bridge consisting of the four switches #1 to #4 and the two clamping diodes $D_5$ and $D_6$ which are connected to the neutral grid terminal at the midpoint of the dc-link capacitance [15]. The diodes limit the voltage which is applied to the switches to half of the PV input voltage. This means that the NPC requires twice the PV input voltage in comparison to full-bridge topologies [1]. In case of the NPC the current also contains a switching ripple which is equal to the switching frequency resulting in high filtering effort, but here again the core losses are low due to an unipolar voltage across the filter. One remarkable advantage of this topology is that, in theory, $V_{PE}$ is constantly equal to $-\frac{V_{in}}{2}$ which means that no leakage current is obtained [15].

Based on a full-bridge the HERIC topology (*Highly Efficient*

*and Reliable Inverter Concept*) contains an additional bi-directional switch on the AC side for decoupling the PV inverter from the grid during the freewheeling periods [15]. The topology is shown in Fig. 1 (d). As shown, the bidirectional switch is built up of two switches plus their anti-parallel diodes (#5 and #6, respectively). Similar to the H5 topology high filtering effort is also needed for the HERIC topology due to the fact that the current contains a switching ripple equal to the switching frequency. Nevertheless, low core losses are obtained by the unipolar voltage across the filter and a low leakage current is achieved due to a sinusoidal $V_{PE}$.

## III. SENSITIVITY ANALYSIS OF TL TOPOLOGIES

### A. Sensitivity assessment procedure

The proposed analysis procedure for the evaluation of the inverter performance considering the characteristics of the available commercial power devices and their impact on the overall performance depending on their allocation within the topology is depicted in Fig. 2. It is based on Monte Carlo (MC) simulations with Latin Hypercube Sampling (LHS), which allows the number of required trials to be reduced.

MC simulations can be applied to the statistical analysis of power converters' characteristics and performance. This is the case in [30], where MC allows the lifetime of power electronic components in power converters to be estimated. In [31] a MC based method is applied to the bond wire lifetime
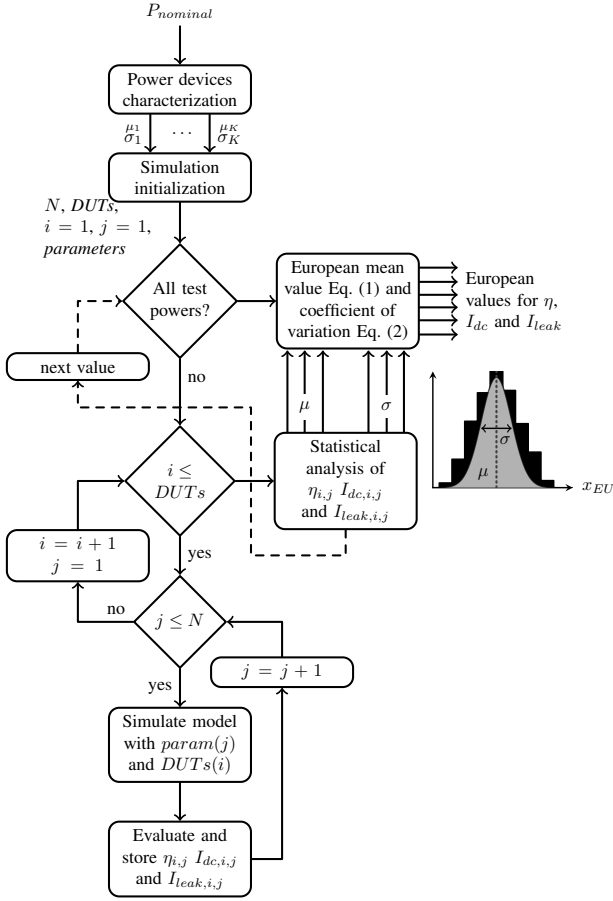


4



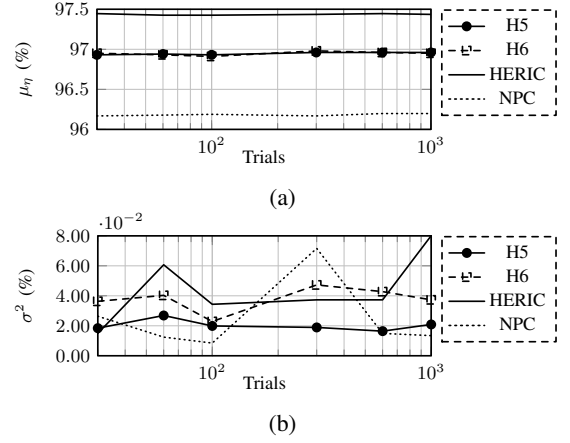Fig. 2: Flowchart of the proposed sensitivity analysis procedure.



Fig. 3: a) Mean and b) standard deviation of the efficiency at nominal power (3.3 $kW$) of the PV inverter as a function of the number of trials (30, 60, 100, 300, 600 and 1000) in case all the device parameters are changed.

TABLE I: Selected switches for the sensitivity analysis.

| Topology | Switches |
|----------|----------|
| H5 | #1, #2 and #5 |
| H6 | #1, #4, #5 and D7 |
| HB-NPC | #1, #4 and D5 |
| HERIC | #1, #4, #5 and #6 |

prediction in IGBT modules for PV inverters. The performance of differential power processing architectures in PV systems is analyzed in [32] and [33] through MC simulations. However, for a given set of samples, LHS can produce more precise estimates than random sampling based MC [34] with a reduced simulation time [35], [36]. Due to this fact, the proposed methodology is based on LHS.

In order to determine the switch which affects the most the performance of each TL topology, a set of switches for each topology has been selected and a full set of simulation tests has been carried out for each switch. The comparison of the obtained results allow the most sensitive switch to be determined considering that the employed switches are practically implemented by means of real power devices subjected to certain variations, given in the data sheets.

The first step of the proposed methodology (Fig. 2) consists of the characterization of the physical parameters of power devices for modeling purposes. These physical characteristics were analyzed in [25] for a set of commercially available IGBT power modules, resulting in the most suitable probability distribution functions (pdfs) applicable to IGBT ($R_{on}$, $\frac{L_{on}}{V \cdot I}$, $\frac{T_f}{V \cdot I}$, $\frac{T_r}{V \cdot I}$ and $\frac{V_{CE,sat}}{I}$, with $V$ and $I$ being the nominal power of the modules) and diode parameters ($R_{on}$, $\frac{I_f}{V}$, $\frac{V_f}{I_f/V}$, $\frac{dI_f}{dt}$, $I_{rrm}$, $\frac{Q_{rr}}{I_f/V}$ and $T_{rr}$). The mean ($\mu$) and the standard deviation

($\sigma$) of these $K = 12$ pdfs, evaluated at a certain power level, are then employed for initialization of MC with LHS. These best fit pdfs are applied within the maximum and minimum values for each parameter for the whole set of analyzed devices.

The simulation initialization establishes the number of required trials ($N$), the set of $N \times K$ parameters to be applied in each iteration and the devices under analysis (DUTs). The number of trials can be evaluated by running *a priori* tests with different sampling sizes and evaluating the mean and deviation of the obtained results. These tests have been applied in case of all the devices' parameters are changing, which allows the maximum number of trials to be established. The topology efficiency at the nominal power for these trials is shown in Fig. 3, where the mean and deviation measurements are plotted. As it is shown, the mean efficiency for all the analyzed topologies does not depend on the number of trials and the values of $\sigma^2$ are kept below 0.1 %. As a consequence, in order to reduce the computational burden, $N$ has been established to 30 trials.

Due to the symmetrical behavior of the topologies for both the positive and negative output voltages only half of the required power devices must be considered during the simulation initialization. Table I shows the selected switches for the sensitivity analysis. In each iteration $i$ only the parameters of the selected switch are changed using the LHS, the parameters of the other switches are kept at the mean values ($\mu_1...\mu_K$) of the employed pdfs.

The procedure finishes once all the selected devices for each topology are evaluated according to the generated parameters in the LHS.

TABLE II: Exemplary set of 6 simulations ($N = 2$, $DUTs = 3$) per power level for H5 topology.

| Switch | Case 1 | Case 2 | Case 3 | Case 4 | Case 5 | Case 6 |
|--------|--------|--------|--------|--------|--------|--------|
| #1 | Parameter Set 1 | Parameter Set 2 | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ |
| #2 | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | Parameter Set 1 | Parameter Set 2 | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ |
| #3 | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ |
| #4 | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ |
| #5 | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | $\mu_1...\mu_K$ | Parameter Set 1 | Parameter Set 2 |

*B. Result analysis*

Subsequent to the sensitivity assessment procedure described in the previous section, the effect of each switch on the topology performance is statistically analyzed for $\eta$, $I_{dc}$, and $I_{leak}$, respectively. These parameters are analyzed for different power levels, according to the European Efficiency requirements (100 %, 50 %, 30 %, 20 %, 10 % and 5 % of the nominal power - 3.3 $kW$) and employing the same controller and LCL filter values.

In order to simplify the analysis of the obtained simulation results, it is proposed to use a calculation method based on the well-known formula for the European Efficiency. Therefore, the resulting pdfs of each analyzed switch at the selected power levels are processed by applying the same weighting factors to the values at the different power levels that are employed in the formula for the European Efficiency in order to obtain one EU pdf of a certain parameter ($I_{leak}$, $I_{dc}$ and $\eta$). The EU formula is given in equation (1) where $x$ is to be replaced by $\mu_{I_{leak}}$, $\mu_{I_{dc}}$, and $\mu_\eta$ as well as for the corresponding $\sigma$ values of the analyzed switch, respectively.

$$x_{EU} = \begin{aligned} & 0.03 \cdot x_{5\%} + 0.06 \cdot x_{10\%} + 0.13 \cdot x_{20\%} \\ & +0.1 \cdot x_{30\%} + 0.48 \cdot x_{50\%} + 0.2 \cdot x_{100\%} \end{aligned} \quad (1)$$

Moreover, for each topology the "global" mean values for each parameter and the corresponding $\sigma$ values of the analyzed switches are calculated (in the following referred to as "European mean values"), so that they can be used as base values for the following analysis. Thus, a simple visualization of the obtained results by means of radar charts can be realized, allowing for a clearly arranged comparison of the parameter sensitivities of the tested switches for each topology.

In addition, in order to compare the topologies with each other, the proposal in this work is the introduction of the "European coefficient of variation" $CV_{EU}$. The EU coefficient of variation expresses the relative standard deviation since it refers the standard deviation $\sigma_{x_{EU}}$ to the mean value $\mu_{x_{EU}}$ of the corresponding parameter, as given in equation (2). Thus, the analyzed parameters of each topology can be compared not in terms of absolute values but by means of relative variabilites, showing which topology is more affected by parameter variability.

$$CV_{x,EU} = \frac{\sigma_{x_{EU}}}{\mu_{x_{EU}}} \quad (2)$$

It should be noted that this analysis is focused on the impact of variations of the physical parameters of the employed switches on the overall performance of the topologies, thereby locating the device that is most sensitive to these variations.

It is not the target to present optimal behaviors but to show a way to think of future optimizations in terms of selection of proper switching devices with respect to their locations inside the corresponding topology. Therefore, the analyzed topologies have not been optimized in order to compare them on an equivalent performance basis. In the case of the HB-NPC topology the main issue is the uneven distribution of the switching losses. This means that by optimizing the switching frequency the losses are reduced and the overall efficiency increases. It has been reported in [37] that the outer switches (here #2 and #4) are stressed more due to the switching losses than the inner switches which operate at grid frequency and that the uneven losses distribution increases with increasing switching frequency. Thus, the optimization of the switching frequency of the HB-NPC topology at fixed LCL parameters, which allows the reduction of the switching frequency in comparison to the other topologies, would lead to lower switching losses of the outer switches and, thus, to an increasing efficiency. However, the aim of this work is not comparing PV inverter topologies in terms of optimal efficiency, but investigating the impact of practical devices' characteristics on the overall inverter performance.

*C. Example of Application: Analysis of H5 topology*

In order to better clarify the procedure, an example is carried out for the H5 topology, considering the sensitivity of devices #1 , #2 and #5 as given in Table I towards the efficiency for two sets of parameters generated by the LHS procedure.

In this exemplary case, the developed tool generates for 3 devices under test (DUTs) with $N = 2$ parameter sets in total 6 simulations per power level, as shown in Table II. As stated in Section III-A, in each iteration (here referred to as Case) only the parameters of the DUT are changed, whereas the parameters of the other devices are kept at the mean values of the employed pdfs. The parameters of the DUT are generated by LHS applied to the pdfs. Each pdf is divided in equal probability regions which are randomly combined to create the set of parameters for simulation purposes. The parameters of all the devices are transferred to a Simulink/PLECS model in each case, where the detailed physical model of the device is employed. The simulation model records the DC current and voltage, the AC current and voltage as well as the leakage current. The efficiency is calculated as the ratio between AC and DC power, the DC current is calculated by averaging the output current, and the leakage current is calculated as the rms value of the saved data. In Fig. 4 exemplary simulation outputs of the grid-side voltage, grid-side current, and leakage current, respectively, are shown for devices #1 and #5 of the H5 topology at both Parameter Set 1 and Parameter Set 2, respectively. It can be noted that the leakage current shows a
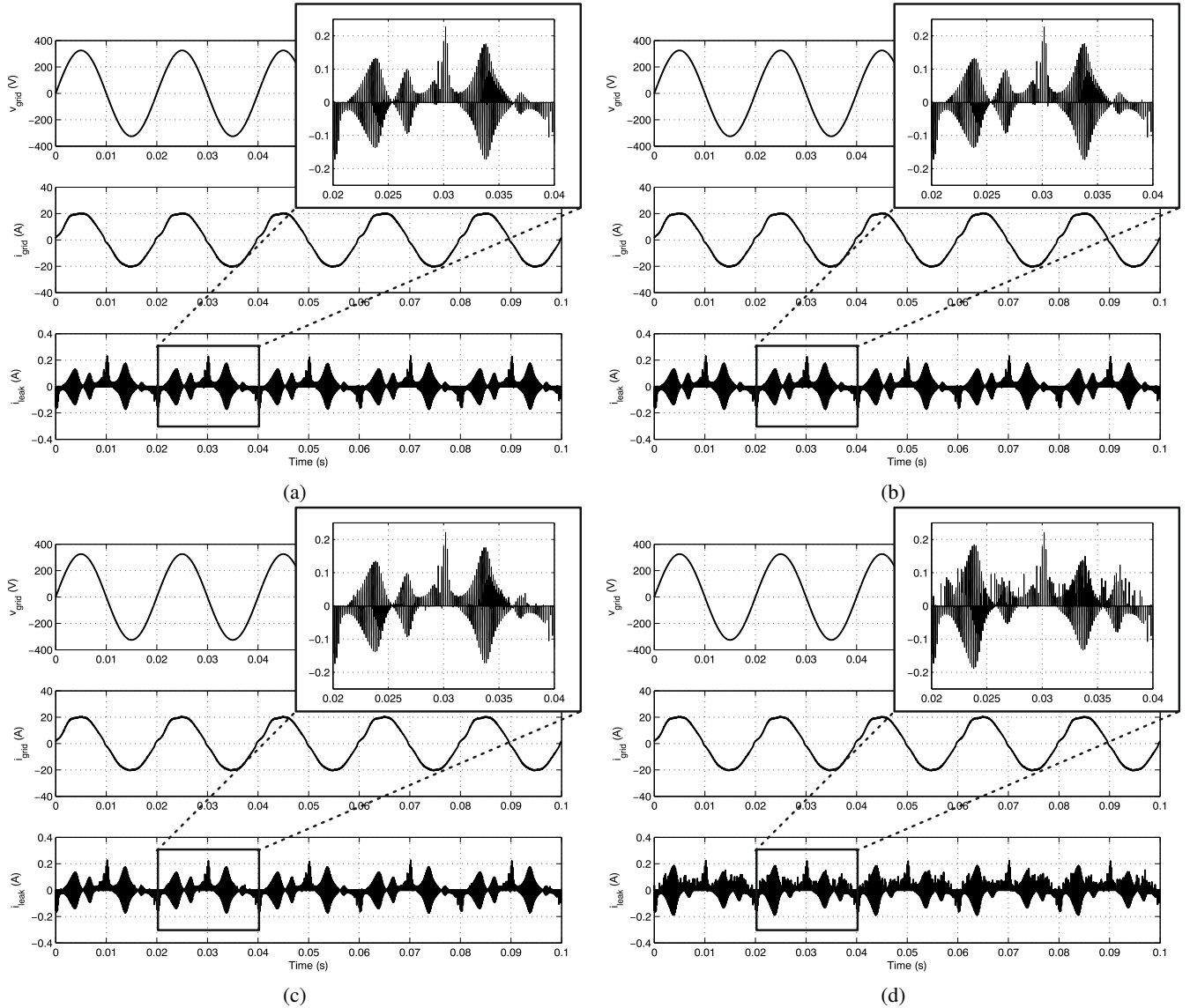
Fig. 4: Exemplary simulation outputs of grid-side voltage, grid-side current, and leakage current for #1 and #5 for Parameter Set 1 and Parameter Set 2 for H5 topology: (a) #1, Parameter Set 1, (b) #1, Parameter Set 2, (c) #5, Parameter Set 1, (d) #5, Parameter Set 2.

more sensitive behavior towards changes in parameters of #5 (Figs. 4 (c) and (d)) than in case of #1 (Figs. 4 (a) and (b)).

The procedure to obtain the results as proposed by the authors shall now be demonstrated for the given example by only considering the efficiency as shown in Table III. For the other parameters, $I_{leak}$ and $I_{dc}$, respectively, the procedure is to be repeated accordingly. As stated before, in this example, the set of 6 simulations is run for each power level. Then, for each DUT the efficiency is recorded for each $N$ simulation, resulting in this example in a set of $N = 2$ efficiencies per DUT per power level (e.g. for #1 at $P_n$: $\eta_{\mathrm{P_n},\#1,1}$ and $\eta_{\mathrm{P_n},\#1,2}$). From this set of $N$ efficiencies per DUT per power level a pdf is obtained by statistical analysis, characterized by its mean value and standard deviation, respectively (e.g. for #1 at $P_n$: $\mu_{\eta,\#1,\mathrm{P_n}}$ and $\sigma_{\eta,\#1,\mathrm{P_n}}$). This procedure is repeated for each power level, resulting in 6 pdfs for each

DUT. Subsequently, these 6 pdfs per DUT are processed by applying the EU formula as given in (1), such that one EU pdf is obtained per DUT (e.g. for #1: $\mu_{\eta_{EU,\#1}}$ and $\sigma_{\eta_{EU,\#1}}$). Finally, in order to present the results for one topology in a clearly arranged radar chart, from the mean and $\sigma$ values of the EU pdfs of the DUTs again the mean values are calculated, resulting in "European mean values", which are used as base values for the analyzed parameters (in case of $\eta$ of the H5 topology: $\mu_{EU,\eta,H5}$ and $\sigma_{EU,\eta,H5}$).

## IV. SIMULATION RESULTS

As stated before, the evaluation of the selected transformer-less topologies has been carried out considering the efficiency at each power level (100 %, 50 %, 30 %, 20 %, 10 % and 5 % of the nominal power), the European Efficiency, the dc component of the grid side current and the leakage current. The

TABLE III: Efficiencies, EU values, and European mean value for the example of application for H5 topology.

| | Case 1 (#1) | Case 2 (#1) | Case 3 (#2) | Case 4 (#2) | Case 5 (#5) | Case 6 (#5) |
|---|---|---|---|---|---|---|
| $P_n$ | $\eta_{P_n,\#1,1}$ | $\eta_{P_n,\#1,2}$ | $\eta_{P_n,\#2,1}$ | $\eta_{P_n,\#2,2}$ | $\eta_{P_n,\#5,1}$ | $\eta_{P_n,\#5,2}$ |
| | $\mu_{\eta,\#1,P_n}, \sigma_{\eta,\#1,P_n}$ | | $\mu_{\eta,\#2,P_n}, \sigma_{\eta,\#2,P_n}$ | | $\mu_{\eta,\#5,P_n}, \sigma_{\eta,\#5,P_n}$ | |
| $0.5P_n$ | $\eta_{0.5P_n,\#1,1}$ | $\eta_{0.5P_n,\#1,2}$ | $\eta_{0.5P_n,\#2,1}$ | $\eta_{0.5P_n,\#2,2}$ | $\eta_{0.5P_n,\#5,1}$ | $\eta_{0.5P_n,\#5,2}$ |
| | $\mu_{\eta,\#1,0.5P_n}, \sigma_{\eta,\#1,0.5P_n}$ | | $\mu_{\eta,\#2,0.5P_n}, \sigma_{\eta,\#2,0.5P_n}$ | | $\mu_{\eta,\#5,0.5P_n}, \sigma_{\eta,\#5,0.5P_n}$ | |
| $0.3P_n$ $0.2P_n$ $0.1P_n$ $0.05P_n$ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| EU value | $\mu_{\eta EU,\#1}, \sigma_{\eta EU,\#1,}$ | | $\mu_{\eta EU,\#2}, \sigma_{\eta EU,\#2,}$ | | $\mu_{\eta EU,\#5}, \sigma_{\eta EU,\#5,}$ | |
| European mean value | $\mu_{EU,\eta,H5}, \sigma_{EU,\eta,H5}$ | | | | | |

simulations have been carried out with MATLAB/Simulink and PLECS. The simulation parameters are given in Table IV. According to the procedure described in the previous section, the results presented in Table V are obtained. In the following discussion of the results, first, the most sensitive switch per topology will be identified and, second, the overall performance of the topologies will be compared with each other.

### A. Identification of the most sensitive switch per topology

*1) European Efficiency:* The findings for the impact of parameter variations on the EU efficiencies are represented in Fig. 5 and Table V for the analyzed switches of each topology. As described before, based on equation (1), the mean value ($\mu$) as well as the standard deviation ($\sigma$) for the corresponding pdf of each switch are provided and referred to the obtained overall "European mean value" for the respective topology. In the case of H5 (Fig. 5 (a)), the analyzed switches show very similar performance. The values of the standard deviation change from $\sigma_{\eta EU} = 2.55$ % to $\sigma_{\eta EU} = 2.66$ % for switches #1 and #5, respectively, and the obtained efficiencies change from $\mu_{\eta EU} = 94.41$ % to $\mu_{\eta EU} = 94.52$ % from switch #5 to switch #1, respectively. Moreover, from Figs. 5 (c) and (d) it is evident that the analyzed switches of HB-NPC and HERIC, respectively, are not much affected by parameter variations, since the values for $\mu_{\eta EU}$ and $\sigma_{\eta EU}$ are nearly the same for all switches per topology. Therefore, the impact of parameter variation on different switches in terms of efficiency is not significant. In case of H6 it is to be observed from Fig. 5 (b) that switch #1 shows the best performance ($\mu_{\eta EU} = 95.05$ %), whereas D7 shows the highest standard deviation with

TABLE IV: Simulation parameters.

| Parameter | Value |
|---|---|
| $P_n$ | 3.3 $kW$ |
| $V_{grid}$ | 230 $V^{rms}$ |
| $f_{grid}$ | 50 $Hz$ |
| $V_{dc}$ | 600 $V$ |
| $f_{sw}$ | 6 $kHz$ |
| $C_{parasitic}$ | 100 $nF$ |
| $L_{inv}$ | 4.7 $mH$ |
| $R_{inv}$ | 0.2 $\Omega$ |
| $L_{grid}$ | 2.1 $mH$ |
| $R_{grid}$ | 0.1 $\Omega$ |
| $C_f$ | 10 $\mu F$ |
| $R_{damp}$ | 10 $\Omega$ |

$\sigma_{\eta EU} = 2.48$ %. In addition, with a range from 1.68 % to 2.48 % the standard deviation changes the most in this case.

*2) Leakage current:* The results for the impact of parameter variations of the analyzed switches for each topology are also presented in Fig. 5 as well as in Table V. From Fig. 5 (a) it can be seen, that for H5 there is no significant impact to be found since the values for $\mu_{I_{leak,EU}}$ and also the standard deviations $\sigma_{I_{leak,EU}}$ are close to the corresponding mean values. In case of HB-NPC (Fig. 5 (c)) switch #1 exhibits the smallest $\sigma_{I_{leak,EU}}$, whereas D5 is affected the most by parameter variations. For the H6 topology it is observed from Fig. 5 (b) that switch #1 exhibits the best performance, resulting in the lowest $\mu_{I_{leak,EU}}$ and $\sigma_{I_{leak,EU}}$, respectively. In contrast, the highest leakage current is obtained for D7, which is also showing the highest standard deviation for the analyzed switches and, therefore, is to be considered the most sensitive switch for H6 with respect to the impact of parameter variations on leakage current. In case of HERIC, in Fig. 5 (d) it is shown that switches #1 and #5 exhibit the best performances, since they result in the lowest $\mu_{I_{leak,EU}}$ and $\sigma_{I_{leak,EU}}$, respectively. The switch, that is showing the worst performance and is therefore affected the most by parameter variations, is switch #4.

*3) Grid-side dc current component:* Based on Table V, the radar charts presented in Fig. 5 also show the obtained results for the impact of parameter variations on the grid-side dc current component for the analyzed switches of the corresponding topology. For H5, H6 and HB-NPC topologies it can be seen, that there is no significant impact of parameter variations on $\mu_{I_{dc,EU}}$. On the contrary, the results for the analyzed switches of the HERIC topology vary a lot. As can be seen from Fig. 5 (d), switch #5 results in the highest $\mu_{I_{dc,EU}}$, switch #6 in the lowest. The largest standard deviation $\sigma_{I_{dc,EU}}$ is obtained for switch #1, switch #6 results in the lowest as referred to the mean value of the topology. Nevertheless, switches #1 and #6 exhibit the highest relative standard deviations ($CV_{I_{dc,EU}}$), and are therefore to be considered the switches which are affected the most by parameter variations for the HERIC topology.

### B. Identification of the most sensitive topology

As stated in Section III for comparing the topologies with each other the coefficient of variance $CV_{x,EU}$ of the mean values of each topology is chosen, since a direct comparison by means of absolute values is not meaningful. The values for each topology are summarized in Table V.
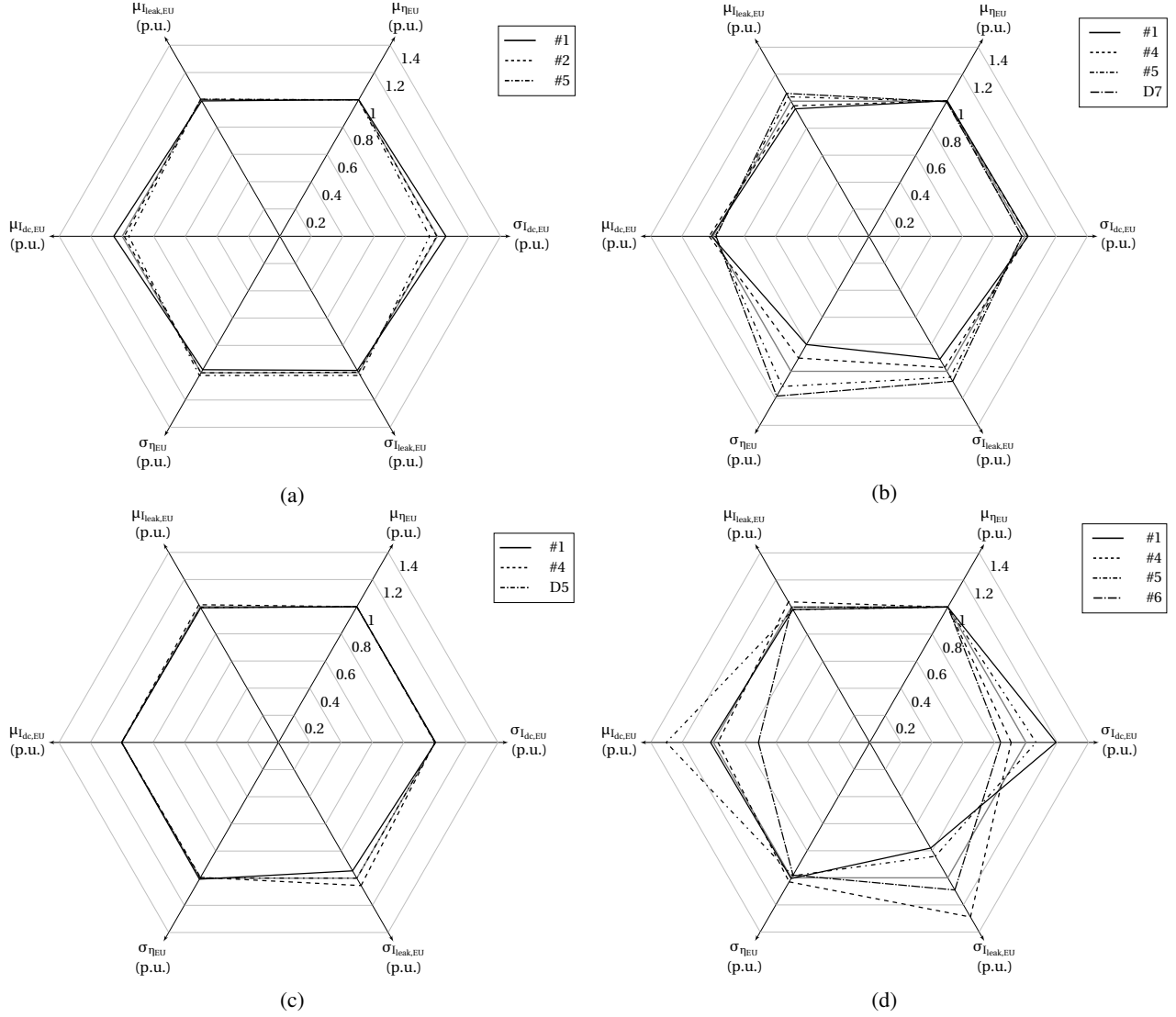
Fig. 5: Identification of the most sensitive switch of each tested topology with respect to the analyzed parameters: (a) H5 topology, (b) H6 topology, (c) HB-NPC topology, (d) HERIC topology.

*1) European Efficiency:* With respect to the European efficiency H5 is the topology which results in the lowest $\mu_{EU,\eta,H5} = 94.46$ % and the highest mean standard deviation $\sigma_{EU,\eta,H5} = 2.61$ %, resulting in a mean relative standard deviation of $CV_{EU,\eta,H5} = 2.76$ %. On the contrary, for the HERIC topology the highest $\mu_{EU,\eta,HERIC} = 95.82$ % as well as the lowest mean standard deviations $\sigma_{EU,\eta,HERIC} = 2.01$ % is obtained. The mean relative standard deviation is $CV_{EU,\eta,HERIC} = 2.10$ %. Therefore, with respect to European efficiency, H5 topology is affected the most by parameter variations of the employed switching devices.

*2) Leakage current:* In terms of mean leakage current the topology resulting in the lowest $CV_{EU,I_{leak}}$ is the HERIC topology with $CV_{EU,I_{leak},HERIC} = 17.51$ %. This means that, even though HERIC exhibits the largest variability for its analyzed switches, the mean relative standard deviation is the lowest of all topologies, since the standard deviations with respect to the magnitudes of $\mu_{I_{leak},EU}$ are very low. The topology resulting in the highest mean relative standard

deviation with respect to leakage current is HB-NPC with $CV_{EU,I_{leak},HB-NPC} = 47.47$ %.

*3) Grid-side dc current component:* For the HB-NPC topology the lowest mean relative standard deviation $CV_{EU,I_{dc}}$ is obtained with $CV_{EU,I_{dc},HB-NPC} = 68.80$ %. On the contrary, the topology showing the highest mean relative standard deviation is H5 with $CV_{EU,I_{dc},H5} = 92.29$ %. Therefore, even though the values for $\mu_{I_{dc},EU}$ are very low compared to the analyzed switches of HB-NPC, the standard deviations $\sigma_{I_{dc},EU}$ referred to the mean values $\mu_{I_{dc},EU}$ are higher in case of H5. Therefore, H5 is the topology that is affected the most by parameter variations with respect to the grid-side dc current component.

## V. CONCLUSION

This work evaluates the sensitivity of H5, H6, HB-NPC and HERIC topologies in $1\phi$ PV inverters to the chosen switching device. Therefore, the applied methodology for the sensitivity analysis and the chosen topologies for the analysis

TABLE V: Simulation results of the analyzed parameters for the sensitivity analysis.

| | | $\mu_{\eta_{EU}}$ (%) | $\sigma_{\eta_{EU}}$ (%) | $CV_{\eta_{EU}}$ (%) | $\mu_{I_{leak,EU}}$ (mA) | $\sigma_{I_{leak,EU}}$ (mA) | $CV_{I_{leak,EU}}$ (%) | $\mu_{I_{dc,EU}}$ (mA) | $\sigma_{I_{dc,EU}}$ (mA) | $CV_{I_{dc,EU}}$ (%) |
|---|---|---|---|---|---|---|---|---|---|---|
| H5 | $\mu_{EU}$ | 94.46 | 2.61 | 2.76 | 292.25 | 92.37 | 31.61 | 41.44 | 38.24 | 92.29 |
| | #1 | 94.52 | 2.55 | 2.70 | 289.80 | 90.83 | 31.34 | 43.68 | 40.30 | 92.26 |
| | #2 | 94.45 | 2.61 | 2.76 | 293.34 | 92.06 | 31.38 | 40.91 | 38.08 | 93.08 |
| | #5 | 94.41 | 2.66 | 2.82 | 293.61 | 94.23 | 32.09 | 39.73 | 36.35 | 91.49 |
| H6 | $\mu_{EU}$ | 94.71 | 2.1 | 2.21 | 88.84 | 28.09 | 31.62 | 44.13 | 36.63 | 83.01 |
| | #1 | 95.05 | 1.68 | 1.77 | 83.82 | 25.56 | 30.49 | 44.55 | 37.38 | 93.91 |
| | #4 | 94.92 | 1.89 | 1.99 | 85.79 | 27.31 | 31.83 | 45.21 | 37.26 | 82.42 |
| | #5 | 94.51 | 2.33 | 2.47 | 91.77 | 29.33 | 31.96 | 43.49 | 35.96 | 82.69 |
| | D7 | 94.35 | 2.48 | 2.63 | 93.97 | 30.17 | 32.11 | 43.25 | 35.91 | 83.03 |
| HB-NPC | $\mu_{EU}$ | 95.36 | 2.21 | 2.32 | 95.09 | 45.14 | 47.47 | 292.91 | 201.52 | 68.80 |
| | #1 | 95.33 | 2.23 | 2.34 | 94.30 | 42.70 | 45.28 | 292.91 | 202.03 | 68.97 |
| | #4 | 95.37 | 2.20 | 2.31 | 96.47 | 47.60 | 49.34 | 293.07 | 200.93 | 68.56 |
| | D5 | 95.37 | 2.21 | 2.32 | 94.51 | 45.13 | 47.75 | 292.74 | 201.60 | 68.87 |
| HERIC | $\mu_{EU}$ | 95.82 | 2.01 | 2.10 | 160.92 | 28.17 | 17.51 | 70.74 | 57.84 | 81.76 |
| | #1 | 95.79 | 2.02 | 2.11 | 157.97 | 21.98 | 13.91 | 71.99 | 68.98 | 95.81 |
| | #4 | 95.76 | 2.07 | 2.16 | 167.13 | 36.32 | 21.73 | 68.61 | 52.35 | 76.30 |
| | #5 | 95.88 | 1.98 | 2.07 | 157.79 | 23.68 | 15.01 | 92.04 | 61.55 | 66.87 |
| | #6 | 95.86 | 1.97 | 2.06 | 160.78 | 30.70 | 19.09 | 50.32 | 48.48 | 96.34 |

were presented first. In order to simplify the comparison of the performance of the analyzed switches within each topology as well as the comparison of the performance of the selected topologies with each other, the processing of the results as "European mean values" and the use of the "European coefficient of variation" were introduced.

The obtained results reveal the most sensitive switches within each topology with respect to the impact of parameter variations on the measures European efficiency, leakage current, and grid-side dc current component, respectively. Based on the pdfs and the European mean values for the analyzed switches of each topology, H6 was found to show the highest spread in terms of European efficiency, whereas HERIC was affected the most by parameter variations with respect to both, leakage current and grid-side dc current component.

By using the European coefficient of variation, the overall relative mean performances of the topologies were compared. Thus, it was found that H5 was affected the most by parameter changes with respect to European efficiency and grid-side dc current component, respectively. For the leakage current HB-NPC was affected the most, since it was showing the highest mean relative standard deviation.

The applied analysis is based on a statistical approach which allows the probability distribution function of the selected performance indicators (European Efficiency, grid-side dc current component and leakage current) to be obtained. The proposed evaluation method can be applied during the design stage in order to select the most suitable power devices for the implementation of each switch within a certain topology or for the choice of a set of topologies, which use best a given set of switching devices, whose choice is driven from supply chain management considerations.

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