Digital Object Identifier (DOI): 10.1109/ISIE.2016.7745070

IEEE 25th International Symposium on Industrial Electronics (ISIE)

Variable frequency voltage control in a ST-fed grid by means of a Fractional-Order Repetitive Control

Giovanni De Carne
Zhixiang Zou
Giampaolo Buticchi
Marco Liserre

Suggested Citation

G. De Carne, Z. Zou, G. Buticchi and M. Liserre, "Variable frequency voltage control in a ST-fed grid by means of a Fractional-Order Repetitive Control," *2016 IEEE 25th International Symposium on Industrial Electronics (ISIE)*, Santa Clara, CA, USA, 2016, pp. 1230-1235.

Variable frequency voltage control in a ST-fed grid by means of a Fractional-Order Repetitive Control

Giovanni De Carne, Zhixiang Zou, Giampaolo Buticchi, Marco Liserre
Chair for Power Electronics
Christian-Albrechts University of Kiel
Kaiserstr. 2, 24143 Kiel
Germany
Email: gdc,zz,gibu,ml@tf.uni-kiel.de

***Abstract*—The greater demand variability caused by the high penetration of Distributed Generation (DG) challenges the LV grids. Although the DG supports the local load demand, its intermittent nature (i.e. renewables) can create undesired conditions: reverse power flow from the Low (LV) to Medium Voltage (MV) grid in case of low load demand and high power production, or overloading of the substation transformer in case of low power production and high load demand. The Smart Transformer (ST) offers the possibility to decouple under certain extents the Low Voltage (LV) grid from the MV grid, when a multiple stage configuration is chosen. In the LV side, the ST can change the grid frequency in order to modify the DG power production. Following a frequency variation, the DG P/f droop controllers adapt the injected power to the new frequency value, providing locally the power demanded by the loads. In this work, this feature is used for avoiding the reverse power flow in the MV grids. Approaching the zero power flow condition, the ST increases the frequency in order to curtail the DG production. However, this method may affect the conventional ST controller, originally designed for working at 50 Hz, that must be optimally designed for working under variable frequency condition. In this work, the Fractional-Order Repetitive Control (FORC) has been proposed as ST controller in order to deal with the frequency change, offering better performance than the Proportional-Resonant (PR) and Conventional Repetitive Controllers (CRC). The effectiveness of this method has been proved using the Control-Hardware-In-Loop (CHIL) evaluation by means of a Real Time Digital Simulator (RTDS).**

I. Introduction

The DG integration in the distribution grids has grown consistently in the last years, mostly wind turbines and photovoltaic plants. Considering the case of Germany, and in particular of north regions like Schleswig-Holstein, where the installed power of wind turbines reaches 9 GW [1], the impact on the grid can not be anymore considered negligible. Thus the distributed generators must participate to the system control, providing ancillary services and increasing the robustness of the grid. The national regulators published new rules in terms of DG control [2]: the DG should not disconnect in presence of a grid disturbance, but it must help in the grid control. In particular, the frequency variations in the grid following a heavy disturbance (e.g., bulk generators disconnection, line switching, fault, etc.) must not cause the DG switching off. For these reasons, the frequency range where the DG must remain connected has been extended from [49.8-50.2 Hz] to [47.5-51.5 Hz], and the DG must decrease linearly the power injection in case of frequency higher than 50.3 Hz. However, in case of Smart Transformer-fed grids, the frequency of the LV grid can be imposed by the ST, independently from the MV grid operating point. The ST, being a three-stages power electronics based transformer [3], enables control of LV grid independently from the MV grid, due to the presence of two DC stages (one in MV and one in LV). Thus, in a ST-fed grid, the Smart Transformer is in charge of controlling the frequency and not the local generators. However, the presence of the droop controllers in the DG may be exploited for creating an interface between the ST and the local generation: varying the output frequency of the ST, the power injection of the DG is changed by the droop controller. This technique has been already implemented in [4] [5], where it has been used for avoiding the ST overload increasing the power production in the LV grid. Decreasing the frequency, the generators present in the LV grid increase the power output in order to reduce the current flowing in the ST. A similar approach has been analyzed in this work for avoiding the reverse power flow conditions. If the active power injection of DG is near or equal to the load consumed power, the ST increases the frequency in order to communicate to the local DG to decrease the energy production, as can be noted in Fig.1. Only when the load power request in the LV grid increases again, the ST decreases the frequency, returning to operate in nominal conditions. In this way the ST avoids to inject active power in the MV grid until it has control capability over the DG.

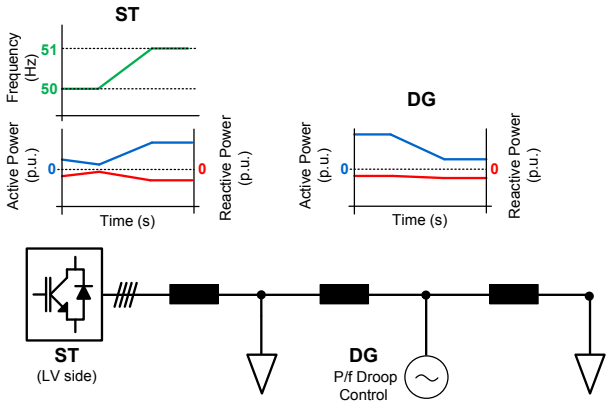

Fig. 1. ST variable frequency voltage control

However, changing the frequency of the system creates some control problems. Currently most of the existing con-

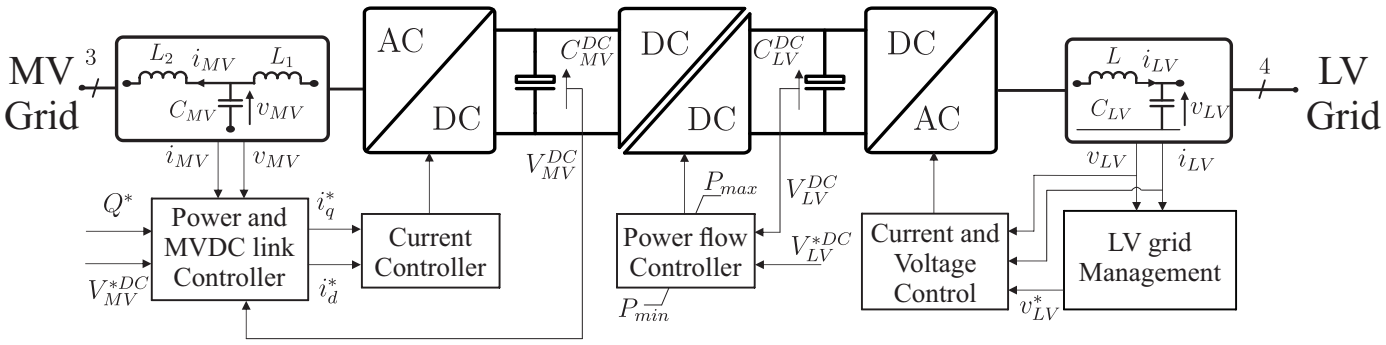

Fig. 2. Smart Transformer control scheme.

trollers for grid connected converters, as well as microgrids application [6], are designed to control signals at the fundamental frequency (e.g. 50/60 Hz). When a variable frequency control is applied in ST-fed grids, the conventional controllers incur in performance degradations [7] [8]. Additionally, the DG may forced to reduce the injected power at the point to not guarantee an acceptable current harmonic profile. In order to cope with this problem, the Fractional-Order Repetitive Control (FORC) is implemented in the ST for the variable frequency control [7]. In this work it has been demonstrated how the FORC shows better performances as ST voltage controller than the Proportional-Resonant controller and the Conventional Repetitive Control (CRC) when a frequency increase is applied in presence of DG. It keeps constant the fundamental frequency amplitude and reduces the overall voltage harmonic content in the grid, also when the DG injects high harmonic currents in the grid due to the droop controller action. This paper is organized as follows: the Smart Transformer control is described in Section II; in Section III the mathematical description of the CRC and the FORC have been given. In Section IV, the CHIL setup has been explained with the description of the simulated grid in RTDS. The proposed controller has been verified in Section V with experimental results obtained in a Real Time Dynamic Simulator (RTDS) by means of CHIL method. Finally, conclusions are drawn in Section VI.

II. Smart Transformer Control

The Smart Transformer (ST) is a three-stage power electronics transformer [3], [9] that adapts the voltage between the MV to the LV grid. The LV side controls the voltage in order to provide sinusoidal and balanced voltage waveforms independently from the load power request. The DC/DC converter transforms the voltage from MV to LV and controls the voltage level of the LV DC link. For these reasons, the Dual Active Bridge (DAB) technology has been adopted in this study. The MV side keeps the MV DC link voltage fixed to the nominal value, absorbing or injecting the needed power in the MV grid. The control strategy of the transformer is shown in Fig. 2.

The MV converter is controlled by means of an outer MVDC link and power loop and an inner AC current loop. The MVDC link loop controls the DC link voltage to the nominal value setting the AC active current reference. The power loop receives the reactive power references from external power controllers in order to provide reactive power injection in the MV grid. The inner loop receives the references from the outer loop and controls the active and reactive currents to be requested from the MV grid. The output of current loop are the PWM signals for the MV converter. The DC/DC converter, for instance the DAB, regulates the power flow between the two DC stages. The DAB controller controls the power flow from the MV side to the LV side in order to keep the LV DC link voltage constant to the nominal value. The reference power is limited between the P_{max}, determined by the ST sizing, and P_{min}. The LV converter is composed of a frequency control loop and the FORC. The frequency controller measures the active power flowing in the ST and approaching the conditions of zero active power it increases the frequency of the voltage waveform reference. The new reference is sent to the FORC, explained in the next section.

III. ST Frequency Control

The conventional control strategies and the proposed frequency-adaptive control scheme are presented in this section.

A. Conventional Control Strategies

At first, the conventional voltage controllers are investigated. The simplified block diagram of the closed-loop control system for a ST LV side inverter is shown in Fig.3, where v_{ref} is the voltage reference input, v_{LV} is the measured ST LV side voltage, $e = v_{ref} - v_{LV}$ is the control error, d represents the disturbance, G_c and G_f are the transfer functions of the voltage controller and the LC filter, G_d is the 1.5 sampling delay taking in account the controller computation time. The delay can be written using a Padé approximation as

$$G_d(s) = e^{-1.5T_s s} \approx \frac{12 - 9T_s s + 2.25T_s^2 s^2}{12 + 9T_s s + 2.25T_s^2 s^2}. \qquad (1)$$

where T_s is the sampling interval of the control system.

For optimal voltage control performance, a Internal Model Principle-based Controller (IMP-C) has been employed for the control part of G_c to track periodic signals or eliminate disturbances. For example, study cases on the Generalized

Integrator (GI) and CRC-controlled voltage feedback systems have been investigated in literature and in power electronics applications, including Uninterrupted Power Supply (UPS) [10], Dynamic Voltage Regulator (DVR) [11], and Distribution Generator (DG) [12]. The transfer functions of GI and CRC can be written respectively as follows

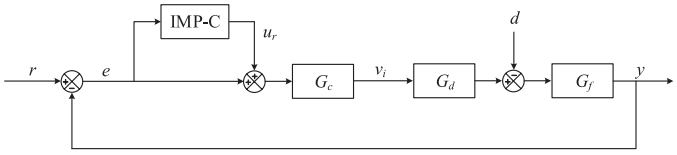

Fig. 3. Simplified block diagram of closed-loop voltage control system.

$$G_{gi}(s) = \frac{s}{s^2 + (k\omega)^2}. \tag{2}$$

$$\begin{aligned} G_{rc}(s) &= \frac{e^{-sT_sN}}{1 - e^{-sT_sN}} \\ &= -\frac{1}{2} + \frac{1}{T_sN}\frac{1}{s} + \frac{1}{T_sN}\sum_{k=1}^{\infty}\frac{s}{s^2 + (k\omega)^2}. \end{aligned} \tag{3}$$

where ω is the fundamental frequency, k is the order of harmonics, and N is the RC order representing the sampling number of each periodic cycle. It is straightforward that the transfer function of CRC is composed of a set of GI at frequencies multiple of the fundamental frequency plus a classic PI controller. In the real system, CRC is usually implemented digitally and its transfer function in z-domain can be written as [13]

$$G_{rc}(z^{-1}) = \frac{z^{-N}}{1 - z^{-N}}. \tag{4}$$

The main features of the IMP-based controllers is the infinite control gains at the interested frequencies due to the corresponding poles on the imaginary axis and therefore achieve zero steady-state error for signal components below the Nyquist frequency. As a results, the IMP-based controllers show competitive advantages in the voltage waveform control application with fixed fundamental frequency.

B. Frequency Adaptive Control

However, in a ST-fed distribution grid, the voltage frequency of LV side is adjustable within a certain range according to the frequency droop characteristic. The conventional controllers, like GI, can no longer maintain good performance under variable frequency conditions. Moreover, in a digital system, the CRC order N would usually be fractional value with a fixed sampling rate. Previous research works adopt the nearest integer value of CRC order but this method cannot precisely track fractional period signals due to the high control gains shift from the interesting frequencies. To address this issue, a frequency-adaptive control strategy based on CRC has been proposed for the ST application. The fractional component of CRC order can be approximated by the Fractional Delay (FD) filters design approach [14] [15], in which z^{-N} can be approximated with a set of integer order delays. Assuming that $z^{-N} = z^{-N_i - F}$ with $N_i = int[N]$ being the integer component of N and $F = N - N_i$ $(0 \leq F < 1)$ being the fractional component of N, the FD filter of z^{-F} can be approximated by a Lagrange interpolation polynomial Finite-Impulse-Response (FIR) filter as follow:

$$z^{-F} \approx \sum_{k=0}^{n} A_k z^{-k}. \tag{5}$$

where $k \in N$, A_k is the Lagrange coefficient and can be calculated as following

$$A_k = \prod_{\substack{i=0 \\ i \neq k}}^{n} \frac{F - i}{k - i} \tag{6}$$

According to the properties of Lagrange interpolation polynomial, the approximation remainder of FD can be written as following

$$\begin{aligned} R_n &= z^{-F} - \sum_{k=0}^{n} A_k z^{-k} \\ &= \frac{\xi^{-F-n}\prod_{i=0}^{n-1}(-F - i)}{(n+1)!}\prod_{i=0}^{n}(F - i) \end{aligned} \tag{7}$$

where $\xi \in [T_{k-1}, T_k]$, T_{k-1} and T_k are the $(k-1)th$ and kth sampling intervals, respectively. With the increasing of the order n, the denominator increases while the nominator almost keeps constant. Therefore, a smaller approximation remainder can be acquired indicating a more accurate approximation can be achieved.

Substituting (5) and (6) into (4), an all-digital Fractional-Order Repetitive Control (FORC) can be obtained as

$$G_{forc}(z^{-1}) = \frac{z^{-N_i}\sum_{k=0}^{n} A_k z^{-k}}{1 - z^{-N_i}\sum_{k=0}^{n} A_k z^{-k}} \tag{8}$$

For instance, if $N_i = N$, the transfer function of FORC will turn into a CRC. As a result, FORC scheme provides a general way to track or reject any periodic signal with arbitrary fundamental frequency. The schematic block diagram of FORC is shown in Fig.4, where all the Lagrange coefficients A_k are derived from the equation of (6). Since the maximum rate of ST frequency variation (e.g. 1 Hz/s) is much slower than the sampling frequency (typically in the range [5 kHz-20 kHz]), the online update of Lagrange coefficients varies smoothly, having limited influence on the FORC output in every sampling interval. With this consideration, the overall control system with a FORC controller can be treated as a Linear Time-Invariant (LTI) system in the theoretical analysis as well as parameter design [16].

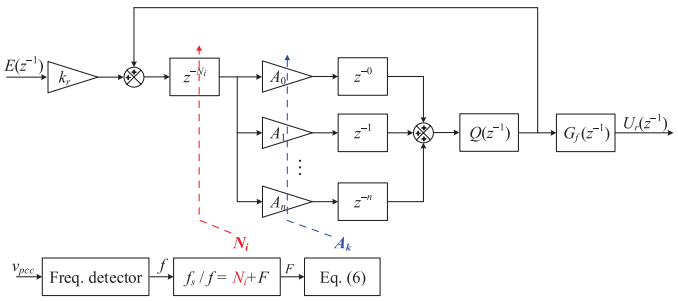

Fig. 4. Schematic diagram of frequency-adaptive control scheme.

IV. Control-Hardware-In-Loop setup

The Control-Hardware-In-Loop evaluations has been performed by means of the RTDS system and a dSPACE1104. In the RTDS a modified CIGRE European LV distribution network benchmark [17] has been simulated, working at 50 Hz and 230 V_{rms}. Without losing in generality for the proposed approach, the following modifications have been made in order to cope with the limited computation capability of the RTDS and dSPACE setup in the lab: 1) the loads are balanced and simulated as constant power model; 2) the two BESSs and PV B active and reactive power set points are set to zero; 3) the wind turbine has been neglected. In RTDS, the ST and the PV A converters are simulated with real switching model converters and controlled in dSPACE. The ST is represented by a Neutral Point Clamped (NPC) converter in RTDS, with a voltage controller implemented in dSPACE. The PV A is simulated with a three-phase full converter in RTDS, controlled in dSPACE by means of a current controller. The loads parameters are listed in Table I, instead the ST and PV converters and plants data can be found in Table II.

TABLE I. Load Data

Load	Bus	Apparent Power (kVA)	cosφ
L1	11	5.7	0.85
L2	15	19.2	0.85
L3	16	19.2	0.85
L4	17	2.7	0.85
L5	18	8.8	0.85

TABLE II. ST and PV converters and plants data

ST Parameter	Value	PV Parameter	Value
fs	5 kHz	fs	5 kHz
V_{LV}^{DC}	900 V	V_{PV}^{DC}	700 V
C_{LV}^{DC}	10 mF	C_{PV}^{DC}	5 mF
L_{LV}	1.7 mH	$L1_{PV}$	4.5 mH
C_{LV}	100 μF	C_{PV}	8 μF
		$L2_{PV}$	0.5 mH

The CHIL in the ST case has been implemented as following: the RTDS sends the 3-phase voltage measurements to the dSPACE, where the chosen voltage controller (for instance PR controller, CRC or FORC) is implemented. The controller outputs are the 3 modulation signals to be sent to the RTDS. In the RTDS the modulation signals are used for obtaining the gate signals by means of the Phase-Disposition PWM (PD-PWM). Similarly, the PV CHIL is performed as following: the RTDS sends the current measurements to the dSPACE and here a PI controller compares them with the reference currents, obtained from the active and reactive power references imposed in dSPACE. The controller outputs, which are the PV converter modulation signals, are sent back to the RTDS where the gate signals are generated with the PWM generator implemented in RTDS. The PV is equipped with a P/f droop controller able to curtail the power injection from 0 % at 50.3 Hz to 100 % at 51.5 Hz, as described in [2].

V. Control-Hardware-In-Loop evaluation

The CHIL evaluation has been performed considering as base case the PR controller implemented in abc frame as ST voltage controller. No resonant harmonic compensator has been taken in account in the base case, due to the following comparison between the CRC and the FORC. In ordinary conditions, the PV converter injects 55 kW with $cos(\varphi) = 1$, corresponding to a current injection of about 80 A. As can be noticed from Fig.6(a), the ST imposes voltage waveforms with the proper amplitude but affected by harmonics. The voltage drop caused by the current harmonics deriving from the DG create the voltage waveform distortion. The same behavior is noticeable in the PV voltages in Fig.6(c), affected from both low and high order harmonics. The CRC controller, offering harmonic compensation for both even and odd harmonics, is able to improve the voltage waveform profile: the harmonic content is reduced both at ST level (Fig.7(a)) and at PV level (Fig.7(c)). In nominal frequency conditions, the CRC results be effective for the amplitude control and harmonic compensation. However, having a fixed resonant frequency, its performances deteriorated if the frequency varies from the nominal value.

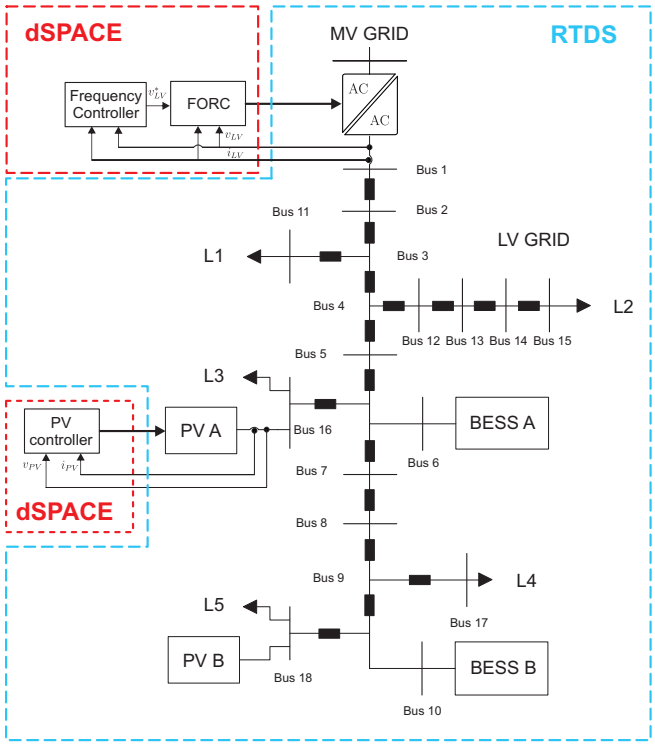

Fig. 5. CHIL: modified CIGRE European LV distribution network benchmark implemented in RTDS (large-dotted cyan square), ST controller implemented in dSPACE (dotted red square), and PV controller (dotted red square).

When the DSO requests to reduce the DG power in order to leave a safety margin from the reverse power flow condition, the ST increases the frequency from the nominal value to 51 Hz. The DG droop controller curtails the power output from 55 kW to 15 kW, working with partial power production. Two different problems can be noticed in Fig.8 from this control action when the conventional PR controller is implemented in the ST: 1) the ST voltage controller still resonate to 50 Hz and it is not able to sense the frequency variation (Fig.8(a)); 2) the PV, working to partial power production, injects higher harmonic currents, noticeable also at the PV bus (Fig.8(c),(d)). Similar conclusions can be drawn for the CRC case in Fig.9. The ST voltage controller resonates still at the 50 Hz and the

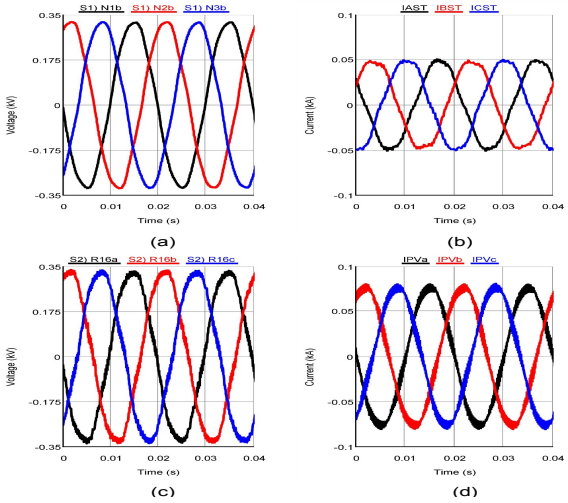

Fig. 6. PR controller, 50 Hz case: (a) ST voltages, (b) ST currents, (c) PV bus voltages, (d) PV grid-side filter inductance currents.

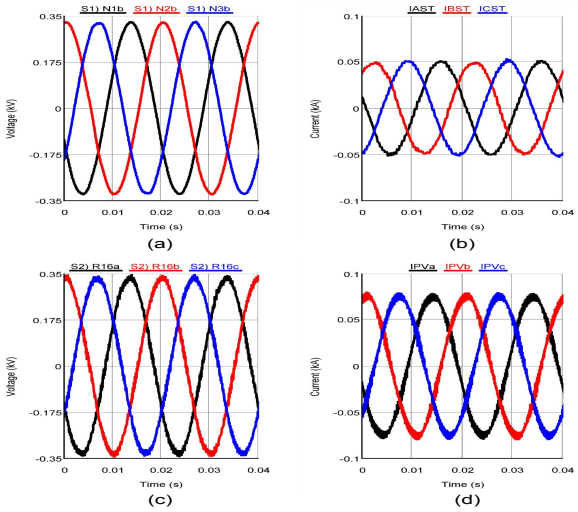

Fig. 7. CRC controller, 50 Hz case: (a) ST voltages, (b) ST currents, (c) PV bus voltages, (d) PV grid-side filter inductance currents.

harmonic compensation is working only partially. The grid voltage harmonics, multiple of the first harmonic, are not synchronized with the CRC resonant peaks, decreasing the effectiveness of the control. When the FORC is applied at 51 Hz, the improvements are bigger than the CRC case (Fig.10): the voltage profile has a reduced harmonic profile both at ST and PV bus (Fig.10(a),(c)), and also the current output from the ST has lower harmonic content (Fig.10(b)). In Fig.11 has

TABLE III. COMPARISON CONTROLLERS

Controller	THD%	V_{peak}	V_{rms}
PR	0.7	323.4	231.8
CRC	1.0	313.7	226.6
FORC	0.4	323	230.1

been plotted the comparison of the FFT profiles of the three aforementioned controllers. The ST voltage waveforms have been sampled for 20 seconds and a FFT with a sampling frequency of 5 ksamples/second has been performed. As can be noted, the FORC shows better performances in case of 3^{rd}, 5^{th}

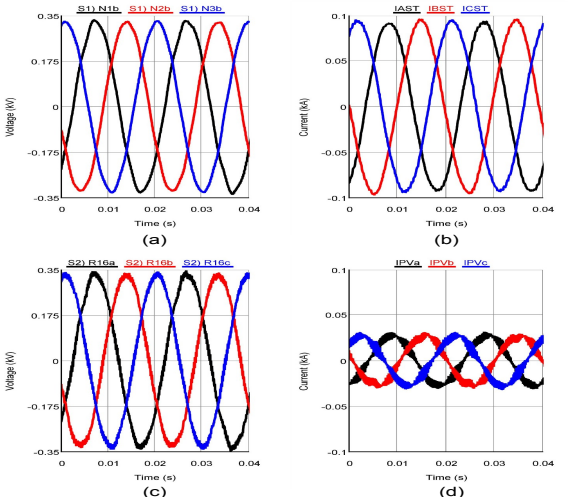

Fig. 8. PR controller, 51 Hz case: (a) ST voltages, (b) ST currents, (c) PV bus voltages, (d) PV grid-side filter inductance currents.

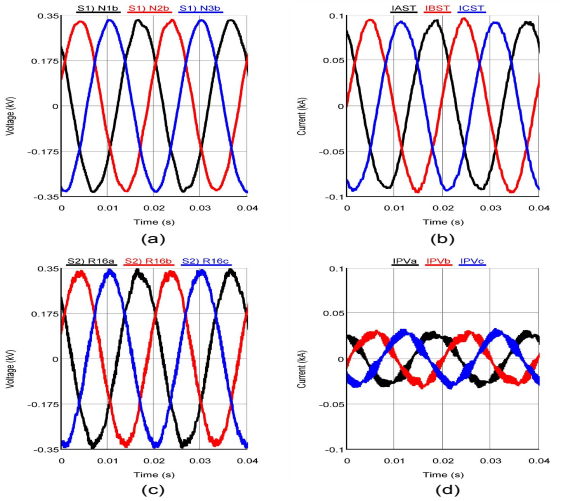

Fig. 9. CRC controller, 51 Hz case: (a) ST voltages, (b) ST currents, (c) PV bus voltages, (d) PV grid-side filter inductance currents.

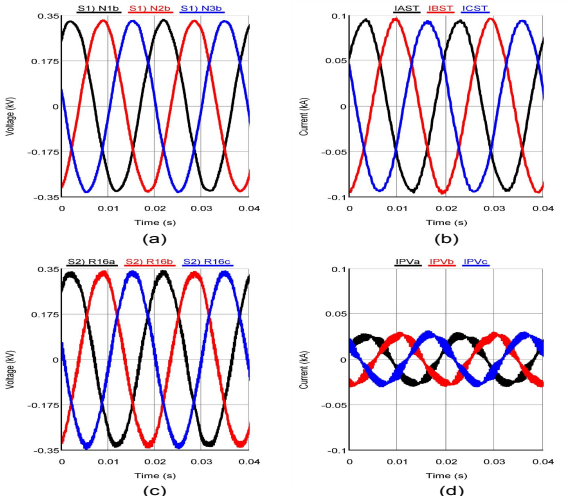

Fig. 10. FORC controller, 51 Hz case: (a) ST voltages, (b) ST currents, (c) PV bus voltages, (d) PV grid-side filter inductance currents.

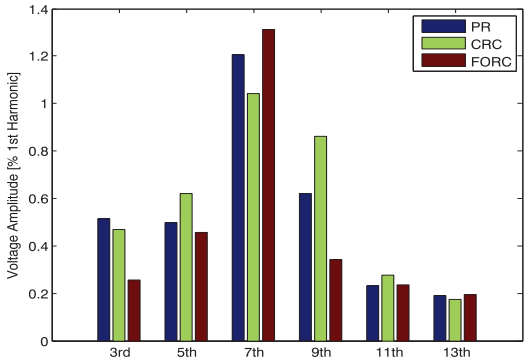

Fig. 11. FFT analysis of the ST Phase A voltage waveform in percentage of the nominal value: PR controller (blue bar), CRC (green bar), FORC (red bar).

and 9^{th} harmonic, while it is deteriorating the performances for the 7^{th}. For the 11^{th} and 13^{th} harmonics, the performances are comparable with PR and CRC. Regarding the THD of the voltage waveforms, substantial improvements have been achieved with the FORC as can be seen from Table III. The FORC is able to reduce the THD at $0.4\,\%$ and at the same time to provide an acceptable voltage peak and rms value. On the contrary, the CRC increases the overall THD till $1\,\%$ and reduces the voltage peak of $3.7\,\%$ from the nominal value.

VI. Conclusion

The ST can interact with the droop controllers of the local DG in the LV grid by means of frequency variations, avoiding the reverse power flow in MV grids. However, the actual ST controllers must be improved in order to cope with the variable frequency in the grid. In this paper a Fractional-Order Repetitive Control for the ST voltage controller has been proposed and compared with fixed-frequency controllers, such as Proportional-Resonant and Conventional-Repetitive-Control. The FORC has shown improved performances in terms of voltage harmonic distortion and amplitude with respect to the other two controllers, when a frequency change to $51\,\mathrm{Hz}$ has been applied.

Acknowledgment

The research leading to these results has received funding from the European Research Council under the European Union's Seventh Framework Programme (FP/2007-2013) / ERC Grant Agreement n. [616344] - HEART.

References

[1] "Chancen und potenziale der energiewendewirtschaft in schleswig-holstein," Ministeriums fuer Energiewende, Landwirtschaft, Umwelt und lndliche Raeume des Landes Schleswig-Holstein, Tech. Rep., 2015.

[2] "Cei 0-21, reference technical rules for the connection of active and passive users to the lv electrical utilities," CEI 0-21, Dec. 2012. [Online]. Available: http://www.ceiweb.it/doc/norme/12333.pdf

[3] X. She, A. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, Sept 2013.

[4] G. De Carne, G. Buticchi, M. Liserre, and C. Vournas, "Frequency-based overload control of smart transformers," in *IEEE Eindhoven PowerTech*, June 2015, pp. 1–5.

[5] G. De Carne, G. Buticchi, M. Liserre, P. Marinakis, and C. Vournas, "Coordinated frequency and voltage overload control of smart transformers," in *PowerTech, 2015 IEEE Eindhoven*, June 2015, pp. 1–5.

[6] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodriguez, "Control of power converters in ac microgrids," *Power Electronics, IEEE Transactions on*, vol. 27, no. 11, pp. 4734–4749, Nov 2012.

[7] Z. Zou, K. Zhou, Z. Wang, and M. Cheng, "Fractional-order repetitive control of programmable ac power sources," *IET Power Electronics*, vol. 7, no. 2, pp. 431–438, February 2014.

[8] Y. Yang, K. Zhou, H. Wang, F. Blaabjerg, D. Wang, and B. Zhang, "Frequency adaptive selective harmonic control for grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3912–3924, July 2015.

[9] R. Pena-Alzola, G. Gohil, L. Mathe, M. Liserre, and F. Blaabjerg, "Review of modular power converters solutions for smart transformer in distribution system," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2013, pp. 380–387.

[10] Z. Zou, Z. Wang, and M. Cheng, "Design and analysis of operating strategies for a generalised voltage-source power supply based on internal model principle," *Power Electronics, IET*, vol. 7, no. 2, pp. 330–339, February 2014.

[11] Y. W. Li, F. Blaabjerg, D. Vilathgamuwa, and P. C. Loh, "Design and comparison of high performance stationary-frame controllers for dvr implementation," *Power Electronics, IEEE Transactions on*, vol. 22, no. 2, pp. 602–612, March 2007.

[12] R. Mastromauro, M. Liserre, T. Kerekes, and A. Dell'Aquila, "A single-phase voltage-controlled grid-connected photovoltaic system with power quality conditioner functionality," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 11, pp. 4436–4444, Nov 2009.

[13] S. Hara, Y. Yamamoto, T. Omata, and M. Nakano, "Repetitive control system: a new type servo system for periodic exogenous signals," *Automatic Control, IEEE Transactions on*, vol. 33, no. 7, pp. 659–668, Jul 1988.

[14] T. Laakso, V. Valimaki, M. Karjalainen, and U. Laine, "Splitting the unit delay [fir/all pass filters design]," *Signal Processing Magazine, IEEE*, vol. 13, no. 1, pp. 30–60, Jan 1996.

[15] Y. Wang, D. Wang, B. Zhang, and K. Zhou, "Fractional delay based repetitive control with application to pwm dc/ac converters," in *Control Applications, 2007. CCA 2007. IEEE International Conference on*, Oct 2007, pp. 928–933.

[16] Z.-X. Zou, G. De Carne, G. Buticchi, and M. Liserre, "Frequency adaptive control of a smart transformer-fed distribution grid," in *IEEE Applied Power Electronics Conference (APEC)*, March 2016, pp. 1–7.

[17] "Benchmark system for network integration of renewable and distributed energy resources c06.04.02," CIGRE, Tech. Rep., 2014.