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Modular DC/DC converter structure with multiple power flow paths for smart transformer applications

Giampaolo Buticchi
Markus Andresen
Levy Costa
Marco Liserre

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Giampaolo Buticchi, Markus Andresen, Levy Costa, Marco Liserre
Christian-Albrechts Universität zu Kiel
Kaiserstrasse 2
Kiel, Germany
Tel.: +49 / (0) – 431 880 6104
Fax: +49 / (0) – 431 880 6103
E-Mail: gibu@tf.uni-kiel.de
URL: http://www.pe.tf.uni-kiel.de/en

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Keywords

High frequency power converter, Multilevel converters, Smart grids

Abstract

Smart Transformers (ST), solid-state transformers with advanced control functionalities, are expected to have an important market by 2020. However, still important technological barriers, in terms of reliability and efficiency, exist and only new semiconductor devices cannot solve them. The use of advanced power converter topologies and architectures can play a role too.
In this paper, a particular structure for the isolated DC/DC converter, core of a typical three-stage ST, is investigated. By employing the concept of Multiple Active Bridge, a modular and redundant architecture, a power converter characterized by multiple power routing paths is investigated.

Introduction

The increasing diffusion of renewable energy sources has created several problems in the transmission and distribution grids. One of the proposed solutions is to use microgrids [1], where each source is able to operate in "universal" mode [2], grid-connected or in an island, and portion of the grids are intentionally disconnected from the main grid. Another approach could be to substitute the distribution power transformer with intelligent solid state transformer [3] that, in addition to behaving like a normal transformer, offers additional characteristic, like dealing with unbalanced distribution of renewable sources [4] and functioning as an aggregator of information from intelligent devices (Figure 1). In this scenario the distributed sources should not be requested to change their operation mode but the Smart Transformer (ST) can use their normal de-rating characteristics requested by the grid codes to regulate the distribution grid [5].

Modular Power Transfer Block with multiple Quadruple Active Bridge

At the moment, the widespread solution to implement a DC/DC stage with HF transformer is represented by the Dual Active Bridge (DAB), as shown in Figure 2. This topology, if a proper design of the HF transformer is realized, allows having soft-switching turn-on of all the devices in the whole power range [6]. In this paper, a more complex structure is adopted, with the aim of increasing the flexibility and allowing the creation of multiple paths for the power flow.

These multiple power path could enable advanced power sharing control to improve the reliability at system level [7].

In Figure 4 an example block scheme of the ST is presented. Three single-phase H-bridge are present in the LV side and three Cascaded H-Bridge (CHB) converters form the MV side, depending on the rated voltage of the devices the number of cascaded cells can vary, in this case six cells were chosen as an example, but the results can be generalized. The power exchange between the low-voltage (LV) and medium-voltage (MV) side is realized with the power transfer block (PTB), which has the function to control the different DC Link voltages and to ensure an equal distribution of power.

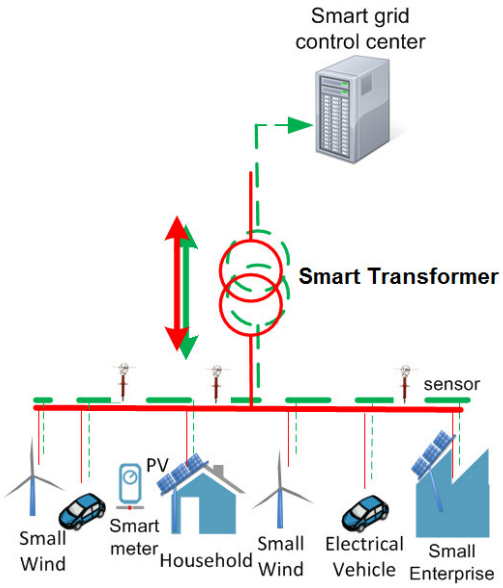

Figure 1. Smart-Transformer-based future grid.

The PTB is formed using standard blocks, that in this case are Quad-Active Bridges (QAB), as in Figure 3, whose characteristic equations are reported below (although a greater number of active bridges can be used [8]).

In order to obtain a greatly modular solution, each QAB should embed part of the control, in order to increase the reliability and simplify the higher level control. The PTB is realized by connecting the QAB between the LV and MV DC Links. However the QAB cells are connected to the MV DC Links with a particular pattern, ensuring that at least two QAB outputs are connected to each MV DC Link (for redundancy purpose) and a path through the MV ports of the QABs exists between each couple of MV DC Links.

As the most challenging case for the DC/DC converter is to operate correctly when there is an imbalance in the LV phases, this condition will be addressed, showing that the multiple power flow paths allow controlling the DC Links by exchanging powers between the QAB cells.

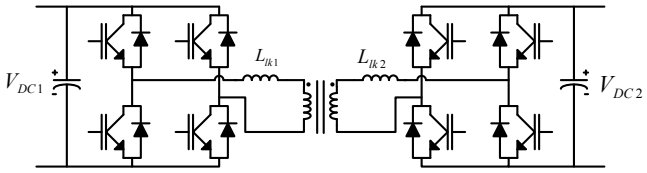

Figure 2. Dual Active Bridge.

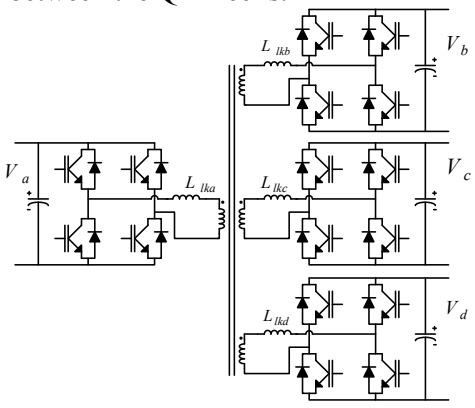

Figure 3. Quadruple Active Bridge.

The control of the QAB is realized by controlling the phase-shift between the different H-bridge.

Since the main goal of this architecture is to realize a very modular power converter, part of the control must be embedded on the single cell. In particular, the choice to implement a voltage controller for the LV DC Link and a balancing controller for the MV DC Links was made.

An outer voltage controller (Figure 5) regulates the LV DC Link, a Proportional Integral (PI) regulator can achieve satisfactory performance. Implementing also an internal power loop controller would imply the measure of the high-frequency pulsating power with a wide-bandwidth current sensor, for the solution of controlling only the phase shift was preferred.

It is important to note that each port participates into the power transfer. L_{lk} is the leakage inductance of the transformer and the phase shift of port a (φ_a) is considered as the reference.

The power reference generated by the voltage regulator of Figure 5 is used to generate a constant term of the phase shift for the three MV H-bridges (see Figure 5). The gain k in Figure 5 represents the linearization of the phase-shift characteristic. It would also be possible to make this term adaptive depending on the operating point, in order to reduce the effect of the intrinsic non-linear characteristic. The balancing controllers modify this constant phase shift term in order to keep the MV DC Links equalized.

The QAB will act as a building block for a more complex power converter, meaning that several modules will be connected in parallel/series to reach the appropriate voltage and power levels. Since the QAB embeds part of the control, non-ideal behavior of the converter must be taken into account. Since the paralleling of multiple DC/DC converter can be realized with a droop control, in Figure 5 a term R_V is introduced in order to generate an artificial voltage drop to stabilize the system. At port a the factor 1/3 is taken into account, considering that that port will process at maximum three times the power of ports b, c and d.

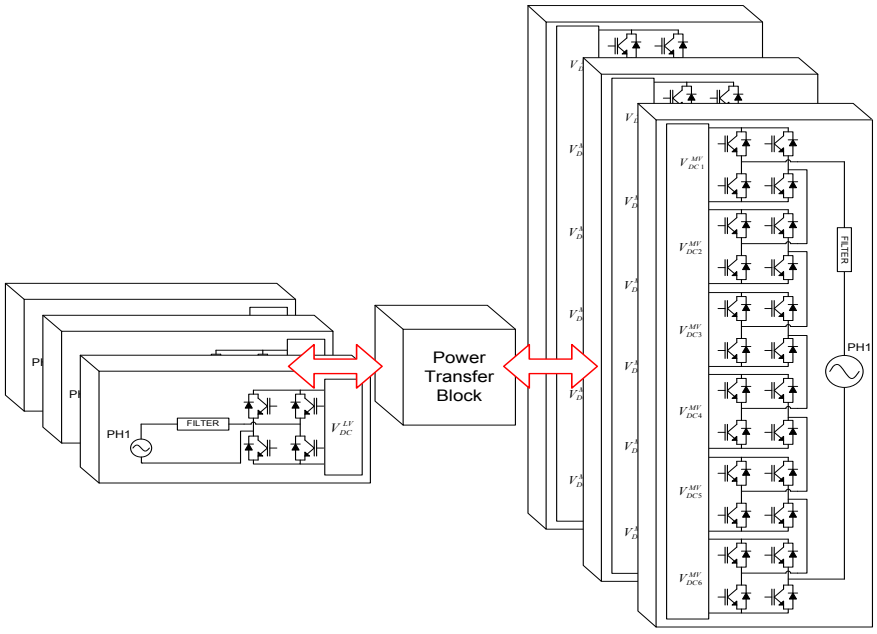

Figure 4. Basic architecture of the ST.

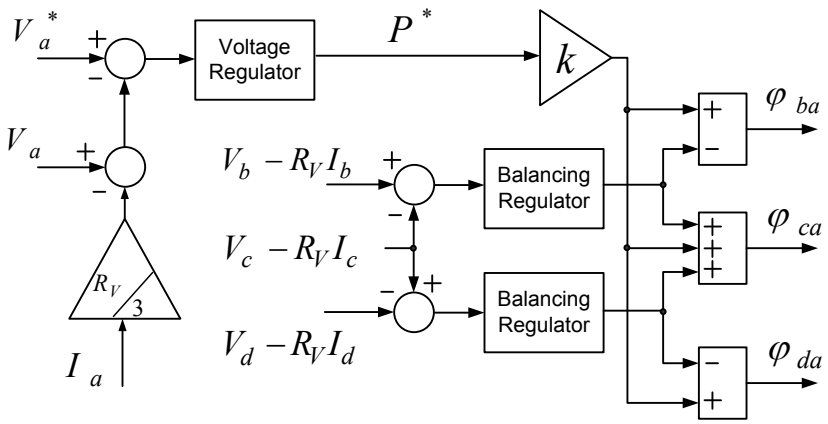

Figure 5. Balancing distributed controller for MV DC Links balancing

Secondary controls

One of the characteristic of the proposed architecture is that it is not necessary for the single cell to have the information of the complete topology. In order to get the maximum flexibility from this architecture, it is necessary that a power flow path exists between the MV DC Links.
Obviously, there are multiple degrees of freedom to perform this connection, and two examples are reported in Figure 6. Configuration (a) allows the minimum insulation requirements between the secondary windings of the HF transformer, while topology (b) features a greater interleaving between the CHB.
With the controls proposed in the previous chapter, the MV side expresses self-balancing capabilities as long as a path able to connect all the MV ports exists. It is assumed, that the control of the total MV side is realized by the MV AC converter, which can be modeled as controlled current sources connected to the MV DC Links. An example of this control is reported in Figure 7, where a PI regulator controls the sum of all the DC Link voltages and each AC cell process the same amount of power.
As a matter of fact, even with a highly asymmetrical architecture, like Figure 6a, if $P_1 > P_2$, the MV side can find a path to re-route the power and keep the cells balanced, as shown with arrows in Figure 8. The main problem is that this feature is achieved thanks to the virtual resistors that can lead to steady-state errors in the reference tracking. In order to limit these errors, the resistor value must be kept small. However, small virtual resistors could lead to circulating power in the case of voltage measure mismatch.
In this framework, it is better to choose a quite high value of virtual resistor, in order to make the system more robust to measurement error, and to employ secondary controls to cope with the steady-state error.
In the following, only the architecture of Figure 6b will be considered, since it exhibits better self-balancing capabilities. For this solution, the secondary controls are reported in Figure 9 and Figure 10 for the LV and MV side, respectively.
The secondary control for the LV side relies on a supervisor control that modifies the reference voltage of the QABs connected to the same LV DC link, in the same way with which DC micro-grids achieve the reference tracking [9].
The secondary control of the MV side has a different operating principle. In particular, it is based on the assumption that an imbalance in the MV is caused by the power routing effect of the modular DC/DC structure, which causes unbalanced voltages due to the drop over the virtual resistor. Since the principle of operations resides in the presence of this virtual resistor, its value will be kept constant in this paper, and the issue is addressed by modifying the control of the AC/DC stage. As a matter of fact, in a CHB converter, each cell is connected in series, so the current is the same for all cells. In balanced conditions, each CHB cells generates an equal part of the converter voltage. It has been shown in several works [10] that by modifying this voltage, the power sharing between the CHB cells can be affected, without essentially increasing the thermal stress of the power semiconductor (the current is the same for all modules). In this way, since the DC/DC converter already balances the MV side, the CHB can restore the power balance by modifying the power processed by each cell. This is modeled by applying different reference to the controlled current sources of Figure 7, and a voltage balancing regulator is used to generate these references, as shown in Figure 10. The basic principle of operations is that in the modular structure, there exists a direct branch between MV DC Link 2 (5) and LV DC Link 1 (2), so by measuring V_{DC2}^{MV} and V_{DC5}^{MV} the control can detect if the LV DC links are unbalanced, and can instruct the CHB to modify the power processing accordingly.

Simulation Results

The architecture of Figure 6b was simulated, and the simulation parameters are reported in Table 1.
Variable current sources connected to the LV DC Links are used to simulate the low-voltage inverters, which would presumably work in voltage-control mode. Controlled current sources are also used to emulate the CHB, which ensures equal input power to each MV cell and controls (with a PI regulator) the total MV DC voltage to 2400V, see Figure 7.

The simulation initial conditions are that an equal current is drawn by the LV DC Links. At time 0.1 s there is a current step, and reduced power is required by the first LV DC Link.
Two sets of simulations are performed, to show the benefits of the secondary controls applied to the structure.
When the secondary controls are not active, a small value of virtual resistor was chosen in order to limit the voltage error (0.5 Ω). Since there is a change between balanced and unbalanced conditions (as the CHB control imposes equal power to each cell, as can be seen in Figure 7), the power handled by the MV ports changes. The DC Links are well controlled, despite the power change, as shown in Figure 11.

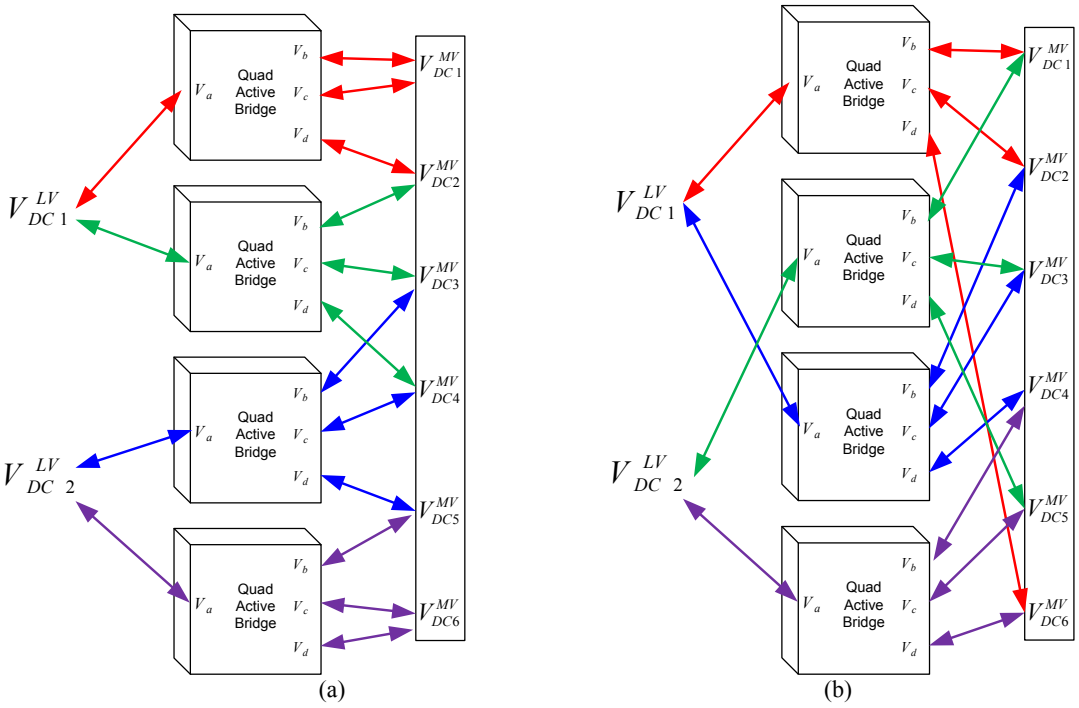

Figure 6. Architecture of the Power Transfer Block with two LV DC Link.

At time 0.2 s, a ±1% voltage measurement error is introduced in the QAB number 2, in order to show the robustness with respect to the normal accuracy levels that can be expected from the voltage sensors. The voltages are still well regulated (with an obvious increase of the steady state error), however, this comes at the expenses of the circulating power. The total circulating power is defined as the sum of the absolute values of the power processed by each QAB port. As a matter of fact, when each LV DC Link requires 10 kW of power, in ideal conditions 40 kW of total circulating power should be expected. As can be seen in Figure 11, when the voltage error is introduced, the circulating power rises from 36 kW (the correct value) to 38 kW, due to the small value of the virtual resistance.
On the other hand, when secondary controls are activated, greater values of virtual resistance can be chosen (3 Ω), the reference voltage is perfectly tracked and the measurement error does not cause any increase of the circulating power, see Figure 12.
For completeness, also the instantaneous power processed by each QAB port is reported in Figure 13 and Figure 14 for the two cases.

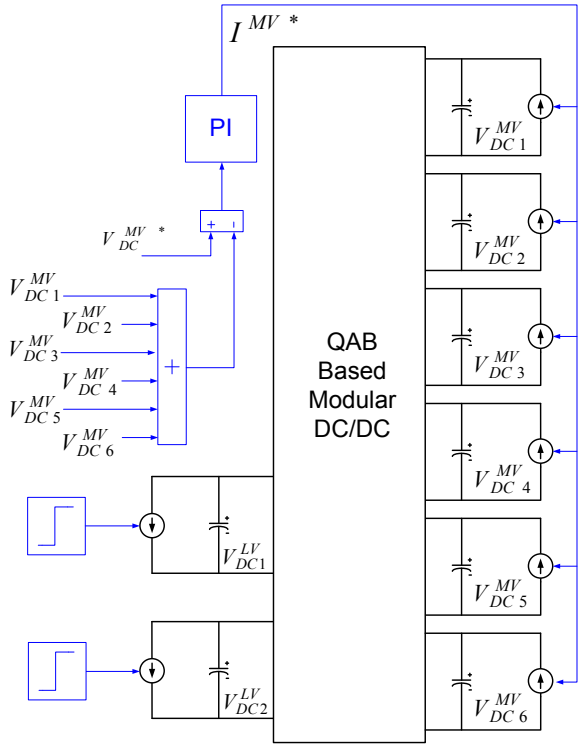

Figure 7. Block scheme of the MV control

$$\begin{cases} P_b = \dfrac{V_b}{2\pi f_s L_{lk}} \left(\begin{matrix} V_a\varphi_{ba}\left(1-\dfrac{\varphi_{ba}}{\pi}\right) + V_c\varphi_{bc}\left(1-\dfrac{\varphi_{bc}}{\pi}\right) \\ +V_d\varphi_{bd}\left(1-\dfrac{\varphi_{bd}}{\pi}\right) \end{matrix} \right) \\ P_c = \dfrac{V_c}{2\pi f_s L_{lk}} \left(\begin{matrix} V_a\varphi_{ca}\left(1-\dfrac{\varphi_{ca}}{\pi}\right) + V_b\varphi_{cb}\left(1-\dfrac{\varphi_{cb}}{\pi}\right) \\ +V_d\varphi_{cd}\left(1-\dfrac{\varphi_{cd}}{\pi}\right) \end{matrix} \right) \\ P_d = \dfrac{V_d}{2\pi f_s L_{lk}} \left(\begin{matrix} V_a\varphi_{da}\left(1-\dfrac{\varphi_{da}}{\pi}\right) + V_b\varphi_{db}\left(1-\dfrac{\varphi_{db}}{\pi}\right) \\ +V_c\varphi_{dc}\left(1-\dfrac{\varphi_{dc}}{\pi}\right) \end{matrix} \right) \end{cases}$$

Equations of the QAB.

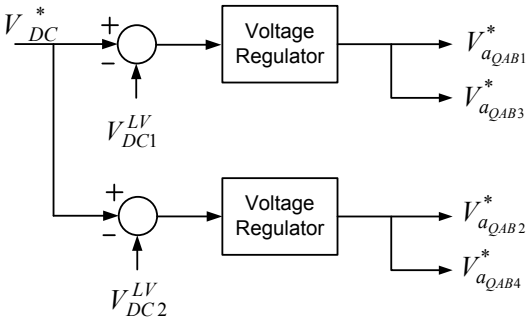

Figure 9. Block scheme of the secondary control for the LV side

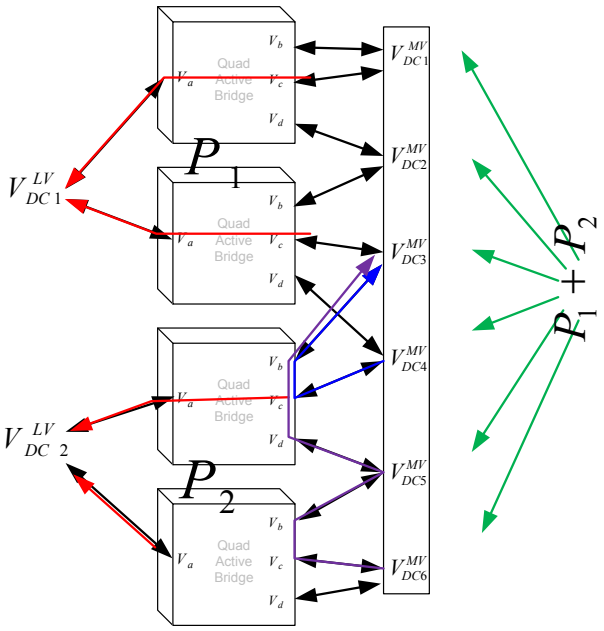

Figure 8. Power transfer between the QAB in the case of unbalanced LV DC Links.

Table 1. Simulation Parameters

Parameter	Value
f_s	$40\ kHz$
C_{DC}	$330\ \mu F$
L_{lk}	$50\ \mu H$
V^*_{DC1}	$400\ V$
R_V (no sec. contr.)	$0.5\ \Omega$
R_V (with sec. contr.)	$3\ \Omega$
P_1	$10\ kW$
P_2	$10 \rightarrow 8\ kW$

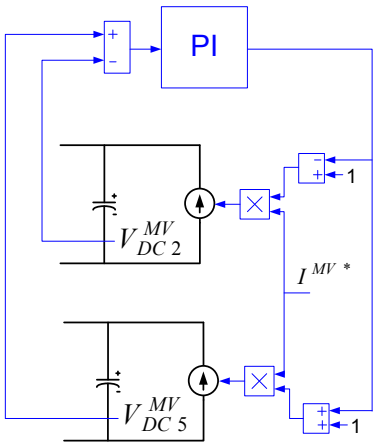

Figure 10. Balancing control of the MV side

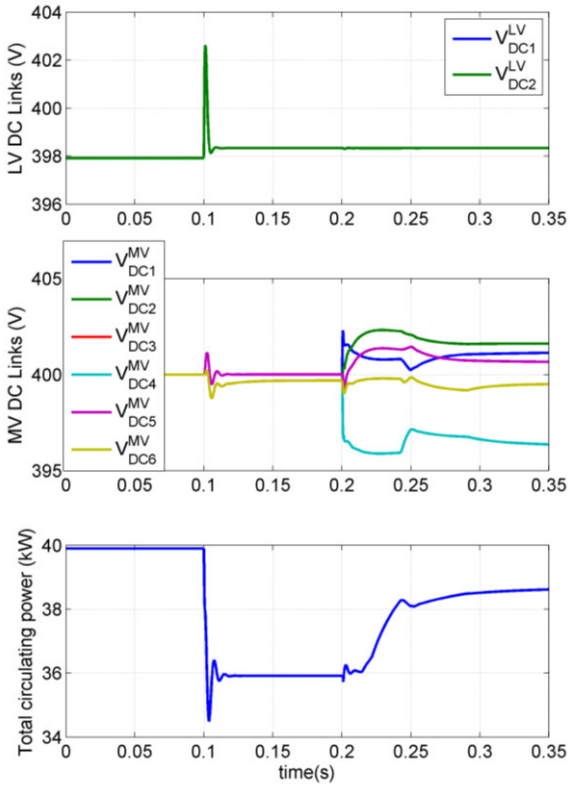

Figure 11. DC Link voltage and circulating power (no secondary controls)

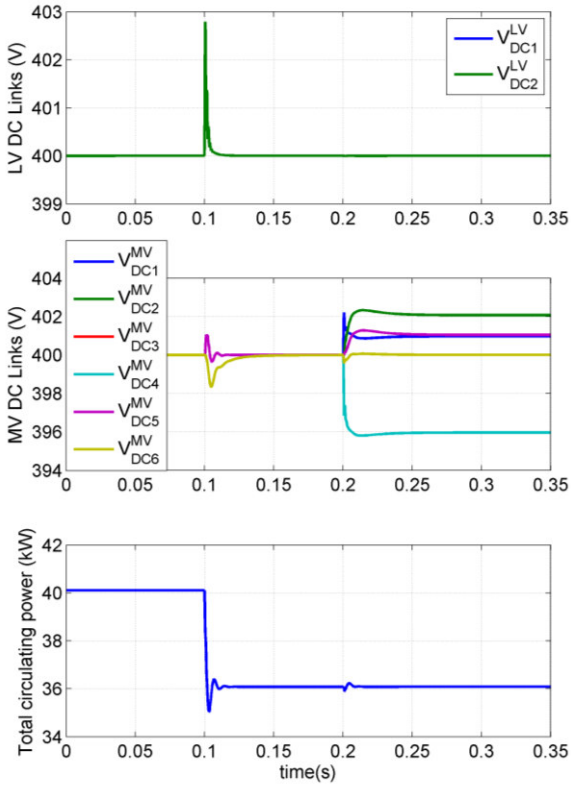

Figure 12. DC Link voltage and circulating power (with secondary controls)

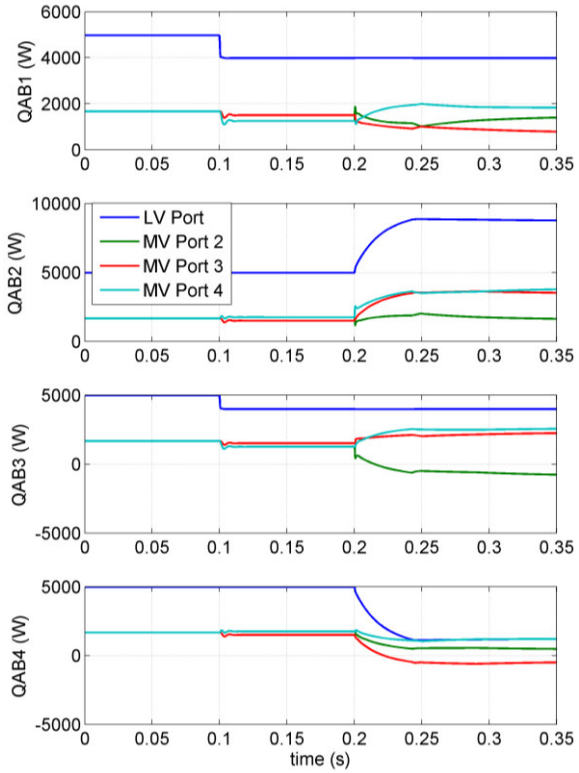

Figure 13. Power processed by the ports of the QAB (no secondary controls)

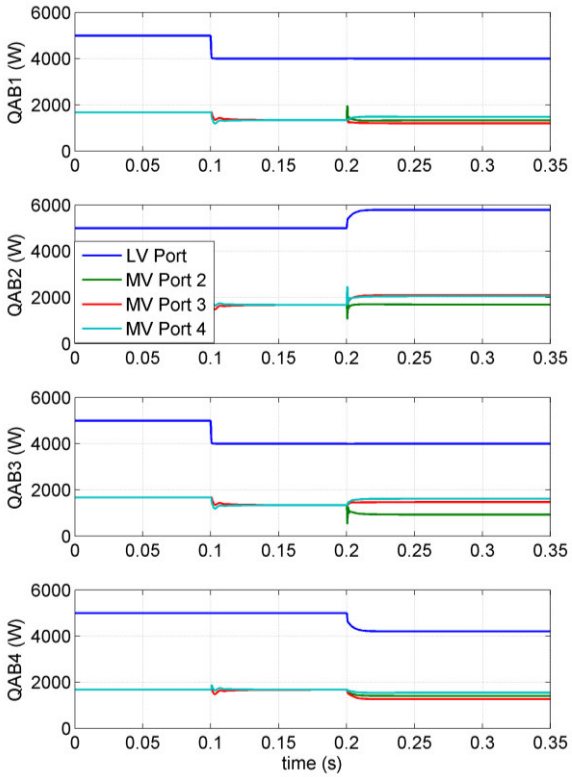

Figure 14. Power processed by the ports of the QAB (with secondary controls)

Experimental results

In order to realize a preliminary testing, a prototype of a QAB was developed. Four H-bridges are embedded in the board (with the possibility to choose semiconductors with greater power rating for the primary side). A DSP Freescale MPC5643L realizes the phase shifted gate signals at 40 kHz and the control shown in Figure 5.
Since only one QAB is present, the controls were tested by connecting a power supply to the primary H-bridge and a resistive load to the three secondary ports connected in parallel to a resistor of 130 Ω. The goal of this test is to show that the currents can be equally shared by the secondary ports and the converter can operate in soft-switching conditions. The experimental configuration schematic is presented in Figure 15, where are also highlighted the voltages and the current measured for the experiments. A 5 Ω virtual resistor was implemented in the controller.

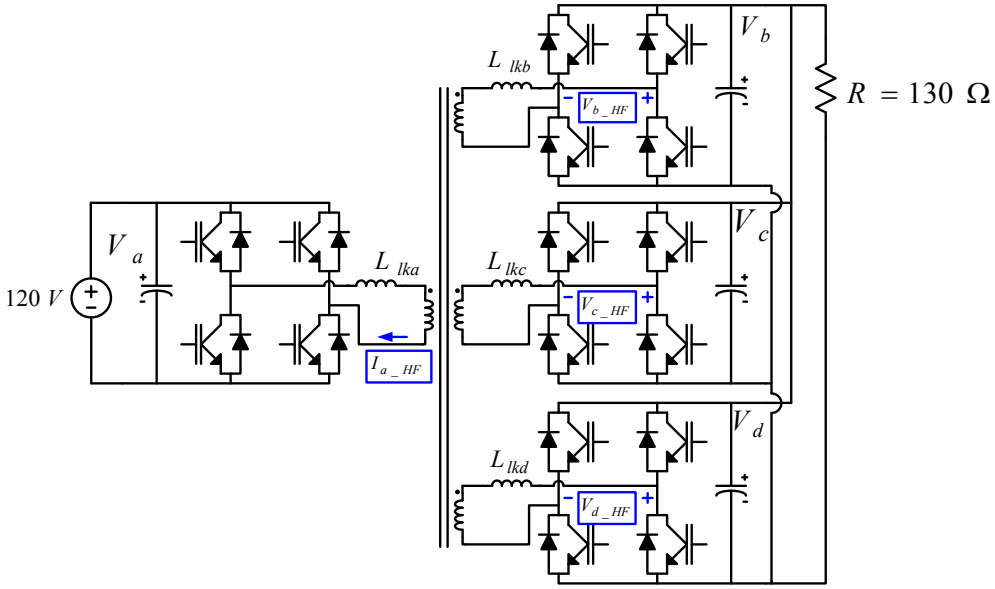

Figure 15. Experimental test configuration

The prototype converter is shown in Figure 16, and the experimental waveforms are presented in Figure 17. The output voltages are at 120V, and the converter is operating in soft-switching conditions (unity voltage ratio).
Also the load current is shared equally among the cells, with a maximum imbalance of 10 mA.

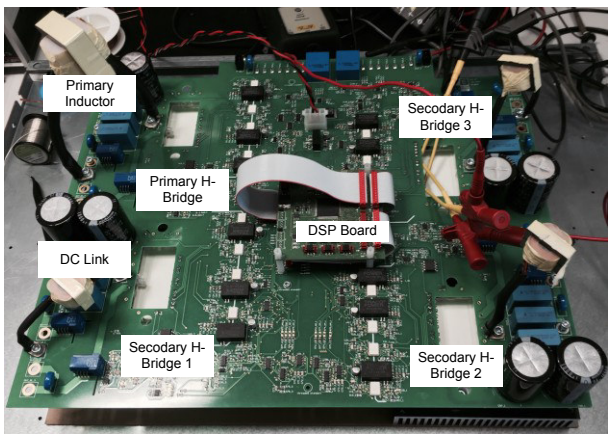

Figure 16. Picture of the QAB prototype

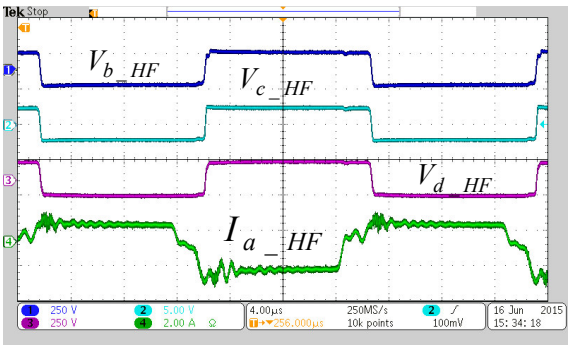

Figure 17. Experimental results

Conclusion

This paper proposes a modular architecture for a multi-port DC/DC stage suitable for medium voltage applications. In particular, this converter can be employed as the DC/DC stage for a smart transformer. The key characteristic is to employ QABs as building block, and to embed a decentralized control at cell level. With simulations, it was shown that this control is able to self-regulate the power flow in the architecture even in the case of unbalanced power absorption at the different ports. Secondary voltage controls were also proposed with the double aim of improving the reference tracking capabilities and the robustness to voltage errors.

References

[1] R. Lasseter, P. Paigi. "Microgrid: a conceptual solution." Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual. Vol. 6. IEEE, 2004.

[2] H. Abu-Rub, M. Malinowski, K. Al-Haddad, Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications, John Wiley & Sons, 2014.

[3] Xu She, A.Q Huang, R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol.1, no.3, pp.186,198, Sept. 2013.

[4] G. De Carne, M. Liserre, K. Christakou, M. Paolone, "Integrated Voltage Control and Line Congestion Management in Active Distribution Networks by Means of Smart Transformers", IEEE International Symposium on Industrial Electronics (ISIE) 2014, 1-4 June 2014.

[5] G. Buticchi, D. Barater, L. Tarisciotti, P. Zanchetta, "A simple deadbeat current control for single-phase transformerless inverters with LCL filter", IEEE Energy Conversion Congress and Exposition (ECCE), 2013, pp.4214,4220, 15-19 Sept. 2013.

[6] G. G. Oggier, Go. O. Garcia, A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-DC converter under soft switching in the whole operating range", IEEE Transactions on Power Electronics, vol.26, no.4, pp.1228,1236, April 2011.

[7] Huai Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J.B. Jacobsen, T. Kvisgaard, J. Landkildehus", Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol.2, no.1, pp.97,114, March 2014.

[8] S. Falcones, R. Ayyanar, Xiaolin Mao, "A DC–DC Multiport-Converter-Based Solid-State Transformer Integrating Distributed Generation and Storage", IEEE Transactions on Power Electronics, vol.28, no.5, pp.2192,2203, May 2013.

[9] Lu Xiaonan, J. M. Guerrero, Kai Sun, J. C. Vasquez, "An Improved Droop Control Method for DC Microgrids Based on Low Bandwidth Communication With DC Bus Voltage Restoration and Enhanced Current Sharing Accuracy", IEEE Transactions on Power Electronics, vol.29, no.4, pp.1800,1812, April 2014.

[10] L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, J. C. Clare, P. W. Wheeler, "Active DC Voltage Balancing PWM Technique for High-Power Cascaded Multilevel Converters", IEEE Transactions on Industrial Electronics, vol.61, no.11, pp.6157,6167, Nov. 2014