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Power-Hardware-In-Loop harmonic analysis of a Smart Transformer-fed distribution grid

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Abstract—The Smart Transformer (ST) offers ancillary services in the low voltage grids. These new services in a real distribution grid can be demonstrated by means of simulation software, but it is difficult to prove them in lab due to the complexity and heterogeneity of the distribution grids. The Power-Hardware-In-Loop (PHIL) evaluation is an interesting solution for emulating the interaction between the real grid, simulated in a Real Time Digital Simulator (RTDS), and the ST. However the PHIL evaluation requires careful analysis. Depending on the interface topology the stability and the accuracy of the loop can be affected. This is mostly true when the interface converter is not a linear power amplifier, but just a simple DC/AC switching converter. Actually, no considerations have been made in the literature about the accuracy and stability of the PHIL in case of non-linear interface converter.

This paper focuses on evaluating the harmonic behavior of the PHIL in case of current harmonic content in the grid. Depending on the bandwidth of the interface converter, the accuracy of the PHIL in simulating harmonic currents can be affected. The analytical considerations on the accuracy of the loop have been verified experimentally in a complex LV grid.

I. INTRODUCTION

The Smart Transformer (ST) represents an enabling technology for the grid of the future. The ST, a power electronics-based transformer [1], [2], aims not only at substituting the traditional Low Voltage (LV)/Medium Voltage (MV) transformer, but also at providing new services to the grid. The ST allows the voltage and current control in MV [3] and LV grids [4], harmonic compensation [5], load identification and control by means of frequency and voltage variations in LV grids [6][7][8]. In order to show the ST features in realistic conditions, the implementation in a test distribution grid is needed. However the simple simulation of ST in software environment may lead to not realistic results due to the models adopted, meanwhile the ST hardware test in a research lab with realistic LV grids results be unpractical due to the grid size and complexity.

In this regard the Power-Hardware-In-Loop (PHIL) simulation by means of a Real Time Digital Simulator (RTDS) system offers new opportunities for hardware testing [9], [10], [11], [12]. With respect to the classical Hardware-In-Loop (HIL) simulations, used for testing controllers and relays, the PHIL simulation allows to analyze the impact on the grid of

the hardware under test using a scaled model connected to the RTDS by means of an interface converter. This feature increases the number of available tests and enables the hardware test without affecting the real grid.

Despite the many advantages that the PHIL has, its implementation is difficult and the stability and accuracy of the loop must be studied in order to replicate accurately the behavior of the simulated grid in the hardware setup. The accuracy of the interface converter is related to the capacity of the converter to follow the reference signals sent by RTDS, keeping the system stable without any resonant or unstable behavior. The stability and accuracy of the loop depend on the chosen interface algorithm between software and hardware and on the interface converter [9], [10], [13]. The interface algorithm must be tailored to the application of the PHIL and incorrect tuning may lead to hardware behavior, which is not consistent with the RTDS simulation.

This paper is focused on the accuracy of the interface converter when a harmonic content is present in a ST-fed distribution grid. The interface converter analyzed is realized with commercial products (Danfoss FC302 converters) and its proper tuning allows an accurate representation of the RTDS simulation with harmonic content. It results in a tradeoff between accuracy at high frequency and stability of the loop. This paper analyzes mathematically the stability and accuracy of the PHIL and then proves it by means PHIL evaluation with several current harmonic content.

The paper is structured as follows: section II depicts the PHIL setup, the interface method implemented and the tuning of the interface converter focusing on the stability and accuracy of the loop; section III describes the grid used in this work; section IV shows the experimental results obtained performing the PHIL evaluation; eventually section V is dedicated to the conclusions.

II. PHIL SETUP

The PHIL facility realized in lab is composed by 4 parts: the Hardware under Test (HuT) (the LV side of the ST), the RTDS, the interface-converter and the two control stations (with RSCAD and dSPACE). The hardware setup is composed

of Danfoss FC302 converters with custom interface cards, controlled by a dSPACE DS1103.

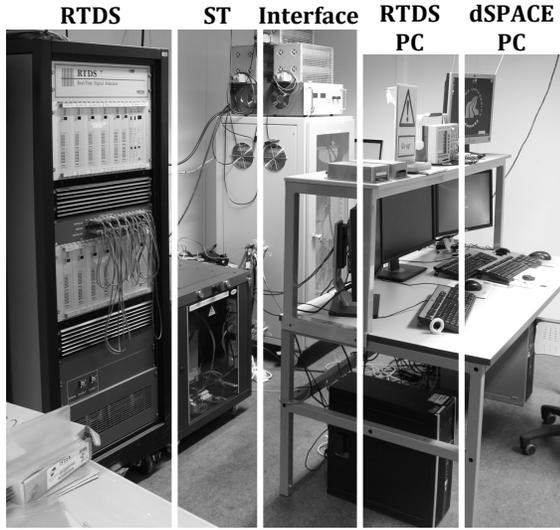


Figure 1: Laboratory setup

A. Hardware under Test: ST

The hardware investigated in this paper is the ST, a three-phase Voltage Source Converter (VSC) that controls the voltage in the LV grid. The ST control, implemented in dq coordinate system, is shown in Figure 2: an outer voltage control loop, implemented with PI controller, gives the reference for the inner current loop, whose output is the converter's duty cycle. Here, the ST setup parameters are listed in Table I and the open loop bode diagram in case of a 2 kW load with power factor equal to 0.9 p.u. are shown in Figure 3; in the PHIL realized in lab, this operation point corresponds to 600 kW grid simulated in RTDS.

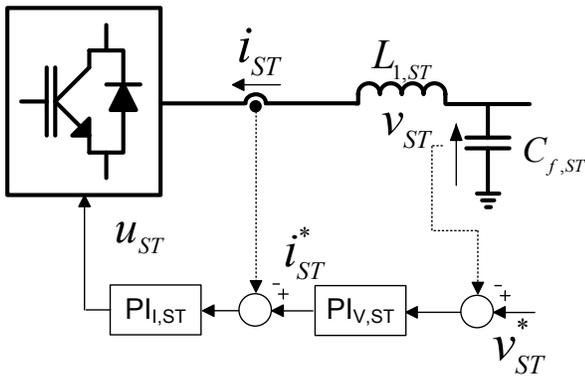


Figure 2: ST control scheme

B. Interface method: power-type Ideal Transformer Method

In this paper the PHIL has been realized by means of a power-type ITM interface algorithm, that derives from a modified version of the current-type ITM described in [13].

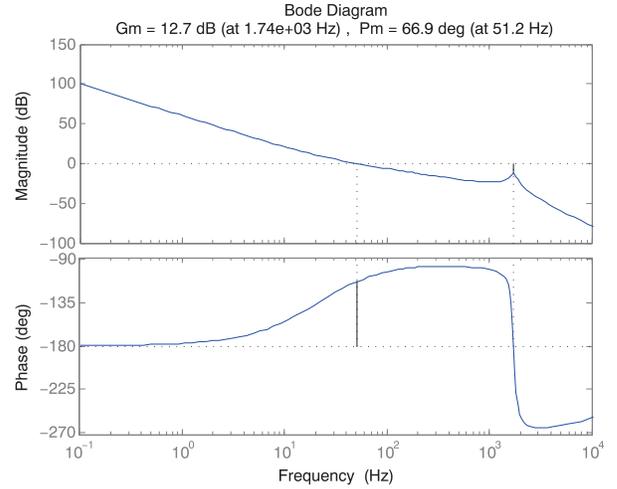


Figure 3: ST voltage open loop transfer function with a 2 kW load

Table I: ST parameters

Parameter	Value	Parameter	Value
S	8 kVA	$Kp_{V,ST}$	0.05
f_{sw}	10 kHz	$Ti_{V,ST}$	0.001
$L_{1,ST}$	1.8 mH	$Kp_{I,ST}$	1.5
$C_{f,ST}$	4.7 μ F	$Ti_{I,ST}$	0.0075

The RTDS transmits to the ST the active and reactive powers instead of the current signals as shown in Figure 4. In RSCAD, the RTDS simulation software, the instantaneous active and reactive powers are calculated at the ST bus and sent as scaled-down current references for the current controller of the interface converter. The ST imposes the voltage waveforms and provides the current requested by the interface converter. The power generated by the ST is equal to the power requested by the interface converter (the references coming from the RTDS) plus the losses generated in the setup. Eventually, the ST voltage is measured at the LC filter capacitor level and sent back to the RTDS, where a voltage source replicates the behavior of the hardware in the software side. In this way the loop is closed and any effect generated in the software are reproduced in the hardware and vice versa.

C. Interface tuning

The proper tuning of the interface converter is fundamental in order to represent accurately in hardware what simulated in RTDS. However, the tuning is usually a tradeoff between stability and accuracy of the loop. As analyzed mathematically in this section and verified experimentally in the Section IV, increasing the bandwidth of the interface converter, the PHIL represents correctly the harmonic content in the grid, though reducing the stability of the loop.

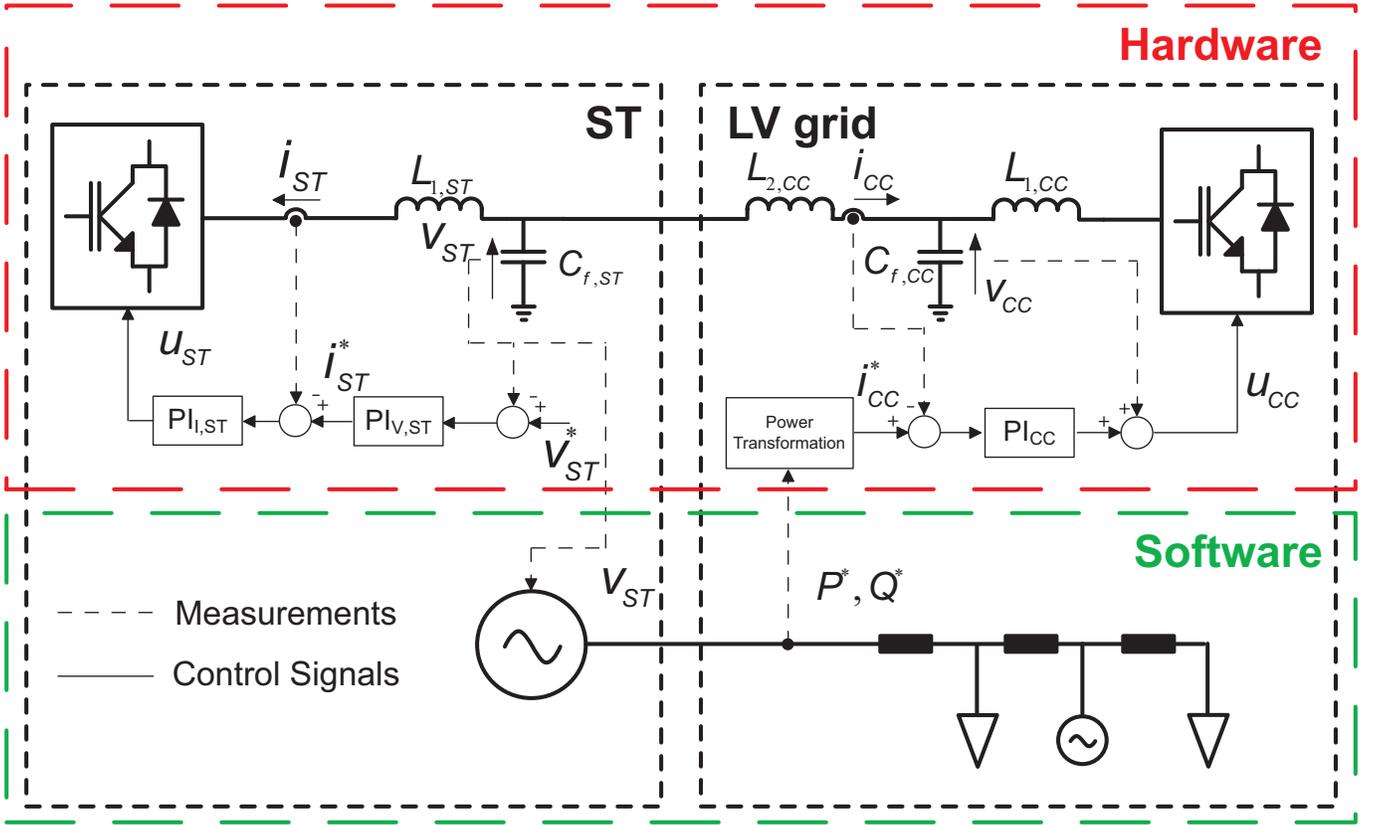


Figure 4: PHIL: Hardware system (red frame), simulated system (green frame).

The PHIL system described in Figure 4 can be represented mathematically as in Figure 5, where $G_{V,ST}(s)$ is the voltage controller of ST, $G_{I,ST}(s)$ the current controller of ST plus the converter delay, $LC(s)$ the ST LC filter transfer function, $RTDS(s)$ the grid transfer function, $G_{I,int}(s)$ the current controller of the interface converter plus the converter delay, and $LCL(s)$ the interface converter LCL filter transfer function. The parameters of the interface converter can be found in in Table II.

Table II: Interface converter parameters

Parameter	Value	Parameter	Value
S	8 kVA	$L_{2,CC}$	1.6 mH
f_{sw}	10 kHz	$C_{f,CC}$	4.7 μ F
$L_{1,CC}$	1.8 mH		

Two main approximations have been made in this representation: 1) the grid simulated in RTDS is evaluated as a static gain K equal to one, emulating the variation of the consumed load power varying the ST voltage; 2) the reference current i_{int}^* has been obtained by means of linearization of the division between the power and the voltage. Following the aforementioned assumptions the system can be described by the transfer function

$$\frac{v_{ST}^*(s)}{v_{ST}(s)} = \frac{G_{V,ST}(s)G_{I,loop}(s)}{1 + G_{V,ST}(s)G_{I,loop}(s)} \quad (1)$$

where

$$G_{I,loop}(s) = \frac{G_{I,ol}(s)}{1 + G_{I,ol}(s)G_{int}(s)Ke^{-2sT_s}} \quad (2)$$

$$G_{int}(s) = \frac{G_{I,int}(s)LCL(s)}{1 + G_{I,int}(s)LCL(s)} \quad (3)$$

$$G_{I,ol}(s) = G_{I,ST}(s)LC(s) \quad (4)$$

In order to evaluate the stability of the PHIL system, the interface converter bandwidth has been increased, incrementing linearly the gain Kp_{CC} , as shown in Figure 6. As can be noticed, a low bandwidth results fundamental for achieving a stable behavior of the PHIL. However, the capacity to simulate correctly frequency higher than the nominal one depends strongly on the bandwidth of the interface converter itself. A low bandwidth leads to incorrect results also at low frequency, as can be seen from the close loop Bode diagram in Figure 7 (blue line, 80 Hz peak). Summarizing, higher interface controller gains are preferred in order to simulate higher frequency behavior, although it can affect the stability of the loop. A tradeoff must be found in order to have accurate results without affecting the stability of the loop.

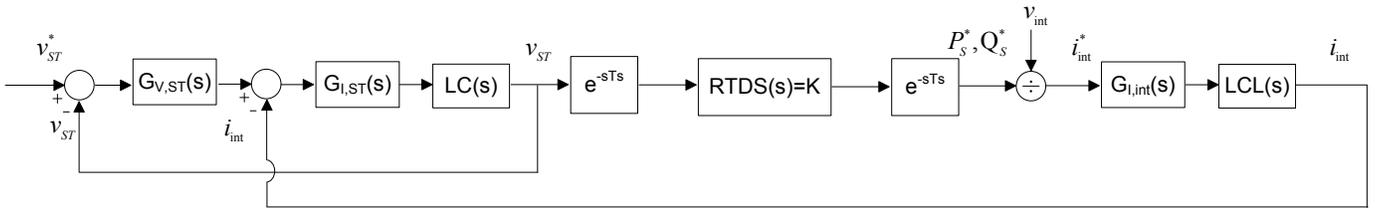


Figure 5: Transfer function representation of the PHIL

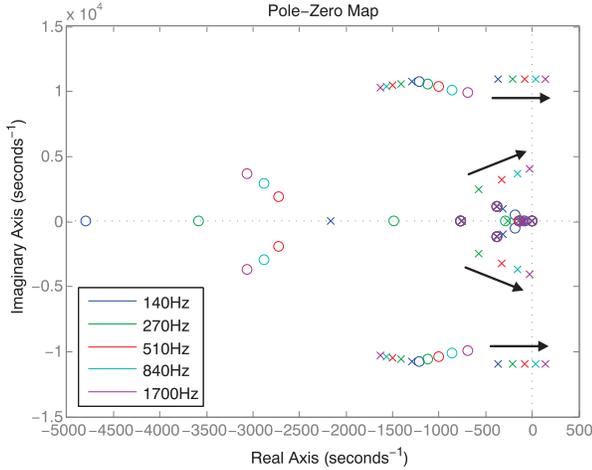


Figure 6: Stability and accuracy analysis: pole-zero map of the PHIL increasing the proportional gain K_{pCC} of the interface converter.

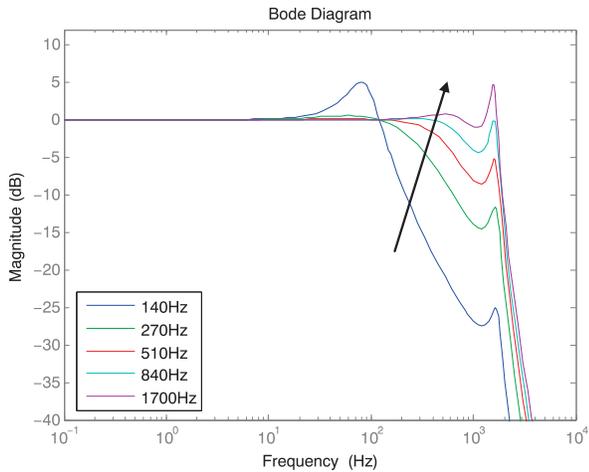


Figure 7: Stability and accuracy analysis: interface converter close loop transfer function increasing the proportional gain K_{pCC}

III. DESCRIPTION OF THE TEST GRID

The LV grid implemented in RTDS is a modified version of the CIGRE European LV distribution network benchmark described in [14] and depicted in Figure 8. The grid has been simulated with a time step of $50\mu s$, typical of the PHIL

applications [9], [10], [13]. The CIGRE grid has been modified with respect to the benchmark one: 1) the three-phase loads have been simulated with a constant impedance model and balanced, being the converters used three-phase three-wires; 2) the Distributed Energy Resources (DER), that are the Battery Energy Storage Systems (BESSs) and the photovoltaic plants, operate with a fixed unity power factor and without any droop control; 3) the wind turbine has been removed for reducing the calculation effort in RTDS; 4) a variable frequency current source has been added in bus 13 in order to introduce harmonic content in the current profile. The loads and DER data are listed in Table III

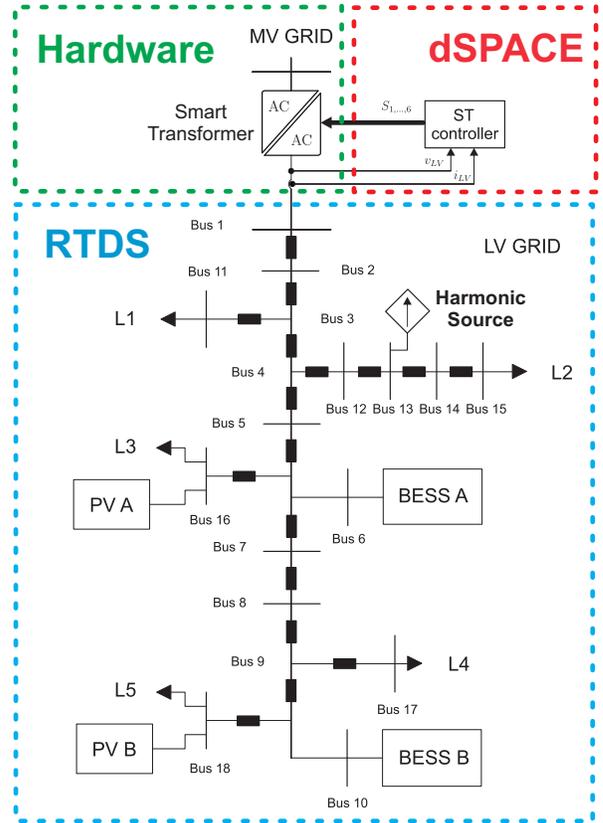


Figure 8: Modified CIGRE European LV distribution network benchmark implemented in RSCAD

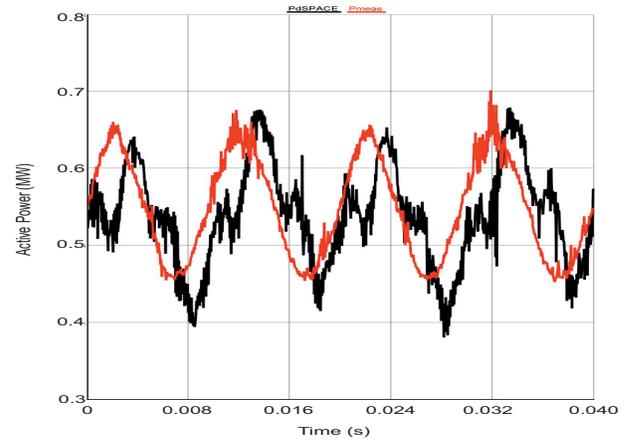
Table III: Load and DER data

Load	Bus	Apparent Power (kVA)	cos ϕ
L1	11	5.7	0.85
L2	15	19.2	0.85
L3	16	19.2	0.85
L4	17	2.7	0.85
L5	18	8.8	0.85
DER	Bus	Apparent Power (kVA)	cos ϕ
BESS A	6	75	1.00
BESS B	10	25	1.00
PV A	16	4	1.00
PV B	18	3	1.00

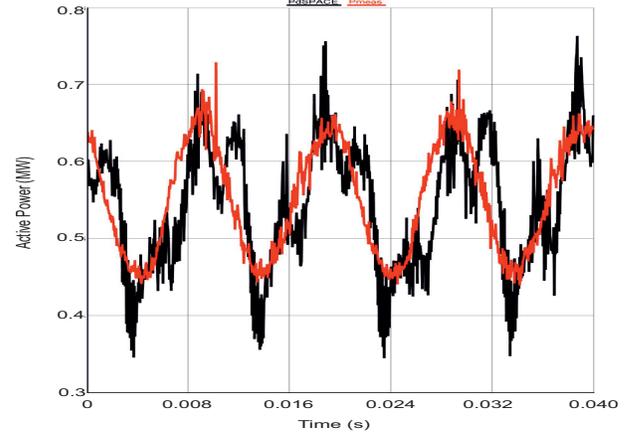
IV. EXPERIMENTAL RESULTS

In order to verify the capability to represent correctly the harmonic content of the PHIL setup, a direct-sequence three-phase 150 Hz harmonic current has been demanded by the harmonic source at bus 13. The amplitude of this current is 100 A in the RTDS, corresponding to 300 mA in the setup. The direct-sequence 150 Hz current has been chosen due to the absence of the 3rd harmonic in the system, being an ungrounded three-phase three-wires converters. The load has been increased to 5 times, in order to increase the stress on the interface converter. The capability of the interface converter to replicate the RTDS power (red lines) in the hardware side (black lines) has been shown in Figure 9 with two different bandwidths: in Figure 9a the bandwidth has been set to 270 Hz (green line in Figure 7); in Figure 9b the bandwidth has been set to 710 Hz, last value that keeps the system stable. The power has a 2nd harmonic component created by the interaction between the 1st voltage harmonic and the 3rd direct sequence current. As can be noticed, the system with lower bandwidth follows the 2nd harmonic reference with a delay (quantified here in 1 – 2 ms) and with lower amplitude, impacting on the accuracy of the PHIL. In the case of higher bandwidth (Figure 9b), the interface converter can follow the 2nd harmonic power reference created by RTDS and without any delay. In the 710 Hz case the phase A current scope waveform (green line) and its online FFT (red line) have been plotted in Figure 10. In this case, the 150 Hz amplitude has been respected ($i_{int,3rd}^* = 300$ mA). It can be concluded that a bandwidth of 710 Hz is sufficient to represent the 150 Hz current harmonic content simulated in RTDS, keeping the PHIL stable.

To verify the limit of the harmonics representation in PHIL with the proposed setup, the frequency of the current absorbed by the harmonic source has been increased to 450 Hz. The phase A current scope waveform (green line) and its online FFT (red line) have been plotted in Figure 11. As can be noticed, the reference current $i_{int,9th}^* = 300$ mA is not respected, and the current amplitude is lower than the reference. This behavior confirms the transfer function representation in Figure 4. It can be observed in Figure 7 that the current at higher frequencies is damped and only an higher interface converter bandwidth permits to replicate correctly the harmonic behav-



(a) Bandwidth 270 Hz.



(b) Bandwidth 710 Hz.

Figure 9: Injection of 150 Hz current: RTDS active power (red line) and interface converter active power (black line).

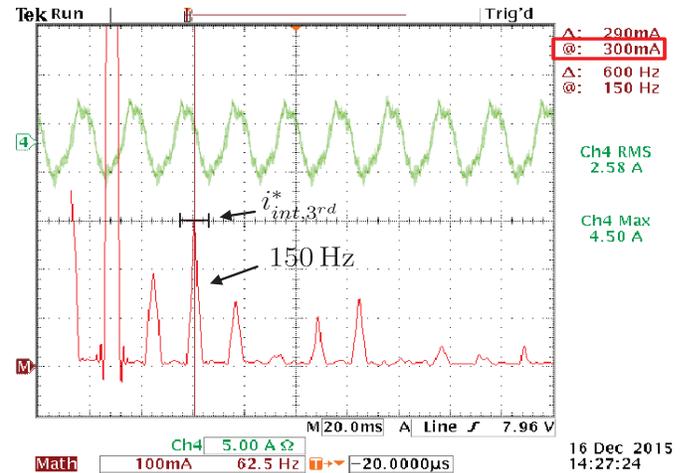


Figure 10: Injection of 150 Hz current: Phase A current (green line) and its online FFT (red line) in case of bandwidth equal to 710 Hz.

