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Giusi Quartarone
Marco Liserre
Friedrich Fuchs
Norma Anglani
Giampaolo Buticchi

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Impact of the modularity on the efficiency of Smart Transformer solutions

Giusi Quartarone*, Marco Liserre*, Friedrich Fuchs* Norma Anglani [†] and Giampaolo Buticchi *
*Chair of Power Electronics
Christian-Albrechts University of Kiel, Germany,
Email: {giqu@tf.uni-kiel.de, ml@tf.uni-kiel.de, fwf@tf.uni-kiel.de, gibu@tf.uni-kiel.de}
[†]Dipartimento di Ingegneria Industriale e dell'Informazione
University of Pavia, Italy,
Email: nanglani@unipv.it

Abstract—Due to the possibility to drastically reduce the Solid State Transformer (SST) volume and weight, its use is becoming a reality in traction and wind power plant applications, while, in the electric distribution system, it is still considered futuristic. A SST, with managerial role in the electric distribution grid, is generally called Smart Transformer (ST). Unfortunately the low efficiency, the low reliability and the high cost still act as barriers for its widespread use in the real world. This paper focuses on the impact of a modular design, by benchmarking different ST topologies. Moreover, the paper provides guidelines on how to choose the semiconductor modules and assessments on how the choice affects the efficiency of the ST.

I. INTRODUCTION

Due to important changes in the electric grid, the traditional transformer is no more suitable to cover its role. The increasing penetration of distributed renewable energy sources, along with energy storage systems and electric vehicles have completely changed the electric distribution grid, which needs to better manage bi-directional power flows. This made the traditional grid components, such as transformers, less and less suitable to cover the actual requirements. Thus, new kind of transformers and voltage regulators would need to be installed throughout the grid, at both distribution and substation level. Besides, because of higher penetration of off-shore wind power plants, the distribution using DC level is becoming more and more attractive in terms of efficiency, as no reactive power is generated/consumed by the transmission cable. For such reasons the idea to replace the conventional transformer is becoming attractive. One of the possible candidate is the Solid State Transformer (SST) that has been defined as one of the 10 most emerging technologies by Massachusetts Institute of Technology (MIT) in 2011 [1].
The SST is a power electronic device that replaces the traditional 50/60 Hz power transformer by means of a high frequency isolated AC-AC transformer and power converters. The basic operation of the SST is firstly to change the 50/60 Hz AC voltage to a high frequency one (normally in the range of few kHz to tens of kHz), then this high frequency voltage is stepped up/down by a high frequency transformer and finally shaped back into the desired 50/60 Hz to feed the load. Additionally, the SST will provide new functionalities with respect to a traditional transformer, such as:

- to protect the medium voltage distribution system from load disturbances, transient and voltage sags;
- to enhance the power quality by balancing the load of the medium voltage distribution system and providing unity power factor (or controllable reactive power) with sinusoidal currents under non-linear loads;
- to accept direct connection to future MVDC power transmission, low voltage DC grid, storage systems and renewable energy systems;
- to be robust and fault-tolerant, by the means of a modular design approach that can increase the availability by reducing the outages.

With the switching frequency at 10's of kHz, the transformer size can be much smaller than the conventional one. Thus there is a clear interest in developing such systems in various applications where space and weight restrictions are critical items like in railway traction and in offshore renewable power generation. The railway electrical traction sector is currently the most important one, being SST prototypes already under testing [2].

One of the drawbacks of the SST is its low efficiency, if compared with the conventional transformer's one. Nonetheless, a slightly lower efficiency (in the order of 97-98%) could be accepted if the additional functionalities are considered. For this reason, part of the research in this field is focused on proposing new power conversion architectures and power devices to improve the efficiency. In [3] and [4] new SST design topologies are presented, aiming to implement new functionalities, with acceptable efficiencies.

In this paper the semiconductor losses for different SST topologies are calculated, by showing the importance of a proper semiconductor choice in the design of SSTs. Even though several works focused the attention on how to improve the SST design, as far as the authors know, no systematic research showing the role of the semiconductor choice on the SST efficiency has ever been performed. This is pursued under the assumption of not considering the power losses in passive components (inductors and capacitors).

All the analyzed topologies have a rated power of $1\ MVA$. In Section II a brief introduction on the possible SST architectures is proposed, while, in Section III, the converter cells are
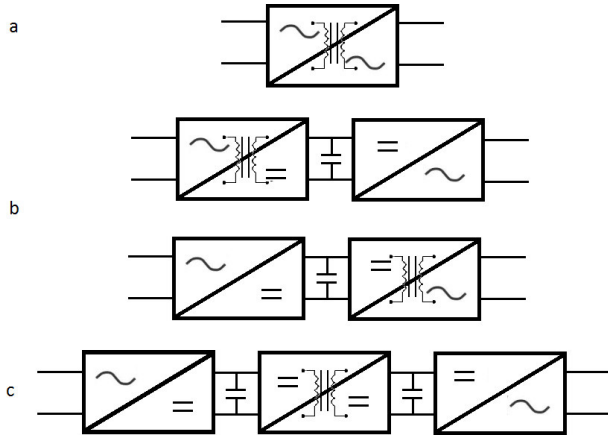
Figure 1: Possible architectures for Solid State Transformer. (a) one-stage SST ; (b) two-stage SSTs with a DC link respectively in low and medium voltage side; (c) three-stage SST.

described, along with their semiconductor losses. Finally, in Section IV, the considered SST topologies are analyzed and compared.

II. SST ARCHITECTURE

According to [5], three main SST architectures can be defined depending on the number of conversion stages (see Figure 1). Each stage is made up of one or more converters performing the proper conversion. The power converter cells can include a three phase converter or three single phase converters.

The *one-stage* SST (see Figure 1-a) performs a direct AC/AC conversion. It does not allow any DC connection like energy storage or local renewable DC energy sources. Moreover, the disturbances on one side can affect the other one. The one-stage transformer is inexpensive, if compared with the other two architectures, and it has a reduced number of components.

The *two-stage* SST is obtained with an AC/DC and a DC/AC conversion. It has a DC link in medium or low voltage side allowing the integration of DC sources or loads: the reactive power compensation is possible if suitable topologies are chosen. The medium frequency transformer can be placed both in the medium as well as in the low voltage side (Figure 1-b). The one and two stage topologies are not suitable for high voltage operation being the zero-voltage-switching (ZVS) hard to guarantee: to reduce the switching losses, a reduction of the switching frequency could be necessary.

In Figure 1-c, a *three-stage* SST is reported. It has DC links in both sides. It is characterized by an AC/DC conversion in the medium voltage side, an isolated DC/DC conversion and finally a DC/AC conversion in the low voltage side. This architecture is characterized by all the above mentioned features.

The choice of the architecture depends on the specific application. In [3] the authors show the advantages/disadvantages of different architectures, presenting some possible topologies. In the distribution system, where the penetration of renewable energy power plants and high power domestic loads (both in AC and in DC) is increasing, the use of a three-stage architecture is preferred. According to that, it was adopted by the main research groups and companies developing SSTs for distribution like FREEDM [6], UNIFLEX-PM [7], EPRI [8] and GE [9].

In [4] the authors focus their attention on three-stage SST, analyzing the semiconductor losses of different topologies. In the following, the topologies proposed in [4] are considered. The additional contribution provided by this paper is to offer a detailed comparison of topologies and devices. In the next sections only the three-stages architecture will be considered.

III. POWER CONVERTER CELLS FOR SST AND SEMICONDUCTOR LOSSES MODELS

The selection of an appropriate configuration is fundamental to accomplish the system requirements. In the following, the converters analyzed in this work are described along with their semiconductor losses.

A. Converter cells

A solid state transformer is made up of a medium frequency transformer, considered as being loss-less in this paper, and converter cells that properly convert the electric features. Below, the analyzed converters are briefly introduced.

1) AC/DC converters: multilevel converters are well suited to high-power medium-voltage applications. In fact, they produce an output voltage with higher number of levels: this reduces the semiconductor stress (supporting a smaller inverse voltage) and it improves the quality spectra compared with the two-level converters. This latter advantage allows the usage of smaller filter components.
The number of levels grows according to the number of series-connected modules in the converter. Nowadays, the most used multilevel converters are the Neutral Point Clamped (NPC) and the Cascaded H-Bridge (CHB). The three-level NPC and the CHB were chosen to implement the AC/DC conversion in the medium voltage side.

2) DC/DC converter: in this study, the only implemented DC/DC converter is the one phase Dual Active Bridge (DAB), being especially suitable highly modular and high power solutions. As reported in Figure 2, it consists of two H-bridges connected by a high-frequency transformer.
The DAB topology can work efficiently when all the switch-
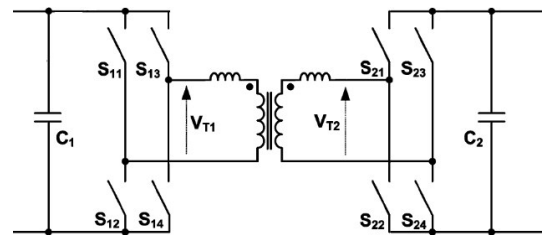

Figure 2: Dual Active Bridge converter

ing devices operate under zero-voltage switching (ZVS). In fact, by suitably controlling the DAB, it can work in soft-switching mode, reducing its switching losses drastically and increasing its efficiency.

3) DC/AC converters: in the low voltage side, the full bridge can be used (alone or in interleaved mode) to convert the voltage from DC to AC. The interleaved modulation (see the low voltage side converter of Figure 3) allows to shift the carrier signals, by reducing the harmonic content in the load current. In fact, being the converters current signals summed, the phase opposition of some harmonics leads to their cancellation in the overall current [10].

In Figure 3 and 4 two solid state transformers are reported. The first is made up of one NPC, five DABs and three IFB (Interleaved Full Bridges). The second has a CHB converter in the medium voltage side and a full bridge in the low voltage side.

B. Conduction and switching losses

In a power converter, four different kinds of losses occur: the conduction losses, the switching losses, the off-state losses and the driving losses. The conduction losses depend on the internal module resistance, while the switching losses are due to the nonzero product between the current and the voltage when the power semiconductor is changing its state. Instead, the off-state losses are caused by the leakage currents when the semiconductors are in the off state and the driving losses are due to the driving signals forcing the semiconductor to switch its state. Compared with the conduction and switching losses, the off-state and driving losses are very small and are, here, neglected [11].
The considered switches are made up of IGBTs and diodes. In what follows below, the models describing the conduction and switching losses are presented.

1) Analytical models for conduction losses: the IGBT conduction losses P_{c_t} depend on the average and the rms values of the current i_C through the semiconductor [11] and it can be modeled as reported below:

$$P_{c_t} = v_{CE_0} \cdot i_{C_{avg}} + r_C \cdot i_{C_{rms}}^2 \qquad (1)$$

where v_{CE_0} is the on-state zero-current collector-emitter voltage and r_C is the collector-emitter on-state resistance.
Similarly, it is possible to define the diode conduction loss P_{c_d}.

$$P_{c_d} = v_{D_0} \cdot i_{D_{avg}} + r_D \cdot i_{D_{rms}}^2 \qquad (2)$$

v_{D_0} represents the diode on-state zero-current voltage and r_D the diode on-state resistance. $i_{D_{avg}}$ and $i_{D_{rms}}$ are respectively the average and rms current through the diode.
The values of the on-state zero-current voltages and the equivalent resistances can be found in the components data sheets, while the current values depend on the specific applications.

2) Analytical models for switching losses: the switching losses models also depend on the selected converter control method. Having decided to control the cells with the continuous PWM in medium and low voltage sides, the adopted

models are reported below [11]. Moreover, the IGBT switching losses depend on the switching frequency f_{sw}, the average voltage V_{dc} and the average current I_t through the transistor and the switch on/off energies (E_{on} and E_{off}). These two last terms are provided in the data sheets for a reference voltage V_{ref_t} and current I_{ref_t}.

$$P_{sw_t} = f_{sw} \cdot (E_{on} + E_{off}) \cdot \frac{V_{dc}}{V_{ref_t}} \cdot \frac{I_t}{I_{ref_t}} \qquad (3)$$

The model describing the diode switching losses P_{sw_d} is similar to the one used for the IGBT where only the diode reverse recovery E_d is considered.

$$P_{sw_d} = f_{sw} \cdot E_d \cdot \frac{V_{dc}}{V_{ref_d}} \cdot \frac{I_d}{I_{ref_d}} \qquad (4)$$

Since the potential of DAB is the ability to get the converter to work in soft switching mode, the control methodology and the switching losses models proposed in [12] are used. The proposed control is to drive one of the two bridges to generate a three-level pulse-width modulated voltage waveform, with an appropriate phase shift δ respect to the waveform on the other side of the transformer.

IV. CONSIDERED SEMICONDUCTOR MODULES AND SST TOPOLOGIES

Considering the converter cells proposed in Section III-A, four main topologies can be realized by them. They are:
1) NPC + DABs + FB;
2) NPC + DABs + IFB;
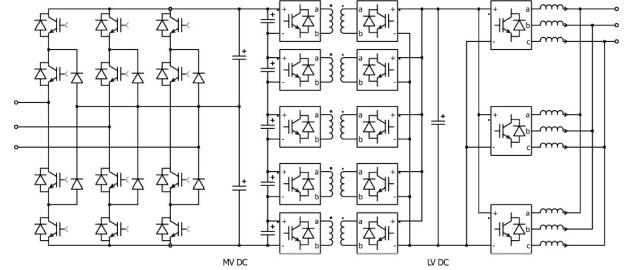3) CHB + DABs + FB;
4) CHB + DABs + IFB.

Figure 3: Example of the simulated topology (topology number 2 of the numbered list). The SST is composed in the MV side by a NPC, the isolation stage is made up of 5 DABs and in the LV side 3 IFB are connected with a common DC-link.

The goal of the presented work is not only to evaluate the semiconductor losses for each topology, but also to show the role of the semiconductor choice. The lower the power rating of the selected semiconductor, the higher the number of switches that must be used. Moreover, depending on the selected cells, the semiconductor choice can affect the modularity level of the converter. The only considered modules are Si IGBTs and diodes, even if other devices (like MOSFETs or SiC devices) or device housing, could represent a better choice. An example, which is not considered here,
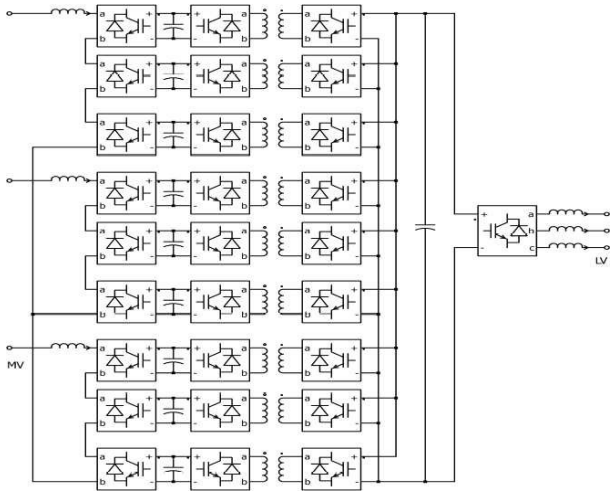
Figure 4: Example of simulated topology (topology number 3 in Section IV). The SST is composed in the MV side by 3 CHBs, the isolation stage is made up of 9 DABs and in the LV side a full bridges is connected.

is given by the possibility to use a hockey-puck housing for MV applications.

A. IGBT and diode modules

A little database, containing the features of some IGBTs and diodes of interest for our purposes, was created. The selected semiconductors are produced by different manufacturers, such as Infineon, ABB, Mitsubishi, Semikron and Powerex. In Table I and II the DC reference voltage and current, of the selected semiconductors for the medium and low voltage sides, are reported. They were grouped based on the reference DC voltage: the different nominal currents are reported for the considered modules. Even if here not reported, each semiconductor is characterized by its own electric features, such as of v_{CE_0}, v_{D_0}, V_{ref_t}, I_{ref_t}, V_{ref_d}, I_{ref_d}, r_C, r_D, E_{on}, E_{off} and E_d.

Table I: Electrical features of the semiconductor used in the MV side

Collector-Emitter voltage [V]	Nominal current [A]
1200	400-450-600-800-1200
3300	800-1200-1500-2000
4500	650-800-1200
6500	200-250-400-500-600-750

By fixing the SST rated power and by considering different semiconductor modules, the topologies and losses vary accordingly. In fact, in order to withstand the high medium voltage level, the lower is the module reference voltage the higher is the number of IGBTs needed, if the NPC converter is selected. If a solution with CHB is considered, the semiconductor DC

Table II: Electrical features of the semiconductor used in the LV side

Collector-Emitter voltage [V]	Nominal current [A]
1200	400-450-600-620-800 900-1200-1800-2400-3600
1700	1600

reference voltage affects the number of modules to be considered in the cascaded mode. Similar considerations can be made for the number of DABs in the DC/DC conversion. Finally, in the low voltage side, the number of the interleaved full bridges depends on the nominal current the semiconductors can support.

In order to increase the system reliability, one redundant module is added for each stage if a CHB, DABs and/or IFB converters are used. Although an increase in the modularity level could suggest a consequent decrease in the system reliability (a higher number of modules can fail), on the other hand, by properly controlling the system, this latter is not affected if a failure in the module occurs.

B. Analyzed topologies

The electric features of the implemented SST topologies are reported in Table III. For all the cases, the rated power is $S_{rat} = 1\,MVA$ and the rated frequency is $f_{rat} = 50Hz$. The medium and low side voltages (ph-ph rms) are 11 kV and 400 V. The medium voltage DC-link, downstream the three levels NPC converter, was selected to 17.88 kV (15% above the natural DC-link voltage). As previously said, depending on the semiconductor features, a proper number of IGBTs must be used: being 6.5 kV the maximum DC voltage supported by the selected modules, at least two IGBTs must be connected in series for the three-level NPC converter.

The medium voltage DC-link downstream the CHB converters, chosen accordingly with the same criteria reported above, is 10.32 kV: for each phase, at least three H bridges must be connected when a 6.5 kV IGBT is chosen.

To calculate the number of converters in the DC/DC conversion stage, the DC-link voltage has been considered as the 20% above the natural DC-link voltage. Starting from this voltage value and the electric feature of the selected semiconductor, the number of DABs was estimated. Moreover, redundant cells were added: an additional parallel DAB if the NPC converter is used in the MV side, while an additional parallel DAB in each phase if CHB converters are selected. According to [12], the transformation ratio was chosen in order to ensure the soft-switching operation in the whole phase shift range, considering m=1.

The low voltage DC-link was selected to 650 V (15% above the natural DC-link voltage). Single or interleaved full bridge inverters, with separate or common DC-links, were considered in the LV side. If interleaved full bridges are chosen, a redundant module is added.

The selected switching frequencies, for each converter cell, are reported in Table III.

V. RESULTS

In this section, the semiconductor losses for each converter cell and different semiconductor modules are reported. The modularity level depends on the semiconductor DC reference voltage for the MV side converters and on the reference current for the LV side converters. Only one redundant DAB and/or H-bridges (for the LV side) module is added as explained in Section IV-B.

Note that the converters' rated power does not change according to the semiconductor choice, but it remains constant in all the simulations.

The presented results were obtained by supposing a semiconductor temperature of $125°C$. As clearly shown in Table IV, by decreasing the semiconductor temperature, the power losses decrease. Thus in order to improve the overall system efficiency, the cooling system must be properly designed.

Table IV: Relation between the turn on/off energies and the semiconductor temperature (Infineon's IGBT FZ2400R12HE4_B9)

Turn-on energy		Turn-off energy	
T $[°C]$	E_{on} $[mJ]$	T $[°C]$	E_{off} $[mJ]$
25	365	25	430
125	460	125	455
150	505	150	480

In Figure 5, each marker represents the semiconductor losses (sum of the switching and conduction losses) for the NPC converter. Depending on the selected semiconductor, hence on its DC reference voltage, two, three or eight IGBTs must be connected in series for each switch. The different semiconductor losses, when two IGBTs are connected in series, depend on the features of the selected modules, whose reference DC voltages are equal. The same consideration can be made when three or eight IGBTs in series are needed.

It must be noticed that losses do not vary significantly if two or three IGBTs are connected in series. On the contrary, when modules withstanding a DC voltage of 1200 V are used (eight IGBTs in series), the total semiconductor losses vary between 8915 W and 13341 W and this significantly increases the converter efficiency. Although it is difficult to connect eight IGBTs in series, being difficult to equalize the voltage drop across each IGBT, this solution is used for several industrial products. In order to overcame such problem, a NPC with a higher number of voltage levels (five or seven) can be used. However, difficult is to balance the DC links, and the semiconductor uneven thermal stress should be carefully considered.

In Figure 6, the total semiconductor losses for a cascaded H-bridges converter with a different number of modules (respectively with 3, 4, 5 and 10 CHBs for each phase) are reported.
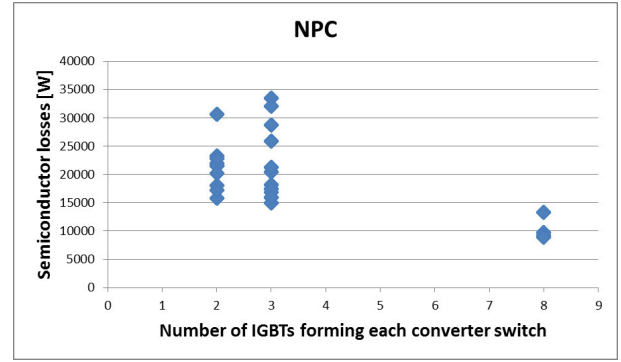

Figure 5: Semiconductor losses in a 3-level NPC converter for different kinds of IGBT modules. Depending on the IGBT features, two, three or eight IGBTs must be connected in series for each switch.

Depending on the DC voltage that the semiconductor can withstand, a different number of modules must be connected (the lower the semiconductor DC voltage, the higher the number of cascaded H-bridges). The figure clearly shows that by using semiconductors that withstand a lower DC voltage, the average converter efficiency improves. However, when a semiconductor module is chosen, a detailed analysis of the converter efficiency must be performed. Moreover, it is worth noticing that the semiconductor losses of a NPC converter are higher than those of a CHB converter, thus being the latter preferred.
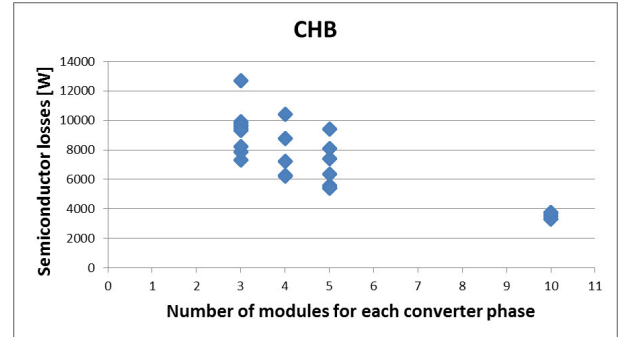

Figure 6: Semiconductor losses (sum of the all modules) in a CHB converter with a different number of cascaded modules for each phase.

In Figure 7 the DAB semiconductor losses are reported when CHB converters are used in MV side. Similarly, in Figure 8, the DAB semiconductor losses are reported but, now, the NPC converter is used in MV side. Differently to the previous results, the semiconductor losses for the DABs do not change significantly according to the switches rated power. Moreover, since the DABs work in soft switching mode, then the switching losses can be neglected if compared to the conduction losses. Such values characterize the trend of Figures 7 and 8.

Finally, in the low voltage too, the efficiency increases with

Table III: Parameters of different SST topologies

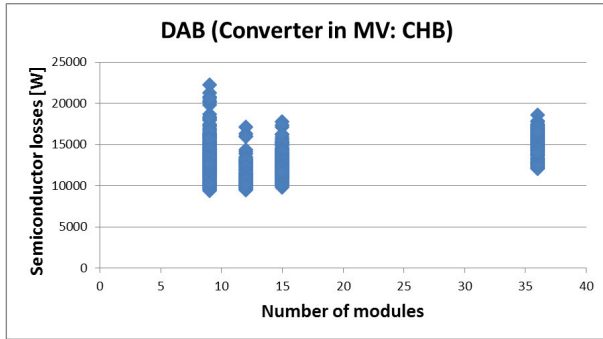| MV-side converter	MV f_{sw}	MVDC-link voltage	Isolation stages	DAB F_{sw}	LVDC-link voltage	LV converters	LV F_{sw}
NPC	$3\ kHz$	$17.88\ kV$	DABs	$10\ kHz$	$650\ V$	FB	$6\ kHz$
NPC	$3\ kHz$	$17.88\ kV$	DABs	$10\ kHz$	$650\ V$	IFB	$6\ kHz/n.IFB$
CHB	$1.5\ kHz/n.CHB$	$10.32\ kV$	DABs	$10\ kHz$	$650\ V$	FB	$6\ kHz$
CHB	$1.5\ kHz/n.CHB$	$10.32\ kV$	DABs	$10\ kHz$	$650\ V$	IFB	$6\ kHz/n.IFB$

Figure 7: Semiconductor losses in the DC/DC converter (sum of the all modules) with a different number of DABs modules. The converters used in MV side are the cascaded H-bridge.
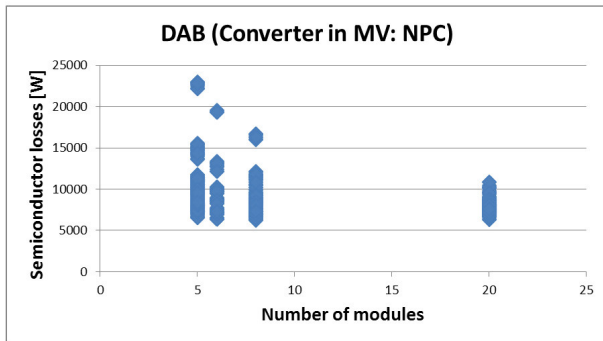

Figure 8: Semiconductor losses in the DC/DC converter (sum of the all modules) with a different number of DABs modules. The converter used in MV side is the neutral point clamp.

the number of interleave full bridges. From Figure 9, note that the semiconductor losses do not vary significantly if 3, 4, 5 or 6 interleaved full bridges are used: 3 interleaved full bridges seem to be the fair trade-off between the converter efficiency and its complexity.

Starting from the results presented above, in Tables V and VI the best and the worst topologies are reported. Their efficiencies, which were estimated by neglecting the passive components losses, are respectively 98.23% and 94.51%. From literature results, the transformer and the filter losses can reduce the efficiency of few percentage points. A reduction of the total efficiency of 1% [13] brings the SST efficiencies to 97.23% and 93.51% respectively.
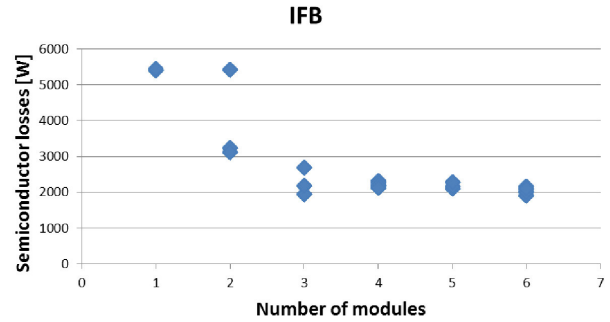

Figure 9: Semiconductor losses (sum of the all modules) considering a different number of full bridges

To further improve the efficiency, a better cooling system can be designed: a decrease of the semiconductor temperature, can improves the total efficiencies in the order of 0.1-0.8%. However, for a real design, the losses and the chip temperature would be calculated and, according to this, the suitable IGBT with suitable current would be chosen. Moreover, for an exact comparison, the virtual concept of fractional IGBT would be taken into account [14]. This will be performed in future works.

Table V: Features of the best topology, with respect to the selected semiconductor modules

Stage	converter	number of IGBTs/diodes	semiconductor losses [W]
AC/DC	10 CHB	120	3559
DC/DC	36 DABs	288	12237
DC/AC	3 IFB	18	1895

Table VI: Features of the worst topology, with respect to the selected semiconductor modules

Stage	converter	number of IGBTs/diodes	semiconductor losses [W]
AC/DC	NPC	24	30675
	(2 IGBT $\sim$)	(+ 6 clamp diode)	
DC/DC	5 DABs	40	22134
DC/AC	5 IFB	30	2049

Finally, some considerations on the total costs: although the topology with higher efficiency requires a bigger number of switches, the total estimated semiconductors cost is lower than what calculated for the worst topology, even if this latter is characterized by a lower number of switches. In fact, the cost of IGBTs, withstanding a DC voltage of 6.5 kV, is currently so expensive that, even a lower number of modules is not enough to offset the cost.

VI. Conclusion

In the presented work the semiconductor losses for different $1\ MVA$ SST topologies were calculated and the role of the semiconductor module, in the overall efficiency, is presented. The considered converters are the three-level NPC and the cascaded H bridges for the medium voltage side. The dual active bridges are used for the DC/DC conversion while the full bridges, alone or in interleaved mode, are used for the low voltage side. The results show that in order (i) to improve the SST efficiency and (ii) to reduce the semiconductors cost, the SST modularity level must be increased. The topologies presenting higher efficiencies are made up of cascaded H-bridges for the medium voltage side, dual active bridges for the isolation stage and interleaved full bridges for the low voltage stage. Finally, it shall be mentioned that a proper cooling system can help to further increase the overall system efficiency.

Acknowledgment

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