Digital Object Identifier 10.1109/TSG.2017.2651147

IEEE Transactions on Smart Grid, Early Access, 2017.

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Suggested Citation

G. De Carne; G. Buticchi; Z. X. Zou; M. Liserre, "Reverse power flow control in a ST-fed distribution grid," in IEEE Transactions on Smart Grid , Early Access.

Reverse power flow control in a ST-fed distribution grid

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***Abstract*—The massive integration of distributed generation in the grid poses new challenges to the system operators, like the reverse power flow from the Low Voltage (LV) to Medium Voltage (MV) grid. In the case of high DG power production and low load absorption, the voltage rises in the line reaching the upper voltage limit. At this regard the Smart Transformer (ST) offers a new possibility to limit the reverse power flow in the MV grids. The ST can adapt the voltage waveform modifying the frequency in order to interact with the local distributed generation, that are normally equipped with droop characteristic.**

However when a fast change in the frequency is applied to avoid reverse power flow to MV grid, stability problems, so far not investigated, arise. In this paper the stability analysis has been performed analytically and validated by means of Control-Hardware-In-Loop (CHIL) in a Real Time Digital Simulator (RTDS) and with experimental results in lab.

I. Introduction

The energy supply system has undergone a deep change in the last few years. The energy production has moved from few big centralized power plants to many small generators in the distribution grids. Frontrunners in this change are the renewables, that in case of Germany represent the $15\,\%$ of the country energy share [1]. However, the distribution grids are not designed for this sudden change of the energy production paradigm. As a consequence, a great number of distributed low power sources have been connected to the LV grid in the last years, leading in some case to grid stability problem such as: transformer reverse power flow, voltage rise, unexpected islanding operations, sympathetic tripping, etc. [2], [3]. Of particular concern is the reverse power flow issue. Being the low-voltage (LV) and medium-voltage (MV) radial, in the case of high power production and low load demand, the power in the feeder reverses, increasing the voltage till reaching the upper limits imposed by the distribution system operator (DSO) [4]–[6]. Of particular concern is the widespread installation of photovoltaic systems in the LV grids. In the worst case scenarios, that is high PV generation / low load consumption, the power flow reverses in the feeder, violating the voltage upper limits [7].

Actually there are no standard solutions to prevent the reverse power flow in MV grid. The options available to keep under control the voltage in the distribution grids can be divided in two categories: control algorithms and installation of intelligent devices. In the first category can be included the demand side management and the optimal power scheduling. In the first case, a central controller varies the load demand by means of energy price signals, limiting the voltage rise during the peak hours of the PV production [8]. The optimal power scheduling coordinates instead several devices (e.g., controllable loads, batteries, transformer tap changers, step voltage regulators, etc.) in order to keep under control the voltage profile during the PV intermittent power production [9], [10]. At device level the currently adopted solutions for voltage control are mainly the OLTC [11], the reactive power injection from DG [12] [13]. The OLTC solution, although simple and cost-effective, suffers from some limitations. OLTC technologies with asymmetrical mechanical topologies (e.g. single resistor OLTC [14]) limit the overload capability to the range $[30 \div 50\,\%]$ in the reverse power flow conditions due to the higher transient currents during the switching [15]. The reactive control of the DG, although more efficient than the OLTC solution due to the spread presence in the grid, depends strongly on the ratio X/R of the line [16].

To partially mitigate these problems, standards have recently imposed to grid-connected inverters to vary their output power in function of the instantaneous value of grid voltage [17], [18] and frequency (CEI-021 [19]). This paper aims at demonstrating the reverse power flow control in a Smart Transformer fed grid. The basic idea lies in the interaction between ST and the DG in order to limit the power produced in the case of low load demand, exploiting regulations allowing a power-frequency derating curve implemented in the DG [19], without the need of a communication infrastructure. This derating characteristic has been initially thought to help the transmission system during frequency instabilities. If the frequency increases due to an imbalance between generation and consumption, or due to a perturbation (e.g., faults, line disconnections, etc.) the DG must reduce its power output. The ST can adapt the voltage frequency in order to control the DG power output in case of reverse power flow conditions. The frequency influence on the LV grid load can be considered negligible as highlighted in the survey [20], where the system operators do not consider it during steady-state and transient studies. Moreover the frequency change adopted in this paper lies still within the limits imposed by the grid regulations. A similar approach has been adopted in a low-voltage micro-grid with photovoltaic sources [21] and to prevent overload in ST-

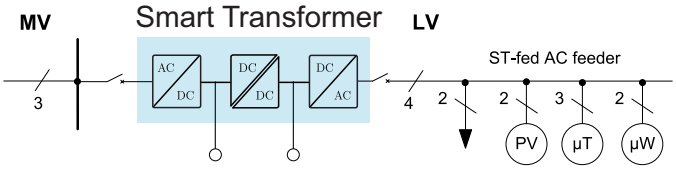

Fig. 1. Smart Transformer-fed distribution grid.

The research leading to these results has received funding from the European Research Council under the European Union's Seventh Framework Programme (FP/2007-2013) / ERC Grant Agreement n. [616344] - HEART.

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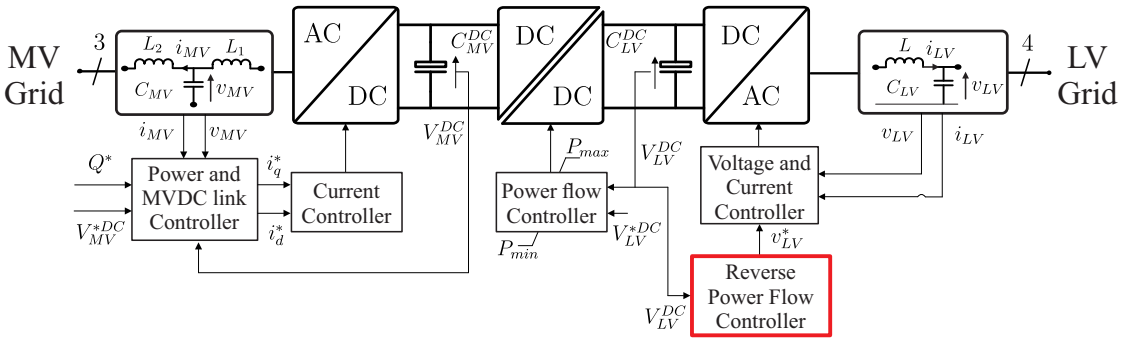

Fig. 2. Smart Transformer control scheme and proposed controller to avoid the reverse power flow in MV grid (red dotted square).

fed grids [22].

The implementation of this solution involves several partners (ST, DG inverter) and stability problems can rise during the control action application. In this paper particular focus has been given to the influence of the PLL bandwidth of the DG inverters and the ST DC-link capacitor. It is shown that a slower PLL bandwidth or a smaller ST DC-link capacitor lead to unstable behavior of the system. The analysis of this issue has been performed in the chapter, and verified by means of the Control-Hardware-In-Loop (CHIL) evaluation using a Real Time Digital Simulator (RTDS) and a micro-grid experimental setup.

This paper is structured as follows: section II describes the ST control scheme and the proposed methodology for avoiding the reverse power flow; section III gives the stability analysis varying the PLL bandwidth; section IV shows the experimental results obtained by means of CHIL evaluation in a LV grid; section V offers the method proof of concept by means of a simplified experimental case performed with two VSC converter; section VI introduces a discussion on the DC link capacitor effect on the controller stability. Section VII is dedicated to the conclusions.

II. Control of the ST-based microgrids

The Smart Transformer (ST) is a three-stage power electronics transformer [23], [24] that transforms the voltage from the MV to the LV grid, makes available the DC grid connections [25], provides new services to the distribution grids like the load identification and control [26], [27] and offers new solutions to current problems, like the possibility to deal with the reverse power flow conditions. A reference system is shown in Fig. 1. Although several topology solutions can be studied for each stage, the control strategies do not differ substantially.

The control strategy of the transformer is shown in Fig. 2.

The MV side keeps the MV DC link voltage fixed to the nominal value, absorbing or injecting the needed power in the MV grid. Moreover, the MV converter controls the reactive power injection in the MV grid. The ST can work under constant power factor, or provide reactive power support injecting reactive power. The reactive power set-point can be set locally by a V/Q droop controller, or remotely from a centralized controller.

The DC/DC converter absolves two duties: to transform the voltage from MV to LV and to control the voltage level of the LV DC link. The DC/DC regulates the power flow between the two DC stages in order to keep the LV DC link voltage constant to its nominal value. The reference power is limited between the P_{max}, determined by the ST sizing, and P_{min}. In order to prevent reverse power flow, P_{min} must be set to zero.

The LV side controls symmetrical voltage waveforms with an amplitude and frequency fixed to the reference values independently from the load power request. The amplitude and shape of the current waveform is decided solely by the load. In this application the voltage waveform reference is given by the reverse power flow controller (Fig. 2, red box), explained in the next section.

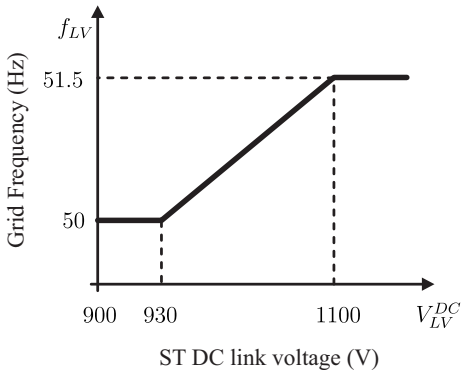

Fig. 3. ST DC link voltage and grid frequency characteristic curves adopted.

A. Reverse Power Flow Controller

In this paper the ST LV controller has been modified in order to implement the reverse power flow limitation control, as shown in the dotted red box in Fig. 2. The voltage reference is created taking in account the LV DC link voltage and it has a variable frequency. When the DC link voltage increases due to the DC/DC controller saturation during the reverse power flow, the AC voltage controller modifies the waveform frequency in accordance with a linear characteristic depicted in Fig. 3. The controller increases linearly the frequency from 50 Hz to 51.5 Hz when the DC link voltage goes above 930 V till reaching the maximum allowable voltage of 1100 V.

Following the frequency change, the local generators decrease the power injection in the grid. The equilibrium is reached when the energy produced by the DG matches the energy consumed by the loads: the DC link voltage is kept to a constant value higher than the nominal one and the reverse power flow is avoided. Only when the DG production naturally reduces (e.g., lower irradiance in the PV plants) or the load

consumption increases, the DC link voltage decreases and the reverse power flow controller brings back the frequency to the nominal value.

III. Stability analysis

In order to investigate the controller stability for this application, the system depicted in Fig. 4 has been adopted. The ST LV side is connected with n grid connected generators, and the PLL+current controllers have been implemented to control the DG power injection in the grid. Fig. 5 represents the mathematical model of the system described in Fig. 4, used to perform the stability analysis of the proposed control.

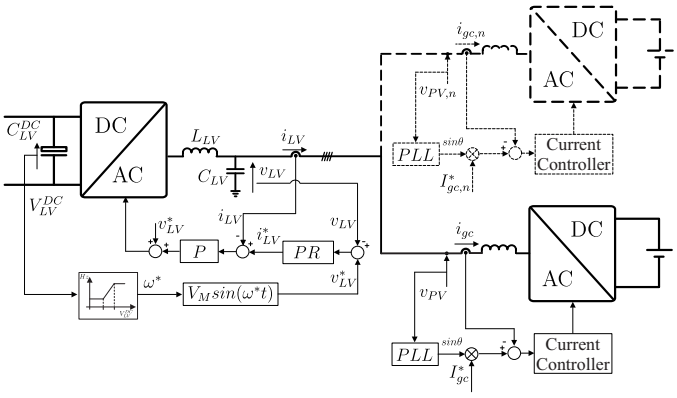

Fig. 4. Grid adopted for the stability analysis, with the ST interfacing n grid connected generators.

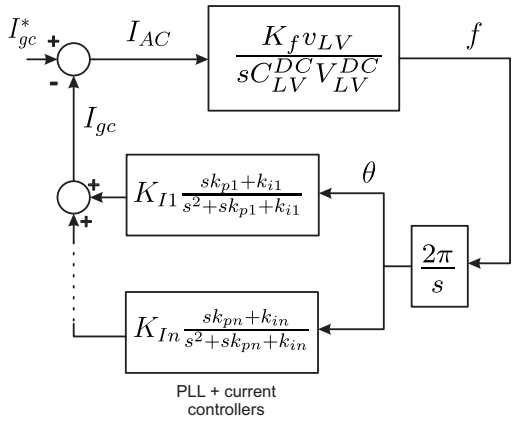

Fig. 5. Block diagram for the stability analysis.

The upper part of Fig. 5 refers to the ST, that responds to a DG power injection higher than the load consumption by increasing the grid frequency, with a dynamic that is decided by the DC Link capacitor C_{LV}^{DC} and the droop coefficient K_f. The integral of the frequency f represents the grid angle θ, that is then processed by the grid connected inverters. The constants k_{ph} and k_{ih} represent the parameters of the PI regulator for the phase-locked loop (PLL) of the grid-connected inverter h. K_I is related to the individual power of the inverter. In fact, for this simplified analysis, it is assumed that the PLL is an ideal feedback system with the grid angle at its output. This corresponds to the case of a synchronous reference frame PLL in a three-phase system and no voltage imbalance, and very high bandwidths can be achieved. In real system, SOGI [28] and notch filters can be adopted to limit the effect of the grid non-idealities, while for single-phase systems the delay introduced by the quadrature system generation should be considered. The PLL is a feedback system that needs to track the frequency and the phase of the input signal with zero steady state error. The input angle is a ramp signal with a slope equal to the grid pulsation. The regulator must be tuned having a target bandwidth (BW) for the frequency tracking and a settling time for the tracking error, that depends on the target phase margin (PM). The parameters can be consequently chosen as equation (1).

$$k_{ph} = \frac{BW}{\sqrt{1+1/\tan^2(PM)}}$$
$$k_{ih} = k_{ph}\frac{BW}{\tan(PM)} \quad (1)$$

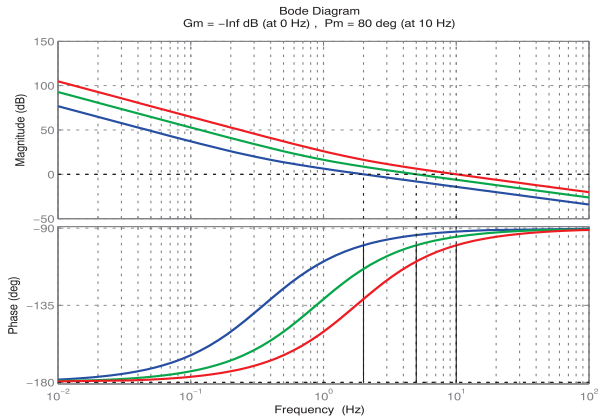

Fig. 6. Bode diagrams of the PLL, considering a tuning with PM = 80 deg.

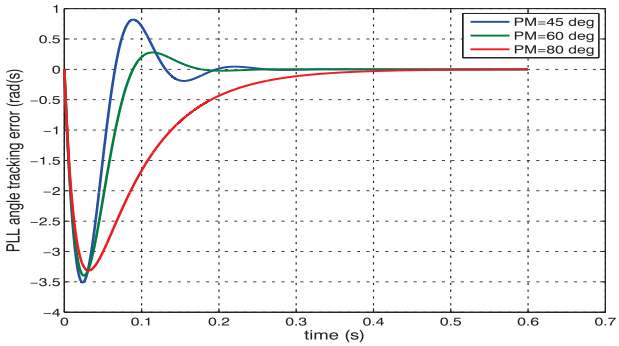

Fig. 7. PLL Tracking error in response to a ramp signal considering different phase margin.

Fig. 6 shows the open-loop transfer function of the PLL when a phase margin of 80 deg is chosen and different bandwidths. Instead, Fig. 7 shows the PLL tracking error when different phase margins are chosen. Reducing the phase margin shortens the settling time, while the frequency tracking is not heavily affected. Since a wide bandwidth and a reduced phase margin imply a higher sensitivity to grid disturbances [29], a conservative tuning is chosen, with PM = 80 deg, and the effect of the PLL bandwidth on the comprehensive system will

be considered. The stability study was carried out considering a small signal analysis (considering the load constant). In order to evaluate the root locus, the characteristic equation of the system is reported in (2). The root locus is then plotted considering a bandwidth varying for 1 Hz to 20 Hz and a single inverter (Fig. 8). This approach does not imply a loss of generality, since the slowest inverter determines the stability behavior of the system.

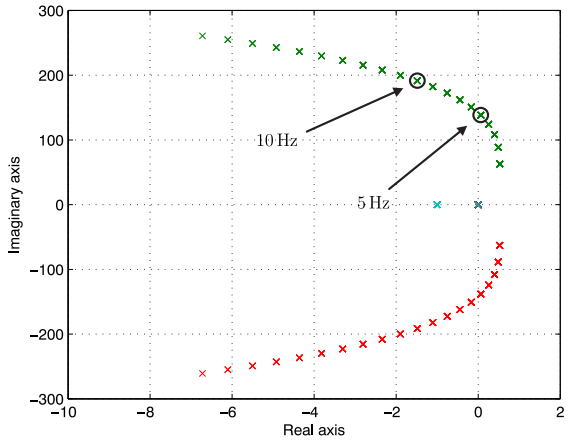

Fig. 8. Root locus with variable PLL bandwidth.

$$1+\frac{2\pi}{s}\frac{K_f v_{LV}}{sC_{LV}^{DC}V_{LV}^{DC}}\sum_{h=1}^{n}K_{Ih}\frac{sk_{ph}+k_{ih}}{s^2+sk_{ph}+k_{ih}}=0 \qquad (2)$$

The parameters refer to the droop curve of a 200 kVA ST LV converter with $v_{LV} = 230V_{RMS}$ and $V_{LV}^{DC} = 900$ V. As can be seen, a narrow bandwidth of the PLL (small gain) leads to instability conditions. A bandwidth of 5 Hz makes the control system unstable, instead a PLL with a 10 Hz bandwidth performs the control action in stable conditions. Nevertheless, as the grid synchronization is a key feature for grid-connected inverters, it is reasonable to expect that the bandwidth of the PLL be sufficiently broad to make the entire system stable.

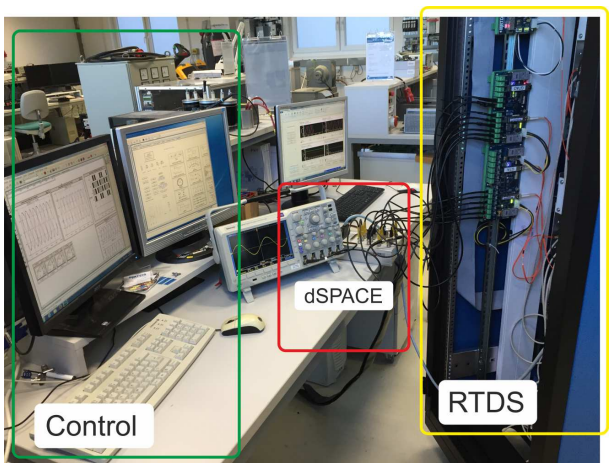

Fig. 9. Picture of the CHIL setup.

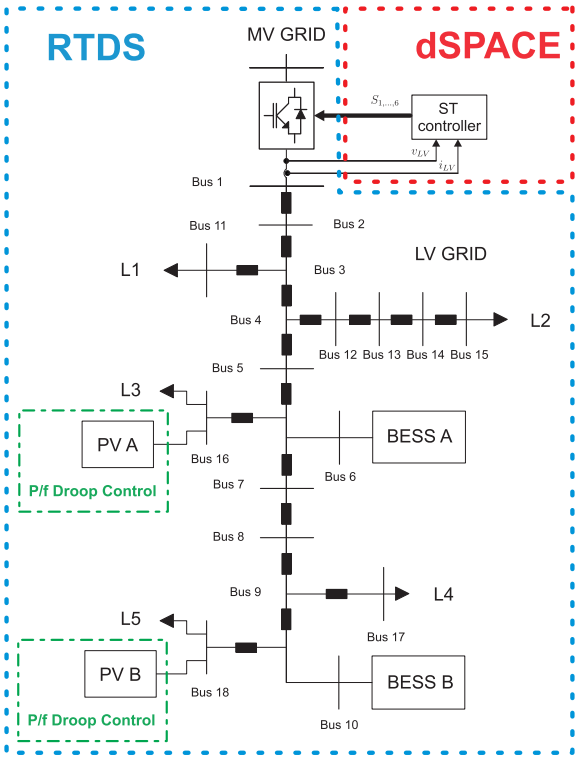

Fig. 10. CHIL: modified CIGRE European LV distribution network benchmark implemented in RTDS (large-dotted cyan square), ST controller implemented in dSPACE (dotted red square), photovoltaic power plants with frequency droop controller (point-dotted green square).

IV. Control Hardware In Loop (CHIL) Evaluation

The effectiveness of the proposed methodology can be proved with a real LV grid by means of Control Hardware In Loop. The ST and the LV grid are simulated in RSCAD, the RTDS software, and the ST is controlled by external equipment, for instance dSPACE 1104. A picture of the laboratory setup is shown in Fig. 9. The voltage and current are measured in RTDS and sent to the ST controller implemented in dSPACE. The output from dSPACE is a digital signal representing the firing pulses to be applied to the ST switching elements simulated in RTDS.

Since this work focuses on the low-dynamic regulators, i.e. the PLL and the reverse power flow control, the high-dynamic controllers, i.e. grid voltage and injected current, are not discussed. Standard tuning techniques [28] can be applied to derive these controllers' parameters.

TABLE I. Load and ST Data

Load	Bus	Apparent Power (kVA)	cosφ	ST Parameter	Value
L1	11	11.4	0.85	fs	2 kHz
L2	15	39.4	0.85	V_{LV}^{DC}	900 V
L3	16	39.4	0.85	C_{LV}^{DC}	10 mF
L4	17	5.4	0.85	L_{LV}	1.7 mH
L5	18	17.6	0.85	C_{LV}	100 μF

The grid analyzed is the CIGRE European LV distribution network benchmark [30] (Fig. 10). The following assumptions have been made due to the limited computation capability of the RTDS system without losing in generality in the proposed methodology: 1) the loads are assumed balanced and

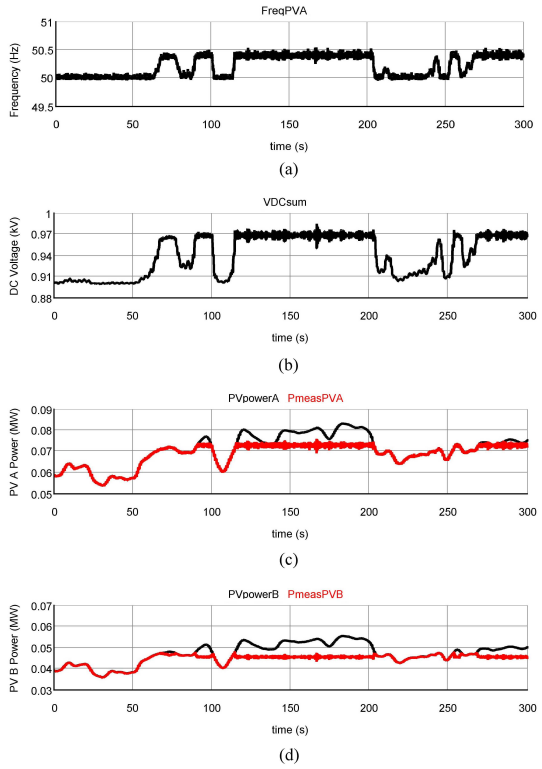

Fig. 11. Test Case A: (a) PLL-frequency of PV A, (b) ST DC voltage, (c) Theoretical PV A active power (black line), measured PV A active power (red line), (d) Theoretical PV B active power (black line), measured PV B active power (red line).

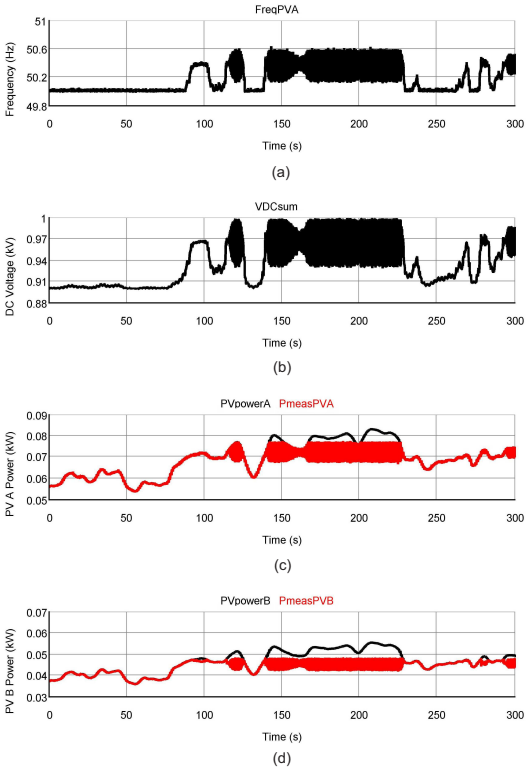

Fig. 12. Test Case B: (a) PLL-frequency of PV A, (b) ST DC voltage, (c) Theoretical PV A active power (black line), measured PV A active power (red line), (d) Theoretical PV B active power (black line), measured PV B active power (red line).

as constant impedance model; 2) the two BESS active and reactive power set points is set to 0; 3) the wind turbine has been removed. The load and ST data are listed in Table I.

Two separate test cases have been considered: Test Case A with the PLL bandwidth equal to 10 Hz; and Test Case B with the PLL bandwidth reduced to 5 Hz. The stability analysis of these two cases are marked in Fig. 8. The analysis has been performed in a time window of 300 s where a variable PV power profile has been given to the photovoltaic power plant PV A and PV B (black lines in Fig. 11(c) and (d)). In the case of a power production of the PV plants that exceeds the power absorbed by the loads, the DC link voltage increases due to the saturation of the DC/DC converter.

In the Test Case A, as soon as the voltage goes above the threshold of 930 V, the frequency controller is activated increasing linearly the frequency, as shown in Fig. 11(a) and (b). The PLL of the PVs calculates the new frequency, and if it results above 50.3 Hz, the PV curtails the power output, as can be noticed in Fig. 11(c) and (d) (red lines). As soon as the PVs reduce the power injection, the DC link voltage decreases and the frequency returns to the nominal value. In this case, the PV can inject in the grid the full available power. It is worth noticing in Fig. 11 that the stability of the PLL is guaranteed also in case of frequency change from the nominal value.

In Test Case B, where the PLL bandwidth is reduced to 5 Hz, the PLL presents an oscillating behavior, affecting the whole grid, as shown in Fig. 12. An oscillatory PV power production leads to an oscillating behavior of the DC link voltage in the ST. This forces the frequency controller to follow the DC voltage oscillation and change continuously the grid frequency. The whole system has an unstable behavior, affecting heavily the quality of the service. This is caused by the slow dynamics of the PLL, not able to follow the frequency change operated by the ST.

V. Experimental Results

The verification of the stability analysis, described in Section III and evaluated with CHIL, has been performed in lab with an experimental setup realized with two three-phase Voltage Source Converters (VSC) and a switchable passive load, as shown in Fig. 13. The controller of the inverter emulating the ST LV side has been realized following the scheme in Fig. 2.

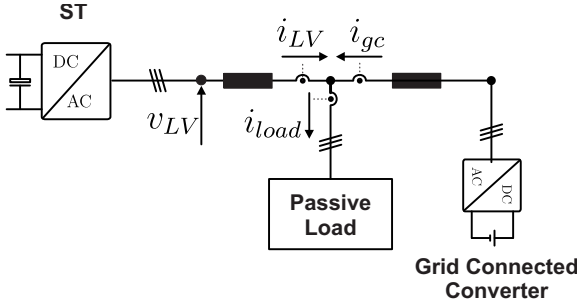

Fig. 13. Experimental setup realized in lab.

The DC side of the ST is supplied by an DC power supply and the DC link unidirectional saturation has been realized

TABLE II. EXPERIMENTAL SETUP PARAMETERS

Parameter	Value	Parameter	Value
V_{LV}^{DC}	650 V	V_{PV}^{DC}	650 V
C_{LV}^{DC}	3.3 mF	L_f	5.03 mH
C_f	10 μF	v_{LV}	220 V_{rms}
f_s	10 kHz	i_{gc}	6.5 A

by means of a series diode, effective to block the reverse power flow in the DC stage. The other VSC, representing the grid connected converter, is supplied with a DC source with a series resistance that emulates the photovoltaic panels. The PV converter is controlled with a classical current control loop, regulating the current injection on the grid. The PLL has been tuned has described in Section III with different bandwidths in order to verify the stability analysis. Three bandwidth cases have been chosen: a) $PLL_{bw} = 10$ Hz, b) $PLL_{bw} = 5$ Hz, c) $PLL_{bw} = 3$ Hz. The experimental setup parameters are listed in Table II and the controllers of both inverters are implemented in a dSPACE 1103.

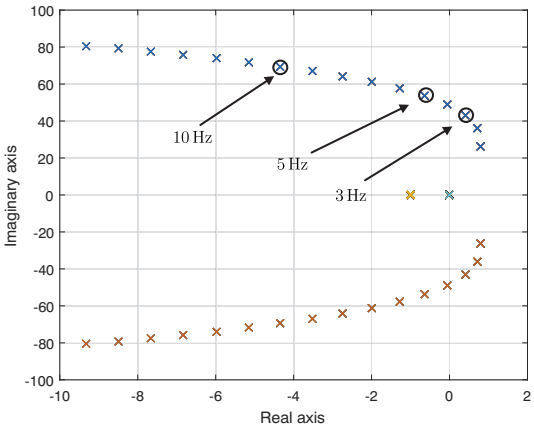

Fig. 14. Root locus with variable PLL bandwidths of the experimental setup

The stability analysis of the experimental setup has been performed and the root locus is shown in Fig. 14. The analysis shows how the system is stable under the cases $PLL_{bw} = 10$ Hz and $PLL_{bw} = 5$ Hz, but not for the case $PLL_{bw} = 3$ Hz. However a degradation of performance is expected for the case $PLL_{bw} = 5$ Hz with respect to the case $PLL_{bw} = 10$ Hz.

The experiments has been carried out performing a step variation of the resistor from 28 Ω to 45 Ω, while the current controlled converter is injecting 6.5 A. As the power flow reverses, the DC Link voltage increases. In Fig. 15 the results for the three chosen PLL-bandwidths have been plotted. In Fig. 15a the system shows a stable behavior. The frequency and DC link voltage are stabilized respectively at 50.55 Hz and 685 V after 500 ms and the DG converter reduces the current output from 6.5 A to 4.9 A. If the PLL bandwidth is decreased to 5 Hz (Fig. 15b) the system results be still stable, however with increased oscillations and longer settling time (more than 1.5 s). In case of further reduction of bandwidth, i.e. 3 Hz (Fig. 15c, the system becomes strongly oscillating till the trip of frequency protection after few seconds.

The experiment results plotted in Fig. 15 confirms what described in the stability analysis and shown in Fig. 14.

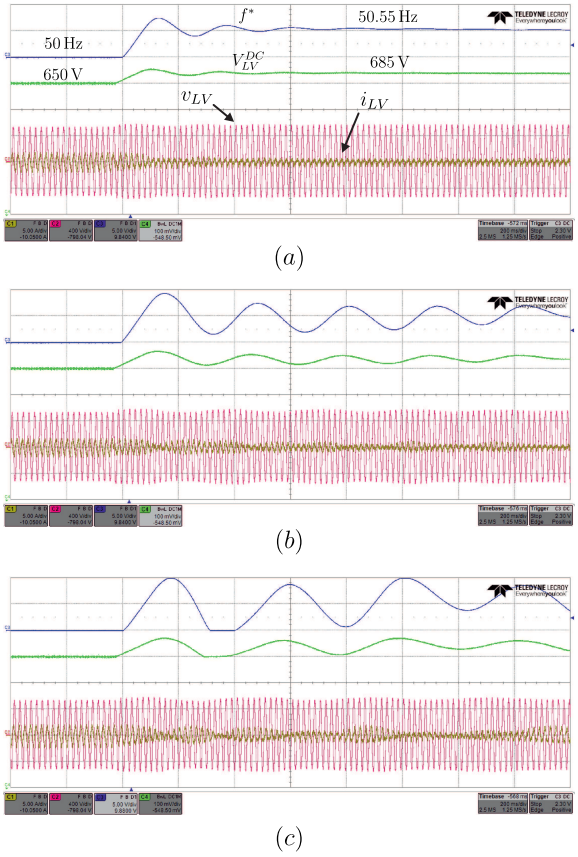

Fig. 15. Experimental results under different PLL-bandwidths: a) $PLL_{bw} = 10$ Hz, b) $PLL_{bw} = 5$ Hz, c) $PLL_{bw} = 3$ Hz.

VI. DISCUSSION ON THE CAPACITOR SIZING OF THE ST

In the bandwidth of the PLL lies the stability of the proposed Reverse Power Flow Limitation controller. However, the limited bandwidth of the DG converters can be compensated acting on the ST DC capacitor, as depicted in Eq.2. In Fig. 16 a PLL bandwidth of 10 Hz has been considered and the stability analyzed varying the capacity of DC link. Two capacitor sizes are considered in this analysis: the one employed in Section IV (10 mF); and the capacitor size that limits the voltage oscillation to 5 % during a 25 % power oscillation in the DC link (2 mF). The choice of the latter lies on the fact that the ST must have a minimum size for the DC capacitor able to handle the 2^{nd} harmonic oscillation deriving from unbalances in the LV loads. As can be noted, with the same bandwidth that kept stable the system in the Test Case A, where the DC capacitance was 10 mF, a capacitor of 2 mF can destabilize the control. In order to verify it, the Reverse Power Flow Limitation control has been performed by means of CHIL in the Test Case C, where the ST DC capacitor is equal to 2 mF. The results are plotted in Fig. 17. The controller becomes unstable as soon as the DC voltage triggers the controller. With respect of the Test Case B (Fig. 12), where the system had a limited oscillation, the DC link voltage oscillates with an amplitude of 100 V and the frequency is continuously changing from 50 Hz to 50.7 Hz during the control and keeps oscillating also in nominal conditions.

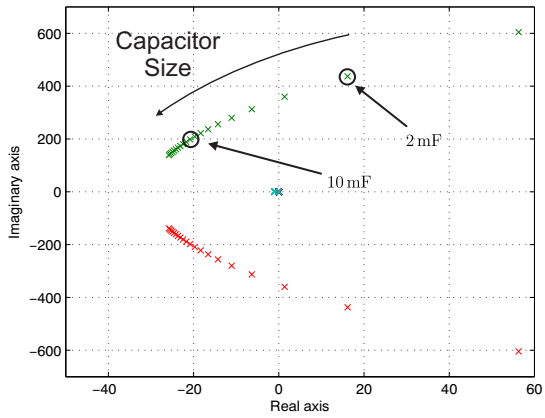

Fig. 16. Stability analysis varying the ST DC link capacitor with PLL bandwidth fixed to 10 Hz

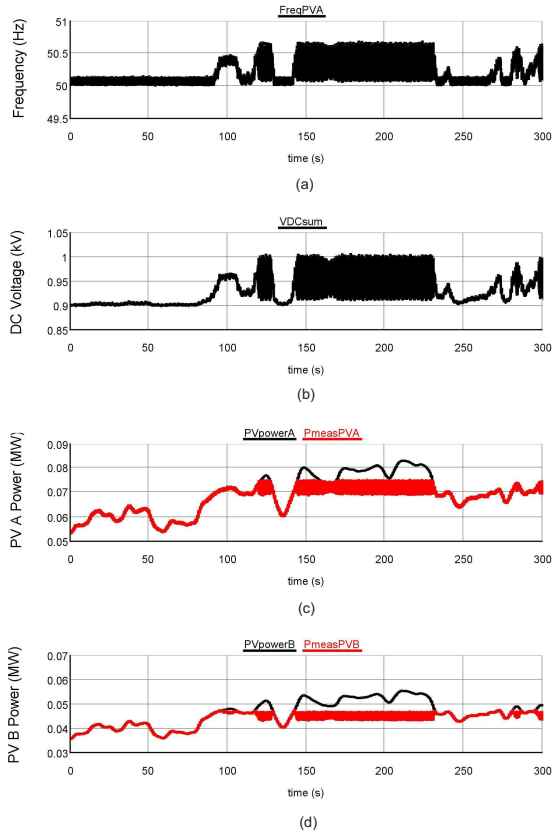

Fig. 17. Test Case C: (a) PLL-frequency of PV A, (b) ST DC voltage, (c) Theoretical PV A active power (black line), measured PV A active power (red line), (d) Theoretical PV B active power (black line), measured PV B active power (red line).

VII. Discussion on Lost Revenue

The proposed reverse power flow limitation controller reduces the power output from the DG in order to avoid the power flow reverse in MV grid. However, this power reduction reduces the revenue of the DG owner. In order to evaluate the impact on the DG owner, an economical analysis is carried out. As highlighted in a report from Energex Limited [31], the reverse power flow events can occur in up to 13 % of the LV/MV substations during the daylight hours, with approximately 20 % of active users in the grid. This condition can be taken as example for active grids with high penetration of renewables. In Fig. 18, the analysis of the annual curtailed energy from the reverse power flow controller has been performed. It has been assumed that the reverse power flow impacts negatively on the MV grid voltage in a reduced number of cases (here considered up to 30 %) and the maximum power that can be curtailed from the DG is 25 %. As can be seen, the annual curtailed energy results be less than 1 %, that is an acceptable tradeoff, considering the risk of overvoltage trips and of local black-outs.

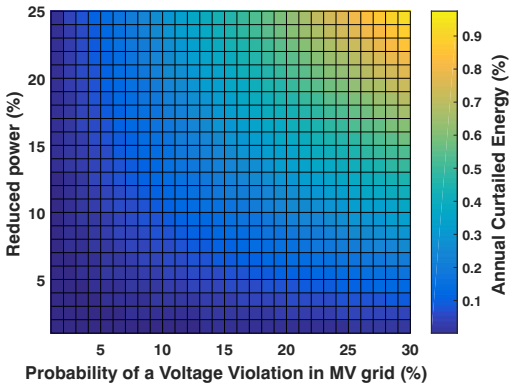

Fig. 18. Annual curtailed energy depending on voltage violation probability in MV grid and DG amount of reduced power.

Referring to the case described in Section IV, an economical evaluation of the lost revenue under Feed-In-Tariff (FIT) strategies developed in different countries has been performed in Table III. Two cases have been considered applying the 2015 FITs in effect in European countries: in the first case, the hypothesis of 10 % of voltage violation in MV grid and with 10 % of reduced power from the PV has been considered; in the second case, the same calculations have been performed under the more conservative hypothesis of 25 % of voltage violation in MV grid and 25 % of reduced power from PVs. Assuming that the PVs work 1100 hours at nominal power, the total revenue is within the range of [9424.8 € (France) ÷ 27104 € (Switzerland)]. As can be noted, the lost revenue for both PV A and PV B is not elevated, considering that the total size of both PV plants is 140 kW. Further revenue mechanisms can be studied for compensating the DG owners for the lost revenue.

TABLE III. Lost Revenue

Country	FIT (€/kWh)	Lost revenue 10% (€)	Lost revenue 25% (€)
France	0.0612	12.25	76.57
Germany	0.1071	21.44	134.01
Greece	0.1150	23.02	143.89
Switzerland	0.1760	35.24	220.22
Spain	0.1217	24.36	152.28

VIII. Conclusion

The massive integration of DG in LV grids may challenge the grid operations. High DG power production and low load consumption reverse the power flow from LV to MV grids generating overvoltage condition and transformer overloading

with particular OLTC topologies. The ST controls the voltage waveform in LV grid, and it can offer the possibility to avoid the reverse power flow. Saturating the DC/DC power controller in case of reverse power flow, the LV DC link voltage increases. The proposed Reverse Power Flow Limitation control measures the voltage increase in the DC link and increases linearly the frequency. The ST interacts with the DG droop controllers, that, measuring a frequency increment, reduce the DG power production.

However, the fast change in frequency causes converter stability problems in case of PLL with slow dynamics. As evaluated analytically in this paper and demonstrated with CHIL and experimental results, in case of low bandwidth, the PLL is not able to track the frequency change, making the control unstable. In particular, it has been demonstrated how a PLL bandwidth of 10 Hz is sufficient to keep stable the converter, instead with a bandwidth of 5 Hz an oscillation in the frequency tracking is present. Moreover the DC link capacitor size influences the system stability. A small DC capacitor leads to unstable conditions of the LV grid, also in case of PLL with sufficient high bandwidth (10 Hz). The reverse power flow controller, although reducing the power output of DG, limits the revenue loss of the DG owner. It is applied only in the non-ordinary conditions of reverse power flow and risk of upper voltage limit violations in MV grid.

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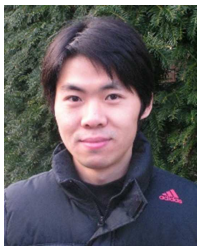

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