



Habilitationsschrift

Memristive Devices for Neuronal Systems

Martin Ziegler

Technische Fakultät

der Christian-Albrechts-Universität zu Kiel

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Preface

The present post-doctoral thesis covers 14 original publications¹, which result from my work as research assistant between 2011 and 2015 at the Institute of Electrical Engineering at the technical faculty of the Christian-Albrecht university at Kiel. During this time my research work was strongly guided by the question how to understand memory and learning in brains and how we can build up non-biological systems, which function similar to those. In particular, I focused on the usage of new non-volatile memory technologies and electronic circuits for neuromorphic systems. Thus, the development of non-volatile devices and electronic circuits as well as biological models based on those devices is at the heart of this post-doctoral thesis.

During the last couple of years I have been deeply grateful to many people; without their help and support this thesis could not have been written. I wish to thank, in particular, Hermann Kohlstedt for his constant encouragement and for all the constructive discussions over the last years. I especially like to thank him for providing me a stimulating and challenging environment in which I have been inspired, welcomed, and where I have found the freedom to realize my own ideas. His suggestions, inspirations, and view of science have a significant influence on this thesis.

I am especially indebted to Thomas Mussenbrock who did the proof reading. His constructive criticism and helpful suggestions helped a lot in the preparation of this thesis and I hope that he will be pleased with the final result.

Further, I wish to express my gratitude to all my colleagues from the AG Nanoelektronik at Kiel University. I thank Adrian Petraru, Rohit Soni, Ondrej Vavra, and Nico Himmel for sharing their experiences and assistances. I wish to thank all the students which have worked with me together over the last years. Especially, I am indebted to Mirko Hansen and Marin Ignatov who helped me to implement and further develop my ideas.

Finally, I like to thank the three most important persons in my live: Kajsa, Mattis and Hannah for the continued encouragement and support during the entire time. A large amount of time which I had to spend for this thesis would have belonged to them.

Martin Ziegler

¹For copyright reasons only the references to the original publications are given in the online version of the published habilitation thesis.

“For Hannah, who opened my mind for the living-nature”

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1 State of the Art

The DNA of a biological cell, the pages of a written book, the sheet of music or the data file on the computer have one thing in common: they are all examples of information and they all underly three typical operations, i.e. transmission, processing and storage [Was12]. While information is a rather general concept, the presentation and handling of information can differ significantly. For example, a language is required to present information, which can only have two characters like the Boolean code or a continuous spectrum of frequencies like the general sound. Moreover, for the transmission, processing and storage of information a physical carrier and medium is required [Was12]. Thus, information is restricted to physical media, which involve matter and energy.

It is the relation between information and physics which builds the basis of information technology and in which without a doubt the invention of digital computers lead to a technological revolution, which strongly changed not only our professional but also our personal life. In Fig. 1.1 the basic fields of information technologies are illustrated together with a few examples of information devices[Was12, Che15]. In particular the ongoing downscaling of electronic devices require continuous new device technologies which can overcome the dimensional scaling limits of the prevailing CMOS (Complementary Metal Oxide Semiconductor)technology and which are often summarized as More than More technology[Che15]. Regardless the tremendous success of digital computers shortcomings are obvious when it comes to cognitive tasks, as for example pattern recognition or unsupervised learning. At this respect, mammal brains are clearly superior to digital computers, which is based on the basically different computing schemes. In nature, learning (or data processing) and memory (or data storage) are inseparably linked, while for digital computers the von Neumann architecture induces a strict separation of serial digital processing and storage, as illustrated in Fig 1.1.

Neuromorphic engineering tries to close the gap between digital and biological computing by building up non-biological systems functioning similar to brains in at least limited terms. In particular, this interdisciplinary

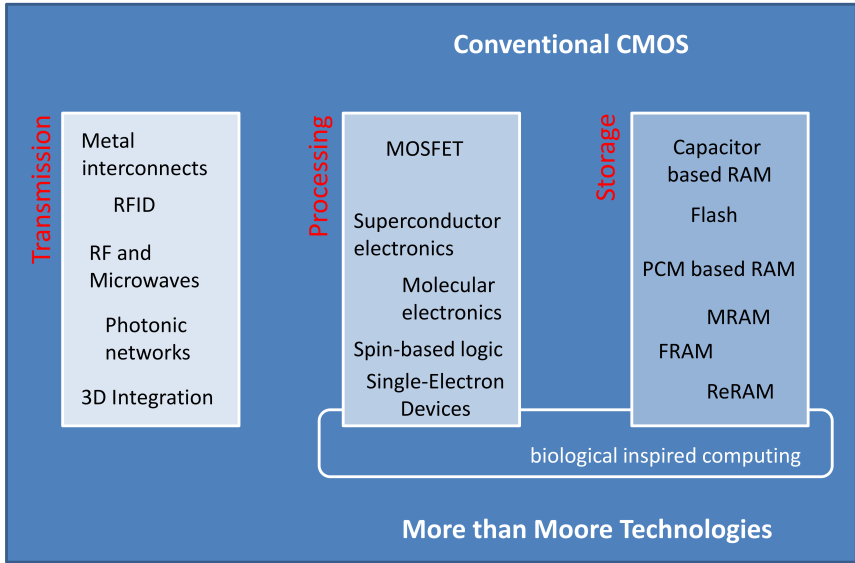


Figure 1.1 Illustration of the basic fields of information technologies and a few examples of information devices. Adapted from [Was12].

topic has been initiated in the 80's of the last century by the electrical engineer Carver Mead, the physicist Richard Feynman and the mathematician John Hopfield. It aims to explore the relationship between structure of neural-networks and their computations, regardless of it being natural or synthetic. For this purpose mainly to direction can be identified: Software dominated neuro-informatics and analogue VLSI (Very Large Scale Integration), which is based on Si CMOS technology.

It is worth to mention that numeric (informatics) approaches has been already used shortly after the invention of digital computers and has found its way into modern *intelligent* software. In particular, the McCulloch-Pitts-neuron [Cul43], already realized in 1943, and the perceptron, investigated by Frank Rosenblatt [Ros58] in 1958, should to be mentioned here. The use of integrated circuit architectures [Mea89] to emulate biological functionality is convincing by power consumption, parallel processing and computation in real time. Regardless of the success of neuromorphic engineering, biological

systems can only be emulated in very limited terms and the current research is still far away from discovering the so-called *brain code*. Moreover, humans, mammals and even simple forms of living species as invertebrates outperform neuromorphic systems in terms of power dissipation, fault tolerance and their adaptation to specific environmental conditions. This might be appearing not very surprising, since biological systems are a result of millions of years of evolution explained by Darwinism [Sha04].

In the last couple of years a renewed interest in resistive switching phenomena has lead to new and improved non-volatile memristive devices [Was09, Str12], which leverage analogue circuit approaches for neural applications [Jos13]. In particular, memristive devices, which are two-terminal devices consisting of a capacitor-like metal-insulator-metal layer sequence. In contrast to linear resistors, memristive devices are able to *remember* the history of applied electric potentials and therefore feature a device characteristic that cannot be emulated by one of the other basic two-terminal circuit elements (resistance, inductance, and capacitance). Recent investigations have recognized the analogue to the memristor, which had been predicted by Leon O. Chua in 1971 [Chu71]. Actually, memristive devices are considered as building blocks for future RRAMs which might show superior properties in comparison to charge based Flash technology [Was09]. In the field of neuromorphic applications memristive devices have been used to mimic synaptic functionalities, where important cellular mechanisms have been already emulated with single memristive cells [Zam11, Jo10, Ohn11].

From the materials point of view numerous concepts based on a broad material spectrum have been developed over the last years, including valence and phase change mechanisms [Was09, Str12], electrochemical metallization cells [Was09] and multiferroic tunnel junctions [Cha12]. Nonetheless, there is still a gap between the performance of single memristive devices with respect to the necessary requirements for a successful implementation of these devices in neuronal circuits. Although the progress of memristive devices is considerable, complex material issues paired with the superposition of phenomena as mixed conduction, local heating, and diffusion led to a hardly manageable situation from the point of theoretical description as well as for fabrication of devices with a sufficient yield and reliability, small parameter spreads, retention, etc. [Jos13].

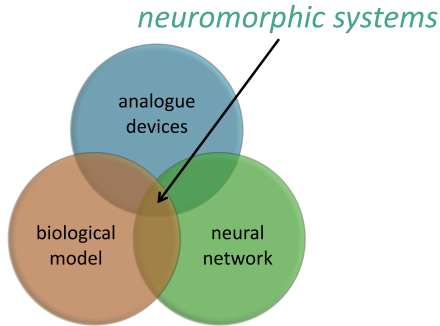


Figure 1.2 Illustration of the key topics for the development of neuromorphic systems.

1.1 Outline of the Thesis

This post-doctoral thesis aims to extrapolate neural mechanisms of learning and memory to electronic circuits based on memristive devices. Therefore, this thesis is dealing with three different topics, i.e. biological modeling, neural network architectures, and the development of memristive devices suitable for the use in those systems. Neuromorphic systems are thereby located in the intersection between those topics and based on their mutual interactions, as schematically sketched in Fig. 1.2. This thesis is structured in three parts, which give a brief overview over the publications [Maz:1 - [Maz:14].

First, I answer the question how memristive devices can be used for the emulation of learning and memory and what the basic (desired) requirements to build-up artificial neurons and synapses with memristive devices are. This is done in chapter 2 which sum up the findings of [Maz:1], [Maz:2], and [Maz:3].

Thereafter, in chapter 3 different memristive device concepts are presented and discussed with regard to their use as artificial synapses in neural networks. In particular, the presented devices ranging from nano-ionic cells with defined interfacial quantum mechanical effects, as origin for the resistive switching mechanism, to purely electronic devices, which are based on a floating gate transistor, named MemFlash cell. Chapter 3 summarizes the publications [Maz:4 - [Maz:12].

Finally, I present and discuss in chapter 4 neuromorphic systems, which are based on memristive devices. The overview in chapter 4 is guided by question how to integrate memristive devices in bio-inspired electronic circuits. In particular, neuromorphic circuit schemes are presented, which range from cellular networks for implicit learning [Maz:13] and anticipation [Maz:4] to a neural memristive network which allows unsupervised learning [Maz:14].

2 Towards artificial Memristive Synapses

The basic building blocks of every neural network are neurons and their inter-cellular connections, called synapses. In nature, synapses play a crucial role for learning and memory, since they are plastic, which means that they change their state in dependence on the neural activity of the respectively coupled neurons [And07, Byr09, Bea09]. Therefore, it is rather natural to use the non-volatile memory technology to mimic synaptic functionality [Zam11, Jo10]. Hence, every new device is highly appreciated which improves the design of neuromorphic circuits and reduces the circuit complexity. Therefore, memristive devices are promising candidates for the use as artificial synapses in neuromorphic systems, as sketched in Fig. 2.1. But a number of questions arise: How can functionalities of synapses with memristive devices be emulated? What are the basic requirements to realize artificial inorganic neurons and synapses? Which material systems and device structures can be used for this purpose? This chapter addresses these questions by giving an overview of the publications [Maz:1], [Maz:2], and [Maz:3].

2.1 Memristive Devices as Chemical Synapses

The basis of learning and memory in biological systems are activity dependent changes in the coupling strength of individual neurons, named synaptic plasticity. Synaptic plasticity ensures a temporary potentiation or depression of inter-cellular connections. Here, chemical synapses rather than electrical synapses play a decisive role with their spike-time-dependent plasticity (STDP) [Bi98] as well as long-term potentiation (LTP) and long-term depression (LTD) [Bli73]. At the cellular level, the famous Hebbian learning rule [Heb49], which states “*neurons that fire together wire together*”, allows to define a mathematical framework for cellular learning processes and can be regarded as an asymmetric form of STDP [Ger02]. In particular,

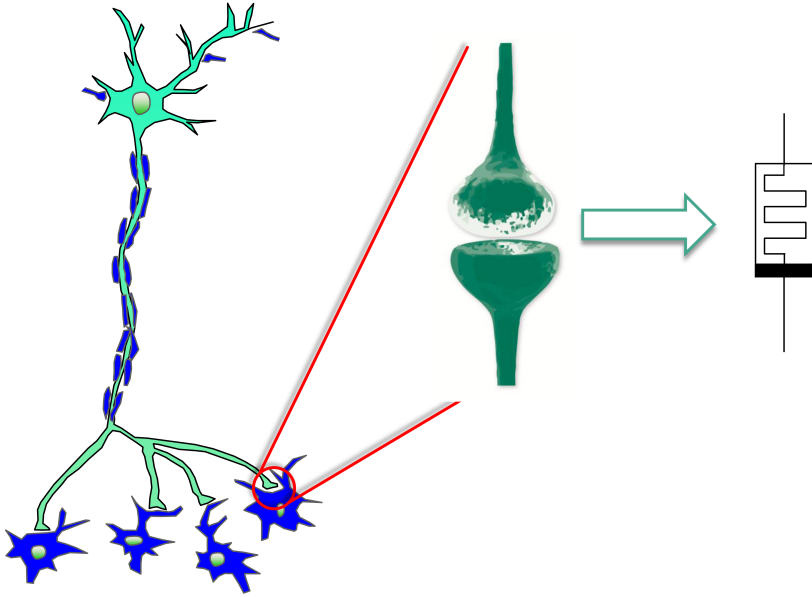


Figure 2.1 Towards memristive synapses: Schematic of a single neuron including several synapses. Close-up view of a single synapse, whose functionality might be emulated by a memristive device.

the Hebbian learning rule can be expressed as

$$\frac{d\omega}{dt} = F(\omega(t), \nu_{pre}, \nu_{post}) \quad (2.1)$$

Here, the synaptic weight growth $d\omega/dt$ depends on both the activities of the pre- and post-synaptic neuron, respectively, ν_{pre} and ν_{post} and the synaptic weight $\omega(t)$ itself. In particular, the Hebbian learning rule implies that the synaptic coupling strength is variable, if both, the pre- and the post-synaptic neurons, are simultaneously active. Therefore, the function F reads in the easiest form

$$F(\nu_{pre}, \nu_{post}) = \beta \nu_{pre} \cdot \nu_{post}, \quad (2.2)$$

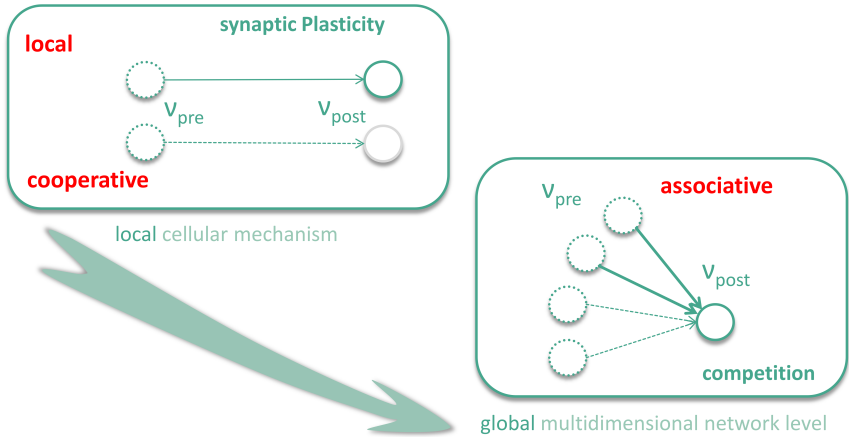


Figure 2.2 Illustration of the key properties of Hebbian learning, which are locality cooperativity and associativity.

where β is a constant, named learning rate. The aim of cellular plasticity models is to find appropriate descriptions of F , ranging from empirical (phenomenological) models, like the Bienenstock-Cooper-Munro rule (BCM) [Bcm82] or the Oja rule [Oja82] to biological models. In particular, during the last decades, a large number of plasticity models have been developed to describe the functional consequences of synaptic modification, including post synaptic membrane potential, spike timing, and the dynamics of intercellular calcium concentration [Gau10, Clo10], which itself depends on the post- and pre-synaptic activities. However, for learning and memory processes three properties are of particular importance: locality, cooperativeness and associativity, as illustrated in Fig. 2.2. Locality, or in other words, input specificity means, that the change of synaptic efficacy is critically depending on the activity of two interconnected neurons by a specific synapse but not on the activity of other neurons in the network. Cooperativeness implies that the probability of the induction of LTP increases with the number of stimulated presynaptic axons. The third aspect, associativity bridges a gap between the one-dimensional cellular learning mechanism to the multi-dimensional network level. Hence, neurons in networks face a competitive

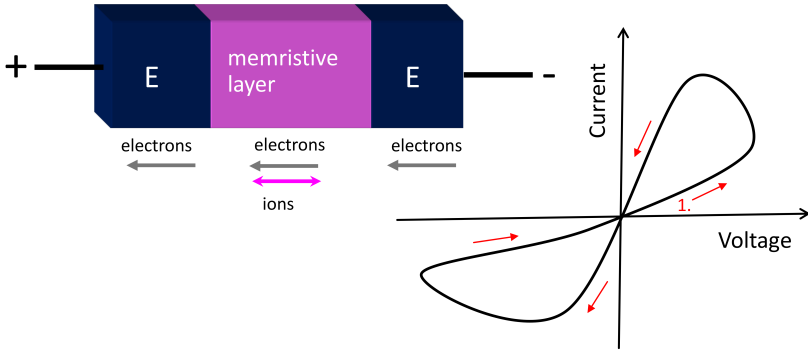


Figure 2.3 Schematic of a memristive device, which consists of a solid-state electrolyte sandwiched in between two metallic contacts together with a schematic current-voltage characteristic (I - V curve) of a single memristive device. As typical characteristic of a memristive device the I - V curve shows a pinched hysteresis.

situation in a way that synaptic weights grow at the expense of others [Ger02].

For the emulation of synaptic plasticity processes memristive devices are promising candidates because their conductance is depending on both the applied voltage as well as on the voltage history. By using the voltage driven ideal memristor model [Chu71, Str08] the memristive behaviour of the device can be described by

$$I(t) = M(x(t), V(t)) \cdot V(t) \quad (2.3)$$

$$\frac{dx}{dt} = f(x(t), V(t)), \quad (2.4)$$

where the conductance M (or memductance) depends on a structural parameter x , which itself is a function of the applied voltage V . Here, f is a continuous function describing the dynamics of the resistance switching process.

The easiest structure of a real memristive device consists of two electrodes separated by a dielectric material (MIM layer sequence), as sketched in

Fig. 2.3 together with a schematic current-voltage curve, which shows the typically memristive pinched hysteretic. In particular, in the most state-of-the-art memristive devices ionic movements within the dielectric layer effecting the resistance switching process [Str12]. Generally speaking, via the external applied electric field an ionic current, within the dielectric material, lead to structural changes, which in turn modifies the electronic conductance (i.e. the resistance). Recently, Zamarreno-Ramos et al. [Zam11] showed that in the above mentioned memristor model the change in the synaptic weight $d\omega/dt$ can be directly related to

$$\frac{d\omega}{dt} = \frac{dx}{dt} = f(x(t), \Delta t, \Delta V) \quad (2.5)$$

where f describes the weight change for a specific pulse duration (Δt) and pulse height (ΔV), associated to pre- and post-synaptic membrane potentials via $\Delta V = V_{post} - V_{pre}$. By using this challenging device characteristic of memristive devices important synaptic behaviours have been mimicked so far with single memristive cells [Jo10, Ohn11], which let memristive devices to be promising candidates for artificial neural systems.

2.2 Towards Artificial Synapses: A Materials Point of View

(from [Maz:3])

Several efforts have been made in the last couple of years to emulate synaptic functionalities with memristive devices. Important synaptic processes like spike-time-dependent-plasticity (STDP) [Jo10] and the fundamental precondition of learning in biological systems, i.e. long term potentiation (LTP) [Ohn11] has been emulated as far. Therefore various functional systems and materials with different resistive switching mechanisms have been explored. The paper [Maz:3] overviews over the variety of material systems by mainly focusing on those systems which are thought to deal with the keywords threshold, analogue, and plasticity. In the following the key aspect for artificial synapses is shortly summarized. A detailed discussion of the devices relevant for this thesis, their underlying concepts, and mechanisms can be found in chapter 3.

In Fig. 2.4 a classification of memristive devices is presented, which are

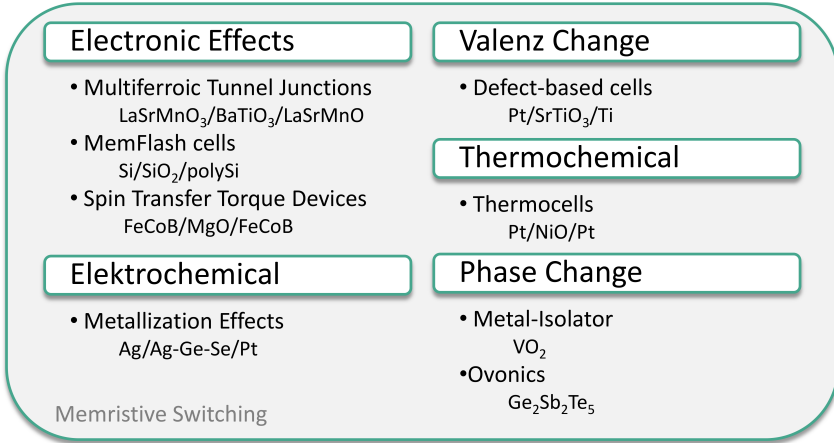


Figure 2.4 Classification of resistive switching processes, functional materials, and systems which are considered for memristive devices. Adapted from [Was09].

currently investigated as devices for the emulation of synaptic functionality. In particular, the present research is dealing with a high variety of materials used as electrodes and insulators (resistive switching layer) in memristive cells. The majority of memristive devices relies on nano-ionic mechanism including electrochemical metallization effects, thermochemical memory effects, phase change memory effects, or valence change memory effects [Str12, Was09]. Moreover, new switching mechanisms observed in spintronics devices [Krz12] and multiferroic tunnel junctions [Krz12, Pan12, Wan12] are considered as further candidates for memristive devices. Here, synaptic functionalities have already been successfully emulated. Furthermore, memristive functionality can be implemented in (modified) Field Effect Transistors [Lai08, You10] or conventional Flash cells, as it will be discussed in section 3.2.

In general, the combination of the different types of physical and chemical effects, which resistive switching is based on, together with the complex material systems gives a very interesting but complex research area. However, it is worth to mention that for most of the ionic motion based memristive devices the physical understanding of the relevant process on a mesoscopic and atomic scale remains unclear. Within this context, quite different models

have been developed, which again illustrates both the complexity as well as the relevance of this topic [Jos13]. In particular, reliability, retention, fatigue, as well as parameter spreads are only some examples that actually hinder the implementation of real memristive devices in the market or as a part of complex networks. Moreover, most of the current used materials for memristive devices are not compatible with state-of-the-art Si-fabrication technology and a further obstacle for commercialization. Therefore, a deep understanding and an appropriate control of the electrical parameters of memristive devices combined with Si-technology are highly appreciated.

It is worth to mention that learning and memory in neural systems are network processes and can therefore not be mimicked at the cellular level by investigating single memristive devices. Thus, the investigation of network architectures suitable for memristive devices is essential which might allow to determine which functionalities of single memristive cells have to be caught and how these functionalities work within neuromorphic systems. This in fact enables a tagged engineering of memristive devices for neural circuits and helps to better understand of relevant synaptic functionalities for the emulation of memory and learning. This question is addressed in chapter 4.

2.3 Hebbian Plasticity Model

(from [Maz:1] and [Maz:2])

The wide variety of memristive materials, devices and their working conditions make the search for the “*best*” memristive device for neural systems quite complicated and much of the yet presented devices show promising potentials for the realization of memristive synapses. From a functional level one may classify memristive devices by their resistance switching characteristics under voltage application, i.e. binary resistance switching or homogeneous gradual resistance change. Therefore, it might be possible to reduce the question for the “*best*” device to what the desired switching characteristics of a memristive synapse are. This question has been addressed by experimentally investigating three different types of memristive devices. While, the first type belongs to the class of mixed electron/ionic conductors, the second type of device functionality relies on a purely electronic transport mechanism. The layer structures of the ionic based devices are TiN/Al₂O₃/TiO_{2-x}/TiN and Al/Al₂O₃/TiO_{2-x}/Al (from bottom to top). The purely *electronic* memristive device (named MemFlash) is achieved

using a conventional EEPROM cell with a particular wiring scheme. Further details of the switching mechanisms and device concepts are given in chapter 3, while for this section the focus is on the current- voltage (I - V) nonlinearity and there implications for plasticity emulation.

As it has been shown in [Maz:1] and [Maz:2] suitable plasticity functionality can be reached if appropriate voltage pulse schemes are used for the respective device structures, which are feeding the distinct I - V nonlinearities. However, different pros and cons have been found: The challenge for ionic switching based memristive devices are found to be the device variability, while for the MemFlash cell the power consumption and switching time has to be reduced. However, the compatibility to Si-technology combined with the opportunity to model the MemFlash-cell using a simple capacitive model are attractive features of this device for the usage in neuromorphic circuits, as discussed in more detail in chapter 3.

Furthermore, it is of general interest to have a plasticity model at hand, which account for biological data and which are suitable to describe common plasticity measurements of memristive devices. In particular, such a model should only depend on parameters which are available from current-voltage measurements and should be applicable to different device concepts to compare them among each other. The model presented in [Maz:2] fulfils these requirements and in addition to this consist a limited weight growth together with a weight dependent (memristive) learning rate. The basic ingredient of the model is the correlation between resistance change (synaptic weight modification) and voltage pulse courses. In the following the model is briefly introduced.

The basic idea of the phenomenological learning model is to use the logistic differential equation to describe the synaptic weight change, since the logistic differential equation provides a strong synaptic weight change at the beginning, which gradually decreases with increasing weight and converges to zero if the maximal synaptic weight is reached. Therefore, Eq. 2.1 can be reformulated as

$$\frac{d\omega(t)}{dt} = \beta(\omega, t)\omega(t)\left(1 - \frac{1}{\omega_{max}}\omega(t)\right), \quad (2.6)$$

where, $\beta(\omega, t)$ is a weight dependent learning rate and ω_{max} the maximal synaptic weight. In order to solve Eq. 2.6 potentiation and depression have

been described as independent functions according to:

$$\omega^p(t) = \omega_0^p(t) + \frac{\omega_{max}}{1 + \exp(-\beta_p(t - t_0))} \quad (2.7)$$

$$\omega^d(t) = \omega_0^d(t) - \frac{\omega_{max}}{1 + \exp(-\beta_d(t - t_0))} \quad (2.8)$$

Here β_p and β_d are the distinct learning rates for the potentiation and depression respectively, and ω_0^p and ω_0^d are the inertial synaptic weights at the time t_0 .

A fundamental behaviour of memristive devices is that the emulated synaptic weight is directly proportional to the device conductance. i.e. $\omega(t) = \gamma G(t)$ (γ is a positive constant). Therefore, the learning rates are depending on the current conductance of memristive devices, as assumed by

$$\beta_{i=p,d} = \beta_i(\omega, \Delta V, t) = \frac{1}{C^i} G(\omega, \Delta V, t). \quad (2.9)$$

Here C^p and C^d are effective capacitances describing the kinetics of the weight change process. Thus, β provide both, a weight and voltage dependence of the plasticity model. In particular, this voltage dependence can be used for the emulation of plasticity processes, which depends on the post-synaptic membrane potential and ensure associativity as sketched in Fig. 2.2. Moreover, such a behaviour is basically compatible with advanced biophysical plasticity models like the Bienenstock-Cooper-Munroe rule (BCM) [Bcm82] and allows to predict regimes of both LTD and LTP, depending on the post-synaptic membrane voltage. Therefore, a voltage dependent sliding threshold can be defined, which separates both regimes in agreement with the BCM rule.

3 Memristive Devices

As it has been discussed in the previous section, the non-volatility, simple structure, as well as the scalability down to the atomic length scale make memristive devices especially interesting for neuromorphic systems. However, the majority of today’s memristive devices is designed for “*standard*” memory applications with partly different requirements compared to the needs in neuromorphic systems [Maz:1 - Maz:3]. For instance, for their use as a *random-access memory* data retention over more than ten years are required combined with read/write times of only several nano-seconds. Here, neural systems may differ significantly, because their time span of memory is ranging from several seconds (short-term memory) over days to years (long-term-memory) [And07, Byr09, Bea09], whereby the data processing is done at the milliseconds range. Moreover, depending on the neural circuit architecture, as it will be discussed in the following chapter, non-volatile memristive devices are desired, which are far beyond state-of-the-art device concepts.

Different device concepts are realized in the framework of this theses and have been published in [Maz:4 - Maz:12]. While for devices discussed in [Maz:4, Maz:5] the switching mechanism is based on filamentary driven transport mechanisms, which leads to binary switching characteristics. The device presented in [Maz:6] shows interface based resistive switching. Ferroelectric tunnel junctions (FTJs) have been attracted valuable attention for the use in neuromorphic systems [Cha12] and are shortly discussed in Sec. 3.1.3. In particular, in those devices interfacial related effects between the ferroelectric barrier and their connecting electrode play a crucial role and have to be distinguished from “*redox*”-based resistive switching effects, as it has been investigated in [Maz:7]. In Sec. 3.1.4 a concept for the development of laterally structured devices are overviewed. This overview is based on the publications [Maz:8] and [Maz:9] and allows to get access to the memristive layer from the top, which might be of interest for in-situ imaging investigations. The use of floating-gate transistors with a particular wiring scheme as memristive devices is briefly overviewed in Sec. 3.2, which summarizes the publications [Maz:10 - Maz:12]. In particular, the

so-called MemFlash-cells can be considered as a potential substitute for any-state-of-the-art memristive device and is additionally compatible with up-to-date Si-Fabrication technology.

3.1 Nanoscale Memristive Devices

The major class of today's memristive devices is functionally based on nanoionic mechanisms, which are classified in Ref. [Was09] as anion devices and cation devices (cf. Sec. 2.2). Common for all of those devices is that the non-volatile resistive switching is triggered by the migration of ions and is related to redox reactions [Was09, Jos13, Str12]. While the memristive material of anion devices include oxide insulator, such as transition metal oxides, large band gap dielectrics, and nitrides and chalcogenides, cation devices are typically consisting of an electrochemical active material and are often referred to electrochemical metallization cells (ECM). Here, an electroforming process causes structural changes to the memristive layer by forming nano scale conductive channels for the electronic transport, often referred to filaments, and is at the heart of the overall resistance variation of the complete device. In the following cation devices, which have been realized for this thesis, are briefly summed up.

3.1.1 Electrochemical Metallization Cells

(from [Maz:4] and [Maz:5])

ECM cells are realized in the framework of this theses for experimental implementation of different neuromorphic circuits discussed in chapter 4. However, in the following only the relevant aspects for [Maz:4], [Maz:12], and [Maz:13] are briefly discussed, while for a more detailed description of those class of devices the reader is referred to [Was09, Jos13, Str12].

A typical ECM stack consists of an insulating solid state electrolyte (SSE) sandwiched between an inert counter electrode (CE) and an electrochemically active electrode (AE). A possible realization of such a system is shown in Fig. 3.1(a), which has been adapted from [Maz:4]. In particular, Al, TiO_x , and Ag are used in this case as, respectively, CE, SSE, and AE. Here, the switching arises from the formation and dissolution of metallic filaments in TiO_x , which results from Ag-involving electrochemical (redox) reactions [Was09]. A typical eight wise bipolar I - V curve is presented in Fig. 3.1(b), in which a voltage was applied to the Ag electrode, while the Al was grounded.

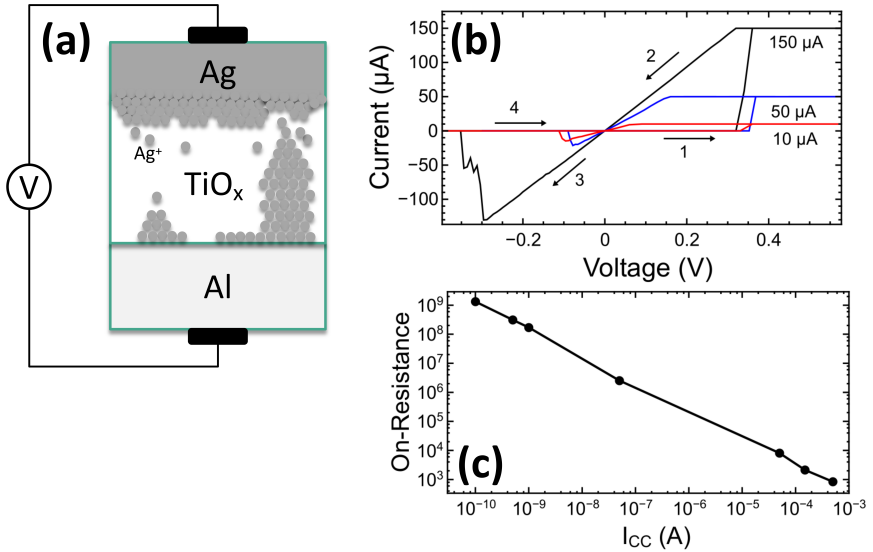


Figure 3.1 Electrochemical metallization cell (ECM): (a) Schematic of an Ag-doped TiO_x -based memristive device, as fabricated for [Maz:4]. (b) I-V curve of the Ag-doped TiO_x memristive device with three different settings of the current compliance I_{CC} . (c) The “On” resistance as a function of I_{CC} describing the multi-level behavior of the device.

In particular, ECM cells contain two distinct resistance states, i.e. a low resistance state (LRS) and a high resistance state (HRS), where the resistance of the LRS can be varied to some extent by the use of a compliance current, as depicted in Fig. 3.1(c).

Even, if the switching mechanisms of those class of devices are relatively well understood [Was09], the target development of devices underlies a controlled adjustment and knowledge of several kinetic parameters, such as redox reaction rate constants and mobility of active ions. Beside thermodynamic properties also the sequence of materials in the device stack itself might have enormous impact on the device characteristics, in particular in the case of dual-layer solid state oxides, which may allow an additional degree of freedom for a target development of memristive devices.

In [Maz:5] bipolar switching behaviour of ECM cells with such a dual-layer solid electrolytes ($\text{SiO}_x - \text{Ge}_{0.3}\text{Se}_{0.7}$) were investigated. While Pt (bottom electrode)/ $\text{SiO}_x / \text{Ge}_{0.3}\text{Se}_{0.7} / \text{Cu}$ (top electrode) cells exhibited typical eight wise current voltage (I-V) hysteresis, ECM cells with the layer sequence Pt(bottom electrode)/ $\text{Ge}_{0.3}\text{Se}_{0.7} / \text{SiO}_x / \text{Cu}$ (top electrode) showed counter eight wise hysteresis. An attempt to understand this electrolyte-stack-sequence-depending switching polarity reversal was made in terms of the ECM cell potential change upon the electrolyte stack sequence and the consequent change in Cu filament growth direction. Relevant experimental evidence for the hypothesis was obtained regarding the switching behaviours.

3.1.2 A Double Barrier Memristive Device

(from [Maz:6])

In addition to chemical switches based on anion and cation ions as discussed in the previous section also physical changes can be involved in the switching process as well. In particular, electronic switches might be of general interest for neuromorphic applications, since the resistance change stems from charge trapping (de-trapping) at an electrode/insulator interface and restrict the resistance switching to interfacial effects [Saw06]. The use of defined interfacial states instead of randomly created conductive filaments allows a better control of the switching process combined with a decrease of the device variability [Saw06]. In particular, for neuromorphic applications interfacial resistive switching is of interest, since here a homogeneous gradual change of the device resistance under voltage application instead of a fast binary resistance switch is desired in several network topologies [Maz:3]. However,

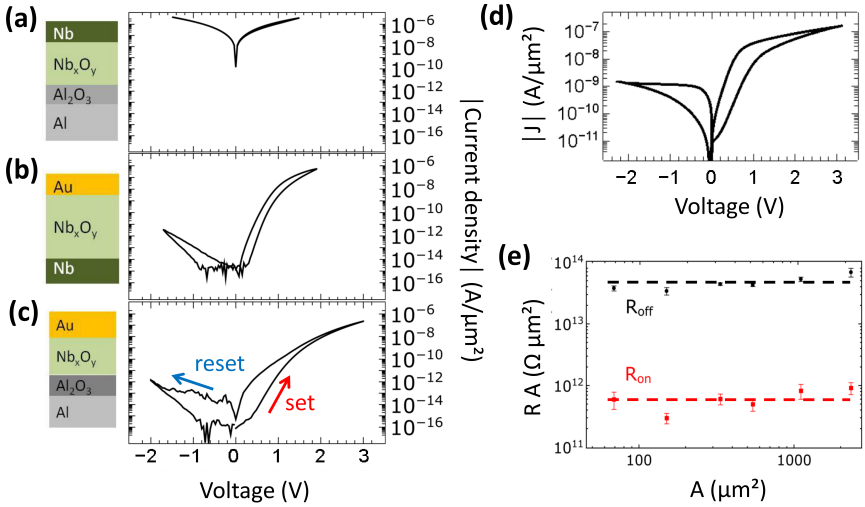


Figure 3.2 Memristive double barrier device [Maz:6]: Schematic of the particular device stack together with the absolute value of the current density $|J|$ versus applied bias voltage of (a) an $\text{Al}/\text{Al}_2\text{O}_3/\text{Nb}_x\text{O}_y$ tunnel junction, (b) an $\text{Nb}/\text{Nb}_x\text{O}_y/\text{Au}$ Schottky contact and (c) the $\text{Al}/\text{Al}_2\text{O}_3/\text{Nb}_x\text{O}_y/\text{Au}$ double barrier device. (d) Calculated I-V curve using an equivalent circuit model for the double barrier memristive device. (e) The area-resistance product vs. junction-area curve of the double barrier device measured at 0.5 V indicates a homogeneous area dependent charge transport. The error bars are obtained from 5 cells of each area. Junction areas were confirmed with optical microscopy

in comparison with filamentary switching-based nanoionic devices, interfacial switching is less studied and only a small number of functional devices are published so far [Saw06, Mik14, Aok14, Bai10, Jeo11, Hu11, Par08, Bai03, Koh93, Mey08, Fuj05]. In particular, the most striking disadvantage of those devices seems to be the poor retention and the high “On” resistances, which make an application in future non-volatile memory questionable. Moreover, also for those devices the interplay between ionic and electronic processes additionally complicates the device description and make a target device development difficult. However, for applications in neuromorphic circuits retention times of few months to years might be sufficient. If a separation of ionic and electronic processes is possible, interfacial resistive switching represents promising opportunities for neuromorphic circuits.

The combination of ionic and electronic processes for resistive switching in a single memristive cell was investigated in [Maz:6]. Therein, a double barrier device with an ultra-thin memristive layer sandwiched between a tunnel barrier and a Schottky-like contact is presented. The layer sequence of the device is Al/Al₂O₃/Nb_xO_y/Au, with a thickness of 1.3 nm for the Al₂O₃ tunnel barrier and 2.5 nm for the Nb_xO_y layer, as sketched in Fig. 3.2(c) together with a characteristic I-V curve of this device. In particular, as shown in Fig. 3.2(e) a highly uniform current distribution for the LRS (low resistance state) and HRS (high resistance state) for areas ranging between 70 μm² and 2300 μm² were obtained, which indicates a non-filamentary based resistive switching mechanism.

In order to get a deeper understanding of the particular interfacial contributions to the observed switching characteristics, single barrier devices were fabricated, i.e. an Al/Al₂O₃/Nb_xO_y/Nb tunnel junction excluding the Schottky contact (cf. Fig 3.2(a)) and an Nb/Nb_xO_y/Au Schottky contact without the tunneling barrier (cf. Fig 3.2(b)). By analyzing those experimental data in detail and with the help of an equivalent circuit model (see calculated I-V curve in Fig 3.2(d)) it has been shown evidence in [Maz:6] that resistive switching originates from oxygen diffusion and modifications of the local electronic interface states within the Nb_xO_y layer, which influences the interface properties of the Au (Schottky) contact and of the Al₂O₃ tunneling barrier, respectively.

The presented device in [Maz:6] offers several benefits: For example, the properties of the Al₂O₃ tunnel barrier could define the lower resistance boundary (i.e. the LRS) of the junction. In particular, amorphous Al₂O₃ is known to be a good tunnel barrier (i.e. elastic electron tunneling dominates

the transport), where the barrier thickness can be effectively controlled during growth [Gur83]. The tunnel barrier thickness acts as a current limiter and represents an essential design parameter as it is explained in detail in [Maz:6]. The tunnel barrier and the gold electrode define chemical barriers for the ionic species, confining them within the Nb_xO_y . A saturation of the ion density (number of ions per area) at either interface will define the LRS and HRS, respectively. Moreover, no current compliance is needed due to the self-limited ion assembly at either interface. The finite activation energies of the ionic species will lead to a frozen (memory) resistance state in case of zero bias and will therefore improve the data retention compared to a purely electronic switching mechanism, which face a voltage-time dilemma [Sch10].

3.1.3 Ferroelectric Tunnel Junctions

(from [Maz:7])

Ferroelectric tunnel junctions are purely physical switching based memristive devices, whose function is based on ferroresistive switches and consist of an ultra-thin ferroelectric material as tunnel barrier. By applying an external voltage, the electrical field across the tunnel junction induces a polarization reversal in the ferroelectrical tunneling layer and changes therewith the transmission probability for the tunnelling electrons. This concept seems promising [Tsy06], specially for neuromorphic applications [Cha12]. But different switching mechanisms, such as redox based interfacial switches, might contribute additionally to the switching characteristics and complicate the analysis of experimental data [Koh08].

In [Maz:7] the role of ferroelectric/electrode interfaces and the separation of the ferroelectric-driven TER effect from electrochemical (“redox”-based) resistance-switching effects is investigated. Therefore a comprehensive study of epitaxial junctions comprising BaTiO_3 barrier, $\text{La}_{0.7}\text{Sr}_{0.3}\text{MnO}_{0.3}$ bottom electrode and Au or Cu top electrodes has been done, which demonstrates a giant electrode effect on the tunneling electro resistance of these asymmetric ferroelectric tunnel junctions. The revealed phenomena are attributed to the microscopic interfacial effect of ferroelectric origin, which is supported by the observation of redox-based resistance switching at much higher voltages.

3.1.4 Exploring Resistive Switching Effects on the Atomistic Scale

(from [Maz:8] and [Maz:9])

As it has been discussed in the previous part of this chapter, the relevant effects for the resistive switching occurring at the atomistic and mesoscopic scale. However, even after an intensive study of resistive switching phenomena in insulator materials since the 1960s, the understanding of relevant effects for the resistive switching phenomena on the atomistic and mesoscopic scale are still under debate and various mechanisms have been proposed [Was09]. Thus, new measurement strategies which allow to study resistive switching effects at the atomistic length scale are strongly asked for. Thus, a direct access to the active part of the device for structural, electrical, and chemical characterization is desired and might be delivered by using lateral resistive switching junctions.

In [Maz:8] a simple and robust strategy to enable such a direct view to the active part of resistive switching devices at the atomistic scale is presented. In particular, electron beam lithography (EBL) was employed to define nanometer size bridges on oxide substrates and a subsequent controlled electromigration according to the method of Ref. [Str05] was used to define nanometer sized lateral junctions on SiO_2 and TiO_2 , as archetypical resistive switching insulator materials. In particular, two different kinds of resistive switching behaviours were observed after electroformation under vacuum conditions: Unipolar resistive switching for junctions on SiO_2 and bipolar resistive switching for those junctions which have been realized on TiO_2 substrates. Hence, [Maz:8] shows that the common switching behaviors can also be reached in lateral geometries with nanometer separated electrodes with the advantage to get access to the active part of the memristive device.

The most striking part of the method presented in [Maz:8] is, however, the electron beam lithography step of the nanometer size bridges, which limited the number of available junctions. Thus, a high resolution lithography technique, which allows to texture large substrate areas combined with a nanometer feature size and which reduces in an addition the lithography expense is highly required. In [Maz:9] such a lithography technique is presented. Therefore, UV- capillary force lithography was employed, which allows to imprint a multiscale system, consisting of 250 nm wide nano bridges and a 8-20 μm wide wiring in one lithography step. Moreover, it is shown that an additional annealing step to 75°C improves capillary rise.

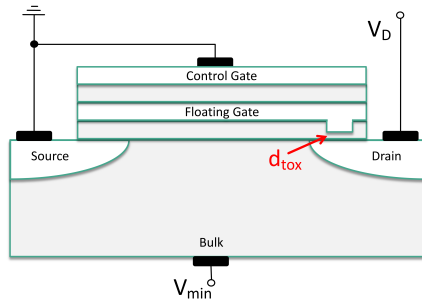


Figure 3.3 MemFlash cell: Diode configuration wiring scheme of an EEPROM cell that enables a memristive operation mode. Adapted from [Maz:10].

3.2 Floating Gate Transistors as Memristive Devices

In neuromorphic engineering the use of non-volatile memory devices for the emulation of synaptic functionality has been a long tradition and already in the first days of floating gate transistors those devices were used in artificial neural networks [Dio96, Car89]. Therefore, it is important to mention that integrated silicon circuit technology (VLSI), which is based on field effects transistor (FET), is today's mature technique for the realization of artificial neuronal circuits [Mea89]. This technique had its breakthrough in 1991, when Mahowald and Douglas [Mah91] were able to realize an analogue integrated circuit with the functional characteristics of real nerve cells for the first time. However, despite the success of VLSI based circuits, two-terminal memristive devices may allow several inventions to neuromorphic circuits, such as a reduced circuit complexity due to the simultaneous write/read access, improved power consumption compared with the possibility to down-scale the device into the nanometer range. In particular, three-terminal floating-gate transistors may not be regarded as memristive devices according to Eq. 2.4, since in those devices read and write processes are independent cycles, whereas for memristive devices the simultaneous read/write functionality is required. In the following such a memristive operation model of a floating gate transistor and his applications for neuromorphic circuits are briefly overviewed by summarizing the original publications [Maz:10] - [Maz:12].

3.2.1 MemFlash: Working Principle and Device Model

(from [Maz:10] and [Maz:12])

The in [Maz:10] presented specific wiring scheme of a single EEPROM cell (electrical erasable programmable read only memory) that enables the memristive operation mode of the device is depicted in Fig. 3.3. In order to ensure the memristive operation mode the external accessible terminals source (S) and control gate (CG) are connected to the common ground potential of the circuitry, while a bipolar voltage supply is connected to the drain terminal (D). Further, the bulk terminal (B) is set to the minimum voltage of the bipolar voltage supply in order to guarantee the formation of a conductive channel between source and drain and to avoid a short-circuit fault to the source. The obtained current-voltage characteristics of the two-terminal circuit using a single EEPROM cell is depicted in Fig. 3.4(a). Therefore, the bipolar voltage is linearly ramped between ± 12 V, while the drain current is recorded simultaneously.

The functional working principle of the MemFlash cell can be understood, as discussed in [Maz:10], in the framework of the Fowler-Nordheim tunneling process. At positive voltages electrons are tunneling from the floating gate (FG) through the tunneling oxide into the channel and vice versa for negative voltages applied to the drain terminal. Hence, depending on the current charge on the floating gate during the voltage sweep the device resistance is affected. Following [Maz:10] those changes can be illustrated in a purely capacitive device model, in which the floating gate potential for the MemFlash cell reads

$$V_{FG} = \frac{Q_{FG}}{C_T} + k_D V_D, \quad (3.1)$$

where Q_{FG} is the charge stored on the floating gate and k_D the coupling constant to the floating gate defined as $k_D = C_D/C_T$ with C_D the drain capacitance and C_T the total capacitance consisting of the sum of a respective capacitances $C_T = C_C + c_D + C_S + C_B$. In fact, Eq. 3.1 suggests that V_{FG} depends on both the current voltage V_D applied to the drain terminal, as well as on their history through Q_{FG} , which can be calculated by

$$Q_{FG} = Q_{FG}(t_0) + \int I_{FN}(V_{FG}, V_D) dt, \quad (3.2)$$

where I_{FN} is the Fowler-Nordheim tunneling current, which mostly dominated the charging and discharging of the floating gate during V_D voltage

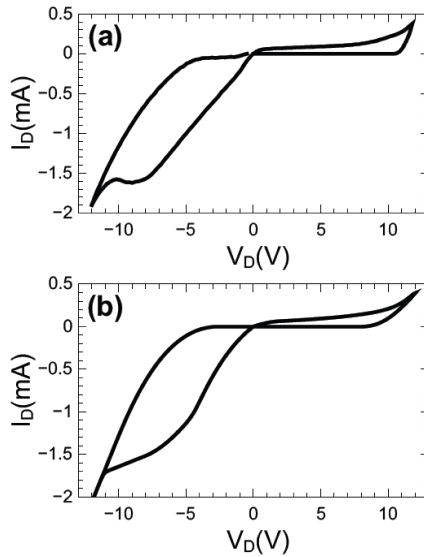


Figure 3.4 Comparison of an experimental (a) and a simulated (b) current-voltage characteristic of the two-terminal circuit, addressing a single EEPROM cell. The used simulation parameters are taken from [Maz:12].

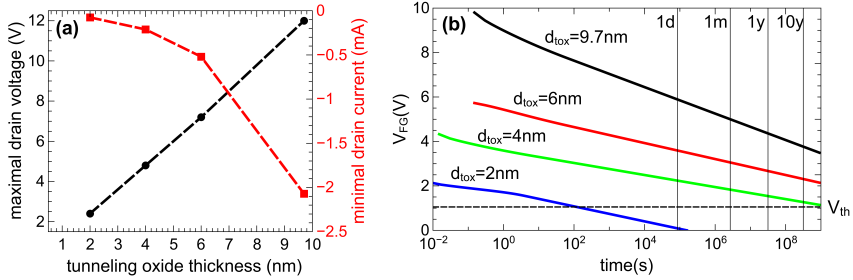


Figure 3.5 (a) Estimation of power consumption for thinner tunneling oxides. (b) Resulting retention times of the floating gate potential for different tunnelling oxide thicknesses. Figures are adapted from [Maz:12].

sweeps. However, as discussed in [Maz:12] localized defect states inside the tunneling oxide, described by the Poole-Frenkel current, as well as injections of hot electrons might contribute additionally to the overall charging and discharging process of V_{FG} and have to be taken into account for a physical modeling of the device behavior [Maz:12]. By taking those contributions into account and by using the standard MOSFET equations, the I - V curve shown in Fig.3.4(b) can be obtained from the simple capacitive device model.

3.2.2 Down-Scaling of Floating Gate Oxide Thickness (from [Maz:12])

The most striking disadvantage of a MemFlash cell compared to state-of-the-art memristive devices is the power consumption. This may cause problems for usages in large circuits with many of these cells. One reason for the high power consumption of the investigated cell is that the cells have a floating gate area of $A_{FG} = 84.98 \mu m^2$ [neb02]. State-of-the-art EEPROM cells consist of floating gate areas in the nanometer range [Sze07], which would reduce the source drain current by several orders of magnitude. On the other hand commercial EEPROM cells are designed for memory applications, for which data retention of more than 10 years is required with the disadvantages of the need of relatively high programming voltages. At this respect, the gate oxide thickness represents a trade-off between low bias voltage (for low power consumption) and a safe data storage over years in conventional

EEPROM cells. For neuromorphic circuit applications a retention time of 10 years might not be necessary. Therefore thinner floating gate oxide thicknesses could be accepted, leading to lower power consumption during programming. In [Maz:12] the influence of thinner floating gate oxide thicknesses on the MemFlash concept is investigated. It has been found that thinner tunneling oxides provide a good trade off between power consumption and data retention, as shown in Fig.3.5.

3.2.3 Application in Neuromorphic Systems

(from [Maz:11] and [Maz:12])

In [Maz:11] the opportunities of a MemFlash cell for the use in future neuromorphic circuits to mimic synaptic plasticity process are discussed. In particular, a learning rule was derived by the comparison to those memristive devices, which can be modeled in accordance to the ideal Memristor model described through Eq. 2.4. However in contrast to state-of-the-art memristive devices, the state variable of the MemFlash cell is not directly proportional to the device conductance. It is rather defined by the floating gate charge Q_{FG} . Consequently, the synaptic weight change can be expressed in accordance to Sec. 2.3 by

$$\frac{d\omega}{dt} = \frac{Q_{FG}}{dt} = I_{FN}(V_{FG}, V_D). \quad (3.3)$$

This relation is proportional to the tunneling current and controllable by the applied voltage on the drain terminal in the memristive operation mode of the EEPROM cell. In particular, as discussed in [Maz:11] and [Maz:12] this learning rate exhibits two important characteristics of synaptic learning. First, the learning rate exponentially changed with the applied voltage, which is due to the underlying Fowler-Nordheim tunnelling process. Second, the learning rate saturates after the exponential change to a constant value due to the finite storage capacitance of the floating gate. Therefore the finite capacitance of the floating gate stack introduces a saturation limit for the synaptic weight, which might be relevant in the context with more advanced learning rules as discussed in chapter 2. Hence, together with their behaviour that the device conductance can be precisely adjusted the MemFlash cell can be regarded as a realistic substitute for artificial synapses.

4 Neuromorphic Systems

The impressive properties of single memristive devices for synaptic plasticity emulation, as discussed in the previous chapters, make memristive devices to one of the promising candidates for future neuromorphic circuits. But how is it possible to implement neural circuits based on memristive devices? In particular, since the possible benefits of memristive devices in neuromorphic circuits are not that obvious and the current research mainly focus on the development of single devices rather regarding their network behavior.

This chapter addresses the question how to integrate memristive devices in bio-inspired electronic circuits and focus on their particular benefit. Therefore, different neuromorphic circuit schemes are presented, which range from cellular networks for implicit learning [**Maz:13**] and anticipation [**Maz:4**] to a neural memristive network which allows unsupervised learning [**Maz:14**]. The common goal of all of those presented investigations was to explore essential requirements for the development of optimal memristive devices for neuromorphic circuits.

4.1 Learning and Memory at the Cellular Level

The possibility to get a detailed understanding of the human brain and to develop artificial brains at the same time seems to be hopeless if one considers the number of neurons and their interconnections. In particular, a human brain consists of up to 100 billion neurons, which are individually linked to each other representing a huge and complex network of 10^{14} to 10^{15} possible connections. Hence, suitable strategies are required, which allows to discover the unique functionalities of the human brain, i.e. the functionalities of memory and learning. In biology, Eric Kandel got successfully access to the principles of memory and learning by applying a radical reductionistic strategy [Kan76, Kan09]. By doing so, Kandel was able to show that the principles of implicit memory in mammal brains can be already understood on the cellular level, where learning alters the function and structure of neurons and their interconnection strength and where only a few of neurons

and synapses are involved. In particular, Kandel was able to discover the basic aspects of implicit learning, which underlies habituation, sensitization, and classical conditioning [Kan76, Kan09].

In the following a brief overview over the publications [Maz:4] and [Maz:13] is given, where Kandel's reductionistic strategy has been successfully applied.

4.1.1 Implicit Learning

(from [Maz:13])

In Fig.4.1(a) and (b) the basic concepts of implicit learning are schematically shown. Whereas habituation and sensitization are exclusively non-associative (c.f. Fig.4.1 (a)), classical conditioning exhibits an associative character (c.f. Fig.4.1 (b)). In [Maz:13] all of this forms of implicit memory has been emulated by using a single Pt/ $\text{Ge}_{0.3}\text{Se}_{0.7}$ / SiO_2 /Cu electrochemical metallization cell (cf. Sec. 3.1.1) together with a few cent cheap analogue electronic circuit, as sketched in Fig. 4.1(c).

In particular, the simple circuit of Fig.4.1(c) already enables to mimic associative learning, as it was first studied in 1927 by Ivan Pavlov and is referred in our days as Pavlov's dog [Pav28]. In Pavlov's experiment, food for the dog was used to activate an unconditioned stimulus (UCS). Pavlov's dog started to salivate (unconditioned response, UCR) when ever noticing food. The neutral stimulus (NS) was a ring of a bell. At first the ring alone did not lead to any salivation by Pavlov's dog. After a few training sequences, i.e. by feeding the dog and ringing the bell, Pavlov's dog learned to associate the neutral stimuli with that of the unconditioned stimulus. As a result Pavlov's dog salivated by even hearing the bell ring alone. The unconditioned response became a conditioned response (CR), while the NS became a conditioned stimulus (CS).

In [Maz:13] Pavlov's experiment was emulated with the circuit depicted in Fig. 4.1(c), which consists of a voltage adder to merge two weak stimuli which alone do not affect the resistive state of the memristive cell. Moreover, a voltage divider consisting of an ohmic resistance and the memristive cell was employed to emulate synaptic plasticity in terms of the voltage drop across the memristive device V_m in dependence of his resistant state. The response of Pavlov's dog (salvation) was mimicked by introducing a second threshold voltage V_{cth} using a comparator. Hence, V_{cth} offers the possibility to set an output criteria to the modulatory circuit, so that the comparator gives only

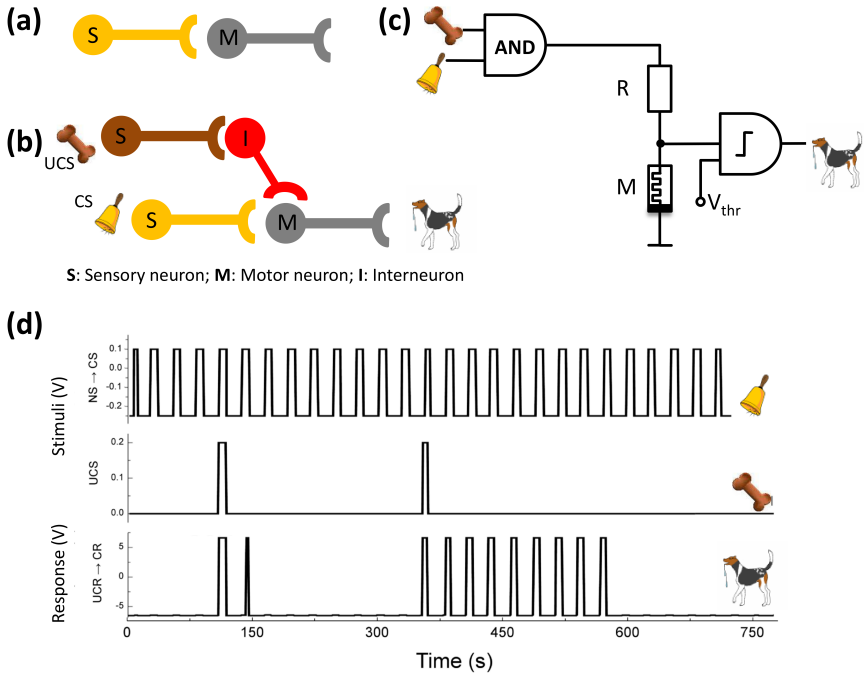


Figure 4.1 Implicit learning [Maz:13]: While a neural mediating circuit (a) for non-associative learning consists of a sensory neuron (S) and a motor-neuron (M), a neural circuit (b) for associative learning requires two sensory neurons (S), a strengthening interneuron (I), and a motor-neuron (M). (c) Electronic circuit layout for the emulation of implicit memory consisting of a voltage adder, a voltage divider including a linear ohmic resistance and a memristive device, and a comparator to mimic the response of the dog. (d) Experimental demonstration using a Pt/Ge_{0.3}Se_{0.7}/SiO₂/Cu based solid electrolyte nonvolatile memristive cell inside the voltage divider: If the neutral stimulus (upper curve) merges the unconditional stimulus (lower curve), the resistance of the system is enhanced. After two sequences the circuit learned to associate the neutral stimuli with that of the unconditioned stimulus, affecting an output of the comparator (response of the dog).

for $V_m = V_{cth}$ a distinct output signal, otherwise the initial value of $V_{init} = -6.5$ V is kept. In Fig. 4.1(d) the in [Maz:13] used periodic stimulus pulse train is shown, which reflects the process of associative learning as a result of the resistance transition from the inertial low resistance state (LRS) to his high resistance state (HRS). Moreover, if the conditional stimulus V_{CS} was applied a few times without V_{UCS} , a depression of the resistive state occurred because of a back transition from HRS to LRS. Hence, the overall resistance of the device decreased and the dog has extinct the before trained CR, when the bell alone was ringed eight times without presenting food.

Even though the presented memristive circuit are quite simple compared to those networks, which are responsible in mammal brains for memory and learning, it already shows evidence that memristive devices may provide a valuable benefit for future neuromorphic architectures. In particular, this investigation shows that memristive devices must exhibit a threshold voltage to be considered as a realistic substitute for basic building blocks in nerve cells. Thus, effective threshold voltages can be consider as fundamental design parameters in analogue neuromorphic circuits comprising memristive devices [Maz:13].

4.1.2 Towards Cognitive Systems: Anticipation

(from [Maz:4])

The cognitive capability of mammal brains is without doubt unique in nature and allows us to react to persons, objects, and external influences in a flexible and dynamical manner. Therefore, cognitive processes use the existing knowledge in order to generate new knowledge, i.e. the system performance is forced in dependence of previous learned events. In fact, this behavior is at the heart of decision making, which we are often confronted with during day. A basic functionality of a cognitive process is believed to be anticipation. This cognitive process allows a system to estimate future events and to react to it based on the history. Interestingly enough, anticipation can be already observed in simple unicellular organisms like amoeba, which are able to memorize and react to environmental changes by slowing down their locomotive speed [Ter08].

In a biological model the capability of anticipation of amoebas has been described in terms of an internal biological oscillator with a natural frequency [Ter08]. Varying environmental conditions may be different from this frequency so that amoebas can recognize patterns and predict events.

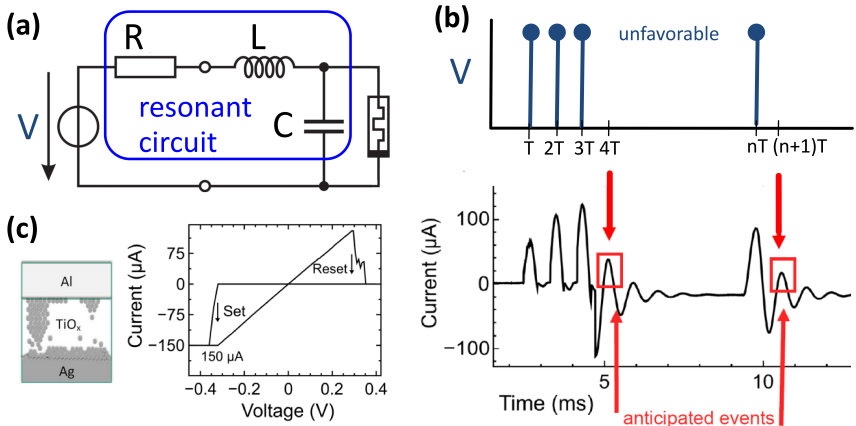


Figure 4.2 Emulation of anticipation [Maz:4]: (a) Schematic of the LC circuit used to mimic amoeba anticipating events according to Ref. [Per09]. (b) Experimental demonstration: If a periodic sequence of three pulses is applied (upper curve), the circuit learns and will react more efficiently to later voltage pulses (lower curve). (c) Schematic of the device stack and I - V curve of an Ag-doped TiO_{2-x} -based memristive device.

Pershin et al. [Per09] follow this idea and model amoeba anticipation with an electric LC circuit model including a memristive device, as depicted in Fig. 4.2(a). Moreover, these authors were able to expand the model of [Ter08] by a memory effect due to the memory behavior of memristive cells.

In [Maz:4], the in [Per09] proposed electric circuit model has been implemented. Therefore, a theoretical analysis of the electronic circuit has been employed in order to get important information about the transfer characteristic, resonant frequency, and damping behavior depending on the resistance state of the memristive device. In particular, it has been found that the transfer function of the circuit shows a pronounced peak at around the resonant frequency, which is drastically decreased with a decreasing resistance of the memristive device. While the shift in resonant frequency can be neglected in the high-resistance “Off” state of the memristive device. However, at the low-ohmic “On” resistance state of the memristive device the circuit is strongly damped, broadened, and the resonant frequency is shifted. As shown in [Maz:4] the in Fig. 4.2(c) (cf. Sec. 3.1.1) presented Ag/TiO_{2-x}/Al electrochemical metallization cell fulfills all of the theoretical defined circuit requirements and provides the desired damping behavior of the anticipation circuit, as depicted in Fig. 4.2(b).

4.2 Unsupervised Learning on Network Level

(from [Maz:14])

While the investigation of learning and memory processes at the cellular level provides important insights into the basic functionalities of neural systems and Kandel’s strategy has been applied very successfully to many systems [Kan09], there is still a considerable lack to explore the implications of those discovered principles at the system level. In other words the *brain code* is not yet understood and it is up to now practically impossible to develop neuromorphic systems which mimic the computing architecture of the entire brain. Thus, the realization of smaller networks which mimic specific feature of biological nerve systems are a more realistic approach. For example, the development of pattern recognition systems is here of interest, since it has many real world applications, such as autonomous robots and transportation, classifiers, front and speech recognition, and more general unsupervised learning strategies [Ste12].

In [Maz:14] the in [Que11, Que13, She14] reported computing paradigms

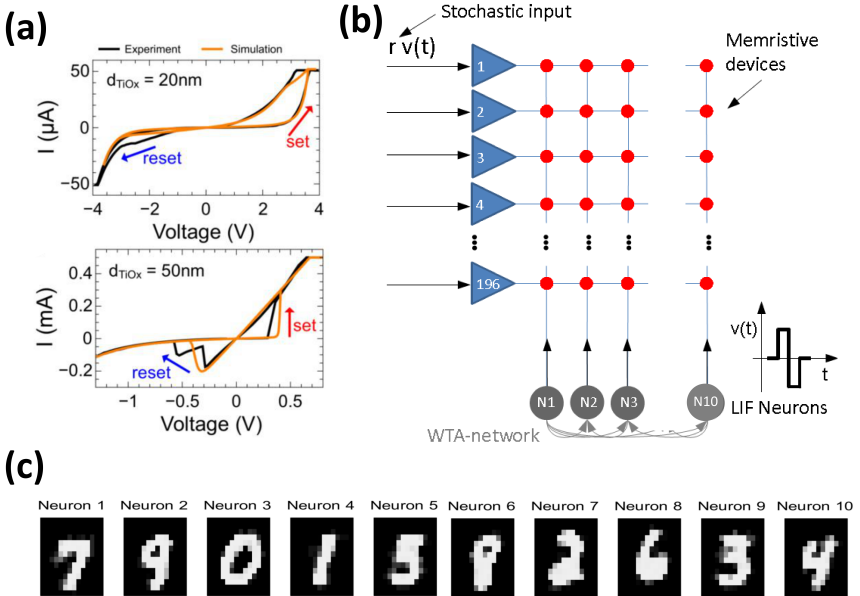


Figure 4.3 Pattern recognition [Maz:14]: (a) Typical I - V curves of $\text{Al}/\text{AlO}_x/\text{TiO}_{2-x}/\text{Al}$ devices comprising 20 nm thick TiO_{2-x} (upper curve) and 50 nm TiO_{2-x} (lower curve). Black lines correspond to I - V measurements, while orange lines are simulation results. (b) Schematic of the simulated neural network. Blue triangles correspond to the respective pixel of the input pattern, while gray circles are leaky integrate and fire output neurons (LIF), which are laterally coupled in an inhibitory winner-take-it-all network (WTA) topology. Red dots are the single memristive devices. (c) Obtained receptive fields for the ten output neurons of the neural network after unsupervised learning for memristive devices consisting of 20 nm thick TiO_{2-x} .

for pattern recognition have been used as guidelines to investigate the performance of memristive devices in a bio-inspired network for pattern recognition. In particular, simulations of a spiking neural network are presented in [Maz:14], which allows for pattern recognition. As input pattern handwritten digits, taken from the MNIST Data base, have been used [LeC98]. In total the MNIST Database consist of 60,000 handwritten digits from 250 different writers, while every digit is stored in a 256 grayscale image. The in [Maz:14] used feed-forward network is depicted in Fig. 4.3(b). Therein, the memristive devices are arranged in a cross-bar array connected by 196 input neurons and ten output neurons. While each input neuron corresponds to a specific pixel of the image of the input pattern, the output neurons were implemented as spiking neurons. In addition, the output neurons were inhibitoryly linked within a winner-take-it-all network and consist of a homeostasis-like behaviour for their spiking thresholds.

For the network memristive devices consisting of 20 nm and 50 nm thick TiO_{2-x} layers are experimentally explored, which are sandwiched in a capacitor-like structure between a metallic Al- (bottom and top) electrodes, and AlO_x tunneling barrier. While for 50 nm thick TiO_{2-x} devices, binary resistive switching was recorded (see Fig. 4.3(a) lower panel), a reduction of the oxide thickness to 20 nm leads to much more homogeneous resistance switching characteristics (see Fig. 4.3(a) upper panel). A physical-based equivalent circuit model is employed to analyze the obtained switching characteristics in some more detail and to provide a realistic device model for network level simulations.

In Fig. 4.3(c) the obtained receptive fields of the memristive devices at the specific site in the cross-bar-array assigned to each of their particular output neurons are shown. In particular, during learning each of the ten output neurons has learned without supervision one of the input digits and is capable to separate those digits thereafter. An important finding of [Maz:14] is that those devices which exhibit a homogeneous resistive switching behavior as well as a symmetric set and reset behaviour are suitable for pattern recognition.

Bibliography

- [And07] *The HippocampusBook*, Eds. P. Andersen, et al., 2007.
- [Aok14] Y. Aoki et al., *Bulk mixed ion electron conduction in amorphous gallium oxide causes memristive behaviour*, Nat. Commun. **5**, 3473 (2014).
- [Bai10] S.J. Baik and K.S. Lim, *Bipolar resistance switching driven by tunnel barrier modulation in TiO_x/AlO_x bilayered structure*, Appl. Phys. Lett. **97**, 072109 (2010).
- [Bai03] A. Baikalov, et al., *Field-driven hysteretic and reversible resistive switch at the Ag-Pr_{0.7}Ca_{0.3}MnO₃ interface*, Appl. Phys. Lett. **83**, 957 (2003).
- [Bea09] Mark F. Bear, Barry W. Connors, Michael A. Paradiso, *Neurowissenschaften. Ein grundlegendes Lehrbuch für Biologie, Medizin und Psychologie*, Hersg. Andreas K. Engel, 3. Auflage 2009, Spektrum Akademischer Verlag Heidelberg.
- [Bi98] Bi, Guo-qiang, and Mu-ming Poo. *Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type*, The Journal of neuroscience **18**, 10464-10472 (1998).
- [Bcm82] Elie L. Bienenstock, Leon N. Cooper, and Paul W. Munro. *Theory for the development of neuron selectivity: orientation specificity and binocular interaction in visual cortex*, The Journal of Neuroscience **2**, 32-48 (1982).
- [Bli73] T.V. Bliss, T. Lomo, *Long-lasting potentiation of synaptic transmission in the dentate area of the anaesthetized rabbit following stimulation of the perforant path*, J. Physiol, **232**, 331-356 (1973).

- [Byr09] *From Molecules to Networks: An Introduction to Cellular and Molecular Neuroscience*, Eds. by J. H. Byrne and J. L. Roberts, Elsevier Inc. 2009.
- [Car89] H.C. Card and W. R. Moore, *EEPROM synapses exhibiting pseudo-Hebbian plasticity*, Electronics Letters **25**, 805-806 (1989).
- [Cha12] A. Chanthbouala et al. *A ferroelectric memristor*, Nature materials **11**, 860-864 (2012).
- [Che15] A. Chen, J. Hutchby, v. Zhirnov, and G. Bourianoff, *Emerging Nanoelectronic Devices*, John Wiley and Sons Ltd, 2015.
- [Chu71] L. O. Chua, *Memristor-the missing circuit element*, IEEE Trans. Circ. Theo. **18**, 507 (1971).
- [Clo10] C. Clopath, and W. Gerstner. *Voltage and spike timing interact in STDP - a unified model*, Frontiers in synaptic neuroscience **21**, 25 (2010).
- [Cul43] W. McCulloch und W. Pitts, *A logical calculus of the ideas immanent in nervous activity*, Bulletin of Mathematical Biophysics **5**, 115-133 (1943).
- [Dio96] C. Diorio et al., *A single-transistor silicon synapse*, IEEE Transactions on Electron Devices **43**, 1972-1980 (1996).
- [Fuj05] T. Fujii et al., *Hysteretic current-voltage characteristics and resistance switching at an epitaxial oxide Schottky junction Sr-RuO₃/SrTi_{0.99}Nb_{0.01}O₃*, Appl. Phys. Lett. **86**, 012107 (2005).
- [Gau10] M Graupner, and N. Brunel. *Mechanisms of induction and maintenance of spike-timing dependent plasticity in biophysical synapse models*, Frontiers in computational neuroscience **4**, 136 (2010).
- [Ger02] Gerstner, Wulfram, and Werner M. Kistler. *Spiking neuron models: Single neurons, populations, plasticity*, Cambridge university press, 2002.
- [Gur83] M. Gurvitch, M. A. Washington, and H. A. Huggins, *High quality refractory josephson tunnel junctions utilizing thin aluminium layers*, Appl. Phys. Lett. **42**, 472 - 474 (1983).

-
- [Heb49] *Organization of Behavior*, D. O. Hebb, John Wiley (1949).
- [Hu11] J. Hu et al., *Impact of fixed charge on metal-insulator-semiconductor barrier height reduction*, Appl. Phys. Lett. **99**, 252104 (2011).
- [Jeo11] D.S. Jeong, B. Cheng, and H. Kohlstedt, *Pt/Ti/Al₂O₃/Al tunnel junctions exhibiting electro forming-free bipolar resistive switching behaviour*, Solid-State Electron. **63**, 1 (2011).
- [Jo10] Jo, Sung Hyun, et al. *Nanoscale memristor device as synapse in neuromorphic systems*, Nano letters **10**, 1297-1301 (2010).
- [Jos13] J. Joshua Yang, Dmitri B. Strukov, and Duncan R. Stewart. *Memristive devices for computing*, Nature nanotechnology **8**, 13-24 (2013).
- [Kan76] E. R. Kandel, *Cellular Basis of Behavior-An Introduction to behaviour Neurobiology*, W. H. Freeman and Company 1976.
- [Kan09] E. R. Kandel, *In Search of Memory*, W. W. Norton & Company Ltd. Castle House 2009.
- [Koh93] H. Kohlstedt, S. Kuriki, and K.-H. Gundlach, *Electro forming and telegraph noise in Pb/Bi/InOx/Pb/Bi tunnel junctions*, J. Appl. Phys. **73**, 2564 (1993).
- [Koh08] H. Kohlstedt et al., *Method to distinguish ferroelectric from non-ferroelectric origin in case of resistive switching in ferroelectric capacitors*, Appl. Phys. Lett. **92**, 062907 (2008).
- [Krz12] P. Krzysteczko et al. *The Memristive Magnetic Tunnel Junction as a Nanoscopic Synapse Neuron System*, Advanced Materials **24**, 762-766 (2012).
- [Lai08] Qianxi Lai et al., *An organic/Si nanowire hybrid field configurable transistor*, Nano letters **8**, 876-880 (2008).
- [LeC98] Y. LeCun, L. Bottou, Y. Bengio, and P. Haffner, *Gradient-based learning applied to document recognition*, Proceedings of the IEEE, **86**, 2278-2324 (1998).
- [Mah91] M. Mahowald and R. Douglas, *A silicon neuron*, Nature **354**, 515 - 518 (1991).

- [Mea89] Mead, C.A. *Analog VLSI and Neural Systems*, Reading, MA: Addison Wesley, 1989.
- [Mey08] R. Meyer, et al., *Oxide dual-layer memory element for scalable non-volatile cross-point memory technology*, NVMTS **9**, 1-5 (2008).
- [Mik14] E.Mikheev, B. D. Hoskins, D. B. Strukov, and S.Stemmer, *Resistive switching and its suppression in Pt/Nb:SrTiO₃ junctions*, Nat. Commun. **5**, 3990 (2014).
- [neb02] L. Nebrich, *Entwicklung eines Makromodells für die Schaltungs- und Zuverlässigungssimulation von EEPROM-Zellen im erhöhten Temperaturbereich*, Ph.D. thesis, Christian-Albrechts-University of Kiel, 2001.
- [Ohn11] T. Ohno, et al. *Short-term plasticity and long-term potentiation mimicked in single inorganic synapses*, Nature materials **10** 591-595 (2011).
- [Oja82] E. Oja, *Simplified neuron model as a principal component analyzer*, Journal of mathematical biology **15**, 267-273 (1982).
- [Pan12] D. Pantel et al. *Reversible electrical switching of spin polarization in multiferroic tunnel junctions*, Nature materials **11**, 289-293 (2012).
- [Par08] C. Park, Y. Seo, J. Jung, and D.-W. Kim, *Electrode-dependent electrical properties of metal/Nb-doped SrTiO₃ junctions*, J. Appl. Phys. **103**, 054106 (2008).
- [Pav28] Ivan P. Pavlov, *Experimental Psychology and Psychopathology in Animals*, Volume 1, pages 47-60 in Lectures on Conditioned Reflexes, New York: International Publishers 1928.
- [Per09] Y. V. Pershin, S. La Fontaine, and M. Di Ventra, *Memristive model of amoeba learning*, Phys. Rev. E **80**, 021926 (2009).
- [Que11] D. Querlioz, O. Bichler, and C. Gamrat, *Simulation of a Memristor-Based Spiking Neural Network Immune to Device Variations*, International Joint Conference on Neural Networks (IJCNN): 1775-1781 (2011).

- [Que13] D. Querlioz, O. Bichler, and P. Dollfus, *Immunity to Device Variations in a Spiking Neural Network with Memristive Nanodevices*, IEEE Transactions on Nanotechnology: 12, 288 - 295 (2013).
- [Ros58] Frank Rosenblatt, *The perceptron : a probabilistic model for information storage and organization in the brain*, Psychological Reviews **65**,386-408 (1958).
- [Saw06] A.Sawa, *Resistive switching in transition metal oxides Mater.*, Today **88**, (2006).
- [Sch10] H. Schroeder, V. V. Zhirnov, R. K. Cavin, and R. Waser, *Voltage-time dilemma of pure electronic mechanisms in resistive switching memory cells*, J. Appl. Phys. **107**, 054517 (2010).
- [Sha04] T. Shanahan, *The Evolution of Darwinism, Selection Adaption and progress in Evolutionary Biology*, Cambridge 2004.
- [She14] P. Sheridan, W. Ma, W. Lu, *Pattern Recognition with Memristor Networks*, Circuits and Systems (ISCAS), 1078 - 1081 (2014).
- [Ste12] T.C. Stewart, F.X. Choo, and C. Eliasmith, *Spaun: A perception-cognition-action model using spiking neurons*, Proceedings of the 34th Annual Conference of the Cognitive Science Society (2012).
- [Str05] D. R. Strachan, et al., *Controlled fabrication of nanogaps in ambient environment for molecular electronics*, Appl. Phys. Lett. **86**, 043109 (2005).
- [Str08] D. B. Strukov, et al. *The missing memristor found*, Nature **453**, 80-83 (2008).
- [Str12] D. B. Strukov and H. Kohlstedt, *Resistive switching phenomena in thin films: Materials, devices, and applications*, MRS Bulletin **37**, 108 (2012) and papers therein.
- [Sze07] S.M. Sze and K.K.Ng, *Physics of Semiconductor Devices*, New York: Wiley, 2007.
- [Ter08] T. Saigusa, A. Tero, T. Nakagaki, and Y. Kuramoto, *Amoebae anticipate periodic events*, Phys. Rev. Lett. **100**, 018101 (2008).

- [Tsy06] E. Y. Tsymbal and H. Kohlstedt, *Tunneling across a ferroelectric*, Science **313**, 181-183 (2006).
- [Wan12] Wei-Gang Wang et al. *Electric-field-assisted switching in magnetic tunnel junctions*, Nature materials **11** 64-68 (2012).
- [Was09] R. Waser et al. *Redox based resistive switching memories; nanoionic mechanisms, prospects, and challenges*, Advanced Materials **21**, 2632-2663 (2009).
- [Was12] R. Waser (Ed.). *Nanoelectronics and Information Technology*, Weinheim (Germany): Wiley-VCH, 2012 **21**, 2632-2663 (2009).
- [You10] Hu Young Jeong et al., *Graphene oxide thin films for flexible non-volatile memory applications*, Nano letters **10**, 4381-4386 (2010).
- [Zam11] C. Zamarreo Ramos, et al, *On Spike Timing Dependent Plasticity, Memristive Devices, and building a Self Learning Visual Cortex*, Front. Neurosci. **5**, 26 (2011).

Vita

Dr. rer. nat. Martin Ziegler

Date of birth: 24 January 1980

Nationality: German

Marital status: Married, three children

Work Experience

Since Apr 2010 Scientist at the Institute of Electrical and Information Engineering, Kiel University (research group: Nanoelectronics)

Mar 2006 - Mar 2010 Ph.D. student at the Institute of Experimental and Applied Physics, Kiel University (research group: STM)

Education

2003-2006 **Christian-Albrechts-Universität zu Kiel**
Oct 03 - Oct 04 Academic Studies of Physics
Nov 04 - Feb 06 Diploma Thesis in Elementary Particle Physics

2002-2003 **Université de Bordeaux I**
Sep 02 - May 03 Academic Studies of Physics
May 04 - July 04 Internship at the Observatory

2000-2002 **Technische Universität Darmstadt**
Apr 00 - Sept 02 Undergraduate Studies of Physics
Mar 02 Intermediate Diploma

1990 - 1999 **Heinrich-Böll-Schule in Hattersheim am Main**
June 1999 High School Diploma

List of Original Publications

- MAZ:1** Ziegler, M.; Hansen, M.; Ignatov, M.; Kohlstedt, H., *Building memristive neurons and synapses*, IEEE International Symposium on Circuits and Systems (ISCAS) 1066, 1069 (2014).
- MAZ:2** Ziegler, M., Riggert, C., Hansen, M., Bartsch, T., Kohlstedt, H., *Memristive Hebbian Plasticity Model: Device Requirements for the Emulation of Hebbian Plasticity Based on Memristive Device*, IEEE TBio CAS 9: 197-206 (2015).
- MAZ:3** Jeong, D.S., Kim, I., Ziegler, M., Kohlstedt, H., *Towards artificial neurons and synapses: a materials point of view*, RSC Adv. Volume: 3 Issue: 10 Pages: 3169-3183 (2013).
- MAZ:4** Ziegler, M., Ochs, K., Hansen, M., Kohlstedt, H., *An electronic implementation of amoeba anticipation*, Appl. Phys. A 114, , Issue 2, pp 565-570 (2014).
- MAZ:5** Soni, R., Meuffels, P., Adrian Petraru, Hansen, M., Ziegler, M., Vavra, O., Kohlstedt, H., Jeong, D. S., *Bipolar switching polarity reversal by electrolyte layer sequence in electrochemical metallization cells with dual-layer solid electrolytes*, Nanoscale 5, 12598-12606 (2013).
- MAZ:6** Hansen, M., Ziegler, M., Kolberg, L., Soni, R., Dirkmann, S., Mussenbrock, T., and Kohlstedt, H., *A double barrier memristive device*. Scientific Reports 5, 13753 (2015).
- MAZ:7** Soni, R., Petraru, A., Meuffels, P., Vavra, O., Ziegler, M., Kim, S. K., Jeong, D. S., Pertsev, N. A., Kohlstedt, H., *Giant electrode effect on tunneling electroresistance in ferroelectric tunnel junctions*, Nature Communications 5, 5414 (2014).
- MAZ:8** Ziegler, M., Harnack, O., Kohlstedt, H., *Resistive switching in lateral junctions with nanometer separated electrodes*, Solid-State Electronics Volume: 92, p. 24 - 27 (2014).

- MAZ:9** Hansen, M., Ziegler, M., Kohlstedt, H., Pradana, A., Rädler, M., Gerken M., *UV capillary force lithography for multiscale structures*, J. Vac. Sci. Technol. B 30(3) (2012).
- MAZ:10** Ziegler, M.; Oberlaender, M.; Schroeder, D.; Krautschneider, W., Kohlstedt, H., *Memristive operation mode of floating gate transistors: A two-terminal MemFlash-cell*, Appl. Phys. Lett. Volume: 101 Issue: 26 (2012).
- MAZ:11** Ziegler, M., Kohlstedt, H., *Mimic synaptic behavior with a single floating gate transistor: A MemFlash synapse*, J. Appl. Phys. Volume:114 Issue:19 (2013).
- MAZ:12** Riggert, C., Ziegler, M., Schroeder, D., Krautschneider, W.H., Kohlstedt, H., *MemFlash device: floating gate transistors as memristive devices for neuromorphic computing*, Semicond. Sci. Technol. 29, 104011 (2014).
- MAZ:13** Ziegler, M., Soni, R., Patelczyk, T., Ignatov, M., Bartsch, T., Meuffels, P., Kohlstedt, H., *An electronic version of Pavlov's dog*, Adv. Func. Mat. 143, Volume: 22 Issue: 13 Pages: 2744-2749 (2012).
- MAZ:14** Zahari, F., Hansen, M., Mussenbrock, T., Ziegler, M., and Kohlstedt, H., *Pattern recognition with TiOx-based memristive devices*, AIMS Materials Science 2: 203-216 (2015).