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Voltage Balancing of Modular Smart Transformers Based on Dual Active Bridges

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***Abstract*—Modular medium voltage power converters have gained increasing attention in context of Smart Transformers (STs) in the electrical distribution grid. A possible ST architecture can be built by a Cascaded H-Bridge (CHB) converter in the Medium Voltage side and Dual Active Bridges (DABs) in the isolation stage. One of the main issues in the CHB control is represented by the voltage balancing. This work investigates the control for the two converter stages comparing the voltage balancing by the MV stage with the voltage balancing by the isolation stage under unbalanced loading conditions. The proposed balancing technique, applied in the isolation stage is demonstrated to offer higher bandwidth than the commonly used balancing in the MV-stage, which is especially important in case of high number of CHB-cells and different power transfer of the CHB cells. These conclusions are supported by simulation and experimental results.**

I. Introduction

The increasing electric power generation by renewable energy sources connected to the electrical distribution grid leads to the challenge for the grid operators to balance the time varying power injection. The ST, which is a power electronics based transformer with additional control and communication capability, is a possible solution to perform this management and to increase further the hosting capacity for renewable energy sources [1]. A remaining challenge for this system is to maintain a high quality of service by means of a high availability for the grid when installing STs instead of traditional transformers in the electrical distribution grid.

Modular power converters enable to realize the ST with standard power semiconductors and to include fault tolerance for increasing the availability of the system. Thereby, the ST based on the CHB-converter connected to DABs is a promising solution [2], [3] . Particularly, the use of Silicon requires a high number of H-bridges to connect the power converter to the MV grid, because these devices are limited in the blocking voltage. The high number of cells challenges the voltage balancing of the converter, which is commonly applied in the medium voltage stage of the ST as shown in Fig. 1, where $V_{DC,i}$ denotes the i-th output voltage of the AC/DC power conversion stage and V_o the LV DC link voltage. With a high number of cells, the switching frequency of the single devices is low and special algorithms are required to balance the DC-links [4], [5].

The voltage balancing control is getting even more important in case of a unsymmetrical loading of the different building blocks [6], [7]. Unequal processed power leads to different voltage ripples on the capacitors in the H-bridge of the CHB-converter and power variations affect a variation of the DC-link voltage. Particularly the voltage variations caused by power variations should be minimized for not affecting the power transfer of the system. To reduce the effect of the power variations on the voltage variations without increasing the DC-link capacitance, the DC-links in the CHB converter need to be balanced with fast dynamics [8].

In order to obtain a balancing controller with fast dynamics, in this paper the balancing controller is operated at the isolation stage level while a stress-balancing controller is applied to the MV stage. It does not balance the power in the DAbs, but the stress for the components in the system as shown in Fig. 2.

First, this work develops the average model and a small signal model for the balancing controller in the isolation stage in section II and demonstrates the controller design in section III. The superior dynamics are demonstrated analytically in section IV and the models are validated experimentally in section V. For this purpose, the voltage balancing in the isolation stage is implemented on a low voltage test bench and compared to the voltage balancing by the medium voltage stage. Finally, the results are concluded in section VI.

II. System Description and Modeling

The analyzed ST consists of a single phase active rectifier in the MV stage connected to isolated DC/DC converters (DABs) in the isolation stage. The DABs are series connected in the MV stage and parallel connected in the Low Voltage (LV) stage, feeding a common load. This is shown in Fig. 3 for a 5-level CHB, which is considered in the design of the average model for greater clarity. Despite performing the analysis only for the 5-level CHB, the analysis can be extended to a higher number of levels.

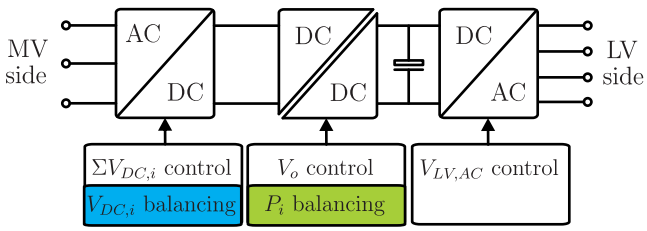

Fig. 1: Voltage balancing performed by the MV-inverter

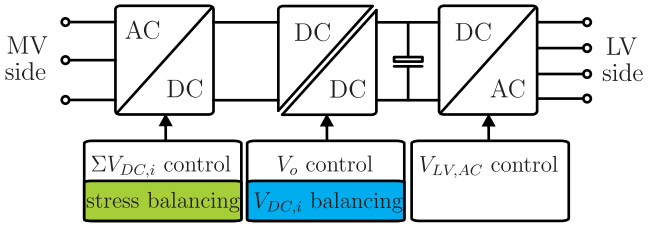

Fig. 2: Voltage balancing performed by the DC/DC converter.

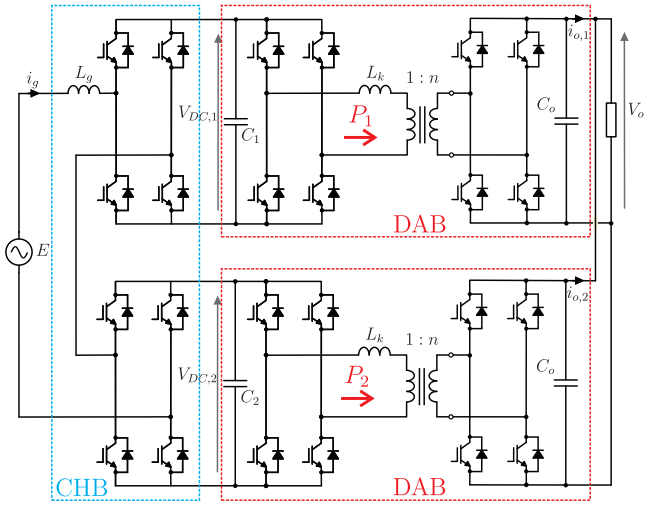

Fig. 3: ST architecture based on the CHB and DABs.

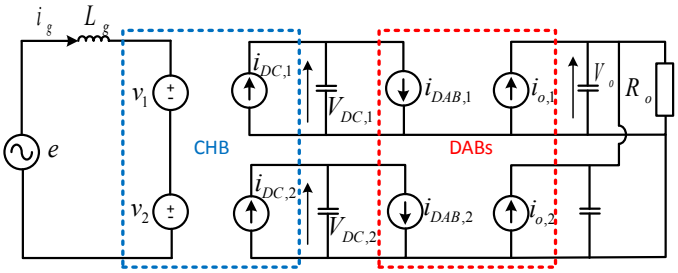

Fig. 4: CHB and DAB Average Model for $N = 2$.

A. Average model of the ST

The average model of the ST is developed to derive the small signal model and the tuning procedure of every control loop. A complete scheme is depicted in Fig. 4. The CHB is represented as the sum of $N = 2$ voltage sources connected to the main grid voltage E through an inductive filter L_g. The output voltage of each CHB cell v_i is modeled in the AC side with (1), where $V_{DC,i}$ is the corresponding DC-link voltage and m_i the corresponding modulation index.

$$v_i = V_{DC,i} m_i \quad \textit{with i=1,2} \tag{1}$$

The $i-th$ DC-side current of the CHB $i_{DC,i}$ can be expressed with (2).

$$i_{DC,i} = i_g m_i \quad \textit{with i=1,2} \tag{2}$$

The DABs are represented in MV-side and LV-side as current sources with the MV-side current $i_{DAB,i}$ and the LV-side current $i_{o,i}$, which can be expressed with (3) - (4).

$$i_{DAB,i} = \frac{V_o T_{DAB} \varphi_i (1-\varphi_i)}{2 L_k n} \quad \textit{with i=1,2} \tag{3}$$

$$i_{o,i} = \frac{V_{DC,i} T_{DAB} \varphi_i (1-\varphi_i)}{2 L_k n} \quad \textit{with i=1,2} \tag{4}$$

Here T_{DAB} is the DAB switching period, φ ($-0.5 < \varphi < 0.5$) is the phase-shift between the primary and secondary voltage of the Medium Frequency Transformer (MFT), n is the MFT turn ratio, L_k is the leakage inductance. V_{DC} and V_o are the input and output DAB voltages.

B. Small signal model of the CHB

Based on the average model of the CHB in Fig. 4 the system is transformed from the stationary reference frame into the rotating system [9]. The small signal model of the CHB is derived, whereas m_1 and m_2 are the modulation indexes of the H-bridge 1 and H-bridge 2, respectively:

$$L_g \frac{di_g}{dt} = m_1 V_{DC,1} + m_2 V_{DC,2} - e \tag{5}$$

In the following $m_1 = m_2 = m$ and $V_{DC,1} = V_{DC,2} = V_{DC}$ are assumed and Kirchhoff's current law is applied to the MV-side DC-link in (6).

$$C \frac{dV_{DC}}{dt} = \frac{1}{2} m i_g - i_{DAB} \tag{6}$$

Assuming the second-order signal perturbations to be zero, the small-signal linearization of (5) and (6) leads to:

$$L_g \frac{d\tilde{i}_g}{dt} = 2\tilde{m} V_{DC} + 2M\tilde{V}_{DC} \tag{7}$$

$$2C \frac{d\tilde{V}_{DC}}{dt} = \tilde{m} I_g + M\tilde{i}_g - 2\tilde{i}_{DAB} \tag{8}$$

This is transformed into the Laplace domain in (9)-(10).

$$\tilde{i}_g(s) = \frac{2\tilde{m}(s) V_{DC} + 2M\tilde{V}_{DC}}{L_g s} \tag{9}$$

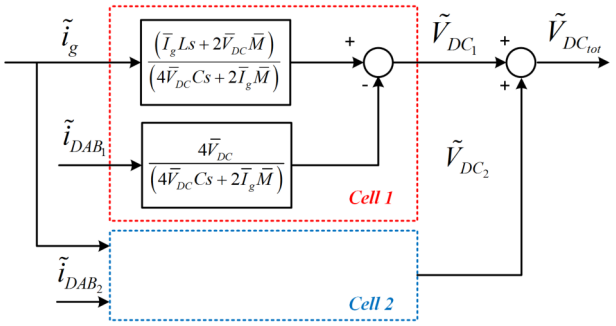

Fig. 5: CHB Small Signal Model for $N = 2$.

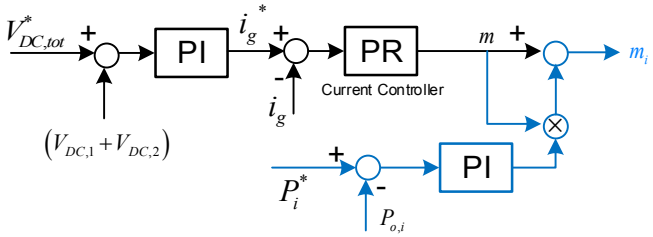

Fig. 6: Control scheme of the CHB-converter for $N = 2$.

$$\tilde{V}_{DC} = \frac{\tilde{m} I_g + M \tilde{i}_g - 2\tilde{i}_{DAB}}{2Cs} \tag{10}$$

From (9), the small signal modulation signal $\tilde{m}$ is derived as:

$$\tilde{m}(s) = \frac{L_g \tilde{I}_g(s) s - 2M \tilde{V}_{DC}}{2V_{DC}} \tag{11}$$

By substituting (11) in (10), the transfer function between the DC-link voltage $\tilde{V}_{DC}$ and the correspondent AC current and MV-side current of the DAB is obtained. The resulting transfer function is expressed with (12).

$$\begin{aligned} \tilde{V}_{DC}(s) = & \frac{I_g L_g s + 2V_{DC} M}{4V_{DC} C s + 2 I_g M} \tilde{i}_g(s) \\ & - \frac{4V_{DC}}{4V_{DC} C s + 2 I_g M} \tilde{i}_{DAB}(s) \end{aligned} \tag{12}$$

Finally, the resulting small signal model of the 5-Level CHB is shown in Fig. 5.

C. Small signal model of the DAB

From the average model of the DAB in Fig. 4, the small signal-linearization of the $i-th$ DAB in the MV-side and the LV-side respectively leads to:

$$\tilde{i}_{DAB,i} = \frac{T_{DAB}}{2L_k n} [\tilde{\varphi}_i (1 - 2\Phi_i) V_{o,i} + \tilde{V}_{o,i} (1 - \Phi_i) \Phi_i] \tag{13}$$

$$\tilde{i}_{o,i} = \frac{T_{DAB}}{2L_k n} [\tilde{\varphi}_i (1 - 2\Phi_i) V_{DC,i} + \tilde{V}_{DC,i} (1 - \Phi_i) \Phi_i] \tag{14}$$

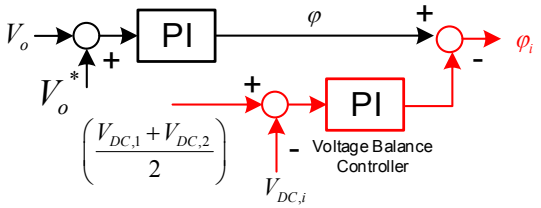

Fig. 7: Control scheme of the DAB-converter for $N = 2$.

Applying Kirchhoff's voltage law to output port of the two DAB, considering equal parameter for each DABs, (16) is obtained:

$$\tilde{i}_o = \tilde{i}_{o,1} + \tilde{i}_{o,2} \qquad \tilde{V}_o = \frac{R_0}{R_0 C_0 s + 1} \tilde{i}_o \tag{15}$$

Substituting (15) in (14) leads to:

$$\tilde{V}_o = \frac{R_0}{R_0 C_0 s + 1} \frac{T_{DAB}}{L_k n} [\tilde{\varphi}(1 - 2\Phi) V_{DC} + \tilde{V}_{DC}(1 - \Phi)\Phi] \tag{16}$$

III. Controller Design

A. CHB-grid current and DC-voltage control loop

The control of the DC voltage through the AC current is implemented in two loops, an outer DC voltage control loop and an internal current control loop as shown in Fig. 6. The inner loop is tuned to achieve short settling times, while the outer loop is tuned for optimum regulation and stability. If the current control loop is adjusted to be optimally damped a second-order transfer function $G_i(s)$ is derived for the current loop [10]:

$$G_i(s) = \frac{\tilde{i}_g}{\tilde{i}_g^*} = \frac{\frac{2}{(3T_s)^2}}{s^2 + \frac{2}{3T_s} s + \frac{2}{(3T_s)^2} s)^2} \tag{17}$$

Then, the open loop transfer function of the voltage control loop leads to:

$$\frac{\tilde{V}_{DC,tot}}{(V^*_{DC,tot} - \tilde{V}_{DC,tot})} = G_i(s) \frac{K_p (T_i s + 1)}{T_i s} \frac{I_g L_g + 2V_{DC} M}{2V_{DC} C s + I_g M} \tag{18}$$

K_p and T_i are the parameters of the PI-controller and they are tuned in order to guarantee voltage loop dynamics, which is at least ten times slower then the closed current loop. The effect of $\tilde{i}_{DAB}$ in (12) has been considered as an external disturbance.

B. DABs Output Voltage control loop

The control scheme of the DABs is shown in Fig. 7. Based on (16), which represents the differential equation of the DABs output voltage, a control law can be defined considering φ as the control variable and V_{DC} as a measurable disturbance. The effect of V_{DC} in the behavior of the output voltage V_o can be reduced with a feed forward and results in (19).

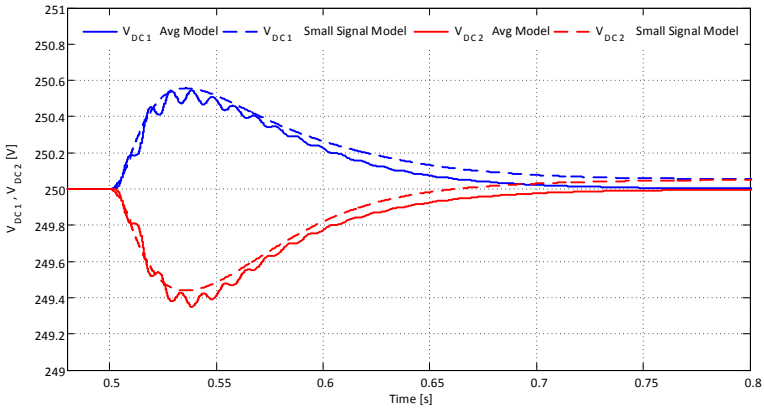

Fig. 8: Comparison of the small signal model with the average model of the converter.

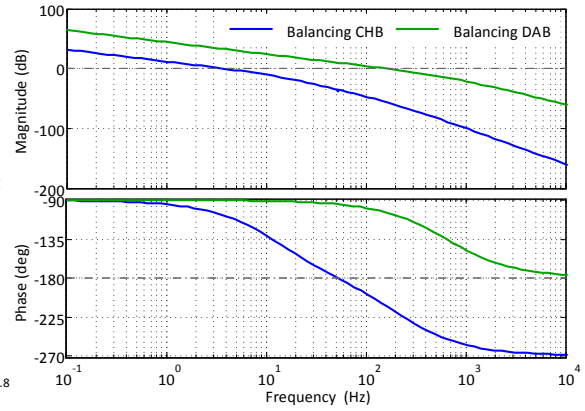

Fig. 9: Comparison of the bandwidth for capacitor balancing in the MV-stage and in the isolation stage.

$$\frac{\tilde{V}_o}{(V_o^* - \tilde{V}_o)} = \frac{T_{DAB}(1-2\Phi)V_{DC}}{L_k}\frac{K_{po}}{T_{io}}\frac{T_{io}s+1}{s}\frac{R_0}{R_0C_0s+1} \tag{19}$$

K_{po} and T_{io} are the proportional and the integral constant value respectively. Choosing T_{io} equal to R_oC_o (pole-zero cancellation), the resulting closed loop transfer function $G_{Vo}(s)$ is derived:

$$G_{Vo}(s) = \frac{K_{DAB}K_{po}}{s + K_{DAB}K_{po}} \quad with \quad K_{DAB} = \frac{T_{DAB}(1-2\Phi)V_{DC}}{L_kC_o} \tag{20}$$

This transfer function represents a first order system with a bandwidth dependent on the value of K_{po}, whereby increasing $K_{po} > 0$ improves the tracking and increases the disturbance rejection capability.

C. DABs input voltage balancing loop

The ability to impose a different power reference in the DABs is closely related to the concept of DC-link voltage balancing. In fact, the voltage control loop is not able to balance the DC-link voltage. To avoid overvoltages for the power semiconductors, it is necessary to introduce an additional control loop in the DAB control stage. Such control is carried out with a PI controller for each DC-link. Considering also the acquisition and the PWM delay, the open loop transfer function of the balancing loop is:

$$G_{BAL,i}(s) = \frac{K_{p,BAL,i}(1-2\Phi)V_{DC}}{3L_kC} \cdot \frac{s + \frac{1}{T_{BAL,i}}}{s(s+\frac{1}{1.5T_{DAB}})(s+\frac{I_gM}{2V_{DC}C})} \tag{21}$$

Choosing $T_{BAL,i} = \frac{2V_{DC}C}{I_gM}$ and thereby cancelling the slower pole, the new open loop transfer function is:

$$G_{BAL,i}(s) = \frac{K_{p,BAL,i}(1-2\Phi)V_{DC}}{3L_kCs(s+\frac{1}{1.5T_{DAB}})} \tag{22}$$

IV. Model validation and controller comparison

The obtained average model is compared to a switching model in Matlab/Simulink and Plecs in Fig. 8. The DC-link voltages are shown and at $t = 0.5$ the power in DAB 1 is increased, while it is reduced in DAB 2, maintaining the same output power. It can be seen that the step in the power implies a transient variation of the DC-link voltage variation and the average model fits well the switching model with only a small deviation.

A comparison of the proposed voltage balancing controller performed by the DABs is made with the commonly used balaccing performed in the MV-converter. Based on the open loop transfer function for both systems, the crossover frequency is a good index for the estimation of the bandwidth and the speed. The open loop transfer function of the classical controller $\tilde{V}_{MVbalancing,DC,i}$ is expressed with (23).

$$\tilde{V}_{MVbalancing,DC,i} = K_{sys}K_{p,BAL}\frac{1}{1.5T_{CHB}s+1}\frac{1}{L_gs+R_g} \cdot \frac{R_i}{R_iCs+1}\frac{T_{BAL,i}s+1}{T_{BAL,i}s}\left(\frac{\tilde{V}_{DC,1}+\tilde{V}_{DC,1}}{2} - \tilde{V}_{DC,i}\right) \tag{23}$$

The crossover frequency in both models is derived for a fixed phase margin of 75 °, showing a significant difference in the bandwidth of the two controllers ($BW_{CHB} = 4\,Hz$, $BW_{DAB} = 160\,Hz$) and the disturbance rejection capability. The voltage balancing controller in the isolation stage is superior to the commonly implemented controller in the MV stage, because of the higher switching frequency in the isolation stage. This is commonly required for the medium frequency DC/DC converters, while the switching frequency of the DAB is targeted to be minimized for minimizing the related switching losses.

The different dynamic performances can be observed also in Fig. 10 and Fig. 11 respectively. As expected from the Bode

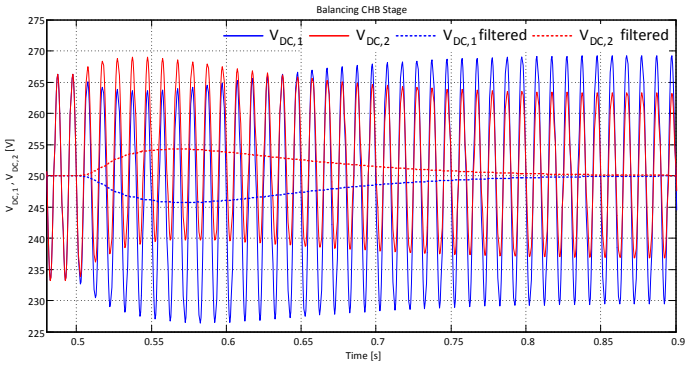

Fig. 10: DC-link voltage response to a step in the power distribution between P_1 and P_2 for CHB based voltage balancing.

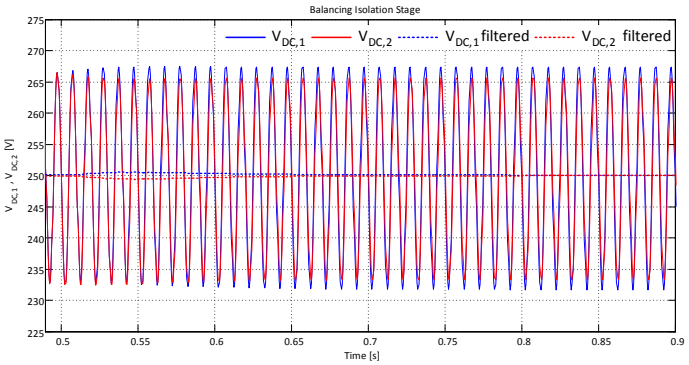

Fig. 11: DC-link voltage response to a step in the power distribution between P_1 and P_2 for DAB based voltage balancing.

Symbol	Description	Value
e (rms)	Grid voltage (rms)	$230\,V,\ 50\,Hz$
L_g	Filter inductance (MV side)	$3.8\,mH$
$V_{DC,1} = V_{DC,2}$	DC-link voltage reference	$250\,V$
V_0	DC-link voltage (LV side)	$250\,V$
$C_{cell,1} = C_{cell,2}$	MV capacitance	$930\,\mu F$
C_0	LV capacitance	$920\,\mu F$
R_0	Load resistance	$32\,\Omega$
$L_{k,1} = L_{k,2}$	Leakage inductance MFT	$63\,\mu F$
n	MFT turn ratio	$1:1$
$f_{sw,CHB}$	Switching frequency of the CHB	$3\,kHz$
$f_{sw,DAB}$	Switching frequency of the DAB	$12\,kHz$

TABLE I: Power Stage Parameters.

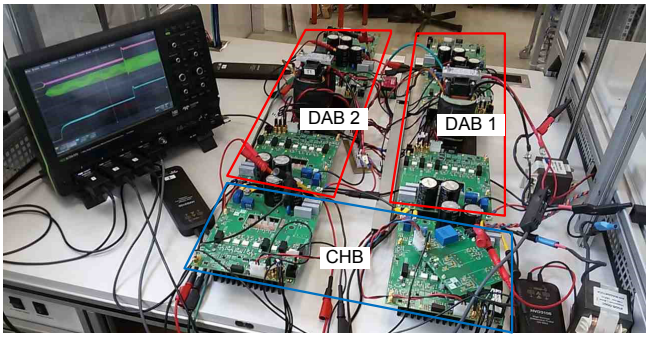

Fig. 12: Experimental setup for the validation consisting of a 5 level CHB and two DABs.

diagram, the response of the isolation stage based balancing controller is faster than the balancing controller in the MV-stage, resulting in a lower voltage ripple.

V. Experimental validation

For the validation of the different controller dynamics, a small scale ST prototype has been developed as shown in Fig. 12. It consists of a five level CHB active rectifier connected to the grid and DABs connected to each of the MV DC-links. The DABs are connected in parallel at the output side and feed a resistive load. All H-bridges in the CHB converter and the DABs have been assembled with the same IGBT Danfoss module DP25H1200T101616 and the system is controlled with a dSPACE SCALEXIO system based on three DS2655 FPGA base boards; each board has been programmed with a FPGA Xilinx blockset toolbox. The power stage parameters are summarized in Table I.

The CHB converter is connected to the electrical distribution grid (see table I) and in balanced condition the power delivered by the CHB active rectifier is $P_{DAB,1} = P_{DAB,2} = 1\,kW$. Consequently, the power is shared equally between the two DC-links. The dynamic behavior of the two voltage balancing approaches is evaluated by changing from equal power distribution to unequal power distribution. This has been conducted by keeping the overall reference power P_n constant and chancing the power references of the DABs to $P_{DAB,1} = 3 \cdot P_{DAB,2}$. For $P_n = 2\,kW$, the new reference power results in $P_{DAB,1} = 1.5\,kW$ and $P_{DAB,2} = 0.5\,kW$.

In Fig. 13 and Fig. 14 the two step responses are compared in terms of the DC-link voltage responses. As expected from the simulation results, the settling time of the balancing in the isolation stage is shorter and a lower peak voltage is validated. This indicates a fast rejection of the external disturbance and suggests to use the voltage balancing method in the isolation stage rather than in the medium voltage stage. Remarkably, the experimental results fit the simulation results shown in Fig. 10 and Fig. 11. This proves the validity of the average model.

Finally, Fig. 15 and 16 show the output currents of the two DABs before and after the change in the power distribution. Before the change in the reference, the output currents of both DABs obtain a similar mean value and their ripples are canceling out each other, which is resulting in a constant output current $i_{o,1}$. After the new command in the output reference, the output current of the DABs obtain the expected dynamic behavior and the mean values of the currents are $i_{o,1} = 6\,A$ and $i_{o,2} = 2\,A$. As a result of the unequal power transfer between the DABs, the currents obtain higher distortion.

VI. Conclusion

The voltage balancing for the CHB converter connected to DABs can be performed in the MV-converter or in the DC/DC converter. An average model and a small signal model are developed for the systems and it is demonstrated that the

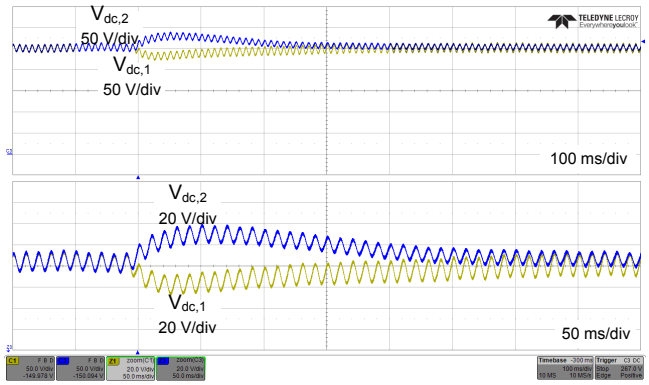

Fig. 13: DC-link voltage response to a step between $P_1 -> P_2$ for CHB based voltage balancing.

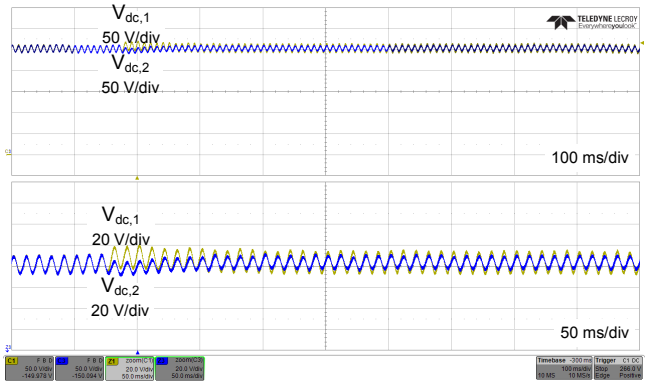

Fig. 14: DC-link voltage response to a step between $P_1 -> P_2$ for DAB based voltage balancing.

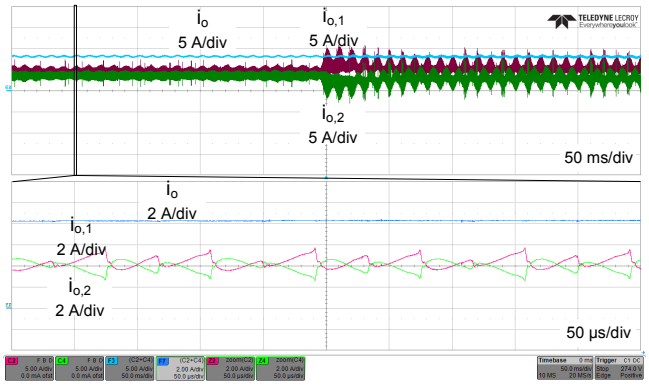

Fig. 15: Output currents $i_{o,1}$ (red), $i_{o,2}$ (green), i_o (light blue) before and after the power variation.

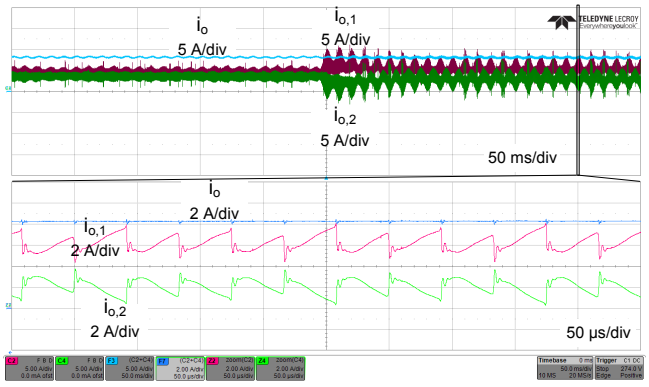

Fig. 16: Output currents $i_{o,1}$ (red), $i_{o,2}$ (green), i_o (light blue) before and after the power variation.

balancing in the DC/DC converter can achieve a significantly higher bandwidth than the commonly performed balancing in the MV-converter. For the particular case study, the voltage balancing control is performed in the MV-stage and the bandwidth is measured to be limited to $4\,Hz$. Differently the balancing controller in the isolation stage allows a bandwidth increase up to $160\,Hz$.The superior dynamic performances are verified by simulation and experimental results on a five level CHB converter.

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