Digital Object Identifier (DOI): 10.1109/TPEL.2017.2691012

IEEE Transactions on Power Electronics

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Suggested Citation

F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, "Thermal Analysis and Balancing for Modular Multilevel Converters in HVDC Applications," IEEE Transactions on Power Electronics, vol. 33, no. 3, pp. 1985–1996, March 2018.

Thermal Analysis and Balancing for Modular Multilevel Converters in HVDC Applications

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***Abstract*—The modular multilevel converter (MMC) has become a very attractive solution for interfacing high voltages in hybrid networks. The MMC enables scalability to different power levels, full controllability provided by IGBTs and can achieve very high efficiencies by using a low switching frequency method as the nearest level modulation. However, the nearest level modulation requires a capacitor voltage balancing algorithm, which can result in unbalanced loading for the power semiconductors in the different submodules. Particularly at low power factor operation, which could occur in case of low-voltage ride through and of reactive power injection, the conventional algorithm is not effective anymore. This article provides thermal stress analysis of the MMC in operation and proposes a thermal balancing approach, which is embedded in the capacitor voltage balancing algorithm. The purpose of the thermal balancing is to achieve similar stress distribution among the different submodules to enhance the lifetime. The junction temperatures in the different submodules are studied for HVDC applications and the article proves experimentally, that the thermal balance within the submodules is significantly improved.**

I. Introduction

The modular multilevel converter (MMC) was firstly proposed by Marquardt and Lesnicar in 2003 [1] and has become a very popular solution in HVDC transmission systems. Projects up to 1000 MW are realized or planned to be built [2]. The HVDC systems have to be designed and controlled to provide high efficiency, availability and reliability during steady state operation as well as during fault conditions being very challenging at DC side [3], [4], [5], [6]. In general, the MMC particularly profits from its scalability to different power and voltage levels by using standard components (IGBTs) [1], [7]. Since a very high number of IGBTs is required to block high voltages, even low switching frequency methods can achieve a suitable output waveforms [8], [9]. The minimization of the switching frequency and consequently a maximization of the efficiency is achieved with the nearest level modulation (NLM) [8], [10]. The NLM, which approximates the voltage reference to the closest available voltage level, can be easily adopted even for multilevel converters [8].

In addition to the efficiency, the reliability is a very important design criterion for high power converters, especially for maritime converter stations, where the access is limited. With respect to reliability, in power converters the power semiconductors have been found to be among the most sensitive components and are prone to fail because of applied thermal stress. Their expected lifetime is evaluated based on thermal cycle's magnitude and the related average junction temperatures [11]. For increasing the lifetime, active thermal control can regulate the junction temperature profile by adjusting the power losses [12], [13]. For application in the MMC, it was proposed to circulate reactive power for reducing the thermal fluctuations [14]. However, this thermal control approach is not addressed to the thermal imbalances among the different submodules (SMs) which can occur at low switching frequencies or due to parameter variations, as it has been done instead in [15] and [16], respectively.

As a problem resulting from the very low switching frequency with NLM, the turn on times are not similar for the different power semiconductors in the different SMs and can result in uneven thermal stress distribution [15]. This uneven stress affects the lifetime and can result in failures of power semiconductors.

In this article an MMC converter for HVDC applications with 150 SMs per arms is considered with NLM and the effect of unequal stress for the different power semiconductors in the SMs is demonstrated. It is shown, that the NLM can result in highly different lifetime expectations for the different power semiconductors in the SMs. To overcome this problem, a thermal balancing algorithm is introduced and validated experimentally by emulating the behavior of different SMs and by measuring the junction temperature with a high speed infrared camera.

The article is organized as follows. Section II introduces the MMC including the used mathematical model, control and capacitor voltage balancing. A thermal analysis with experimental validation is done in Section III showing the limitations in steady-state MMC operation. In Section IV the basic principle and the potential of active thermal balancing is presented and validated for different operation points. Finally, the conclusion is given in Section V.

II. MMC Description

A. Topology

The circuit of a three-phase MMC in double-star connection is shown in Fig. 1 [17]. In each arm, there are N series-connected SMs designed as chopper-cells. Both switching states and the paths of the arm current are illustrated in Fig. 2

This work was supported by the European Research Council under the European Union's Seventh Framework Programme (FP/2007- 2013) / ERC Grant Agreement 616344 HEART - the Highly Efficient And Reliable smart Transformer.

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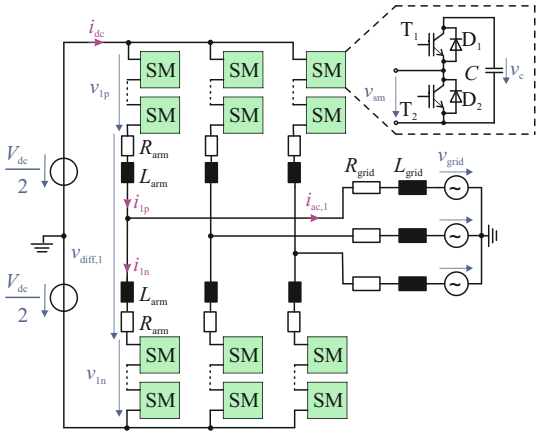


Fig. 1: Three-phase circuit of a modular multilevel converter (MMC) in double-star connection.

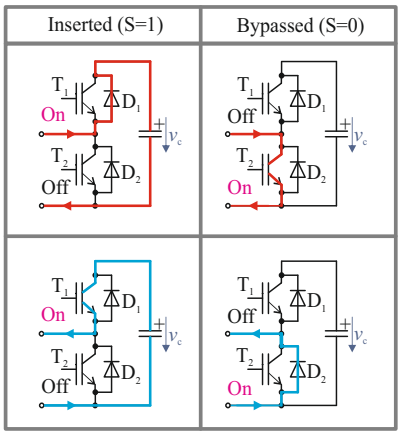


Fig. 2: Current paths in a submodule (SM) during normal MMC operation.

[18]. The three-phase grid is represented as 120° phase-shifted grid voltages v_{grid} and resistive-inductive grid impedances, divided in R_{grid} and L_{grid}.

B. Mathematical Model

The overall voltage across the SMs in the upper and the lower arm are given in (1) and (2). S(x) describes the switching state of the x^{th} SM. During normal MMC operation only two switching states are used.

$$v_{\text{p}} = \sum_{x=1}^{N} S_{\text{p}}(x) \cdot v_{\text{c,p}}(x) \tag{1}$$

$$v_{\text{n}} = \sum_{x=1}^{N} S_{\text{n}}(x) \cdot v_{\text{c,n}}(x) \tag{2}$$

Each phase voltage is described in (3). The AC current can be controlled by the difference between v_{n} and v_{p}. Half of the voltage difference can be defined as the converter voltage in (4) [19].

$$v_{\text{ac}} = R_{\text{grid}} \cdot i_{\text{ac}} + L_{\text{grid}} \cdot \frac{\text{d}i_{\text{ac}}}{\text{d}t} + v_{\text{grid}} \tag{3}$$

$$v_{\text{conv}} = \frac{v_{\text{n}} - v_{\text{p}}}{2} \tag{4}$$

The arm currents can be separated into two parts: the differential current i_{diff} and the contribution to the phase current i_{ac}. Considering an equal contribution, the arm currents can be described in (5) and (6). The differential current i_{diff} is contained both in the upper and in the lower arm current without being measurable directly [20].

$$i_{\text{p}} = i_{\text{diff}} + \frac{i_{\text{ac}}}{2} \tag{5}$$

$$i_{\text{n}} = i_{\text{diff}} - \frac{i_{\text{ac}}}{2} \tag{6}$$

The differential voltage v_{diff} is described in (7). The differential current is controlled by the sum of v_{p} and v_{n}.

$$v_{\text{diff}} = 2L_{\text{arm}} \cdot \frac{\text{d}i_{\text{diff}}}{\text{d}t} + 2R_{\text{arm}} \cdot i_{\text{diff}} \tag{7}$$

C. Control and Modulation

The power transmission and the average capacitor voltages are separately controlled by the AC current and the differential current, respectively [15]. The energy stored in the upper and the lower arm are equalized [21]. The current controllers are designed following the technical optimum principle [22]. The average capacitor voltage control is tuned to minimize the differential current ripple to relieve the semiconductors. The number of inserted SMs (n_{on}) is calculated in order to follow the reference voltages v^*_{conv} and v^*_{diff}. Assuming that the DC voltage and the capacitor voltages are ideally regulated, the equations (8) and (9) are obtained [23]. Since the number of SMs is an integer, the results have to be rounded.

$$n_{\text{on,p}} = \text{round}\left(\frac{N}{2} - \frac{v^*_{\text{conv}}}{V_{\text{co}}} - \frac{v^*_{\text{diff}}}{2V_{\text{co}}}\right) \tag{8}$$

$$n_{\text{on,n}} = \text{round}\left(\frac{N}{2} + \frac{v^*_{\text{conv}}}{V_{\text{co}}} - \frac{v^*_{\text{diff}}}{2V_{\text{co}}}\right) \tag{9}$$

D. Capacitor Voltage Balancing

The balancing of the capacitor voltages is one important challenge in the MMC as addressed in [1], [20], [24]–[31]. The goal is to achieve an equal power distribution among the SMs. In general, it is possible to separate voltage balancing methods in distributed and centralized methods [26].

Distributed methods are controlling the voltage of each capacitor in a closed-loop and are usually adopted with carrier phase-shifted pulse-width modulation [20], [24], [25]. The balancing control causes a modification in the modulating signals and requires a sufficiently high switching frequency [26]. However, the hardware and software costs for controllers would become excessive in an HVDC application due to the huge number of SMs.

Centralized methods are directly combined with the modulator and can be applied to NLM in HVDC applications [32]. The modulator provides the number of inserted SMs which are selected depending on the capacitor voltages and the arm current direction [1], [27], [28]. However, additional switching actions can be required [29]. One big challenge is

the sufficiently fast sorting of the capacitor voltages for a high number of SMs [30], [31].

III. Thermal Analysis of MMC

A. Thermal Principles and Lifetime Expectation

The junction temperature of power semiconductors is of major importance because it is influencing the efficiency of the converter and the lifetime of the system. For IGBTs an increase in the junction temperature T_j affects a reduction in the efficiency, while the design for a low maximum junction temperature counteracts the goal of a compact and cost effective systems. The influence of the chip temperature on the lifetime is given with several failure mechanisms, which are dependent on the junction temperature [33]. The number of power cycles to failure N_f can be approximated by (10) whereas the constants a_1, a_2 and a_3 have to be fitted by cycling tests [34].

$$N_\mathrm{f} = a_1 \cdot (\Delta T_\mathrm{j})^{-a_2} \cdot \exp^{\frac{a_3}{T_\mathrm{j}}} \tag{10}$$

This mathematical lifetime model only considers a single magnitude of thermal cycles ΔT_j, which is not sufficient to estimate the lifetime based on a real mission profile. In this case, the Miner rule is commonly applied with linear damage accumulation as shown in (11).

$$C_\mathrm{m} = \sum_{i=0}^{\infty} \frac{n_\mathrm{i}}{N_\mathrm{i}} \leq 1 \tag{11}$$

In this equation, N_i is the number of cycles to failure in the stress range i and n_i the number of detected cycles in the i^{th} stress range. As soon as the accumulated damage $C_\mathrm{m} = 1$, the device is expected to fail. Based on this equation, the lifetime is obtained as the inverse of the damage divided by the time period in which this damage was affected. The approach is developed for IGBTs and diodes, as well. However, the interpretation of the diodes' lifetimes should be done carefully since the theoretical model is primary applied to IGBTs.

Despite the high importance of the junction temperature, there is still no suitable low cost method for accessing the junction temperature of the power semiconductors: Direct measurement is only practical in laboratory environments, Thermo Sensitive Electrical Parameters (TSEP) affect additional components and sensor costs and observers or estimators deal with parameter uncertainties and high complexity for high precision [35]. Particularly, in modular power converters, there is the additional challenge of a high number of power semiconductors, resulting in many junction temperatures to be taken into account. A cheaper solution can be realized by model based approaches only requiring low bandwidth case temperature measurement and the thermal characteristics provided in the datasheet [36]. The computation effort can be reduced by transforming the fourth order Foster model to second order [36]. A disadvantage of the model based approaches are model uncertainties and often the neglected thermal coupling between different power semiconductors.

TABLE I: MMC simulation parameters.

Description	Parameter	Value	Unit
SMs per arm	N	150	
DC voltage	V_dc	300	kV
Arm inductance	L_arm	72	mH
Arm resistance	R_arm	200	mΩ
SM's capacity	C	10	mF
Capacitor voltage limit	$V_\mathrm{c,lim}$	2500	V
Grid voltage	$V_\mathrm{grid,ll}$	120	kV
Grid inductance	L_grid	25	mH
Grid resistance	R_grid	1	Ω
Cooling resistance (IGBT)	$R_\mathrm{th,CH,T}$	5.2	$\frac{\mathrm{K}}{\mathrm{kW}}$
Cooling resistance (Diode)	$R_\mathrm{th,CH,D}$	11.7	$\frac{\mathrm{K}}{\mathrm{kW}}$
Sampling time	T_s	20	μs

B. Analysis of MMC Operation

The used simulation model is based on the mathematical model derived in Section II and discretized in MATLAB by using a sampling time of $20\,\mu$s. In Table I the simulation parameters for an HVDC application are summarized, whereby the DC voltage is assumed to be constant. The MMC consists of 150 SMs per arm and is rated for a nominal power of 300 MW. A high-voltage grid and the corresponding grid transformer are emulated.

The control was described in Section II and in [15] and NLM is applied to achieve high efficiency. (1.3) A centralized method is applied for capacitor voltage balancing due to the huge number of SMs. Not only the modulation but also the balancing algorithm is selected to provide a very low switching frequency. This is achieved by only inserting SMs which are currently switched off and vice versa [29]. Additional switching operations can be required because the capacitor voltages are limited to 2500 V for protection.

As semiconductors the IGBT module *CM1200HC-90R* from Mitsubishi is considered, the power losses are calculated by the datasheet characteristics according to [37]. The thermal model is based on the Foster Network as illustrated in Fig. 3, and the thermal impedances of the semiconductors from junction to case are obtained from the datasheet. Furthermore, the thermal resistances between case and heatsink $R_\mathrm{th,CH}$ are given in Table I. Since the time constants of the cooling elements would be relatively high, a constant temperature difference between cooling and case is assumed for steady state operation. The semiconductors are cooled by a water temperature of $T_\mathrm{a} = 40\,^\circ$C.

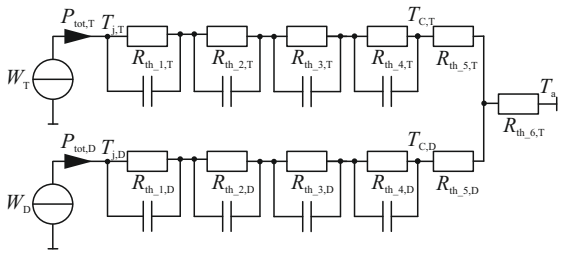
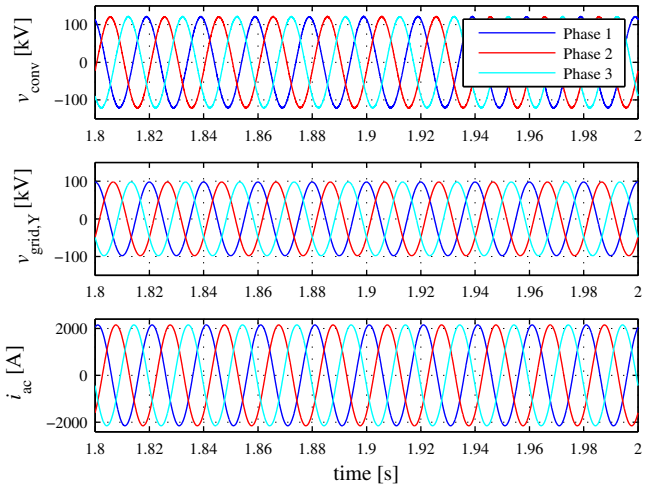
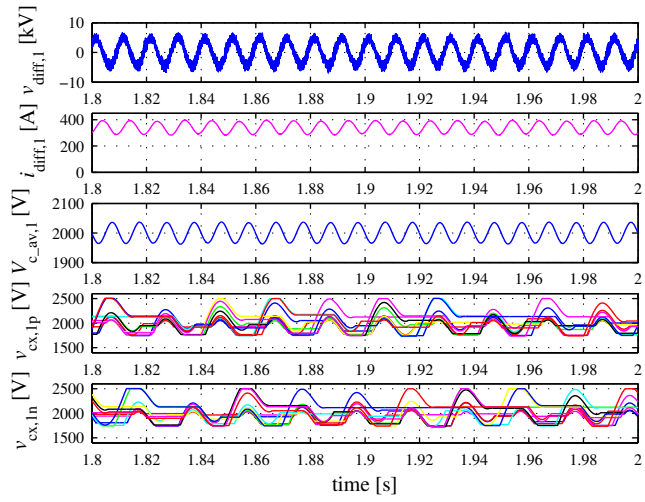


Fig. 3: Foster model for IGBT module and cooling system.

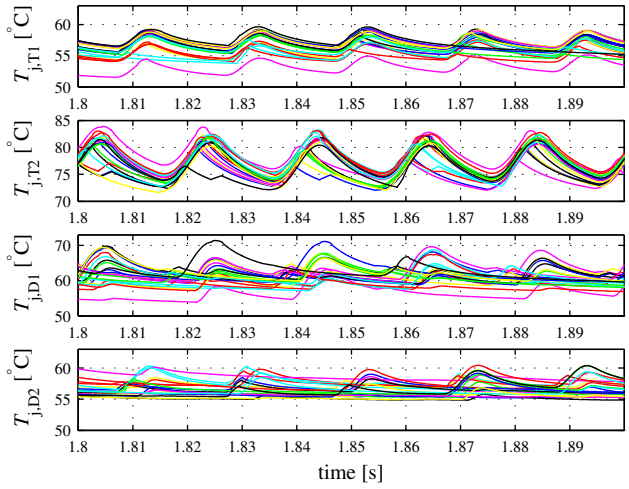


(a)

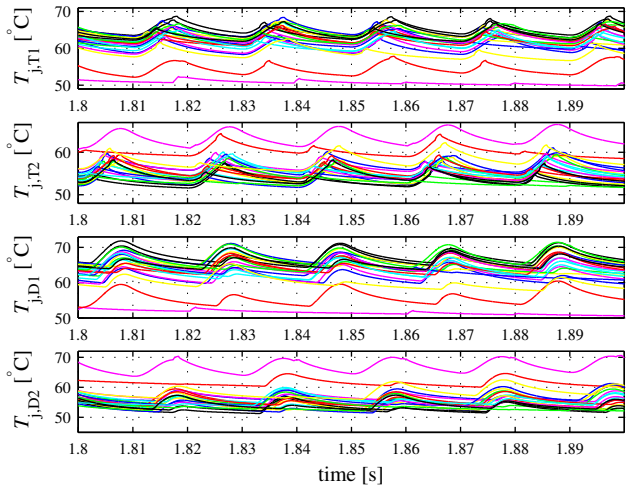


(b)

Fig. 4: Electrical behavior of the MMC in OP1 (steady state: $P_{\text{grid}} = 300\,\text{MW}$, $\cos\varphi = 0.95$): a) Converter phase voltages, grid voltages and phase currents (3 phases), b) Differential voltage, differential current and capacitor voltages of the first 21 SMs (phase 1). [15]



(a)



(b)

Fig. 5: Thermal behavior of the semiconductors in the first 21 SMs in the upper arm (phase 1): a) OP1 (steady state: $P_{\text{grid}} = 300\,\text{MW}$, $\cos\varphi = 0.95$), b) OP2 (steady state: $Q_{\text{grid}} = 300\,\text{Mvar}$, $\cos\varphi = 0$). [15]

The MMC is considered in steady state operation and the rated power is transmitted from DC to AC side. The three-phase converter voltages, the grid voltages and phase currents are depicted in Fig. 4a for a power transmission of 300 MW, defined as operation point 1 (OP1). A power factor of $\cos\varphi = 0.95$ corresponds to a reactive power of 98.6 Mvar. The phase currents reach an amplitude of around 2150 A. The differential voltage and the differential current (phase 1) are depicted in Fig. 4b. The peak-to-peak ripple of the differential current is around 120 A, by obtaining an average capacitor voltage oscillating of about 70 V. The individual capacitor voltages are balanced and limited to 2500 V.

The thermal behavior of the semiconductors is considered in the upper arm (phase 1) and is depicted for the first 21 SMs in Fig. 5a. The highest junction temperatures occur in IGBT T_2 and is caused by the considered power flow direction. T_2 is active when the corresponding SM is inserted and when the arm current is positive. The cyclic behavior of power losses also causes thermal cycles with the fundamental frequency of the grid (50 Hz). As it can be seen, the temperatures are already regulated by the capacitor voltage balancing up to a certain degree. However, the loading of the SMs can be quite different. Especially at low power factors, the spread in the temperatures becomes very significant. This is illustrated in Fig. 5b where the temperatures are depicted for a maximum reactive power (OP2: $Q_{\text{grid}} = 300\,\text{Mvar}$, $\cos\varphi = 0$). The individual capacitors are not charged as fast as before since the arm currents are oscillating around zero. Therefore, the semiconductors can conduct the current for a longer time without being changed by the capacitor voltage balancing. An active thermal balancing can solve this problem and will be demonstrated in Section IV.

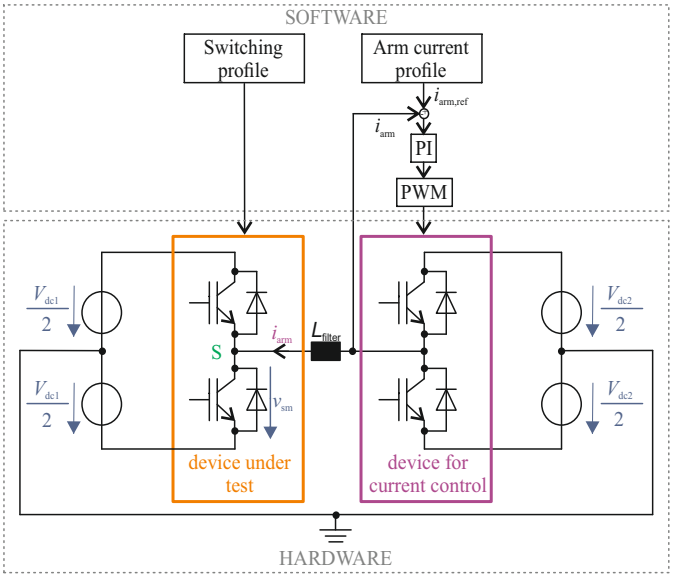


Fig. 6: Experimental bench for electrical and thermal evaluation of one MMC SM.

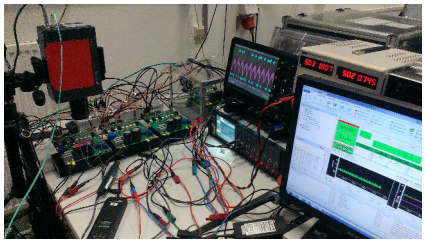


Fig. 7: Setup of the experimental bench.

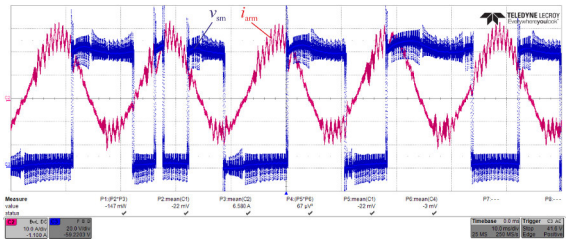


Fig. 8: Experimental validation of arm current and voltage at one SM (no. 61).

C. Experimental Validation

For the validation of the theoretical results, an experimental bench has been developed and puts the focus on one single SM. Both the electrical behavior of each SM and the thermal behavior of its semiconductors can be validated on this bench. The emulation of each SM with and without the proposed method can show qualitatively the impact on the semiconductor's junction temperature.

The experimental bench for the emulation of one SM is depicted in Fig. 6. The prototype consists of one half-bridge as device-under test and an additional half-bridge to emulate the reference arm current. The submodule's capacitor voltage V_{dc1} is generated by a DC source. Voltage oscillations can be neglected for thermal evaluation since they are only small, just relevant for the switching losses and would be mostly filtered due to higher thermal time constants. The device-under test is fed by a DSPACE system with the switching pattern of one SM from the simulation. The reference arm current is controlled by a PI controller whereas $V_{dc2} > V_{dc1}$ has to be fulfilled. In this way, both simulated operation points are investigated experimentally. The system parameters are summarized in Table II.

One half-bridge of the open 1200 V IGBT module *DP25F1200T101666* from Danfoss was selected as device under test. The SM capacitor voltage is downscaled to 100 V for protection since the absence of the filling gel makes high-voltage operation riskier. The reference arm current is limited by a downscaling factor of 50. The changed power rating of the semiconductors is not a critical issue since the conduction losses are dominant at low switching frequencies. The conduction losses are directly related to the switching sequence and the arm current. Thus, the relative temperatures between the full system in simulation and the temperatures in the downscaled system are highly correlated. The reduction of thermal spread by thermal balancing will be verified by means of the changing switching sequences. The temperatures of the module are measured and recorded by the infrared camera *ImageIR 8300*.

TABLE II: System parameters.

V_{dc1}	100 V
V_{dc2}	200 V
L_{filter}	3.6 mH
f_{sw}	10 kHz

Fig. 7 shows a photo of the setup. The electrical waveforms for one SM (no. 61) are depicted in Fig. 8 for OP1 ($P_{grid} = 300\,\text{MW}$, $\cos\varphi = 0.95$). The SM voltage is obtained according to its switching profile. The reference arm current is properly controlled, independent from the SM's switching state. The temperature distribution in the IGBT module is illustrated in Fig. 9. The junction temperatures of IGBTs T_1, T_2 and diodes D_1, D_2 are recorded and shown with the simulated temperature behavior in Fig. 10. Just the temperature ranges are downscaled by the experimental results due to the reduced power level and the usage of different power semiconductors. Beyond that, both thermal profiles match together proving the validity of the experimental results.

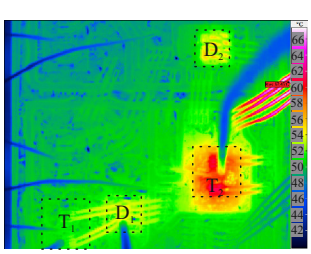


Fig. 9: Temperature distribution in the IGBT module recorded by infrared camera for one SM (no. 61).

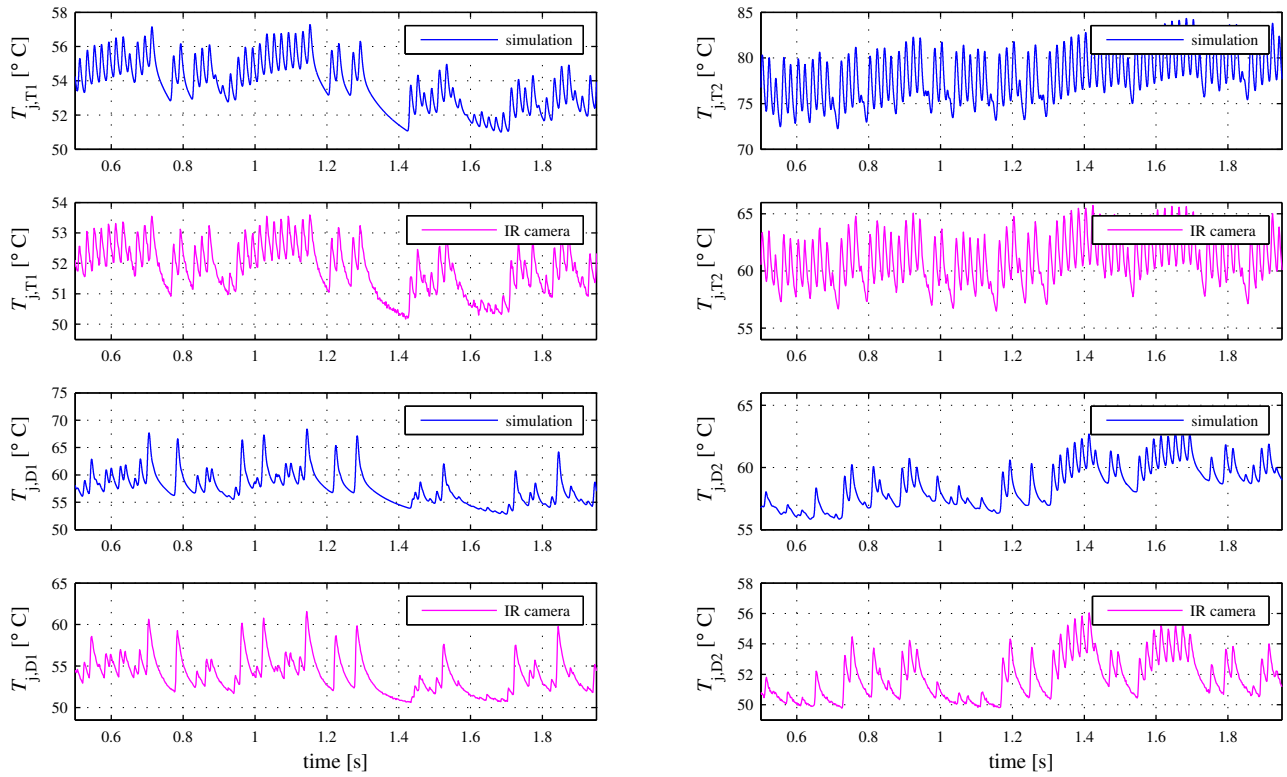


Fig. 10: Junction temperature profile for one SM (no. 61) from simulation and from test bench from infrared camera for OP1 (steady state: $P_{\text{grid}} = 300\,\text{MW}$, $\cos\varphi = 0.95$).

IV. Active Thermal Balancing

A. Active Thermal Balancing Approach

Active thermal balancing algorithms are presented in [15] and [16] with the purpose of an equalized heat and stress distribution among all SMs. Unbalanced stress distribution, affecting the semiconductors' lifetimes, can occur at very low switching frequencies in HVDC applications [15] or due to parameter variations as demonstrated for fast switching medium-voltage applications [16]. Active thermal balancing relieves the conducting semiconductor by changing the corresponding SM's switching state as soon as the temperature becomes relatively high. The algorithm can be applied to all semiconductors [15] or to the most stressed semiconductor [16] and can be always activated [15] or in predefined scenarios [16]. The thermal balancing methods are software based and integrated in the capacitor voltage balancing algorithm, limiting the costs.

Usually, the capacitor voltage balancing algorithm takes decision of switching on or off SMs only based on the capacitor voltages and on the arm current direction. However, in this manner the temperatures of the semiconductors can be different. An active thermal balancing takes the junction temperatures into account with the purpose to select the SMs by minimizing the temperatures of the semiconductors carrying the current after one switching operation. A possible principle for a thermal balancing is summarized in Table III, whereas n_{on}^{k} and $n_{\text{on}}^{\text{k}-1}$ describe the actual and the previous number of SMs which have to be inserted according to the modulator.

TABLE III: Active thermal balancing principle.

$n_{\text{on}}^{\text{k}} - n_{\text{on}}^{\text{k}-1}$	i_{arm}	Action
positive	> 0	insert SM(s) with lowest temperature in D_1
positive	< 0	insert SM(s) with lowest temperature in T_2
negative	> 0	bypass SM(s) with lowest temperature in T_1
negative	< 0	bypass SM(s) with lowest temperature in D_2

In (12)-(15) cost functions are defined to include both: the SM capacitor voltage and the junction temperature of the most stressed power semiconductor. The weighting factor α is used to adjust the strength of active thermal balancing whereas it is disabled for $\alpha = 0$. A simplified flowchart of active thermal balancing embedded in a capacitor voltage balancing is depicted in Fig. 11. The cost function is selected for each sampling time by taking into account the arm current direction and whether SMs have to be switched on or off. The SMs to be inserted or bypassed are selected by minimizing the applied cost function so that the current will be redirected to the less stressed anti-parallel semiconductor. In addition to the thermal balancing, a maximum temperature should be defined as thermal protection.

$$c_1 = (v_{\text{c}} - v_{\text{c,min}}) + \alpha_1 (T_{\text{j,D1}} - T_{\text{j,D1,min}}) \tag{12}$$

$$c_2 = (v_{\text{c,max}} - v_{\text{c}}) + \alpha_2 (T_{\text{j,T2}} - T_{\text{j,T2,min}}) \tag{13}$$

$$c_3 = (v_{\text{c,max}} - v_{\text{c}}) + \alpha_3 (T_{\text{j,T1}} - T_{\text{j,T1,min}}) \tag{14}$$

$$c_4 = (v_{\text{c}} - v_{\text{c,min}}) + \alpha_4 (T_{\text{j,D2}} - T_{\text{j,D2,min}}) \tag{15}$$

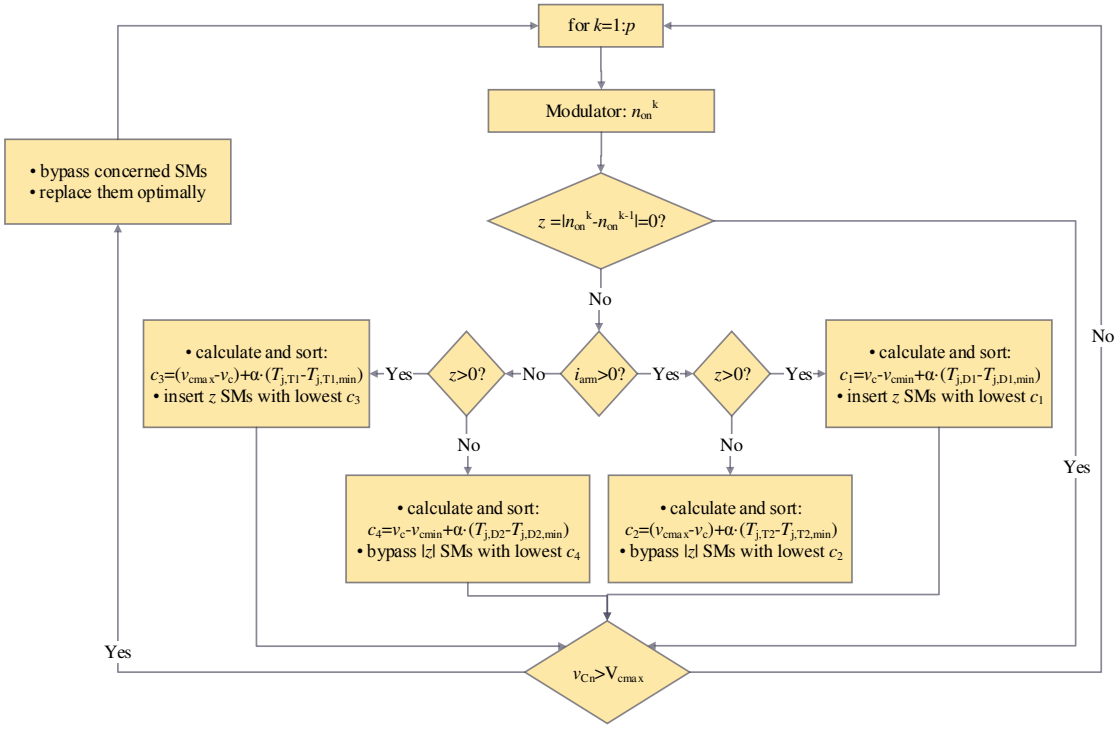


Fig. 11: Simplified flowchart of active thermal balancing embedded in capacitor voltage balancing related to one arm (p: number of iterations, z: auxiliary variable).

The junction temperatures can be directly obtained by one of the methods discussed in Section III-A. The junction temperatures are provided for the thermal balancing algorithm by a feedback loop to balance the temperatures.

The active thermal balancing is activated to reduce the spread in the temperatures for both operation points from Section III. The weighting factor α is selected to achieve a similar weighting between capacitor voltage and thermal balancing. The capacitor voltage oscillations are expected within a range of around 750 V referring to Fig. 4b (OP1). The factor α is set constant to 50 for the different cost functions: $\alpha = \alpha_1 = \alpha_2 = \alpha_3 = \alpha_4$. This corresponds to a realistic temperature range of 15 K.

The maximum, the minimum and the average temperatures for IGBTs T_1 and T_2 and for the capacitor voltages of the 150 SMs are depicted in Fig. 12 for OP1 ($P_{grid} = 300$ MW, $\cos\varphi = 0.95$). The average temperature is approximately constant independent from the weighting factor due to almost constant semiconductor losses according to Table IV. The spread of the capacitor voltages is not significantly changed and the switching frequency is kept almost constant. However, the spread in the temperatures is reduced by the active thermal balancing ($\alpha = 50$) in comparison to the usual capacitor voltage balancing ($\alpha = 0$). The averaged difference between highest and lowest junction temperature are summarized in Fig. 14a for both weighting factors. A reduction between 19.5 % (T_2) and 35.1 % (D_1) is achieved by the active thermal balancing without deteriorating the performance of the operation.

This effect becomes even stronger in OP2 ($Q_{grid} = 300$ Mvar, $\cos\varphi = 0$) as shown in Fig. 14b. The thermal spread in the temperatures is clearly reduced by the active thermal balancing as shown in Fig. 13 with almost constant semiconductor power losses. The spread of the capacitor voltages is slightly increased due to changed commutation times without negatively affecting the switching frequency. The averaged difference between highest and lowest junction temperature is decreased by between 12.4 K (T_2) and 21.6 K (D_1). This corresponds to a reduction between 71.4 and 79.7 %. The reduction of the thermal spread and of the maximum temperatures can be exploited for a more economic rating, especially for the diodes and the related cooling system.

TABLE IV: Comparison of power losses in semiconductors, efficiency and switching frequency with and without thermal balancing for OP1 and OP2.

OP1	power losses (upper arm)	switching frequency
$\alpha = 0$	395.3 kW	53 Hz
$\alpha = 50$	392.4 kW	49 Hz
OP2	power losses (upper arm)	switching frequency
$\alpha = 0$	297.5 kW	51 Hz
$\alpha = 50$	297.9 kW	49 Hz

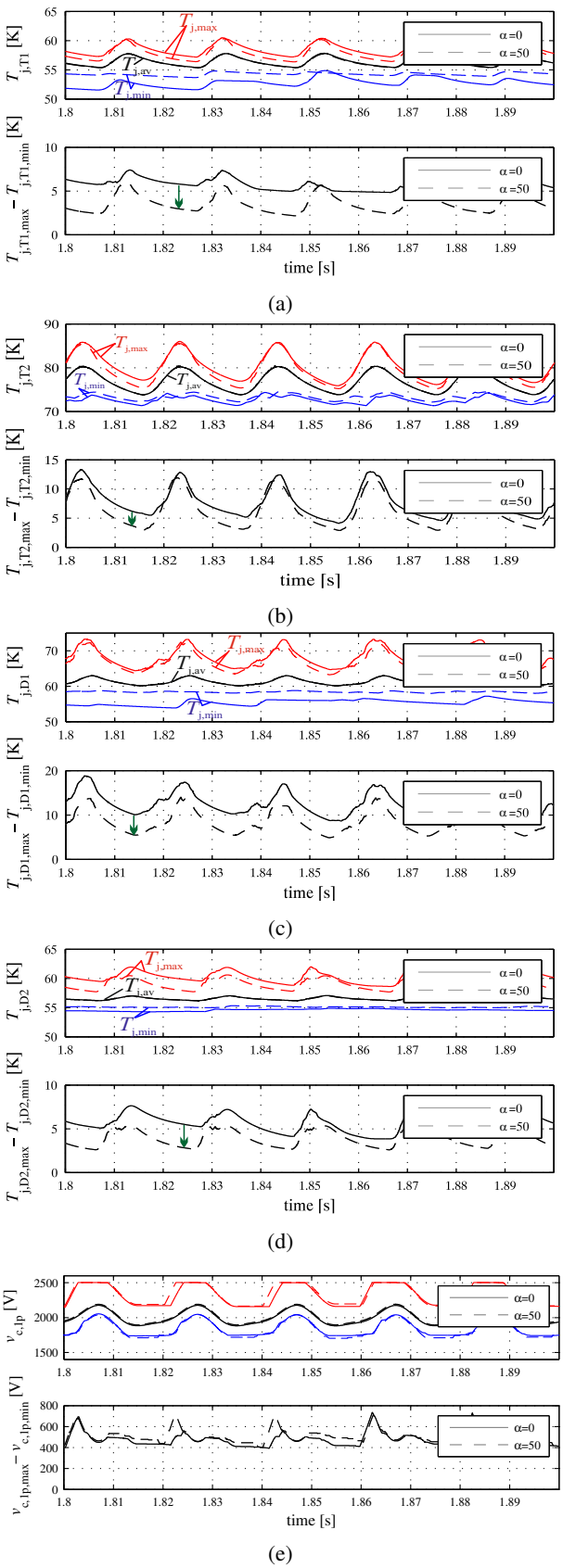


Fig. 12: Maximum, minimum, averaged junction temperatures and capacitor voltages in the upper arm (ph. 1) in OP1 (steady state: $P_{\text{grid}} = 300\,\text{MW}$, $\cos\varphi = 0.95$): a) IGBTs T_1, b) IGBTs T_2, c) Diodes D_1, d) Diodes D_2, e) Capacitor voltages.

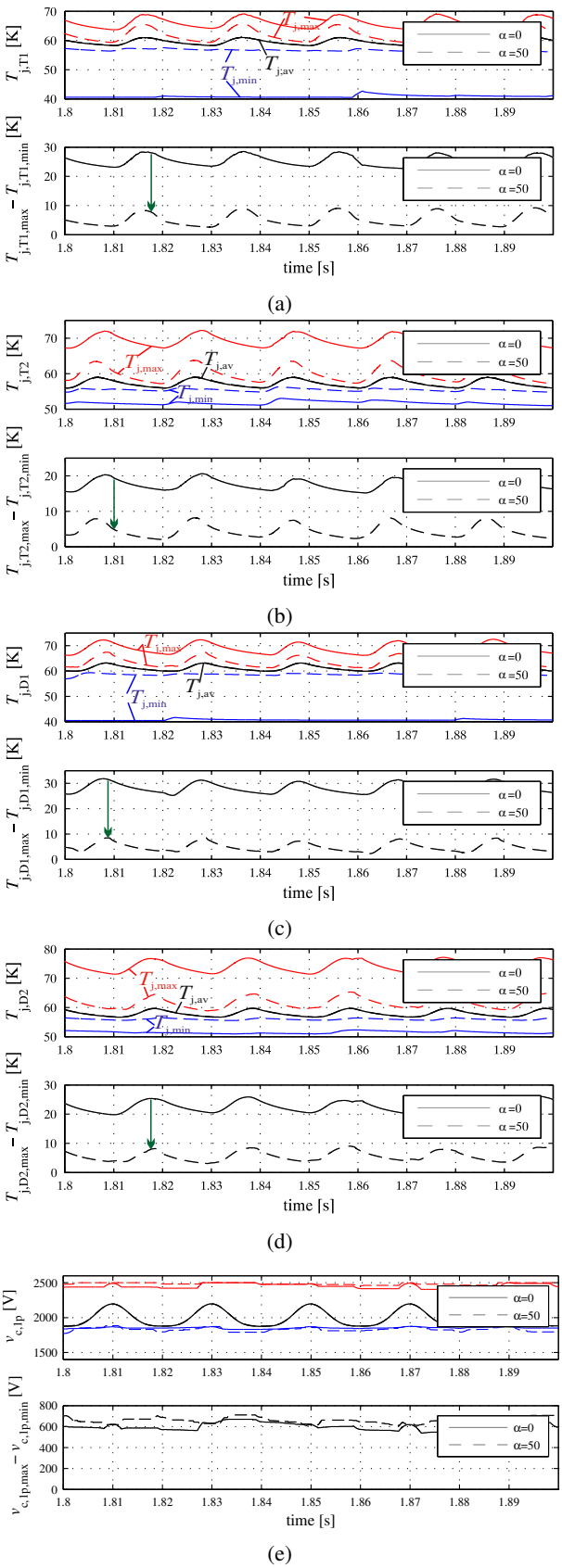


Fig. 13: Maximum, minimum, averaged junction temperatures and capacitor voltages in the upper arm (ph. 1) in OP2 (steady state: $Q_{\text{grid}} = 300\,\text{Mvar}$, $\cos\varphi = 0$): a) IGBTs T_1, b) IGBTs T_2, c) Diodes D_1, d) Diodes D_2, e) Capacitor voltages.

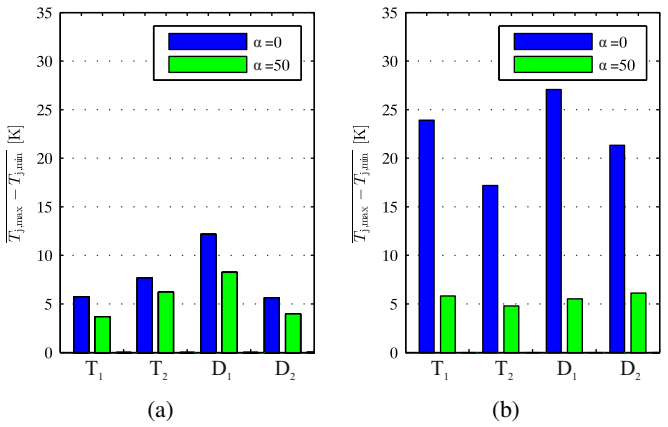


Fig. 14: Maximum temperature difference (averaged) among all 150 SMs in the upper arm (phase 1): a) OP1 (steady state: $P_{\text{grid}} = 300\,\text{MW}$, $\cos\varphi = 0.95$), b) OP2 (steady state: $Q_{\text{grid}} = 300\,\text{Mvar}$, $\cos\varphi = 0$).

The impact of active thermal balancing is particularly strong in OP2. The corresponding lifetime expectations under this profile are calculated based on (10), (11) and illustrated in Fig. 15 for all semiconductors whereas unrealistic long lifetimes have been set to 100 years. Without active thermal balancing, failures can occur very early in many SMs. Compared to this, the thermal stress is much better balanced by active thermal balancing. The lifetime of each semiconductor has been increased by minimum 50 % for at least the 20 SMs with the lowest expected lifetime. Additionally, the mean lifetime has been increased for all power semiconductors. The enhanced reliability can be exploited for longer maintenance intervals or for the usage of less SMs in the system.

B. Experimental Validation of Active Thermal Balancing of MMC

Three different SMs are selected from simulation for each operation point to further demonstrate the effect of active thermal balancing. The corresponding switching profiles and junction temperatures are depicted in Fig. 16 for OP1. The SM no. 122 can be seen as a kind of reference for a balanced loading. In comparison, the switching profile and the temperatures of SMs no. 61 and 94 are not always homogenous without active thermal balancing. As a consequence, the temperature spread among the three SMs is relatively high. By means of active thermal balancing, the inhomogeneity and the temperature spread among the SMs has been strongly reduced. Remarkably, not only the spread among the SMs is reduced but also the number of fast and high temperature changes in single power semiconductors.

These thermal cycles can be particularly evident at low power factors as illustrated in Fig. 17 for OP2. The switching profile of one SM can be quite inhomogeneous without thermal balancing as seen in SM no. 146. The SM is switched off for a long time whereas only the semiconductors T_2 and D_2 are loaded. During this time the submodule's capacitor voltage does not change so that the sole capacitor voltage balancing is not effective anymore to achieve a thermal balance.

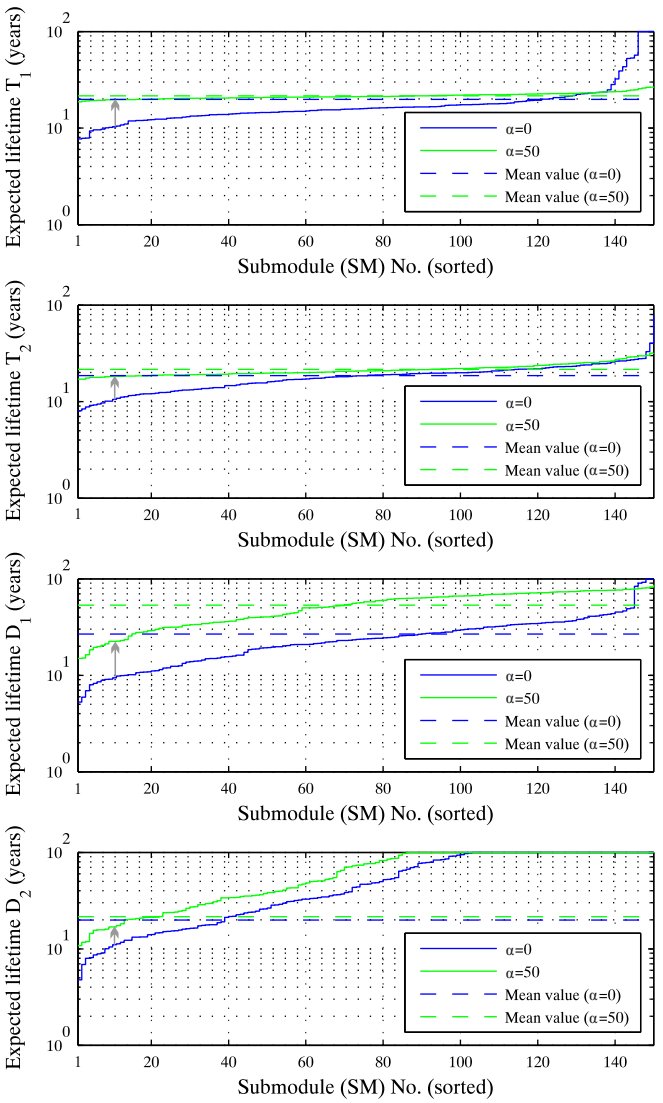


Fig. 15: Lifetime expectation for the power semiconductors of all submodules in the upper arm (phase 1) in OP2.

The active thermal balancing reduces the spread and the cycles in the temperatures by providing a more homogenous switching profile. The remaining thermal cycles are linked to the extremely low switching frequency since not each SM will be automatically changed in each period. Nevertheless, the thermal stress is strongly reduced by active thermal balancing by maintaining the very high efficiency. Thus, an active thermal balancing has the potential to significantly enhance the semiconductors' lifetime of the system by preventing imbalanced loading of the SMs.

For medium-voltage applications the thermal spread is highly damped by the capacitor voltage balancing due to lower number of SMs and due to increased switching frequencies as it has been demonstrated in [28]. This is the reason why the presented thermal balancing algorithm is mainly relevant for HVDC applications. The experimental validation can be provided by the emulation of the thermal behavior of single SMs with the switching pattern from the HVDC-MMC as demonstrated in this article.

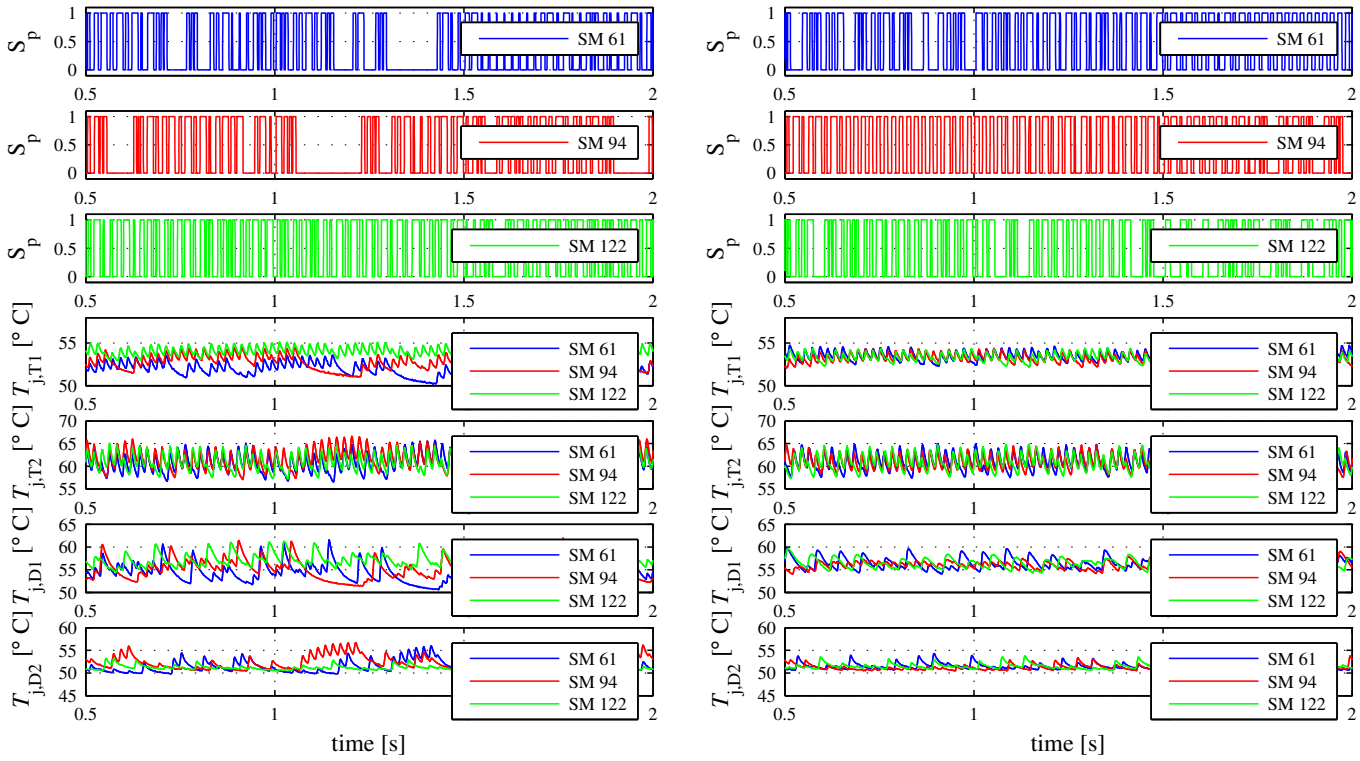


Fig. 16: Switching states and junction temperatures in three MMC SMs (no. 61, 94, 122) recorded by infrared camera in OP1: a) Disabled active thermal balancing ($\alpha = 0$), b) Enabled active thermal balancing ($\alpha = 50$).

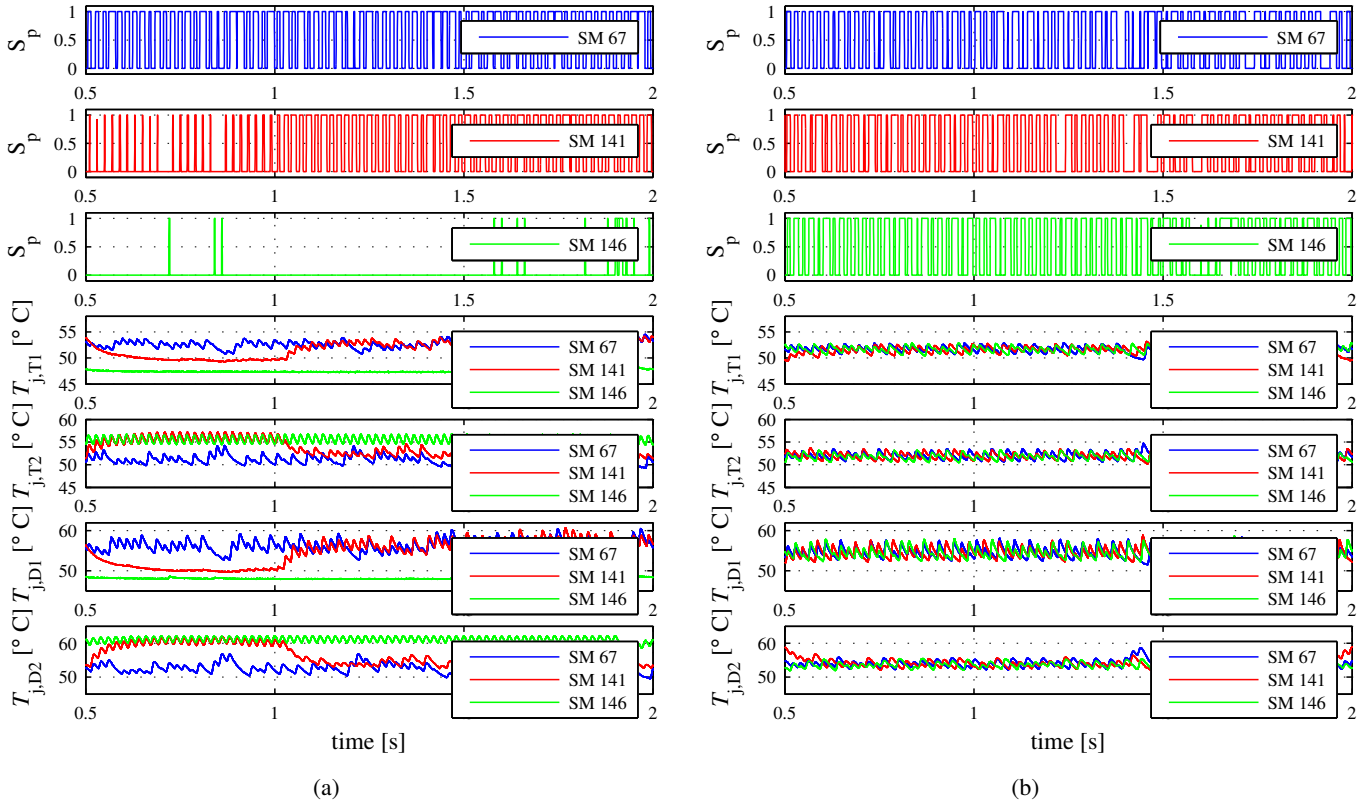


Fig. 17: Switching states and junction temperatures in three MMC SMs (no. 67, 141, 146) recorded by infrared camera in OP2: a) Disabled active thermal balancing ($\alpha = 0$), b) Enabled active thermal balancing ($\alpha = 50$).

V. Conclusion

The thermal stress distribution of the power semiconductors in an MMC for HVDC application has been investigated. It has been demonstrated, that the NLM algorithm does not effectively balance the stress among the devices, which is getting even more relevant at low power factors. For balancing the stress among the power semiconductors in the SMs, an active thermal balancing algorithm has been proposed to better distribute the loading of the SMs, which takes into account the capacitor voltage and the junction temperature of the most stressed power semiconductor in each SM.

The thermal balancing algorithm is demonstrated to reduce the difference in the junction temperature spread among the SMs in all operating conditions without deteriorating the performance of the system. The decreased thermal spread among the SMs leads to lower maximum temperatures of the power semiconductors and can be exploited for the optimization of the system. Either the rating of the power semiconductors and the related cooling system can be reduced or the lifetime of the power semiconductors can be enhanced due to the reduction in thermal stress. For pure reactive power supply the lifetime has been increased by minimum 50 % for the first failing power semiconductors. The effectiveness of the algorithm is validated experimentally by emulating the thermal behavior of different SMs.

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