

© 2016 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

Digital Object Identifier (DOI): 10.1109/EPE.2016.7695611

European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)
Active Thermal Balancing for Modular Multilevel Converters in HVDC Applications

Frederik Hahn
Giampaolo Buticchi
Marco Liserre

Suggested Citation

F. Hahn, G. Buticchi, and M. Liserre, "Active thermal balancing for modular multilevel converters in HVDC applications," in 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Sept 2016, pp. 1–10.

Active Thermal Balancing for Modular Multilevel Converters in HVDC Applications

Frederik Hahn, Giampaolo Buticchi, Marco Liserre
Chair of Power Electronics
University of Kiel
Kaiserstraße 2
Kiel, Germany
Phone: +49 (0) 431/880-6105
Email: {frha,gibu,ml}@tf.uni-kiel.de
URL: <http://www.pe.tf.uni-kiel.de/en>

Keywords

<<Multilevel converters>>, <<HVDC>>, <<Thermal cycling>>, <<Thermal stress>>, <<High voltage power converters>>

Abstract

The modular multilevel converter (MMC) has become a very attractive solution for interfacing high voltages hybrid networks. The MMC enables scalability to different power levels, full controllability provided by IGBTs and can achieve very high efficiencies by using a low switching frequency method as the nearest level modulation (NLM). However, in order to limit failures of the power modules, the thermal stress of the submodules (SMs) should be properly studied. For NLM a capacitor voltage balancing algorithm is required and this algorithm, as demonstrated in this paper, offers already good thermal balance among the cells of the MMC. However, at low power factor, operation which could occur in case of low-voltage ride through and of reactive power injection, the mentioned algorithm is not effective anymore. This paper proposes an active thermal balancing algorithm which is embedded in the previously mentioned capacitor voltage balancing algorithm. The purpose of the active balancing is to achieve an equal heat distribution among the submodules to enhance the lifetime. The junction temperatures with and without active thermal balancing are studied in simulation for an HVDC application. The paper proves that thermal balance of MMC can be significantly improved.

Introduction

The modular multilevel converter (MMC) was firstly proposed by Marquardt and Lesnicar in 2003 [1] and has become a very popular solution in HVDC transmission systems. Projects up to 1000 MW are realized or planned [2]. The MMC especially profits from its scalability to different power and voltage levels by using standard components (IGBTs) [1]. Since a very high number of IGBTs is required to block high voltages even low switching frequency methods can achieve a suitable waveform [3]. A minimum possible switching frequency is achieved by a nearest level modulation (NLM) [3]. The NLM can be easily adopted even for multi-level converters and approximates the voltage reference to the closest available voltage level [3]. Also due to the high efficiency achieved by low switching frequencies the MMC is very interesting for high- and medium-voltage power conversion.

In addition to the efficiency, the reliability is a very important design criterion for high power converters especially for maritime converter stations. The expected lifetime of one power module strongly depends on the thermal stress. The thermal stress can be evaluated by the absolute junction temperatures and their thermal cycles [4]. In order to increase lifetimes, an active thermal control can regulate the temperature

profile by adjusting the power losses [5]. Different approaches are summarized in [5],[6]. Compared to a simple two-level converter the degrees of freedom in a high-voltage MMC converter are strongly increased. This creates additional opportunities and challenges for an improved thermal management. An indirect thermal control for MMCs by utilizing the differential (circulating) current was recently proposed in [7]. Apart from that, publications regarding the thermal management in MMCs are very scarce.

In this paper an active thermal balancing is presented to achieve an equal heat distribution among the different submodules (SMs). By this strategy the conducting semiconductor is relieved when the temperature becomes relatively high. The thermal balancing is integrated in the capacitor voltage balancing algorithm and is applied to NLM.

The paper is organized as follows. The first section introduces the MMC including the used mathematical model, control and capacitor voltage balancing. The next section introduces and describes the principle of the active thermal balancing in detail. In the third section simulation results with and without active thermal balancing are analyzed for different operation points. The conclusion is given in the final section.

MMC Description

Topology

The circuit of a three-phase MMC in double-star connection is shown in Fig. 1 [8]. Each three-phase leg is divided in an upper arm (p) and a lower arm (n). In each arm there are N series-connected SMs. The SMs are designed as chopper-cells. Each SM can be seen as discrete voltage source able to switch between the capacitor voltage v_c and zero at its terminals. An inductor L_{arm} is inserted in each arm to limit the inrush arm current while switching on or off a SM and to control the circulating current which is regulating the voltages of the SM capacitors [9]. The occurring losses in each arm are expressed by the resistance R_{arm} . A resistance R_c is put in parallel to the SM's capacitor to consider its leakage current. The three-phase grid is represented as 120° phase-shifted grid voltages v_{grid} and resistive-inductive grid impedances divided in R_{grid} and L_{grid} .

Mathematical Model

The overall voltage across the SMs in the upper and the lower arm are given in equations (1) and (2). $S(x)$ describes the switching state of the x th SM. During normal MMC operation only two switching states are used.

$$v_p = \sum_{x=1}^N S_p(x) \cdot v_{c,p}(x) \quad (1) \quad v_n = \sum_{x=1}^N S_n(x) \cdot v_{c,n}(x) \quad (2)$$

Both switching states and the paths of the arm current are illustrated in Fig. 2 [10]. When a submodule is inserted, the corresponding capacitor is charging or discharging.

Each phase voltage is described in equation (3). The AC current can be controlled by the difference between v_n and v_p . Half of the voltage difference can be defined as the converter voltage in equation (4) [11]:

$$v_{ac} = R_{\text{grid}} \cdot i_{ac} + L_{\text{grid}} \cdot \frac{di_{ac}}{dt} + v_{\text{grid}} \quad (3) \quad v_{\text{conv}} = \frac{v_n - v_p}{2} \quad (4)$$

The arm currents can be separated into two parts: the differential current i_{diff} and the contribution to the phase current i_{ac} . Considering an equal contribution, the arm currents can be described in equations (5) and (6). The current i_{diff} is a circulating current which is contained both in the upper and in the lower arm current without being measurable directly [12].

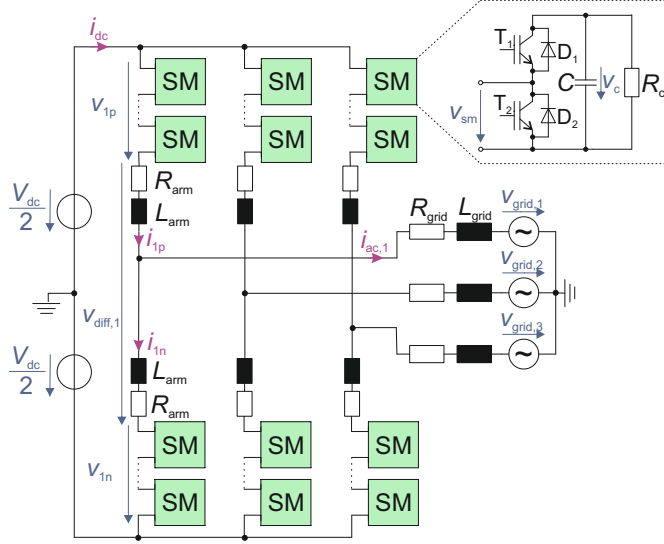


Figure 1: Three-phase circuit of a modular multilevel converter (MMC) in double-star connection

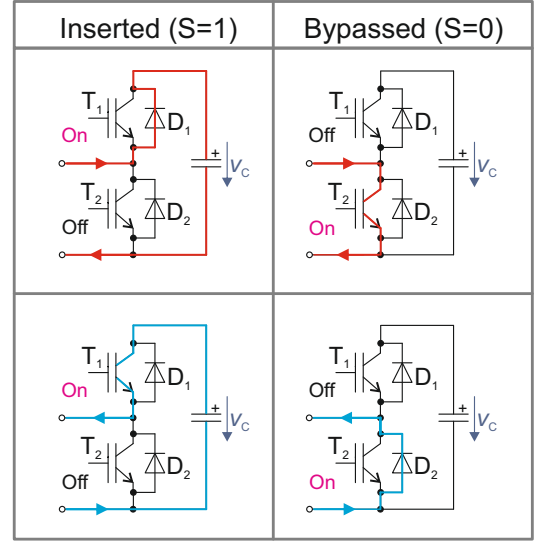


Figure 2: Current paths in an SM during normal MMC operation

$$i_p = i_{diff} + \frac{i_{ac}}{2} \quad (5)$$

$$i_n = i_{diff} - \frac{i_{ac}}{2} \quad (6)$$

The differential voltage v_{diff} is described in equation (7). The differential current can be controlled by the sum of v_p and v_n .

$$v_{diff} = 2L_{arm} \cdot \frac{di_{diff}}{dt} + 2R_{arm} \cdot i_{diff} \quad (7)$$

Control Scheme and Modulation

The power transmission and the average capacitor voltages are separately controlled, as illustrated in Fig. 3. The power transfer to the grid is controlled by the AC current. The coupling between d and q component is not depicted. The average capacitor voltage is controlled by the corresponding differential current in each phase [12]. The energy stored in the upper and the lower arm are equalized by eliminating the difference between their average capacitor voltages [13]. The voltage difference is multiplied by the modulation signal f_m to take into account the number of inserted SMs [13].

The current controllers are designed following the technical optimum principle [14]. The average capacitor voltage control is tuned to minimize the differential current ripple to relieve the semiconductors. The control parameters used in simulation are listed in Table I.

The number of inserted SMs n_{on} is calculated in order to follow the reference voltages v_{conv}^* and v_{diff}^* . Assuming that the DC voltage and the capacitor voltages are ideally regulated, the equations (8) and (9) are obtained [15]. Since the number of SMs is an integer, the results have to be rounded.

$$n_{on,p} = \text{round} \left(\frac{N}{2} - \frac{v_{conv}^*}{V_{co}} - \frac{v_{diff}^*}{2V_{co}} \right) \quad (8)$$

$$n_{on,n} = \text{round} \left(\frac{N}{2} + \frac{v_{conv}^*}{V_{co}} - \frac{v_{diff}^*}{2V_{co}} \right) \quad (9)$$

Capacitor Voltage Balancing

Beside the MMC control, a capacitor voltage balancing algorithm is required for NLM in order to achieve an equal power distribution among the SMs [16]. The arm currents are charging and discharging the ca-

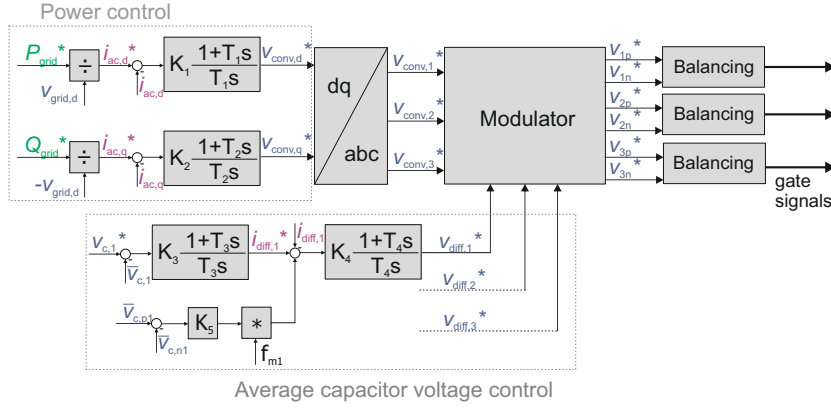


Table I: Control parameters

Parameter	Value
K_1, K_2	1016.7
T_1, T_2	55.5 ms
K_3	0.36
T_3	540 μ s
K_4	2400
T_4	0.36 s
K_5	0.005

Figure 3: Overall MMC control structure

capacitors of the inserted SMs whereas the capacitor voltages of bypassed SMs are approximately constant (cf. Fig. 2). The NLM is based on the calculation of the number of inserted SMs in each arm (cf. equations (8),(9)). Profiting by the number of switching combinations, the modulator can already balance the capacitor voltages up to a certain degree taking into account the direction of the arm current i_{arm} . In addition to this embedded balancing approach an active capacitor voltage balancing is useful to enhance the performance and to protect the semiconductors [15]. The goal is to keep the voltage in a predefined range. Depending on this range additional switching operations can be required. For active capacitor voltage balancing there are different approaches proposed and compared in literature [15].

Active Thermal Balancing

Losses occur when the semiconductor is conducting the arm current (conduction losses) and when the semiconductor is switching on or off (switching losses). The path of the arm current can be changed by changing the switching state of one SM (cf. Fig. 2).

The purpose of an active thermal control is the equal heat distribution among all SMs. The goal can be achieved by changing the switching state of SM as soon as the junction temperature of the active semiconductor becomes relatively high. In this way the spread in the junction temperatures can be minimized.

Usually, the capacitor voltage balancing algorithm takes decision of switching on or off SMs only based on the capacitor voltages and on the arm current direction. However, in this manner the temperatures of the semiconductors can be quite different. An active thermal balancing will take the junction temperatures into account so that the temperature of the semiconductor which carries the current after one switching operation should be minimal. A possible principle for a thermal balancing is summarized in Table II.

In equations (10)-(13) cost functions are defined to include both the SM capacitor voltage and the junction temperature of the active semiconductor. The weighting factor α is used to adjust the strength of active thermal balancing. The SMs to be inserted or bypassed are selected by minimizing the relevant cost

Table II: Active thermal balancing principle

$n_{on} - n_{on,old}$	i_{arm}	Action
positive	> 0	insert SM(s) with lowest temperature in Diode D_1
positive	< 0	insert SM(s) with lowest temperature in IGBT T_2
negative	> 0	bypass SM(s) with lowest temperature in IGBT T_1
negative	< 0	bypass SM(s) with lowest temperature in Diode D_2

Table III: Approach of active thermal balancing embedded in capacitor voltage balancing

Arm current	Switching on ($0 \rightarrow 1$)	Switching off ($1 \rightarrow 0$)
positive	$\min\{c_1\}$	$\min\{c_2\}$
negative	$\min\{c_3\}$	$\min\{c_4\}$

function according to Table III. When the weighting factor α is set to zero the active thermal balancing is disabled. In addition to the thermal balancing a maximum temperature should be defined as thermal protection.

$$c_1 = (v_c - v_{c,\min}) + \alpha_1 (T_{j,D1} - T_{j,D1,\min}) \quad (10)$$

$$c_3 = (v_{c,\max} - v_c) + \alpha_3 (T_{j,T1} - T_{j,T1,\min}) \quad (12)$$

$$c_2 = (v_{c,\max} - v_c) + \alpha_2 (T_{j,T2} - T_{j,T2,\min}) \quad (11)$$

$$c_4 = (v_c - v_{c,\min}) + \alpha_4 (T_{j,D2} - T_{j,D2,\min}) \quad (13)$$

Simulation Results

The simulation model is based on the mathematical model derived in the second section. The model is discretized in MATLAB by using a sampling time of $20\mu s$. The simulation parameters for an HVDC application are summarized in Table IV whereby the DC voltage is assumed as constant. The MMC consists of 150 SMs per arm and is rated for a nominal power of 300 MW. A high-voltage grid and the corresponding grid transformer are emulated. The employed control was described in the third section. A NLM is considered to achieve high efficiency. In addition to the capacitor voltage balancing embedded in NLM, the individual capacitor voltages are limited to 2500 V as protection. As semiconductors the IGBT module *CM1200HC-90R* from Mitsubishi is considered. The power losses occurring in the IGBTs and diodes are calculated by the datasheet characteristics according to [17]. The thermal model is based on the Foster Network whereby the thermal impedances of the semiconductors from junction to case are obtained from the datasheet. The thermal resistances of cooling between case and heatsink are given in Table IV as well. Since the time constants of the cooling elements would be relatively high, a constant temperature difference between cooling and case is considered for steady state operation. The temperature difference is calculated by the product of thermal resistance and the averaged power losses. The semiconductors are cooled by a water temperature of $T_a = 40^\circ C$.

Electrical and Thermal Behavior

The MMC is considered in steady state operation whereby the rated power is transmitted from DC to AC side. The three-phase converter voltages, the grid voltages and phase currents are depicted in Fig. 4a for a power transmission of 300 MW. A power factor of $\cos\phi = 0.95$ corresponds to a reactive power of 98.6 Mvar. The phase currents reach an amplitude of around 2150 A. The differential voltage and the differential current (phase 1) are depicted in Fig. 4b. The peak-to-peak ripple of the differential current

Table IV: MMC simulation parameters

Description	Parameter	Value	Unit	Description	Parameter	Value	Unit
SMs per arm	N	150		DC voltage	V_{dc}	300	kV
Arm inductor	L_{arm}	72	mH	Arm resistance	R_{arm}	200	m Ω
SM's capacity	C	10	mF	Cap. voltage limit	$V_{c,lim}$	2500	V
Grid voltage	$V_{grid,\Delta}$	$\frac{120}{\sqrt{3}}$	kV	Grid inductance	L_{grid}	25	mH
Grid resistance	R_{grid}	1	Ω	Sampling time	T_s	20	μs
Cool. resist. (T)	$R_{th,CK,T}$	5.2	$\frac{K}{kW}$	Cool. resistance (D)	$R_{th,CK,D}$	11.7	$\frac{K}{kW}$

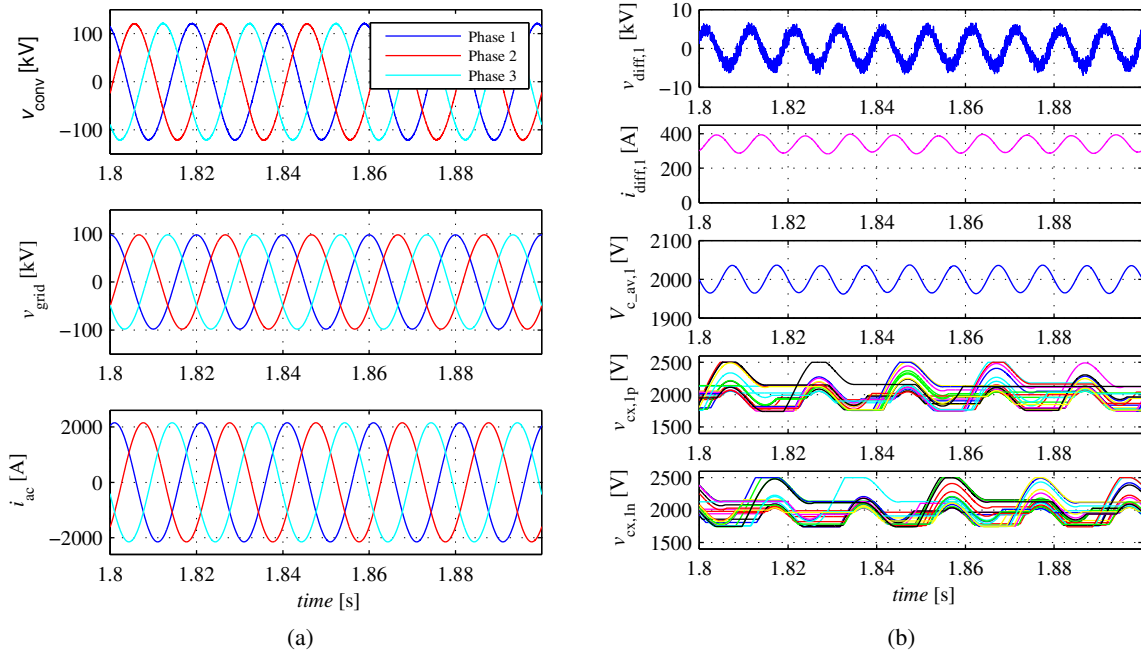


Figure 4: Electrical behavior of the MMC, steady state ($P_{grid} = 300\text{MW}$, $\cos \phi = 0.95$, $V_{c,lim} = 2500\text{V}$, $\alpha = 0$): a) Converter phase voltages, grid voltages and phase currents (3 phases), b) Differential voltage, differential current and capacitor voltages (phase 1)

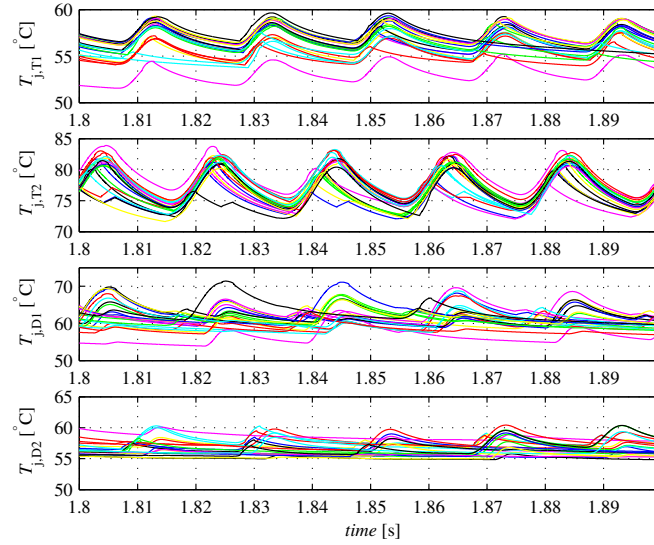


Figure 5: Thermal behavior of the semiconductors in the first 21 SMs in the upper arm, phase 1 (steady state: $P_{grid} = 300\text{MW}$, $\cos \phi = 0.95$, $\alpha = 0$)

is around 120 A, by obtaining an average capacitor voltage oscillating with about 70 V. The individual capacitor voltages are balanced and limited to 2500 V.

The thermal behavior of the semiconductors is considered in the upper arm (phase 1) and is depicted for the first 21 SMs in Fig. 5. The highest junction temperatures occur in IGBT T_2 caused by the considered power flow direction. T_2 is active when the corresponding SM is inserted and when the arm current is positive. The cyclic behavior of power losses also causes thermal cycles (50 Hz). Moreover, switching operations during a high arm current cause high peaks of power losses and quick changes in the junction temperatures. Basically, the temperatures are already regulated by the capacitor voltage balancing up to a certain degree.

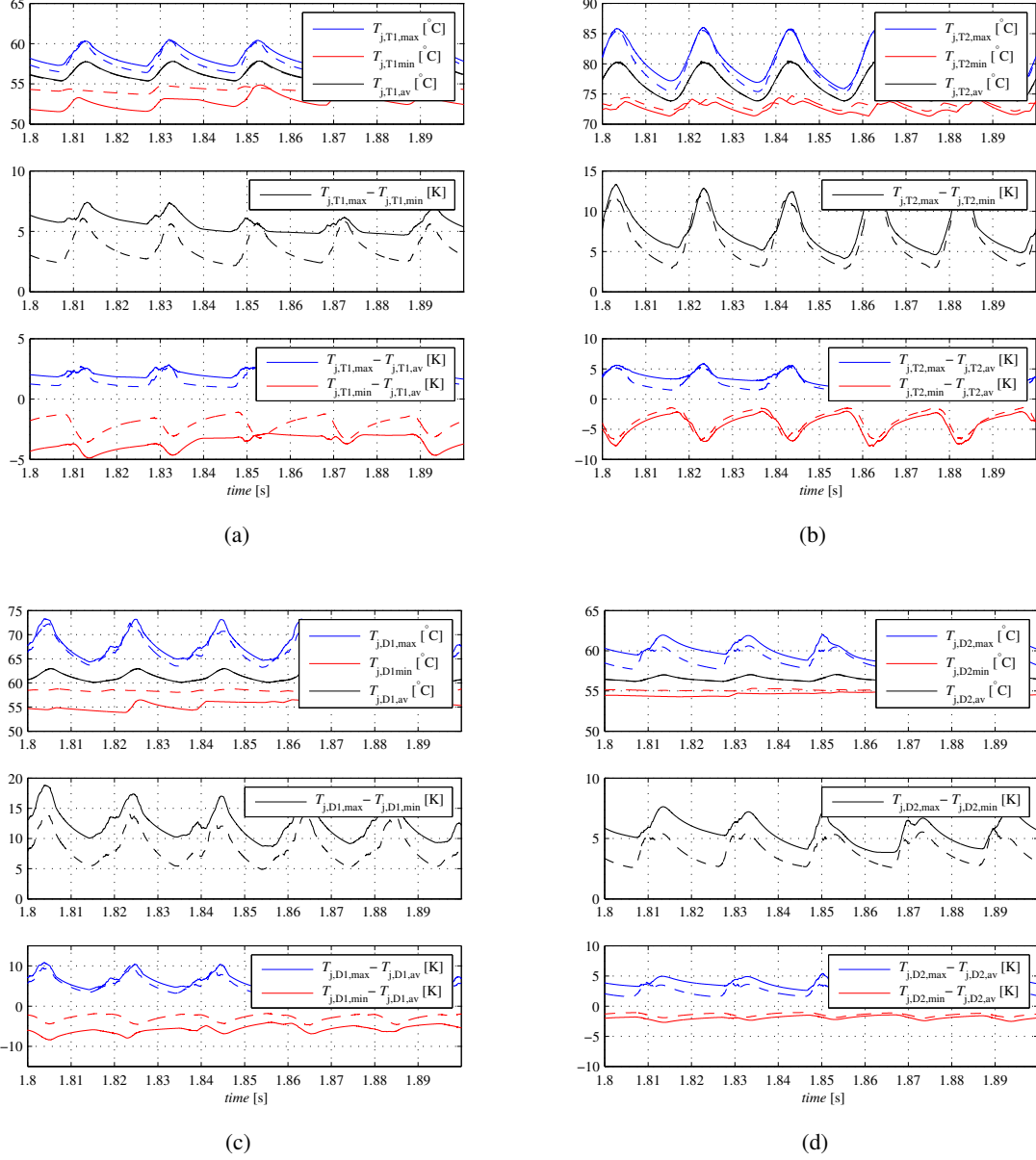


Figure 6: Maximum, min. and averaged junction temperatures in the upper arm, phase 1 (solid: $\alpha = 0$, dashed: $\alpha = 50$): a) IGBTs T_1 , b) IGBTs T_2 , c) Diodes D_1 , d) Diodes D_2 ($P_{\text{grid}} = 300\text{MW}$, $\cos\varphi = 0.95$)

Active Thermal Balancing

In order to further reduce the thermal spread in the temperatures, the active thermal balancing will be activated. The weighting factor α is set constant for the different cost functions: $\alpha = \alpha_1 = \alpha_2 = \alpha_3 = \alpha_4$.

In Fig. 6a and 6b the maximum, the minimum and the average temperatures for IGBTs T_1 and T_2 of the 150 SMs are depicted. The average temperature is almost constant independently from the weighting factor. For an active thermal balancing the switching frequency is only slightly increased caused by the capacitor voltage limitation which becomes more active. However, the spread in the temperatures is reduced by an active thermal balancing ($\alpha = 50$) compared to the usual capacitor voltage balancing ($\alpha = 0$). The same effect is shown for the semiconductors D_1 , D_2 in Fig. 6c and 6d. The averaged difference between highest and lowest junction temperature are summarized in Table V depending on the weighting factor. A reduction of between 1.5 K (T_2) and 4 K (D_1) is achieved by the active thermal balancing. This corresponds to a reduction of 19.5 % and 35.1 %.

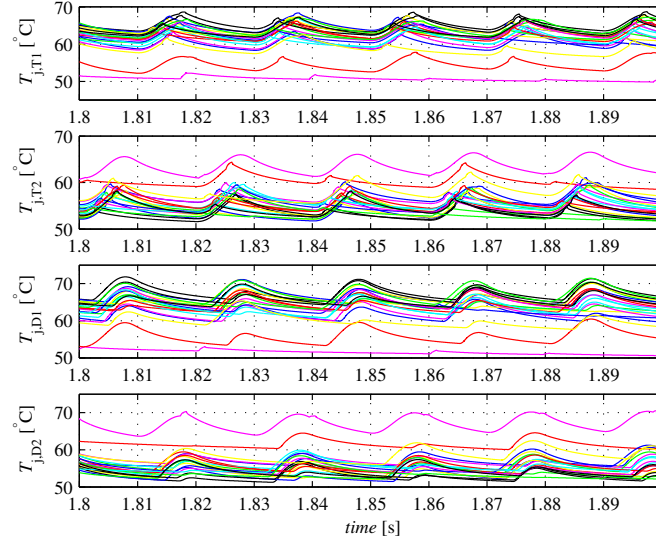


Figure 7: Thermal behavior of the semiconductors in the first 21 SMs in the upper arm, phase 1 (steady state: $Q_{\text{grid}} = 300\text{Mvar}$, $\cos \phi = 0$, $\alpha = 0$)

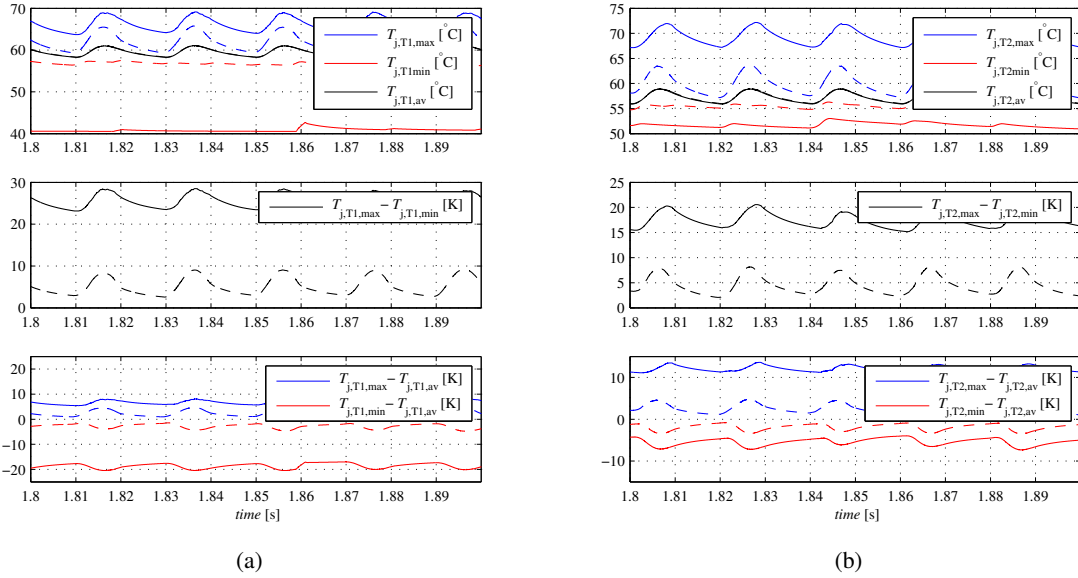


Figure 8: Maximum, minimum and averaged junction temperatures in the upper arm, phase 1 (solid: $\alpha = 0$, dashed: $\alpha = 50$): a) IGBTs T_1 , b) IGBTs T_2 ($Q_{\text{grid}} = 300\text{Mvar}$, $\cos \phi = 0$)

The effect of active thermal control for a high reactive power ($Q_{\text{grid}} = 300\text{Mvar}$) is considered in the next step. The thermal behavior of the semiconductors is depicted in Fig. 7 for the first 21 SMs without active thermal balancing. The spread in the temperatures is strongly increased. Since the arm currents are oscillating around zero, the individual capacitors are not charged as fast as before. For this reason, the semiconductors can conduct the current for a longer time without being changed by the capacitor voltage balancing.

The maximum, minimum and average temperatures for the semiconductors are depicted in Fig. 8 and 9 without and with active thermal balancing. The spread in the temperatures is strongly reduced by the active thermal balancing. According to Table VI the averaged difference between highest and lowest junction temperature is reduced by between 12.4 K (T_2) and 21.6 K (D_1). This corresponds to a reduction of between 71.4 and 79.7 %.

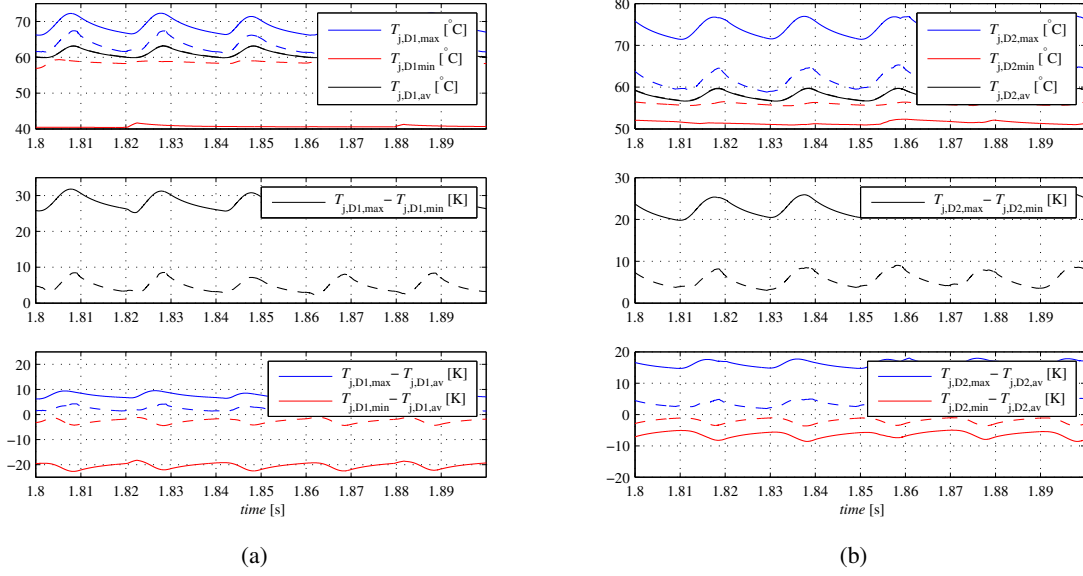


Figure 9: Maximum, minimum and averaged junction temperatures in the upper arm, phase 1 (solid: $\alpha = 0$, dashed: $\alpha = 50$): a) Diodes D₁, b) Diodes D₂ ($Q_{\text{grid}} = 300 \text{ Mvar}$, $\cos \varphi = 0$)

Table V: Maximum temperature difference (averaged) among all 150 SMs in the upper arm, phase 1 ($P_{\text{grid}} = 300 \text{ MW}$, $\cos \varphi = 0.95$)

α	T ₁	T ₂	D ₁	D ₂
0	5.7 K	7.7 K	12.2 K	5.6 K
50	3.7 K	6.2 K	8.2 K	4.0 K

Table VI: Maximum temperature difference (averaged) among all 150 SMs in the upper arm, phase 1 ($Q_{\text{grid}} = 300 \text{ Mvar}$, $\cos \varphi = 0$)

α	T ₁	T ₂	D ₁	D ₂
0	23.9 K	17.2 K	27.1 K	21.3 K
50	5.8 K	4.8 K	5.5 K	6.1 K

Conclusion

In this paper, an active thermal balancing for an MMC in an HVDC application was embedded in the capacitor voltage balancing algorithm by defining cost functions. Simulation studies performed in MATLAB showed that the proposed control reduces the spread in the junction temperatures. On the other hand, it has been shown that the capacitor voltage balancing algorithm also balances the temperatures up to a certain degree. Nevertheless, a significant improvement in the MMC thermal management can be achieved with the proposed control at the expense of a slight increase of the switching frequency. Especially for low power factors, the potential of an active thermal balancing is very promising.

References

- [1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, June 2003, pp. 6 pp. Vol.3–.
- [2] M. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *Power Electronics, IEEE Transactions on*, vol. 30, no. 1, pp. 4–17, Jan 2015.
- [3] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," *Industrial Electronics Magazine, IEEE*, vol. 2, no. 2, pp. 28–39, June 2008.
- [4] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of igbt modules in traction application," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, vol. 1, May 1997, pp. 425–430 vol.1.
- [5] D. Murdock, J. Torres, J. Connors, and R. Lorenz, "Active thermal control of power electronic modules," *Industry Applications, IEEE Transactions on*, vol. 42, no. 2, pp. 552–558, March 2006.
- [6] M. Andresen, M. Liserre, and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, Aug 2014, pp. 1–10.

- [7] M. Bakhshizadeh, K. Ma, P. C. Loh, and F. Blaabjerg, "Indirect thermal control for improved reliability of modular multilevel converter by utilizing circulating current," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, March 2015, pp. 2167–2173.
- [8] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (mmcc)," *Power Electronics, IEEE Transactions on*, vol. 26, no. 11, pp. 3119–3130, Nov 2011.
- [9] X. She, A. Huang, X. Ni, and R. Burgos, "Ac circulating currents suppression in modular multilevel converter," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct 2012, pp. 191–196.
- [10] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann and D. Soerangr, "HVDC PLUS - Basics and Principle of Operation," Siemens, Tech. Rep., August 2008.
- [11] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back hvdc system," *Power Delivery, IEEE Transactions on*, vol. 27, no. 3, pp. 1538–1547, July 2012.
- [12] M. Hagiwara and H. Akagi, "Pwm control and experiment of modular multilevel converters," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, June 2008, pp. 154–161.
- [13] J. Pou, S. Ceballos, G. Konstantinou, V. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *Industrial Electronics, IEEE Transactions on*, vol. 62, no. 2, pp. 777–788, Feb 2015.
- [14] V. Blasko and V. Kaura, "A new mathematical model and control of a three-phase ac-dc voltage source converter," *Power Electronics, IEEE Transactions on*, vol. 12, no. 1, pp. 116–123, Jan 1997.
- [15] A. Hassanpoor, L. Angquist, S. Norrga, K. Ilves, and H.-P. Nee, "Tolerance band modulation methods for modular multilevel converters," *Power Electronics, IEEE Transactions on*, vol. 30, no. 1, pp. 311–326, Jan 2015.
- [16] M. Guan, Z. Xu, and H. Chen, "Control and modulation strategies for modular multilevel converter based hvdc system," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, Nov 2011, pp. 849–854.
- [17] F. Erturk and A. Hava, "A detailed power loss analysis of modular multilevel converter," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, March 2015, pp. 1658–1665.