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ISBN 978-3-8007-4424-4

Proceedings of PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management.

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**Suggested Citation**

G. De Carne, M. Langwasser, X. Gao, G. Buticchi and M. Liserre, "Power-Hardware-In-Loop Setup for Power Electronics Tests," PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2017, pp. 1-7.

# Power Hardware In Loop setup for power electronics tests

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## Abstract

Evaluating the power electronics behavior in real grid conditions is challenging. In simulation, large grids and complex systems can be simulated, however the power electronics, simulated with simplified models, cannot show realistic performances, due to the difficulty to quantify parameters such as delays, damping, and noise impact. On the other hand, lab experiments give more accurate analysis, but in smaller scale than the simulation, due to space and resources limitation. The Power Hardware In Loop (PHIL) evaluation solves this problem, simulating complex grids in software, and interfacing them with real hardware by means of an interface converter. In this work, the PHIL is applied to the Smart Transformer (ST) case in order to show the full benefit of this technique.

test power electronics devices by means of Power Hardware Loop (PHIL) [13, 14, 15, 16]. The power electronics under test (e.g., ST), can prove its performances in realistic conditions, such as the simulated grid in the Real Time Simulator (RTDS), difficult to reproduce in laboratory. The PHIL allows to take into account phenomena not easily evaluable, like control and communication delays, filter damping, and sensor accuracy of the power electronics during the tests, that are difficult to evaluate in software environment. On the other hand, a pure lab validation may be challenging to realize due to the extension of a real LV grid and the complexity of grid behavior. Moreover, such phenomena, like the drop of voltage along the lines, are difficult to reproduce due to the unpractical realization of long lines under laboratory conditions.

## 1. Introduction

The electrical grid must be facing multiple challenges due to the high penetration of Distributed Energy Resources (DER), such as Distributed Generation (DG) and new loads, like the Electric Vehicles (EV). They can easily affect the grid operation [1], making the grid control difficult. The Smart Transformer (ST) (Fig. 1) is a power electronics based transformer [2, 3] that in addition to the voltage transformation from Medium Voltage (MV) to Low Voltage (LV) grids, offer additional services to both grids [4, 5, 6]. However, the ST advantages in the MV/LV grids have been addressed mainly with simulations or oversimplified lab experimental setup: balancing of LV grid voltage and MV grid current [5], on-line load sensitivity identification in LV grids [7], frequency and voltage amplitude control [4, 6, 8, 9, 10], power management in DC grids [11], and the increase of hosting capacity for DERs integration [12].

This paper instead aims to show the possibility to

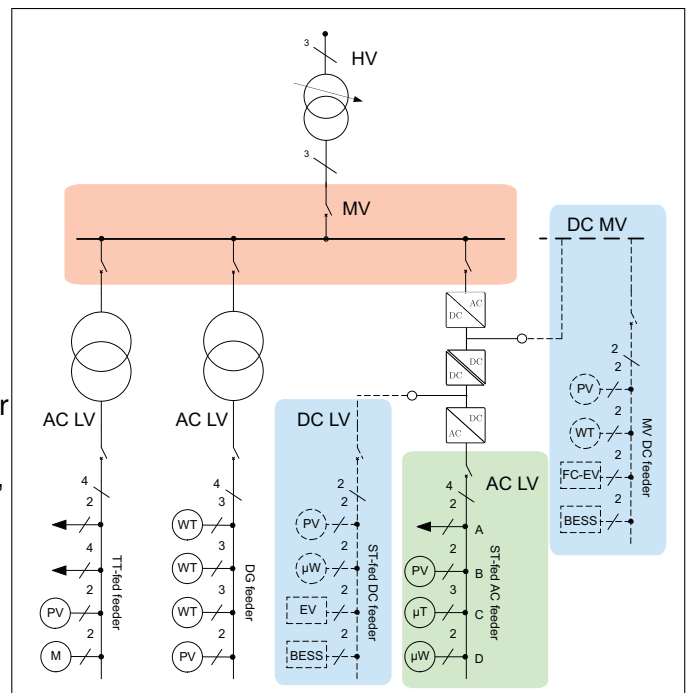


Fig. 1: Smart Transformer-fed AC/DC distribution grid.

This paper is structured as follows: section II gives an overview on the ST technology and its control; section III describes the PHIL facility implemented

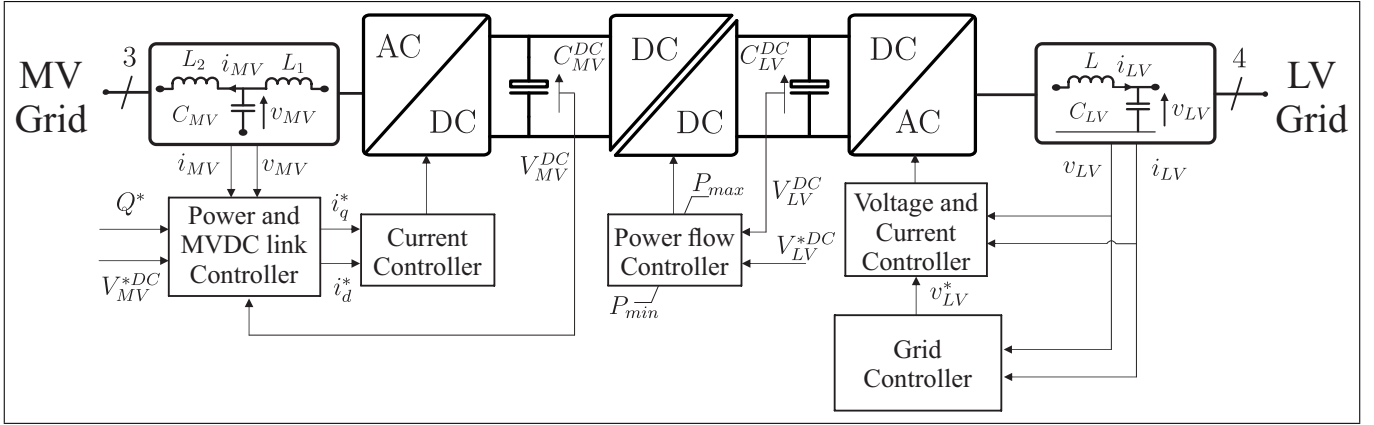


Fig. 2: Smart Transformer control scheme

at the Chair of Power Electronics at the University of Kiel; the PHIL evaluation capability for the ST grid services case is demonstrated experimentally in section IV. Finally, section V is dedicated to the conclusions and future work.

## 2. Concept and control of the Smart Transformer

The Smart Transformer (ST) is a three-stage power electronics-based transformer composed of a MV converter, that transforms the voltage from the MV AC grid to the MV DC link; a DC/DC stage, transforming the voltage levels; and a LV converter interfacing the LV grid. The ST can offer new ancillary services to the grid and offers a possibility for DC grid connections.

The control strategy of the ST depicted in Fig. 2 do not differ substantially, despite several topology solutions exist for each stage.

The MV side controls the MV DC link voltage at the nominal value by controlling the current in the MV grid. In addition, the MV converter controls the reactive power injection in the MV grid. The DC/DC converter (a Dual-Active Bridge (DAB) has been adopted in this work) has two tasks: to transform the voltage from MV to LV and to control the LV DC link voltage, exchanging power between the two DC stages. The LV side controls the voltage waveform to be sinusoidal with amplitude and frequency fixed to the reference values independently from the load power request.

The MV converter controller consists of an outer

Reactive power / DC voltage loop and an inner AC current loop. In the outer loop the DC link voltage is controlled setting the new AC active current reference. The reactive current loop controls the reactive power injection receiving the power reference either remotely, by an external power set point, or locally, by means of Q/V droop controller. The inner loop is composed of two separate loops enabling the independent control of the reactive and active current to be requested from the MV grid.

In order to regulate the power flow between the two DC stages the DAB controller has a power flow controller. It controls the LV DC link voltage setting the power reference of the DAB. The reference power is limited between the  $P_{max}$ , determined by the ST sizing, and  $P_{min}$ . If  $P_{min}$  is set to 0, it can avoid the power flow reversal in MV grid.

The LV converter has two control loops: the outer one controls the AC voltage and the inner one the AC current. The outer loop, controlling the voltage, generates the new AC current reference for the inner loop. The current loop outputs, added to the voltage reference waveforms, are the modulation signals to control the DC/AC converter.

## 3. Power Hardware In Loop

The PHIL adopted in the Chair of Power Electronics is realized by means of a current-type loop. The PHIL scheme is depicted in Fig.3 and the PHIL setup realized in lab is shown in Fig.4. The PHIL shown in Fig.3 has been realized to test the ST performances. The ST controls the voltage  $v_{HuT}$

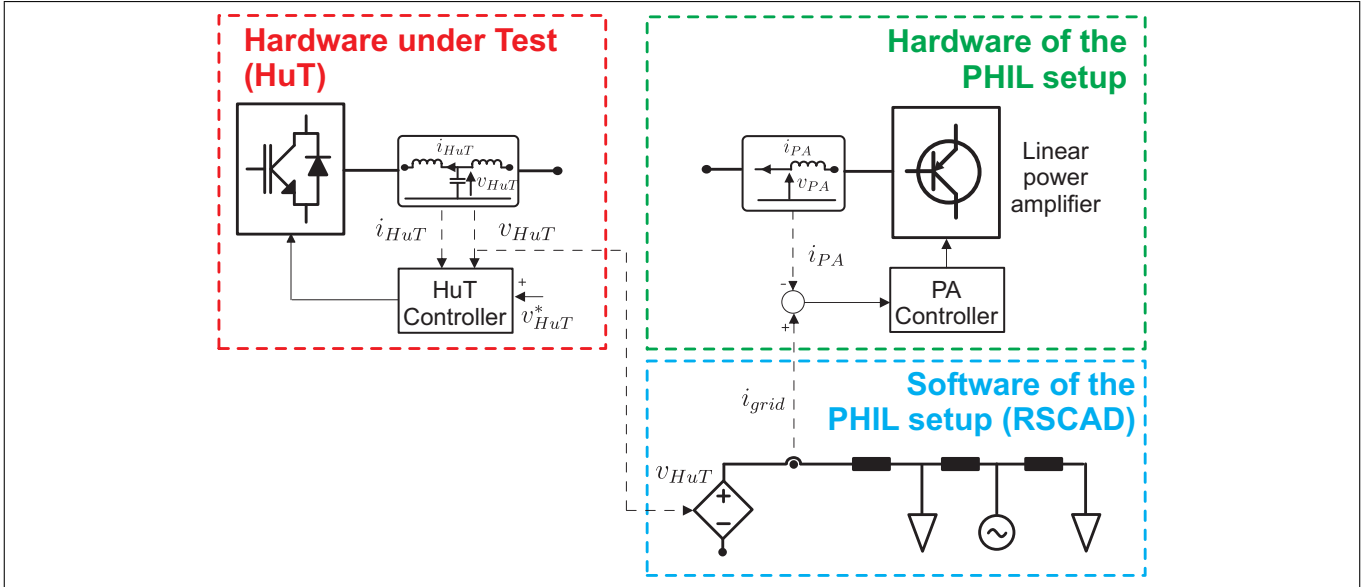


Fig. 3: PHIL: Hardware under Test (HuT) (red frame), Hardware of the PHIL setup (green frame), Software of the PHIL setup (RSCAD) (blue frame).

on the filter capacitor. The measurement system measures the voltage and send the measurement signals  $v_{HuT}$  to the RTDS software, RSCAD. Here the voltage is applied directly in the simulated grid by means of an ideal controlled voltage source. The current demanded by the grid  $i_{grid}$  is sampled in RTDS and sent to a current controller, that controls the current injection  $i_{PA}$  of the linear power amplifier (3 phase, 4 quadrant Spitzenberger&Spies PAS15000) in order to reproduce accurately the grid current  $i_{grid}$ , closing the loop. Between the simulated grid and the ST hardware, a current scale factor can be chosen to represent in hardware systems bigger than the HuT size. In this case a scale factor of 50 has been introduced in the current to cope with the limited power capability of the hardware in lab. It means that 1 kW power change in the hardware side corresponds to 50 kW power change in RSCAD. Any change in the current absorption in RSCAD, due to a different load demand, influences the ST controller, and, vice-versa, any change in the ST voltage amplitude or frequency, impacts on the grid power consumption.

The parameters of the ST setup are specified in Table 1, where  $K_{pV,ST}$ ,  $T_{iV,ST}$ ,  $K_{pI,ST}$ ,  $T_{iI,ST}$  are the proportional gain and the integral time constant of the ST voltage and current controllers, respectively.

No standard model of the LV grid has been pro-

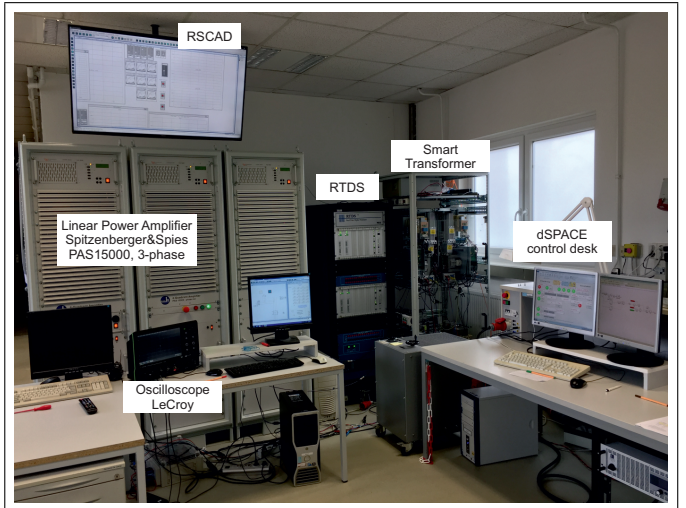


Fig. 4: PHIL facility realized in the lab

Tab. 1: ST parameters

Parameter	Value	Parameter	Value
S	4 kVA	$K_{pV,ST}$	0.2
$f_{sw}$	8 kHz	$T_{iV,ST}$	0.004
$L_{1,ST}$	5.0 mH	$K_{pI,ST}$	1.25
$C_{f,ST}$	1.5 $\mu$ F	$T_{iI,ST}$	0.004

posed in literature due to the heterogeneity of the LV grids. This work applies a modified version of the CIGRE European LV distribution network benchmark described in [17] and depicted in Fig.5. The LV grid has been implemented in RSCAD and simu-

Tab. 2: Load Data

Load	Bus	Active Power (kW)	$\cos\varphi$
$L_1$	11	6.7	0.95
$L_2$	15	19.2	0.95
$L_3$	16	19.2	0.95
$L_4$	17	2.7	0.95
$L_5$	18	8.8	0.95

lated with a time step of  $45 \mu\text{s}$ , typical of the PHIL applications [18].

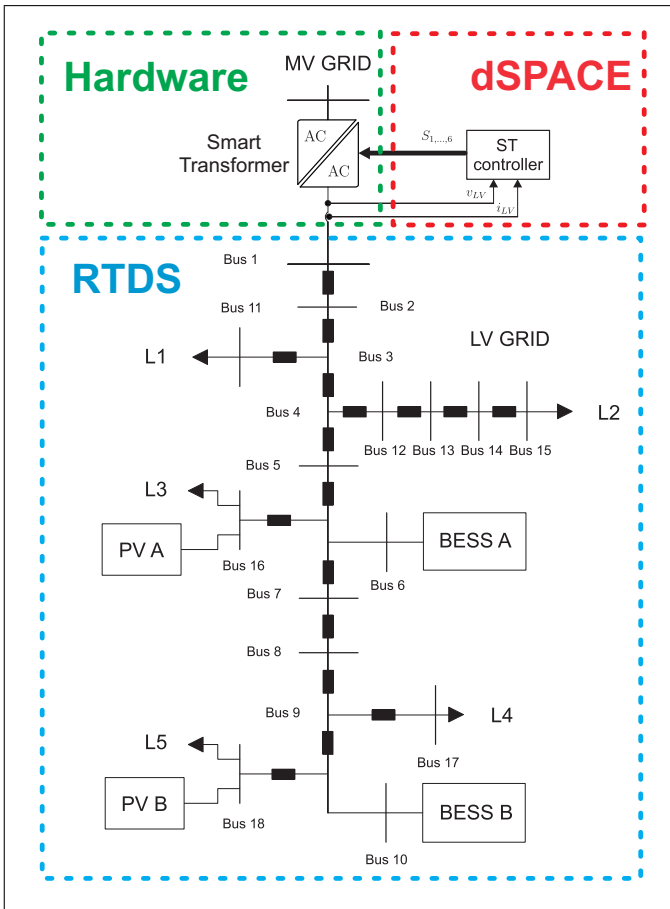


Fig. 5: modified CIGRE European LV distribution network benchmark implemented in RSCAD.

The CIGRE grid has been realized under the following assumptions: 1) the three-phase loads have been considered as constant impedance model and balanced, 2) the wind turbine has been neglected, 3) the battery energy storage systems (BESS)  $A$  and  $B$  are initially set to 10 kW and  $-20$  kW respectively. Table 2 itemizes the load data and the position in the grid, while Table 3 itemizes the location of the two BESSs and the two PV power plants.

Tab. 3: DERs Data

DER	Bus	Apparent Power (kVA)	$\cos\varphi$
BESS A	6	75	1.00
BESS B	10	25	1.00
PV A	16	4	1.00
PV B	18	3	1.00

## 4. PHIL experimental evaluation

The PHIL allows to analyze the impact of grid phenomena on the grid devices and on the hardware under test, here the ST. Two different test cases have been considered to analyze the capability of PHIL at the Chair of Power Electronics. In the first case a BESS power change has been performed to analyze the impact on hardware of software's side variation. In the second case, the ST varies its voltage amplitude set point, and the behavior of the LV grid is observed.

### 4.1. BESS power variation

In this section the case of power variation of BESS  $A$  from 10 to 50 kW, leaving invariant the reactive power (Fig. 6b), has been analyzed. The ST active power decreases to compensate the power unbalance in the LV grid, decrementing the provided power from 100 to 55 kW. This variation can be seen also in the hardware side (Fig. 7). The ST current varies passing from  $4 A_{peak}$  to  $2.5 A_{peak}$  (Fig. 7b), while the ST voltage remains constant during the transient and in steady state (Fig. 7a). The ST active power changes from 2 kW to 1.1 kW, reflecting the power change seen in the software side, scaled down of a factor 50.

The same current profile shown in (Fig. 7b) can be visualized as RTDS plot in Fig. 8. The current waveform in red represents the current measured in the RTDS simulated grid (scaled down of a factor 50). The black curve is the measured current in the hardware side. As can be noticed, the current controller of the interface can control in hardware the current measured in the RTDS simulation, both in steady-state and during transients.

During the transient the PHIL follows correctly the current change that occurs in the hardware side, as

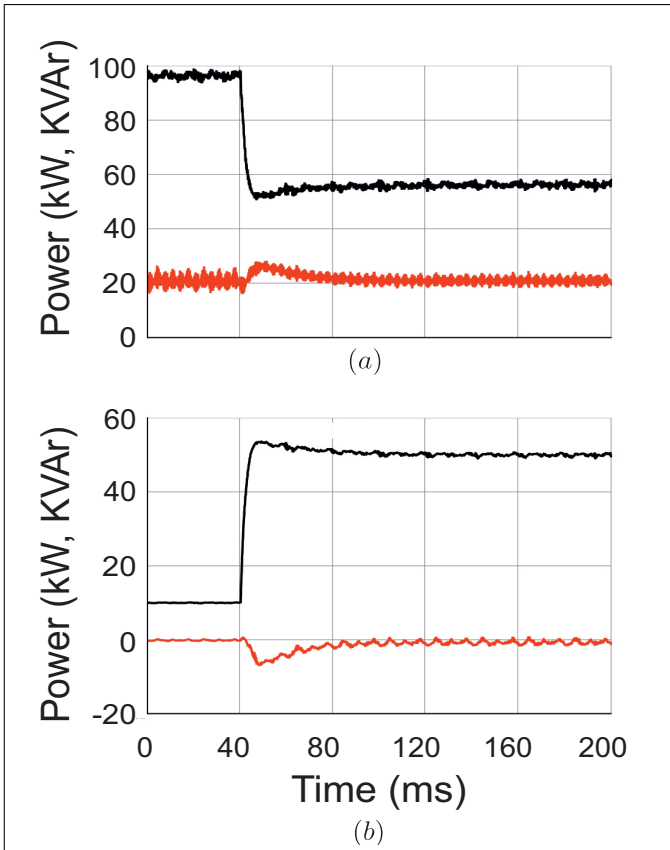


Fig. 6: RTDS side: (a) ST active (black line) and reactive (red line) power; (b) BESS A active (black line) and reactive (red line) power

depicted in Fig. 9. The RTDS current controller is able to reproduce the current behavior also in case of fast transients. In Fig. 9, only a small amplitude variation can be seen during the transient (around 1% of relative error). However this small attenuation is compensated after half cycle, restoring in the hardware side the reference current value.

One of the main advantages to perform a PHIL evaluation is the possibility to analyze which impact certain actions have on the grid. In Fig. 10 the rms voltage profiles have been plotted during the BESS power variation. This allows to determine if certain control actions can impact negatively in the grid, that is difficult to realize in pure hardware environment.

#### 4.2. ST voltage amplitude variation

In this section, the impact of a hardware change on the RTDS simulated grid side is considered. In

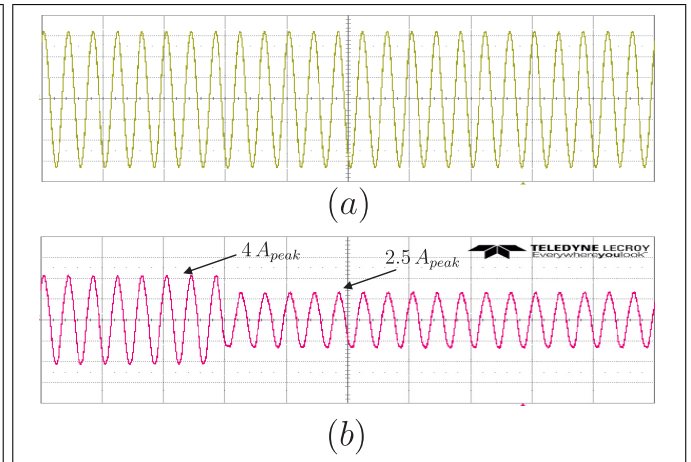


Fig. 7: Hardware side: (a) ST voltage, and (b) ST current during the power transient

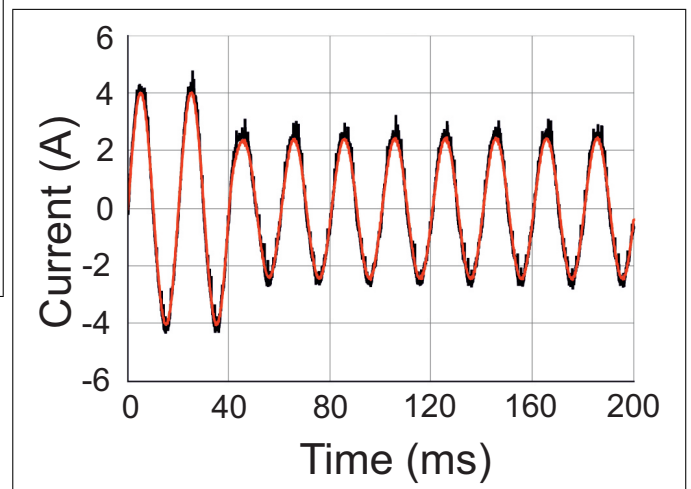


Fig. 8: ST current: measured current in RTDS (red line) and measured current in hardware side (black current).

particular, the ST applies a voltage amplitude variation to the downstream LV grid. This kind of actions have their use in services like Soft Load Reduction [6] or the ST overload control [4]. In this case a voltage decrease from  $325 V_{peak}$  to  $300 V_{peak}$  has been applied, corresponding to about 8% voltage variation. The impact on the grid can be seen in Fig. 11. The voltage decreases in not uniform way in the grid, and in several of them (the furthest away from the MV/LV substation) the voltage drop is severe (below 0. pu). On the hardware side, the voltage variation can be seen in Fig. 12a. The voltage decreases of the requested amount and the ST injected power decreases from 2 kW to 1.75 kW.

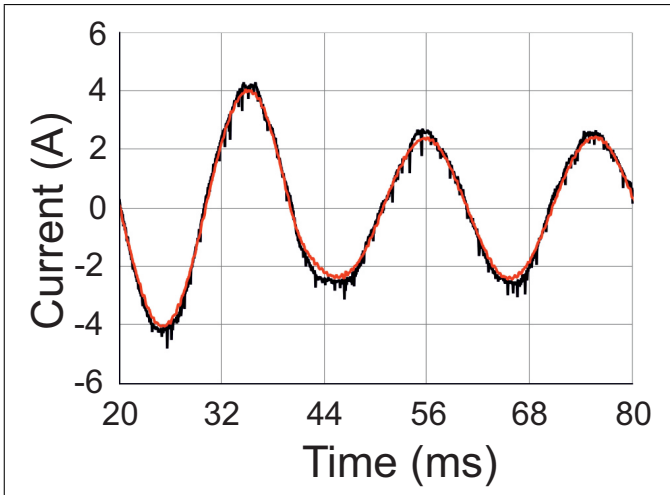


Fig. 9: ST current, zoomed: measured current in RTDS (red line) and measured current in hardware side (black current).

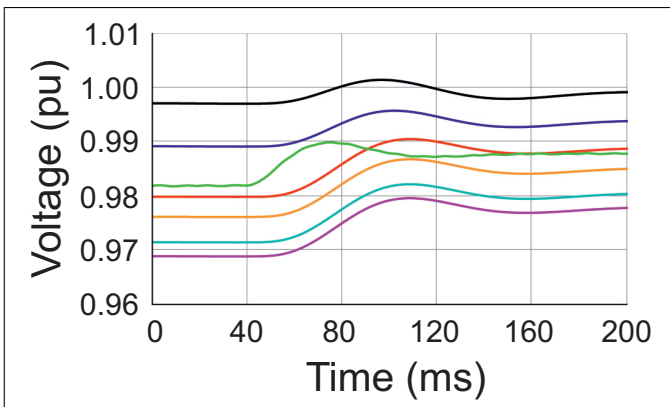


Fig. 10: Voltage profiles in different grid buses.

## 5. Conclusions

The Power Hardware In Loop represents an interesting tool for hardware testing in realistic grid conditions. The PHIL realized at the Chair of Power Electronics enables the possibility to test grid-forming converters, like the Smart Transformer, in realistic grid conditions. It proved to be an optimal solution to test the interaction of the grid and hardware under test. In particular, the impact of LV grid power consumption change on the ST has been considered. Changing the BESS power set-point, the ST power injection varies, and this has an impact on the voltage profile in the LV grid. The ST can vary the voltage amplitude set-point in order to provide services to the distribution grid. With a PHIL evaluation, the impact on the downstream LV grid can be easily observed, analyzing the voltage profiles in

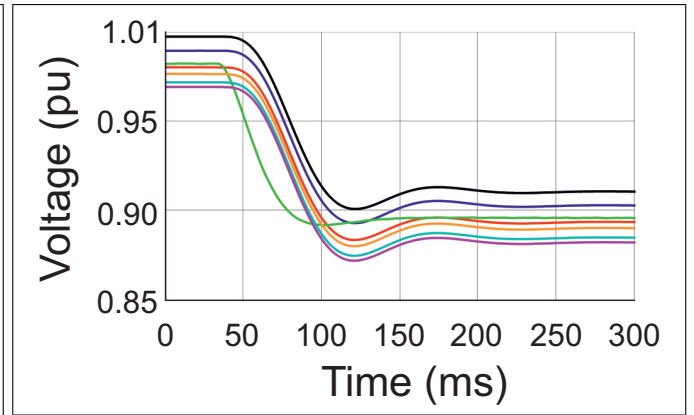


Fig. 11: Voltage profiles in different grid buses.

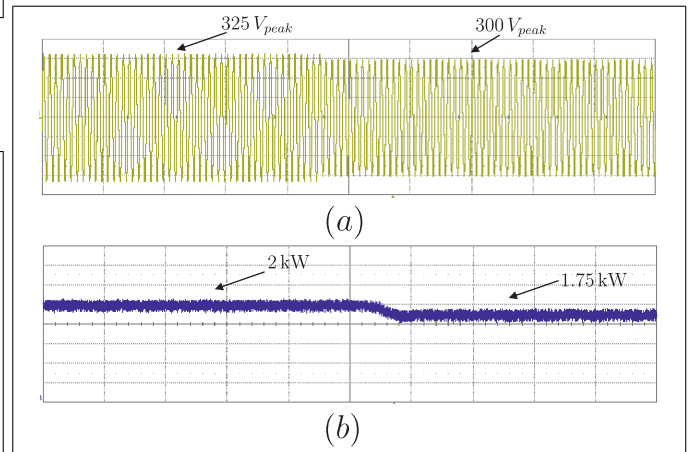


Fig. 12: Hardware side: (a) ST voltage, (b) ST power during the power transient

each bus of the grid.

## Acknowledgment

The research leading to these results has received funding from the European Research Council under the European Union's Seventh Framework Program (FP/2007-2013) / ERC Grant Agreement n. [616344] - Heart.

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