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Frequency-Adaptive Control of Smart Transformer-Fed Distribution Grid

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***Abstract*—The Smart Transformer (ST), a solid-state transformer with control and communication functionalities, that interfaces Medium Voltage (MV) and Low Voltage (LV) grids, enables the control of the frequency in the LV grid independently from the MV one. In a ST-fed distribution grid, the ST can interact with the droop controllers of local generators and loads frequency characteristic to control the LV power demand. However, most of the existing controllers for power converters cannot guarantee good harmonic control under variable frequency condition. To address this issue, a frequency-adaptive control scheme based on the Fractional-Order Repetitive Control (FORC) and the frequency-adaptive Phase-Locked Loop (PLL) are proposed in this paper. The proposed scheme provides fast online parameter tuning capability in order to be highly adaptive to variable frequencies, and it can be easily implemented in the power converters controllers of a ST-fed distribution grid. Moreover, the stability analysis of the frequency-adaptive system considering the effect of synchronization has been investigated in the paper. Simulation and experiments have been carried out to verify the effectiveness of the proposed scheme as well as the considered scenarios.**

***Index Terms*—Solid state transformer, distribution grid, frequency control, synchronization, stability.**

I. Introduction

THE increasing integration of Distributed Energy Resources (DERs) poses new challenges to the distribution grids. The intermittent nature of these sources may create problems to the traditional distribution grids in terms of voltage limit violation, current congestion, unintentional islanding, harmonic pollution, and protection issue [1], [2]. These problems not only jeopardize the performance and reliability of local grids, but also propagate to the other voltage level grids (e.g. MV grids) through transformers. Of particular concern is the voltage violation phenomenon due to the reverse power flow created by high renewables power injection. For instance, if a high amount of photovoltaic power plants are installed in a distribution grid, the power in the grid can reverse during low load conditions, causing an upper voltage limit violation [3]. If this phenomenon is not delimited, but it is widespread to many branches, the voltage control can represent a difficult task to accomplish. To solve these problems, the three-stage power electronics-based ST represents a promising solution [4]: it provides new features and ancillary services to distribution grids, for instance, voltage and current profiles improvement [5], balancing services in both MV and LV sides [6], load identification and control [7], and stability and reliability improvement of overall system [8].

One of the promising features of ST is the decoupling of the MV and LV grids, that becomes independent from the voltage and frequency point of view (see Fig. 1). One of the possible scenarios is to adapt the LV frequency in order to interact with the frequency-dependent DERs and loads in distribution grids [9]. The idea is to modify the power sharing between ST and DERs by means of the ST frequency control with two goals: 1) the current flow through the ST can be limited so that overload can be avoided [10]; 2) the reverse power flowing of the distribution grid can be avoided [9], [11].

One of the main challenges of frequency control is to regulate ST voltage and DER current waveforms under variable frequencies. The design of the controller of a power converter in traditional distribution grid/microgrid usually assumes signals with specific fundamental frequency (e.g. $50/60\,\mathrm{Hz}$ signal) and offers good voltage/current control performance as well as harmonic elimination under nominal frequency condition [12]. In case of grid with variable frequencies, for example in a ST-fed distribution grid, some of the conventional control strategies as well as design criteria may lead to performance degradation. There are several conventional frequency-adaptive control strategies including: hysteresis control [13], deadbeat control [14], proportional integral (PI) control and proportional resonant (PR) control with frequency adaptivity [15], which could independently maintain their performance of grid frequency to some extent. Nevertheless, these methods have drawbacks: the hysteresis control can suffer from high switching stress or inaccurate harmonic elimination due to its nonlinear nature; the deadbeat control is sensitive to the accuracy of system parameters; both PI and PR with frequency adaptivity can well handle the fundamental frequency signals but may not perform optimally in case of high harmonic content. Multiple resonant controllers with frequency adaptivity can indeed achieve good tracking ability at selective harmonic frequencies, however it is computational heavy and complex to tune. Based on the Internal Model Principle (IMP), repetitive control offers a simple way to achieve zero steady-state error

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tracking of any periodic signal with a known period due to the introduction of high gains at interested harmonic frequencies [16], but the Conventional Repetitive Control (CRC) with fixed sampling rate is sensitive to the frequency variation from the harmonic control point of view. In this context, a simple and compact structure frequency adaptive Fractional-Order Repetitive Control (FORC) scheme has been proposed [17], derived from the IMP and able to provide high control performance with arbitrary frequency. Several case studies on FORC-controlled systems have been proposed in literature for different applications, such as programmable AC power supply [17], grid-connected power converter [18], and active noise cancellation [19]. In this paper, a FORC plus PI along with fast frequency detection scheme is proposed and has been implemented in both ST and DERs to achieve a frequency-adaptive distribution grid. Equipped with the proposed scheme, the ST-fed distribution grid is able to modify online the generator production and load consumption by changing LV grid frequency, while maintaining good voltage/current waveforms under variable frequency condition.

The concept of frequency-adaptive ST-fed grid was firstly proposed in [20], where the system configuration and a system-level simulation based on the Hardware-In-the-Loop (HIL) method were given. On this basis, further investigations in terms of control design, stability issue, and implementation are provided in this paper. In general, this paper proposes a comprehensive design of the frequency-adaptive control systems for ST-fed grid, and investigates on stability issues that may arise in certain operative conditions. To study the effects of synchronization on the system stability, a complete analysis considering the FORC and the PLL is given. Experimental results have been provided to validate the control strategies experimentally, using commercial converters as power-electronics components of the system. The paper structure is organized as follows: the concept of a frequency-adaptive ST-fed distribution grid is presented in Section II. The proposed control strategy and control design are comprehensively presented in Section III. The stability issue study of the frequency-adaptive applications, the stability analysis considering FORC and the influence of frequency detection methods are given in Section IV. Case studies are investigated in Section V with the validation of the proposed system as well as of the control strategy by means of a laboratory micro-grid. Eventually, conclusions are drawn in Section VI.

II. Frequency-Adaptive ST-Fed Distribution Grid

Differently from the traditional transformer-fed grids, a ST-fed distribution grid offers advanced control capability and ancillary services to the overall system. The ST can modify the frequency of LV grid within the allowed limits of the local grid codes and interact with the droop controlled-DERs as well as frequency-dependent loads (e.g., induction motors). By changing the frequency, the injected/consumed power of generators/loads can be varied. The typical power/frequency characteristics of DER and loads in a distribution grid are shown in Fig. 2, in which the DER and loads characteristics are represented by the red and blue curves, respectively. It

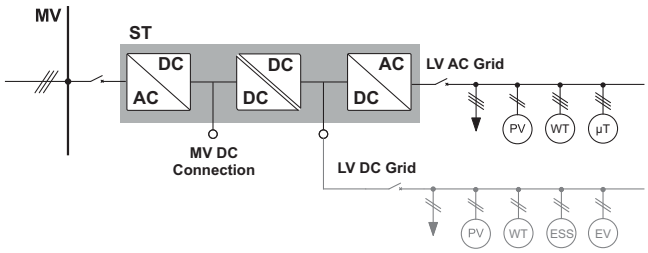


Fig. 1. LV Smart Transformer-fed grid.

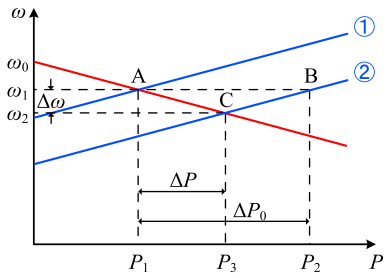


Fig. 2. Typical steady-state power-frequency curves of DER (red curve) and loads (blue curves).

is seen that the power electronics-interfaced DER with droop control reproduces the $P-f$ droop behavior of synchronous generators used in conventional power system [21].

The ST can deploy a frequency control to modify the power sharing in the distribution grid, demanding a variation of the power set-points of local DERs. As presented in [12], the grid converters of DERs can be classified as: grid-feeding power converter and grid-supporting power converter. The latter one has the main task to supply the local load imposing the voltage, and can absolve complementary tasks, like grid support services. Among these, the DG power control by means of frequency variation is present. A droop curve allows the DER to output a given amount of power to the grid for regulatory purposes. In the case of a load increase and current exceeding the ST security limit, the frequency control decreases the frequency in the LV grid. The droop controllers of DERs correspondingly react to the frequency variation and increase the active power generation (assuming the DERs operates at unity power factor), while the frequency-dependent load demand decreases following its $P-f$ characteristic. On the other hand, when the generation of DERs is higher than the load demand and the storage rating, the frequency control increases the LV side frequency to allow the reduction of DERs production and the increase of load consumption. As an example of the proposed method, in Fig. 2 the distribution grid has its initial equilibrium at point A. When a change from curve 1 to curve 2 in the electric demand occurs (point $A \rightarrow B$), with a power increase of ΔP_0, the frequency control decreases the frequency from ω_1 to ω_2. Finally, the system reaches a new equilibrium point (i.e., point C) and an eventual overload of the ST can be avoided. Within this context, the frequency-adaptive ST-fed distribution grid shows two main advantages: 1) can mitigate overloading issue; 2) can reduce the power rating of controllable load and storage systems.

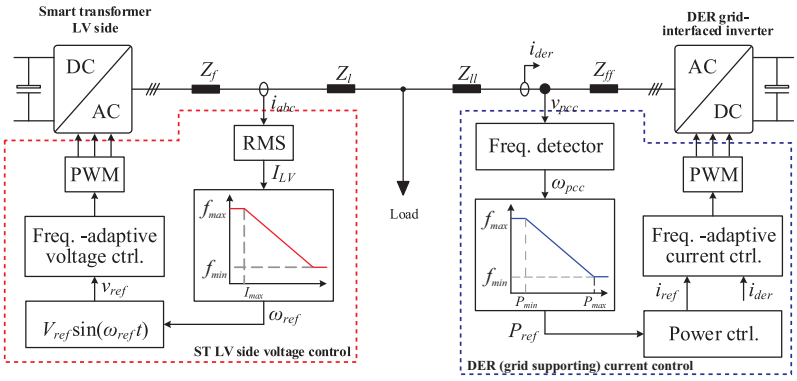


Fig. 3. Schematic diagram of a frequency-adaptive ST-fed distribution grid.

The simplified system configuration of a ST-fed distribution grid with frequency control is given in Fig. 3, which is composed of 1) the LV side ST and its voltage controller, and 2) the DER and its current controller. Z_f, Z_{ff} are the output filters of ST LV side, and DER, Z_l and Z_{ll} are the equivalent line impedances. Droop controllers based on power-frequency curves have been employed in both the ST LV side voltage control and the DER power/current control: for the ST voltage control, the droop control provides the frequency set-point for the grid according to the ST output power; for the DER power/current control, the droop control determines the DER active power set-point according to the grid frequency.

To better illustrate the scheme, an overloading scenario is given as an example. During the normal operation, namely i_{abc} within the safe range, the LV grid frequency is kept constant at the nominal value (50 Hz). When the load increases, i_{abc} increases as well, and the frequency of LV side voltage is modified according to the droop curve, with a frequency range from 49 Hz to 50 Hz in this scenario. The characteristic of the droop curve is defined based on the control objectives. As soon as the RMS value of i_{abc} exceeds the security limit I_{max}, the frequency decreases. In the DER side, the frequency change is detected by a frequency detection device. Two possible alternatives can be adopted to achieve fast frequency detection: 1) fast PLL (e.g. Second Order Generalized Integrator (SOGI)-PLL), whose dynamic response is much faster than the maximum rate of grid frequency [22]; 2) real-time communication (e.g. powerline carrier communication) between ST and DERs [23]. Once the frequency is detected, the DER varies the power generation following the P-f droop curve till reaching a new equilibrium point.

III. Frequency-Adaptive Control

Compared to the conventional frequency adaptive control, the FORC derived from the IMP-based control is able to achieve zero steady-state error tracking of any periodic signal with a known period. In this section, a simple frequency-adaptive control adopting PI and FORC in the $\alpha\beta$ frame is proposed. A preview of the frequency-adaptive FORC is presented in Section III-A. The detailed design of the frequency-adaptive controllers for both the ST voltage control and DER current control is given in Section III-B.

A. Frequency-Adaptive FORC

The IMP-based control schemes, for instance, CRC, have been well developed for power converters because of their zero steady-state error tracking ability [24]. Including the internal model of a generic periodic signal, the CRC can accurately track or suppress any periodic input or disturbance. A typical closed-loop digital control system with a plug-in CRC for a power converter is shown in Fig. 4a, where $R(z^{-1})$ is the reference input, $Y(z^{-1})$ is the system output, $E(z^{-1})$ is the control error, $D(z^{-1})$ represents the disturbance; $G_c(z^{-1})$ is the transfer function of the original feedback controller, $G_d(z^{-1})$ is the $1.5T_s$ (sampling time) delay of the computation and PWM, and $G_f(z^{-1})$ is the transfer function of the output filter. A CRC can be plugged into the feedforward channel and its transfer function is given by [16]

$$G_{rc}(z^{-1}) = \frac{U_r(z^{-1})}{E(z^{-1})} = k_r \frac{z^{-N}Q(z^{-1})G_{lf}(z^{-1})}{1 - z^{-N}Q(z^{-1})}. \quad (1)$$

where k_r is the gain of CRC, $G_{lf}(z^{-1})$ is the phase leading element which stabilizes the overall system, $Q(z^{-1}) = a_1 z + a_0 + a_1 z^{-1}$ with $2a_1 + a_0 = 1$ is the low-pass filter which improves the system robustness, $N = f_s/f \in \mathbb{N}$ with f_s and f being the sampling frequency and the fundamental frequency, is the so-called CRC order. It is worthy noting that the poles of CRC are exactly located at $2m\pi f$, with $m \in \mathbb{N}$. Therefore, the magnitudes of CRC at frequencies of $2m\pi f$ approach infinite if $Q(z^{-1}) = 1$, which allows the CRC to provide zero steady-state tracking error of DC, fundamental component and all harmonic components below the Nyquist frequency.

Nevertheless, in a frequency-adaptive ST-fed distribution grid, the frequency of LV side can be modified within a certain range. With a fixed sampling rate, the RC order N would often be a fractional value during frequency changes. A fractional order indicates that a Fractional Delay (FD) appears and it cannot be directly implemented in a digital controller. To address this issue, one solution is to use variable sampling rate while it will significantly increase the real-time implementation complexity [25]. On the other hand, the FORC scheme with a fixed sampling rate has been proposed. The fractional order N can be splitted into a integer order N_i and a small fractional order F, where $N = N_i + F$. The main idea of FORC is to approximate the potential FD z^{-F} by

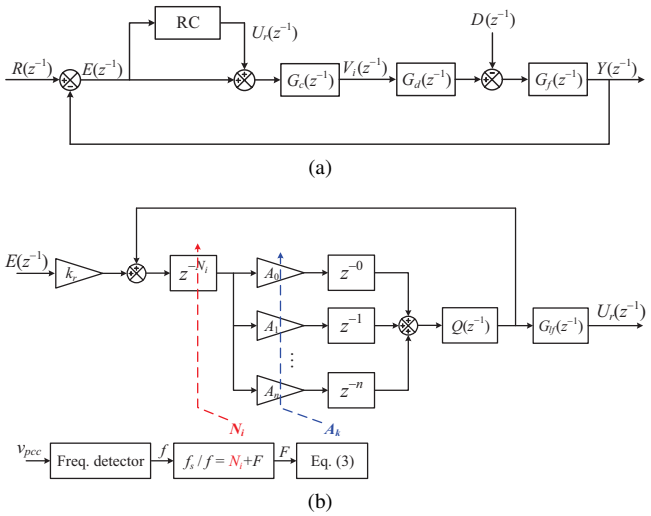


Fig. 4. Block diagrams of a plug-in RC system: (a) overall system and (b) frequency-adaptive FORC.

using the FD design methods [26]. Among these methods, the Lagrange interpolation-based FD design only needs a small number of sums and multiplications and at the same time can provide high approximation accuracy [27]. The FD can be well approximated by a Lagrange interpolation polynomial Finite-Impulse-Response (FIR) filter as follows:

$$z^{-F} \approx \sum_{n}^{k=0} A_k z^{-k}. \tag{2}$$

where $k \in \mathbb{N}$, the Lagrange coefficients A_k of (2) are given by

$$A_k = \prod_{\substack{i=0 \\ i \neq k}}^{n} \frac{F-i}{k-i}. \tag{3}$$

Substituting (2) into (1), the frequency-adaptive FORC will be obtained as

$$G_{forc}(z^{-1}) = \frac{z^{-N_i} \sum_{k=0}^{n} A_k z^{-k} Q(z^{-1})}{1 - z^{-N_i} \sum_{k=0}^{n} A_k z^{-k} Q(z^{-1})} G_{lf}(z^{-1}). \tag{4}$$

The detailed FORC block diagram of (4) is presented in Fig. 4b. It is shown that two time scales have been utilized in the control system: 1) the changing rate of delay orders (N_i and F) is highly dependent on the dynamic response of frequency detector; 2) the update rate of A_k depends on the sampling frequency. In a distribution grid application, the changing rates of both the N_i and F are much slower than the sampling rate. In each sampling interval, the detected frequency as well as N_i and F can be regarded as constant values.

B. Frequency-Adaptive Control Design

As can be seen in Fig. 3, frequency-adaptive control strategy has been implemented in both the ST LV voltage and the DER current control to achieve high performance under variable frequency condition. Fig. 5 depicts the simplified block diagrams of the ST LV side voltage control scheme and the DER current control scheme in the stationary frame.

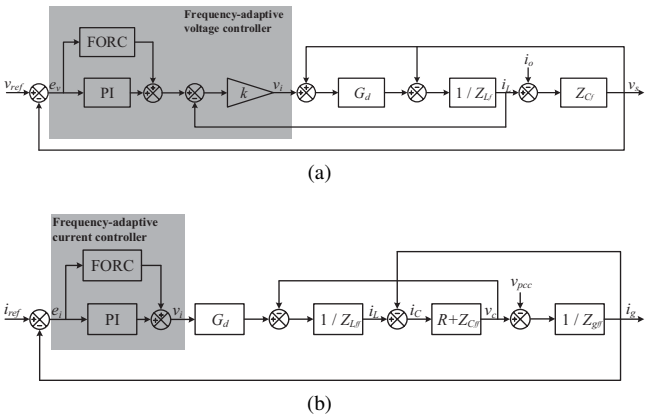


Fig. 5. Block diagrams of frequency-adaptive voltage/current control systems: (a) ST LV side voltage control and (b) DER current control.

The PI-plus-FORC control strategy has been utilized for both control systems to ensure frequency adaptability. It is known that the PI controller under $\alpha\beta$ frame is independent from frequency variation. Using proper gains, the PI-controlled system can offer high stability margin and good transient response. The plug-in FORC controller improves steady-state performance and guarantees zero steady-state error under variable frequency condition.

For the ST LV side voltage control, to alleviate the LC resonance and limit the overcurrent, an inductance current control loop has been used as the inner loop. A proportional gain is employed as the inner loop control since it can effectively increase the damping ratio and limit the current during overcurrent conditions [28]. The PI-plus-FORC control has been applied to the outer voltage loop to meet error-tracking requirements with specific bandwidth. A voltage feed-forward compensation is used to improve the transient response of the overall system. The selection of control bandwidth BW_{st} refers to $BW_{st} < f_s/10$, where f_s is the sampling frequency. Meanwhile, the necessary attenuation at the neighborhood of the LC cut-off frequency should be achieved to damp the filter resonance. Without the FORC, the PI controller decides the control bandwidth as well as phase margin of the overall system. The phase margin is selected between $45°$ and $60°$ according to the usual design rules. The gains of the PI controller for ST voltage control can be determined based on the above-mentioned rules. The open-loop Bode diagrams are presented in Fig. 6a using the system parameters listed in TABLE I. The blue plot represents the open-loop frequency response of the control system without FORC. By using the control parameters of TABLE I, the bandwidth is $267\,Hz$ and the phase margin is $47°$. The frequency response of the control with plugged-in FORC is shown by the red plot, where large magnitudes and zero phase shifts at interested frequencies have been introduced.

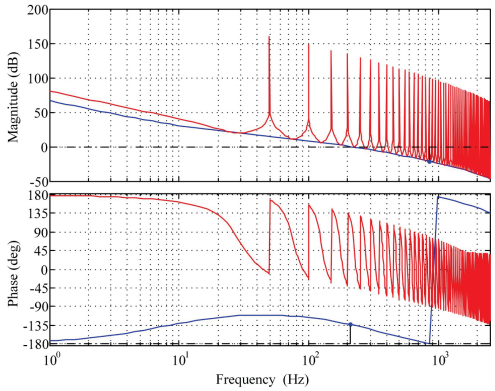
For the DER current control, a passive damping resistor has been employed to alleviate the LCL resonance and the PI-plus-FORC is adopted to deal with the variable frequency current. The design of the PI controller follows the same procedure of voltage control design for the ST LV side inverter. Because of the lack of inner loop, a higher bandwidth between

TABLE I
SYSTEM PARAMETERS OF ST LV CONVERTER

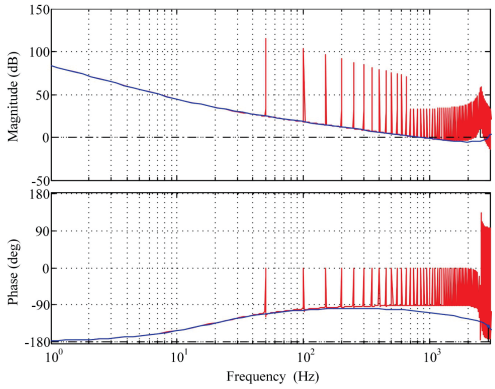
Symbol	Quantity	Value
v_g	LV grid voltage	230 V (RMS)
L_f	inductance of LC filter	2.4 mH
C_f	capacitance of LC filter	8 μF
T_s	sampling frequency	10 kHz
k_{pv}	proportional gain of PI	5e-3
k_{iv}	integral gain of PI	0.25
k	gain of inner loop	10
k_{rv}	gain of FORC controller	0.1

TABLE II
SYSTEM PARAMETERS OF DER GRID INVERTER

Symbol	Quantity	Value
i_{der}	DER nominal current	7.5 A (RMS)
L_{ff}	inverter-side inductance of LCL filter	2.4 mH
C_{ff}	capacitance of LCL filter	1 μF
R_{ff}	damping resistance of LCL filter	2 Ω
L_{gf}	grid-side inductance of LCL filter	0.5 mH
T_c	sampling frequency	10 kHz
k_{pi}	proportional gain of PI	2.5
k_{ii}	integral gain of PI	300
k	gain of inner loop	10
k_{rv}	gain of FORC controller	0.1



(a)



(b)

Fig. 6. Bode diagrams of frequency-adaptive voltage/current control systems: (a) ST LV side voltage control and (b) DER current control.

$f_s/5$ and $f_s/3$ can be selected for PI controller to better reject the grid disturbance and the low-order harmonics. The recommended phase margin is still between $45°$ and $60°$. As a result, the gains of PI controller for DER current control can be designed based on these two rules and listed in Table II. A $1220\,Hz$ bandwidth and $45°$ phase margin system can be obtained. The open-loop Bode diagrams with/without FORC are shown in Fig. 6b. It is seen that the designed PI-plus-FORC current control introduces attenuation at medium/high frequency range and large magnitudes at the frequencies of interest, ensuring low grid current THD.

IV. STABILITY ANALYSIS

A. FORC Stability Conditions

The generic stability conditions of a FORC-controlled system have been given in literature [17]. Before the FORC is added to the system of Fig. **??**, the transfer function of the basic closed-loop system is

$$H(z^{-1}) = \frac{Y(z^{-1})}{R(z^{-1})} = \frac{G_c(z^{-1})G_d(z^{-1})G_f(z^{-1})}{1 + G_c(z^{-1})G_d(z^{-1})G_f(z^{-1})}. \quad (5)$$

Let the open-loop transfer function $G_{op}(z^{-1}) = G_c(z^{-1})G_d(z^{-1})G_f(z^{-1})$. When the FORC is plugged in, the error transfer function of the overall system becomes:

$$\begin{aligned} G_e(z^{-1}) &= \frac{E(z^{-1})}{R(z^{-1}) - D(z^{-1})} \\ &= \frac{(1 - z^{-N_i}\sum_{k=0}^{n} A_k z^{-k})(1 + G_{op}(z^{-1}))^{-1}}{1 - z^{-N_i}\sum_{k=0}^{n} A_k z^{-k} Q(z^{-1})(1 - k_r G_{lf}(z^{-1})H(z^{-1}))}. \end{aligned} \quad (6)$$

Based on the error transfer function of (6), two generic stability conditions can be obtained. A FORC-controlled system is asymptotically stable if the following two conditions hold: 1) the roots of $1 + G_{op}(z^{-1}) = 0$ are inside the unity circle; 2) the roots of $1 - z^{-N_i}\sum_{k=0}^{n} A_k z^{-k} Q(z^{-1})(1 - k_r G_{lf}(z^{-1})H(z^{-1})) = 0$ are inside the unity circle.

$$\left|1 - k_r G_{lf}(z^{-1})H(z^{-1})\right| < \left|Q(z^{-1})\sum_{k=0}^{n} A_k z^{-k}\right|^{-1}. \quad (7)$$

It is worth noticing that the magnitudes of the Lagrange interpolation polynomial are always less than or close to 1 (abs) within the Nyquist frequency. The inequality of (7) can be simplified in practical case study:

$$\begin{aligned} \left|1 - k_r G_{lf}(z^{-1})H(z^{-1})\right| &< \left|Q(z^{-1})\right|^{-1} \left|\sum_{k=0}^{n} A_k z^{-k}\right|^{-1} \\ &< \left|Q(z^{-1})\right|^{-1}. \end{aligned} \quad (8)$$

Then, (8) yields

$$0 < k_r < \frac{1 + \left|Q(z^{-1})\right|}{\left|Q(z^{-1})\right| \left|G_{lf}(z^{-1})H(z^{-1})\right|}. \tag{9}$$

If (9) is satisfied and provided the basic closed-loop system $H(z^{-1})$ is asymptotically stable, a stable FORC-controlled system can be achieved.

From (8), it is observed that the gain of FORC controller would be restricted by the norm of the low-pass filter. As indicated in [20] that the Lagrange interpolation polynomial behaves like a low-pass filter when lower degree ($n \leq 3$) is used. With this consideration, the low-pass filter $Q(z^{-1})$ can be removed while the stability conditions can still be fulfilled. For instance, if the cut-off frequency of the proposed polynomial FD filter is less than that of $Q(z^{-1})$, (8) turns out to be

$$\begin{aligned}\left|1 - k_r G_{lf}(z^{-1})H(z^{-1})\right| &< \left|Q(z^{-1})\right|^{-1} \left|\sum_{k=0}^{n} A_k z^{-k}\right|^{-1} \\ &< \left|\sum_{k=0}^{n} A_k z^{-k}\right|^{-1}.\end{aligned} \tag{10}$$

indicating $Q(z^{-1})$ can be omitted while the stability conditions are still fulfilled with the pre-designed k_r. In some practical cases, it can save the design of the low-pass filter for the system and avoid additional phase shift which is introduced by the low-pass filter.

B. System Stability Considering the Synchronization

The impact of synchronization on the stability of FORC-controlled system has seldom been considered. However, as pointed out by [29] and [30], the utilization of synchronization (e.g. SOGI-PLL) in current-controlled inverter could lead to stability issues especially in a weak grid. As a result, the characteristics of PLL must be taken into account for the stability of the control of the DER inverter.

The schematic diagram of Fig. 4a in each frame can be updated and is shown in Fig. 7, where a PLL is considered: the input signal I_{ref} is the amplitude of the current reference, v_{pcc} is the PCC voltage.

Considering that the proportional gain k_{pi} of the PI controller mainly determines the stability margin, the root loci of the DER inverter control with the variation of k_{pi} are shown in Fig. 8. In Fig. 8a, the root locus of the original current feedback system in the gray box of Fig. 7 is plotted, while the root locus of the overall system (considering the synchronization in the blue dash box) is plotted in Fig. 8b. It is observed that the control system considering PLL introduces additional poles in the low-frequency range, which lead to a smaller gain range, compared to the original current feedback system. As a result, the effects of the synchronization are likely to compromise the system stability.

With this consideration, the closed-loop transfer function $H(z^{-1})$ has to be reconsidered, since an asymptotically stable

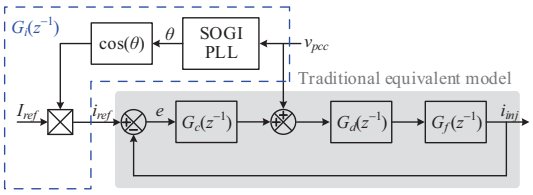
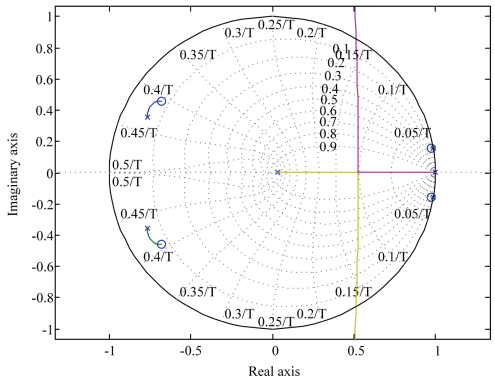
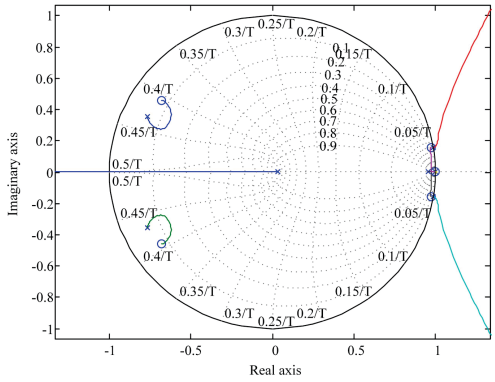


Fig. 7. Simplified block diagram of a grid-interfaced inverter for DER.



(a)



(b)

Fig. 8. Root locus of the overall system when k_{pi} changes: (a) with only current feedback control and (b) considering the PLL.

system should be achieved before the FORC is plugged in. In the system of Fig.7, $H(z^{-1})$ can be updated by

$$H(z^{-1}) = \frac{G_i(z^{-1})G_{op}(z^{-1}) - G_d(z^{-1})G_f(z^{-1})}{1 + G_{op}(z^{-1})}. \tag{11}$$

where $G_i(z^{-1})$ is the transfer function of PLL as well as current reference generator, and thus the stability condition should be evaluated by using the updated $H(z^{-1})$ that considers the synchronization. Accordingly, the range of the k_r would be limited depending on the characteristics of PLL.

On the other hand, the participation of the frequency-adaptive control of local DERs requires updating online the frequency, which ensuring the accuracy of the Lagrange coefficients. Nevertheless, the intrinsic delay of frequency detection of PLL (the delay between the actual frequency and the detected frequency) has an influence on the FORC-controlled system. The frequency delay is dependent on the dynamic response of PLL (e.g. rising time and settling time). For

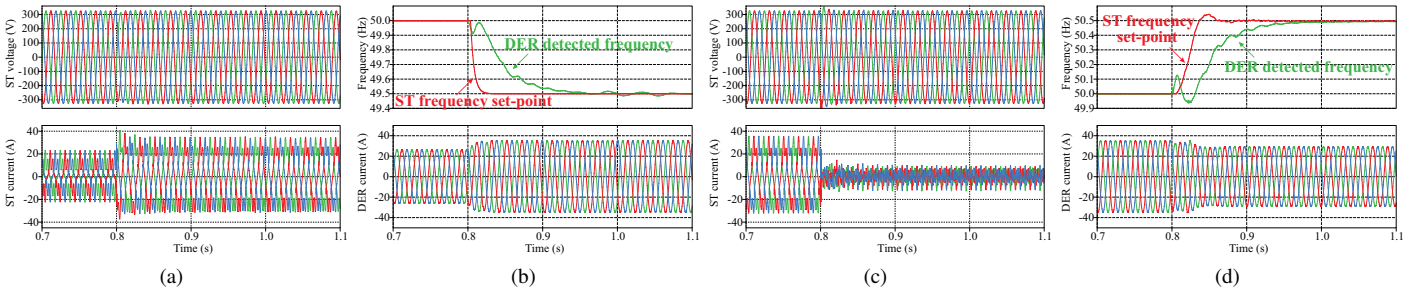


Fig. 9. Performance evaluation of frequency-adaptive ST-fed grid under two scenarios (overloading, reverse power flow): (a) ST voltage (top) and current (bottom) under overloading scenario, (b) DER detected frequency (top green), ST frequency set-point (top red) and DER output current (bottom) under overloading scenario, (c) ST voltage (top) and current (bottom) under reverse power flow scenario, and (d) DER detected frequency (top green), ST frequency set-point (top red) and DER output current (bottom) under reverse power flow scenario.

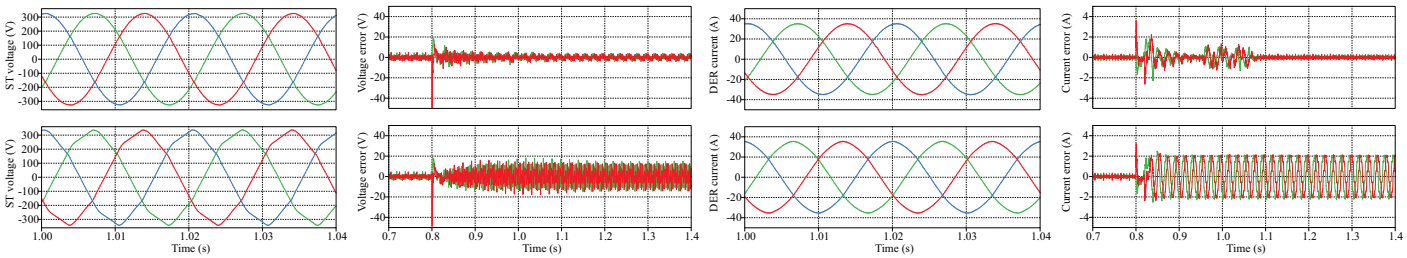


Fig. 10. Performance comparisons of two different control strategies (FORC, CRC) under overloading scenario: (a) zoomed ST voltages at 49.5 Hz by using FORC (top) and CRC (bottom), (b) voltage control errors by using FORC (top) and using CRC (bottom), (c) zoomed DER currents at 49.5 Hz by using FORC (top) and CRC (bottom), and (d) current control errors by using FORC (top) and using CRC (bottom).

analysis simplicity, a N_2 steps delay z^{-N_2} has been employed to represent the frequency delay, so that the transfer function of the Lagrange interpolation polynomial FIR becomes

$$Y_f(z^{-1}) = z^{-N_2} \sum_{k=0}^{n} A_k(z^{-1}) z^{-k}. \tag{12}$$

Substituting (12) into (7), it is seen that the form of the second condition remains the same. This indicates that the FORC-controlled system is not sensitive to the frequency delay as long as the first stability condition is fulfilled. For a slow PLL with longer settling time, if the control system is stable before the FORC is plugged in, the delay of frequency can barely jeopardize the system stability after FORC is applied. However, the control accuracy does rely on the accuracy of the frequency detection. The delay of frequency can shift the large magnitudes away from the actual frequencies of interested and thus deteriorate the control performance. As a result, synchronization with the capabilities of real-time measurement and frequency adaptivity is crucial to the performance of the frequency-adaptive distribution grid. A set of frequency-adaptive synchronization algorithms were proposed in literature [31], [32], [33], allowing the grid-interfaced converters to fast and accurately detect the phase sequencing under variable frequency condition. In the frequency control scenarios, a combination between these frequency-adaptive synchronization and the FORC could be a promising candidate that provides higher power quality and reduced power oscillation.

V. Simulation and Experimental Verification

A. Simulation Results

To validate the proposed frequency-adaptive control strategy, it has been simulated in a ST-fed distribution grid of Fig. 3 in MATLAB/Simulink with PLECS toolbox. Two case studies are investigated in the following section: the frequency-based overloading scenario [10] and the frequency-based reverse power flow scenario [9]. The system parameters listed in Table I and Table II have been utilized for the simulations. In both case studies, the frequency range of the ST-fed distribution grid is defined as 49-51 Hz.

In the overloading scenario, the security limit of ST LV current is 25 A (RMS). The DER is assumed to operate at unity Power Factor (PF) with 17 kW nominal power. Initially, the overall system operates at 50 Hz, the power rating of the DER is 12.8 kW at the nominal frequency, a 15.9 kVA (PF$=0.9$) linear load and a 6.1 kVA nonlinear load are connected to the grid. At $t = 0.8$ s, the load increases from 22 kVA to 32.6 kVA. As soon as the current of ST LV side exceeds the security limit, the frequency-based overloading control of ST is activated. As shown in Fig. 9a, when the load increases at $t = 0.8$ s, the ST LV side current increases as well and activates the frequency control. The ST current decreases till below the security limit and reaches its new equilibrium by means of the frequency control. The voltage amplitude remains constant and it regains the nominal value in less than one cycle after the application of the frequency change. The DER behavior during the frequency control is shown in Fig. 9b. A SOGI-PLL is utilized as the synchronization

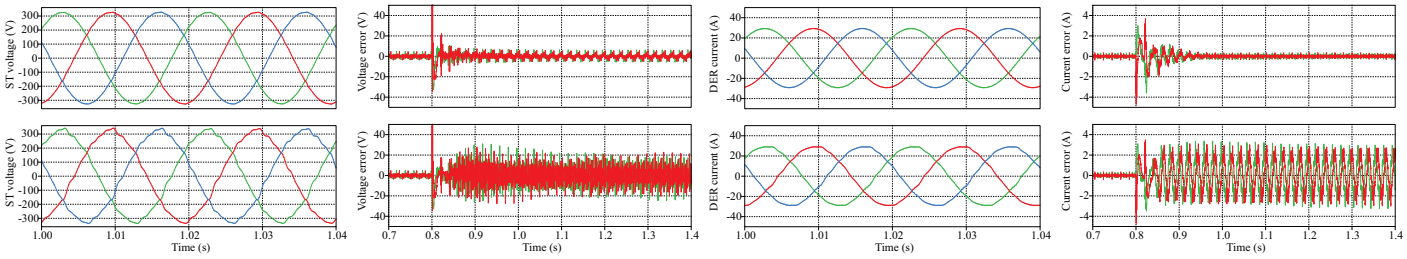


Fig. 11. Performance comparisons of two different control strategies (FORC, CRC) under reverse power flow scenario: (a) zoomed ST voltages at 50.5 Hz by using FORC (top) and CRC (bottom), (b) voltage control errors by using FORC (top) and using CRC (bottom), (c) zoomed DER currents at 50.5 Hz by using FORC (top) and CRC (bottom), and (d) current control errors by using FORC (top) and using CRC (bottom).

element, and a comparison between the detected frequency and the ST frequency set-point is presented, showing a fast and accurately tracking of the frequency with a delay inferior to two cycles (40 ms). Following the frequency change, the DER proportionally increases its power generation according to the given P-f droop curve. A new power equilibrium is established and the frequency holds the line of 49.5 Hz.

In the reverse power flow scenario, the overall load consumption is 32.6 kVA and the DER is operated initially at the nominal power. At $t = 0.8$ s, the load demand decreases from 32.6 kVA to 16.7 kVA. As a result, a reverse power flow occurs shown in Fig. 9c, the frequency-based reverse power flow control of ST is activated. The ST LV side frequency increases until the power flow direction is changed and a new equilibrium is reached. The voltage amplitude remains constant and it regains the nominal value in less than one cycle after the frequency change. The DER behavior during the frequency control is shown in Fig. 9d. The frequency detected by the SOGI-PLL can well follow the ST frequency change. Following the frequency change, the DER proportionally decreases its power generation according to the given P-f droop curve. A new power equilibrium is established and the frequency holds the line of 50.5 Hz.

The effectiveness of the proposed frequency-adaptive control strategy is verified in both scenarios as follows. Comparisons of ST voltage control and DER current control by using CRC and FORC schemes during the frequency control are presented in Fig. 10 and Fig. 11. In the overloading scenario (Fig. 10), it is seen that both the ST LV side voltage and the DER output current are well controlled by using FORC-based frequency-adaptive control, providing satisfactory performance even during the frequency control, while the CRC-controlled systems present considerable control errors when frequency deviates from the nominal value, leading to worse voltage and current waveforms. Similarly, in the reverse power flow scenario (Fig. 11), the FORC-based frequency-adaptive control offers better accuracy compared to the CRC-based control in terms of waveform and control error. Generally speaking, the FORC-based control is adaptive to the frequency variation, whereas the CRC-based control is not.

Fig. 12. Experimental setup.

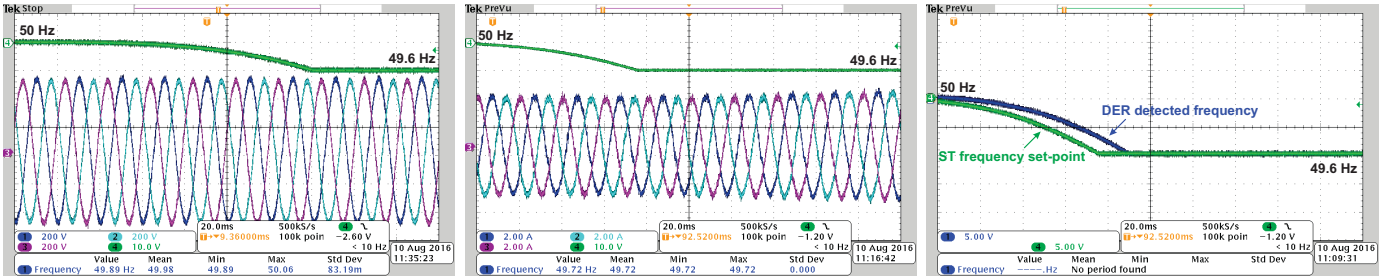
TABLE III
SETUP PARAMETERS

Symbol	Quantity	Value
f_c	switching frequency	10 kHz
V_{dc}	DC-link voltage	650 V
v_n	rated voltage of inverters	3×380 V (RMS)
S_n	rated power of inverters	4 kW

B. Experimental Results

In the following section, the effectiveness of the frequency-adaptive control in a ST-fed grid has been experimentally validated. The experimental setup is shown in Fig. 12, where two Danfoss FC-302 inverters have been used, one for the LV side inverter of ST, another for the grid-interfaced inverter of DER: a dSPACE 1006 has been utilized to control both inverters. The system configuration of the experimental setup is same to that of Fig. 3. A 3.75 kW linear load and 1.12 kVA nonlinear load have been connected into the grid. The detailed parameters of the overall system are listed in TABLE III. The system parameters listed in TABLE I and TABLE II are used for the control systems and the output filters of both inverters.

Firstly, the distribution grid initially works under nominal

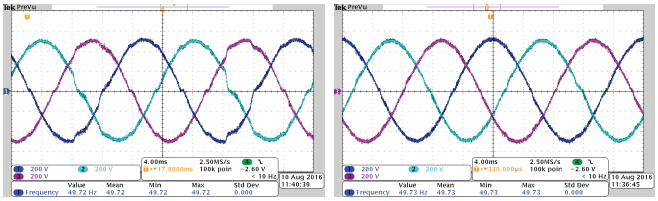


(a) (b) (c)

Fig. 13. Voltage and current waveforms of a ST-fed distribution grid during overloading condition (time: 20 ms/div, voltage: 200 V/div, current: 2 A/div): (a) ST LV side frequency (top green) and ST LV side voltage (bottom), (b) DER detected frequency (top green) and DER output current (bottom), and (c) ST frequency set-point (green) and DER detected frequency (blue).

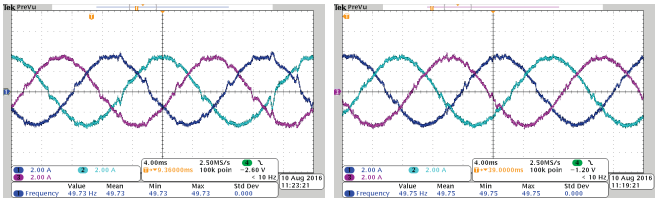
condition (50 Hz), with the above-mentioned linear load. Then, the nonlinear load connects to the ST-fed grid, leading to a higher loading. The frequency control is activated when the ST current exceeds its security limit. In order to alleviate the overloading issue, the frequency gradually decreases from 50 Hz to 49.6 Hz so that the DER production increases and the load consumption decreases. A new power balance is eventually reached at 49.6 Hz. The ST LV side voltage waveform and its frequency set-point during frequency control are shown in Fig. 13a. The DER output current and the detected frequency during frequency control are shown in Fig. 13b. It is shown that the voltage amplitude stays constant and the power quality is ensured during both the steady-state and the transient stage. The current amplitude linearly increases according to the droop curve of the DER. To guarantee accurate frequency detection, the SOGI-PLL has been adopted in the DER for grid synchronization. The comparison between the ST frequency set-point and the detected frequency via SOGI-PLL is shown in Fig. 13c. It is seen that the frequency detected by the PLL can timely follow the ST frequency with less than 10 ms delay, offering good performance during frequency control stage.

Following, the zoomed voltage and current waveforms in a ST-fed grid during frequency control stage by using different control strategies are compared. In Fig. 14a and Fig. 15a, the CRC scheme has been employed for both the ST voltage control and the DER current control. It is seen that both the ST LV side voltage and DER output current are distorted during frequency control (e.g. 49.7 Hz). When the proposed FORC-based voltage and current control are used, the ST LV side voltage and DER output current are shown in Fig. 14b and Fig. 15b, with less harmonic distortion. More details of the performance comparison have been listed in TABLE IV. The case study shows that CRC is sensitive to grid frequency variation in terms of THD and amplitude, whereas FORC is not. By using the proposed frequency-adaptive control, the ST-fed distribution grid can provide satisfactory performance in terms of control accuracy and power quality.



(a) (b)

Fig. 14. Comparison of ST LV side voltages with different control strategies during overloading condition ((time: 20 ms/div, voltage: 200 V/div): (a) CRC-controlled ST LV side voltage and (b) FORC-controlled ST LV side voltage.



(a) (b)

Fig. 15. Comparison of DER currents with different control strategies during overloading condition ((time: 20 ms/div, current: 2 A/div): (a) CRC-controlled DER current and (b) FORC-controlled DER current.

TABLE IV
PERFORMANCE COMPARISON OF CRC- AND FORC-CONTROLLED SYSTEMS

Control	Frequency	Voltage	Current	THD_V	THD_I
CRC	$50\,Hz$	$0.987\,p.u.$	$0.987\,p.u.$	2.90 %	3.76 %
	$49.8\,Hz$	$0.967\,p.u.$	$0.938\,p.u.$	6.54 %	6.97 %
	$49.6\,Hz$	$0.959\,p.u.$	$0.917\,p.u.$	7.21 %	8.36 %
FORC	$49.8\,Hz$	$0.981\,p.u.$	$0.975\,p.u.$	3.12 %	4.21 %
	$49.6\,Hz$	$0.979\,p.u.$	$0.958\,p.u.$	3.35 %	4.69 %

VI. CONCLUSION

This paper proposes a frequency-adaptive ST-fed distribution grid. In the proposed scenarios, the ST is able to flexibly modify the LV side frequency with the purposes of achieving power sharing among different DERs and establishing power balance between production and consumption. In this way, the overload and reverse power flow issues can be largely avoided and therefore the power rating of controllable load or storage can be reduced. Differently from the existing control schemes, the proposed FORC scheme ensures better performance of the ST and the grid-interfaced DER in the distribution grid under

variable frequency condition. Comprehensive control design and stability analysis considering delay and PLL are presented in this paper. Case studies of the proposed frequency-adaptive ST-fed distribution grid are performed in both the simulation and experimental platform. The results prove the power sharing ability of frequency-adaptive ST-fed distribution grid and the effectiveness of the proposed control strategies under variable frequency condition.

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