

© 2016 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

Digital Object Identifier (DOI): 10.1109/TPEL.2018.2799680

IEEE Transactions on Power Electronics

Optimum Design of a Multiple-Active-Bridge DC-DC Converter for Smart Transformer

Levy Ferreira Costa

Giampaolo Buticchi

Marco Liserre

Suggested Citation

L. Costa, G. Buticchi and M. Liserre, "Optimum Design of a Multiple-Active-Bridge DC-DC Converter for Smart Transformer," in IEEE Transactions on Power Electronics, vol. PP, no. 99, pp. 1-1.

Optimum Design of a Multiple-Active-Bridge DC-DC Converter for Smart Transformer

Levy Costa, *Student Member, IEEE*, Giampaolo Buticchi, *Member, IEEE*, and Marco Liserre, *Fellow, IEEE*

Abstract—The modular Smart Transformer (ST) is composed by several basic converters rated for lower voltage and power. In this paper the quadruple active bridge (QAB) is used as the basic block for the modular ST. In this application, the efficiency and cost are the most important design parameters. Therefore, the paper focus on the design of the converter, with the aim to optimize its efficiency, taking the cost into consideration. To do so, the losses of all components are carefully modeled and a computer-aided design is used, where an algorithm to calculate the losses and cost is developed, allowing to perform multi-objective optimization. Additionally, Silicon IGBTs and Silicon Carbide MOSFETs are considered for the design and the performance of the converter using both semiconductors technology is compared. Experimental results obtained for the optimized 20 kW QAB converter has shown an efficiency of 97.5%.

Index Terms—Dc-dc converter, reliability, high efficiency, silicon-carbide devices, smart transformer.

I. INTRODUCTION

Over the past years, many researches have been focused on efficiency improvement of dc-dc converters and several design optimization methods and power converter topologies have been discussed [1]–[9]. Among the most investigated topologies, the Dual Active Bridge (DAB) converter [10], composed of two active bridges connected through a high frequency transformer, is highlighted as a high performance solution, because of its soft-switching feature and high power density. Therefore, this converter has been widely used in application with different power and voltage levels, mainly those that required high efficiency.

In Smart Transformer (ST) application, the DAB converter became a standard solution for the dc-dc stage, mainly because of its simple power flow control [1]. However, not only the efficiency, but also the cost plays a very important role during the design and the topologies choice for the system implementation. Recent investigations have shown the economic advantages of the Multiple Active Bridge (MAB) over the DAB, when applied to ST [11], [12]. The MAB is an extension of the DAB converter, where more bridges are coupled to the same multiwinding high frequency transformer (HFT). Consequently, employing the MAB instead the DAB in ST, the total number of HFT, LV cells, as well as auxiliary components (communication system and auxiliary power supply) are reduced, resulting in lower cost. In addition to that, the MAB

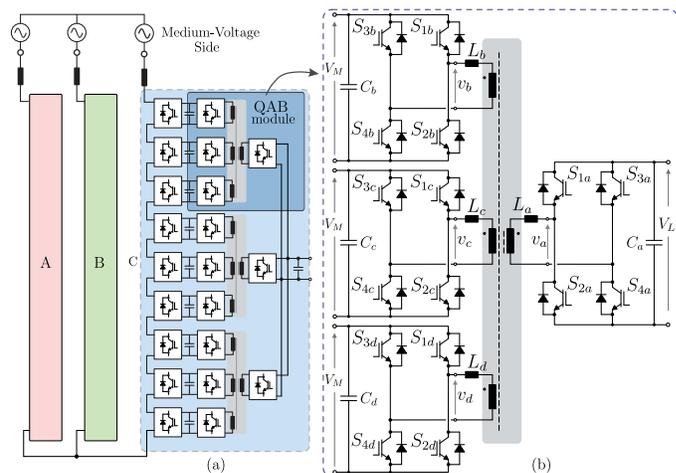


Figure 1. (a) Modular ST architecture using the QAB converter as a basic module of the dc-dc stage. (b) QAB converter topology.

operates similarly to the DAB, preserving the same advantages and then high performance is also expected.

On the other hand, most of the publications related to this converter were focused on the power control between the bridges, and little attention was paid to the design and efficiency improvement. In [13], the design of a MAB converter based on three active bridges (TAB) is presented, but a peak efficiency of only 91.5% was obtained for the built converter. Similarly, a MAB converter is designed and implemented in [14], [15], where a maximum efficiency of 92% is reported. The high performance of the MAB converter has not yet been demonstrated in literature.

In this context, this paper presents the design of a MAB converters, with the aim to optimize the efficiency, but considering the cost of the converter. To do so, a computer-aided design is used, where the parameters are properly selected and the losses on the main power components are carefully calculated. Additionally, Silicon IGBTs (Si-IGBT) and Silicon Carbide MOSFETs (SiC-MOSFETS) are considered in the design, in order to reduce the switching and conduction losses and verify the performance of the converter using different semiconductors technology. Furthermore, the cost of the components are considered, allowing to perform a multi-objective (efficiency and cost) optimization.

The economical advantages of the MAB in ST application was proved in [12], and the main goal of this paper is to validate theoretically and experimentally its high performance in terms of efficiency, demonstrating the feasibility of the MAB in this application.

Manuscript received November 1, 2017; revised January, 2017. The research leading to these results has received funding from the European Research Council under the European Union's Seventh Framework Programme (FP/2007-2013) / ERC Grant Agreement n. [616344] - HEART.

The authors are with the Christian-Albrecht-University of Kiel, Germany.

The paper is divided as follows: in section II, the ST concept is briefly introduced, where its characteristics and requirements used for the MAB designed is presented. Then, the MAB converter is introduced in Section III, where its main equations used on the design are provided. In section IV, the design methodology is presented, where the components are selected, the losses are calculated and theoretical efficiency is estimated. Finally, experiments results for building prototype is presented, where an efficiency of 97.5% is demonstrated.

II. MODULAR SMART TRANSFORMER ARCHITECTURE

Smart Transformer (ST) is a power electronics-based system usually composed of three conversion stages (AC-DC, DC-DC and DC-AC) with advanced control and communication functionality [1], [2]. Because of its high control performance, it became a promising system to solve the current problems of the modern distribution system, and its advantages and benefits in distribution system have been discussed in [1], [2]. Different architectures can be used to implement the ST [1], but the modular one has shown more advantages, because it enables the fault tolerance. Using this approach, the dc-dc stage is composed by several basic dc-dc converters rated for low power and low voltage. In this work, the MAB converter is employed as a basic cell, where four bridges (named quadruple active bridge - QAB) are used, as shown in Fig. 1. This converter was employed in ST application in [16], focusing on the comparison of different modulation strategies. This study has shown that the QAB converter presents higher performance when the Phase Shift Modulation (PSM) scheme is used. On the other hand, only an initial studies was presented in [16], without substantial results. In this context, the current work focus on the optimum multi-objective design of the QAB converter, with the aim to maximize efficiency and minimize cost.

The general block diagram of the MAB is shown in Fig. 2 (a), where the MV cells and LV cells are highlighted. The number of MV cells ($N_{MV(cell)}$) and LV cells ($N_{LV(cell)}$) of the MAB converter can be freely determined and when $N_{MV(cell)} = N_{LV(cell)}$ the converter is symmetrically configured and the power of the individual cells are equal. This example is depicted in Fig. 2 (b) for the QAB converter, in which $N_{MV(cell)} = N_{LV(cell)} = 2$. When $N_{MV(cell)} \neq N_{LV(cell)}$, on the other hand, the converter is then configured asymmetrically and the power rating of the MV cells differs from the power level of the LV cells. This case is exemplified in Fig. 2 (c), in which $N_{MV(cell)} = 3$, $N_{LV(cell)} = 1$ and the power level of the MV cells is given by $P_{QAB}/N_{MV(cell)}$, while the power rating of the LV cells is $P_{QAB}/N_{LV(cell)}$, where P_{QAB} is the total power of the converter. Consequently, the number of MV cells and LV cells must be defined, before to analyze and design the converter.

According to [12], if properly designed, the MAB converter should perform similarly regardless the number of cells, implying in equivalent efficiency. However, the cost is highly affected by the number of cells and reducing them implies in cost saving. Still according to [12], it is very advantageous to select three bridges on the MV side and one on the LV side

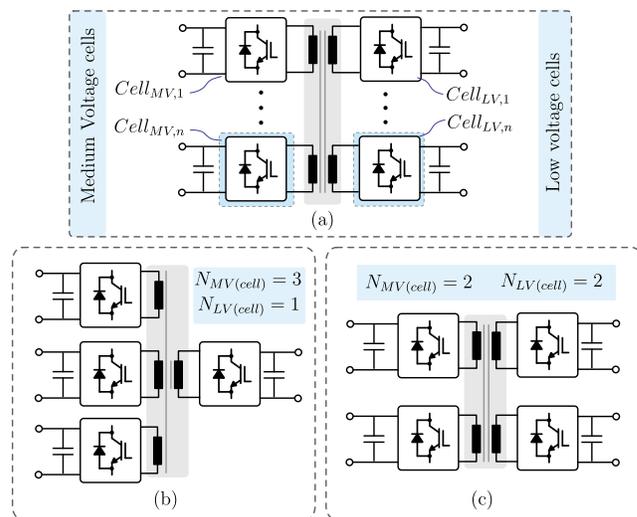


Figure 2. Block diagram of the MAB converter: (a) generalized MAB converter, (b) asymmetrical configuration, (c) asymmetrical configuration of the QAB converter.

Table I
SPECIFICATION OF THE GRID AND QAB CONVERTER

Rated Power	MVAC	LVAC	Grid frequency
500 kVA	10 kV	400 V	50 Hz
QAB Converter Specification			
Rated Power	Input Voltage	Output Voltage	Switching freq.
20 kW	800 V	700 V	20 kHz

(see. Fig. 1), because the total number of HFT and LV cells are reduced, while the semiconductors with lower blocking voltage can be used in the MV cells [12]. For this reason the QAB converter with $N_{MV(cell)} = 3$ and $N_{LV(cell)} = 1$ is adopted.

A typical ST specification for distribution system is presented in Table I, as well as the specification of the QAB converter, and the QAB converter design is carried out based on these specifications.

III. OPERATION PRINCIPLE OF THE MAB CONVERTER

The QAB is composed of four active bridges and for the analysis, each of them is denoted by the letters a , b , c and d . The elements of the bridges have sub-index $i = \{a, b, c, d\}$ to indicate the bridge the element belongs to. Fig. 3 (b) shows the block diagram of the converter, where the main parameters (voltage, current and inductance) of each bridge are illustrated with its respective sub-index. To analyze the converter, an equivalent circuit based on the Y-model and depicted in Fig. 3 (b) is used, in which the bridges are replaced by rectangular voltage sources (v_a , v_b , v_c and v_d). The parameters of the equivalent circuit shown in Fig. 3 (b) are reflected to the LV side and they are determined using the original parameters shown in Fig. 1 and the transformer turns ratio n . The reflected parameters of the equivalent circuit are calculated by (1), where n is the number of turns of the LV side in relation to the MV side, i.e. $n = n_{LV}/n_{MV}$.

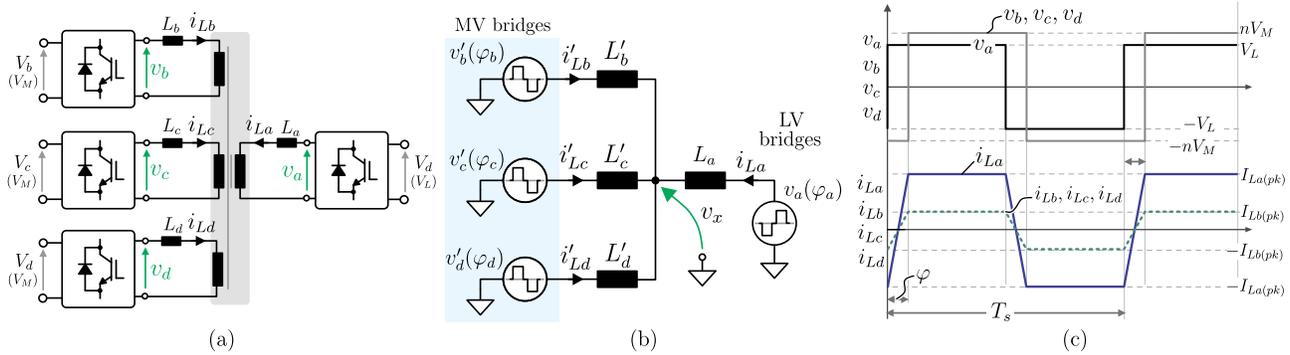


Figure 3. Model of the QAB converter and main waveforms of the QAB converter using the PSM.

$$\begin{cases} v'_b = \frac{v_b}{n} & i'_b = i_b n & L'_b = \frac{L_b}{n^2} \\ v'_c = \frac{v_c}{n} & i'_c = i_c n & L'_c = \frac{L_c}{n^2} \\ v'_d = \frac{v_d}{n} & i'_d = i_d n & L'_d = \frac{L_d}{n^2} \end{cases} \quad (1)$$

The voltage at the central point v_x and the current slope of each inductor are given by (2) and (3), respectively, where $k = \{a, b, c, d\}$.

To modulate the converter, the Phase-Shift Modulation (PSM) strategy is employed. Using this modulation scheme, rectangular voltages v_a, v_b, v_c and v_d with phase shift $\varphi_a, \varphi_b, \varphi_c$ and φ_d , respectively, and constant switching frequency f_s are applied to the transformer. The power is controlled by the phase difference among the bridges and it can be generally described in (4), where, $i = a, b, c, d$ and $k = a, b, c, d$, according to [17], [18]. The main waveform of the PSM is shown in Fig. 3 (c).

$$v_x = \frac{v_a + v_b + v_c + v_d}{4} \quad (2)$$

$$\frac{di_{Lk}}{dt} = \frac{(v_k - v_x)}{L_{eq}} \quad (3)$$

$$P_{ik} = \frac{V_i V_k}{2\pi f_s L_{eq} n} \varphi_{ik} \left(1 - \frac{|\varphi_{ik}|}{\pi} \right), \varphi_{ik} = \varphi_i - \varphi_k \quad (4)$$

The PSM is characterized by ZVS turn-on, but this features depends on the input and output voltages relation and also on the load. In this application, the input voltage of the QAB (all the three cells) is regulated by the first stage of the ST, i.e. the MV rectifier, while the QAB controls the output voltage. As the input and output voltage are considered constant, the converter can be properly designed to work with ZVS operation for its entire range of operation. Consequently, this scheme offers several advantages for the converter operation.

In ST application, equal power sharing is normally assumed (i.e. power balanced condition), and the MV cells operate with the same phase shift angle. In this condition, there is no circulating power among the MV cells, but only power exchange between the MV and LV sides. Consequently, the

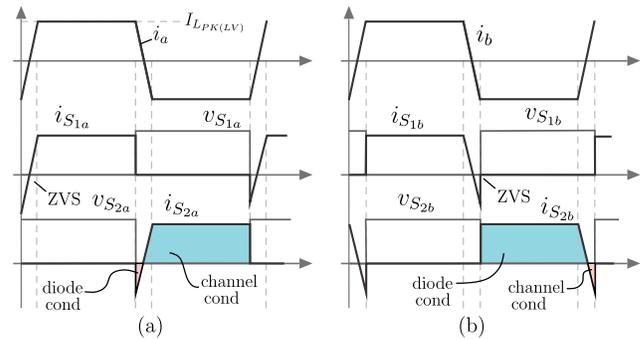


Figure 4. Current and voltage waveforms on the (a) LV side semiconductors ($i_{S1a}, v_{S1a}, i_{S2a}, v_{S2a}$) and (b) MV semiconductors ($i_{S1b}, v_{S1b}, i_{S2b}, v_{S2b}$) of the QAB converter. Diode and channel refer to the power device (MOSFET and/or IGBT).

equation (4) can be simplified to (5), where φ is the phase-shift angle between the MV cells and LV cell.

$$P_o = \frac{V_M V_L}{2\pi f_s n L_{eq}} \varphi_{nom} \left(1 - \frac{|\varphi_{nom}|}{\pi} \right) \quad (5)$$

In this equation, L_{eq} is the equivalent inductance seen by the LV side, and it can be calculated in terms of the LV inductance and MV inductance by equation (6). Assuming a nominal power, nominal phase-shift angle and voltage, the required equivalent inductance can be calculated then by (7). This can be implemented physically on the MV side and/or LV side, but the relation shown in (6) must be satisfied.

$$L_{eq} = L_a + \frac{L_b + L_c + L_d}{3n^2} \quad (6)$$

$$L_{eq} = \frac{V_M V_L}{2\pi f_s n P_o} \varphi_{nom} \left(1 - \frac{|\varphi_{nom}|}{\pi} \right) \quad (7)$$

As can be noticed in (5), the input and output voltages are constant, as well as the switching frequency (f_s); hence, the power transference depends only the equivalent inductance and the nominal phase-shift angle. The choice of the nominal phase-shift is critical and further discussion is presented as follows.

The voltage and current waveforms on the semiconductor of the MV side bridge and LV bridge of the QAB converter are depicted in Fig. 4. If properly designed, the current and voltage

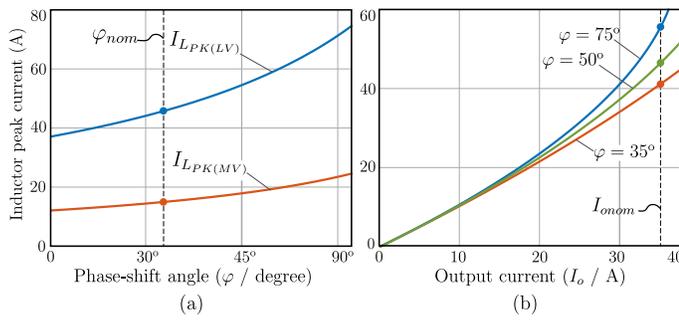


Figure 5. (a) The peak current on the LV inductor and MV inductor in function of the nominal designed phase-shift angle and (b) the same current in function of the output current, for different designed phase-shift angle.

waveforms on the semiconductors will be same as depicted in Fig. 4. In this figure, the peak current on the LV side inductor ($I_{LPK(LV)}$) is calculated by (8).

$$I_{LPK(LV)} = \frac{V_L - \sqrt{V_L^2 - 8L_{eq}f_s n V_L I_o}}{4L_{eq}f_s} \quad (8)$$

$$i_{S1a,rms} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_{S1a}^2(t) dt} \quad (9)$$

$$i_{S1a,avg} = \frac{1}{T_s} \int_0^{T_s} i_{S1a}(t) dt \quad (10)$$

Fig. 5 (a) shows the variation of the peak current on the LV and MV side inductors, according to the nominal phase shift angle chosen on the design, while the Fig. 5 (b) shows the variation of the same current in function of the load for different designed φ . As can be noticed, higher φ implies in higher peak current, and consequently rms current and losses on the semiconductors, inductors and transformer. It means, more reactive power flowing on the converter [10]. Then, a range between 30 degrees and 50 degrees is desired and in this work $\varphi_{nom} = 35^\circ$ is selected.

To calculate the current effort and consequently the losses on the semiconductors and transformer the equations (9) and (10) are used, considering the current waveforms presented in Fig. 4 and positive power flow, i.e. from MV to LV side. As a result, the average and rms current on the semiconductor of the MV cell are calculated by (11) to (14).

$$i_{D1b(avg)} = \frac{I_{LPK(LV)} \varphi}{3n \cdot 8\pi} \quad (11)$$

$$i_{D1b(rms)} = \frac{I_{LPK(LV)}}{3n} \sqrt{\frac{\varphi}{12\pi}} \quad (12)$$

$$i_{S1b(avg)} = \frac{I_{LPK(LV)}}{6n} \left(1 - \frac{3\varphi}{4\pi}\right) \quad (13)$$

$$i_{S1b(rms)} = \frac{I_{LPK(LV)}}{3n} \sqrt{\frac{1}{2} \left(1 - \frac{5\varphi}{12\pi}\right)} \quad (14)$$

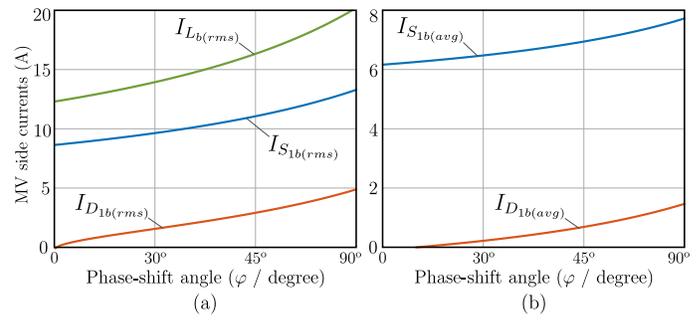


Figure 6. The (a) rms and (b) average currents on the MV side in function of the nominal designed phase-shift angle.

Similarly, the average and rms currents on the semiconductor of the LV cell are calculated by (15) to (18).

$$i_{D1a(avg)} = \frac{I_{LPK(LV)}}{2} \left(1 - \frac{3\varphi}{4\pi}\right) \quad (15)$$

$$i_{D1a(rms)} = I_{LPK(LV)} \sqrt{\frac{1}{2} \left(1 - \frac{5\varphi}{12\pi}\right)} \quad (16)$$

$$i_{S1a(avg)} = I_{LPK(LV)} \frac{\varphi}{8\pi} \quad (17)$$

$$i_{S1a(rms)} = I_{LPK(LV)} \sqrt{\frac{\varphi}{12\pi}} \quad (18)$$

The rms current on the MV and LV inductors are calculated by

$$i_{L1a(rms)} = I_{LPK(LV)} \sqrt{1 - \frac{2\varphi}{3\pi}} \quad (19)$$

$$i_{L1b(rms)} = \frac{I_{LPK(LV)}}{3n} \sqrt{1 - \frac{2\varphi}{3\pi}} \quad (20)$$

Figs. 6 and 7 show the rms and average currents on the semiconductors (intrinsic body diode and channel) and inductors on the LV side and MV side, respectively, in function of the designed φ . The current efforts on the semiconductors and inductors, and consequently losses, increases with φ . Furthermore, when the power flows from the MV to the LV, most of the current flows through the channel of the MV side semiconductors, whereas it flows mostly through the body diode on the LV side. Therefore, it is very important to select a power semiconductor for the LV side with low forward drop voltage for the body diode.

IV. LOSSES ANALYSIS AND DESIGN OF THE QAB CONVERTER

As mentioned before, the losses in the main components of the QAB must be carefully computed in function of the main converter parameters, with the aim of properly selecting these parameter, minimizing the losses.

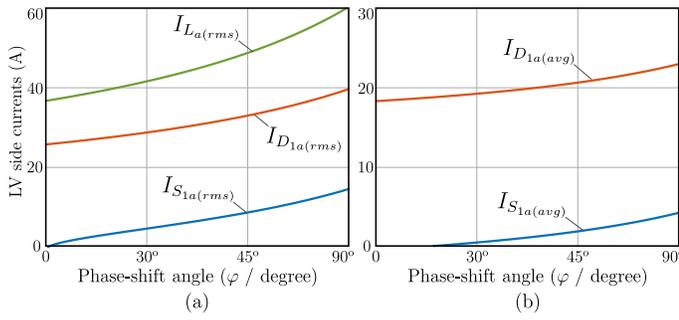


Figure 7. The (a) rms and (b) average currents on the LV side in function of the nominal designed phase-shift angle.

Table II
SPECIFICATION OF THE SEMICONDUCTORS CONSIDERED IN THE DESIGN

SiC-MOSFET / 1.2 kV					
Name	Reference	I	$R_{ds(on)}(@150C)$	V_F	E_{off}
SiC-2	C2M0040120D	30 A	84mΩ	3.3 V	0.3 mJ
SiC-2	C2M0040120D	40 A	84mΩ	3.3 V	0.3 mJ
SiC-3	C2M0025120D	90 A	43mΩ	3.3 V	0.3 mJ
Si-IGBT / 1.2 kV					
Name	Reference	I	$V_{CE(on)}(@150C)$	V_F	E_{off}
IGBT-1	IHW40N120R3	40 A	2.4V	1.3 V	3.1 mJ
IGBT-2	IHW40N120R3	40 A	1.9V	1.3 V	3.1 mJ
IGBT-3	IHW40N120R3	40 A	2.4V	1.3 V	2.03 mJ

A. Semiconductors

An important feature of the modular ST architecture is possibility to use lower blocking voltage semiconductors, implying in a wide variety of device choice during the design. From the converter's specification shown in Table I, 1.2 kV semiconductors can be employed in both sides of the converter, benefiting both efficiency and cost.

In order to take advantage of the high performance of the new SiC devices, SiC-MOSFETs of 1.2 kV voltage rating are considered on the design. These devices are characterized by a very low switching energy and a very low $R_{DS(on)}$. Although the converter is supposed to operate with ZVS, this characteristic is achieved only during the turn-on of the switch, while it turns-off under hard switching. Therefore, by using SiC-MOSFETs, the QAB converter will not only take the advantage of their low $R_{DS(on)}$, reducing the conduction losses considerably, but also the low switching energy, reducing the turn-off losses. Besides that, standard Si-IGBT of 1.2 kV are also taken into consideration during the converter's design, in order to compare the performance of the different devices technologies in this application. The list of the considered semiconductors is presented in Table II. As can be noticed, three different SiC-MOSFETs devices and three different Si-IGBTs are considered on the design. Since different devices can be used on the LV and MV sides, it results in 36 combinations and then 36 designs iterations.

The conduction losses of the MOSFETs can be calculated by (21), where the on-resistance ($R_{ds(on)}$) is function of the drain-source current (i_{ds}), junction temperature (T_J) and gate voltage (V_{gs}). Assuming a constant junction temperature of

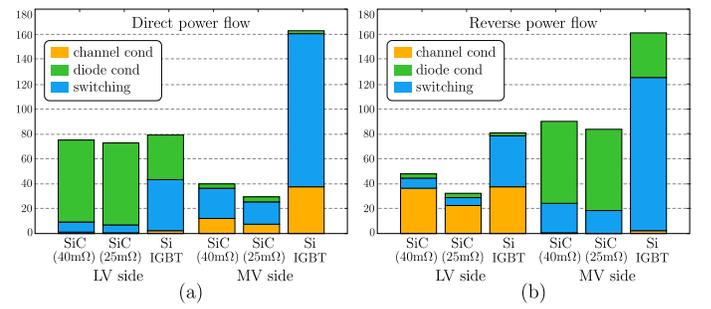


Figure 8. Power dissipation on different semiconductors for the MV and LV side of the QAB converter, for both (direct (a) and reverse (b)) power flow direction.

100°C and a constant gate voltage, the equation is simplified to (22). Similarly, the conduction losses on the diode and IGBT are calculated by (23), where V_f is the forward drop voltage (for diode case) or collector-emitter voltage (for IGBT case), while i_f is the current that flows on the device. The equation can also be simplified to (24).

$$P_{MOS(cond)} = \frac{1}{T} \int_0^T R_{ds(on)}(i_{ds}(t), T_J, V_{gs}) \cdot i_{ds}^2(t) dt \quad (21)$$

$$P_{MOS(cond)} = R_{ds(on)} \cdot I_{S1(rms)}^2 \quad (22)$$

$$P_{IGBT(cond)} = \frac{1}{T} \int_0^T V_f(i_f(t), T_J, V_{gs}) \cdot i_f(t) dt \quad (23)$$

$$P_{IGBT(cond)} = V_f \cdot I_{f(avg)} + R_f \cdot I_{f(rms)}^2 \quad (24)$$

The switching losses can be generally calculated by (25), where $N_{sw(on)}$ and $N_{sw(off)}$ are the number of turn-on and turn-off commutations, respectively, during the time interval T_s . R_g is the gate resistance. As the converter switches always with a constant voltage and it is assumed a constant temperature junction, as well as the V_{gs} and R_g . Because of the ZVS operation, the turn-on losses are neglected, and a simplified equation can be written as presented in (26). The equation as is written in (25) is suitable for a computer implementation, because it is already discretized.

$$P_{(sw)} = \frac{1}{T} \left(\sum_{n=1}^{N_{sw(on)}} E_{on}(V_{ce}, I_d, T_J, V_{gs}, R_g) + \sum_{n=1}^{N_{sw(off)}} E_{off}(V_{ce}, I_d, T_J, V_{gs}, R_g) \right) \quad (25)$$

$$P_{(sw)} = \frac{1}{T} \left(\sum_{n=1}^{N_{sw(off)}} E_{off}(I_d) \right) = E_{off} \cdot f_s \quad (26)$$

Replacing the equations (14) to (18) in (22) and using the parameters of Table II, the conduction losses are calculated. Likewise, the switching losses are calculated using the parameters of Tables I and II in equation (26).

A computer-aided algorithm is used to calculate the semiconductors losses and further details are given in the next section. To verify the losses distribution and performance for different technologies, three devices were selected (SiC-2,

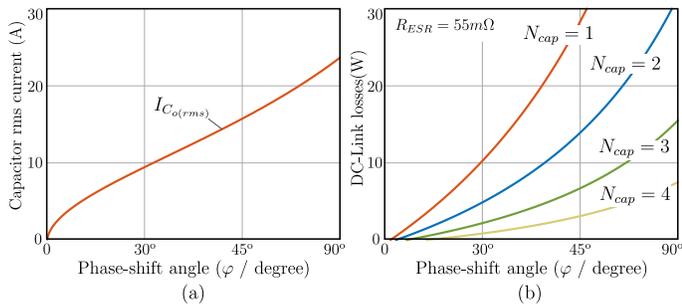


Figure 9. (a) Rms current on the output dc-link capacitor bank, (b) power dissipated on the capacitors dc-link, according to number of parallel capacitors.

SiC-3 and IGBT-1) and their losses are calculated for direct and reverse power flow; the result is illustrated in Fig. 8.

Despite of the soft-switching turn-on, the turn-off losses of the QAB are very relevant, mainly when IGBT are employed, because of the high switching energy compared to the SiC-MOSFETS. When the SiC-MOSFET is employed, the current flows through the channel of the LV side semiconductors, instead the body diode, because the gate signal is applied, providing a lower impedance path to the current. Consequently, the losses are reduced even further when compared to the Si-IGBT. For these reason, the diode losses on the SiC-MOSFETS devices are not relevant in Fig. 8. As expected, the performance of the QAB converter is superior when the SiC-3 is used in both sides, regardless the power flow direction.

B. Output DC-Link Capacitor

The rms current through the output capacitor is calculated by (27).

$$I_{C_o(rms)} = \sqrt{I_{LPK(LV)}^2 \left(1 - \frac{2\phi}{3\pi}\right) - \left(\frac{V_L}{R_{load}}\right)^2} \quad (27)$$

For the dc-link capacitor, the aluminum electrolytic capacitor from EPCOS (*long-life* series), with $1000\mu F$ capacitance and voltage rating of 450 V is used. This type of capacitor is chosen because of its high energy storage density. The capacitor has an equivalent-series resistance of $R_{ESR} = 55m\Omega$. Because of the voltage rating of the capacitors, two devices needs to be connected in series. The losses on this component are calculated according to

$$P_{C_o} = 2 \cdot R_{ESR} \cdot I_{C_o(rms)}^2 \quad (28)$$

The rms current on the output dc-link in function of the designed ϕ and also the losses on the LV dc-link capacitor in function of the designed ϕ for different number of parallel capacitors are illustrated in Fig. 9. Parallel capacitors are considered to reduce the current effort, losses and also to provide a relatively high energy storage on the dc-link, guaranteeing the decoupling between both ac sides.

C. HFT Design

To design the HFT, different core shapes as well as winding construction were considered, as presented in Fig. 10. For the

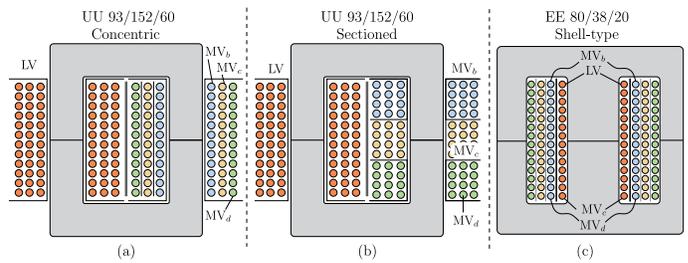


Figure 10. Different HFT implementations: (a) U-shape core with concentric winding, (b) U-shape core with sectioned windings, (c) E-shape core.

Table III
TRANSFORMER SPECIFICATION USED FOR ITS IMPLEMENTATION

parameters	UU93 concentric	UU93 Sectioned	EE-80
Core losses	105 W	85 W	60 W
Wire losses	340 W	98 W	84 W
Leakage ind (LV)	145 μH	140 μH	40.7 μH
Winding res (LV)	0.146 Ω	0.064 Ω	0.08 Ω
Leakage ind (MV 1)	4.17 μH	70.7 μH	16.5 μH
Winding res (MV 1)	0.046 Ω	0.047 Ω	0.072 Ω
Leakage ind (MV 2)	2.3 μH	40.3 μH	13.5 μH
Winding res (MV 2)	0.036 Ω	0.037 Ω	0.059 Ω
Leakage ind (MV 3)	4.5 μH	73.17 μH	15 μH
Winding res (MV 3)	0.049 Ω	0.053 Ω	0.065 Ω
Mag inductance	4.46mH	4.2mH	3.2mH
Implemented HFT			
Core	3 parallel cores - E 80/38/20		
N° of turns (LV)	$n_{LV} = 21$		
N° of turns (MV)	$n_{MV} = 24$		
wires - (LV)	2000 x AWG44		
wires - (MV)	90 x AWG32		

U-shape core, two different winding methods were considered and investigated experimentally: concentric and sectioned. In the concentric winding, the MV coils are wound one over the other (see Fig. 10 (a)), whereas in the sectioned, the MV coils are separated and wound separately, as shown in Fig. 10 (b).

An algorithm was developed to assist the HFT design. In this algorithm, the basic design is performed according to [19], where the number of turns is calculated, wires are selected and so on. The feasibility of implementation is verified by the window utilization factor. Then, the core losses, wire losses and temperature rise are estimated. For the wire losses, the skin and proximity effect are considered additionally to the dc losses. To avoid the skin effect, litz wire is used. Losses caused by proximity effect are estimated based on [20]. For the core losses, the generalized Steinmetz equation [21] is used. Finally, the temperature is estimated according to [19] under the assumption of natural convection cooling.

Three transformers implementations illustrated in Fig. 10 were built and tested experimentally and the main parameters and losses were measured. The results are presented in Table III. Concerning the U-shape core, the sectioned implementation presented much lower wire losses, because of its lower proximity effect losses compared to the concentric. On the other hand, the sectioned implementation presented a very high leakage inductance, whereas the concentric is lower. With the E-shape implementation, it is possible to reach reduced wire losses with lower leakage inductance. However, it is difficult to achieve high isolation voltage between the LV and MV

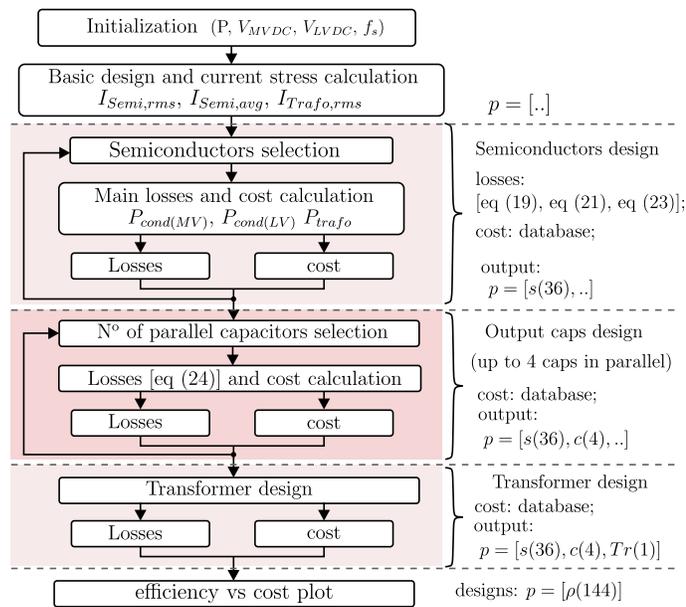


Figure 11. Flowchart of the implemented algorithm used for the QAB design.

side, as desired by the ST application. Considering these three constrains, the E-shape core is selected to implement the HFT of the QAB converter.

D. Final Converter Design

In order to find a optimum trade-off between efficiency and cost of the QAB converter, a computer-aided based design was used and the flowchart of the developed algorithm is shown in Fig. 11. The precise cost estimation is more difficult to be obtained, because it is highly dependent on the market parameters, that can change the price over the time, like: distributor, quantity acquired, etc. As a matter of comparison, the cost used in this algorithm for the semiconductors were obtained directly from the devices manufactures, i.e. *Infineon Technology* [22] for the Si-IGBT and *Cree Wolfspeed* for SiC-MOSFET [23]. For the capacitor and transformer cost, the cost were obtained through the well-known distributor Mouser Electronics [24].

The algorithm starts with the basic design of the converter, as shown in Section III, where the converter's parameters are calculated, like: required inductance, phase-shift angle, current efforts, etc. Then, it selects the semiconductors and calculate their losses and cost. At this point, there is an iteration to calculate the losses and cost for all possible combination of semiconductors. The next point is the output capacitance selection, where an iteration is performed to find the proper number of parallel capacitors according to cost and losses. Finally, the HFT is designed, as described in the previous section.

As a result, the theoretical efficiency of the QAB versus its cost for several designs performed by the algorithm is plotted in Fig. 12. Three designs are highlighted in this figure: (1) lowest cost and lowest efficiency; (2) best trade-off between cost and efficiency; (3) highest efficiency and highest cost. The semiconductor selected in each of the pointed-out designs is

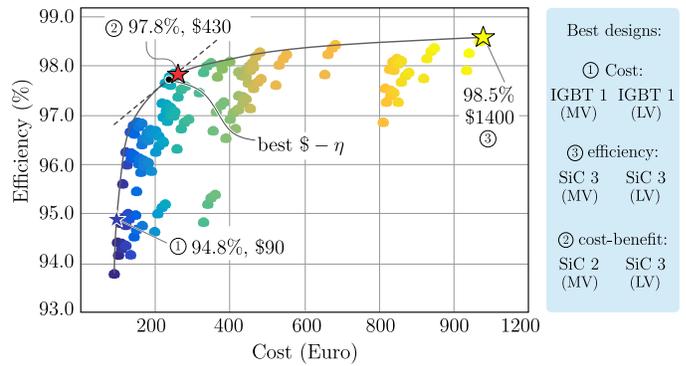


Figure 12. Theoretical efficiency of the QAB versus its cost for different designs.

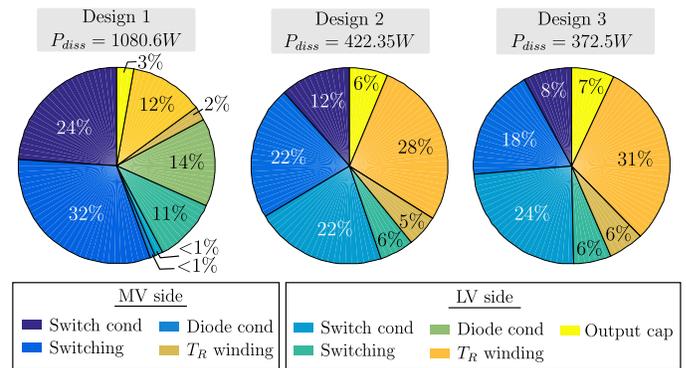


Figure 13. Losses distribution on the main devices for the three designs highlighted: (a) lowest cost, (b) best cost-efficiency trade-off, (c) highest efficiency.

shown in Fig. 12, as well. As can be noticed, the lowest cost and efficiency is obtained when IGBT are employed in both side of the QAB converter. The device SiC-3 provides the best performance, because it has the lowest $R_{DS(on)}$, i.e. conduction losses, and switching losses. However, it is the most expensive solution. When SiC-2 is used in the MV and SiC-3 on the LV side of the QAB, the efficiency decreases slightly, but the cost decreases significantly. Therefore, this design presents the best trade-off between cost and efficiency. The losses distribution on the components of the QAB converter for the three highlighted design are shown in Fig. 13. As can be reinforced, even operating with ZVS during the turn-on, the power dissipated during the turn-off is very relevant, when IGBT is used. Therefore, it is very advantageous and recommended to use SiC-MOSFETs in this converter.

V. PROTOTYPE IMPLEMENTATION AND EXPERIMENTAL RESULTS

In order to evaluate the converter performance experimentally and verify the presented design procedure, a prototype was built and tested. The main specifications are shown in Table I. The details about the converter construction and the final results are discussed.

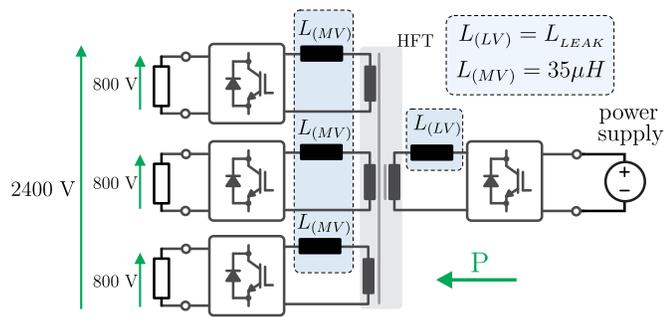


Figure 14. Scheme of the tested prototype, presenting its connection to the load and the external transformer implementation.

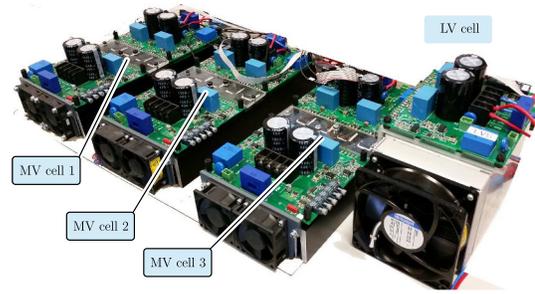


Figure 15. Picture of the implemented prototype 20 kW, 800 V to 700 V QAB converter.

Table IV
SPECIFICATION OF THE IMPLEMENTED INDUCTOR

Parameters	values
Core	E - 42/21/15
Inductance (L_{MV})	$35\mu H$
Winding resistance (R_{coil})	$37m\Omega$
N° of turns	25
wires	90 x AWG32

A. Final Prototype Assembly

From the previous design methodology, the QAB converter presents the best cost for the design 1 and the best cost-benefits for the design 2, (see Fig. 12). Therefore, both combinations are used on the construction and test of the prototype, in order to evaluate experimentally the benefits to use SiC.

As an outcome of the converter's design, the required equivalent inductance seen by the LV side is $L_{eq} = 95\mu H$, in which can be implemented in the MV side and/or LV side, once the relation defined by equation (6) is respected. The imperfect construction of the transformer causes a deviation of the leakage inductance values of the MV side windings ,i.e. $L_{b_{leak}} \neq L_{c_{leak}} \neq L_{d_{leak}}$. To reduce this effect, external inductors should be used on the MV side, resulting in $L_{(b,c,d)} = L_{(b,c,d)_{leak}} + L_{ext}$. To reach the desired inductance value, three additional inductors of $L_{ext} = 35\mu H$ are used in MV side. The value of L_{ext} was calculated according to the equation (6), taken into consideration the leakage inductance of the HFT presented in Table III. The specification used to implement physically the inductors are presented in Table IV, as well as the intrinsic measured resistance. These additional inductors associated to the leakage inductance of the HFT result in the desired inductance value.

Fig. 14 shows the block diagram of the schematic used to test the converter. For simplicity's sake, the converter was tested with reverse power flow, where a single dc power supply was used on the LV side and three loads were connected on the MV side. Fig. 15 shows the picture of the prototype, where the cells of the CHB associated to the QAB converter (see Fig. 1) is observed, sharing the same cooling system.

B. Experimental Results

The experimental results were obtained for the converter operating in steady-state with balanced power, i.e. equal power processed by the MV cells, as well as for unbalanced condition, where the main waveforms were saved. Additionally, the efficiency curve of the QAB is obtained and discussed, when Si-IGBT (design 1) and SiC-MOSFETs (design 2) are used. The results are summarized in Fig. 16 and Fig. 19.

Fig. 16 (a) shows the main waveforms of the converter operating in steady-state, where the currents on the LV cell (i_{La}) and MV cells (i_{Lb} , i_{Lc} , i_{Ld}) are presented. From this result, the balanced operation of the QAB converter is noticed, where each MV cell processes the same amount of power. Similarly, Fig. 16 (b) shows voltage and current on the ac side of the MV bridge (v_{Lb} and i_{Lb}) and LV bridge (v_{La} and i_{La}), where the phase shift operation of these bridges is observed. These waveforms are in accordance with the theoretical one shown in Fig. 3. The commutation of the switches for the LV and MV sides is presented in Fig. 17 (a) and (b). Fig. 17 (a) shows the current and voltage on the LV side semiconductor (s_{1a}), as well as the commutation detail, where soft-switching operation is verified. As expected, the semiconductor turns on in ZVS and turns off under hard-switching. However, the constant current imposed by the inductance during the dead-time of the switches discharges the output capacitance of the switch (s_{1a}), while charges the capacitance of the respective switch of the leg, (i.e. s_{2a}), implying in a commutation losses reduction (almost ZVS operation). This features is obtained only when SiC-MOSFETs are used. Likewise, the current and voltage on the MV side semiconductor (s_{1b}) is illustrated in 17 (b), as well as the commutation details. The same effect described for s_{1a} is also observed in the MV side switch s_{1b} .

An unbalanced operation was forced, where the MV bridges were subjected to different power levels. The aim of this test is to demonstrate the possibility to operate under different power levels on the MV side, even though it is not an usual operation condition in ST application. The result is presented in Fig. 18, where the voltage on the MV cell (v_{Lb}) and three MV cell currents (i_{Lb} , i_{Lc} , i_{Ld}) are presented for balanced (Fig. 18 (a)) and unbalanced (Fig. 18 (b)) power. As can be noticed, the unbalanced power condition deforms the current shape, but the soft-switching features is not affected.

Finally, the efficiency curve in function of the output power is shown in Fig. 19. The efficiency curve was obtained

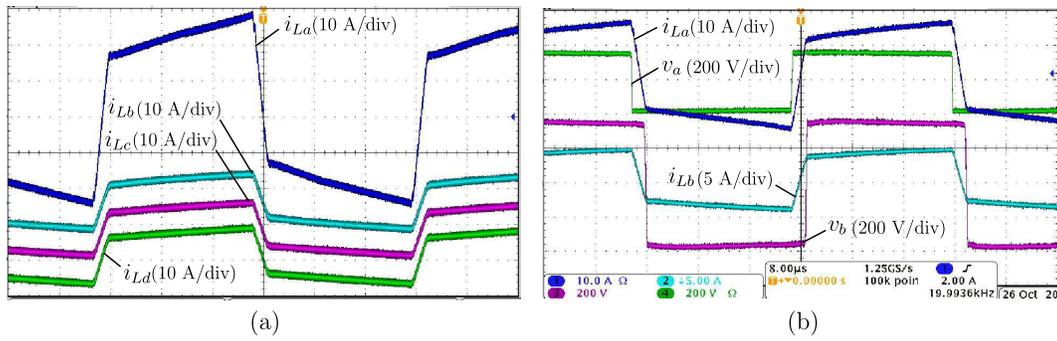


Figure 16. Experimental results of the QAB converter: inductor current waveforms on the LV side (i_{La}) and MV side (i_{Lb} , i_{Lc} and i_{Ld}) of the QAB converter.

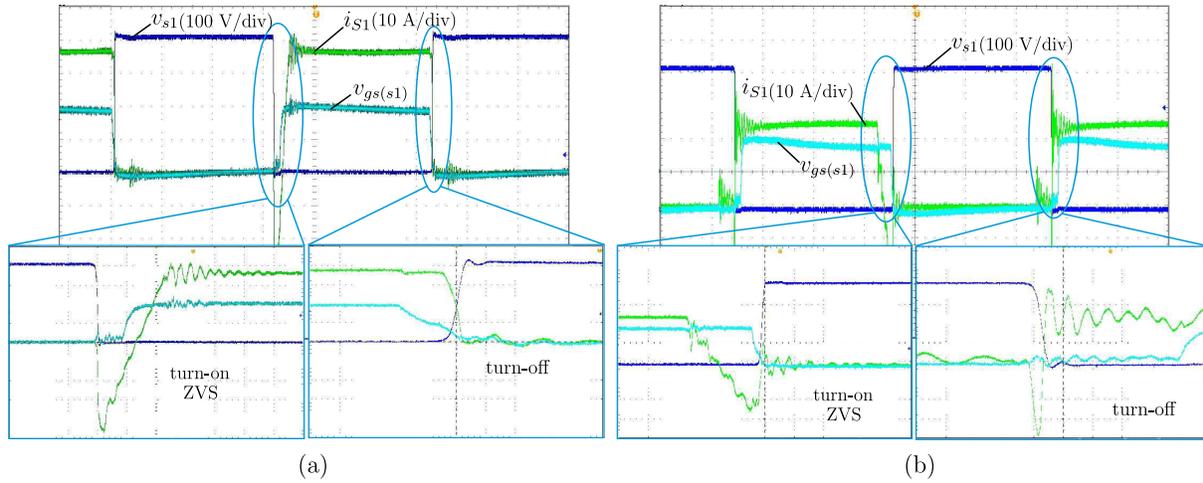


Figure 17. Commutation of the semiconductor including the turn on and turn off detail: (a) LV semiconductor (s_{1a}), (b) MV side semiconductor (s_{1b}).

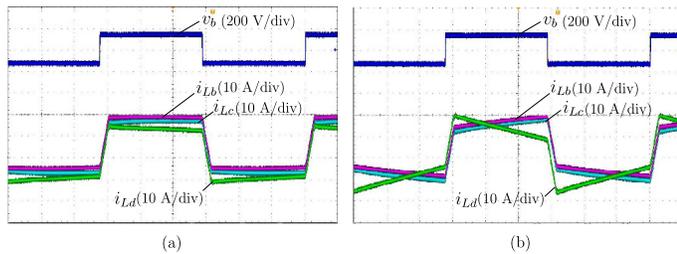


Figure 18. Main voltage (v_{Lb}) and currents (i_{Lb} , i_{Lc} and i_{Ld}) MV side waveforms of the QAB obtained experimentally for: (a) balanced and (b) unbalanced power conditions.

experimentally using the high performance power analyzer WT1800 from Yokogawa. The power analyzer has an accuracy of 0.05% of reading and 0.1% of the full-scale range, for measuring dc quantities. Although it is considered a very precise equipment, a small error is expected. Hence, the error was computed and the Fig. 19 shows the efficiency curve measure by the efficiency, taking into consideration the accuracy of the equipment. As can be seen, the converter has achieved a peak efficiency of 94.28% at a power level of around 8 kW, when IGBT are used (design 1), while at nominal load the converter has achieved around 93.4% of efficiency. For the design 3, where SiC-MOSFETs are used, the converter has achieved a peak efficiency of 97.5% at a

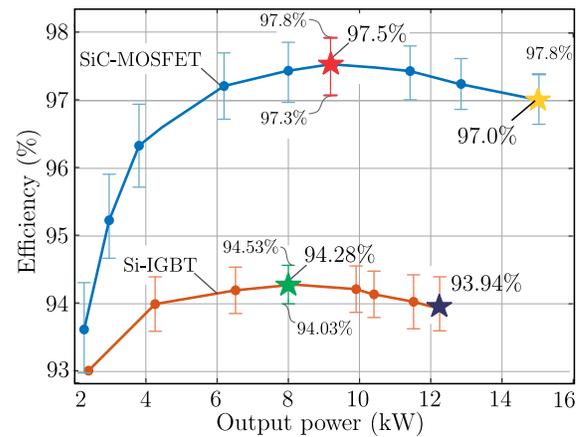


Figure 19. Efficiency curve in function of the output power of the converter.

power level of around 8.5 kW and its efficiency is 97% at nominal load. Therefore, the use of SiC-MOSFETs results in a losses reduction of 57% at 8 kW (increasing the efficiency in 3.3%) and a losses reduction of 56.1% at 12 kW (increasing the efficiency in 3%). These results confirmed the optimum design of the converter, as well as the high potentiality of the SiC technology in this application.

VI. CONCLUSION

In this paper, the quadruple active bridge is used as a basic building block to implement a modular smart transformer. Since the efficiency and cost are very important in this application, a multi-objective optimization algorithm was developed. The losses on the components were modeled and a database with the cost and electric characteristics of each component was created. The algorithm combines these parameters in order to find the optimum point for cost, efficiency and the best trade-off between cost and efficiency. Besides that, SiC-MOSFETs and Si-IGBT were considered on the design of the converter. From these design, a 20 kW prototype was built and tested. The experimental results have shown an efficiency of 97.5%, which is the highest obtained so far for this kind of converter. It demonstrates the effectiveness of the proposed design. Regarding the converter's performance with different semiconductors technology, it was verified that the SiC-MOSFETs is more advantageous, due to its low energy losses, almost ZVS operation (during the switch turn-off) and the conduction of the reverse current through the channel, instead the diode, reducing the conduction losses. Consequently, the use of SiC-MOSFETs reduced the converter's losses in around 57%, compared to the IGBT. These results demonstrate the feasibility of this technology for such application.

REFERENCES

- [1] M. Liserre, G. Buticchi, M. Andresen, G. D. Carne, L. F. Costa, and Z. X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46–58, Summer 2016.
- [2] M. Liserre, M. Andresen, L. Costa, and G. Buticchi, "Power routing in modular smart transformers: Active thermal control through uneven loading of cells," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43–53, Fall 2016.
- [3] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, Sept 2013.
- [4] J. Wang, A. Q. Huang, W. Sung, Y. Liu, and B. J. Baliga, "Smart grid technologies," *IEEE Industrial Electronics Magazine*, vol. 3, no. 2, pp. 16–23, June 2009.
- [5] X. She, X. Yu, F. Wang, and A. Q. Huang, "Design and demonstration of a 3.6-kv 120-v/10-kva solid-state transformer for smart grid application," *IEEE Trans on Power Elect.*, vol. 29, no. 8, pp. 3982–3996, Aug 2014.
- [6] L. Costa, G. Buticchi, and M. Liserre, "Highly efficient and reliable sic-based dc-dc converter for smart transformer," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2017.
- [7] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W. K. Ling, and J. Lam, "Computer-aided design and optimization of high-efficiency llc series resonant converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3243–3256, July 2012.
- [8] C. Gammeter, F. Krismer, and J. W. Kolar, "Comprehensive conceptualization, design, and experimental verification of a weight-optimized all-sic 2 kv/700 v dab for an airborne wind turbine," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 638–656, June 2016.
- [9] R. M. Burkart and J. W. Kolar, "Comparative η ρ σ pareto optimization of si and sic multilevel dual-active-bridge topologies with wide input voltage range," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5258–5270, July 2017.
- [10] R. W. A. A. D. Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63–73, Jan 1991.
- [11] L. Costa, G. Carne, G. Buticchi, and M. Liserre, "Power routing in modular smart transformers: Active thermal control through uneven loading of cells," *IEEE Power Electronics Magazine*, vol. 10, no. 2, Summer 2017.

- [12] L. F. Costa, F. Hoffmann, G. Buticchi, and M. Liserre, "Comparative analysis of mab dc-dc converters configurations in modular smart transformer," in *8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, April 2017.
- [13] C. Zhao, S. D. Round, and J. W. Kolar, "An isolated three-port bidirectional dc-dc converter with decoupled power flow management," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2443–2453, Sept 2008.
- [14] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Family of multiport bidirectional dc-dc converters," *IEEE Proceedings - Electric Power Applications*, vol. 153, no. 3, pp. 451–458, May 2006.
- [15] J. L. Duarte, M. Hendrix, and M. G. Simoes, "Three-port bidirectional converter for hybrid fuel cell systems," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 480–487, March 2007.
- [16] L. F. Costa, G. Buticchi, and M. Liserre, "Highly efficient and reliable dc-dc converter for smart transformer," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 184–190.
- [17] S. Falcones, R. Ayyanar, and X. Mao, "A dc-dc multiport-converter-based solid-state transformer integrating distributed generation and storage," *IEEE Trans on Power Elect.*, vol. 28, no. 5, pp. 2192–2203, May 2013.
- [18] L. F. Costa, G. Buticchi, and M. Liserre, "Quadruple active bridge dc-dc converter as the basic cell of a modular smart transformer," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 2449–2456.
- [19] M. K. Kazimierczuk, *High-Frequency Magnetic Components*. Wiley Publishing, 2009.
- [20] W. G. Hurley, E. Gath, and J. G. Breslin, "Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 369–376, Mar 2000.
- [21] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Computers in Power Electronics, 2002. Proceedings. 2002 IEEE Workshop on*, June 2002, pp. 36–41.
- [22] "Infineon technologies ag," <https://www.infineon.com/>, accessed: 2017-06-12.
- [23] "Cree wolfspeed," <http://www.wolfspeed.com/rf>, accessed: 2017-06-12.
- [24] "Mouser electronics," <http://www.mouser.de/>, accessed: 2017-06-12.



Levy Ferreira Costa (S'14) received the B.S. degree in electrical engineering from the Federal University of Ceara, Brazil, in 2010 and the M.S. degree from the Federal University of Santa Catarina, Brazil, in 2013. From 2013 to 2014, he was an Electrical Design Engineer with Schneider Electric, Brazil. He is currently working toward the Ph.D. degree at the Chair of Power Electronics, Christian-Albrechts-University of Kiel, Germany. His research interests include dc-dc converters, high-power converter systems and wide-bandgap semiconductors.



Giampaolo Buticchi (S10-M13-SM17) received the Masters degree in Electronic Engineering in 2009 and the Ph.D degree in Information Technologies in 2013 from the University of Parma, Italy. In 2012 he was visiting researcher at The University of Nottingham, UK. Between 2014 and 2017 he was a post-doctoral researcher at the University of Kiel, Germany. He is now Associate Professor in Electrical Engineering at The University of Nottingham Ningbo China. His research area is focused on power electronics for renewable energy systems, smart transformer fed micro-grids and dc grids for the More Electric Aircraft. He is author/co-author of more than 130 scientific papers.



Marco Liserre (S'00-M'02-SM'07-F'13) received the M.Sc. and Ph.D degree in Electrical Engineering from the Bari Polytechnic, respectively in 1998 and 2002. He has been Associate Professor at Bari Polytechnic and Professor in reliable power electronics at Aalborg University (Denmark). He is currently Full Professor and he holds the Chair of Power Electronics at Christian-Albrechts-University of Kiel (Germany). He has published over 280 technical papers (more than 70 of them in international peer-reviewed journals), 4 chapters of a book and a book

(Grid Converters for Photovoltaic and Wind Power Systems, ISBN-10: 0-470-05751-3 IEEE-Wiley, second reprint, also translated in Chinese). These works have received more than 16000 citations. Marco Liserre is listed in ISI Thomson report The world's most influential scientific minds from 2014. He has been awarded with an ERC Consolidator Grant for the project 'The Highly Efficient And Reliable smart Transformer (HEART), a new Heart for the Electric Distribution System. He is member of IAS, PELS, PES

and IES. He is Associate Editor of the IEEE Transactions on Industrial Electronics, IEEE Industrial Electronics Magazine, IEEE Transactions on Industrial Informatics, where he is currently Co-Ed, IEEE Transactions on power electronics and IEEE Journal of Emerging and Selected Topics in Power Electronics. He has been Founder and Editor-in-Chief of the IEEE Industrial Electronics Magazine, Founder and the Chairman of the Technical Committee on Renewable Energy Systems, Co-Chairman of the International Symposium on Industrial Electronics (ISIE 2010), IES Vice-President responsible of the publications. He has received the IES 2009 Early Career Award, the IES 2011 Anthony J. Hornfeck Service Award, the 2014 Dr. Bismal Bose Energy Systems Award, the 2011 Industrial Electronics Magazine best paper award and the Third Prize paper award by the Industrial Power Converter Committee at ECCE 2012, 2012. He is senior member of IES AdCom. In 2013 he has been elevated to the IEEE fellow grade with the following citation "for contributions to grid connection of renewable energy systems and industrial drives".