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Highly Efficient and Reliable SiC-based DC-DC Converter for Smart Transformer

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***Abstract*—The series-resonant converter (SRC) has been used in several application and it recently became popular for Smart Transformers (STs). In this application, the efficiency and reliability are of paramount importance. Although many papers have addressed the design challenges to improve the converter efficiency, discussions about the reliability are still missing in literature. In this context, this paper presents a design procedure focusing on the efficiency and reliability improvement of the SRC for ST application. High efficiency is achieved through the use of Silicon-Carbide (SiC) MOSFETs, reducing conduction and switching losses, and the detail design procedure based on accurate losses modeling. High reliability is achieved through a fault tolerant topology and reliability-oriented design of the resonant circuit passive components. Experimental results obtained for the optimized 10 kW series resonant converter has shown an efficiency of 98.61%.**

***Index Terms*—Dc-dc converter, reliability, high efficiency, silicon-carbide devices, smart transformer.**

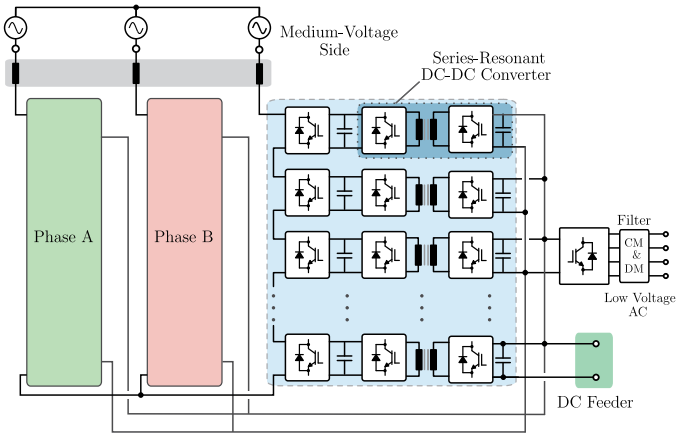

Figure 1. Modular Smart Transformer architecture using the Series-Resonant converter as a building block of the dc-dc stage of the system.

I. Introduction

The series-resonant dc-dc converter (SRC) has been very used in a large range of voltage and power application, such as wireless power transfer for electrical vehicle [1]–[4] (24-600 V / 5-100 kW), battery charger [5] - [6] (24-600 V / 5 100 kW), renewable energy system [7]–[10] (0.1-500 kV / 0.1-100 MW) and high voltage power supply for specific application, as traveling-wave tube (TWT) for satellites [11] (1-10 kV / 1-100 kW). Because of its characteristic of output voltage regulation in open loop, associated to its feature of soft-switching, the converter became very popular in Smart Transformer (ST) [12] application. Hence, this converter has been used to implement the dc-dc stage of ST's architectures based on modular [13]–[15] and also non-modular [16] concept.

In this kind of application, high efficiency is extremely desired and many optimization methods focusing on the efficiency improvement have been discussed in the literature [15]. A computer-aided design approach is proposed in [17] to optimize the efficiency of a resonant converter, in which a peak value of 97.4% was achieved. A modified topology of the resonant converter is proposed in [18], [19] with the aim of reducing the losses. In both studies Gallium-nitride devices are employed and a maximum efficiency of 97.5% and 98.3% is obtained in [18] and [19], respectively. These designs are for low power (up to 300 W) and low voltage (up to 400 V) applications. A high efficiency SRC is reported in [20] for higher power and voltage level application (5 kW, 600 V). In that paper, Silicon-Carbide (SiC) MOSFETs are used, presenting a peak efficiency of 97.6%, in which is one of the highest reported in literature, considering the power/voltage level.

In addition to the high efficiency feature, the continuity of operation is of paramount importance and then a highly reliable system with a long lifetime is required [21]. Although the reliability is considered even more important than the efficiency in ST application, issues related to the SRC reliability has not been intensively investigated. Currently, very few papers have addressed reliability improvement of dc-dc converters by using fault tolerance approach [22], [23] and the lifetime extension approach for dc-dc converters has not yet been discussed on the literature.

In this context, this paper presents an optimum design of the SRC used as a building block of the dc-dc stage of the ST. The design is focused on the efficiency and reliability optimization. The modular ST architecture using the SRC as a module is presented in Fig. 1, while the topology of the SRC (including the parasitic elements) is shown Fig. 2. The input of the converter is connected on the medium voltage (MV) side of the system and its output is connected to the low voltage (LV) side. To achieve a very high efficiency, the loss modeling in all components is carried out and the characteristic equations are obtained. To further improve the efficiency, SiC MOSFETs with very low on-state resistance ($R_{DS(on)}$) are used, reducing drastically the conduction losses. Moreover, the Medium-Frequency Transformer (MFT) is carefully designed in order to obtain lowest losses with the smallest size. The reliability

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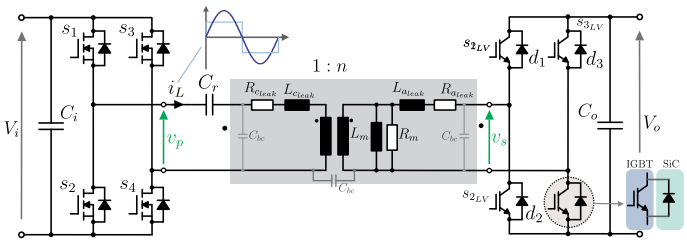


Figure 2. Topology of the Series-Resonant Converter.

Table I
SPECIFICATION OF THE SRC

Input voltage	Output Voltage	Nominal Power	Isolation frequency
600 V	700 V	10 kW	20 kHz

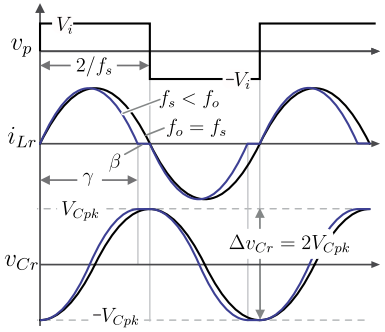


Figure 3. Main waveforms of the SRC.

is addressed by using the converter lifetime assessment and extension approach. One of the most faulty components of the SRC is the resonant capacitor (C_r). Thus, the influence of the converter parameters selection on the capacitor lifetime is evaluated, with the aim to extend the lifetime of this components and, consequently the converter lifetime. Furthermore, a fault-tolerant SRC topology previously presented [22] is proposed to be used in this application. The converter can continuously operate even with a semiconductor fault, contributing significantly to the converter reliability.

The paper is divided as follows: section II describes the operation principle of the SRC, where the main equations for the design are provided. The losses model in all components of the converter are computed and discussed in section III. In section IV, the capacitors lifetime model is derived and a discussion about the influence of the tank circuit components (resonant inductor L_r and capacitor C_r) selection on the capacitors lifetime is presented. Finally, a 10 kW prototype was built, and its high efficiency and reliability are verified through experimental results, validating the approach presented in this work. As main result, an efficiency of 98.61% is presented, which is one of the highest reported in the literature so far.

II. Operation Principle of the SRC

The topology of the SRC based on full-bridge configuration (FB-SRC) is shown in Fig. 2, while its specification is shown in Table I. The most efficient operating point of the SRC is when it operates in the discontinuous conduction mode (DCM) with the switching frequency (f_s) equal or slightly below the resonance frequency (f_o). In this operation mode, the primary-side switches achieve zero-voltage-switching (ZVS) and low-current switching, the output diodes achieve zero-current switching (ZCS). As additional advantages, the converter has good transformer utilization and also low EMI emission, due to the smooth current shape (low di/dt). According to [19], the main problem with the SRC is the lack of input voltage regulation. On the other hand, it is an advantage for ST application, once the system has enough degrees of freedom to control the input voltage by using the front-end rectifier (first stage). Consequently, the open-loop operation of the SRC makes the system simpler and inexpensive, since the number of sensors can be reduced.

The main waveforms in this operation mode are shown in Fig 3. To support the analysis, the variables resonant frequency (f_o), resonant angular frequency (ω_0) and characteristic impedance of the resonant network (Z) are defined by (1), in terms of the resonant inductor (L_r) and capacitor (C_r) of the tank circuit.

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}, \quad \omega_0 = 2\pi f_0, \quad Z = \sqrt{\frac{L_r}{C_r}} \tag{1}$$

To operate in DCM, the converter parameters must satisfy the conditions presented in (2) [24], where γ is the angular length of one half switching period and I_o is the load current. From these conditions it is possible to design L_r and C_r, considering the operation range of the converter.

$$\gamma = \frac{\omega_0}{2f_s} > \pi, \quad f_s < f_0, \quad I_o < 8 f_s C_r V_o \tag{2}$$

As the converter with unit gain, the output voltage is defined as (3).

$$V_o = nV_i \tag{3}$$

Generally, the converter is designed to operate at the resonant frequency ($f_s = f_o$) [25], reaching then the maximum efficiency point. To do so, the pair L_r and C_r have to satisfy the condition imposed in (1). Thus, there is one degree of freedom to select one of these parameters, while the other is chosen consequently. Nevertheless, the selection of the pair L_r and C_r has an impact on the current and voltage effort on the resonant capacitor, influencing its lifetime. Therefore, the selection of L_r and C_r plays an important role not only on the converter efficiency, but also on the components lifetime. This aspect will be discussed in the next sections.

As the converter operates with soft-switching, high switching frequency can be chosen, leading to the reduction of the passive components. However, the MFT requires high voltage isolation, as determined by the application [12], and this sets an upper limit to the operating frequency. In fact, since primary and secondary windings must be spatially separated, proximity effect would increase copper losses. Moreover, given a constant probability of partial discharge, a higher switching frequency translates to more partial discharge events, with detrimental effects on the transformer lifetime. For these reasons, 20 kHz was selected, as shown in Table I.

III. Losses Analysis of the SRC

As mentioned before, the losses in the main components of the SRC must be carefully computed in function of the main converter parameters, with the aim of properly selecting these parameter, minimizing the losses.

A. Semiconductors

In order to take advantage of the high performance of the new SiC devices, SiC MOSFETs of 1.2 kV voltage rating are considered for the primary side. These devices are characterized by a very low switching energy and a very low $R_{DS(on)}$. By using them, the SRC will mainly take the advantage of its low $R_{DS(on)}$, reducing the conduction losses considerably. For the secondary side, bidirectional switches need to be used, because of the bidirectional power flow requirement of the converter. IGBTs in parallel with high performance SiC diodes are therefore utilized because the converter will operate for the majority of the time transferring the power from MV to LV side, making the use of SiC MOSFETs even in the secondary side not economically justifiable. The list of the considered semiconductors is presented in Table II.

The conduction losses of the primary side MOSFETs can be calculated by (4), where the on-resistance ($R_{dc(on)}$) is function of the drain-source current (i_{dc}), junction temperature (T_J) and gate voltage (V_{gs}). Assuming a constant junction temperature of $100°C$ and a constant gate voltage, the equation is simplified to (5). As can be observed, the conduction losses depends on the inductor peak current (i_{Lpk}) and also γ. Both parameters are highly depends on the tank circuit components (L_r and C_r).

The conduction losses of the secondary side diodes can be calculated in function of the current and devices parameters by (6). Similarly as for the MOSFET, the diodes conduction losses are highly dependent on L_r and C_r. The influence on L_r and C_r is discussed in section V.

As the converter operates under soft-switching condition with ZVS and ZCS on the primary side and ZCS on the secondary, the switching losses can be neglected.

$$P_{prim(cond)} = \frac{1}{T}\int_0^T R_{ds(on)}\left(i_{ds}(t), T_J, V_{gs}\right)\cdot {i_{ds}}^2(t)\,dt \tag{4}$$

$$P_{S_1(cond)} = R_{ds(on)}\cdot I^2_{S_1(rms)} = R_{ds(on)}\cdot\left(i_{Lpk}\cdot\frac{1}{2}\sqrt{\frac{\gamma}{2}}\right)^2 \tag{5}$$

$$P_{\sec(cond)} = \frac{1}{T}\int_0^T V_F\left(i_F(t), T_J, V_{gate}\right)\cdot i_F(t)\,dt \tag{6}$$

$$\begin{aligned} P_{D_1(cond)} &= V_F\cdot I_{D_1(avg)} + R_F\cdot I^2_{D_1(rms)} \\ &= V_F\cdot\left(\frac{i_{Lpk}}{2n\cdot\pi}\right) + R_{ds(on)}\cdot\left(\frac{i_{Lpk}}{2n}\cdot\sqrt{\frac{\gamma}{2}}\right)^2 \end{aligned} \tag{7}$$

Table II
Specification of the semiconductors considered in the design

MOSFET - MV side				
Type	Reference	V	I	$R_{ds(on)}$ (@150 C)
SiC	C2M0040120D	1.2 kV	40 A	$84m\Omega$
SiC	C2M0025120D	1.2 kV	90 A	$43m\Omega$
IGBT - LV side				
Type	Reference	V	I	$V_{CE(on)}$ (@150 C)
Si	IHW40N120R3	1.2 kV	80 A	$2.4V$
Diode - LV side				
Type	Reference	V	I	$V_{F(on)}$ (@25 C)
SiC	C4D20120D	1.2 kV	16,5 A	$3V$
SiC	C4D40120D	1.2 kV	40 A	$3V$

B. DC-Link Capacitor

For the dc-link capacitor, the aluminum electrolytic capacitor from EPCOS (*long-life* series), with $1000\mu F$ capacitance and voltage rating of 450 V is used. This type of capacitor is chosen because of its high energy storage density, compared to other type of capacitors. The capacitor has an equivalent-series resistance of $R_{ESR} = 55m\Omega$. Because of the voltage rating of the capacitors, two devices needs to be connected in series. The losses on this component are calculated according to

$$P_{C_o} = 2\cdot R_{ESR}\cdot I^2_{C_o(rms)} = 2\cdot R_{ESR}\cdot\left(\frac{i_{Lpk}}{n}\cdot\sqrt{\frac{\gamma}{2}}\right)^2. \tag{8}$$

C. Medium-Frequency Transformer Design

In order to optimize the transformer losses, taking into account also the transformer size, a computer-aided design was carried out, and the algorithm flowchart is depicted in Fig. 4. The database populated with suitable E-type ferrite cores was created and it is shown in Table III. The core-type construction as shown in Fig. 4 is also assumed. The algorithm starts with the smallest core selection, in this case a single E 55/28/21, and then the basic design is performed. In this point, the number of turn of both windings is calculated and the wires are selected. In the next point, the implementation feasibility is verified by comparing the available window area of the selected core with the area required for the design. If the transformer can not be built, a bigger core is selected and the procedure starts again. Otherwise, the algorithm goes to the next point: losses calculation.

For the wire losses, the skin and proximity effect are considered additionally to the dc losses. To avoid the skin effect, litz wire is used. To losses caused by proximity effect are estimated based on [26]. For the core losses, the Steinmetz equation due to the almost pure sinusoidal current waveforms [27] is used. Finally, the temperature is estimated according to [28] under the assumption of natural convection cooling. The design result is summarized in Table IV. Discussions about the transformer implementation and experimental verification are presented in Section V.

IV. Reliability Assessment

To achieve high reliability, the most frequent device failures are evaluated and a failure mode and effect analysis (FMEA)

Table III
SPECIFICATION OF THE FERRITE CORES CONSIDERED IN THE DESIGN

Core	Ferrite Material	Specification	N° of parallel cores
E 55/28/21	N87/N97	B66335	up to 3
E 65/32/27	N87	B66387	up to 3
E 70/33/32	N87	B66371	up to 2
E 80/38/20	N87	B66375	1

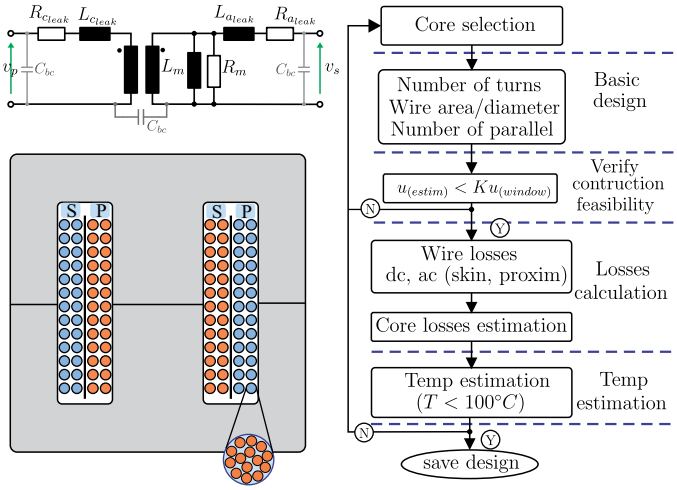


Figure 4. Electric model of the MFT, showing the parasitic elements. Implementation scheme of the MFT, showing the disposition of the primary and secondary windings in the core. The simplified flowchart of the algorithm used to design the optimized MFT.

for the SRC is carried out, as shown in Table V. According to the industries reports [29], [30], the most susceptible device on the SRC is the primary side semiconductor, that is usually implemented using MOSFETs [29], [30]. In the second place is the resonant capacitors (C_r).

To improve the robustness of the converter and consequently the smart transformer reliability, the failure causes on these two components are analyzed and a solution to avoid or postpone the fault in each case is proposed.

Table IV
TRANSFORMER SPECIFICATION USED FOR ITS IMPLEMENTATION

Core	N of turns	wire	N° of parallel cores
2x E 65/32/27	$n_{pri} = 26$	90 x AWG32	up to 3
	$n_{sec} = 22$	2000 * AWG44	up to 2

Table V
FAILURE MODE AND EFFECTS ANALYSIS OF THE SRC

Most faulty device	Failure mode	Failure cause	Solution
Semiconductors Devices	Short-circuit	current stress Overvoltage Load SC	Fault tolerance scheme
Resonant capacitor (C_r)	open-circuit	current stress Overvoltage/start-up overload/SC	Optimum parameter selection

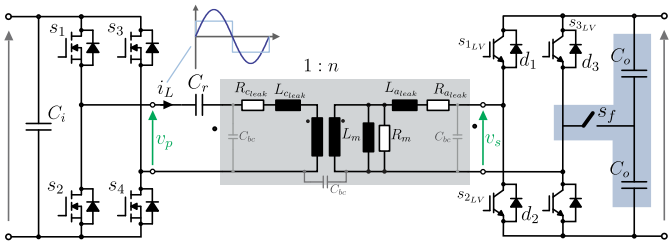


Figure 5. SRC topology with fault tolerance capability used as a basic cell of the dc stage of the ST.

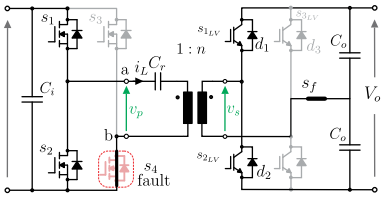


Figure 6. Operation of the fault tolerant SRC, under fault condition: short-circuit on semiconductor s_4.

A. Primary side semiconductor failure

As can be observed in Table V, the fault on the switches reported in [30], regardless the reason, leads to a short-circuit (SC) state of this device. Hence, a solution to avoid this problem, keeping the converter still operational, is to use the fault tolerant SRC topology proposed in [22] (shown in Fig. 5), instead of the classic one shown in Fig. 2. Additionally, the topology presented in Fig. 5 is also resilient to open-circuit (OC), making it a suitable solution for every kind of semiconductor fault of the primary side.

The basic idea of this topology is to remain operating the converter after the fault, i.e. SC or OC of a semiconductor, but as a half-bridge SRC (HB-SRC), instead the full-bridge SRC (FB-SRC), isolating the faulty leg. As an example, it is assumed that the switch s_4 is damaged in SC, as depicted in Fig. 6, so that s_3 must remain open. Since the switch s_4 is short-circuited, the point b highlighted in Fig. 6 is directly connected to the primary side ground resulting in the HB-SRC. Meanwhile, the healthy leg (composed of s_1 and s_2) operates normally. As a result, the effective value of voltages v_p and v_s drop to half of their original values, implying an output voltage (V_o) reduction. To avoid that, a reconfigurable rectifier is used. In faulty case, the switch s_f is activated, as shown in Fig. 6, and the secondary side operates as a voltage-doubler rectifier, preserving the output voltage. More detail about the converter operation can be obtained in [22].

B. Resonant capacitor failure

The resonant capacitor is listed as the second most susceptible device to failure. The reasons for that are the start-up conditions (leading to an overvoltage), and also the current stress caused by the load variation (as short-circuit or overload). Normally, most of the failures lead to an OC condition [31]. In order to postpone as much as possible the capacitor failure, its lifetime model is evaluated, in order to implement a reliability-based design.

The Metalized Polypropylene Film (MPPF) capacitors from WIMA (MKP10 series) are used to implement the tank circuit. The considered capacitors are: $150nF$, $330nF$, $680nF$, all rated for 400 V_{ac} / 650 V_{dc}. According to [31], for this kind of capacitor, the lifetime model is given by (9), where L_o is the expected lifetime tested by the manufacturer, V_{Cpk} and V_o are the capacitor voltage at use condition and test condition, respectively. T and T_o are the temperature at use condition and test condition, respectively, in Kelvin. K_B is Boltzmanns constant (8.62105 eV/K), E_a is the activation energy, and n is the voltage stress exponent and theses last constants depends on the manufacturer [31]. As can be noticed in (9), the capacitors lifetime (L) does not depend only on the capacitor voltage (V_{Cpk}), but also from the rms inductor current ($i_{L(rms)}$), which is directly related to the operation temperature. Since both parameters V_{Cpk} and $i_{L(rms)}$ can be rewritten in terms of L_r and C_r, as demonstrated in equations (10) and (11), then the capacitor lifetime depends L_r and C_r, as shown in (12).

In this context, the influence of the L_r and C_r pair selection on the capacitor lifetime is evaluated. To do so, the main parameters that has influence of the lifetime capacitor, i.e. the rms inductor current, capacitor voltage and output voltage ripple are analyzed in function of L_r and C_r, resulting in the graphics plotted in Fig. 7. Although the output voltage ripple and output voltage overshoot have no effect on the capacitors lifetime, they are analyzed, because these parameters are very important for the converter and they also depend from L_r and C_r. To plot these graphics, two operation conditions were considered: normal condition, i.e. steady-state and depicted in Fig. 7 (a) to (c); and abnormal condition, i.e. start-up and load variation Fig. 7 (d) to (f). Furthermore, the resonant frequency (f_o) was kept constant and the operation point of $f_o = f_s$ is highlighted in those plots. For normal operation and assuming a constant resonant frequency, it is noticed that the L_r and C_r does not affect the rms inductor current (see Fig. 7 (a)) and output voltage ripple (see Fig. 7 (c)). Nevertheless, the rms voltage on the capacitor (see Fig. 7 (b)) is minimized if the C_r value is the biggest possible. Under abnormal operation, if a small L_r and big C_r are chosen, the output voltage overshoot (represented in Fig. 7 (f)) and tank capacitor voltage overshoot (see Fig. 7 (e)) are minimized, whereas the inductor current overshoot is maximized (see Fig. 7 (d)), influencing negatively the capacitor lifetime. On the other hand, if a big L_r and small C_r are chosen, the inductor current overshoot is minimized, whereas the output voltage overshoot and the tank capacitor voltage overshoot are maximized, also influencing negatively the capacitor lifetime. Hence, to verify quantitavely the influence of L_r and C_r on the capacitor lifetime, all these graphics are combined, and a capacitor lifetime model based in L_r and C_r is obtained, as plotted in Fig. 8 (b). Similarly, the efficiency curve of the SRC in function of the L_r and C_r also plotted in Fig. 8 (a), by using the losses equations described previously.

$$L = L_o \cdot \left(\frac{V_{C_r}}{V_o}\right)^{-n} \cdot e^{\left[\left(\frac{E_a}{K_b}\right)\cdot\left(\frac{1}{T(i_{L(rms)}, i_{L(os)})} - \frac{1}{T_o}\right)\right]} \quad (9)$$

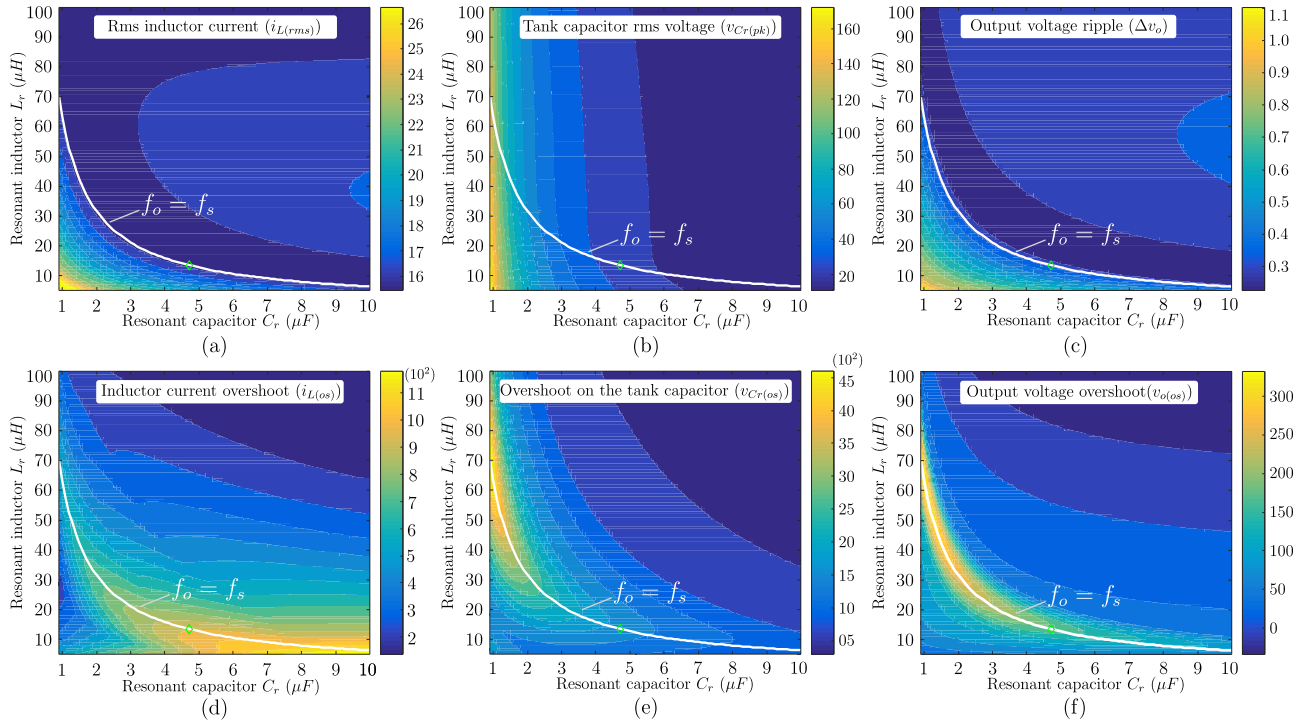


Figure 7. Current and voltage stresses (during normal and abnormal condiction) on the main components of the SRC on the as a function of the tank circuit parameters (L_r and C_r): (a) rms current on the resonant inductor ($I_{L(rms)}$), (b) rms voltage on the resonant capacitor, (c) output voltage ripple, all of them for normal operation condition (steady-state). Similarly: (a) current overshoot on the resonant inductor, (b) voltage overshoot on the resonant inductor, (c) output voltage overshoot, all of them for abnormal operation.

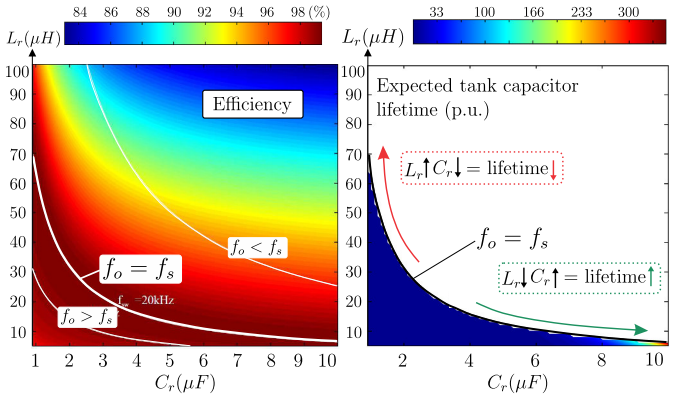


Figure 8. Graphic analysis of the SRC efficiency (a) and resonant capacitor lifetime (reliability) (b) in terms of the L_r and C_r.

$$V_{Cpk}(C_r) = \frac{I_i}{8 f_s C_r} \tag{10}$$

$$i_{L(rms)}(L_r, C_r) = i_{Lpk} \cdot \sqrt{\frac{\gamma}{2}} = i_{Lpk} \cdot \sqrt{\frac{1}{2 \cdot f_s \sqrt{L_r C_r}}} \tag{11}$$

$$L(V,T) \sim L(i_{L(rms)}, i_{L(os)}, V_{Cpk}) \sim L(L_r, C_r) \tag{12}$$

C. Tank Circuit Parameter Selection

Analyzing the efficiency curve and lifetime capacitors presented in 8, it is noticed that the efficiency reaches its maximum value when $f_o = f_s$, as expected and already discussed. In the graphic 8 (b), the capacitor lifetime is longer for lower values of L_r and higher values of C_r. Therefore, to extended as much as possible the capacitor lifetime, the inductance L_r must be as smaller as possible, while the capacitance C_r should be as big as possible, keeping f_o constant. The minimum inductance value possible is constrained by the leakage inductance of the transformer. Therefore, only the leakage inductance of the transformer should be used and no external inductance is added.

V. Prototype Implementation and Experimental Results

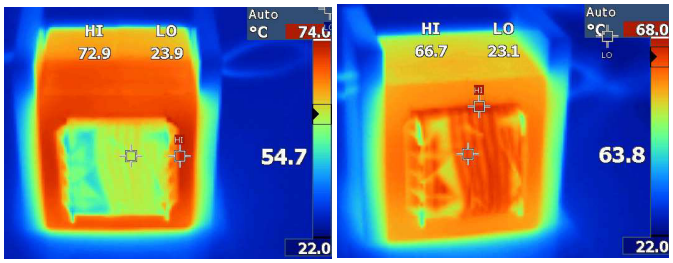
In order to evaluate the converter performance experimentally and verify the presented design procedure, a prototype was built and tested. The main specifications are shown in Table I. The transformer implementation, converter construction and the final results are discussed.

A. Medium-Frequency Transformer Implementation and Tests

The MFT was implemented according to the design presented in Section III. As a result of the design, 2 cores E65/32/27 from EPCOS/TDK were used in parallel and the physical implementation is described in Table IV. The implemented transformer was experimentally evaluated and its main parameters, as well as the core losses and wire losses were obtained. The intrinsic parameters of the transformer are shown in Table VI.

Table VI
Measured Parameters of the MFT

Leakage inductance	$L_{leak} = 13.5\mu H$
Winding resistance (primary and secondary)	$R_{wire} = 86m\Omega$
Magnetizing inductance	$L_m = 7.93mH$
Core Losses	$R_{core} = 309.5k\Omega$
Total Losses	$P_{MFT} = 56.4W$



(a) (b)

Figure 9. Temperature obtained during the open-circuit and short-circuit test on the transformer: (a) core losses (open-circuit test) and (a) wire losses (shot-circuit)

In order to evaluate more carefully the power dissipated on the transformer, the open-circuit and short-circuit tests were performed according to [32]. From these tests, it is possible to separate the core losses from the wire losses, and to obtain the wire losses decomposition in ac and dc losses. The total losses of the MFT are presented in Table VI, while the losses distribution is depicted in Fig. 14. As can be observed, the wires are responsible for most of the losses (61%), where 22% of this value are the ac losses, due to the proximity effect. The expected ac losses is between 20% and 30% of the total wire losses. Thus, the obtained value is in accordance to the analysis, showing a good implementation of the transformer.

Finally, the temperature were measured in both tests, in order to check the temperature rise due to the core and wire losses individually. The results are presented in Fig. 9 and it is observed that the temperature is well below the maximum of $100°C$.

B. Final Prototype Assembly

Once the resonant frequency and the transformer leakage inductance are chosen, the resonant capacitance (C_r) can be selected. As discussed in section IV, the resonant inductance should be the transformer leakage inductance, then $L_r = 13.5\mu H$. To select the resonant frequency, the dead-time between the semiconductors of the same leg should be taken into account. Moreover, a resonance frequency slight above the switching should be selected, so that the inductor current can have a small zero-time, allowing the semiconductors to deplete their stored charge. Therefore, assuming a dead-time of $1\mu s$, the resonance frequency of $f_o = 21.7kHz$ is select. To obtain this value, the resonant capacitance should be $C_r = 4.3\mu F$. Thus, the C_r is implemented by using 9 capacitors of $330nF$ and 2 capacitors of $680nF$ connected in parallel.

For the semiconductor selection, those devices that provide the minimum conduction losses are selected, since the

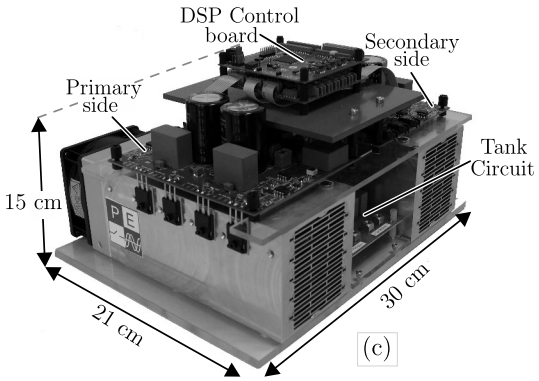


Figure 10. Implemented 10 kW SRC converter hardware prototype (mechanical dimensions: 300 mm x 210 mm x 150 mm).

switching losses are neglected, due to soft-switching operation of the converter. For the primary side, two SiC-MOSFET were considered during the design (see Table II). The SiC MOSFET C2M0025120D is select to be used on the prototype implementation, because of its lower $R_{DS(on)}$ and consequently lower power dissipation. For the secondary side, IGBT and a SiC diode are used in parallel as discussed in Section III. The silicon IGBT IHW40N120R3 optimized for lower conduction losses is chosen. For the SiC diode selection, two options are provided in Table II and they perform similarly from the conduction losses viewpoint. However, the device C4D20120D presents a lower reverse recovery charge, and for that reasons it is selected for the prototype implementation.

C. Experimental Results

The experimental results were obtained for the converter operating in steady-state at nominal load, where the main waveforms were saved and the thermal behavior of the main components was evaluated by a temperature measurement system. Additionally, the converter efficiency and the losses distribution on the components are verified and discussed. The results are summarized from Fig. 11 to Fig. 14.

The main waveforms obtained experimentally for the converter operating in steady-state in nominal condition (i.e. 10 kW, 600 V to 700 V) are shown in Fig. 11. In Fig. 11 (a), the primary side voltage (v_p), the voltage over the resonant capacitor (v_{Cr}) and the tank circuit current (i_{Lr}) are presented. Fig. 11 (b) shows the current and voltage on the primary side semiconductor (s_1), where soft-switching operation is verified. As expected, the primary side semiconductors turn on in ZVS and turn off in ZCS. The commutation detail is also depicted in Fig. 11 (b). Similarly, the current and voltage on the secondary side diode (d_1) are presented in Fig. 11 (c), where ZCS operation during turn-on and turn-off is observed. Therefore, these results confirmed that the switching losses can be completely neglected during the design of the converter.

The temperatures of the transformer, the primary and secondary side semiconductors for the converter operating at nominal condition are depicted in Fig. 12. As can be noticed, the hotspot on the transformer has an temperature of 89°C, which is below the maximum of 100°C defined by the design.

Finally, the efficiency curve in function of the output power is shown in Fig. 13, while the losses distribution is presented in Fig. 14. The efficiency curve was obtained experimentally using the high performance power analyzer WT1800 from *Yokogawa* (basic power accuracy of 0.02%). As can be seen, the converter has achieved a peak efficiency of 98.61% at a power level of around 4 kW, while at nominal load the converter has achieved around 98.1% of efficiency. This results confirmed the optimum design of the converter, as well as the high potentiality of the SiC technology in this application.

Evaluating the losses distribution depicted in Fig. 14, the transformer is responsible for most of the losses, with 39% of the total power dissipated by the converter. Furthermore, the conduction losses of the secondary side semiconductor (around 34% of the total losses) are higher than the primary side ones, that are responsible for 24% of the total power dissipated by the converter. This effect is also noticed in Fig. 12, in which higher temperatures are observed in the secondary side devices (around 86°C, see Fig. 12(c)) with respected to the primary side semiconductors (see Fig. 12 (a)). In spite of having higher rms current, the primary side semiconductor dissipate less power, when compared to the secondary side semiconductor. It is explained by the fact that the SiC-MOSFETs presents a very low $R_{DS(on)}$, contributing significantly to the conduction losses reduction and making this device very suitable for such application.

D. Fault Tolerance Capability Evaluation

In order to verify the reliable operation of the converter and proof its capability to handle faults, as described in Section IV, the converter is tested under fault condition. A short-circuit is imposed on the primary side semiconductors s_2 and the dynamic behavior of the converter is observed. For safety reasons, the test was performed considering an input voltage of 350 V and output voltage of 500 V. The dynamic behavior during the fault on semiconductor s_2 is presented in Fig. 15, showing that the converter remains operational after the failure. Moreover, the converter provides a constant output voltage (500 V) even after the fault. This result attests the effectiveness of the topology shown in Fig. 5, demonstrating the ability of the SRC to handle fault.

Besides to being a highly efficient converter, as demonstrated by the efficiency curve in Fig. 13, the SRC using the proposed design approach is also presented as a highly reliable solution, as demonstrated in this section. Hence, the SRC meets all the requirement of the smart transformer system.

VI. Conclusion

The series resonant converter is a promising topology to be used as building block of the modular dc-dc stage of smart transformer. In this system, high efficiency and reliability are extremely desired. In this paper an optimum design of a series resonant converter to obtain not only high efficiency, but also high reliability was proposed.

To obtain high efficiency, the losses were carefully modeled and a minimization procedure is performed. Additionally, SiC-MOSFETs with very low on-resistance were used on the

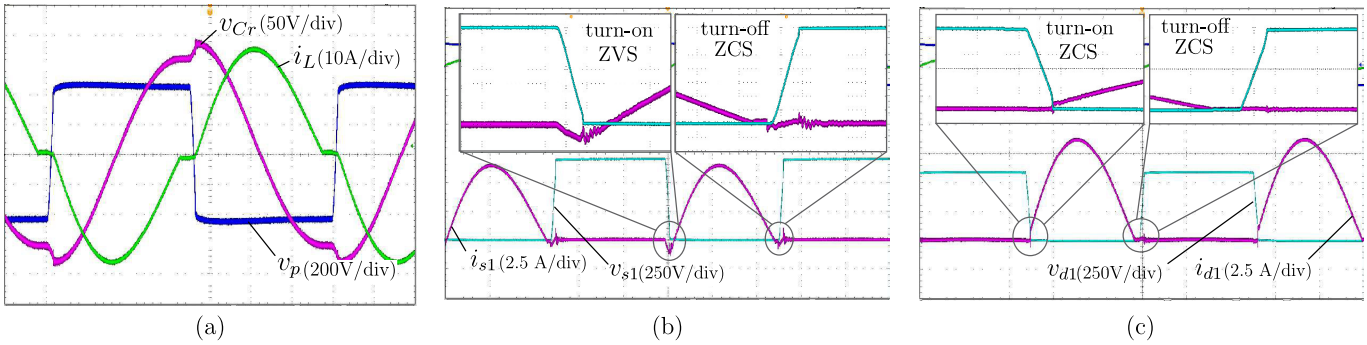


Figure 11. Experimental results obtained in steady-state: (a) primary side voltage (v_p), voltage over the resonant capacitor (v_{Cr}) and tank circuit current (i_{Lr}), (b) current and voltage on the primary side semiconductor (s_1), (c) current and voltage on the secondary side semiconductor (d_1).

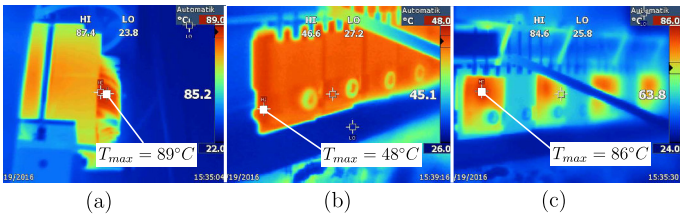


Figure 12. Thermal behavior of the main components of the converter operating under nominal condition: (a) MFT (hotspot: 85.2°C), (b) primary side semiconductor (SiC-MOSFETs) (hotspot: 48°C), (c) secondary side semiconductor (SiC-diodes) (hotspot: 86°C).

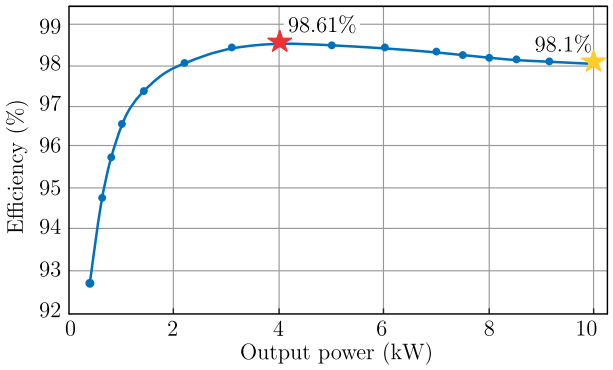


Figure 13. Efficiency curve of the converter as a function of the output power obtained experimentally.

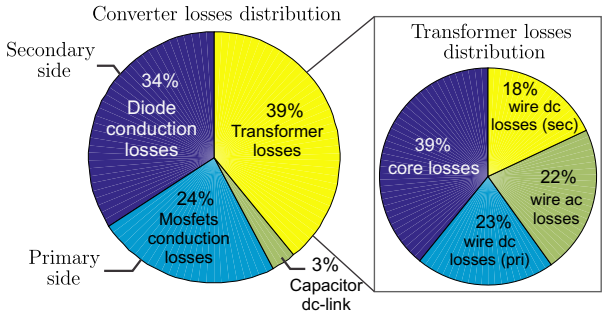


Figure 14. Losses distribution on the main components of the converter and also the losses distribution on the MFT.

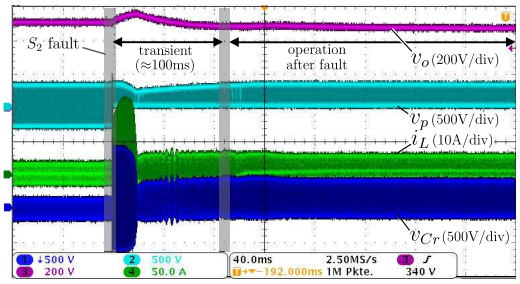


Figure 15. Experimental result of the SRC under a fault condition. Dynamic behavior of the converter during the short-circuit fault of the semiconductor s_2.

primary side, while SiC diode associated with IGBT were used on the secondary side of the converter.

To increase the reliability, the two most critical devices are analyzed: the primary side semiconductor and the resonant capacitor. To avoid fault on the switch, a fault-tolerant SRC topology was proposed to be used instead the classic one, avoiding the interruption of the system in faulty case. To extend the reliability of the resonant capacitor, its lifetime model is used and a trade-off between the resonant tank parameters selection is found. As a results, the resonant tank circuit should have a high capacitance value (C_r) and small inductance value (L_r) (for a given resonant frequency). Following this procedure, the capacitor lifetime is extended. In that case, only the leakage inductance of the transformer should be used as the resonant inductor, and no additional components should be included.

Finally, experimental results were provided for a 10 kW prototype. The converter was tested under fault condition, demonstrating its high reliable characteristic. Furthermore, the proposed converter has obtained a peak efficiency of 98.61%, proving the validity of the presented design.

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REFERENCES

[1] B. X. Nguyen, D. M. Vilathgamuwa, G. H. B. Foo, P. Wang, A. Ong, U. K. Madawala, and T. D. Nguyen, "An efficiency optimization scheme

for bidirectional inductive power transfer systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6310–6319, Nov 2015.
[2] A. Berger, M. Agostinelli, S. Vesti, J. A. Oliver, J. A. Cobos, and M. Huemer, "A wireless charging system applying phase-shift and amplitude control to maximize efficiency and extractable power," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6338–6348, Nov 2015.
[3] M. Petersen and F. Fuchs, "Load dependent power control in series-series compensated electric vehicle inductive power transfer systems," in *European Conference on Power Electronics and Applications (EPE-ECCE Europe)*, Aug 2014, pp. 1–10.
[4] N. Liu and T. G. Habetler, "Design of a universal inductive charger for multiple electric vehicle models," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6378–6390, Nov 2015.
[5] I. O. Lee, "Hybrid pwm-resonant converter for electric vehicle on-board battery chargers," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3639–3649, May 2016.
[6] N. Shafiei, M. Ordonez, M. Craciun, C. Botting, and M. Edington, "Burst mode elimination in high-power llc resonant battery charger for electric vehicles," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1173–1188, Feb 2016.
[7] D. Jovcic and B. Ooi, "High-power, resonant dc/dc converter for integration of renewable sources," in *IEEE Bucharest PowerTech*, June 2009, pp. 1–6.
[8] D. Jovcic and L. Zhang, "Lcl dc/dc converter for dc grids," *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2071–2079, Oct 2013.
[9] X. Sun, Y. Shen, Y. Zhu, and X. Guo, "Interleaved boost-integrated llc resonant converter with fixed-frequency pwm control for renewable energy generation applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4312–4326, Aug 2015.
[10] C. Meyer and R. De Doncker, "Design of a three-phase series resonant converter for offshore dc grids," in *42nd IAS Annual Meeting. Conference Record of the 2007 IEEE Industry Applications Conference*, Sept 2007, pp. 216–223.
[11] T. Lazzarin, O. Custodio, C. C. Motta, and I. Barbi, "An isolated dc-dc converter with high-output-voltage for a twta," in *International Telecommunications Energy Conference (INTELEC)*, Sept 2014, pp. 1–7.
[12] M. Liserre, G. Buticchi, M. Andresen, G. D. Carne, L. F. Costa, and Z. X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46–58, Summer 2016.
[13] D. Dujic, G. Steinke, E. Bianda, S. Lewdeni-Schmid, C. Zhao, and J. Steinke, "Characterization of a 6.5kv igbt for medium-voltage high-power resonant dc-dc converter," in *Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 1438–1444.
[14] C. Zhao, D. Dujic, A. Mester, J. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer:medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, July 2014.
[15] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio dc/dc converter cells for phase-modular solid-state transformers," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 5021–5029.
[16] J. Wang, A. Q. Huang, W. Sung, Y. Liu, and B. J. Baliga, "Smart grid technologies," *IEEE Industrial Electronics Magazine*, vol. 3, no. 2, pp. 16–23, June 2009.
[17] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W. K. Ling, and J. Lam, "Computer-aided design and optimization of high-efficiency llc series resonant converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3243–3256, July 2012.
[18] T. LaBella, W. Yu, J. S. . Lai, M. Senesky, and D. Anderson, "A bidirectional-switch-based wide-input range high-efficiency isolated resonant converter for photovoltaic applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3473–3484, July 2014.
[19] T. LaBella and J. S. Lai, "A hybrid resonant converter utilizing a bidirectional gan ac switch for high-efficiency pv applications," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3468–3475, Sept 2014.
[20] Y. Nakakohara, H. Otake, T. M. Evans, T. Yoshida, M. Tsuruya, and K. Nakahara, "Three-phase llc series resonant dc/dc converter using sic mosfets to realize high-voltage and high-frequency operation," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 4, pp. 2103–2110, April 2016.
[21] M. Liserre, M. Andresen, L. Costa, and G. Buticchi, "Power routing in modular smart transformers: Active thermal control through uneven loading of cells," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43–53, Fall 2016.
[22] L. Costa, G. Buticchi, and M. Liserre, "A fault-tolerant series-resonant dc-dc converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 900–905, Feb 2017.
[23] E. Ribeiro, A. Cardoso, and C. Boccaletti, "Fault-tolerant strategy for a photovoltaic dc-dc converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 3008–3018, June 2013.
[24] K. Afridi, "Resonant and soft-switching techniques in power electronics," Department of Electrical, Computer and Energy, Colorado University, Colorado, USA, Lectures Note, 2014.
[25] H. Wu, T. Mu, X. Gao, and Y. Xing, "A secondary-side phase-shift-controlled llc resonant converter with reduced conduction loss at normal operation for hold-up time compensation application," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5352–5357, Oct 2015.
[26] W. G. Hurley, E. Gath, and J. G. Breslin, "Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 369–376, Mar 2000.
[27] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Computers in Power Electronics, 2002. Proceedings. 2002 IEEE Workshop on*, June 2002, pp. 36–41.
[28] M. K. Kazimierczuk, *High-Frequency Magnetic Components*. Wiley Publishing, 2009.
[29] "Power technology roadmap: Trends 2012-2017," Power Sources Manufacturers Association, USA, Report, 2013.
[30] W. s. Choi, S. m. Young, and D. w. Kim, "Analysis of mosfet failure modes in llc resonant converter," in *INTELEC 2009 - 31st International Telecommunications Energy Conference*, Oct 2009, pp. 1–6.
[31] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters: An overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.
[32] I. Villar, "Multiphysical characterization of medium-frequency power electronic transformers," Ph.D. dissertation, Swiss Federal Institute of Technology Lausanne, 2010.

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