Digital Object Identifier (DOI): 10.1109/ECCE.2017.8095991
Print ISBN: 978-1-5090-2999-0

IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017

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Suggested Citation

V. Raveendran, G. Buticchi, A. Mercante and M. Liserre, "Comparison of voltage control methods of CHB converters for power routing in smart transformer," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 1652-1658.

Comparison of Voltage Control Methods of CHB Converters for Power Routing in Smart Transformer

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***Abstract*—For Smart Transformers (ST), reliability is one of the major problems when compared to the traditional low-frequency transformers. Modular ST with advanced control algorithms could increase the reliability compared to the non-modular solutions. This could be achieved by distributing differently the power among the cells depending on their aging. This unequal power transfer is a challenge for Cascaded H-Bridge converters (CHB). ST based on a CHB rectifier with different capacitor voltage balancing schemes are analyzed in the paper. The goal is to evaluate the best scheme for unequal power transfer while maintaining the dc-link voltages constant. The paper focuses on validating the operating power unbalance limits of each cell of the modular system for unbalanced power transfer while maintaining the voltage balance in the medium voltage dc-link stage. The power unbalance limits are established with analytical calculations and verified through simulations and experiments.**

I. Introduction

The increasing proliferation of renewable energy resources and distributed generation demands novel power transfer technologies in the electric grid. Solid-state transformer (SST) is a promising solution for flexible grid connectivity and power flow control with power electronic converters. A smart transformer (ST) can be defined as an SST with minimum two stages and enhanced ac and dc connection management capability through advanced identification and control algorithms [1]. The conventional low-frequency transformer offers very high reliability with decades of operation and low maintenance requirement compared to the SST. The "smart transformer" challenges the conventional SSTs by increasing reliability through advanced control strategies like "power routing" introduced in [1]–[3]. By unequal power distribution, power dependent failure mechanisms can be delayed to lower the maintenance requirements.

This paper focuses on the challenges of implementation of power routing concept in ST comprised of Cascaded H bridge (CHB) for MVAC to MVDC stage. The main challenge in control of CHB is the dc-link capacitor balancing. In literature, strategies to balance the capacitor voltages for unequal loads have been studied [4], [5]. But the goal of this paper is to identify the best suitable voltage balancing scheme for the intentional unequal power sharing and to identify the power unbalance limits. A comparison study between a PI-based Voltage Balancing Controller and a Modulator-Embedded Voltage Balancing Algorithm is performed to evaluate the range of power unbalance between each H-bridge without losing the voltage balance. For the MVDC to LVDC stage of ST, a Quadruple Active Bridge (QAB) is used. CHB and QAB configuration offers flexibility to route the power through the modules unequally.

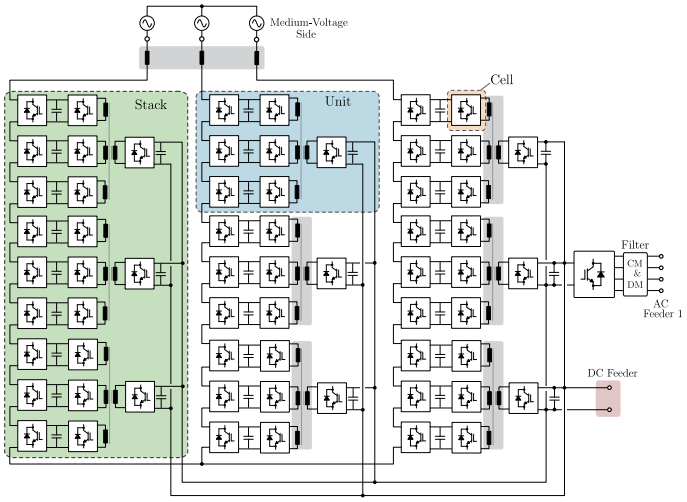

Fig. 1: ST with CHB and QAB.

The power routing concept is presented in section II. ST modeling focusing on analytical comparison of CHB voltage balancing schemes is discussed in section III. Section IV shows the simulation results of the voltage balancing methods, and the experimental results from the CHB and QAB prototype are presented in section V. Finally, the conclusion is given in section VI.

II. Power Routing Concept

The challenge of the ST in the distribution grid is to provide a high quality of service, ensuring no blackouts for the connected loads. For this reason the availability of the system needs to be maximized. Furthermore, in competition with the traditional transformer, which has expected lifetimes of 60 - 80 years, a long lifetime of the ST needs to be ensured. For this reason, it is proposed to design a modular system in which the health of the components is monitored and which replaces aged components. The failure mechanisms for different components are different and in some cases, depend

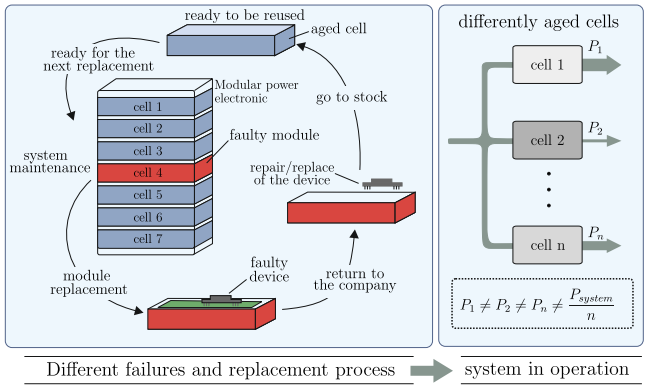

Fig. 2: Replacement cycle in the repairable modular ST and uneven loading based on remaining estimated lifetime [1].

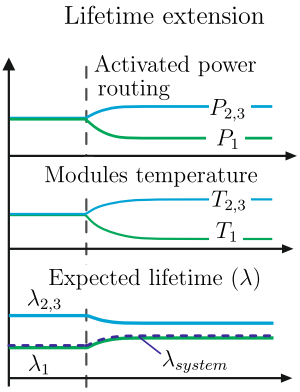

Fig. 3: Demonstration of the power routing concept for Lifetime extension [1].

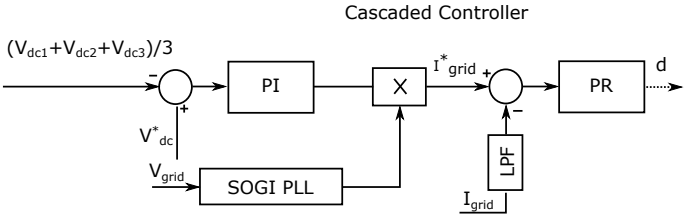

Fig. 4: Single phase CHB controller structure with resonant current controller.

on processed power. If cells in a modular system fail, they are sent to maintenance and replaced. Thus the replaced cells have different ages compared to existing ones. Power routing is a strategy to delay the failures dependent on processed power by shifting the power distribution according to the aging of the cells in a modular architecture. Thus the more aged cell process less power than others and hence the power dependent deterioration can be delayed. This concept is illustrated in Fig. 2 for the ST.

The aging and wear out of semiconductor switches is dependent on the junction temperature fluctuations as shown in (1), which expresses the number of thermal cycles to failure N_f in dependence of the junction temperature's thermal swing ΔT, the average junction temperature $T_{j,av}$ and the device dependent parameters a_1, n and a_3. Remarkably, the parameter $a_3 \approx 5$, which makes the number of cycles to failure, consequent the lifetime of the power semiconductors very sensitive to variations [6].

$$N_f = a_1(\Delta T)^n \cdot e^{\frac{a_3}{T_{j,av}}} \tag{1}$$

The expected lifetime λ can be calculated from the lifetime models based on damage accumulation [7]. By routing the power within the system, the junction temperature is influenced and the stress is reduced for the unloaded parts of the system, while the stress for higher loaded parts is increased. The Fig. 3 demonstrates this concept for an ST unit comprised of a seven level CHB and QAB with unevenly aged cells. Here, the power processed by each H-bridge is shown as P_{1-3} with corresponding temperatures T_{1-3} and expected lifetime λ_{1-3}. When the power routing strategy is activated, the expected lifetime of the total system increases by the reduced loading of the more aged cell. The next section deals with the controller design for CHB and QAB with power routing capability while ensuring normal operation of the ST.

III. ST Modeling and Control

This section deals with the controller design for CHB and QAB focusing on the power unbalance limits of CHB. For the analysis, without the loss of generality, a scaled down prototype is considered. ST consists of a seven level CHB modular topology for the rectification of ac voltage of 1.1kV to dc voltage of 2.1kV with each dc-link capacitor having 700V. The QAB converts the 700V dc to 600V dc with high frequency transformer isolation. Compared to the dual active bridge (DAB), QAB has reduced number of transformers and modules with the possibility to exchange power among the modules. Therefore, QAB is an attractive solution for Power Routing with a semi-modular topology [8].

Parameter	Value
Input ac voltage, V_{grid}	$1100V$
Power rating, P	$15kVA$
Line inductance, L	$3.8mH$
MV dc-link voltage, V_{dc}	$700V$
LV dc-link voltage, V_L	$600V$
CHB switching frequency, f_{sw}	$10kHz$
QAB switching frequency, f_{qab}	$20kHz$

TABLE I: System parameters

A. Control of CHB

The CHB rectifier stage controls the input power factor, input ac current and regulates the 700V dc-link voltage. Several control strategies have been discussed in literature [4], [9]–[11]. The CHB rectifier connected to QAB is shown in Fig. 1. The CHB topology is derived by connecting n H-bridges in series and thereby supplying n dc loads. The main challenge of CHB topology is the regulation of dc-link

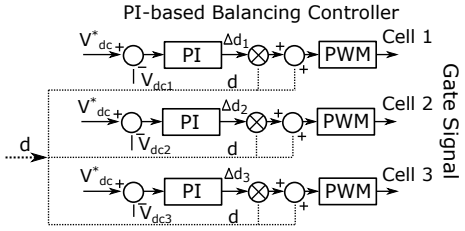

Fig. 5: PI-based voltage balancing controller

voltages when delivering unequal power through each cell and many solutions have been proposed in the literature extensively [4], [5]. The current and voltage control is performed by the cascaded controller based on Proportional-Resonant (PR) current controller and Proportional Integral (PI) voltage controller. The outer loop maintains the total capacitor voltage to the reference value and the voltage controller output is given to the inner loop as current reference. The inner loop current controller maintains the power factor and sinusoidal shape of the input current. The PR controller can be easily implemented to achieve zero phase and amplitude steady-state error. The Fig. 4 shows the controller structure with cascaded controller for providing reference duty cycle. The tuning of cascaded controller for CHB rectifier has been discussed in literature [12], [13].

The maximum power that can be processed by the converter is given by (2).

$$P_{tot\_max} = \hat{V_{grid}} \frac{\sqrt{(\sum V_{dci})^2 - \hat{V_{grid}}^2}}{2\omega L} \tag{2}$$

where $\omega = 2\pi f_{sw}$. But the power distribution among H-bridges is determined by the modulation scheme. For the implementation of power routing, two methods are analyzed in this paper. (I) Conventional PI balancing controller and (II) Modulator-Embedded Voltage Balancing algorithm (hybrid modulation) [5].

PI-based Voltage Balancing Controller: The Fig. 5 shows the configuration of capacitor voltage balancing with PI controllers for each H-bridge. The idea is to adjust the duty cycle of individual H-bridges to balance the dc-link capacitor voltage according to the power fed to the load. The transfer function to design the capacitor voltage balancing is given in (3), where i_d is the direct axis component of converter current, *C* is the dc-link capacitance and *R* is the equivalent resistance of the dc-dc converter connected to the dc-links.

$$G_{b(s)} = \frac{i_d}{\sqrt{2}(Cs + \frac{1}{R})} \tag{3}$$

Assuming the rectifier is operated without over-modulation, the maximum power delivered by each cell is given as [4]:

$$P_{max}^{'} = p \frac{V_{dc}^*}{\hat{V_{grid}}} \sqrt{1 - \left(\frac{\omega L i_{grid}}{3V_{dc}^*}\right)^2} \tag{4}$$

The minimum power delivered by a cell in an n cell system is given as:

$$P_{min}^{'} = P - \sum_{1}^{n-1} P_{max,n}^{'} \tag{5}$$

The maximum power and minimum power that is delivered by an individual H-bridge without dc-link voltage unbalance with the parameters given in Tab.I is obtained as 6.75kW and 1.5kW respectively. The nominal power delivered by each dc-link is $5kW$.

Modulator-Embedded Voltage Balancing Algorithm: The aim of modulator-embedded algorithm is to synthesize ac voltage V_{grid} using the dc-link voltages V_{dci}. The switches of H-bridge are operated in 3 modes to generate $+V_{dci}$, $-V_{dci}$ and 0 voltage at the input. The capacitor voltages are sorted in ascending order and only one H-bridge operates in PWM mode at any instant. The rest of the cells are charged, discharged or operated in zero mode according to the current direction to follow the grid voltage. The cascaded controller maintains the total dc-link voltage. Since only one cell operated in PWM mode at any instant, device switching losses are reduced. The maximum and minimum power that can be delivered by each H-bridge is given by the (6) & (7) respectively [5].

$$\begin{aligned} P_{max} = \frac{\hat{i_{grid}}}{\pi}[&\int_{\theta}^{\gamma} \hat{V_{grid}} sin(\alpha) sin(\alpha - \theta) d\alpha \\ &+ \int_{\gamma}^{\pi-\gamma} V_1 sin(\alpha - \theta) d\alpha \\ &+ \int_{\pi-\gamma}^{\pi} \hat{V_{grid}} sin(\alpha) sin(\alpha - \theta) d\alpha] \end{aligned} \tag{6}$$

$$\begin{aligned} P_{min} = \frac{\hat{i_{grid}}}{\pi}[&\int_{0}^{\theta} \hat{V_{grid}} sin(\alpha) sin(\alpha - \theta) d\alpha + \\ &\int_{\beta}^{\pi-\beta} \hat{V_{grid}} sin(\alpha - V_1 - V_2) sin(\alpha - \theta) d\alpha] \end{aligned} \tag{7}$$

$$\gamma = sin^{-1}\left(\frac{V_1}{\hat{V_{grid}}}\right) \tag{8}$$

$$\beta = sin^{-1}\left(\frac{V_1 + V_2}{\hat{V_{grid}}}\right) \tag{9}$$

$$\theta = sin^{-1}\left(\frac{\omega L \hat{i_{grid}}}{\hat{V_{grid}}}\right) \tag{10}$$

where $V_1 < V_2 < V_3$ and they represent the sorted dc-link voltages. The power limits calculated are given as $P_{max} = 8.3kW$ and $P_{min} = 0.7kW$ for the system with parameters in Tab. I.

B. Control of QAB

QAB has been introduced as the dc-dc converter stage of ST in [8]. The Fig. 1 shows the QAB configuration with four active bridges with three bridges connected to the MV side and one connected to the LV side. In this paper, phase shift modulation is used to transfer power between the MV and LV

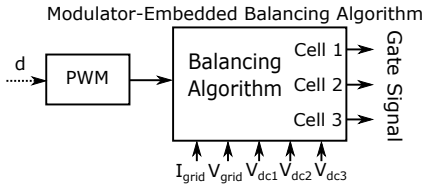

Fig. 6: Modulator-embedded voltage balancing algorithm.

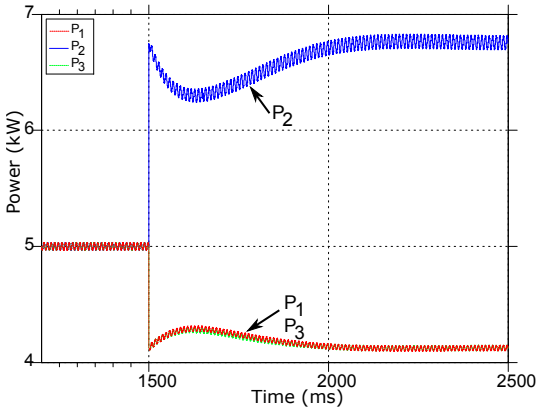

Fig. 7: PI-based balancing : power processed by each H-bridge

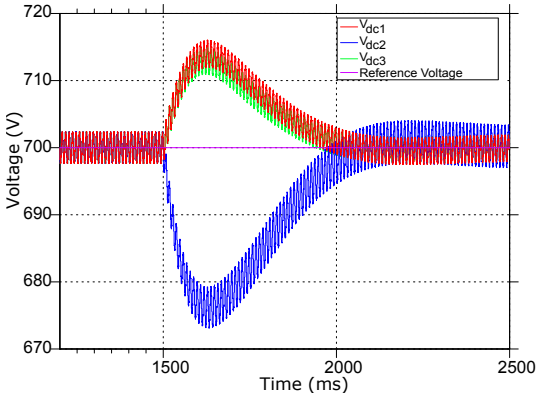

Fig. 8: PI-based balancing : CHB dc-link voltages

side [14]. The operating principle of QAB is similar to that of the DAB and thus the power equation of the DAB can be extended to QAB. The average power transferred from port j to port k in the QAB is given as:

$$P_{jk} = \frac{V_j{}' V_k{}'}{\omega L_{jk}} \phi_{jk} \left(1 - \frac{|\phi_{jk}|}{\pi}\right) \tag{11}$$

Where $j, k = \{1, 2, 3, 4\}, j \not\equiv k, \omega = 2\pi f_{sw}$. f_{sw} is the switching frequency, ϕ_{jk} and L_{jk} are the phase shift and equivalent inductance between the ports j and k and V_j and V_k represent dc-link voltages.

The control objectives are the regulation of LV dc-link voltage and to individually control the power transferred from MV side to LV side through each cell. The MV dc-link voltages are controlled by the CHB control loop. A control structure composed of a LV dc-link voltage controller coupled with

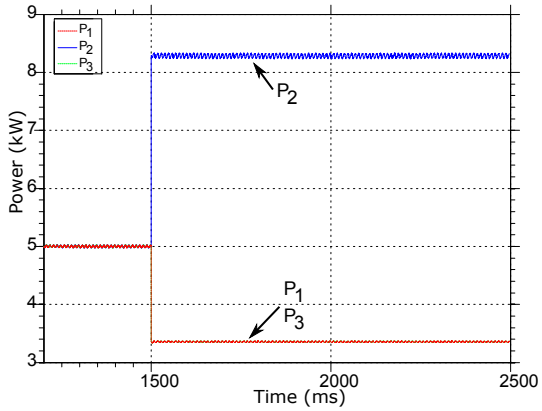

Fig. 9: Modulator-embedded balancing algorithm : power processed by each H-bridge

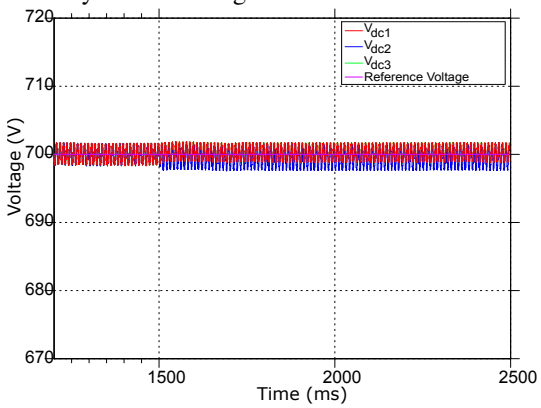

Fig. 10: Modulator-embedded balancing algorithm : CHB dc-link voltages

power control loop provides the phase shift values to each cell [8].

IV. Simulation

The control scheme developed for the CHB with cascaded PI and PR controllers with modulator-embedded balancing algorithm is implemented in SIMULINK PLECS environment and tested. The analytical power limits calculated in section III are validated for both PI and modulator-embedded balancing algorithm voltage balancing methods. The dc-link voltages and the power processed by each H-bridges for PI and modulator-embedded balancing algorithm are shown in Fig. 8 - 9 at the theoretical power limits for each method. It is clear that the response and power unbalance capability of the modulator-embedded balancing algorithm method is better than that of conventional PI based balancing method. However, the Total Harmonic Distortion (THD) of the input grid current for modulator-embedded balancing algorithm method is twice that of the PI balancing scheme.

The Tab. II shows the power unbalance limits obtained by simulation for the two methods where P is the system input power, 15kW. The lower and upper power unbalance limits are the power processed by one H-bridge when the voltage control is not able to maintain the reference dc-

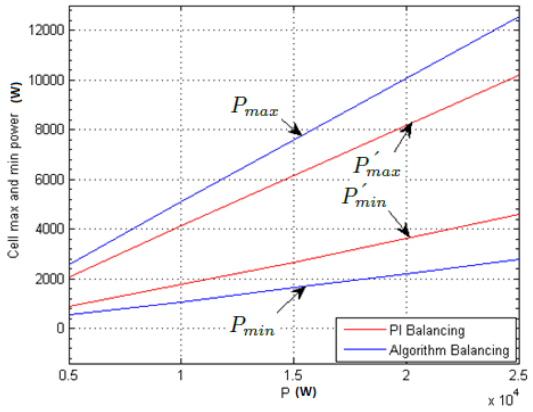

Fig. 11: The minimum and maximum power limits by the both voltage balancing methods in section III.

Method	P_{max}	P_{min}	THD
PI-based Voltage Balancing Controller	$0.44P$	$0.12P$	3.1%
Modulator-embedded Voltage Balancing Algorithm	$0.55P$	$0.06P$	6.1%

TABLE II: Comparison of power unbalance limits for two methods by simulation at input power $P = 15kW$

link voltage. The simulation results are in accordance with the analytical results and the modulator-embedded balancing algorithm provides an extended range of power unbalance, but the THD is much higher than the conventional PI based on PWM modulation. Therefore, a larger filter inductance is required for the modulator-embedded balancing algorithm method to comply with the grid code. The Fig. 11 shows the minimum and maximum power limits of both methods over the range of input power 5kW to 25kW. It is evident that the modulator-embedded voltage balancing algorithm has a wider range of operation without unbalance in the dc-link voltages compared to the PI-based control method.

V. Experimental Validation

The seven level CHB rectifier prototype coupled with the QAB is developed with IGBTs and controller is implemented in Freescale MPC5643L microcontroller as illustrated in Fig. 12. Each MV cell of the ST is composed of one H-bridge of the CHB and one MV active bridge of QAB. The three

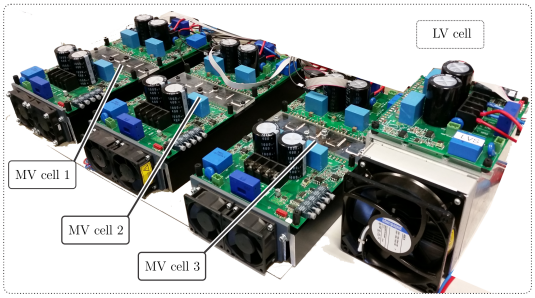

Fig. 12: CHB and QAB Prototype

H-bridges of the CHB are connected to the three MV bridges of QAB and the LV active bridge is connected to a resistive load. The scaled down prototype to test the power unbalance limits of the CHB has the parameters listed in Tab. III. The two voltage balancing methods, Modulator-embedded Voltage Balancing Algorithm and PI-based Voltage Balancing Controller, are implemented on the microcontroller and are tested to find the maximum and minimum power unbalance limit for each cell.

Parameter	Value
Input ac voltage, V_{grid}	$230V$
Power rating, P	$2.1kVA$
Line inductance, L	$3.8mH$
MV dc-link voltage, V_{dc}	$130V$
LV dc-link voltage, V_L	$115V$
CHB switching frequency, f_{sw}	$10kHz$
QAB switching frequency, f_{qab}	$20kHz$

TABLE III: Experimental parameters

The results of the PI-based Voltage Balancing Controller is shown by Fig. 13 and Fig. 14. The Tab. IV shows the power processed by each cell of the CHB. To find the maximum power processed by each cell without voltage unbalance and over-modulation, the power delivered by one cell is increased by controlling the phase-shift of QAB. The total input power is kept constant. The Fig. 13 shows the seven level converter voltage output and the balanced three dc-link capacitor voltages when delivering the power given by Tab. IV. When the power through one cell is further increased, the controller enters into over-modulation. This is verified by using a flag for checking over-modulation as shown in Fig. 14 and the grid current becomes non-sinusoidal. Thus the maximum power unbalance limit of each bridge without entering over-modulation is experimentally calculated. The minimum power unbalance limit is experimentally verified by operating the two H-bridges at the $P_{max}^{'}$.

The modulator-embedded voltage balancing algorithm is tested in the CHB and QAB experimental setup to validate the power limits. The power processed by each cell of the CHB is given in Tab. V. The power delivered by one cell is increased by controlling the phase-shift of QAB while the total input power is kept constant. The Fig. 15 shows the grid current and the balanced three dc-link capacitor voltages when delivering the power given by Tab. V. When the power through one cell is further increased, the controller enters into over-modulation and the dc-link voltages start to deviate from the reference value. The experimentally calculated maximum power without unbalance and the analytically calculated values are given in Tab. V and are in agreement. The minimum power limit is also experimentally verified and the results are given in Tab. V.

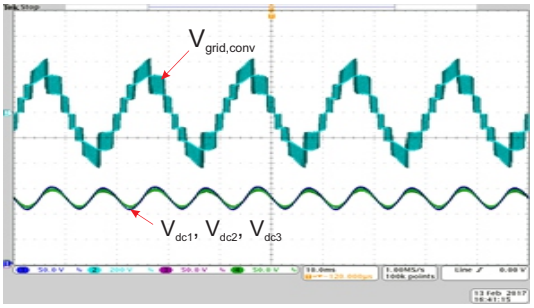

Fig. 13: CHB with PI-based voltage balancing controller V_{dci} - $(50V/\text{div})$, $V_{grid,conv}$ - $(200V/\text{div})$

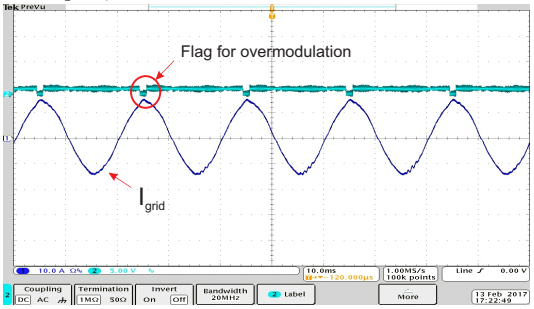

Fig. 14: CHB with PI-based voltage balancing controller I_{grid} - $(10A/\text{div})$

Parameter	Power	Power (in terms of P)
P_1	$820W$	$0.39P$
P_2	$640W$	$0.30P$
P_3	$640W$	$0.30P$
$P_{max,analytical}$	$839W$	$0.40P$
$P_{max,experimental}$	$820W$	$0.39P$
$P_{max,analytical}$	$420W$	$0.20P$
$P_{max,experimental}$	$460W$	$0.22P$

TABLE IV: Processed power of CHB for PI-based voltage balancing controller

VI. Conclusion

A comparison of dc-link voltage balancing methods for CHB rectifier in ST application is presented in this paper. The analysis focuses on the limit of power unbalance possible in each H-bridge so that different powers can be processed by each cell, while maintaining the dc-link voltages equal to the reference value. Analytical power limits for both methods are discussed and are validated through simulations and experiments. The results show that the modulator-embedded balancing algorithm offers extended power unbalance limits while maintaining the dc-link voltages at their reference. However, the higher THD is the drawback for the modulator-embedded balancing algorithm scheme.

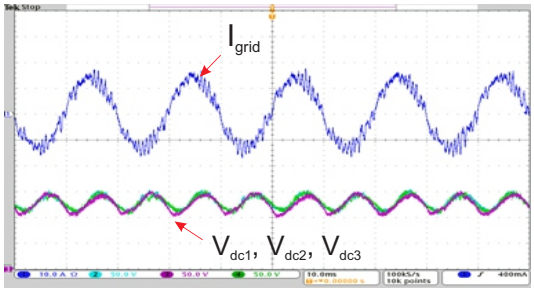

Fig. 15: CHB with modulator-embedded voltage balancing algorithm V_{dci}-$(50V/\text{div})$, I_{grid}-$(10A/\text{div})$

Parameter	Power (W)	Power (in terms of P)
P_1	1020	$0.48P$
P_2	540	$0.26P$
P_3	540	$0.26P$
$P_{max,analytical}$	$1038W$	$0.49P$
$P_{max,experimental}$	$1020W$	$0.48P$
$P_{max,analytical}$	$276W$	$0.13P$
$P_{max,experimental}$	$300W$	$0.14P$

TABLE V: Processed power of CHB for modulator-embedded voltage balancing algorithm

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