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Active Thermal Control of a DC/DC GaN-based Converter

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***Abstract*—Advanced packaging technologies in Wide band gap devices like GaN avoid wire bonds thereby making the solder joints more susceptible to thermo-mechanical fatigue. To limit the thermal cycling induced failures, an active thermal control scheme using a two step gate driver for a buck converter is presented in this paper. In contrast to the active thermal control techniques employing variation of switching frequency, this method does not alter the converter operation point. A simple temperature control algorithm which actively varies the device losses is proposed. The effectiveness of the control scheme has been validated through experimental results.**

I. Introduction

GaN devices in comparison with IGBTs do not have tail current during turn off and have very low or zero reverse recovery charge. Due to the superior material properties they are able to switch much faster in the order of *ns* and also have very low values of R_{dson} (Drain-source on resistance). Despite several advantages, there are challenges related with GaN transistors, i.e. the Electro Magnetic Interferences (EMI) related to the fast switching in hard switching applications, the necessary minimization of stray inductance and the design of the package [1] which should also take into account the temperature. The smaller footprint packages along with the higher thermal resistance offered by GaN over Silicon could mean thermal management to be critical. Also articles on Solder fatigue induced reliability issues have been discussed as well [2] [3]. For the near future, it is assumed that GaN transistors will replace Si-based IGBTs and MOSFETs in some applications in the voltage range between $600\text{V}-1{,}000\text{V}$ [1].

One means of failure is the thermo-mechanical fatigue in the connection point between different materials. Components with different thermal expansion coefficients are subjected to different thermo-mechanical stresses. When such components which are in contact are subjected to thermal cycling, the consequent mechanical fatigue could result in failure. When using GaN transistors, with AD-HOC developed compact packaging which minimizes possible mechanical fatigue [4], these stresses may shift from within the device to the PCB solder contacts. This happens because of the absence of wire bonds and solder contacts within the packaging [5]. GaNSystems GaNPX [4] packaging makes use of copper-filled vias to make contacts to the device. The vias also function as heat exchange from within the device to the case, thereby reducing the thermal resistance values of these packages. In short, large magnitude thermal cycling can introduce considerable thermo-mechanical fatigue to those mechanical contacts with different thermal expansion coefficients. Care should be taken to assess the effect of thermal cycling and the components that are affected by thermal cycling.

Thus with the aim of reducing thermal stress in power modules, various active thermal control algorithms had been proposed in [6] - [7]. Normally, converters are designed to limit the losses, thermal cycling reduction can be achieved, as an example, by increasing the losses when the load is decreasing. This comes at the expense of the overall efficiency, so a tradeoff should be found for a proper system design. Using GaN devices the switching losses and conduction losses will be relatively lower compared to Si based power devices. As a result, a smaller compromise on overall efficiency for improved reliability seems highly interesting for applications which require longer lifetimes (such as Space, Electro-Mobility, Highly critical power converter applications).

Several active thermal control schemes are discussed in [8]. The solutions include thermal cycling reduction by control of switching frequency, implementing different modulation schemes etc. to actively control losses in a device [9], [10]. Study on impact of thermal interface material (TIM) on GaN devices at higher power losses is presented in [11], which shows that GaN device junction temperatures are highly influenced by TIM and thermal management network.

In this paper an active gate driver developed in [12] which can control device voltage and/ current slew rates (dv/dt and/ di/dt) is used for implementing active thermal control. By controlling the device turn-on rise time (t_r), it is possible to vary the GaN device turn-on switching losses needed for active thermal control. The schematic of the proposed active thermal control using this two-step gate driver scheme for a DC/DC GaN Buck converter is shown in Fig. 1. This paper is divided into the following sections: Section II explains the effect of thermal cycling on causing solder fatigue [2] [13] to the solder profiles. Section III introduces the two step gate driver concept with experimental test results showing the loss control possibilities using this gate driver. Section IV discusses the Active thermal control scheme implemented here using the developed two step driver. Here the temperature measurement and thermal control algorithm used will be covered. Section V provides experimental results obtained using the Two step gate driver for Active thermal control.

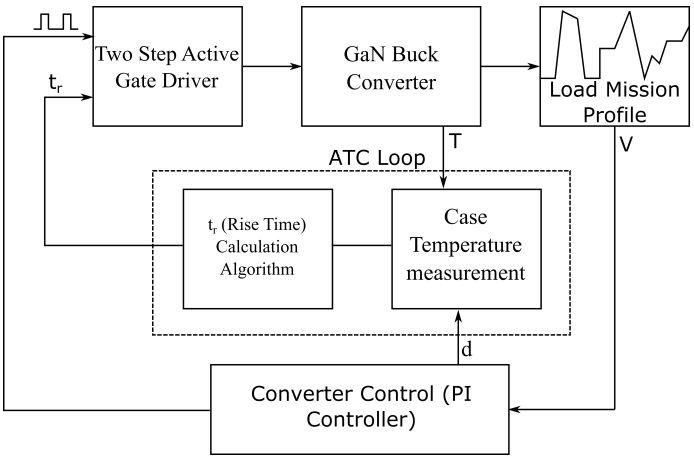

Figure 1: Active thermal control scheme

In this paper, active thermal control using a two step gate driver developed in [12] for a GaN Enhancement Mode High Electron Mobility Transistor (E-HEMT) GS66508T, from GaN Systems [14] is analyzed. The suitability of this active gate control method is investigated for the GaN E-HEMT for a single pulse. The effect of the developed active gate driver unit on slew rate control, switching and conduction losses are presented briefly from [12]. The simulation results from [12] show that the active thermal control using the two step driver can be used to reduce the variation of the case temperature. This in turn means control on the solder temperature profile.

II. Effect of thermal cycling in GaN

Some power converter applications undergo vigorous power cycling which can result in thermal cycling of the power devices. Considering the power device losses as the source of thermal cycling, the first step is to detect various thermo-mechanical fatigues introduced by this mechanism. The device used here is GaN Systems GS66508T configured as a half-bridge buck converter in a 4-layer PCB for optimized layout and performance. The gate driver with two-step driving scheme is also implemented in the same. GaN devices presently available in the market comes in WLCS (wafer level chip-scale packaging) [5], GaNSystems GaNPX packaging [4], in TO-247 and TO-220 packages cascode GaN HEMTs, PQFN packages etc.. and some other packages for easier replace and fit option from Si based converters. The thermo-mechanical fatigue introduced varies from package to package. A brief on the effects of various packaging technologies are presented below.

A. Wafer level Chip scale packaging:

Features:

- Extremely low inductance
- Absence of wire bonds
- Consists of solder bars to make contacts
- Extremely small foot print
- Package enables very fast switching transients
- No plastic encapsulation
- Larger CTE (coefficcient of thermal expansion) mismatch between die and PCB

As mentioned before thermo-mechanical fatigue arises between two materials having large difference of coefficient of thermal expansion. From the above features of the package it can be deduced that the thermo-mechanical fatigue is no longer something that may be present inside the device. But the thermal stress is now present externally between the solder joints and the PCBs to which chips are soldered onto [13]. The resulting solder joint strain due to thermal cycling may be represented by the following Eq. 1 [13]:

$$\varepsilon = \Delta\alpha \cdot \Delta T(DNP/t) \tag{1}$$

where where ε is the shear strain in the solder joint, $\Delta\alpha$ is the CTE mismatch between the die and the PCB, ΔT is maximum temperature change during a cycle, DNP is the distance of the solder joint from the neutral point of the die, and t is the solder joint standoff height. Thus it is clear from the above equation that the magnitude of strain is proportional to the thermal cycling magnitude. The resulting shear stress/strain energy may cause cracked solder joints reducing the lifetime of the power converters. The best fit equation for the resulting number of cycles to failure for the power devices is given by the following Eq. 2 [13]:

$$N_f = (260 cycles).E_s^{-2} \tag{2}$$

This explains the necessity of active thermal control even with WLCS packages owing to the possibility of solder fatigue.

B. GaNPx Packaging:

This is the technology of packaging used by GaNSystems in their commerical GaN products at the time of writing this paper. The features include:

- Extremely low inductance
- No wire bonds
- Copper filled vias to make contacts
- Extremely small foot print
- Package enables very fast switching transients
- The package consists of FR4 and glass layers
- CTE mismatch is less between device FR4 layers and PCB but exists between solder joints to both

Solder fatigue due to thermal cycling is still present between the solder joints from device to PCB as explainable based on Eq. 1 and Eq. 2.

C. TO 247, TO 220 packages

These are some of the very common commercially used packages for Si devices and hence have the benefit of easy replacement structures for conventional power converter PCB layouts. Hence these are highly attractive. However the additional lead inductance introduced by these packages significantly limit the performance capability of GaN semiconductors. The effect of common source inductance (CSI)

becomes a dominant factor at very fast transients [15]. This is applicable in case of SiC and GaN devices. The absence of separate power and gate current return paths could mean higher susceptibility to CSI induced turn on of the devices at very fast transients di/dt. In addition the low gate threshold voltage level makes GaN devices even more susceptible to CSI effects. Provision of separate source pins for gate and power (kelvin connections); provision of negative gate voltage as off-state etc. could help minimize these effects.

Some commercially available TO 247 and TO 220 packages have Cascode GaN structures and hence have wire bonds for connection between GaN and cascoded Si. This means the problem of thermo mechanical fatigue is present within device packaging. Thermo-mechanical fatigue induced reduction of lifetime studies have been performed in [3].

Some active thermal control schemes and their effects on IGBTs are presented in [16] and [17].

D. Other packages

In addition to these there exists also gate driver integrated GaN power ICs from Texas instruments and Navitas semiconductors. Also VisIC technologies have patented special ALL-Switch System in Package (SIP) GaN switches which have extremely low R_{dson} values compared to similar rated GaN devices from other manufacturers. Here the study is focused on WLCS and GaNPx packaging examples. For the experimental study the device used is GS66508T from GaNSystems [14].

III. Two-Step Gate Drive Unit

The considered two-step gate voltage shape for turn-on and turn-off is shown in Fig. 2. By adjusting the gate voltage shape parameters T_{on} , T_{off} and V_{on}, the charge delivered to the gate can be varied. $V_{\text{g,nom}}$ represents the manufacturer specified nominal Gate source Voltage for the GaN device.

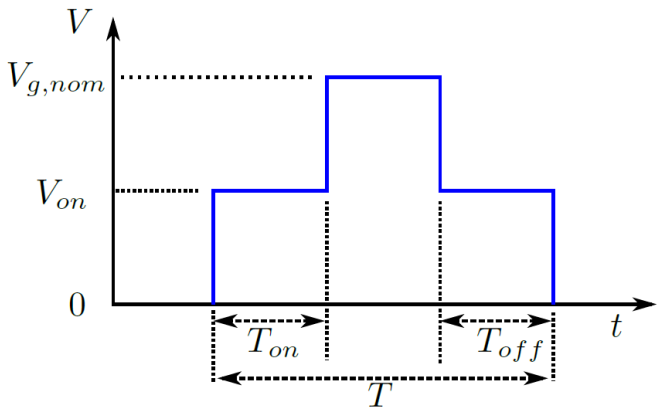

Figure 2: Waveform of the two-step gate driver

The two-step gate driver designed and developed in this work is for GS66508T (top side cooled GaN device from GaNSystems). Using similar terms to define parameters for a MOSFET, it can be seen that the gate plateau voltage (Vg, pl) is at 3.0 V and the gate threshold voltage (Vg, th) is at 1.3

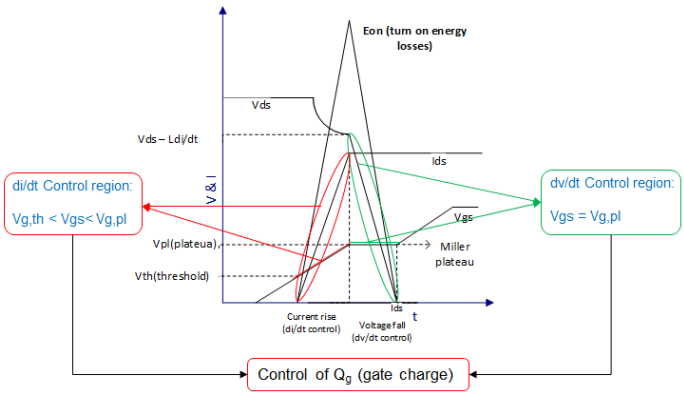

Figure 3: Commutation of Wide band gap devices

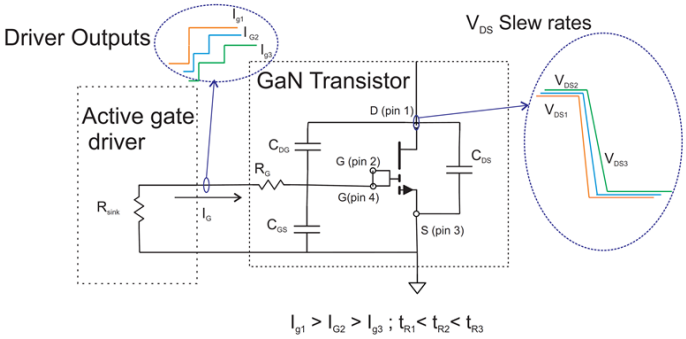

Figure 4: Gate charging control and effect

V. This means that during turn-on gating $(Vgs > 0)$, when $Vg, th < Vgs < Vg, pl$, the current (I_{ds}) in the device rises up to the steady state value. Similarly, for the duration when $Vgs = Vg, pl$ (miller plateau region), the device will undergo voltage (V_{ds}) fall or transient. This is shown in Fig. 3 [12].

The turn-on time or voltage fall is determined basically by the amount of charge $(Q_{g,pl})$ supplied by the gate driver during miller-plateau. Thus by limiting $Q_{g,pl}$, the device turn-on voltage transition may be controlled. As can be seen in Fig. 3 the voltage transition phase begins only after $V_{gs} = V_{g,pl}$. Referring to Fig. 2, thus the first step (V_{on}) of the 2-step driver is set to 3.0 V. The second step voltage is always set at typical gate voltage desired which is 6.0V for GS66508T. The time T_{on} (interval between steps) can now be adjusted to vary the charge Q_g delivered during device turn-on. This helps to adjust dv/dt during turn-on by adjusting only T_{on}. The concept with different steps and their effect on V_{ds} is shown in Fig. 4. During turn-off the voltage setting $V_{off} = V_{g,pl}$ will not have an effect since the gate discharge for V_{ds} rise begins only after V_{gs} falls below $V_{g,pl}$ [12].

Similarly, by setting V_{on} between $V_{g,th}$ and $V_{g,pl}$ during turn-on, the device turn-on current transient time (di/dt) can be regulated. And by setting voltage step V_{on} between $V_{g,th}$ and $V_{g,pl}$ during turn-off, the voltage V_{ds} fall time during turn-off can be adjusted by varying T_{off}. The oscilliscope readings of two cases of T_{on} = 46ns and 32ns are shown in Fig. 6 and Fig. 7 which shows turn-on times of 38.8ns and 22.8ns.

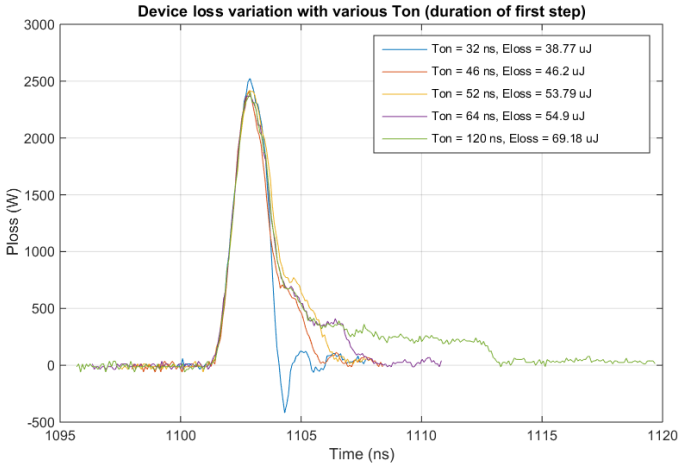

Figure 5: Results showing Energy loss variation with various Ton($I_{DS} = 6\,A$, $V_{DS} = 300\,V$)

Table I: Energy loss vs T_{on}

Energy loss (μ)J	**T_{on}(ns)**
38.77	32
46.2	46
53.79	52
54.9	64
69.18	120

This means it is possible to actively control the losses GaN GS66508T using the developed 2-step gate driver. The control on conduction loss is explained in [12]. From the Fig. 8, the possible loss control regions and required type of losses can be determined.

The experimental results from this section prove that the 2-step gate driver is capable of actively introducing switching and conduction losses if the parameter T_{on} is adapted online.

IV. Active Thermal Control for the DC/DC Converter

The impact of the active thermal control on a bidirectional single-phase DC/DC converter is briefly presented here. The topology of the buck converter is shown in Fig. 9. The block diagram of active thermal control implemented is shown in Fig. 1. The measured case temperature is used to determine the required T_{on} to limit the thermal cycling. The idea is to increase the switching losses and/ conduction losses when the output power cycles rapidly, in order to prevent large magnitude temperature cycling (ΔT). Thus by introducing small amount of device losses the idea is to limit the magnitude of temperature cycling(ΔT) within a particular margin to improve lifetime as per Eq. 2.

The losses of the DC/DC converter and therefore its temperature variation can be controlled by the two step gate driver. The first possibility is the application of the active gate driver to increase the turn-off and turn-on switching losses of V_1 when there is a very large drop in device power dissipation.

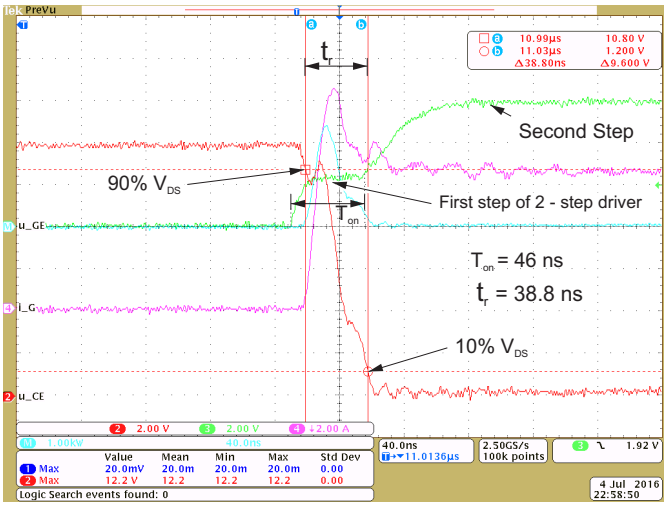

Figure 6: Device Turn-on characteristics for T_{on} = 46ns, (Green - Gate Voltage, Red - V_{DS} (need to scale by multiplying by 25 - 300V to 0V), Maroon - Device current (0A to 6A), sky blue - Turn-on switching energy loss)

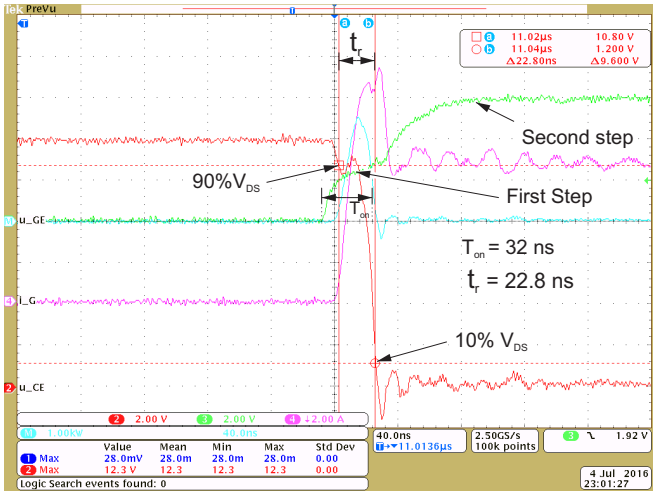

Figure 7: Device Turn-on characteristics for T_{on} = 32ns, (Green - Gate Voltage, Red - V_{DS} (need to scale by multiplying by 25 - 300V to 0V), Maroon - Device current (0A to 6A), sky blue - Turn-on switching energy loss)

The conduction losses of V_1 in Fig. 9 during the time period can be controlled by proper selection of the gate voltage level. The conduction losses of V_2 (being a GaN transistor) during free wheeling operation can be modified by an adjustment of the gate voltage level again similar as in synchronous rectifiers.

Despite the increase of the overall losses which implies an over all reduction of the efficiency, the reduced thermal stress on the power converter could balance this drawback. Applying the two-step gate voltage approach, it is possible to adapt either the turn-on and turn-off switching losses, the conduction losses

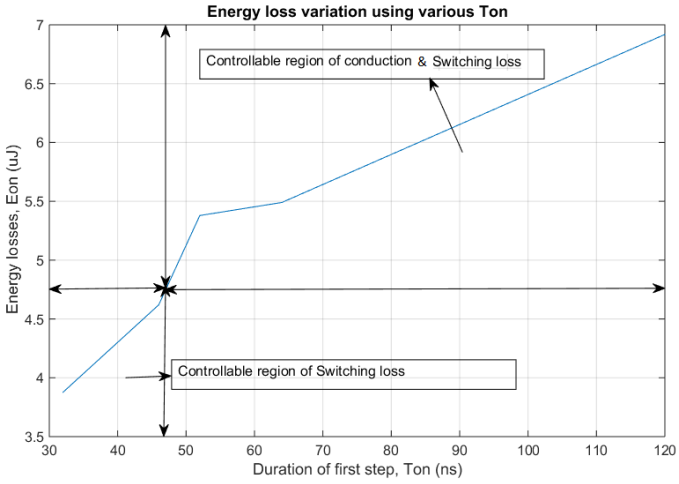

Figure 8: Energy loss controllable regions with various Ton ($I_{DS} = 6\,A$, $V_{DS} = 300\,V$)

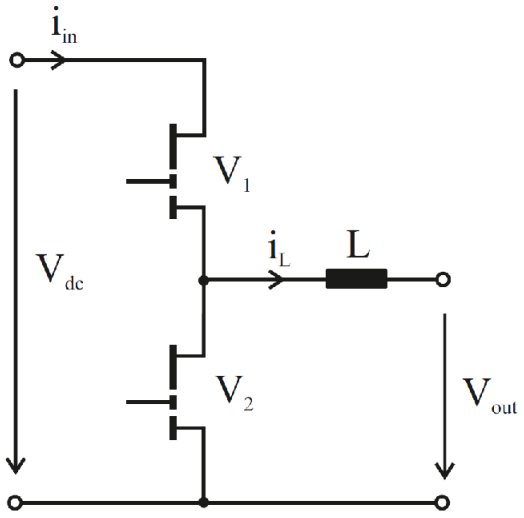

Figure 9: DC/DC buck converter

or both. The experimentally measured energy losses can be used to simulate the junction temperature in PLECS and the possibilities of reducing the thermal cycles can be understood. The simulation results and methods are discussed in [12]. At lower power levels, the switching losses of V_1 are increased by 1.5 to 2 times so as to limit the magnitude of thermal cycling within a predefined temperature range.

The simulations are ideal in the fact that only one type of loss (conduction or switching) is introduced at a time. However from the laboratory results the losses introduced due to the two step gate driver is such that above a certain duration of first step (T_{on} = 48ns) (from Fig. 8), both switching and conduction losses are introduced/increased simultaneously.

The device thermal cycling can be controlled with the aim of reducing the thermal stress on solder. The developed two-step gate driver unit and half-bridge in which the proposed active thermal control can be implemented is shown in Fig. 10.

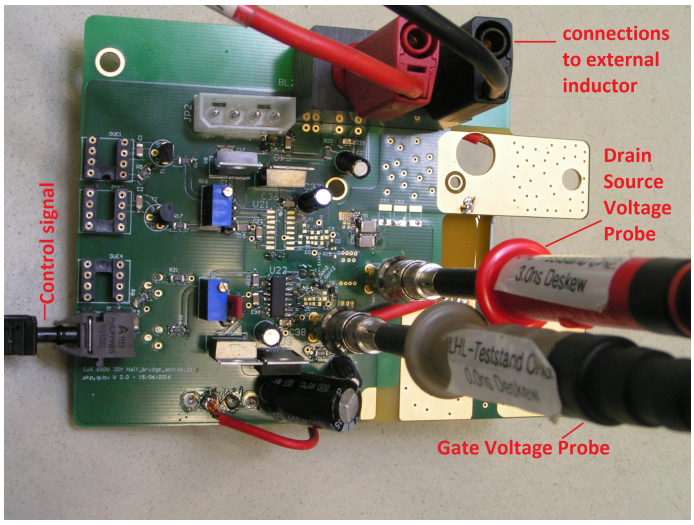

Figure 10: Developed two-step gate driver unit and GaN HEMTs in half-bridge configuration

Temperature and T_{on} Estimation for Active thermal control

One means for active thermal control is to use the load current measurement in the control loop [16], [17]. The RC time constants are in the range of *ms* which means the change in case temperature gets reflected after a certain time period from the load change. Hence the load current information can be used to determine the magnitude by which the losses need to be introduced into the device for active thermal control.

With the objective of limiting the thermal cycling of solder temperature, it is not necessary to determine the absolute value or rate of change of junction temperature. It is sufficient to determine a quantity which is proportional and has fast transient responses compared to solder temperature variations. Here this could be the case temperature measurement. The limitation with relying on load current information is that additional measurement circuitry may be needed. The idea behind the two step gate driver is to introduce switching or conduction losses into the device without affecting the system operational point and component design. This means the load current remains the same although the device losses are changed. Hence the same load current can introduce different switching and conduction losses into the device. Thus the load current will not be a suitable feedback for closed loop Active thermal control using two step gate driver scheme. More over the methods employed using switching frequency variation for active thermal control affects the design and operation of passive components apart from the switches.

Hence the measure able quantity that the authors would like to propose and consider here would be the rate of change of case temperature ($\frac{dT}{dt}$). Irrespective of the operating point, for a specific change in device power dissipation (dW), the change in device temperature (dT) is fixed assuming that other

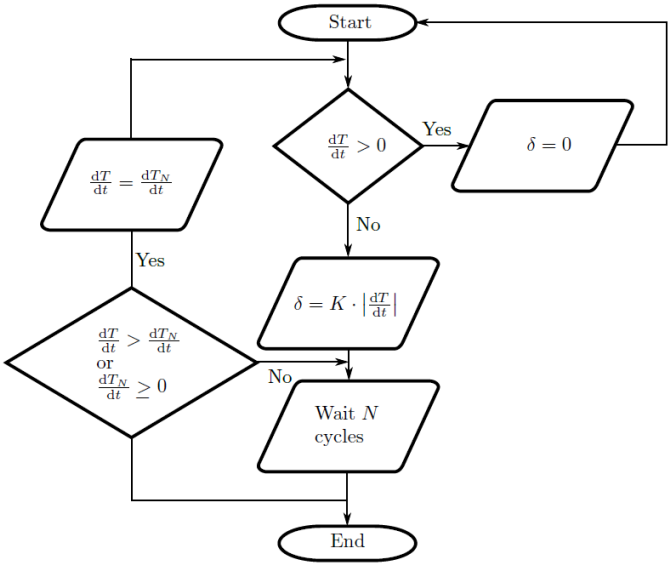

Figure 11: Active Thermal Control algorithm

quantities like the ambient temperature, humidity or other temperature influencing parameters remain unchanged. In this regard, it is then possible to determine the amount of additional losses that need to be introduced into the circuit to limit the temperature cycling of the device within a desired margin. This method doesn't require the load profile information in advance or measurement of the power converter load current or profile for temperature control. Since the control loop utilizes the temperature derivative, it inherently includes the feature of reducing the magnitude of active device loss dissipation to zero if the load variation or fluctuation slows down to nil (no load variation). The active thermal control algorithm implemented here is shown in Fig. 11. Hence by using just the temperature measurement system, it is possible to achieve closed loop active thermal control scheme.

For achieving this mode of temperature control, the energy loss variation measurements from the DPT (Double pulse test) setup is used. This helps to initially form a simple look up table like Table I that provides a relation between energy loss with the first step duration (T_{on}). This may be used to define the closed loop control system which varies the first step (T_{on}) according to the temperature variations in order to limit the temperature fluctuations. This is achieved with a proportional controller with $\frac{dT}{dt}$ as input and the T_{on} variation δ as output. The proportional constant K can be calculated with energy loss lookup table. The flowchart depicted in Fig. 11 shows the control algorithm execution. The algorithm waits for N cycles and then checks whether the new rate of change of temperature ($\frac{dT_N}{dt}$) has increased than the initial rate of $\frac{dT}{dt}$. If yes, it again increases the losses introduced otherwise it continues to execute until $\frac{dT}{dt}$ becomes non negative. The optimal cycling margin may be determined based on a proper trade off between the effect on converter efficiency and lifetime of the GaN devices.

V. Experimental Results

The case temperature measurement is carried out using Prosens temperature measurement system from Opsens. The experimental setup along with the power converter arrangement and the electronic load is shown in Fig 13. The parameters of the designed buck converter is given in Table II. The temperature measurement is given to the controller which generates suitable two step gate driver voltage according to desired temperature cycling limit. The associated thermal cycling of the case temperature without active thermal control for a particular load profile is shown by the blue trace in Fig. 12. The infrared thermal camera measurement shown in Fig. 14 has been used to validate the temperature measurement using Prosens. The case temperature fluctuates about 10 degrees. The amount of device power dissipation for a temperature cycling of 10 degrees can be determined. This information along with the energy loss look up table forms the basis for the active thermal control algorithm that is implemented.

The idea implemented in the micro controller and the corresponding decision algorithm loop formed by the active thermal controller has been discussed in the previous section and is shown in Fig. 11.

The percentage of losses to change the temperature cycling by a few degrees could be quite negligible for a system with large power in the range of kWs. Thus the compromise on efficiency for lifetime enhancement can be negligible.

The control signals to the gate driver are sent via optical fiber. The Active thermal controller algorithm has been implemented in the micro controller MPC5643L. The green

Table II: Buck converter parameters

Parameters	Values
Input Voltage	400 V
Output Voltage	200 V
Switching Frequency	100 kHz
Inductance, L	380 mH
Output Capacitor	1 μF

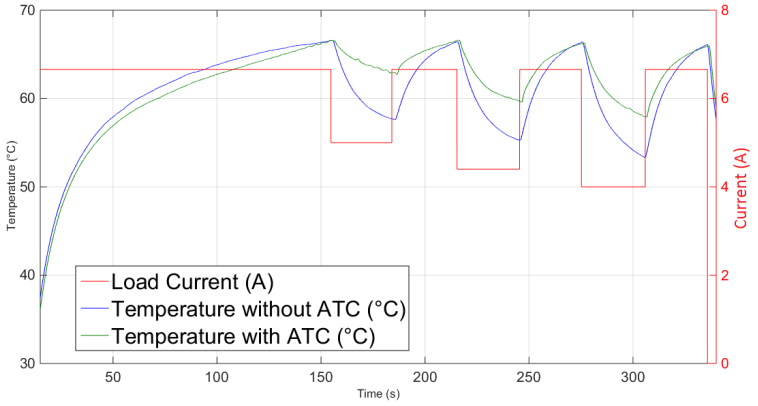

Figure 12: GaN Case temperature measurement with (green) and without (blue) active thermal control along with load current (red)

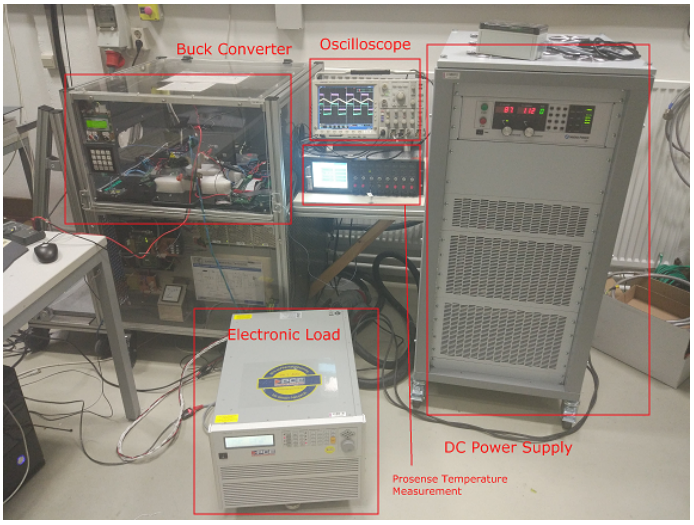

Figure 13: Measurement setup

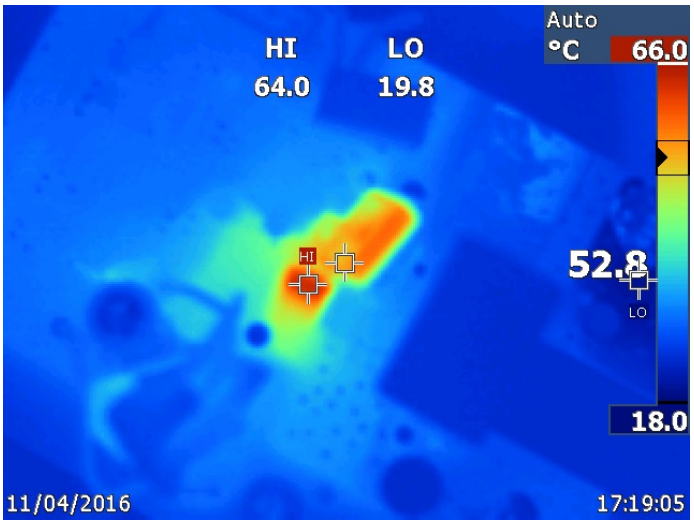

Figure 14: GaN case Temperature measurement with Fluke IR Thermal Camera

trace in Fig. 12 shows the results of the system for the same mission profile case with the active thermal control scheme implemented.

The subsequent reduction in the thermal cycling from a maximum of 13 °C (without active thermal control) to a maximum of 7 °C (with active thermal control) can be noted. This proves the effectiveness of the Active thermal control algorithm implemented here using the two-step gate driver concept. The capability of the micro controller to vary the duration of first step T_{on} in the range of *ns* further enhances the thermal controllability precision that can be achieved according to the measured data given in Table I.

VI. Conclusion

In this paper, a simple but effective active thermal controller for a GaN based DC/DC converter has been implemented and verified. The controller makes use of a two-step gate driver for actively modifying the device switching and conduction losses to minimize the solder thermal cycling. The proposed algorithm uses the rate of change of case temperature for actively controlling the device losses. Then the effectiveness of the proposed active thermal control scheme using the two step gate driver for GaN has been verified in the laboratory. This method of active thermal control scheme presents and shows the benefit of gate driver based thermal control which does not affect the switching frequency or modulation schemes of a system.

Acknowledgment

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