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Voltage Control Strategies of Smart Transformer Considering DC Capacitor Lifetime

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Abstract—Distribution grids unbalance challenges the DC-link of the Smart Transformer leading to higher ripples and then the lifetime of the DC aluminium electrolytic capacitors (AEC) is reduced. Additionally, dead time and nonlinearity characteristic of IGBT also may introduce ripple current in DC link, potentially decreasing the lifetime of AEC. Based on physical characteristic of AEC, the lifetime estimation of AEC is investigated considering aforementioned impacts. To suppress these impacts, an improved voltage control strategy that can reduce AEC current ripple and then preserve AEC lifetime is proposed. The theoretical analysis has been demonstrated by the simulation results.

Keywords—solid-state transformer, smart transformer, aluminum electrolytic capacitor, unbalanced load

I INTRODUCTION

With the increasing of the penetration of the distributed generator (DG), the conventional power transformer (CPT)-based distribution grid suffers voltage variation, poor power quality, and great demand variability [1], [2]. Recently, the smart transformer (ST), which is based on the solid-state transformer, uses communication and control to offer ancillary services for the distribution grid [3]–[6], as shown in Fig. 1.

Power converter system includes power semiconductors, DC capacitors and inductance components. Therefore, each component affects the whole system reliability. The leading manufactures could provide 20-year warranty for the power converter in renewable energy system. However, the average lifetime is 5-year for PV inverters [7], [8]. According to the recent investigation, the failure ratio is about 37% for photovoltaic inverters [7], [8] and is about 27% for the wind turbine converters [9], [10]. The failure ratio of electrolytic capacitor is 60%. Therefore, the lifetime estimation of the capacitor shall be correctly analyzed in every new application.

The lifetime of aluminium electrolytic capacitor (AEC) is mainly determined by the mission profiles and operation conditions (such as temperature, humidity, pressure, vibration, voltage and current) [3]. Even if the distribution grid planing is to keep three-phase load as balanced as possible, in practice three-phase grids are unbalanced. Therefore, the fundamental neutral-line current will degrade the lifetime of the AEC, significantly.

In this paper, the effects of the dead time and nonlinear characteristic of the power semiconductor as well as the unbalanced loads on the AEC are studied in detail to indicate AEC lifetime reduction. Unlike CPT, the ST can actively regulate the PCC voltage, and in turn an improved voltage control strategy is proposed to preserve AEC lifetime.

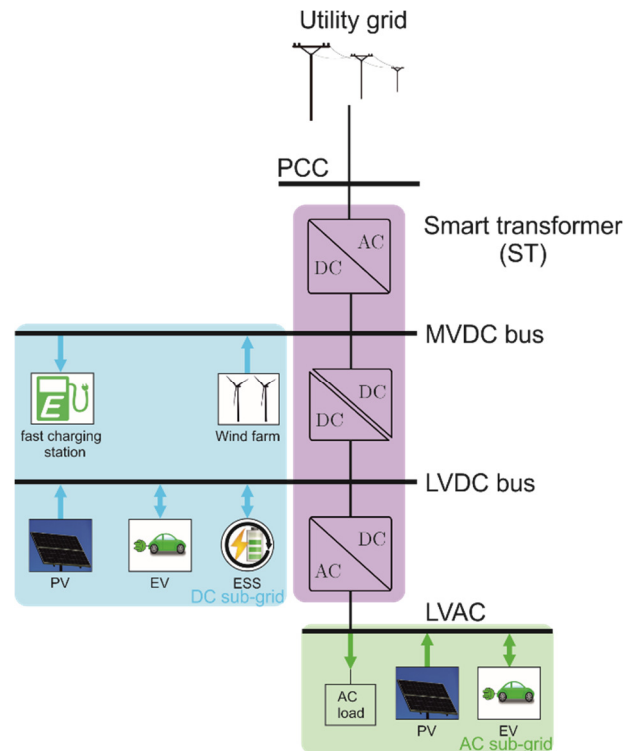


Fig. 1 Smart Transformer feeding hybrid grids.

The rest of this paper is organized as follows. The effect of the dead time and unbalanced loads on the ST DC capacitor current ripple is studied in Section II. In Section III, the lifetime model of the AEC is presented to estimate the AEC lifetime under three cases. An improved voltage control strategy is proposed to preserve AEC lifetime in Section IV. Section V concludes this paper.

II SMART TRANSFORMER

The configuration of the ST is a three-stage AC/DC/DC/AC system, as shown in Fig. 1. The MV AC/DC converter is

controlled as the conventional front-end rectifier, which can compensate MV grid harmonic and reactive power. The DC/DC stage offers both MV and LV DC buses. The LV DC/AC converter forms the voltage of distribution grid, where the ST must feed four wires because of the single-phase customer.

This paper only focuses on the ST LV side DC/AC converter voltage control and LV DC AEC lifetime improved. The detail structure of the ST LV side DC/AC converter is shown in Fig. 2. The neutral line is connected to the midpoint of the DC capacitors.

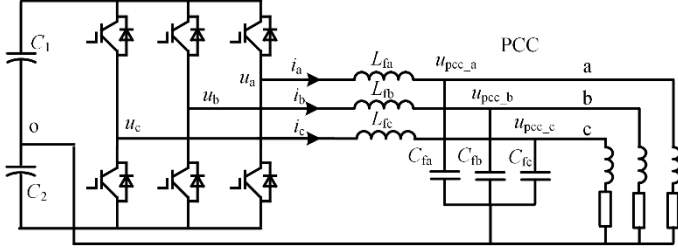


Fig. 2 Structure of the ST LV side converter

A. Control system of the ST

The overall control block diagram of the ST is shown in Fig. 3, where the outer loop controls three-phase PCC voltage and inner loop controls three-phase converter current.

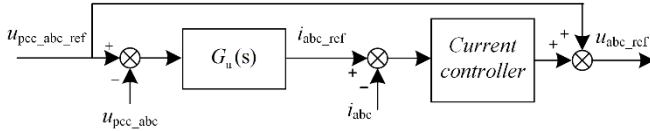


Fig. 3 Control block diagram of the ST

As the basic function of the converter is to form the PCC voltage, the DC-link performances are affected by loads, directly. Assumed three-phase load unbalanced, the three-phase current will be unbalanced and then voltage drop on the internal impedance of ST (LC filter) will be unbalanced as well. Consequently, the PCC voltage may be unbalanced if the voltage controller can not effectively control the negative and zero sequence component. In order to increase the controllability on the negative and zero sequence component, a proportional and resonant controller (PR) is adopted.

$$G_u(s) = k_p + k_r \frac{s}{s^2 + \omega_c s + \omega_0^2} \quad (1)$$

where ω_0 is the control signal frequency in rad., ω_c is the cutoff frequency in rad. k_p , k_i and k_r are the proportional, integral and resonant gains, respectively.

B. Effects of dead time and unbalanced loads

The dead time T_d is needed to avoid short-circuit of the converter leg. The dead time and nonlinearity characteristic of power semiconductor introduce voltage disturbance, which can be equivalent as a zero sequence voltage, resulting in disturbance current in neutral line. The neutral line current flows into DC capacitor directly, as shown in Fig. 2. Additionally, the nonlinear characteristics of the power semiconductor also introduce voltage disturbance.

By neglecting the voltage drop on IGBT and parallel diode, the absolute value of voltage disturbance can be obtained as,

$$|V_d| = \left| \frac{T_d + t_{ON} - t_{OFF}}{2T_s} \right| V_{dc} \quad (2)$$

where V_d is the voltage disturbance, t_{ON} , t_{OFF} and T_s are the turn-on time, turn-off time and switching period, respectively. V_{dc} is the DC-Link voltage.

Assumed that the power factor is 1.0, the Fourier Series of (2) can be expressed as,

$$V_d = \frac{2(T_d + t_{ON} - t_{OFF})V_{dc}}{\pi T_s} \left[\sum_{n=1}^{\infty} (-1)^{n+1} \frac{1}{2n-1} \cos((2n-1)\omega t) \right] \quad (3)$$

It depicts that the voltage disturbance includes odd-order harmonic component and the corresponding odd-order harmonic current will exist in DC capacitor.

On the other hand, when three-phase loads are unbalanced, PCC current may include positive sequence, negative sequence and zero sequence current. Obviously seen from Fig. 2, the zero sequence current flows into the DC capacitor directly through the neutral line.

In order to validate above theoretical analysis, the simulation is carried out based on Matlab/Plecs. The main circuit of the ST LV side DC/AC converter is the same as Fig. 2 and the simulation parameters are listed in TABLE I.

TABLE I SIMULATION PARAMETERS

Parameters	Value
AC output voltage (V)	400
DC link voltage (V)	800
DC capacitor (μ F)	2250
Filter inductance (mH)	5.2
Filter capacitor (μ F)	6.8
Load inductance (mH)	4
Load resistance (Ohm)	5

The performances of PCC voltage and current as well as the DC capacitor current under balanced load and neglecting the dead time conditions as base case are shown in Fig. 4 (a). Three-phase PCC voltages and currents are both balanced and sinusoidal, and the DC capacitor current ripple is less than 1A. In case 1, considering 2.5 μ s dead time, the results are shown in Fig. 4 (b). Three-phase PCC voltages are still controlled well and balanced, while the DC capacitor current includes third and high order components, as shown in Fig. 4 (b). This matches with the theoretical analysis in (3).

In case 2, considering both 2.5 μ s dead time and unbalanced loads, the results are shown in Fig. 4 (c), where three-phase load inductances are fixed at 4mH while load resistances are 5, 3 and 5 ohm, respectively. In comparison with Fig. 4 (a) and (b), the voltage is also balanced, due to the PR controller. However, the three-phase PCC current is unbalanced and DC capacitor current includes high 50Hz component with more than 40A peak-to-peak value, as shown in Fig. 4 (c). This also matches with the theoretical analysis.

In above three cases, the DC capacitor current performances

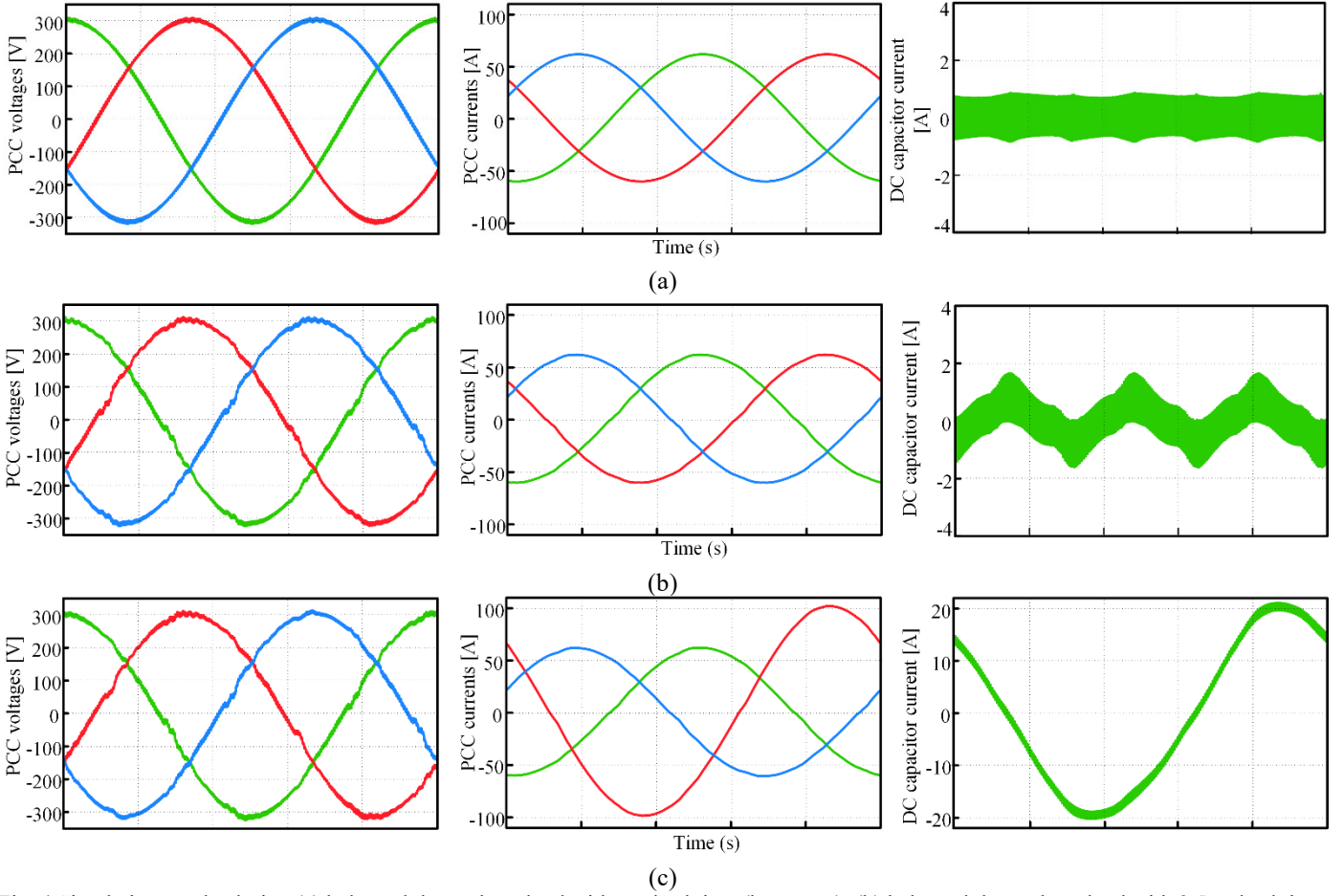


Fig. 4 Simulation results during (a) balanced three-phase load without dead time (base case), (b) balanced three-phase load with 2.5us dead time (case 1), and (c) unbalanced three-phase load with 2.5us dead time (case 2), the time scale is 0.004s/div.

are different, resulting in various impacts on DC capacitor lifetime, which will be discussed in the following section.

III LIFETIME ESTIMATION OF AEC

A Lifetime Model of AEC

For AEC, the lumped model depicted in Fig. 5 is widely accepted in literature [11]–[13]. Apart from the ideal capacitance C , the model accounts for the frequency dependent dielectric losses by means of the parallel configuration of R_d and C_d as well as the constant ohmic resistance R_s due to the foils, tabs and terminals of the construction. The inductive part of the AEC is modeled by the equivalent series inductance L_s . The real part of the AEC impedance represents the equivalent series resistance (ESR) R_{ESR} of the AEC which is of paramount importance to the lifetime and thus the reliability of the AEC.

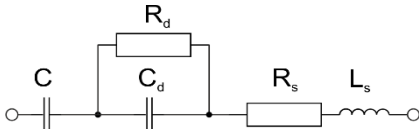


Fig. 5 Lumped model of AEC [11]

In addition to the frequency dependence, the ESR of an AEC exhibits a temperature dependence since the viscosity of the electrolyte, which is the main part of the AEC, changes with temperature [11]. Thus, the ESR is less for higher temperatures.

The impact of frequency and temperature on the AEC's ESR is depicted in Fig. 6. It is commonly known, that the power dissipation P_d of the AEC is determined by the square of RMS ripple current flowing through the capacitor and its ESR as given in Fig. 6. Since the ESR is frequency dependent the ripple current has to be decomposed into its spectral components.

$$P_d = \sum I_{RMS,h}^2 R_{ESR,h} \quad (4)$$

The hotspot temperature T_h of the AEC is determined by its thermal resistance R_{th} and P_d , which result in the hotspot temperature increase ΔT_h , and the ambient temperature T_a .

$$T_h = R_{th} P_d + T_a = \Delta T_h + T_a \quad (5)$$

In order to approximate the lifetime L of the AEC, the lifetime model given in (6) can be applied, where L_0 denotes the base lifetime as given by the manufacturer, V_0 and $T_{h,0}$ are voltage and hotspot temperature at testing conditions, respectively, V and T_h are the operating voltage and operating hotspot temperature, n is a voltage stress factor, which is manufacturer dependent [7].

$$L = L_0 \left(\frac{V}{V_0} \right)^{-n} 2^{\left(\frac{T_{h,0} - T_h}{10K} \right)} = L_0 K_V K_T \quad (6)$$

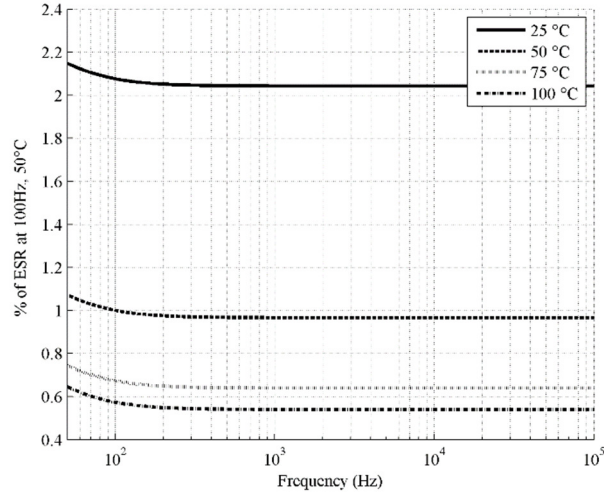


Fig. 6 ESR of AEC over frequency for different temperatures [11]

The impacts of operating voltage and operating hotspot temperature on the lifetime can be represented by the voltage factor K_V and the temperature factor K_T , respectively. By inserting (T_h equ.) into (L equ.), K_T can be split into two parts as given in (7), where K_{Ta} and K_I denote the ambient temperature factor and the ripple current temperature factor, respectively.

$$K_T = 2^{\left(\frac{T_{h0} - T_a}{10K}\right)} 2^{\left(\frac{-\Delta T_h}{10K}\right)} = K_{Ta} K_I \quad (7)$$

By use of (7) the impact of ambient temperature and the hotspot temperature increase due to the ripple current on the AEC lifetime can be studied separately. Since the DC link

voltage can be considered constant, it is to be noted that the lifetime of the AEC is mainly dependent on the hotspot temperature. Thus, apart from the ambient temperature conditions, the ripple current can be considered the main stressor for the AEC. Therefore, examination of the latter is needed for AEC lifetime estimation purposes.

B Lifetime estimation of AEC

In order to analyze the impact on the capacitor lifetime, it is assumed that both, operating voltage and ambient temperature, are the same for each case. Thereby, it is sufficient for the analysis of the relative lifetime L_{rel} with respect to the base case to compare only the impacts of the corresponding capacitor ripple currents, as shown in (7), on the respective lifetime, where $x = \{1, 2\}$ represents case 1 and 2, respectively.

$$L_{rel,x} = \frac{K_{I,x}}{K_{I,base}} \quad (8)$$

In order to clearly show the DC capacitor current ripples, the corresponding capacitor current spectrum is shown in Fig. 7. Under the base case, the capacitor current spectrum shows that the harmonic current has high amplitude in low frequency and switching frequency, as shown Fig. 7 (a). In Fig. 7 (b), since the unbalanced load leads to large fundamental current in neutral line, the 50Hz component has high value (19.65A) for case 2. Additionally, the 3rd-order component is also obvious for case 1 and 2, as shown in Fig. 7 (c). In high frequency range, the effects on DC current ripple are less and DC current ripples are similar for base case, case 1 and 2, as shown in Fig. 7 (d), (e) and (f).

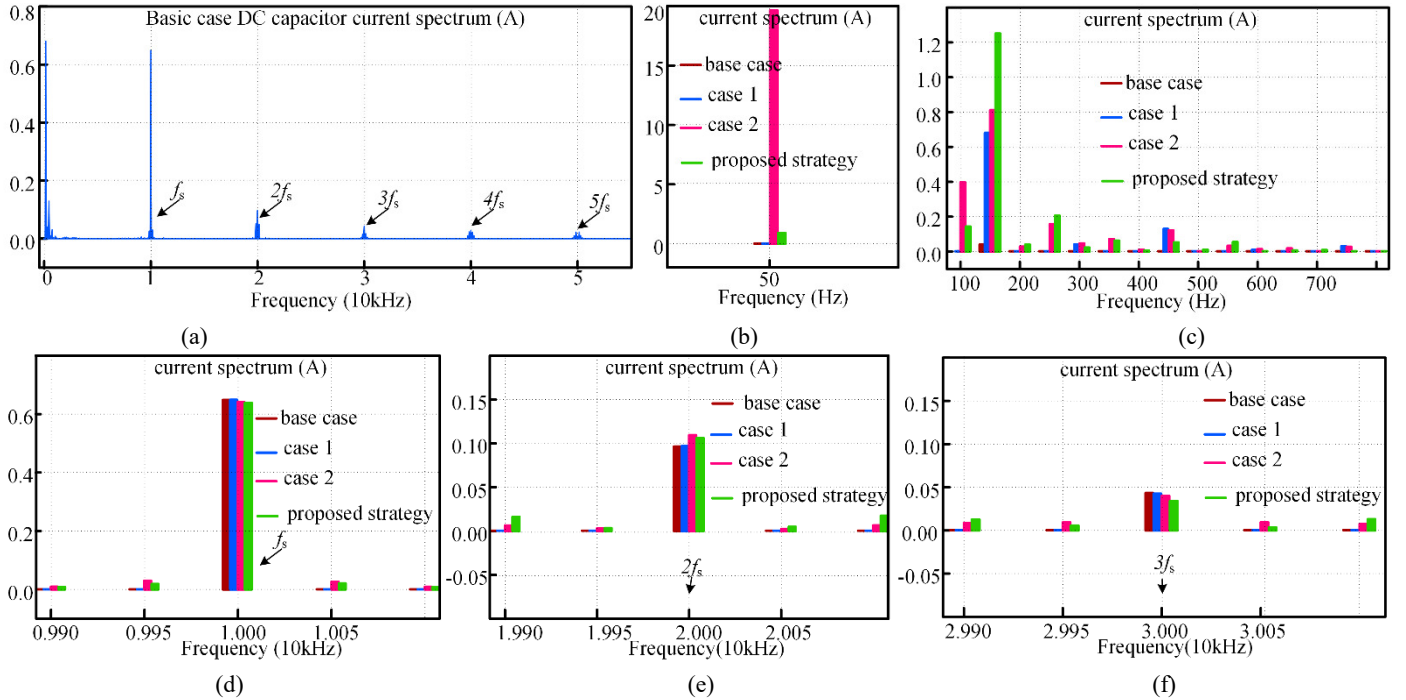


Fig. 7 DC capacitor current spectrum, (a) under balanced load condition and dead time is zero (base case), comparison of base case, case 1, case 2 and proposed strategy at different frequency range (b), (c), (d), (e), (f) are capacitor current spectrum zoomed in at 50Hz, low frequency, f_s , $2f_s$, and $3f_s$, respectively.

Moreover, the DC-link in this paper is configured by a series connection of two AECs, as shown Fig. 2, with the parameters given in Table II in order to meet the requirements in terms of operating DC-link voltage and capacitance. Thus, the full DC-link capacitor current is seen by both capacitors. For the analysis, it is further assumed that the capacitors share the DC-link voltage equally and that they have identical parameters. In addition, the temperature dependence of the ESR is neglected. Therefore, in combination with the parameters given in Table II the impact of the different control targets on the lifetime of a single capacitor can be estimated.

TABLE II DATA OF DC-LINK CAPACITORS

Parameters	Values
Nominal capacitance (uF)	4500
Nominal voltage (V)	500
Nominal R_{ESR} at 100 Hz (mOhm)	21.1
Thermal resistance (K/W)	2.9

Based on the capacitor current spectrum depicted in Fig. 7 and the ESR characteristics discussed in Section II the losses of the capacitor for each case are calculated. Subsequently, with respect to the thermal resistance the hotspot temperature increase ΔT_h is obtained. The results are summarized in TABLE III.

TABLE III HOTSPOT TEMPERATURE INCREASE AND RELATIVE LIFETIME OF DIFFERENT CASES

Simulation case	AEC RMS current I_{cap} (A)	Hotspot temperature increase ΔT_h (°C)	Relative hotspot temperature change $\Delta T_{h,rel}$ (°C)	Relative lifetime L_{rel} referred to base case (pu)
Base case	0.47	0.01	0.00	1
Case 1	0.69	0.03	0.02	0.999
Case 2	13.90	14.01	14.00	0.379

The base case, is chosen as reference for the following analysis, resulting in $L_{rel}=1$ and $\Delta T_{h,rel}=0^\circ\text{C}$. It can be seen that in case of the considered dead time the relative hotspot temperature increase of the AEC is 0.03°C for case 1. This translates in to a relative lifetime of $L_{rel,1}=0.999$. Thus, the impact of the dead time on the AEC's lifetime is negligible in this case. In the event of a load unbalance, the lifetime of the capacitor will be dramatically reduced due to the presence of the high 50 Hz component in the capacitor current spectrum. For this case the relative hotspot temperature increase is 14.00°C , which leads to $L_{rel,2}=0.379$, thus a reduction in the AEC's lifetime of 62.1% as compared to the base case. The tendency of the obtained results is also indicated by the AEC RMS currents given in Table III. From the analysis of the relative lifetime it is evident that the effect of a load unbalance needs to be considered when designing the DC-link for the LV side converter, since the direct connection of the neutral line causes significant low frequency ripple current components and, thus, high thermal stress for the AEC. Apart from design considerations improving the control strategy is another option for preserving the AEC's lifetime.

IV VOLTAGE CONTROL STRATEGY TO REDUCE DC RIPPLES

The conventional strategy controls the three-phase AC voltage, as shown in Fig. 3, which includes the positive sequence, negative sequence and the zero sequence component, simultaneously. Thus, the negative and zero sequence component of the voltage at PCC is controlled to be zero, which leads to neutral line current during not ideal conditions. As analyzed above, the DC capacitor lifetime will be significantly reduced because of the large neutral current. In order to solve this problem, an improved control strategy is proposed.

The overall control diagram of the proposed strategy is shown in Fig. 8. The voltage control loop includes positive sequence PCC voltage and negative sequence PCC voltage, which are connected in parallel. The negative sequence voltage control is necessary due to the distribution grid code requirement on voltage unbalanced ratio, which is defined in (9) (less than 2% during most cases).

$$K_{un} = \frac{U_{neg}}{U_{pos}} \quad (9)$$

In order to control the neutral line current and in turn to limit the capacitor current ripples, an extra current control loop is added as shown in Fig. 8. By tuning the neutral current controller gains, the neutral current can be effectively suppressed.

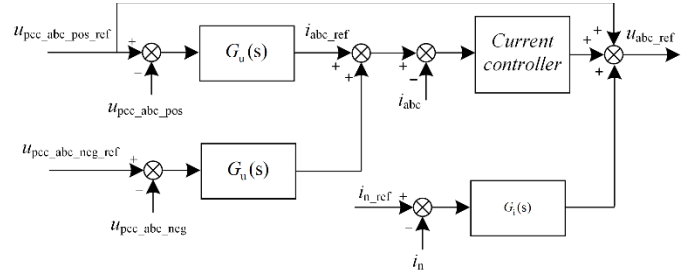


Fig. 8 Overall control diagram of the proposed voltage control

The simulation results of the proposed strategy is shown in Fig. 9. Compared to in Fig. 4 (c), considering the same dead time and unbalanced load, the capacitor current amplitude is significantly reduced, as shown in Fig. 9.

The corresponding DC capacitor current spectrum is also shown in Fig. 7 (b)-(g). It clearly shows that the capacitor current spectrum is significantly reduced, as compared to case 2. The lifetime estimation of the proposed strategy is given in TABLE IV.

The AEC RMS current is reduced to 1.2 A. Based on the DC current spectrum, the relative hotspot temperature change is $\Delta T_{h,rel}=0.08^\circ\text{C}$, which leads to a relative lifetime of $L_{rel,3}=0.995$. Therefore, by applying the proposed control strategy, the current stress and, subsequently, the thermal stress for the AEC is reduced significantly. The reduction in lifetime is decreased to 0.5% and, thus, the AEC lifetime in case of load unbalance is nearly preserved completely.

TABLE IV HOTSPOT TEMPERATURE INCREASE AND RELATIVE LIFETIME OF DIFFERENT CASES

Simulation case	AEC RMS current I_{cap} (A)	Hotspot temperature increase ΔT_h (°C)	Relative hotspot temperature change $\Delta T_{h,rel}$ (°C)	Relative lifetime L_{rel} referred to base case (pu)
Proposed strategy	1.2	0.09	0.08	0.995

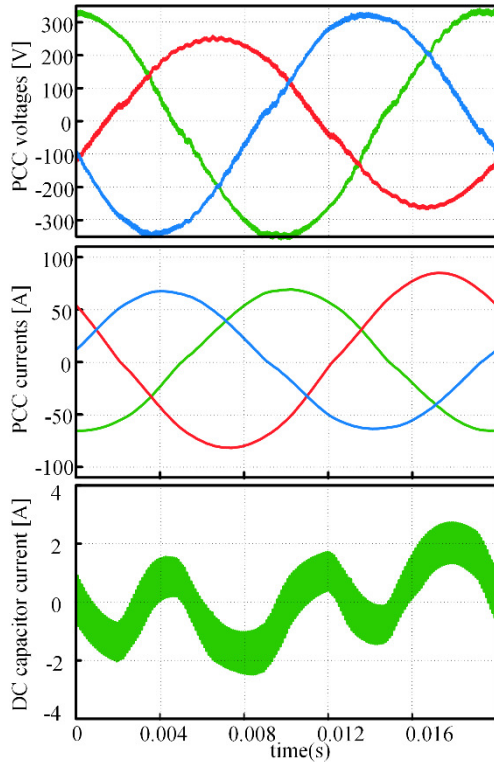


Fig. 9 Simulation results of the proposed strategy considering 2.5us dead time and unbalanced loads.

In Fig. 10, it clearly shows that the unbalanced voltage ratio for base case, case 1 and 2 and the proposed strategy are all smaller than 2%, which satisfies the grid code requirement on voltage unbalanced ratio in distribution grid.

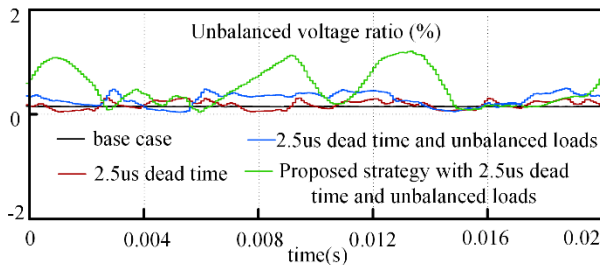


Fig. 10 Unbalanced ratio of PCC voltage

V CONCLUSIONS

In this paper, challenges of the distribution grid on the ST DC-Link is studied. Based on these impacts, the DC electrolytic

capacitor lifetime is estimated for the ST low voltage side converter. The dead time, nonlinear characteristic of the IGBT and unbalanced loads can lead to increase of DC capacitor current ripples in low frequency range, especially at 50Hz and 150Hz. This ripple current significantly reduces DC electrolytic capacitor lifetime. An improved voltage control strategy is proposed to effectively suppress the neutral line current, significantly reduce the capacitor current ripple and in turn increase the lifetime of the electrolytic capacitor.

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