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Topology and Control Strategy for Accelerated Lifetime Test Setup of DC-Link Capacitor of Wind Turbine Converter

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Abstract—Back-to-back converters for wind turbine systems (WTS) feature capacitors in the DC-link to maintain a stable DC-link voltage and to decouple the generator from the grid. Electrolytic and film capacitors can be chosen to this purpose. Long-term field experience and recorded failure data reveal that capacitor failures are one of the main reasons for the downtime of WTS. The ripple current accelerates the wear-out of the capacitors, which is strongly dependent on the mission profile of the system. Therefore, it becomes important to estimate the useful lifetime of a capacitor as a function of the ripple current. In this paper, aging characteristics of electrolytic capacitors are described, and a power converter topology and its control strategy are designed to perform accelerated lifetime tests. The voltage and ripple current of the capacitor under test (CUT) can be controlled with low THD to correlate wear-out with ripple.

Keywords—Reliability, Accelerated lifetime test, Electrolytic capacitor, Wind turbine converter, Controller design

I. INTRODUCTION

Many efforts have been devoted to the research of WTS in terms of system integration, optimization of the employed power converter topologies (such as bidirectional, multilevel, and parallel configurations), as well as the application of novel control strategies in order to maximize the efficiency of the energy conversion [1]-[6]. However, challenging operating conditions due to variable wind power and increasing grid code requirements lead to a high stress variability for the electrical system of the WTS. Therefore, unexpected failures occur that come along with high costs due to downtime and maintenance of the WTS.

As shown in Fig. 1, the electrical system is one of the main reasons for failures of WTS. More precisely, electrolytic capacitors, which are typically used as DC-link in back-to-back converters of WTS since they offer the advantages of higher rated voltage, energy density, and capacitance, respectively, at lower costs compared to other capacitor types, exhibit the highest failure rate inside the electrical system [7], [8]. Research papers on capacitor reliability have been mainly focused on degradation diagnosis methods by analysis of internal parameters, such as the equivalent series resistance

(ESR) and the capacitance, including complex algorithms and models [9]-[11]. The lifetime of electrolytic capacitors is influenced by the ambient temperature, the ripple current flowing through the capacitor, and the applied voltage, respectively [12]. To date, capacitors' lifetime models take into account the operating temperature and the current RMS value. The operating temperature is then dependent on the power dissipated by the capacitor. However, a clear correlation between the ripple current frequency and the lifetime of the capacitors is missing. The analytic lifetime model based on thermos-mechanical characteristics can more precisely consider the correlation between the lifetime and the operating conditions [13], [14]. For this model the number of cycle to failure is required and the test is accomplished under over-rated condition, which is called the accelerated lifetime test.

This paper proposes a power converter setup and its control strategy to subject the capacitors to arbitrary current/voltage profiles. By applying a stress greater than the nominal conditions, accelerated lifetime tests can be performed. The main challenge is to generate current waveforms with a high fundamental frequency, great amplitude and a low THD, in order to obtain a better correlation between the single frequency and the capacitor damage.

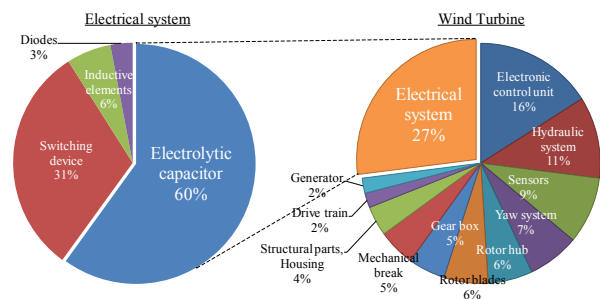


Fig. 1. Components failure rate in wind turbine [7], [8].

II. ELECTROLYTIC CAPACITOR

A. Electrolytic Capacitor Model

A simplified model of an electrolytic capacitor is depicted in Fig. 2, where C is the terminal capacitance, C_D and R_D account for the losses caused by the dielectric, R_0 is the combined constant resistance of terminals, tabs and foils, respectively, and R_t is the resistance of the electrolyte [10]. It should be noted that the capacitor model is also containing an inductive part in series, that is dominant, when the capacitor is operated above its resonance frequency. For the following analysis this inductance will be neglected, following the assumption that the capacitor is operated well below its resonance frequency. The equivalent series resistor (ESR) represents the real part of the capacitor's impedance. Therefore, it can be expressed as

$$R_{ESR} = R_0 + R_f + R_t \quad (1)$$

where R_f represents the frequency dependent resistance of the dielectric layer, which is composed by C_D and R_D , and R_t is the temperature dependent part due to the characteristics of the employed electrolyte [10], [15]. Since with increasing temperature the viscosity of the electrolyte changes, its conductivity increases, which in turn leads to a reduction in ESR due to R_t . This effect can be modeled by applying (2), where $R_{t,b}$ is R_t at base temperature T_b , T_s is the surface temperature of the capacitor, and SF denotes a capacitor dependent temperature sensitivity factor [10].

$$R_t = R_{t,b}(T_b) \cdot e^{\frac{T_b - T_s}{SF}} \quad (2)$$

In Fig. 3 the ESR is plotted against frequency for different temperatures in accordance to [10]. As discussed before, it can be seen that the ESR decreases as temperature increases. Moreover, it can be noted that increasing frequencies also lead to a decrease in ESR due to R_f .

B. Impact of Ripple Current on Lifetime

The lifetime of an electrolytic capacitor is strongly influenced by its operating conditions or mission profiles, respectively (such as temperature, humidity, pressure, vibration, voltage, and current). Apart from ambient temperature, which accelerates electrochemical reactions, and the applied voltage level, the ripple current flowing through the capacitor is one of most critical stressors as discussed in [12]. The latter is of crucial importance, since it causes additional internal heating due to the power dissipation caused by ESR. The surface temperature of the capacitor can be estimated by applying (3), where T_a denotes the ambient temperature, ΔT is the additional heating caused by the power

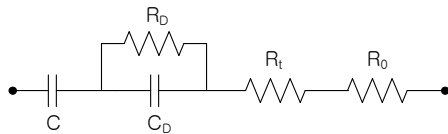


Fig. 2. Equivalent model of electrolytic capacitor.

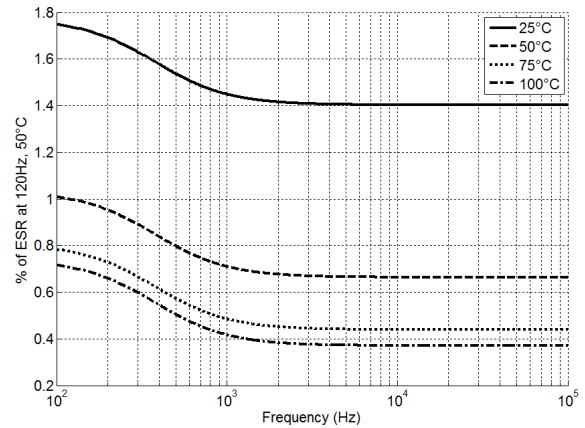


Fig. 3. Variation of ESR with respect to ripple current frequency and temperature [10].

dissipation P_d and the thermal resistance of the capacitor R_{th} .

$$T_s = T_a + \Delta T = T_a + P_d \cdot R_{th} \quad (3)$$

Since the ESR exhibits a frequency dependent behavior, for the correct calculation of P_d the knowledge of the RMS capacitor currents at the corresponding frequencies is needed [16], [17]. Therefore, a spectral analysis of the ripple current has to be carried out in order to derive its harmonic content. By knowing the current harmonics, P_d can be calculated by

$$P_d = \sum_{i=1}^n I_{R,i}^2 \cdot R_{ESR,i} \quad (4)$$

where $I_{R,i}$ and $R_{ESR,i}$ denote the RMS ripple current and the ESR at frequency harmonic i , respectively, with $i = 1, 2, \dots, n$.

$$L = L_0 \cdot 2^{\frac{T_{max} - T_a}{10K}} \cdot 2^{-\left(\frac{I_a}{I_0}\right)^2 \frac{\Delta T_0}{A}} \cdot \left(\frac{V_a}{V_0}\right)^{-m} \quad (5)$$

The lifetime model of an electrolytic capacitor is shown in (5), where L_0 denotes the lifetime at nominal values as given in the manufacturer's datasheets, T_{max} is the maximum permissible temperature, I_a is the applied ripple current, I_0 is the rated ripple current, ΔT_0 is the temperature increase when I_0 is applied, A is a temperature coefficient, V_a is the applied voltage, V_0 is the nominal voltage, and m accounts for the manufacturer dependent voltage factor as discussed in [18]. The model consists of three parts, where each part is considering one of the three major stressors. The impact of the ambient temperature follows the well-known rule of Arrhenius, which constitutes a doubling in lifetime for each 10 K temperature decrease. Moreover, the applied voltage is taken into account in this model, since an increasing voltage level causes degradation due to electrolyte evaporation effects, which in turn affects the lifetime of the capacitor. As mentioned above, the ripple current is influencing the capacitor's lifetime by acting on the temperature rise ΔT , which is also taken into account in (5). The factor A accounts for the higher impact of ΔT on the lifetime, since it is

evaluated experimentally by some manufacturers, that the lifetime is bisected by an increase of, e.g., 7...10 K in ΔT [19].

Degradation of the capacitor is not included in (5). Since the heat rise due to the ripple current causes electrolyte evaporation, it leads to a degradation of the capacitor's parameters, being the ESR and the capacitance C , respectively. As discussed in [12] the ESR will increase with time, while C might decrease. An increasing ESR will have an impact on the power dissipation as shown in (4) and, thus, affects the lifetime of the capacitor as well. For this reason, more research efforts have to be devoted to better understand the correlation between parameter degradation and lifetime of capacitors.

DC-link capacitors of power converters are subject to very different ripple current profiles. The ripple current flowing through the DC-link capacitors in a back-to-back converter of a wind turbine system, for example, is dependent on the operating conditions at both ends of the converter. As presented in [16] the frequency spectrum of the capacitor current is depending on factors such as the modulation scheme, the employed carrier-frequency, the power factor, amplitude, and frequency of the output currents of the converter. Based on the above formulas, from Fig. 3 it becomes evident that ripple currents of lower frequencies have a bigger impact on the capacitor's lifetime than currents of higher frequencies, since the ESR is higher in the low frequency region. This effect is also discussed in [18].

In order to achieve a better understanding of degradation methods due to mission profiles, it is necessary to investigate the impacts of ripple current harmonics (and their combinations) on the capacitor's parameters and lifetime. Therefore, a careful analysis of different operating conditions has to be carried out in order to enable the application-oriented verification of both, the thermal model and the lifetime model of the capacitor, which can be of assistance to create a tool that can help to reach a more reliable and cost effective system. The proposed system is useful for detailed analysis of ripple current stresses, which are derived from mission profiles of wind turbine converters, since it provides the application of combined stresses as will be discussed in the following sections.

III. PROPOSED ACCELERATED LIFETIME TEST SETUP

A. Topology Description

The goal of the test setup is to apply accelerated stress tests to electrolytic capacitors by means of ripple currents of both, high RMS amplitude and frequency, in order to investigate thermal effects and aging characteristics based on mission profile data. In order to investigate the impact of single frequency harmonic ripple currents, a low THD and therefore proper filtering of the switching frequency components is required. Moreover, since the focus is put on application-oriented stress tests for DC-link capacitors in WTS, the setup needs to be able to provide a high DC voltage to the capacitor under test (CUT). Therefore, the test setup has to be carefully designed in order to meet the required specifications and to ensure that no components other than the CUT fail during the

tests. Apart from the test specifications, for the reasons of cost effectiveness and lower system complexity, standard switching devices (IGBTs) are to be implemented into the test setup. Based on this, two possible solutions are discussed in this section, which can be used to achieve high frequency ripple currents in combination with a DC voltage at the output side of the converter.

The first possible configuration, the cascaded H-bridge (CHB), is shown in Fig. 4 (a). It consists of three H-bridge converter cells connected in series, allowing the output voltage to be three times the DC source voltage of each cell. The modulation is accomplished with the phase shifted PWM as shown in [20]. With this topology, the effective inverter switching frequency is six times higher than the device switching frequency of each cell. This offers the advantage of using standard switching devices in the test setup. Moreover, with a higher switching frequency ripple on the output side of the converter a smaller filter can be realized, since the filter inductance is inversely proportional to the switching

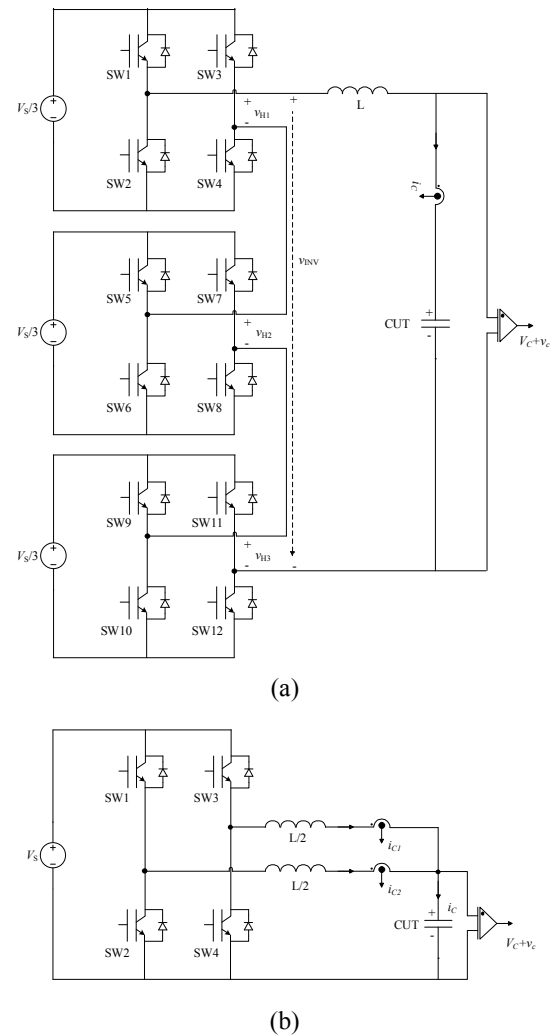


Fig. 4. Possible topologies for test setup. (a) cascade half-bridge (CHB), (b) interleaved bidirectional (IB).

frequency (see below).

From the system complexity's point of view, a much simpler solution could be used. In Fig. 4 (b) the configuration of an interleaved bidirectional DC/DC converter (IB) is shown [21]. It is based on an H-bridge and can therefore be realized with less switching devices than the CHB, which reduces the overall complexity of the system by means of control and hardware efforts. Nevertheless, in order to fulfill the above mentioned test requirements the CHB topology is chosen, since the IB configuration has certain limitations as discussed in the following paragraph.

Equations (6) and (7) describe the relation between the switching frequency and the filter inductor in case of IB and CHB, respectively [22], [23].

$$\begin{cases} f_{sw} = \frac{V_S}{\Delta I_L \cdot L} \frac{(1-2D)D}{1-D} & \text{for } 0.0 < D < 0.5 \\ f_{sw} = \frac{V_S}{\Delta I_L \cdot L} \frac{(2D-1)(1-D)}{D} & \text{for } 0.5 < D < 1.0 \end{cases} \quad (6)$$

$$f_{sw} = \frac{V_S}{18 \cdot \Delta I_L \cdot L} D(1-D) \quad \text{for } 0.0 < D < 1.0 \quad (7)$$

where f_{sw} is the switching frequency, V_S is the DC source, L is the filter inductor, ΔI_L is the switching ripple component which determines the THD of the output ripple current, and D is the duty ratio. The DC voltage and the frequency of the output current, both of them required for the determination of the required filter inductor size, are given by the test requirements and can therefore be considered as constants for the following analysis. Resulting from this the switching frequency is a function of the inductance and the duty ratio. Moreover, V_S is composed of the DC voltage on the CUT, V_C , and the voltage drop on the filter inductor, $2\pi f L I_C$, as

$$V_S = V_C + 2\pi \cdot f \cdot L \cdot I_C \quad (8)$$

Considering (8), Fig. 5 shows the switching frequency against the inductance, when V_S is 1.5 kV, V_C is 1 kV, ΔI_L is 1 A (5% of 20 A), the frequency of the ripple current, f , is 3 kHz, and D is 0.75 for the IB and 0.5 for the CHB where each topology reaches its maximum THD at this duty ratio. The values are arbitrarily chosen as an example, but a DC-link voltage within the range of 1 kV is typical for WTS applications. As can be seen, in order to achieve the same THD and, thus, the same quality of the ripple current applied to the CUT, either a bigger filter inductance needs to be chosen or the switching frequency needs to be increased in case of the IB. Since the target of this paper is to propose a setup which makes use of standard IGBT devices, a very high switching frequency is not applicable. Due to this fact, for the operation of the IB at the same THD a bigger filter would be required which, in turn, would lead to a higher voltage drop across the filter and, thus, to a lower effective DC voltage for the CUT. Since one requirement for the setup is the ability to provide high a DC voltage to the CUT, a bigger DC source would be required in order to compensate for the voltage drop across the filter. Consequently, this would lead to the fact that

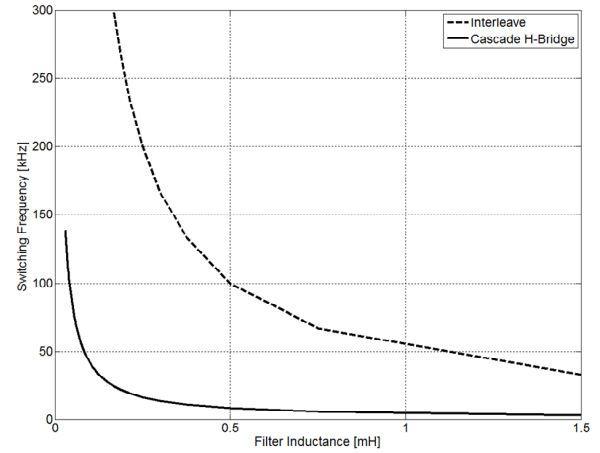


Fig. 5. Switching frequency against filter inductance to satisfy the required THD.

the blocking voltage of the IGBT devices would limit the capability of the setup. For this reason, the choice of the CHB topology is reasonable, since the output voltage can be shared equally by the three converter cells, thus, requiring smaller DC sources. On the one hand, the choice of the CHB leads to the burden of a higher system complexity but, on the other hand, it makes it possible to realize the system with standard devices.

B. Control Strategy and Analysis

The proposed controller of the accelerated lifetime test setup is shown in Fig. 6. As can be seen, it consists of a voltage control loop, which is employed to control the DC voltage of the CUT, and a current control loop for the application of the ripple current stress.

The current control loop consists of a PI current controller, which regulates the RMS amplitude of the applied ripple current, a frequency control block, that is needed to achieve the desired ripple current frequency, and the RMS feed-back. The measured capacitor ripple current i_C is fed back to the current controller via the RMS feed-back block that filters the RMS amplitude of the ripple current from the measured signal. Since the measured ripple current, as expressed as (9), can be converted by help of square operation and triangular functions into (10).

$$i_C = I_C \cdot \sin(\omega t + \alpha) \quad (9)$$

$$i_C^2 = I_C^2 \sin^2(\omega t + \alpha) = \frac{1}{2} I_C^2 \left[1 - \cos\left(\frac{\omega t + \alpha}{2}\right) \right] \quad (10)$$

where i_C denotes the measured ripple current, I_C is the amplitude, ω is the angular frequency of the ripple current, and α denotes the phase displacement angle of the current with respect to the output voltage of the CHB. It is evident that the DC quantity of the current can be found by the application of a simple low-pass filter (LPF). Thus, the RMS value can be found as the square root of the LPF output value as

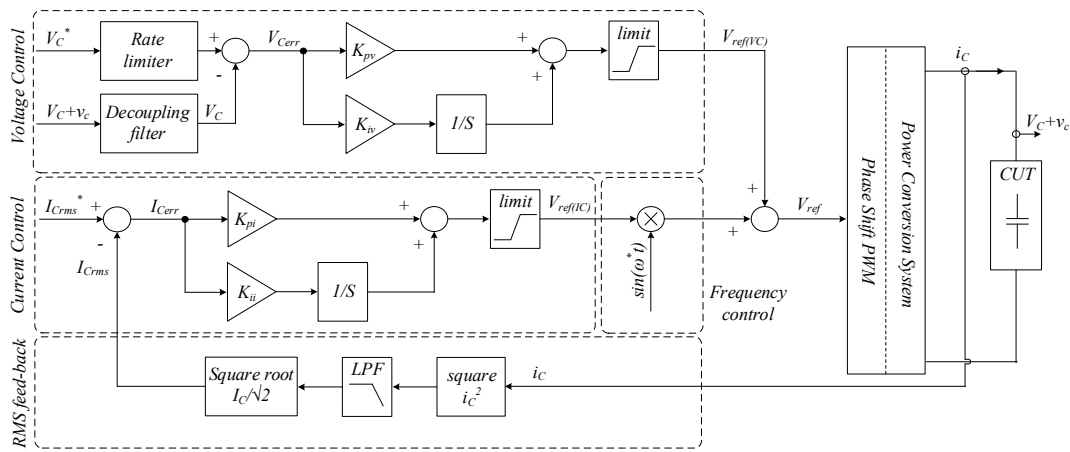


Fig. 6. Control block diagram of accelerated lifetime test setup.

$$\frac{1}{2} I_C^2 \Rightarrow \frac{1}{\sqrt{2}} I_C \quad (11)$$

Due to the fact that the PI controller is only acting on the RMS amplitude of the ripple current, its output value is multiplied with a unity sinusoidal signal that accounts for the reference ripple current frequency. Therefore, the frequency of the ripple current can be controlled by adjusting the frequency of the sinusoidal signal.

For the control of the DC voltage, which is applied to the CUT, a voltage control loop is required. In order to prevent the possibility of surge currents, that might occur because step changes in the output voltage across the CUT, the voltage reference is processed by a rate limiter. The ripple current through the CUT is causing a ripple component v_c that is superimposing the DC voltage V_C . Therefore, a decoupling filter is adopted to filter the ripple voltage components. Thus, the DC quantity V_C is fed into the voltage control, so that the voltage control can be considered decoupled from the current control. In addition, the regulation of the DC voltage can now be done by means of a PI voltage controller.

Due to its simplicity, the proposed control scheme offers certain advantages compared to other methods. Instead of the employed RMS feed-back block a conventional phase-locked loop (PLL), such as the SRF-PLL method presented in [24], could be used in order to obtain the RMS value of the ripple current. However, this method would require an additional feed-back control loop, which would lead to an unnecessary increase in the complexity of the system. Moreover, the control of both, the amplitude and the frequency, of the ripple current could be realized by implementing a proportional resonant (PR) controller. However, a PR controller is tuned to a certain frequency, which would mean for the application at hand that a number of PR controllers would be needed corresponding to the required frequency range of the controlled ripple current [25].

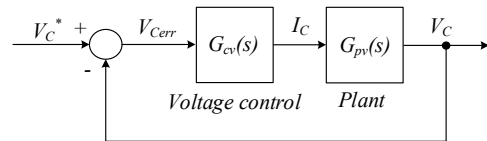
Before designing the controllers, the output load composed of the filter inductor and the capacitor is described as

$$T_S(s) = \frac{1}{L} \cdot \frac{s}{s^2 + 1/LC} \quad (12)$$

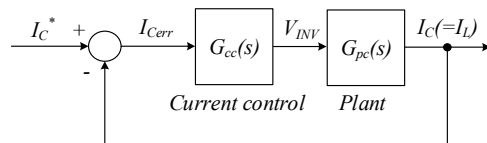
From the above transfer function, it becomes evident that the design of filter inductance is dependent on the capacitance of the CUT as well as on the required frequency range of the stress ripple current. In this application, the filter inductance is chosen such that the test setup is operated within the inductive region and to achieve the required damping respect to the CUT.

The simplified linear models of the voltage controller and the current controller are shown in Fig. 7 (a) and (b), respectively. To simplify the model, the rate limiter and the decoupling filter are not considered in the voltage controller model, and the RMS feed-back block is not involved in the current controller model. The open loop transfer function and the closed loop transfer function for the voltage controller are represented as (13) and (14), respectively.

$$G_v^o(s) = G_{cv}(s) \cdot G_{pv}(s) = (K_{pv} + \frac{K_{iv}}{s}) \cdot \frac{1}{sC} \quad (13)$$



(a)



(b)

Fig. 7. Simplified linear model of (a) voltage controller and (b) current controller.

$$G_v^c(s) = \frac{G_v^o(s)}{1 + G_v^o(s)} = \frac{\frac{K_{pv}}{C}s + \frac{K_{iv}}{C}}{s^2 + \frac{K_{pv}}{C}s + \frac{K_{iv}}{C}} \quad (14)$$

where G_{cv} is the transfer function of voltage controller, G_{pv} is the transfer function of load, K_{pv} and K_{iv} are the proportional and the integral gain of the voltage controller, respectively, and C is the capacitance of the CUT. The load is considered as only capacitive load in G_{pv} since the DC quantity is controlled by means of the decoupling filter and the inductor works as short circuit at DC. The gains can be found by comparing the coefficients of (14) with the typical 2nd order transfer function in (15).

$$T(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (15)$$

where ω_n is the cut-off frequency and ζ is the damping ratio. Finally, the gains for the voltage control are found as

$$\begin{aligned} K_{pv} &= 2 \cdot \zeta \cdot \omega_n \cdot C \\ K_{iv} &= \omega_n^2 \cdot C \end{aligned} \quad (16)$$

The open loop transfer function and the closed loop transfer function of the current controller are expressed in (17) and (18), respectively.

$$G_c^o(s) = G_{cc}(s) \cdot G_{pc}(s) = \left(K_{pc} + \frac{K_{ic}}{s} \right) \cdot \frac{1}{sL^*} \quad (17)$$

$$G_c^c(s) = \frac{G_c^o(s)}{1 + G_c^o(s)} = \frac{\frac{K_{pc}}{L^*}s + \frac{K_{ic}}{L^*}}{s^2 + \frac{K_{pc}}{L^*}s + \frac{K_{ic}}{L^*}} \quad (18)$$

where G_{cc} is the transfer function of current control, G_{pc} is the transfer function of the load, K_{pc} is the proportional gain, K_{ic} is the integral gain of the current controller, and L^* is the equivalent inductance at the ripple current frequency. For the current controller design, the load is considered as inductive load because the inductance is designed such that the setup is operated in the inductive region with respect to capacitance of the CUT as mentioned before. The equivalent inductive load at ripple current frequency can be calculated as

$$L^* = L - \frac{1}{C \cdot \omega^2} \quad (19)$$

The gains can be obtained as (20) with the same procedure as for the voltage control design.

$$\begin{aligned} K_{pc} &= 2 \cdot \zeta \cdot \omega_n \cdot L^* \\ K_{ic} &= \omega_n^2 \cdot L^* \end{aligned} \quad (20)$$

To define the control ability of the DC voltage on the CUT, the control strategy is mathematically analyzed in Table I, where C and I_{Cmax} are the required values and L and V_S are the

TABLE I. ANALYSIS OF CONTROL STRATEGY

Impedance	$Z = \omega L - \frac{1}{\omega C}$
Maximum duty ratio of the maximum ripple current	$D_{\max, I_C} = \frac{I_{C\max} \cdot Z}{V_S}$
Maximum DC voltage on CUT	$V_C \leq V_S(1 - D_{\max, I_C})$

designed values for satisfying the requirements mentioned in this section.

IV. EXPERIMENTAL RESULTS

In order to verify the analytical findings experimentally, a first prototype of the proposed accelerated lifetime test setup has been built. Thereby, the CHB topology is evaluated with respect to the proposed control strategy. Moreover, the ability to control the ripple current frequency as well as the controller design are verified. Table II describes the parameters of the test setup, the specifications of the CUT, the test requirements, and the designed setup parameters and controllers, respectively.

With the determined specification of the CUT and the test requirements, the DC source and the inductance are chosen as explained in the previous section. The cut-off frequency of the decoupling filter is designed at 25 Hz in order to obtain only the DC quantity from the measured voltage. Subsequently, the bandwidth of the voltage controller is set to 2 Hz which is lower than 10 times of the cut-off frequency of the decoupling filter for the stable feed-back control. The cut-off frequency of the RMS feed-back is configured at 50 Hz for eliminating the signal which has 0.5ω in (10). For the same reasons as for the voltage controller, the bandwidth of the current controller is chosen as 5 Hz.

TABLE II. SYSTEM PARAMETERS

Parameter		Value
Power conversion system	Device Switching frequency (f_{sw})	20kHz
	DC source (V_S)	300V (100V*3EA)
Capacitor under test	Capacitance	500uF
	Rated voltage	250V
Test requirement	Ripple current (I_{Crms})	I_{Crms} : 10~15A _{rms} ω : 2~3kHz
Design	Inductance (L)	0.3mH
	Maximum DC voltage (V_{Cmax})	224.1V @2kHz 183.4V @3kHz
	Voltage controller	ω_m : 2Hz / ζ : 0.707 decoupling filter: 25Hz rate limiter: 1000V/s
	Current controller	ω_{ni} : 5Hz / ζ : 0.707 RMS feed-back: 50Hz

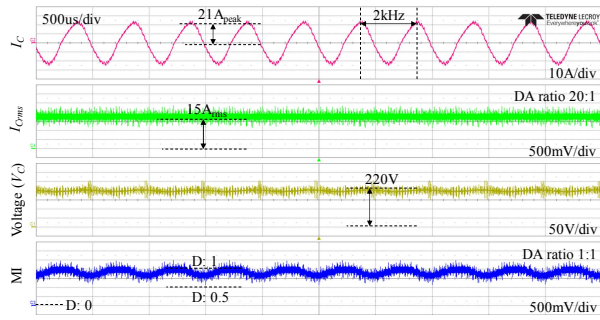
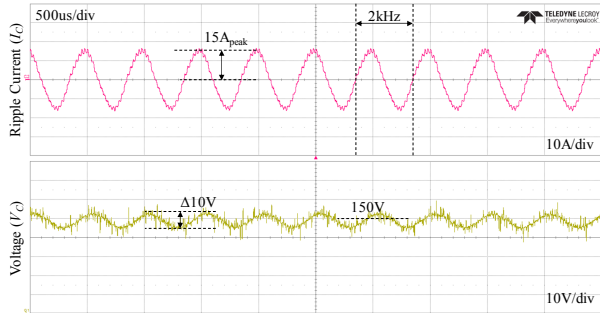
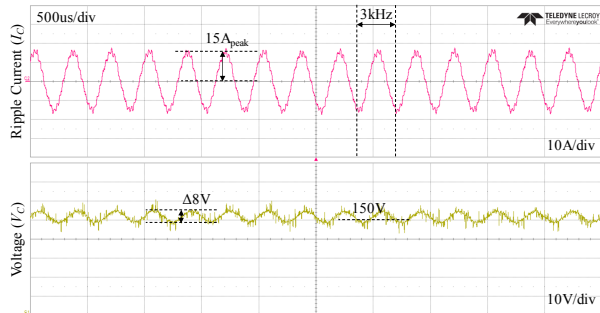


Fig. 8 Verification of DC voltage control boundary.



(a)



(b)

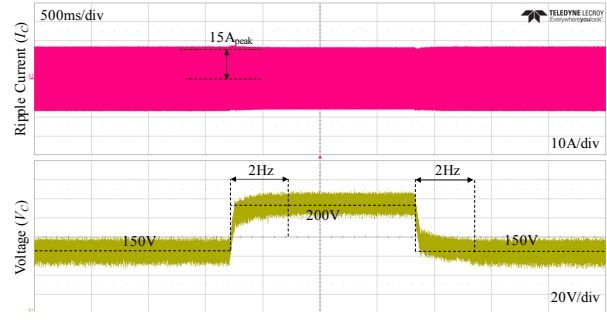
Fig. 9. Verification of frequency control and steady state (a) at 2kHz, (b) at 3kHz.

A. Verification of Control Boundary

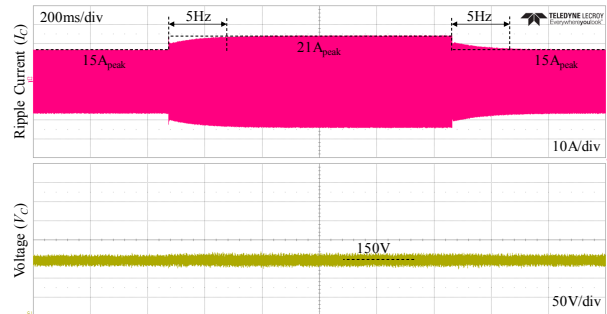
As shown in Fig. 8, the analyzed control boundary is verified by applying a 2 kHz ripple current in order to ensure whether the designed setup can cover the stress requirements. The duty ratio reaches near its maximum value when the controlled stress is 224 V/15 A_{rms} as described in Table II. The theoretical boundary and the experimental boundary are identical.

B. Verification of Frequency Control and Steady State

The performance of the frequency feed-forward control is presented in Fig. 9. The ripple currents of 2 kHz and 3 kHz are stably regulated at 10 A_{rms} as shown in Fig. 9 (a) and (b), respectively. For both cases the V_C is set to 15 V, which lies well below the control ability limits (see Table II).



(a)



(b)

Fig. 10. Verification of controller design. (a) voltage controller, (b) current controller.

C. Verification of Controller Design

Fig. 10 (a) indicates the dynamic response of the voltage controller. The voltage is varied from 150 V to 200 V and vice versa while the current is regulated at 10 A_{rms}. In Fig. 10 (b), the current is changed from 10 A_{rms} to 15 A_{rms} and vice versa while the voltage is controlled at 150 V. The results are suitable for the designed dynamic response requirements (bandwidth for voltage control is 2 Hz and for current control is 5 Hz).

V. CONCLUSION

This paper presented the design of a test setup, developed to apply accelerated stress tests to capacitors based on mission profile data of WTS. Therefore, aging characteristics of electrolytic capacitors and effective factors which affect its lifetime were discussed. It was concluded that the ripple current stress of DC-link capacitors in WTS is the most important factor with respect to lifetime. Based on this, the objective of this paper was to design a test setup based on standard switching devices with which the correlation of both, ripple current frequency and amplitude, in combination with a high DC-voltage offset with lifetime can be achieved. Hence, it was demonstrated that the CHB combined with the proposed control scheme is a feasible solution. Even though it offers an increased complexity compared to other possible topologies, a high DC-voltage offset as well as low THD in the output current can be achieved with low rated standard switching devices. Finally, experimental results verified the applicability

of the proposed test setup for application-oriented capacitor ripple current stress tests.

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