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Optimized Modulation in Parallel Neutral-Point Clamped Inverters for Circulating Current Reduction: A Space Vector Analysis

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Abstract—Parallel Neutral-Point Clamped (NPC) inverters are commonly employed in medium voltage high power applications, such as wind energy system, smart transformer, and power conditioners. In literature, it is shown that the Phase Disposition modulation (PD) strategy provides better performance in terms of harmonic profile and current ripple for single NPC application. Therefore, the PD has been commonly employed as an optimal solution and used for optimized Space Vector Modulation (SVM). However, in case of interleaved operation and common dc-link, one of the main challenges is: the circulating current between inverters. With this consideration, comparisons between the PD and another carrier-based modulation - Alternative Phase Opposite Disposition (APOD) are carried out based on the space vector representation. The analysis shows that the APOD modulation offers much lower circulating current compared to the PD modulation, maintaining similar current ripple as well as spectrum quality of the total current. As a result, an APOD-based SVM technique is proposed in this paper, in order to reduce the circulating current and meanwhile maintain other superior characteristics. Full switching sequences as well as design criteria are presented for all sectors. Simulation and experimental results are provided to validate the effectiveness of the proposed modulation technique.

Index Terms—NPC inverters, PD, APOD, interleaved operation, circulating current, space vector representation.

I. INTRODUCTION

Parallel NPC inverters are widely utilized in high power applications, for instance multi-MW wind energy systems [1], smart transformer [2], static synchronous compensators (STATCOMs) [3], active power filters (APFs) [4], and electric drives [5]. To reduce the current ripple, interleaved operation can be used to shift the carrier phases among different modules [6], [7]. However, the circulating current issue raises in the case of a common dc-link, which causes severe problems such as overcurrent, higher voltage drop, and higher thermal stress for semiconductors and dc capacitor. In literature, it is known that the modulation technique is one of the key factors that determine the circulating current between parallel inverters [6]. For parallel two-level voltage-source inverters, optimized SVM techniques have been proposed in order to minimize the circulating current and thus improve the overall performance [8], [9]. Nevertheless, for the three-level NPC, the issue of

circulating current and the optimum modulation regarding this issue were seldom studied in literature.

Traditionally, the Phase Disposition modulation (PD) is considered as the best carrier-based solution for the single three-level NPC inverter, which leads to better waveform and spectrum quality [7], [10]. As a result, the conventional SVM and most of the optimized SVM for three-level NPC are derived from the switching sequences of the PD modulation [11], [12]. However, for the parallel NPC inverters with a common dc-link, the superiority of the PD modulation and the PD-based SVM are not longer established. An example is presented in [13], showing that the PD modulation has negative influence on the current balancing between cells of the same phase, while the Alternative Phase Opposite Disposition (APOD) is better in terms of the differential model of phase current. With this consideration, this paper starts with investigating the impact of different three-level NPC carrier-based modulation techniques on the circulating current under interleaved operation and then develops a superior solution for the SVM design. Based on their space vector representation, the common-mode voltage as well as the circulating current of both the PD and the APOD modulation techniques are studied, showing that the APOD offers much lower circulating current while maintaining similar current quality. Therefore, an APOD-based SVM is proposed and its full switching sequences in all sectors are given. The performance evaluation in the time-domain and the phase-domain are carried out by theoretical analysis and simulation/experimental validations.

The paper structure is organized as follows: In Section II, the problem description of circulating current between two parallel NPC inverters under interleaved operation is discussed. In Section III, the two common three-level carrier-based modulation techniques are studied by their space vector representation and their performance is evaluated in terms of common-mode voltage and circulating current. Based on the evaluation, an optimized SVM based on the APOD modulation is proposed for circulating current reduction. Simulation and experimental results are provided in Section IV to validate the effectiveness of the proposed modulation. Conclusions are drawn in Section V.

II. CIRCULATING CURRENT

The operation of parallel inverters provides additional degrees of freedom for the modulation. For instance, a cancellation of current harmonics can be achieved by the application of interleaved modulation methods. Such interleaved operation can be easily applied for carrier-based PWM by shifting the carriers among the inverters by $360^\circ/n$, where n is the number of inverters [7]. For two parallel inverters, it leads to a carrier shift of 180° . Since the switching sequences of the inverters are shifted to each other, a common-mode voltages between both inverters occurs according to:

$$v_{cm} = v_{cm1} - v_{cm2} = \frac{v_{az1} + v_{bz1} + v_{cz1}}{3} - \frac{v_{az2} + v_{bz2} + v_{cz2}}{3}, \quad (1)$$

where the common-mode voltages of the inverters 1 and 2 (v_{cm1} , v_{cm2}) are expressed by the phase-to-neutral voltages v_{kz1} and v_{kz2} ($k = a, b, c$), respectively.

Due to the common dc-link, a circulating current is generated by the common-mode voltage between the inverters:

$$i_{cir} = \frac{3}{2L} \int v_{cm}(t) dt. \quad (2)$$

The problem of circulating current is further illustrated in Fig. 1, where the switching states [POP] and [ONO] are applied as study case. According to (1), the common-mode voltage between both inverters is obtained by the half dc-link voltage. The full common-mode voltage profile depends on the applied modulation technique and is crucial for the circulating current. The impact of modulation techniques on the circulating current has already been well studied in literature for parallel two-level inverters [6], [14]. Different optimized modulation techniques have been proposed to reduce the circulating current while maintaining other grateful features in terms of power quality and switching losses [6], [12], [14], [15]. However, for parallel NPC inverters, where the number of switching states increases, further analysis is required to find the best modulation technique for this application. The analysis will be provided in the next sections.

III. OPTIMIZED MODULATION FOR PARALLELED NPC INVERTERS

In this section, two well-known carrier-based modulation techniques: PD and APOD, are evaluated for parallel NPC inverters. The common-mode voltage and the circulating current between two parallel inverters are analyzed. An optimized SVM technique will be designed based on the superior carrier-based modulation, aiming at circulating current reduction.

A. Division of Sectors and Regions in Space Vector Representation

According to (1) and (2), the common-mode voltage as well as the terminal voltages of both inverters should be obtained for the calculation of the circulating current. Since the switching sequences determine the terminal voltages, all the switching sequences of the both modulation techniques

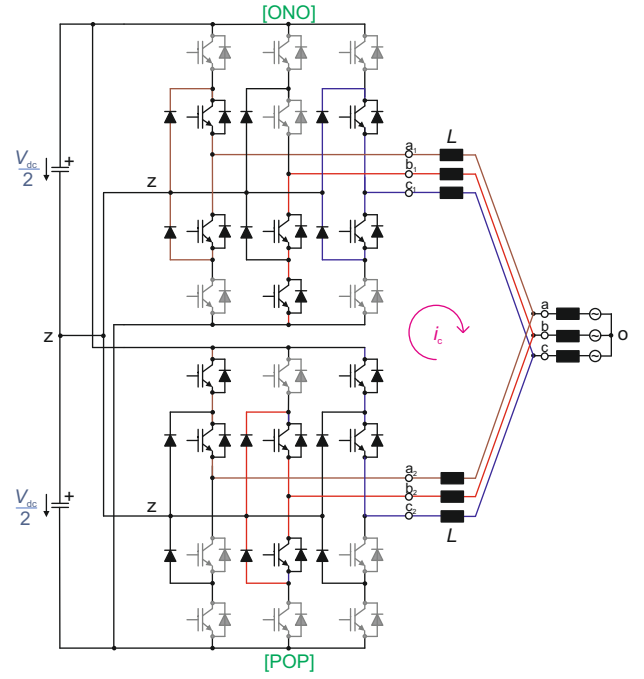


Fig. 1. An example of the common-mode voltage and the circulating current in the parallel NPC inverters.

should be enumerated and utilized for evaluation. For analysis convenience, the division of sectors and regions, which is used in the SVM can be utilized for categorizing the switching sequences. In particular, the switching sequences of the PD modulation is identical to that of the SVM given in [11], [12].

For three-phase fundamental signals, six sectors are divided according to [12]. Depending on the switching sequences, each sector can be further divided into four triangular regions (e.g. 1 to 4 in Sector I). The division of sectors and regions as well as the switching states is given in Fig. 2a. Since the characteristics (e.g. switching states) of each sector are similar to the others, only Sector I has been taken into account for the sake of simplicity. In the switching sequence design for SVM, one small vector among three selected vectors is commonly adopted to minimize the neutral-point voltage deviation [7], and a typical seven-segment switching sequence is obtained. It is worth noting that each small vector can be generated by two switching states (e.g. [OON] or [POO]), which leads to the fact that the region 1 and 2 can be further divided into two subregions as shown in Fig. 2b. As a result, two types of seven-segment switching sequences will be employed in the subregion-a and subregion-b, respectively. For instance, in the Sector I region 1, the seven-segment switching sequences in Sector I-2a and Sector I-2b are [ONN], [OON], [PON], [POO], [PON], [OON], [ONN] and [OON], [PON], [POO], [PPO], [POO], [PON], [OON], respectively.

B. PD vs. APOD under Interleaved Operation

The interleaved operation of two parallel inverters causes undesired circulating current which has to be limited. The circulating currents can be calculated by the common-mode

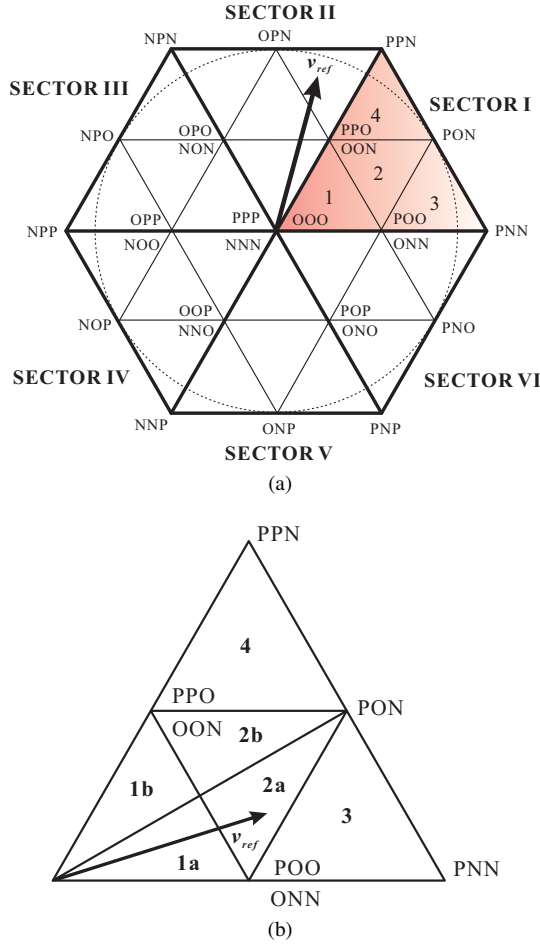


Fig. 2. Division of sectors and regions: (a) six sectors and (b) six regions of Sector I.

voltage between the two inverters according to (2). The common-mode voltage of one inverter can be obtained by the three-phase terminal voltages which are directly linked to the corresponding switching states. For further investigation, the switching sequences of one region of Sector I is considered for both PD and APOD modulation. Based on Sector I-1a, the PWM carriers, the switching states and the terminal voltages are exemplary shown in Fig. 3 (a) and (b), respectively. The duty cycles are represented by d_a , d_b , and d_c , while the terminal voltages are defined as v_{kz1} and v_{kz2} ($k = a, b, c$) for the first and the second inverter, respectively. By taking into account the modulation index m_k , the time durations of turn-on (T_{kz}) and turn-off (\bar{T}_{kz}) can be easily calculated:

$$T_{kz} = |d_k| \cdot T_s \cdot m_k \quad k = a, b, c. \quad (3)$$

$$\bar{T}_{kz} = |1 - d_k| \cdot T_s \cdot m_k \quad k = a, b, c. \quad (4)$$

The corresponding common-mode voltage (v_{cm}) and the circulating current waveform (i_{cir}) between the inverters are depicted in Fig. 3 (c) and (d), respectively ($E = V_{dc}/6$). The maximum common-mode voltage between both inverters occurs during the switching states [ONN] and [POO], generated by PD modulation. The other regions of Sector I are

TABLE I
COMPARISONS OF COMMON-MODE VOLTAGE OF SECTOR I

PD Modulation						
Segment	1a	1b	2a	2b	3	4
1st	$3E$	$3E$	$3E$	$3E$	$3E$	$3E$
2nd	$2E$	$2E$	$2E$	$2E$	$2E$	$2E$
3rd	E	E	E	E	E	E
4th	0	0	0	0	0	0
5th	$-E$	$-E$	$-E$	$-E$	$-E$	$-E$
6th	$-2E$	$-2E$	$-2E$	$-2E$	$-2E$	$-2E$
7th	$-3E$	$-3E$	$-3E$	$-3E$	$-3E$	$-3E$
APOD Modulation						
Segment	1a	1b	2a	2b	3	4
1st	$-E$	E	$-E$	E	$-E$	E
2nd	0	0	0	0	$-2E$	$2E$
3rd	E	$-E$	$-E$	E	$-E$	E
4th	0	0	0	0	0	0
5th	$-E$	E	E	$-E$	E	$-E$
6th	0	0	0	0	$2E$	$-2E$
7th	E	$-E$	E	$-E$	E	$-E$

not further investigated. Nevertheless, the circulating current characteristics of those regions can be easily obtained by the demonstrated method. In Table I the common-mode voltage of all considered switching states is summarized. Since the PD modulation generates a higher common-mode voltage in each segment, the circulating current increases as well compared to the APOD modulation.

C. Design of an APOD-based Space Vector Modulation

Since the APOD modulation shows advantages in the parallel NPC inverters, an APOD-based SVM is proposed in this subsection. According to the carrier-based APOD modulation, all the switching sequences can be derived and presented in Fig. 4. Similar to the conventional SVM technique, the APOD-based SVM is also based on "volt-second balancing" principle, namely, the product of the reference voltage vector v_{ref} and sampling interval T_s equals the sum of the selected vector vectors multiplied by the corresponding dwell time. Instead of synthesis by three nearest stationary vectors, v_{ref} in the APOD-based SVM can be synthesized by four nearest vectors (three nearest stationary vectors and one zero vector). With this consideration, each sector can be divided into two triangular regions as shown in Fig. 4b. For instance, when v_{ref} falls into Sector I-a, the three nearest vectors are V_1 , V_2 , and V_3 , which are represented by the switching states of [POO], [PNN], and [PON], and meanwhile the zero vector V_0 that is represented by the switching state of [OOO] is adopted. For the dwell time calculation, the two following equations are required:

$$\begin{aligned} V_1 T_a + V_2 T_b + V_3 T_c + V_0 T_0 &= v_{ref} T_s \\ T_a + T_b + T_c + T_0 &= T_s. \end{aligned} \quad (5)$$

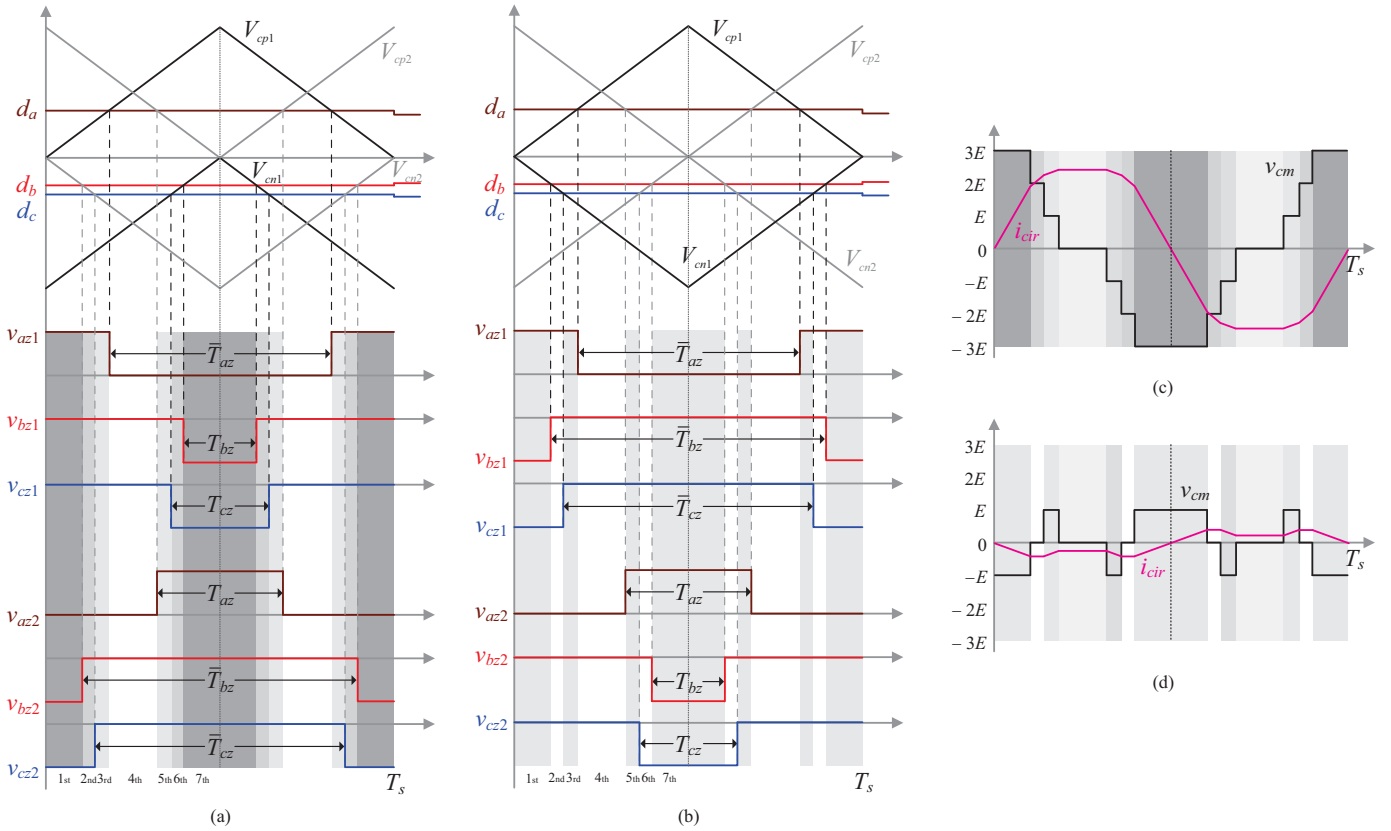


Fig. 3. Terminal voltages of parallel NPC inverters in Sector I-1a, common-mode voltage waveform and circulating current for PD (a,c) and APOD (b,d).

where T_a , T_b , T_c , and T_0 are the dwell times for V_1 , V_2 , V_3 , and V_0 , respectively. Note that, the dwell times are more than the equations which leads to infinite solution from the mathematical point of view. To address this issue, one more equation can be added with the purposes of optimization, for instance, harmonic elimination and dc voltage balancing, etc. In this paper, an example of the APOD-based SVM without other optimization is shown, in which the dwell times are directly derived from the carrier-based APOD technique. It is worth noting that one of the small vectors which is represented by [ONN] in Sector I-a is utilized in conventional SVM but it is neglected in the APOD-based SVM. The combination of [ONN] and [POO] would slightly improve the effects of neutral-point voltage balancing. However, it will cause higher common-mode voltage between two NPC inverters, which is undesirable in parallel NPC inverters.

The switching sequences in all six sectors are summarized in Table II. It can be observed that when v_{ref} crosses the border between every two sectors, the transition does not involve any switching, and an extra switching takes place when v_{ref} moves from region a to b within a sector. From the above features, it can be expected that the switchings and the number of commutations of the APOD-based SVM are similar to those of the conventional SVM but the design and implementation are simpler since less regions as well as stationary vectors are

employed in each sector.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The performance of two parallel NPC inverters with common dc-link under interleaved operation is validated for the different modulation techniques by simulation and experiments. The results and performance evaluation are presented in this section.

A. Simulation Results

To validate the analyses, two parallel NPC inverters with common dc-link are simulated in the MATLAB/Simulink environment with the PLECS toolbox. Both the PD and the APOD techniques are tested under interleaved operation. The dc-link voltage is 700 V and the nominal ac voltage is 230 V (rms); and the switching frequency is 10 kHz. In the open-loop control case, the modulation index of $m = 0.7$ is considered.

Comparisons in terms of total current (i_{total}) of two NPC inverters, common-mode voltage, and circulating current are shown in Fig. 5a and Fig. 5b. It can be seen that the performance of total currents using two modulation techniques are identical in terms of waveform quality and current ripple. The THDs of both waveforms are evaluated and are 3.05 % for both techniques. Nevertheless, the common-mode voltages and the circulating currents using different modulation techniques are different. It is obvious that both the common-mode voltage

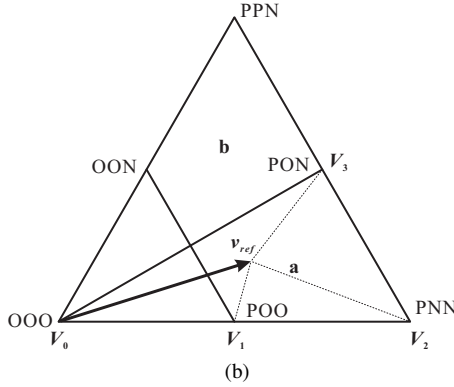
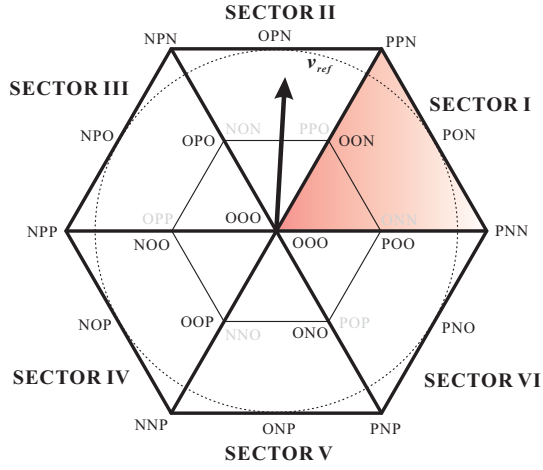


Fig. 4. APOD-based space-vector modulation: (a) division of sectors and regions and (b) division of two regions of Sector I.

and the circulating current of the PD modulation technique are higher than that using the APOD modulation. It is worth noting that the voltage vector is sweeping region 2, 3, and 4 of every sector (in case of the PD) in every cycle according to the modulation index. As a result, it can be expected that the common-mode voltage of the PD modulation would be 3/2-times to that of the APOD in region 3 and 4, and 3-times to that of the APOD in region 2, according to Table I, which is validated by the common-mode voltage waveforms in Fig. 5.

The results of the APOD-based SVM is presented in Fig. 5c. The proposed APOD-based SVM has been implemented in both NPC inverters with interleaved switching sequences. It can be seen that the performance of the proposed SVM in terms of total current, common-mode voltage, and circulating current is identical to that of the carrier-based APOD modulation, which indicates it to be an optimal SVM technique for parallel NPC inverters.

B. Experimental Validation

In Fig. 6 the developed laboratory setup for experimental evaluation is depicted. Two NPC inverters are connected in parallel, where the power units are realized by the IGBT module *F3L75R07W2E3_B11* from Infineon with a current rating of 75 A. Each module is driven by the dedicated eval-

TABLE II
SWITCHING SEQUENCE OF APOD-BASED SVM

Sector I							
a	[PNN]	[PON]	[POO]	[OOO]	[POO]	[PON]	[PNN]
b	[PPN]	[PON]	[OON]	[OOO]	[OON]	[PON]	[PPN]
Sector II							
a	[PPN]	[OPN]	[OON]	[OOO]	[OON]	[OPN]	[PPN]
b	[NPN]	[OPN]	[OPO]	[OOO]	[OPO]	[OPN]	[NPN]
Sector III							
a	[NPN]	[NPO]	[OPO]	[OOO]	[OPO]	[NPO]	[NPN]
b	[NPP]	[NPO]	[NOO]	[OOO]	[NOO]	[NPO]	[NPP]
Sector IV							
a	[NPP]	[NOP]	[NOO]	[OOO]	[NOO]	[NOP]	[NPP]
b	[NNP]	[NOP]	[OOP]	[OOO]	[OOP]	[NOP]	[NNP]
Sector V							
a	[NNP]	[ONP]	[OOP]	[OOO]	[OOP]	[ONP]	[NNP]
b	[PNP]	[ONP]	[ONO]	[OOO]	[ONO]	[ONP]	[PNP]
Sector VI							
a	[PNP]	[PNO]	[ONO]	[OOO]	[ONO]	[PNO]	[PNP]
b	[PNN]	[PNO]	[POO]	[OOO]	[POO]	[PNO]	[PNN]

uation drive board (*F3L030E07-F-W2*). Filter inductors of 1.8 mH are applied in each phase to limit the current ripple of the inverter and the circulating current. Each NPC inverter is controlled by a local board for signal processing and measurement with high bandwidth. A centralized open-loop control is implemented in a master control board (Xilinx Zc702 evaluation board), being able to adjust the modulation index of both inverters online. The communication between the master control board and the local board is realized by optic fiber cables.

The two parallel NPC inverters are performed under interleaved operation with a dc-link voltage of 700 V and a switching frequency of 10 kHz to compare the performance of both modulation methods (PD and APOD). The three-phase total currents are compared in Fig. 7, showing a similar performance in terms of current ripple and power quality. The obtained THD values of the current waveforms are 15.95 % (PD) and 16.14 % (APOD), respectively.

For evaluation of circulating currents, a modulation index of $m = 0.98$ has been applied to both inverters, corresponding to the voltage space vector regions 2, 3, 4. The common-mode voltage of the PD modulation would be 1.5-time higher compared to APOD during most of the cycle (region 3 and 4) and be 3-time higher in short periods (region 2) according to the analysis in Section III and Table I. The measured circulating current waveforms are depicted in Fig. 8, confirming the increased circulating current by PD modulation, especially in the adjoining areas between two rhombi (related to region 2 of all sectors).

It can be concluded that the total current quality for PD and APOD is comparable under interleaved operation. However, the circulating current between the two inverters is signifi-

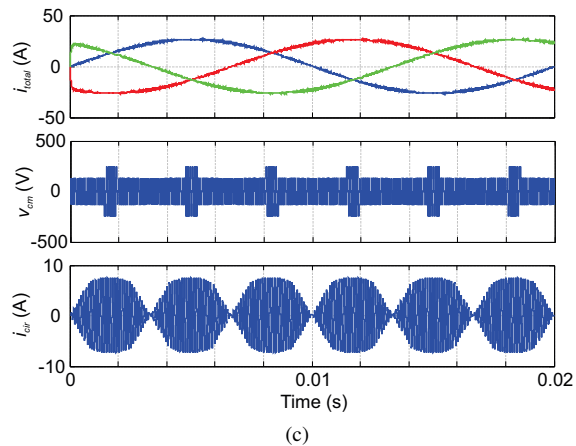
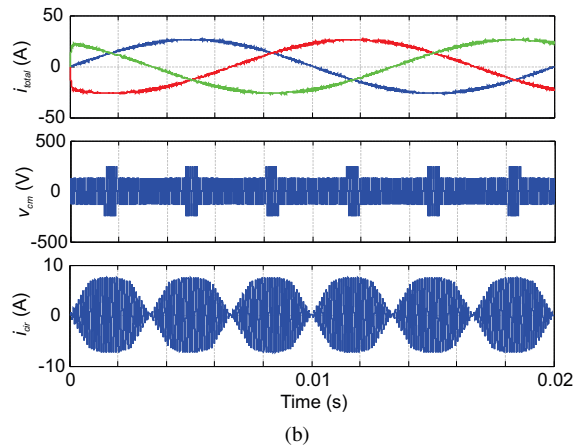
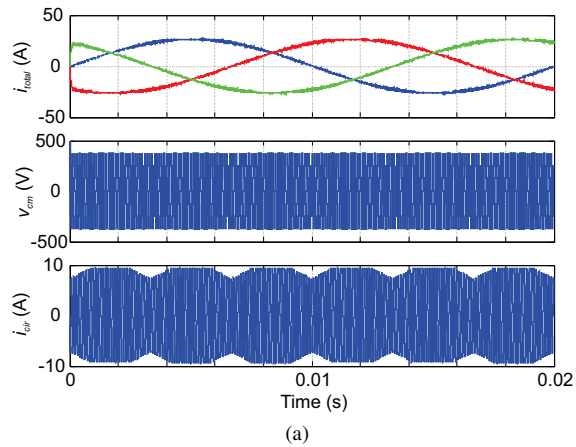


Fig. 5. Performance evaluation of two parallel NPC inverters during interleaved operation using different modulation (modulation index: $m = 0.7$): (a) carrier-based PD, (b) carrier-based APOD, and (c) APOD-based space-vector modulation.

cantly reduced by the APOD modulation, especially for small voltage vectors (region 1 and 2). For this reason, the APOD modulation can be considered as the preferred choice for the application of parallel NPC inverters with common dc-link. As a result, it can be a basic modulation for SVM design in such application.

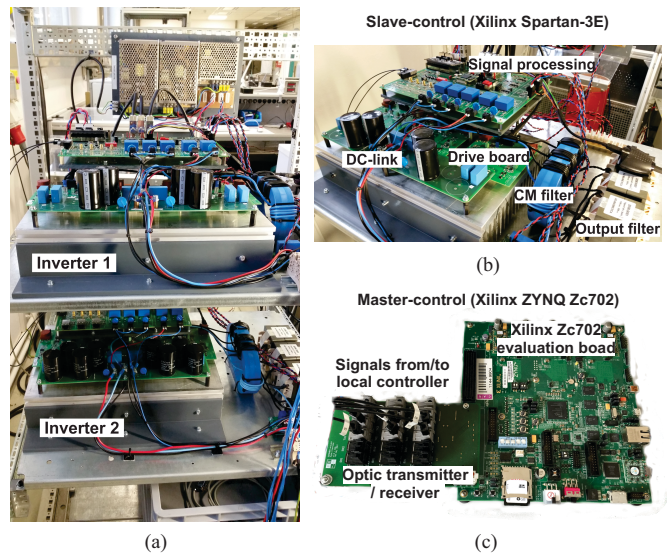


Fig. 6. Experimental Setup: (a) overall prototype, (b) details of inverter 1 as well as the slave control board, and (c) master control board.

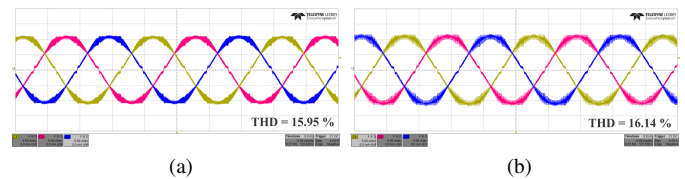


Fig. 7. Three-phase total current of two NPC inverters by using different modulation techniques (modulation index: $m = 0.85$, time: 5 ms/div, current: 5 A/div): (a) PD and (b) APOD.

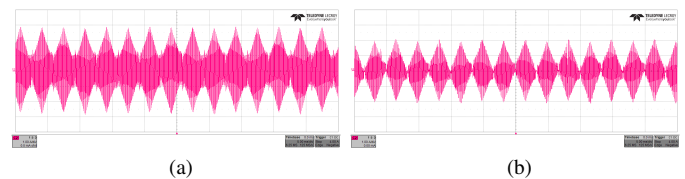


Fig. 8. Circulating current between the parallel NPC inverters using different modulation (modulation index: $m = 0.98$, time: 5 ms/div, current: 1 A/div): (a) PD and (b) APOD.

V. CONCLUSIONS

The interleaved operation of parallel NPC inverters has been used for improving the quality of the current waveform. However, in the case of a common dc-link, the circulating current issue emerges and could lead to critical problems. To minimize the circulating current of parallel NPC inverters, this paper has investigated two common modulation techniques for NPC inverters (PD and APOD) and then found a superior solution for SVM design. Though it is well-known that the PD modulation offers better performance in a single NPC inverter, the APOD modulation has the advantage of lower circulating current in the parallel NPCs under interleaved operation. In this regard, an APOD-based SVM is proposed with full switching sequences and design criterion. It is shown

that the proposed SVM can not only maintain lower circulating current but also offers possibility of further optimization. Simulation and experimental results are provided to compare the two carrier-based modulation techniques and to verify the effectiveness of the proposed SVM.

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