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Stability Analysis of Synchronization of Parallel Power Converters

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Abstract—Interactions between power electronic converters are typically investigated by means of impedance-based model analysis. The effects of the PLL are usually neglected, but recent studies have shown the importance of including those effects for stability analysis purposes. This paper focuses on the investigation of interactions between synchronization units of converters operating in parallel. The impedance-based approach is used for the investigation in the frequency-domain. The converters are supposed to share the same point of common coupling (PCC) and the characteristic of the grid at the connection point is crucial for determining the effects of the interactions between the operating units. In order to isolate the effects of the synchronization, the converters is modeled as a current sources, whose reference currents are calculated using the angle detected by their PLLs. Time-domain simulations are performed as well as experimental laboratory tests in order to validate the presented analysis.

I. INTRODUCTION

In the past decades the issues related to the synchronization of power converters to the main utility grid have been deeply investigated due to the increasing number of operating units and the always more demanding grid codes. Indeed, maintaining the connection to the grid during transients and faults and in certain cases even providing support by injecting specific amount of current become standard requirements for grid connected converters. Different synchronization strategies have been proposed in the past decades both for single-phase as well as for three phase applications [1]-[6]. The commonly adopted solution is the use of a phase-locked loop (PLL) for detecting the angle of the grid voltage and the synchronous reference frame PLL (SRF-PLL) is among the techniques most widely proposed in the literature [5], [7]. It provides excellent results under balanced and undistorted grid conditions, but results very sensitive to unbalances and harmonics disturbances in the grid voltage [3], [4]. The easiest solution to overcome these drawbacks consists in decreasing the bandwidth of the PLL. Other solutions have been proposed in literature, which consist in the introduction of filters in the loop [7]. Also these expedients in most of the cases result in a lower bandwidth compelling to a compromise between dynamic performances and disturbance rejection. The inevitable reduction of the PLLs bandwidth has been considered to be the main drawback due to the fact that controllers for modern power converters are usually implemented in synchronous rotating reference frames, requiring an accurate knowledge of the grid angle. Recent works have proposed new filtering processes and their respective optimal tuning in order to obtain accurate phase tracking without compromising the bandwidth of the synchronization unit [5]-[6]. The stability of grid connected converters has been investigated by means of impedance-based analysis [8]-[10]. Some researchers have adopted this approach in order to investigate the interaction between controller loops of voltage source converters (VSCs) and their output filters or between parallel operating VSCs, neglecting the impact of the synchronization units [11], [12]. Recently, the importance of the synchronization unit for the stability and performance of the control has been shown and therefore should be designed carefully in order to avoid interactions with the other loops of the controller [9], [13]-[15]. It is often taken for granted that multiple PLLs in a system may compete each other leading to instability [16], but actually this issue has not been properly investigated in literature. Aim of this work is the investigation of interactions between synchronization units of parallel operating converters by means of an equivalent impedance-based approach. It will be shown that despite a proper tuning of the PLL, the presence of electrically close converters having synchronization units designed with unknown characteristics may affect the stability of the converter, which is stable when operating alone. Furthermore, these effects are more accentuated when decreasing the short circuit ratio (SCR) of the grid. The paper is organized as follows: in Section II the modelling of parallel inverters for stability analysis purposes is presented and the PLL's design procedure will be discussed, in Section III a practical case will be analyzed. In Section IV time-domain simulations and experimental laboratory tests will be presented so as to validate the performed analysis. Finally, conclusions will be drawn in Section V.

II. MODELLING OF PARALLEL INVERTERS FOR STUDYING SYNCHRONIZATION ISSUES

A. System under Study

In order to investigate the interactions between synchronization units of parallel operating converters, a simplified system composed of two inverters sharing the same PCC is

considered. The two converters have fixed reference current setpoints according to the desired injected amount of active and reactive power into the grid. Each converter measures the voltage at the point of common coupling (PCC) and tries to extract the grid angle. In order to isolate the effects of the PLL from the other controllers loop (current control, DC-Link, active power control, voltage feed-forward, etc...), the converter can be assumed to behave as a current source, whose inputs are calculated by transforming the reference currents from *dq* to the *abc* reference frame by using the angle estimated by the PLL. The grid is modelled just using a simple Thevenin equivalent, where Z_g represents the equivalent grid impedance seen by the converter at the PCC. Interaction effects are investigated according to variations of PLL bandwidths as well as SCR of the grid. In fact, in the case of a very strong grid, the converters are connected to a nearly ideal voltage source and are not coupled with each other, but increasing the values of the grid impedance the coupling effects between the two converters become more significant.

In Fig. 1 the equivalent impedance-based model of the system under study is shown. The converter is represented by a Norton equivalent circuit, namely a current source I_{inv} in parallel with its output admittance Y_{out} [8]-[9]. This element includes the effects of the synchronization unit and its derivation will be presented in the following.
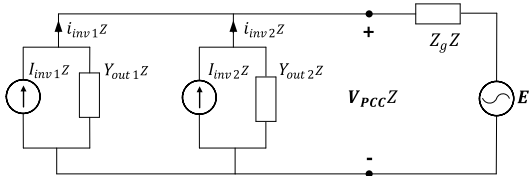

Figure 1: Equivalent model of the system under study.

B. Linearization of the PLL equations

The derivation of an equivalent input admittance term from the linearization of the PLL equations has been recently investigated [9], [13]. In this paper the approach presented in [13] was adopted and will be briefly explained in the following. In Fig. 2(a) the structure of a standard SRF-PLL is reported. It is basically composed of three different stages: the phase detector (PD), the loop filter (LF) and the voltage controlled oscillator (VCO) [1], [2], [7], while in Fig. 2(b) its linearized model is shown.

The measured grid voltages are transformed in *dq* coordinates by means of Park's transformations using the estimated angle θ_{PLL}. The standard implementation of the LF is normally a simple PI controller, whose transfer function is expressed below:

$$LF(s) = K_p + \frac{K_i}{s}, \tag{1}$$

with K_p and K_i representing the proportional and integral gain respectively. The VCO is usually an integrator with the

feed-forward gain ω_0 (rated grid frequency). In steady-state the estimated angle θ_{PLL} corresponds to the real grid angle θ_g, while during transients the two angles may deviate from each other. Therefore, due to the presence of the PLL, we can consider having two separate reference frames, one rotating at speed ω_g (instantaneous grid frequency) and the other one rotating at the speed ω_{PLL} estimated by the synchronisation unit. A picture of the described situation is reported in Fig. 3.

According to the generalized reference frame theory, it is always possible to relate variables in one reference frame to variables in another reference frame rotating at different speeds by using the following transfer matrix:

$$T_{\Delta\theta} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix}, \tag{2}$$

where $\Delta\theta$ is the angle difference between the two rotating reference frames, therefore:

$$\begin{bmatrix} V_d^{PLL} \\ V_q^{PLL} \end{bmatrix} = T_{\Delta\theta} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad ; \quad \begin{bmatrix} I_d^{PLL} \\ I_q^{PLL} \end{bmatrix} = T_{\Delta\theta} \begin{bmatrix} I_d \\ I_q \end{bmatrix} . \tag{3}$$

Eq. (3) can be linearized for small-signal perturbations as:

$$\begin{bmatrix} \Delta V_d^{PLL} \\ \Delta V_q^{PLL} \end{bmatrix} = \begin{bmatrix} \Delta V_d + V_q \Delta\theta_{PLL} \\ -V_d \Delta\theta_{PLL} + \Delta V_q \end{bmatrix} \quad ; \tag{4}$$

the output angle is obtained [13]:

$$\Delta\theta_{PLL}(s) = \Delta V_q^{PLL} \frac{LF(s)}{s}, \tag{5}$$

and substituting (5) into (4), results:

$$\Delta\theta_{PLL}(s) = \Delta V_q \frac{LF(s)}{s + V_d LF(s)} = H_{PLL}(s)\Delta V_q. \tag{6}$$

Eq. (6) describes the relation between a small perturbation of the input grid voltage ΔV_q and the output angle $\Delta\theta_{PLL}$ of the SRF-PLL. Perturbations of the grid voltages have an impact on the detected angle θ_{PLL} and therefore everywhere in the control where a transformation is involved [8], [12], [14]. Repeating the same linearization process for the currents in (3), the following relation will be obtained:

$$\begin{bmatrix} \Delta I_d^{PLL} \\ \Delta I_q^{PLL} \end{bmatrix} = Y_{out} \begin{bmatrix} \Delta V_d \\ \Delta V_q \end{bmatrix} + \begin{bmatrix} \Delta I_d \\ \Delta I_q \end{bmatrix}, \tag{7}$$

where with Y_{out} the equivalent input admittance matrix of the converter is indicated:

$$Y_{out} = \begin{bmatrix} 0 & I_q H_{PLL}(s) \\ 0 & -I_d H_{PLL}(s) \end{bmatrix}, \tag{8}$$

and I_d and I_q represent the converter currents in the θ_g reference frame, while I_d^{PLL} and I_q^{PLL} the converter currents in the θ_{PLL} reference frame.
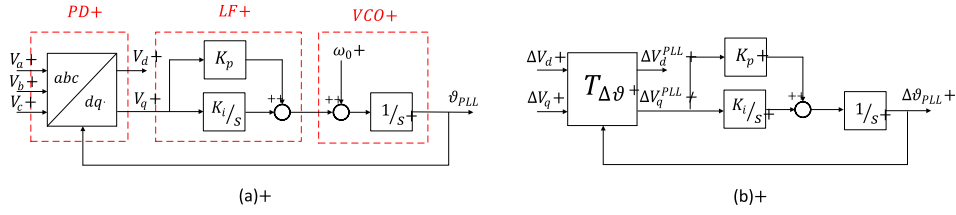
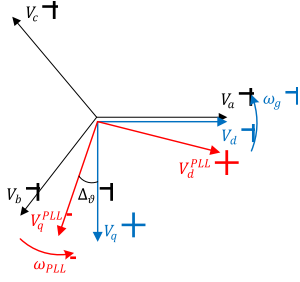Figure 2: (a) Scheme of a standard SRF-PLL, (b) linearized model of the SRF-PLL.

Figure 3: Grid voltages vectors (black), dq rotating reference frame (blue), dq PLL rotating reference frame (red).

C. Impedance-Based Stability Analysis

Assuming that the grid impedance shown in Fig. 1 has a resistive-inductive behaviour, $Z_g(s)$ is expressed by the following equation:

$$Z_g(s) = \begin{bmatrix} L_g s + R_g & -\omega L_g \\ \omega L_g & L_g s + R_g \end{bmatrix} \quad , \quad (9)$$

with L_g and R_g representing the inductive and resistive terms respectively. The output current of the Inverter 1 can be calculated as:

$$I_{inv1}(s) = I_{ref1} + Y_{out}(s)V_{PCC}. \quad (10)$$

Due to the fact that the inner current control loop is neglected, (10) differs from the expressions used in [9]-[12], where the closed loop current control transfer function has to be considered. Considering the case when only the first inverter is in operation, it is valid $V_{PCC} = E - Z_g(s)I_{Inv1}$, therefore:

$$I_{inv1}(s) = H(s)[I_{ref1} + Y_{out}(s)E], \quad (11)$$

with

$$H(s) = \frac{1}{1 + \frac{Y_{out}(s)}{Y_{geq}(s)}}, \quad (12)$$

where Y_{geq} (s) in this case simply corresponds to the inverse of Z_g. When instead two (or more) inverters are operating in parallel, the same approach can be adopted by including

the effects of the other converters on the equivalent grid impedance $Y_{geq}(s)$, such as [12] :

$$\begin{cases} Y_{geq}(s) = \frac{1}{Z_g(s)} & one\ inverter \\ Y_{geq}(s) = \frac{1}{Z_g(s)} + Y_{out2} + ... + Y_{outn} & n\ inverters \end{cases} \quad (13)$$

Differently from the cases analyzed in [11]-[12], the system is not anymore a SISO system, rather a MIMO one. Therefore in this work the stability of the overall system was assessed by looking at the eigenvalues of the closed loop transfer function $H(s)$ [9].

D. PLL's Design

The SRF-PLL design has been addressed in many works [2], [4], [7]. The linearized model of the SRF is basically a second order transfer function, whose open and closed loop transfer functions are reported below [2]:

$$OP(s) = V_{in}\frac{K_p + \frac{K_i}{s}}{s} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega n s + \omega_n^2}, \quad (14)$$

$$CL(s) = V_{in}\frac{s^2}{s^2 + K_p s + K_i} = \frac{s^2}{s^2 + 2\zeta\omega n s + \omega_n^2}, \quad (15)$$

where V_{in} is the amplitude of the input voltage and K_p and K_i are the proportional and integral gains of the previously introduced PI controller respectively. Being a second order system, it is often recommended to set the damping factor $\zeta = 1/\sqrt{2}$ [1], [2], [4]. Fixing the settling time to a determined value, the parameters K_p and K_i can be calculated as in the following [2]:

$$K_p = \frac{9.2}{t_s} \qquad and \qquad K_i = \frac{21.16}{t_s^2\ \zeta^2}\ . \quad (16)$$

The settling time t_s of the PLL is one of the most crucial tuning parameters and it is directly related to its bandwidth. Unfortunately, no clear specifications for this parameter can be found in literature. In [7] the behaviours of three PLLs with different bandwidths have been compared under different grid conditions. Some simulation results of two PLLs having $f_c = 700$ Hz and $f_c = 10$ Hz respectively are shown in Fig. 4 and Fig. 5, where f_c indicates the frequency corresponding to $|OP(s)| = 0$ dB (cross-over frequency). The two bandwidths have been chosen so as to correspond to the highest and the lowest in [7]. Their behaviours are compared for two different

cases: perfectly sinusoidal grid voltages without harmonic distortion and unbalanced grid voltages with 5th and 7th harmonics components. Fig. 4 shows the phase angle detected by the PLLs, while Fig. 5 shows the error $\Delta_{\omega g}$ and V_q for a step of the grid frequency of 2 Hz. It can be clearly seen how disturbances propagate in the angle detected by the fastest PLL (Fig. 4 (d)), as well as in the estimated grid frequency (Fig. 5 (c)). However It has a much faster tracking performance, but at the cost of not attenuating the impact of imbalances and harmonics when compared to the slow one (Fig. 5).
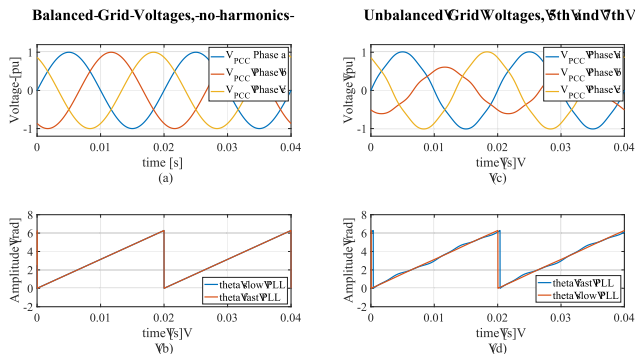

Figure 4: (a) Grid voltages without harmonic distortion, (b) detected phase angles by the two PLLs for balanced voltages, (c) unbalanced grid voltages with 2 % 5th and 1 % 7th harmonics,(d) detected phase angles by the two PLLs with unbalanced voltages.
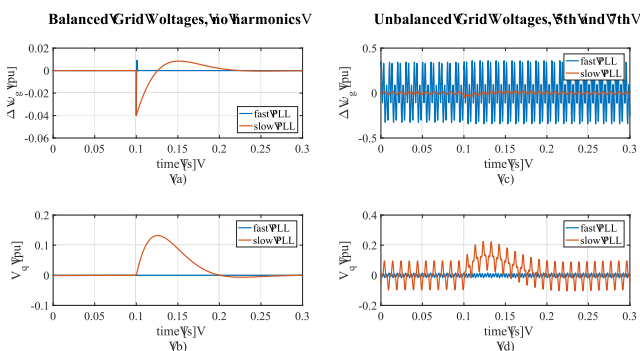

Figure 5: (a) $\Delta_{\omega g}$ and (b) V_q for a step of grid frequency of 2 Hz and grid voltages of Fig. 4(a); (c) $\Delta_{\omega g}$ and (d) V_q for a step of grid frequency of 2 Hz and and grid voltages of Fig. 4(c)

III. TEST CASE DESCRIPTION

The case of two parallel operating converters has been investigated. It is assumed that the two inverters are injecting their rated power, identical for the two of them. The power of each inverter can be calculated as:

$$P_{rated} = \frac{S_{sc}}{2\ SCR}\ . \qquad (17)$$

In Table I the simulated system parameters are listed. The results obtained when only one inverter is in operation are compared to the case when both of them inject power into the grid. Assuming that Inverter 1 is injecting its rated active

power, the SCR of the grid and the BW of its PLL have been varied in the ranges: f_c = [10 Hz ; 700 Hz] and SCR=[1 ; 3.5] respectively. In Fig. 6 stable and unstable operating regions are shown. For example, when only one inverter is in operation, operating points above the blue line are unstable. The red line is corresponding to the stability borders when the two inverters are operating in parallel injecting both their maximum rated power, while f_c of Inverter 2 has been fixed to 100 Hz and f_c of Inverter 1 is varied in the range previously mentioned. It can be clearly seen how in this case the stable area is reduced.

Table I: System Parameters

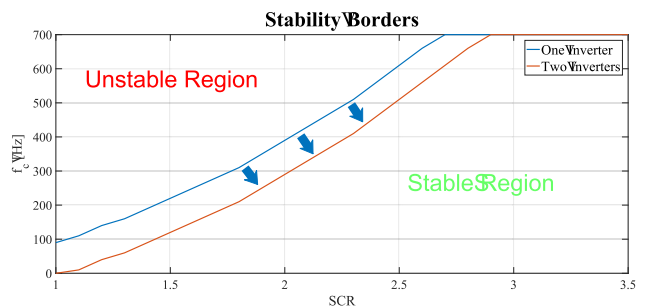| Description	Symbol	Value
Grid Short circuit power	S_{sc}	1 MVA
Grid line-to-line voltage	V_{LL}	400 V (rms)
X/R grid impedance ratio	X/R	10
Rated grid frequency	f_g	50 Hz

Figure 6: Stability borders calculated from eigenvalues analysis of $H(s)$, (blue) only inverter 1 in operation, (red) both converters in operation and PLLs f_c of inverter 2 = 100 Hz.

IV. ANALYSIS VALIDATION

In this Section the results obtained from the frequency-domain analysis will be validated through time-domain simulations and subsequently experimental results will be presented in order to enforce the statements presented in this work.

A. Time-Domain Simulations

Taking Fig. 6 as reference, the case corresponding to a SCR of 2 was simulated. When only Inverter 1 is in operation, its PLL bandwidth can be increased until $f_c \approx 390$ Hz without causing any instability. Instead when the inverter is operating in parallel with another one, whose PLL's cross-over frequency is $f_c = 100$ Hz and is also injecting the same power into the grid, the system becomes unstable, unless the bandwidth of inverter 1 will be further reduced below $f_c \approx 290$ Hz. This condition was simulated in Matlab/Simulink/PLECS and the results are shown in Fig. 7. First the converter is injecting its rated current and its PLL's bandwidth was fixed to a precautionary low value. At $t = 0.5s$ the parameters of the PLL has been modified in order to correspond to a f_c of 300 Hz. Fig. 7(a) and (b) are showing the simulated PCC voltages and the converter currents respectively when only inverter one is in operation and the second inverter is switched off. In Fig. 7(c)

and (d) the same quantities are reported for the case when Inverter 2 is also in operation. The analytical model was able to correctly predict the instability.
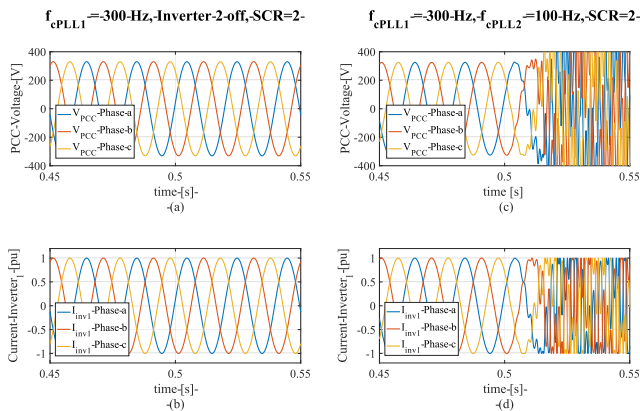

Figure 7: (a)-(b) PCC voltages and Inverter 1 currents when Inverter 1 is injecting its rated current and Inverter 2 is off, (c)-(d) PCC voltages and Inverter 1 currents when Inverter 1 and inverter 2 are injecting their rated currents.

B. Experimental Results

Experimental results have been carried out in a laboratory environment to further confirm the validity of the performed analysis. In order to reproduce a similar condition to the one investigated in this work, the laboratory setup shown in Fig. 8(b) and schematized in Fig. 8(a) was implemented. Two converters Danfoss Series FC-302, 4KW rated power, operating with a switching frequency of 5 KHz having an output inductive filter have been used to emulate the current sources. The internal current control loop of the two converters, indicated as Inverter 1 and inverter 2 in Fig. 8(a), was implemented using PI controllers, whose parameters have been tuned in order to have a very high bandwidth to decouple it from the dynamic of the PLL. Furthermore no voltage feedforward was implemented. Each converter is equipped with an additional transformer in order provide galvanic isolation. The control algorithms of the two converters have been implemented in a dSPACE control Desk DS1202 MicroLabBox. Another converter Danfoss FC-302 of 15KW has been used in order to emulate the grid, whose open loop voltage control was implemented in another dSPACE control Desk of the same type and with the same switching frequency as for the other two inverters. The switch indicated as $S1$ has been used to additionally connect Inverter 2 in parallel to Inverter 1, while $S2$ has been used to switch in series additional inductors so as to emulate a decrease of the SCR of the grid. The Setup parameters are listed in Table II.

Four different cases have been investigated. First only Inverter 1 was connected to the grid injecting only d-component of the current $I_d = 7A$, corresponding to a value of P $\approx$ 3.4 KW. $S1$ was switched off and $S2$ in Position 1. Successively inverter 2 was connected in parallel to inverter 1, also injecting the same amount of power and having the

Table II: System Parameters

Description	Symbol	Value
Inverters 1 and 2 rated powers	$P_{n1} = P_{n2}$	4 KW
Grid emulator rated power	P_{n3}	15 KW
Grid line-to-line voltage	V_{LL}	400 V (rms)
Rated grid frequency	f_g	50 Hz
Filter inductance Inv. 1 and 2	$L_{f1} = L_{f2}$	5 mH
Filter inductance grid emulator	L_{f3}	1.5 mH
Impedance Trafo 1 and 2	$L_{T1} = L_{T2}; R_{T1} = R_{T2}$	0.5 mH; 0.5 Ω
Impedance Trafo 3	$L_{T3}; R_{T3}$	0.3 mH; 0.4 Ω
Additional grid inductance	L_{g2}	2.5 mH
Inverters switching frequency	f_{sw}	5 KHz

same control parameters both for the PLL as well as for current control. The third configuration was similar to the first one but the additional inductor L_{g2} was introduced in series so as to increase the total resulting grid impedance. Similarly to the second configuration, in the fourth case the two inverters were operating in parallel but with increased grid impedance. For each configuration the parameters of the PLL were slowly modified in order to increase its bandwidth until the instability was reached. In Table III the cross-over frequencies of the different PLL configurations, which were causing the instability in the different examined cases are listed, while in Fig. 9 the open loop transfer functions are shown. In the first case the bandwidth needed to be increased until $f_c = 790$ Hz in order to cause instability, while in the last configuration a PLL tuning corresponding to $f_c = 167$ Hz was already enough. In Fig. 10 some measurements results are reported for the first two examined cases. Experimental results confirm the same behaviour observed through the analytical investigation.

Table III: Stability Borders

	One Inverter	Two Inverters
Standard Grid impedance	$f_c = 790$ Hz	$f_c = 520$ Hz
Increased grid impedance	$f_c = 502$ Hz	$f_c = 167$ Hz

V. CONCLUSION

Interactions between PLLs of parallel operating converters have been considered as one of the main challenges for inverter dominated power systems. However this topic has not been yet properly investigated in literature. In this paper this issue was assessed by isolating the effects of the PLL from the other controllers of the grid connected VSC. For this purpose the converter was modeled as a current source, whose reference current has been generated by using the angle detected by a standard SRF-PLL. It has been observed that the tuning of the PLL is important for the system stability, especially for low grid SCR. Furthermore, this situation may be compounded by the presence of another PLL nearby, perhaps with unknown bandwidth. The presented results are validated first through time-domain simulations and subsequently by means of laboratory experiments.
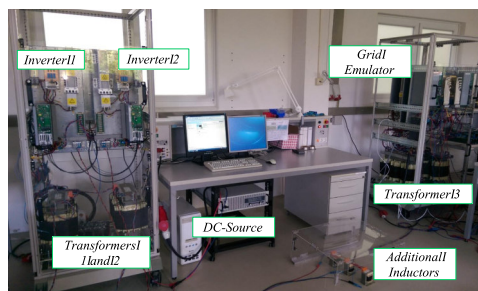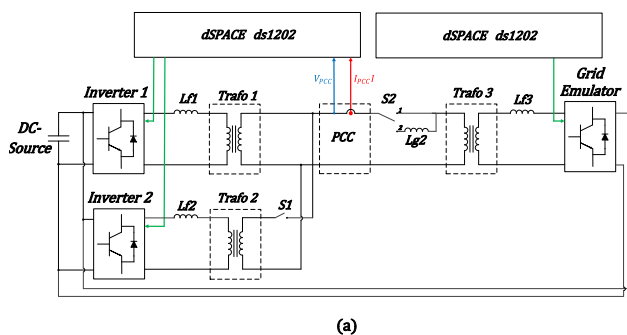
Figure 8: (a) Scheme of the laboratory setup used for the tests, (b) picture of the laboratory setup.
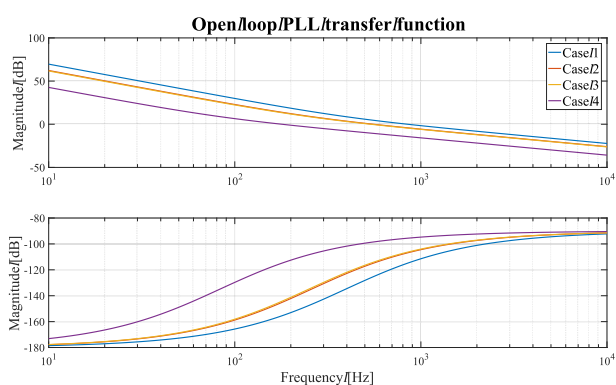

Figure 9: Open loop transfer functions of the PLL configurations that have caused the instability in the four different cases, (blue) case 1, (red) case 2, (yellow) case 3, (violet) case 4.
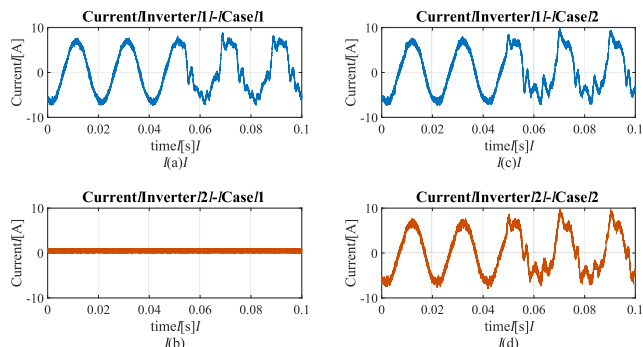

Figure 10: Ocilloscope measurements, Case 1:(a) Phase current Inverter 1, (b) Phase current Inverter 2, Case 2:(c) Phase current Inverter 1, (d) Phase current Inverter 2.

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