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Comparative Analysis of Multiple Active Bridge Converters Configurations in Modular Smart Transformer

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Abstract—In this work, the quadruple active bridge dc-dc converter (QAB) is proposed to be used as a building block to implement the dc-dc stage of a Smart Transformer (ST). Different configurations (symmetrical, asymmetrical, rated for voltage/power) for this converter are considered for investigation. Four different architectures of ST, including one based on the Dual Active Bridge (DAB) converter as a benchmark and three based on the QAB converter, are presented and compared in terms of cost, efficiency, reliability and implementation complexity. As an additional contribution, different semiconductor technologies (silicon IGBT and silicon carbide MOSFETs) are evaluated in order to verify their impact on ST application. The design for each architecture is described and the results are compared. In order to validate the theoretical analysis developed in the paper, a 20 kW prototype was built and experimented.

Index Terms—Dc-dc converter, multiple active bridge converter, multiwinding transformer, smart Transformer.

I. INTRODUCTION

The high penetration of distributed generation and the integration into the grid of new loads (e.g. electric vehicles) has changed the distribution electric system and new challenges have emerged. Among them, the reverse power flow condition, storage integration, management of hybrid grids (dc and ac) and power quality improvement are highlighted [1]–[4]. Smart Transformer (ST), a power electronics-based system with advanced control and communication functionalities, is a promising solution to the aforementioned problems [1].

One of the biggest challenge of this system lays on the implementation of the dc-dc stage, responsible for the connection between medium (MV) and low voltage (LV) dc sides through medium/high frequency (MF/HF) galvanic isolation. Hence, this stage has requirements, such as: high voltage capability in the MV side, high current in the LV side, high voltage isolation, decoupling between the MV dc side and the LV dc side, power flow control, as well as overload and short-circuit protection (working as a dc breaker to protect load/source/microgrid connected to the LV dc-link) [1]–[5]. To meet all of them, the modular architecture brings several advantages, like fault tolerant capability by using redundant modules concept, scalability in power and voltage, reduced dv/dt and di/dt (low EMI emission and isolator stress on

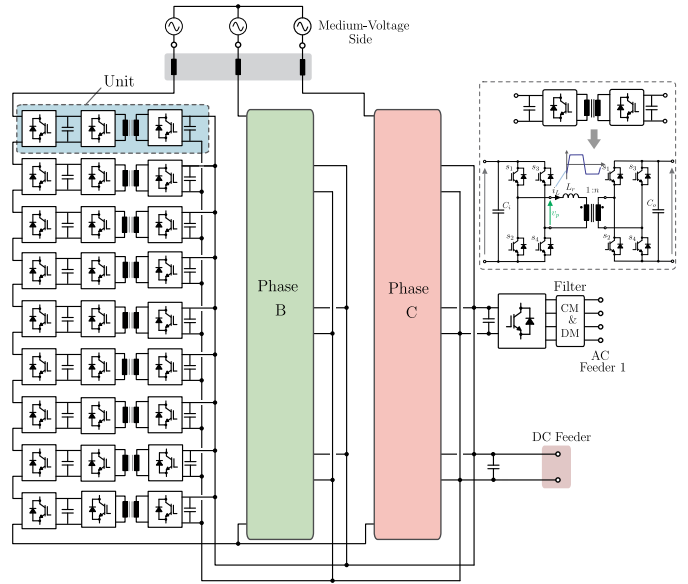


Figure 1. Modular smart transformer architecture using the dual active bridge converter as a building block of the dc-dc stage.

the HF transformer) and the possibility to use standard low voltage/current rating devices. For these reasons, modular architectures are preferable for ST applications.

Based on this approach, several dc-dc converters have been investigated to be used as a building-block of the dc-dc stage, but the Dual-Active-Bridge (DAB) has received more attention, due to its advantages of soft-switching, high efficiency and high power density [3]–[5]. Fig. 1 depicts the modular ST using the DAB converter as a basic cell of the dc-dc stage. This converter, that is composed of two active bridges connected to a high frequency transformer, was generalized in [6]–[9], where more bridges were connected to a multiwinding transformer, leading to the concept of the multiple-active-bridge (MAB), as shown in Fig. 2 (a). The MAB converter presents a reduced number of transformers and modules, when compared to the design based on DAB, while still preserving the same advantages. Consequently, the MAB converter became an attractive solution in ST application, as presented in [1], [2], [8], and this converter was deeply investigated in [8], where four active bridges, named Quadruple-Active-Bridge (QAB), were employed.

The QAB converter has the degree of freedom for the connection: symmetrical (two input and two output) or asym-

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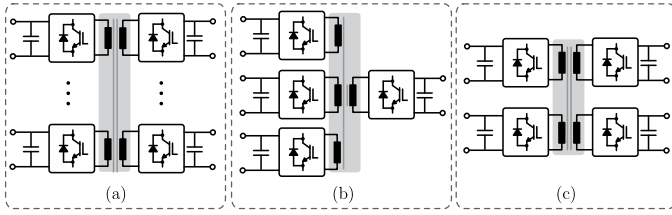


Figure 2. Multiple-Active-Bridge converter topology and the particular case of four bridges (Quadruple-Active-Bridge, QAB): (a) MAB topology, (b) asymmetrical configuration of the QAB converter, (c) symmetrical configuration of the QAB converter.

metrical (three input bridges and one output bridge), as shown in Fig. 2, but the peculiarities and advantages of each of them have not yet been discussed on the literature. This work uses the QAB converter as a building block of the dc-dc stage of the modular ST, where the possible configurations are investigated. Therefore, the configurations are analyzed and compared in term of efficiency, cost, reliability and complexity, considering the ST specifications and requirements. Furthermore, the classical solution based on the DAB converter is included in the analysis for the sake of comparison. The main goal of this work is to investigate the feasibility of the QAB converter in ST application, with respect to the standard solution (the DAB converter) and verify which configuration offers more advantages to the system. As an additional contribution, Silicon (Si) IGBT and Silicon Carbide (SiC) MOSFETS are used on the QAB design and their performances are compared, in order to investigate the potential of different semiconductor technology in ST application.

The paper is divided as follows: in section II, the theoretical analysis of the QAB converter is presented, where its equivalent model is shown and the main equations are derived. The different configurations of the QAB are analyzed and compared in section III, considering the ST scenario. In this section, the configurations are compared and a discussion, showing the most promising one is presented. Finally, a 20 kW prototype of the QAB converter was built and experimental results are provided in Section IV.

II. OPERATION PRINCIPLE OF THE QAB CONVERTER

The QAB is composed of four active bridges and for the analysis, each of them is denoted by the letters a , b , c and d . The elements of the bridges have sub-index $i = \{a, b, c, d\}$ to indicate the bridge the element belongs to. To analyze the converter, an equivalent circuit based on the Y-model and depicted in Fig. 3 (a) is used, in which the bridges are replaced by rectangular voltage sources (v_a , v_b , v_c and v_d). The voltage at the central point v_x and the current slope of each inductor are given by (1) and (2), respectively, where $k = \{a, b, c, d\}$.

To modulate the converter, the Phase-Shift Modulation (PSM) strategy is employed. Using this modulation scheme, rectangular voltages v_a , v_b , v_c and v_d with phase shift φ_a , φ_b , φ_c and φ_d , respectively, and constant switching frequency f_s are applied to the transformer. The power is controlled by the phase difference among the bridges and it can be generally described in (3), where, $i = a, b, c, d$ and $k = a, b, c, d$,

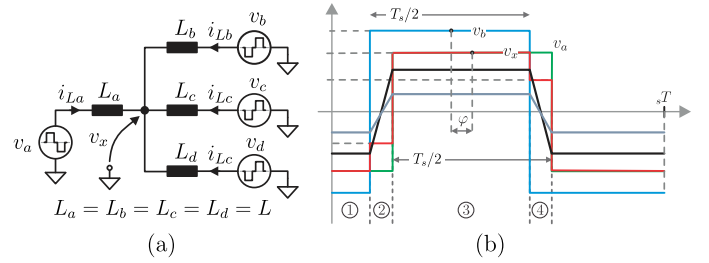


Figure 3. Model of the QAB converter and main waveforms, using the PSM.

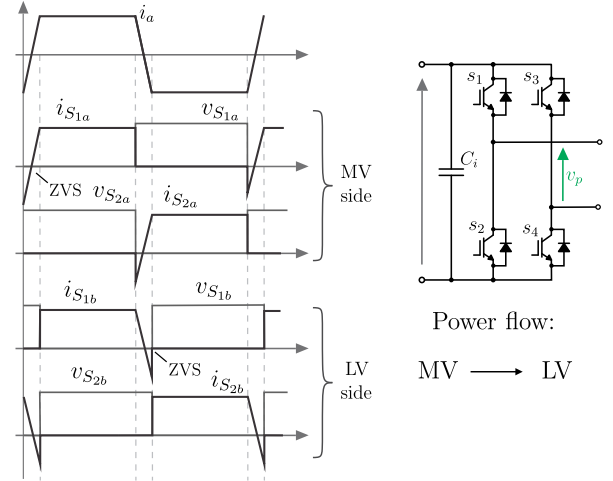


Figure 4. Current and voltage waveforms on the LV side semiconductors (i_{S1a} , v_{S1a} , i_{S2a} , v_{S2a}) and MV semiconductors (i_{S1b} , v_{S1b} , i_{S2b} , v_{S2b}) of the QAB converter.

according to [9], [10]. The main waveform of the PSM is shown in Fig. 3 (b).

$$v_x = \frac{v_a + v_b + v_c + v_d}{4} \quad (1)$$

$$\frac{di_{Lk}}{dt} = \frac{(v_k - v_x)}{L} \quad (2)$$

$$P_{ik} = \frac{V_M V_L}{2\pi f_s L n} \varphi_{ik} \left(1 - \frac{|\varphi_{ik}|}{\pi} \right), \varphi_{ik} = \varphi_i - \varphi_k \quad (3)$$

The PSM is characterized by ZVS turn-on, but this features depends on the input and output voltages relation and also on the load. As the input and output voltage are considered constant, the converter can be properly designed to work with ZVS operation for its entire range of operation. Consequently, this scheme offers several advantages for the converter operation.

Once defined the nominal power and phase-shift angle, the equivalent leakage inductance seen by the LV side is computed by (6). The voltage and current waveforms on the semiconductors of the MV side bridge and LV bridge of the QAB converter are depicted in Fig. 4. If properly designed, the current and voltage waveforms on the semiconductors will be same as depicted in Fig. 4, regardless the configuration of the QAB converter presented in Fig. 2. Based on the currents waveforms depicted in 4, the current stresses (mean and rms) on the semiconductors used to select the proper devices are calculated by (13) to (20).

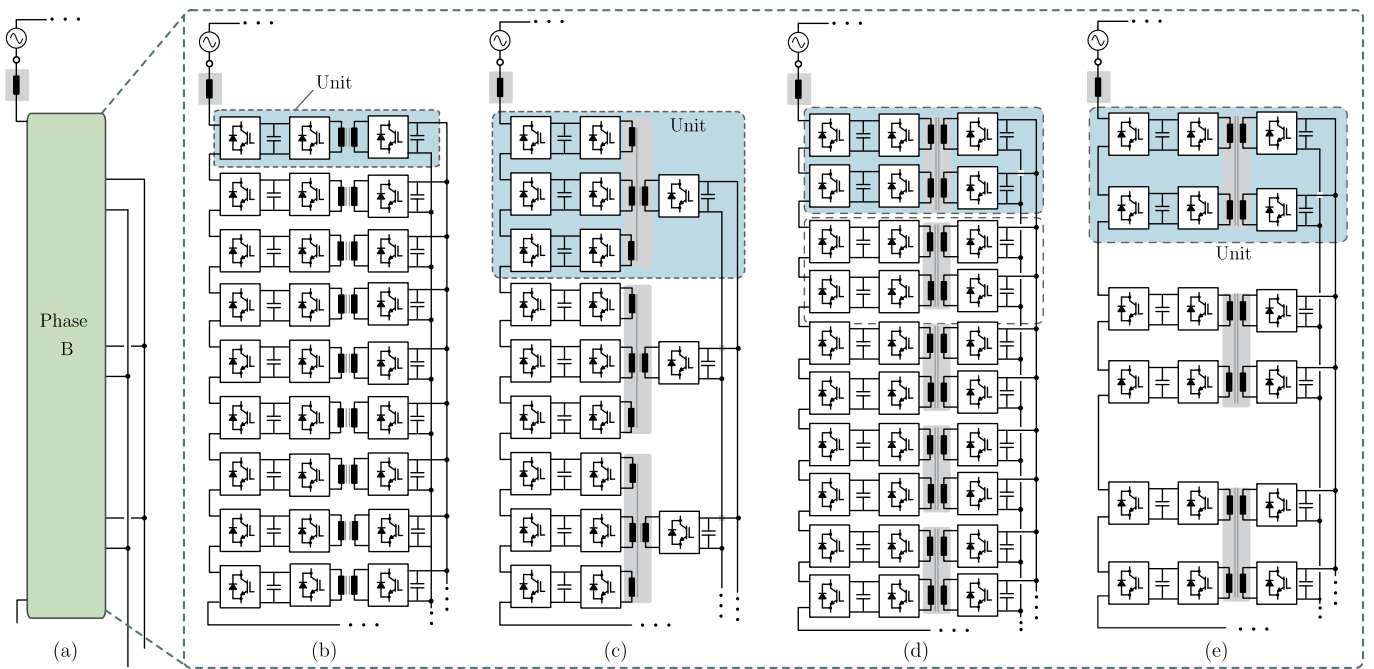


Figure 5. Smart transformer architecture based on different building blocks configuration of the dc-dc converter: (b) DAB: DAB converter as the building block, (c) AQAB: QAB converter in asymmetrical configuration, (d) SQAB-V: QAB converter in symmetrical configuration, preserving the same voltage level of the MV cells of the DAB, (e) SQAB-P: QAB converter in symmetrical configuration, preserving the same power level of the asymmetrical configuration.

Table I
GRID SPECIFICATION

Rated Power	MVAC	LVAC	Grid frequency	LVDC
1 MVA	10 kV	400 V	50 Hz	700 V

III. SYSTEM CONFIGURATION AND DESIGN

The four different architectures considered in this work are shown in Fig. 5. The first one is a modular architecture based on the standard DAB solution (see Fig. 5 (b)), that will be used as a benchmark. The second architecture depicted in Fig. 5 (c) is based on the QAB converter configured asymmetrically and it is named in this work as *AQAB*. The third and fourth cases, shown in Fig. 5 (d) and (e), respectively, are based on the symmetric configuration of the QAB converter. The analysis of the symmetrical configuration was divided in two cases: the first one (Fig. 5 (d)), named as *SQAB-V* uses more units, keeping the same voltage level over the QAB cells (and over the semiconductors) in comparison with the asymmetrical QAB architecture, whereas the second case (Fig. 5 (e)), named as *SQAB-P* uses the same number of units of the asymmetrical QAB architecture, keeping the same power level for each unit.

As can be noticed, all these architectures uses the Cascaded H-Bridge (CHB) topology as a front-end rectifier, because it offers several advantages, as described in [1]. In addition, the CHB cells are considered part of the unit. In the case of a repairable system, the whole unit can be substituted or bypassed. Regarding the number of units selection, 3 units are chosen for the asymmetric QAB architecture, resulting in 9 CHB cells, and then 9 units are used in the DAB architecture to keep the same CHB structure. This number provides a good trade-off between the number of components and the usage of the employed semiconductors (voltage and current rating) [1].

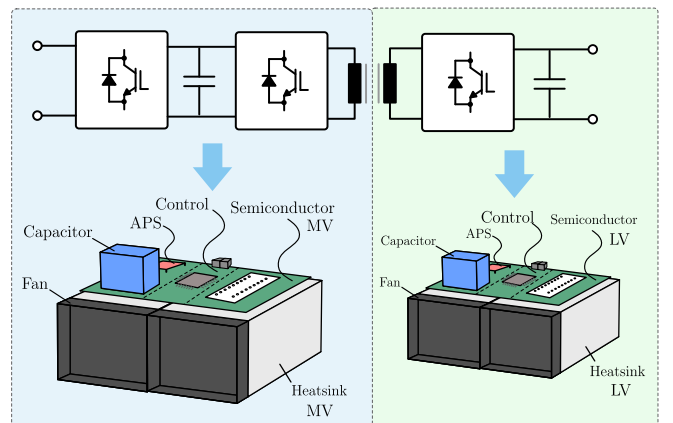


Figure 6. Schematic of the implementation detail of the MV cell and LV cell of the unit.

Table II
QAB SPECIFICATION AND DESIGN CONSIDERATION

Total MVDC link	$V_{MVDC} = 10.2 \text{ kV}$
LVDC link	$V_{LVDC} = 700 \text{ V}$
Switching frequency	$f_s = 20 \text{ kHz}$
Nominal PS angle	$\phi_{nom} = 35^\circ$

A. Design Consideration of the Units

For the comparative analysis, each architecture presented in Fig. 5 must be designed and the losses, efficiency and cost must be calculated.

Regardless the ST architecture, the MV and LV cells used to build the units are composed basically by four parts: semiconductors, capacitors, cooling system and auxiliary components. The semiconductors and capacitors are the responsible for the converter's losses, while the cooling system, semiconductors and capacitors are the major contributors to the converter's

Converter parameters design	Semiconductors stresses	Losses calculation
	MV side	
$P_{unit} = P_{ST}/N_{unit}$ (4)	$i_{D1b(avg)} = \frac{I_{LPK(LV)} \varphi}{3n} \frac{\varphi}{8\pi}$ (13)	$P_{MOS(cond)} = \frac{1}{T} \int_0^T R_{ds(on)}(i_{ds}, T_J, V_{gs}) \cdot i_{ds}^2(t) dt$ (21)
$V_M = V_{MVDC}/N_{cells(CHB)}$ (5)	$i_{D1b(rms)} = \frac{I_{LPK(LV)} \sqrt{\frac{\varphi}{12\pi}}}{3n}$ (14)	$P_{MOS(cond)} = R_{ds(on)} \cdot I_{S1(rms)}^2$ (22)
$L_{eq} = \frac{V_M V_L}{2\pi f_s n P_o} \varphi_{nom} \left(1 - \frac{ \varphi_{nom} }{\pi}\right)$ (6)	$i_{S1b(rms)} = \frac{I_{LPK(LV)} \sqrt{\frac{1}{2} \left(1 - \frac{5\varphi}{12\pi}\right)}}{3n}$ (15)	$P_{IGBT(cond)} = \frac{1}{T} \int_0^T V_f(i_f(t), T_J, V_{gs}) \cdot i_f(t) dt$ (23)
$I_{LPK(LV)} = \frac{V_L - \sqrt{V_L^2 - 8L_{eq}f_s n V_L I_o}}{4L_{eq}f_s}$ (7)	$i_{S1b(avg)} = \frac{I_{LPK(LV)} \left(1 - \frac{3\varphi}{4\pi}\right)}{6n}$ (16)	$P_{IGBT(cond)} = V_f \cdot I_{f(avg)} + R_f \cdot I_{f(rms)}^2$ (24)
$I_{LPK(MV)} = \frac{I_{LPK(LV)}}{k \cdot n}$ (8)	LV side	Switching losses
$i_{L1b(rms)} = \frac{I_{LPK(LV)} \sqrt{1 - \frac{2\varphi}{3\pi}}}{3n}$ (9)	$i_{S1a(rms)} = I_{LPK(LV)} \sqrt{\frac{\varphi}{12\pi}}$ (17)	$P_{(sw)} = \frac{1}{T} \left(\sum_{n=1}^{N_{sw(on)}} E_{on}(V_{ce}, I_d, T_J, V_{gs}, R_g) + \sum_{n=1}^{N_{sw(off)}} E_{off}(V_{ce}, I_d, T_J, V_{gs}, R_g) \right)$ (25)
$i_{L1a(rms)} = I_{LPK(LV)} \sqrt{1 - \frac{2\varphi}{3\pi}}$ (10)	$i_{S1a(avg)} = I_{LPK(LV)} \frac{\varphi}{8\pi}$ (18)	$P_{(sw)} = \frac{1}{T} \left(\sum_{n=1}^{N_{sw(off)}} E_{off}(I_d) \right) = E_{off} \cdot f_s$ (26)
$n = V_M/V_L$ (11)	$i_{D1a(avg)} = \frac{I_{LPK(LV)} \left(1 - \frac{3\varphi}{4\pi}\right)}{2}$ (19)	Capacitor and magnetic losses
$k = \begin{cases} 1, & \text{symmetric config} \\ 3, & \text{asymmetric config} \end{cases}$ (12)	$i_{D1a(rms)} = I_{LPK(LV)} \sqrt{\frac{1}{2} \left(1 - \frac{5\varphi}{12\pi}\right)}$ (20)	$I_{C_o(rms)} = \sqrt{I_{LPK(LV)}^2 \left(1 - \frac{2\varphi}{3\pi}\right) - \left(\frac{V_L}{R_{load}}\right)^2}$ (27)
		$P_{Tr(wire)} = R_{wire} \cdot (I_{Tr(rms)})^2$ (28)
		$P_{core} = \left(\frac{\Delta B}{1}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left \frac{dB}{dt}\right ^\alpha dt$ (29)
		$k_N = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} \cos\theta ^\alpha d\theta}$ (30)

Figure 7. Main equations used for the complete design of the converters.

cost. The auxiliary components in question used on the cells are the gate driver unit (GDU), auxiliary power supply (APS) and control and communication system (CCS). These devices do not contribute to the converter's losses, but they penalize the cost. Therefore, they are taken into account during cost computation. Fig. 6 shows the detail of the implementation scheme of the MV cell and LV cell, considering the four part aforementioned. Note that all units are composed by these cells, regardless the architecture. It means that the DAB architecture has a single MV cell and a single LV cell, while the AQAB converter has four MV cells and only one LV cell per unit. Another component that contributes greatly to the losses and cost of the converter is the HFT and then, it is considered during the design of the converter.

In order to compute the losses and the cost and to find an optimum trade-off between them, a computer-aided based design was used and the flowchart of the developed algorithm is illustrated in Fig. 8. The ST architectures are designed considering the grid specification presented in Table I. The QAB converter is designed using those equations shown in Fig. 7, where the main converter's parameters are calculated by (4) to (12), according to the converter's configuration.

The switching frequency and nominal phase shift angle could have been used as a parameters for the optimization process. However, they are considered constant during the units design, as presented in Table II. The switching frequency selection is crucial during the dc-dc converter design, because the MFT requires high voltage isolation, as determined by

the application [1]. This sets an upper limit to the operating frequency. In fact, since primary and secondary windings must be spatially separated, proximity effect would increase copper losses. Moreover, given a constant probability of partial discharge, a higher switching frequency translates to more partial discharge events, with detrimental effects on the transformer lifetime. For these reasons, 20 kHz was selected. Similarly, a nominal phase shift angle of $\varphi = 35^\circ$ was considered, in order to reduce the reactive power processed by the converter, as explained in [1]. Further design considerations for the QAB converter design are summarized in Table II.

B. Semiconductor Analysis

Considering the voltage and power level of the converter, Silicon IGBT module are often used. On the other hand, the new technology of Silicon-Carbide MOSFETs has emerged as a high performance and economically viable solution. These devices have been used to implement the power converters of the ST architecture in [11], [12]. However, the potential of such semiconductors is still an open question in the power electronic field. For these reasons, both aforementioned semiconductor technologies (Si IGBT and SiC MOSFETs) are taken into account in the design of the power converters, presented in Fig. 8.

For the semiconductor selection, devices from the biggest market players on IGBT modules sector and SiC MOSFETs sector were considered: *Powerex Power Semiconductors/Mitsubishi Electric* and *WolfSpeed/CREE* [13], [14]. Sev-

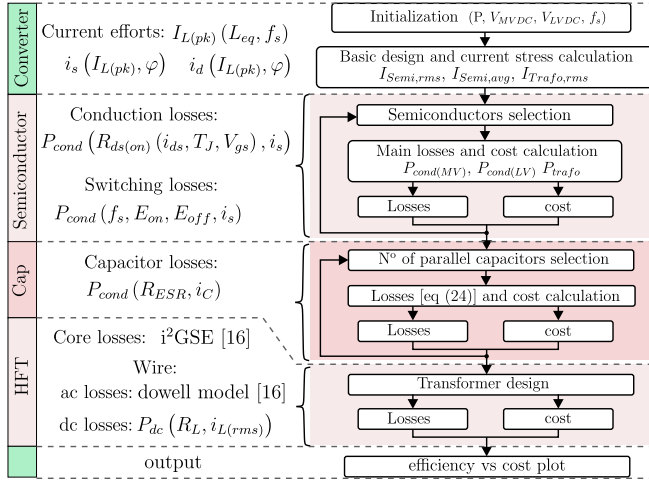


Figure 8. Simplified flowchart of the algorithm used to design the power units of the ST architectures.

eral devices from both manufactures were considered for the converter design and they are listed in Table V of the Appendix A. The semiconductors losses are estimated using the current stresses calculated using equations (13) to (20) and the electric parameters presented in Table V of the Appendix A. The conduction losses of the SiC MOSFETs are calculated by (21), where the on-resistance ($R_{ds(on)}$) is function of the drain-source current (i_{dc}), junction temperature (T_j) and gate voltage (V_{gs}). Assuming a constant junction temperature of 100°C and a constant gate voltage of 15 V, the equation is simplified to (22). Similarly, the losses on the IGBT are calculated by (23), in which can be simplified by (24).

The switching losses can be generally calculated by (25), where $N_{sw(on)}$ and $N_{sw(off)}$ are the number of turn-on and turn-off commutations, respectively, during the time interval T_s . R_g is the gate resistance. As the converter switches always with a constant voltage and it is assumed a constant temperature junction, as well as the V_{gs} and R_g . Because of the ZVS operation, the turn-on losses are neglected, and a simplified equation can be written as presented in (26). Replacing the equations (13) to (20) in (22), (24) and (26), the semiconductors losses (conduction and switching) are obtained for the LV and MV sides.

The cost the devices used on the design were also included on the database of the algorithm, since the total cost of the architecture is an outcome of the design. For the IGBT, the costs were obtained directly with the manufacturer [15], while for the SiC case, the cost were obtained from the distributor (Mouser Electronics). Both costs were considered for 1000 pieces.

C. Capacitor Bank Analysis

Similarly to the semiconductors, the capacitor bank is also one of the most important elements on the converter and then it must be accurately designed. The required capacitance can be calculated as presented in [9], [10], [16]. To select the proper device for implementing the capacitance bank, the metalized electrolytic type capacitors or film type capacitors can be used. The first one, are usually rated for lower voltage (up to 600 V)

with high capacitance, while the second one has normally high voltage rating (over 1 kV), but low capacitance. Although the electrolytic capacitors have higher energy density, its intrinsic resistance is very high, due to its constructive structure. Therefore, to avoid high losses, parallel devices are generally used. The losses are calculated using equation (27). Among the possible options, devices from *EPCOS/TKD* were considered, which is one of the biggest company in this sector. The devices used in the analysis are presented in Table VI of the Appendix A.

Initially, the required capacitance is calculated and each device from Table VI are combined in parallel or series until to reach the required voltage and capacitance. After that, the cost and losses on the total capacitor bank is calculated. The device providing the lowest cost is chosen.

D. Magnetic Components Analysis

An algorithm was implemented to assist the HFT design and calculate its losses. In this algorithm, the basic design is performed according to [17], where the number of turns is calculated, wires are selected and so on. To avoid the skin effect, litz wire is used. Then, only the dc losses on the wires are considered and it is calculated by (28). For the core losses, the generalized Steinmetz equation [18] is used, as presented in (29) and (30).

The cost of the HFT is composed by the cost of the wires and core and they are estimate accurately. As a matter of comparison, a methodology to access the cost of the wire based on the amount ofcopper required is suggested and explain in detail in Appendix B. Concerning the core used, a single specification has been used. The core used is: ferrite core (material N87) from *EPCOS/TKD*, shape UU92/152/60. The cost is obtained also from the distributor (Mouser Electronics) for 100 pieces. During the HFT design, the construction possibility is verified and, in negative case, an additional core is considered in parallel to increase the central leg area (increasing the magnetic flux either).

E. Cooling System Consideration

The cooling system contributed greatly for the ST system cost. A single cooling system is used per cell, where the semiconductors of the CHB and the primary side of the dc-dc converter are attached to it. The air forced cooling system is used for providing an accessible replacement of the modules. The required volume of the heatsink is calculated in order to maintain a maximum junction temperature of the semiconductor of $T_j = 125^\circ\text{C}$, considering an ambient temperature of $T_a = 50^\circ\text{C}$. Following the procedure described in [19]–[22], the total thermal resistance between the junction and the heatsink surface is calculated by

$$R_{HS} = \frac{T_j - T_a}{P_{losses}}, \quad (31)$$

where P_{losses} is the total losses of all semiconductors attached to the heatsink. To define the required volume of the heatsink, the Cooling System Performance Index (CSPI) introduced in [19] can be applied. The CSPI characterizes the

performance of a given cooling system (or heatsink profile) in terms of power dissipation capability per volume, considering a certain temperature difference. In other words, the CSPI can be understood as a volumetric thermal conductivity and it correlates the volume and the thermal resistance of the heatsink, as presented in (32).

$$V_{HS} = \frac{273}{CSPI \cdot R_{HS}} \quad (32)$$

This approach is very useful for cost and performance comparison purpose, because assuming a constant CPSI means that the cooling system performance will be the same for every number of module, and only the heatsink volume changes according to the power dissipated in each case. The cooling system cost is directly proportional to the volume, which will change considering the number of modules. As the cost and volume of the heatsink are correlated proportionally, a cooling cost constant K_{HScost} [USD/dm^3] can be defined as

$$K_{HScost} = \frac{Cost_{HS}}{V_{HS}} \quad (33)$$

Using a constant value of K_{HScost} and CSPI regardless the number of module, the performance will then be constant and only the cost will change according to the number of modules. As reported in [19], [23], for a standard forced air cooling system, the CSPI can be assumed as $CSPI = 10 W / (Kdm^3)$. A suitable heatsink profile that can be used on the power module of the ST is the LA V 22 from *Fischer Elektronik*. The cost of such heatsink profile was obtained directly from the manufacturer *Fischer Elektronik*, resulting in a $K_{HScost} = 0.059 [USD/dm^3]$. Finally, the cooling system is design for each number of modules using equations (31) to (33) and considering the values of CPSI and K_{HScost} presented before.

F. Auxiliary Components

The auxiliary components penalize only the cost of the system, according to the number of modules. Each module has 4 GDU, 1 APS and 1 CCU, which constant price are considered for them, independent of the voltage specification of the semiconductor or dc link. For the GDU and APS, a constant cost of 100 \$ USD is presumed, while 10 \$ USD for the CCU is assumed.

IV. COMPARATIVE EVALUATION

The results from the previously described design are presented in Table III and in Fig. 9. They are divided in two cases, according to the employed semiconductors technology. The first case uses Si-IGBT, whereas the second SiC-MOSFETs, and each case is discussed as follows.

The DAB architecture has more power units, but the power level of each unit is the lowest, compared to the others architectures. Analyzing the parameters of the MV side, the current effort on the semiconductor are the same for all architectures, independently from the voltage and power level. Hence, the current rating of the employed semiconductor is also the same. With respect to the voltage level of the semiconductors, only

the SQAB-P needs to use 3.3 kV devices, while the others require 1.7 kV. Then, DAB, AQAB and SQAB-V use the same devices on the MV side. In spite of the availability of 3.3 kV IGBT on the market, there is no SiC-MOSFET available yet with this voltage rating. According to [13], [14], the 3.3 kV SiC-MOSFET was already developed and it is under test process to be launch on the market in the next years. Previous information for such device were provided in [13], [14], as well as a price estimation. Thus, these information were used in this investigation, to calculate the losses and cost of SQAB-P.

Analyzing the LV side, the AQAB has fewer cells connected in this side, demanding then higher current rating devices. As can be observed in Table III, AQAB requires devices rated for 200 A and such devices are not available for the SiC-MOSFETs considered in this study (see Table V). Thus, two devices C2M0025120D (1.2 kV / 90 A) were used in parallel. Regarding the voltage level, 1.2 kV devices were used for this side in all architectures, because the LV cells are connected in parallel.

A. Losses and Cost Comparison

The cost and efficiency are the most important parameters evaluated in this work and they are compared follows.

From the losses analysis presented in Fig. 9, it can be seen that the AQAB presents the best performance, while SQAB-V the worst, regardless the employed semiconductors. Due to the few number of cells on the LV side, the AQAB architecture requires high current rating device which has usually high performance, i.e. low $R_{ds(on)}$ in case of MOSFETs and low $V_{CE(on)}$ in case of IGBTs. For this reason, the AQAB has presented the best performance. The DAB, used as basis of comparison, has presented the second best performance, but only slightly better compared to the SQAB-P. As an overall analysis, it can be noticed that the losses for all architecture are very similar to each other, when IGBT are used, presenting a difference of around 12% between the best one and the worst one. Note that this design concerns the specifications provided in Table I. Different grid specification might imply different results. Still from these results, the application of SiC MOSFETs has improved the performance in terms of efficiency of the architectures DAB, AQAB and SQAB-P, but deteriorated the efficiency of SQAB-V. Due to the high number of employed modules in this last architecture, the current in the LV side bridges is very reduced, allowing for lower current rating devices, compared to the others. As a result from the design, the SiC MOSFETs C2M0040120D (1200V / 60 A) was selected for the SQAB-V, while the device C2M0025120D (1200V / 90 A) was selected for the others architectures, providing lower on resistance and better performance. Of course, the device C2M0025120D can also be used in SQAB-V, improving its performance, but also increasing its cost.

Regarding the cost analysis, the AQAB has also presented the best results, regardless the semiconductor. However, when SiC-MOSFETs are employed, AQAB and SQAB-V presented similar costs with a small difference of 1%. Only SQAB-P has presented a significant high cost compared to the others,

Table III
COMPARATIVE ANALYSIS OF THE ARCHITECTURES

Basic Information (per Phase)				
	DAB	AQAB	SQAB-V	SQAB-P
Number of Units per Phase	9	3	5	3
Power Level of the Unit	37.04 kW	111.11 kW	66.66 kW	111.11 kW
MVDC link	1.13 kV	1.13 kV	1.02 kV	1.7 kV
Semiconductor Voltage Rating (MV side)	1.7 kV	1.7 kV	1.7 kV	3.3 kV
Total N° of semiconductors (MV side)	36	36	60	36
Total N° of semiconductors (LV Side)	36	12	20	12
Selected Semiconductor				
Si-IGBT (MV side)	CM75DY-34A	CM75DY-34A	CM75DY-34A	QID3310006
Si-IGBT (LV side)	CM75DU-24F	CM200DX-24S	CM75DU-24F	CM75DU-24F
SiC-MOSFET (MV side)	C2M0045170D	C2M0045170D	C2M0045170D	Cree Preliminary 3.3 kV
SiC-MOSFET (LV side)	C2M0040120D	C2M0025120D	C2M0040120D	C2M0025120D
Medium-Frequency Transformer				
N° of HFT	9	3	5	3
Equivalent inductance	27.3 μ	187.96 μH	54.56 μH	34.54 μH
Isolation requirement (Prim. to Prim.)	1.7 kV	1.7 kV	1.7 kV	3.3 kV
Isolation requirement (Prim. to Sec.)	10 kV	10 kV	10 kV	10 kV
Isolation requirement (Sec. to Sec.)	700 V	700 V	700 V	700 V
Auxiliary Components				
Auxiliary Power Supply	18	12	20	12
Gate Driver Unit	36	24	40	24
Control and comm system	36	24	40	24

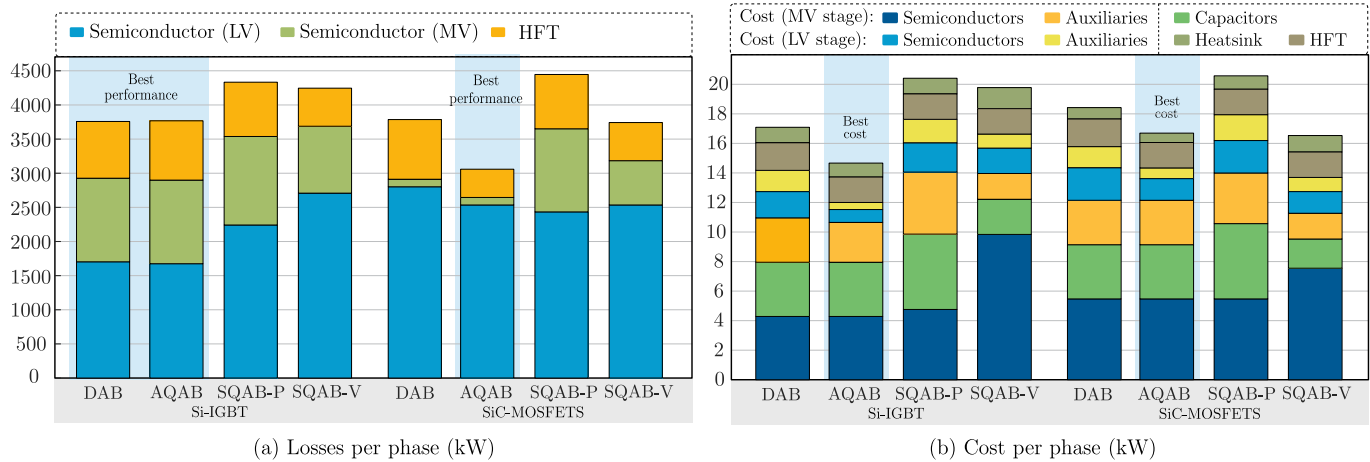


Figure 9. Comparative results for the investigated ST architectures, considering the Si-IGBT and SiC-MOSFETs devices: (a) losses comparison, (b) cost comparison.

because of the price of the high-voltage device required on the MV side of this architecture. Furthermore, the AQAB presents even high economical advantages over the DAB, when SiC-MOSFETs are employed.

B. QAB Configurations

The AQAB that uses the asymmetric configuration of the QAB converter is more advantageous in terms of efficiency and cost. The main reason for that is the reduced number of cells and HFT, compared to SQAB-V, associated to lower voltage rating devices, compared to SQAB-P.

Although higher current rating devices are required to implement the LV cell of the AQAB (see Table III), the individual device cost does not differ much from the cost of the devices required by the others solutions, bringing economic advantages.

As SQAB-P requires semiconductors with voltage rating of 3.3 kV on the MV side, only IGBT can be used. Besides, the price of this device is very high, increasing drastically the

cost of the system. For that reason, SQAB-P is worst option in terms of cost and it is approximately 40% more expensive than the cheapest solution, i.e. the AQAB architecture.

C. Si-IGBT vs. SiC-MOSFETs Comparison

As expected, the performance of all architectures are improved in terms power dissipation, when SiC MOSFETs are used, demonstrating the high performance of such semiconductor technology. On the other hand, its price is still very high, when compared to the classic Si-IGBT solution. Using the results obtained from the AQAB, i.e. the most promising one, the SiC-MOSFETs offer around 10% of losses reduction, but the system cost increases in almost 14%. Then, the energy saving throughout the system operation needs to be economically evaluated according to the application, to verify if the additional installation investment when SiC-MOSFET are used is economically viable.

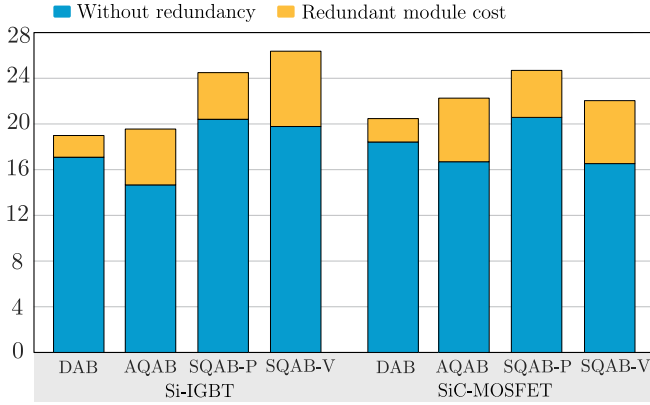


Figure 10. Cost comparison of the different architectures considering the redundant unit for a fault tolerance scheme implementation.

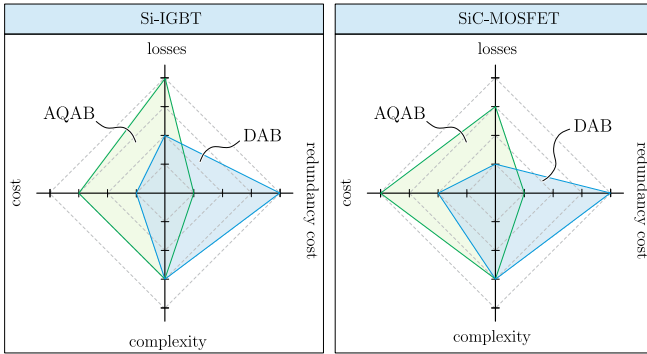


Figure 11. Qualitative comparison of the standard solution based on DAB converter with the proposed QAB solution, considering the most promised configuration (asymmetric configuration): (a) Si-IGBT, (b) SiC-MOSFETs.

D. Further Comparison

In addition to the cost and efficiency, the architectures can be qualitative compared in two more categories:

1) *Redundancy implementation effort*: The fault tolerance scheme is a very important feature for the system, because it increases significantly its availability. This feature is normally obtained by using redundant power units and to implement that, at least one additional power units needs to be used. Depending on the cost of the individual unit and the number of units, the redundancy scheme implementation cost is different for each architecture. Therefore, the cost of redundancy implementation for each architecture is analyzed and compared herein. To do so, it is assumed that the minimum number of additional units is used, i.e. only one extra unit in each architecture. Fig. 10 shows the cost of the different architectures without redundancy and also the cost of the redundant unit. As can be noticed, the cost of the extra unit of the DAB is lowest one, regardless the semiconductor technology used, because of its simplicity. Nevertheless, considering the total cost of the system including the redundant unit, the AQAB and DAB architectures have similar costs, when Si-IGBT is adopting, with a difference of only 2% in favor of the DAB. When SiC-MOSFETs are used, the DAB architecture presents lower cost. From this comparison, it is important to note that the DAB has advantages for the redundancy scheme implementation because the price of the individual unit is lower.

2) *Design Complexity*: The design complexity is very difficult to quantify, then a qualitative discussion is presented. Discussion regarding the QAB design indicates that the architectures based on this converter is more complex than the DAB-based architecture from the control and power stages aspects. The QAB converter requires an additional control loop to equalize the power of the bridges, then the control effort implementation is slightly higher, when compared to the DAB. From the power stage viewpoint, the complexity of the QAB lays on the multiwinding transformer design, compared to the classical two winding used on the DAB converter. In this aspect, the DAB is more advantageous than the QAB based architectures. Nevertheless, the QAB adversities have been discussed in [8], [9].

E. QAB vs. DAB

To evaluate the potential of the QAB converter in ST application, the best configuration (AQAB) is individually compared to the standard solution based on DAB and the results are depicted in Fig. 11.

Due to the fewer number of components (Cells and HFT), the QAB solution is more economically advantageous, as presented in Fig. 9 (b). Adopting this solution instead of DAB and considering the specification of the Table I, the system cost can be reduced by 14.8%, when Si-IGBT are employed.

Regarding the efficiency, the QAB solution presented similar performance to the DAB, although the first one performs slightly better. As the QAB operates similarly to the DAB converter, when processing balanced power, then similar power dissipation is also expected. Of course, semiconductor with different electric characteristic are used in the LV cells for both cases, and also the quantity of semiconductors, resulting in different power dissipation between the solutions.

Then, QAB converter is presented as an economically viable solution and its potential in ST application has been demonstrated from the results obtained in this work.

V. EXPERIMENTAL VALIDATION

In order to demonstrate the effectiveness of the theoretical analysis and design methodology presented and validate the comparative results obtained theoretically, a scaled-down prototype has been developed and tested in laboratory. The main goal of this section is to validate experimentally the design methodology presented in this paper. Once confirmed the efficacy of the design technique, the theoretical results obtained and compared are automatically certified, since they were obtained with such design methodology.

As the asymmetric configuration of the QAB was presented as the most advantageous one from the theoretical studies, it was chosen to be implemented and experimentally investigated. The schematic of the unit is illustrated in Fig. 12.

Therefore, using the specification shown in Table IV and the design algorithm illustrated in Fig. 8, the prototype of an unit of the AQAB architecture (as indicated in Fig. 12) has been designed. As observed in Table IV, the output power is 20 kW, while the input and output are 800 V and 700 V, respectively. The same nominal phase-shift angle and

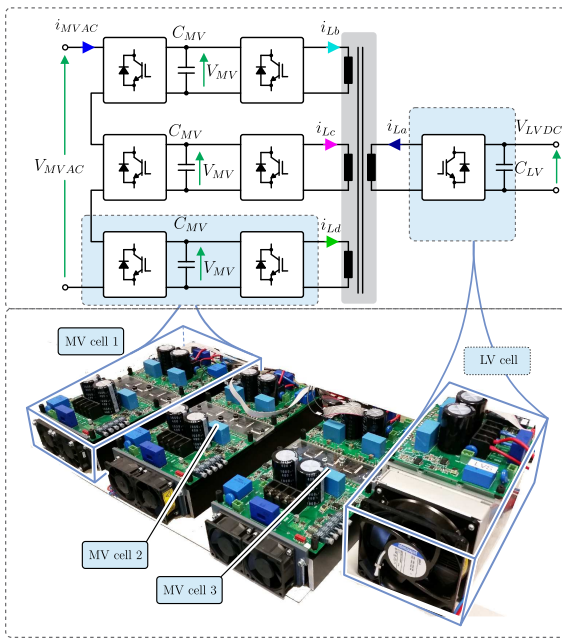


Figure 12. The schematic of the AQAB configuration unit used for the experimental verification and the picture of the implemented prototype based on this scheme.

switching frequency were used either in the real scale design (presented in Section III) and scaled-down design, in order to maintain the consistence of the design methodology. Hence, a switching frequency of 20 kHz and a nominal phase shift angle of 35° were adopted.

As an outcome of the design algorithm, the total losses and cost were computed and they are presented Fig. 13. Note that two different designs were selected, the first one based on Si-IGBT devices and the second one based on SiC-MOSFETs. As the losses on the individual components are computed in the design methodology, the losses distribution for both design cases are also depicted in Fig. 13. As can be noticed, power dissipation of 1080 W is expected on the converter when Si-IGBTs are used, while losses of 422.35 W are expected when SiC-MOSFETs are adopted. It means that the converter should provide an efficiency of 94.8%, when Si-IGBT are employed, and 97.8% when SiC-MOSFETs are used. This suggests a considerable improvement on the efficiency, when SiC-MOSFETs is adopted instead Si-IGBTs. Nevertheless, in this case, the cost of the converter increases in around 70%.

Based on the design, the prototype of the QAB converter was built, tested and its performance was evaluated considering both semiconductors types: Si-IGBT and SiC-MOSFETs. The adopted IGBTs were the IHW40N120R3

Table IV
SPECIFICATION OF THE PROTOTYPE

Nominal Power of the Unit	$P_o = 20 \text{ kW}$
Nominal AC voltage	$V_{ac} = 1.4 \text{ kVrms} / 50 \text{ Hz}$
Individual MVDC link	$V_{MV} = 800 \text{ V}$
LVDC link	$V_{LVDC} = 700 \text{ V}$
Switching frequency	$f_s = 20 \text{ kHz}$

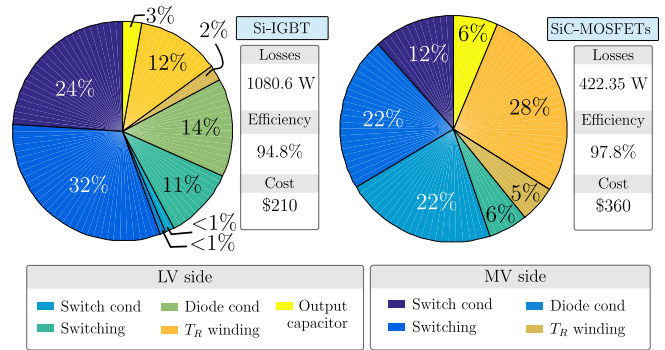


Figure 13. Outcomes of the AQAB design, including the theoretical losses, efficiency, cost, as well as the losses distribution on each component.

from *Infineon Technology*. The adopted SiC-MOSFETs were the C2M0025120D (1200 V / 25 m Ω) for MV side and C2M0040120D (1200 V / 40 m Ω) for MV side, both from *CREE*. Fig. 12 shows the picture of the implement prototype. In this picture, the cells of the CHB associated to the QAB converter is observed, sharing the same cooling system.

For the previous demonstration, the experiments are run with an input voltage of 230 V/50 Hz (available grid voltage) and a power level of 2 kW and the results are depicted in Fig. 14 (a). However, to demonstrate the operation and potential of the QAB converter, it was tested individually with power level of 10 kW, as presented in Fig. 14 (b) and (c).

In Fig. 14 (a), the main waveforms of the front-end MV stage are presented, where the input voltage before and after the ac filter (V_{MVAC}) and the input current (i_{MVAC}) are observed. From this results, a high power factor operation of the system is observed. Fig. 14 (b) shows the main waveforms of the dc-dc stage, where the currents on the LV cell (i_{La}) and MV cells (i_{Lb} , i_{Lc} , i_{Ld}) are presented. From these results, the balanced operation of the QAB converter is noticed, where each MV cell process the same amount of power. Furthermore, soft-switching operation is also observed from the current waveforms. Similarly, Fig. 14 (c) shows voltage and current on the ac side of the MV bridge (v_{Lb} and i_{Lb}) and also on the LV bridge (v_{La} and i_{La}), where the phase-shift operation of these bridges is observed. Note that these waveforms were obtained for the prototype operating with SiC-MOSFETs on the dc-dc converter.

Finally, the efficiency of the QAB converter was measured experimentally using the high performance power analyzer WT1800 from Yokogawa (basic power accuracy of 0.02%). When Si-IGBTs were adopted, the converter has achieved as efficiency of 94.28%. However, due to the equipment accuracy, this value can vary from 94.5% to 94.05%. The difference between the efficiency obtained experimentally and the estimated one is only 0.5%. When SiC-MOSFETs are used, on the other hand, the converter provides an efficiency of 97.5%, which is only 0.3% lower than the expected efficiency. Furthermore, considering the accuracy of the power analyzer, the measured value can vary from 97.3% to 97.8%. These results demonstrate the validity of the design methodology presented in this paper, as well as the capability of the QAB converter to provide high performance.

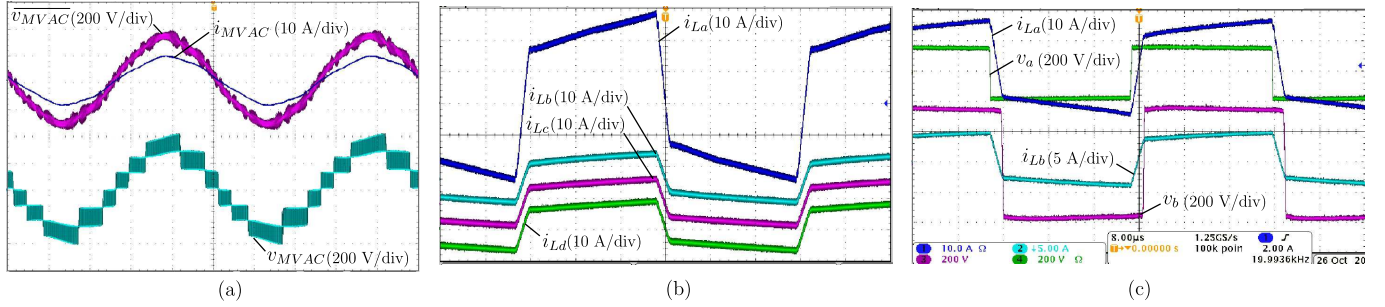


Figure 14. Experimental results of the implemented ST prototype: (a) main waveforms of the MV stage, (b) inductor current waveforms on the LV side (i_{La}) and MV side (i_{Lb} , i_{Lc} and i_{Ld}) of the QAB converter, (c) main voltage and current waveforms on the LV side (v_{La} , i_{La}) and MV side of the QAB (v_{Lb} , i_{Lb}) converter.

VI. CONCLUSION

The potential of the quadruple active bridge converter dc as a building block of a modular smart transformer is evaluated in this work. Four different architectures of ST are presented and compared in terms of cost, efficiency, reliability and implementation complexity. The architectures are: DAB-based architecture, Asymmetrical QAB (AQAB), Symmetrical QAB in voltage (SQAB-V) and Symmetrical QAB in power (SQAB-P). As an additional contribution of this work, different semiconductors technology (Si-IGBT and SiC-MOSFETs) are evaluate, in order to verify their impact on ST application.

The AQAB architecture presented the best performance in terms of efficiency and cost. Compared to the classic DAB solution, the AQAB offers a cost reduction of 14.8%. The efficiency of both solution are very similar, only a slightly improvement of 5% is obtained in the AQAB.

Regarding the potential of SiC-MOSFETs in ST application, this devices offers a losses reduction of around 10%, but is increase the system cost in around 14%. Therefore, to verify the economic feasibility of such devices in this application, a study considering the energy saving over time and the installation cost should to be realized.

Finally, a 20 kW prototype of the ST based on the AQAB architecture was developed and tested, providing an efficiency of around 97.5%. Then, this paper has demonstrated the high potential of the QAB converter as building block of the ST.

APPENDIX A

Power semiconductors from *Powerex Power Semiconductors/Mitsubishi Electric* and *Wolfspeed/CREE* considered in the converter's design presented in Section III.

APPENDIX B - PRICE ESTIMATION OF THE MAGNETIC COMPONENTS

To simplify the analysis and make it employable to different power converters, the basic idea is to obtain an equation that correlates the copper volume required to implement the winding with the rms current that flows on this coil. Using the i_{rms} values through the transformer and a desired current density J , the necessary wire area A_w is

$$A_w = \frac{i_{rms}}{J} \quad (4)$$

Table V

SPECIFICATION OF THE SEMICONDUCTORS CONSIDERED IN THE DESIGN

Si-IGBT Power Modules				
Reference	V	I	$V_{CE(on)}$	$r_{(on)}(25\text{ C})$
CM50DU-24F	1.2 kV	50 A	1.25 V	10.71m Ω
CM75DU-24F		75 A	1.2 V	8m Ω
CM100DY-24A		100 A	1.2 V	5m Ω
CM150DX-24S		150 A	1.2 V	3.5m Ω
CM200DX-24S		200 A	1 V	3.3m Ω
CM300DX-24S1		300 A	1 V	3.1m Ω
CM75DY-34A	1.7 kV	200 A	1.2 V	18m Ω
QID331006	3.3 kV	100 A	1 V	32m Ω
QIC6508001	6.5 kV	50 A	2 V	40m Ω
SiC MOSFETs				
Reference	V	I	$V_{(Diode)}$	$R_{ds(on)}$
C2M0040120D	1.2 kV	60 A	3.1V	40m Ω
C2M0025120D		90 A	3.1V	25m Ω
C2M0045170D	1.7 kV	72 A	3.6V	45m Ω
Cree Preliminary 3.3 kV	3.3 kV	45 A	3.1V	40m Ω

Table VI

CAPACITORS CONSIDERED FOR THE ANALYSIS OF THE OPTIMUM NUMBER OF MODULES

Electrolytic				
PN	V	Cap (μF)	Cost (\$USD)	$R_{SE}(m\Omega)$
B43520B5108M000	0.45	1000	26.13	15
Film				
B32778J1127K000	1.3	120	69.26	15
B25620B1227K321	1.32	220	50.99	15
B25620B1706K981	1.98	70	45.06	15
B25620B1297K983	1.98	295	109.81	15

According to [17], the number of turns for a winding is

$$N = \frac{V_{winding}}{4A_c f_s \Delta B}, \quad (5)$$

where, $V_{winding}$ is the voltage on the winding, A_c is the section are of the selected core. Consequently, the required volume of copper is computed (6), where l_{mlp} is the mean length of one turn.

$$v_{cu} = A_{wire}(Nl_{mlp}) \quad (6)$$

Replacing (4) and (5) in (6) the follow relation is obtained

$$v_{cu} = \frac{V_{winding}}{4A_c f_s \Delta B} \frac{I_{rms}}{J} l_{mlp}. \quad (7)$$

Table VII
CONSIDERED PARAMETERS FOR THE MFT DESIGN

Current density	$J = 3 \text{ A/mm}^2$
Copper density	$d_{cu} = 8.96 \cdot 10^{-3} \text{ g/mm}^3$
Copper Cost	$C_{cu} = 2.96 \cdot 10^{-3} \text{ U\$/g}$
Switching frequency	$f_s = 20 \text{ kHz}$
Mean turn length of wire	$l_{mlp} = 96 \text{ mm}$
Flux density variation	$\Delta B = 0.3$

As the design parameters f_s , ΔB and J are constant and assuming a constant core size, then equation (7) can be rewritten as

$$v_{cu} = k_1 V_{winding} I_{rms}, \quad (8)$$

$$k_1 = \frac{V_{winding} I_{rms}}{4A_c f_s \Delta B J} l_{mlp} \quad (9)$$

The weight of copper used is determined using the volume and the copper density $d_{cu} = 8.96 \text{ g/cm}^3$

$$W_{cu} = v_{cu} d_{cu} \quad (10)$$

Then, replacing (8) in (10), the total amount of copper required is given by (11). Note that the required copper is proportional to the power processed by the winding.

$$W_{cu} = k_1 d_{cu} (V_{winding} I_{rms}) \quad (11)$$

Finally, the cost required to implement the winding is calculated using the copper cost per kg obtained from [24] and also the weight, as defined in (12). From this equation, it is demonstrated that the copper price used to is proportional to the power processed by the winding ($P_{winding}$). Considering the same constant dc voltage imposed on the winding, then the cost became directly proportional to the rms current flowing in the winding.

$$C_{cu} = W_{cu} P_{cu}, \quad (12)$$

$$C_{cu} \propto P_{winding} \propto I_{rms}. \quad (13)$$

Then, using (13) and assuming the parameters presented in Table VII, the cost of the MFT transformer is obtained for each architecture considered in this work.

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