On field-effect transistor concepts beyond traditional application

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Henning Winterfeld

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1. Gutachter: Prof. Dr. Hermann Kohlstedt

2. Gutachter: Prof. Dr. Franz Faupel

Prüfungsvorsitz: Prof. Dr. Lorenz Kienle

Prüfer: Prof. Dr. Rainer Adelung

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Abstract

The metal-oxide-semiconductor field-effect transistor (MOSFET) has been the basis of state-of-the-art electronics for the last decades. Their introduction into integrated circuits (ICs) has opened the door to the immense increase in computational power we have experienced. However, the versatility and potential of MOSFETs far exceeds the mere use as an electric switch in integrated circuits. This thesis presents two novel devices, which are both based on the MOSFET concept, to create approaches to areas beyond conventional computing. Adding a floating gate and applying the specialised MemFlash wiring scheme transforms simple MOSFETs into memristive devices, promising candidates for the application as artificial synapses. Such novel devices are needed to emulate the functionalities of fundamental building block in the brain, in order to implement novel computing systems based on neuronal functionalities. Moreover, MOSFETs have been the basis of numerous sensors, such as Bio- and ChemFETs. In this work, a MOSFET based stress sensing device is presented, called the piezoelectric field-effect transistor.

Utilising MOSFET based memory cells as memristive devices allows the integration of novel approaches to computing into existing fabrication technologies, since it combines neuromorphic engineering with modern silicon technology. However, present memory devices like EEPROM cells experience high power consumption. The same is seen for memristive devices based on the MemFlash concept. In this work, a way to not only reduce power consumption but at the same time adjust the learning behaviour of the memristive MemFlash devices by tuning of the tunnelling oxide thickness is shown.

Furthermore, a novel MOSFET based stress sensor is presented in this work. A piezoelectric layer in the gate stack of the device allowed the transistor to react to externally applied stress. The combination of the highly integrable and CMOS compatible silicon technology of MOSFETs and the piezoelectric effect of low temperature AlN has great potential for application in many fields, such as stress and tactile sensing, accelerometers and even magnetic field sensing. For this novel sensor device fabrication and characterisation procedures were developed, allowing the application of a determined stress across the

piezoelectric field-effect transistor. The usage of different piezoelectric materials allowed CMOS compatible devices with different sensitivities to be created. A touch sensor based on the piezoelectric field-effect transistor concept demonstrates a possible application of this novel device.

Kurzzusammenfassung

Der Metall-Oxid-Halbleiter Feldeffekttransistor (MOSFET) bildet die Basis der modernen elektrischen Geräte der letzten Jahrzehnte. Der imense Anstieg der Leistung von Computern wäre ohne die Inkoorperation von MOSFETs in integrierte Schaltkreise (ICs) nicht möglich gewesen. Ihr Potential geht jedoch weit über den Nutzen in ICs hinaus. In dieser Arbeit werden zwei Bauteile präsentiert, deren grundlegendes Konzept auf einem MOSFET-Ansatz basiert und die Anwendungsmöglichkeiten in Bereichen jenseits der konventionellen Computertechnologie bieten. Durch das Hinzufügen eines elektrisch isolierten Gates und die Anwendung einer speziellen MemFlash Verschaltung lässt sich ein simpler MOSFET als ein memristives Bauteil betreiben. Memristive Bauteile haben das Potential als künstliche Synapsen eingesetzt zu werden und können somit als Grundbaustein für neuartige, neuronal inspirierte Computersysteme dienen. Darüber hinaus werden MOSFETs seit längerem als Basis für verschiedenste Sensoren, wie z.B. Bio- und ChemFETs, verwendet. In dieser Arbeit wird der piezoelektrische Feldeffekttransistor präsentiert; ein Sensor für mechanische Verspannungen auf Basis eines MOSFETs.

Die Nutzung von Speicherzellen auf MOSFET-Basis als memristive Bauteile, ermöglicht die Integration neuer Ansätze der Computerarchitektur in die bereits etablierten Fertigungstechniken der Siliziumtechnologie. Die modernen Speicherzellen haben jedoch einen hohen Energieverbrauch. Memristive Bauteile auf Basis dieser Speicherzellen haben das gleiche Problem. In dieser Arbeit wird ein Ansatz präsentiert, der es erlaubt, den Energieverbrauch dieser memristiven Bauteile zu senken und gleichzeitig ihre Lerneigenschaften zu justieren.

Des Weiteren wird in dieser Arbeit ein neuartiger Sensor für mechanische Verspannungen vorgestellt. Eine piezoelektrische Schicht in der Gate-Struktur ermöglicht es dem Transistor auf Verspannungen zu reagieren. Die Kombination von hoch integrierbarer und CMOS-kompatibler Siliziumtechnologie mit den piezoelektrischen Eigenschaften von AlN bietet großes Potential für verschiedenste Anwendungsbereiche, wie Verspannungs-, Kraft-, Beschleunigungs- und Magnetfeldmessungen. Für diesen neuartigen Sensor

wurden Fertigungs- und Charakterisierungsverfahren entwickelt, welche es erlauben, Verspannungen über dem Transistor anzulegen und zu bestimmen. Die Verwendung verschiedener piezoelektrischer Materialien erlaubten die Herstellung von Bauteilen mit verschiedenen Sensitivitäten. Weiterhin konnte ein Berührungssensor auf Basis des piezoeletrischen Feldeffekttransistors entwickelt werden, der eine mögliche Anwendung des Bauteils demonstriert.

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1 Introduction

Modern computer technology would not have been possible without the invention of the field-effect transistor (FET). As the name suggests, electric fields affect and thus control the current flow through these devices. The metal-oxide-semiconductor field-effect transistor (MOSFET) is one type of FET, utilising the isolating properties of an oxide between the gate and the semiconductor. Its use as an electronic switch in integrated circuits (ICs) revolutionized circuit design [1], [2]. Following the invention of the field-effect transistor and its incorporation into integrated circuits, their size has been reduced steadily. The possibility of fitting millions of devices onto a single chip opened the door for the modern electronic devices we know today. This is a trend commonly known as Moore's Law [3], [4]. Recently node size technology reached the mark of 5 nm [5]. The MOSFET has been used for many years as an electric switch in circuit design. However, the principle of a semiconductor being affected by the application of an electric field to allow charge carrier transport was adapted in a number of devices [6], [7]. Such MOSFET based devices include sensors and memory (see Fig. 1.1 (a)).

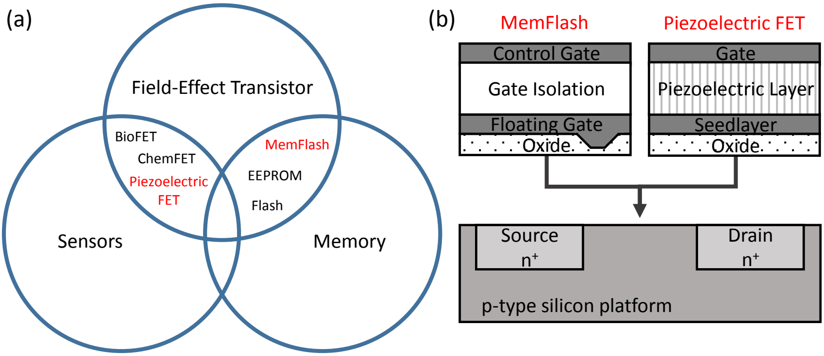


Figure 1.1 (a) Venn diagram showing the usage of field-effect transistors in sensor and memory applications, with devices introduced and investigated in this work highlighted in red. (b) Gate stacks of the two created devices, the MemFlash and the piezoelectric field-effect transistor, with the semiconductor base.

Building on the described versatility of the field-effect transistor, two different devices, the MemFlash cell and the piezoelectric field-effect transistor, have been fabricated and investigated in this work. Both devices are based upon the MOSFET principle and use a floating gate approach (see Fig. 1.1 (b)).

With the introduction of an electrically isolated floating gate into the gate stack of the MOSFET a memory device can be created. The amount of charge on the floating gate determines the electrical conductivity of the channel within the semiconductor. Furthermore, due to the encapsulation, said charges stay on the floating gate unless they are deliberately removed. Using this principle of a floating gate within the gate stack of a MOSFET, it was possible to create a number of memory devices, such as electrically programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM) and Flash cells [6], [8], [9].

The first device investigated in this work is the MemFlash cell. With the limitations of the commonly used von Neumann computer architecture becoming more apparent, neuromorphic computing is believed to provide a way to tackle the issues of increasing power consumption and low transmission speeds between memory and processor [10]–[12]. The architecture of the human brain follows a more interconnected approach, incorporating processing and storage. Additionally, complex problems are solved using the high degree of parallel data processing of the human brain [13]. One key building block of neuronal networks used in neuromorphic computing are resistors that are able to gradually change their resistance based on the previously seen charge, so-called memristive devices. Since memristive devices are still in the early stages of research, a number of different structural and functional concepts have been presented [14]. The MemFlash approach is a way to use state-of-the-art silicon memory cells as memristive devices [15]. It is therefore offering the possibility of combining complementary metal-oxide-semiconductor (CMOS) compatibility and well known silicon technology, with novel approaches to computing. Furthermore, the MemFlash cell uses electron movement as a working principle, whereas many other memristive devices are based on ion movement [14], [16]. However, with the adaptation of a standard EEPROM memory cell, the high power consumption is still an issue [17].

With the approach presented in this work, a way to not only reduce power consumption but at the same time adjust the learning behaviour of the memristive MemFlash devices by tuning of the tunnelling oxide thickness is shown [18], [19]. In order to achieve this, MemFlash devices were fabricated, optimised and characterised. The optimization of the electrical isolation of the floating gate as a means to attain the retention times needed for valid device performance comparison was investigated thoroughly. Furthermore, the underlying MOSFET and the charging mechanism of the floating gate will be described. This includes the need for the creation of a customized recoding and analysis software.

In addition to memory devices, MOSFETs have been at the heart of numerous sensors. Examples of such sensors using a field-effect transistor as their base are the ChemFET and the BioFET [7], [20], [21]. In ChemFETs the conductivity of the channel in the semiconductor of the field-effect transistor is influenced by the chemical solution placed on top of the gate oxide. The channel current is pinned at a certain value by constant gate and drain voltages, with the solution leading to the forming of an electrical surface charge. Determined by the charge layer which forms in the solution at the gate oxide interface, the concentration of a solution can be determined quantitatively [21]. Furthermore, beyond the determination of chemical concentrations, other sensing approaches comprising field-effect transistors exist and are used for the determination of different parameters.

In this work a force sensor based on a piezoelectric field-effect transistor is presented. When thinking about the application of force or tactile sensors, the field of robotics naturally comes to the mind of an engineer. Tasks which are simple for a human, like picking up an egg without breaking it, may challenge a robot. Without feedback of how much pressure is applied to an object, a robot can only perform pre-defined routines with well-known objects. In this case, a human acts as the sensor and defines the action. If a robot was able to evaluate its grasp on a fragile object, it could learn to perform a task for a number of different objects without external adjustment in the program controlling it. However, despite the high rate of innovation in robotics in the last decades, tactile and force sensing as well as the corresponding sensors have not shown improvement at the same rate [22], [23]. Imitating the haptic feedback from the sensing embedded in the human skin is crucial for improving prosthetics and to the same degree improving the grasp control in robots [24]. Most tactile and force sensors are based on either strain-gauge, capacitance, optical or piezoelectric effects [23], [25]. A commonly used layout for piezoelectric sensors is a sandwich structure where the applied force is transferred into an output voltage [26]. Such a setup usually involves an amplifier near the sensor to strengthen the signal and improve the signal-to-noise ratio.

In the sensor developed in this thesis, the piezoelectric sensing material is positioned in the gate stack of a MOSFET and therefore as closely to an amplifier as possible [27], [28]. This piezoelectric field-effect transistor will be used in combination with a cantilever structure to detect applied forces. In addition to an investigation of the basic functionality of the sensor, frequency and sensitivity analyses were performed. Furthermore, the possibility of increasing device performance through introduction of different piezoelectric materials into the gate stack was evaluated. In order to investigate this behaviour, measurement setups and protocols were designed and implemented. In a final step, the application of the created piezoelectric field-effect transistor in a neuronal inspired force sensor setup will be shown.

The following chapter describes the theoretical fundamentals of the MOSFET, MemFlash and piezoelectric field-effect transistor concepts. The working principles within the devices are highlighted and explained. Chapter three shows the processes used for the fabrication of the devices and gives a short overview of all fabricated sample types. In chapter four the measurement setups created for the characterisation of the samples are explained. The results of the measurements obtained with said setups are presented and discussed in chapter five. The final chapter summarizes the achievements of this work.

2 Theory

This chapter presents the basics needed for full comprehension of the fabricated devices and the corresponding characterisation. Firstly, the underlying building block of all devices fabricated in this work, the MOSFET, is discussed. Secondly, floating gate devices and their electrical behaviour are explained. Following this, the fundamentals of neuromorphic computing and the corresponding devices are examined. Finally the piezoelectric field-effect transistor and its theoretical basis are presented.

2.1 MOSFET

The Metal-Oxide-Semiconductor Field-Effect Transistor has often been named as one of the, if not the most important invention for integrated circuits [2], [29], [30]. Without the invention of the MOSFET, there would not be the large amount of computer products we are used to today. The basic principle of the field-effect transistor was proposed by Lilienfeld [31] and Heil [32] in the 1930s, studied intensively during the following decades [33], [34] until the first working MOSFET was reported by Kahng and Atalla in 1960 [35]. The device history, physics and applications have at length been discussed in literature [29], [30], [36].

In modern CMOS (complementary MOS) fabrication, n-channel and p-channel MOSFETs are formed next to each other on the same chip. CMOS circuits replaced pMOS and nMOS, because CMOS circuits are more efficient and need virtually no power when on standby [30]. In this work, n-channel MOSFETs are used as a base for all fabricated devices. Therefore, the focus is placed on the working principles and formulas of n-channel field-effect transistors. However, the principles and equations are the same for p-channel devices, providing the change of sign.

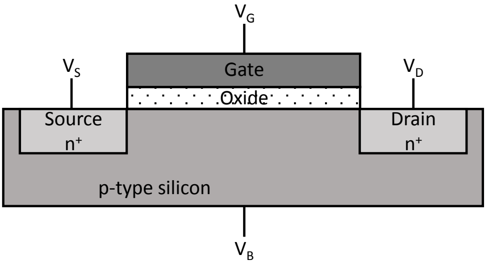


Figure 2.1 Schematic cross-sectional view of an ordinary Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).

The schematic of a typical n-channel MOSFET is shown in Fig. 2.1. The transistor is built into a p-type doped silicon wafer and has three connections: source, drain and gate. The additional connection to the substrate is called the bulk connection. The n-doped source well is the origin of electrons for the current flow to the drain. This flow will take place through an n-channel formed in the p-type substrate underneath the gate oxide. This oxide isolates the metal gate from the substrate. Applying a sufficient voltage to the gate (V_G) and a second potential difference between source and drain (V_{DS}) allows a current flow from source to drain.

It can be differentiated between two different basic modes of operation. For the first, the source and substrate potentials are set to ground ($V_S = V_B = 0$ V) and constant voltages are applied at the gate and drain. Due to the gate potential, a channel forms in the semiconductor at the oxide layer interface. Therefore, a current can flow from source to drain, aided by the potential difference. For the second operation mode, the source and substrate potentials are again set to ground and a constant voltage is applied to the drain. In contrast to the previous operation mode no voltage is applied at the gate ($V_G = 0$ V). Therefore, no channel forms underneath the oxide and, consequently, no current flows between source and drain. The differentiation between these two modes of operation is important, as the MOSFET in its simplest form is used as a switch. The first mode can therefore be described as a MOSFET in the "ON" state and the second as "OFF". From this short introduction into the basic functions of a

MOSFET one can see that the metal-oxide-semiconductor (MOS) stack is of great importance.

2.1.1 Metal-Insulator-Semiconductor Structure

The MOS structure used in this work will be described in the following paragraph. MOS structures can be categorized as a special form of metal-insulator-semiconductor (MIS) structures. In an ordinary capacitor an insulating material separates two metal electrodes. As the name suggests, in a MOS capacitor one electrode is made from a semiconductor. This substitution leads to a change in behaviour of the capacitor. Unlike in a metal-insulator-metal (MIM) capacitor, a MOS capacitor's behaviour can be split into three parts. These parts are dependent on the voltage applied to the capacitor.

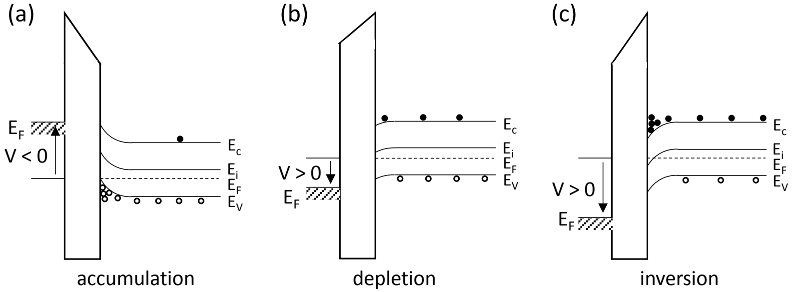


Figure 2.2 Band diagrams of metal-insulator-semiconductor structures, showing the band bending for the application of different voltages. Here, shown for p-type semiconductors. Three different types of behaviour for these structures (a) accumulation, b) depletion and c) inversion) can be defined and the corresponding band structures are displayed (adapted from [29]).

Accumulation:

Applying a negative voltage to a MOS capacitor with a p-type semiconductor leads to an upwards bending of the energy levels near the oxide boundary (c.f. Fig. 2.2). This band bending in the semiconductor near the oxide interface indicates a surface charge [37]. This surface charge is a direct reaction to the negative voltage applied at the metal, with a reversed polarization. The accumulation of majority carriers in the semiconductor leads to a positive charge at the oxide interface. This layer is called the accumulation layer. In this voltage regime, the MOS capacitor behaves like an ordinary parallel-plate MIM capacitor. From this the thickness of an isolation layer of a MOS structure can be determined. The capacitance is calculated as follows [29]:

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d_{ox}} \equiv C_{ox} \tag{2.1}$$

Here ε_0 is the permittivity of vacuum ($\varepsilon_0 = 8.85 \times 10^{-12}$ C/Vm), ε_r is the permittivity of the insulator, A is the area of the capacitor and d_{ox} is the thickness of the insulator. Additionally, in this case the capacitance is equal to C_{ox}, the gate oxide capacitance.

Depletion:

If a small positive voltage is applied at the metal, majority carriers in the semiconductor are repelled into the bulk. A negative charge is created in the semiconductor near the oxide interface. This negative charge counterbalances the doping of the substrate. Therefore, the two charges cancel each other out and no large surface charge can be determined. Since the band bending is an indicator of said charge, it is less dominant and pointed in a downwards direction, compared to the accumulation state. The depletion region extends into the semiconductor and has the characteristics of a dielectric layer. The capacitance of the MOS structure at this point is therefore a serial connection of the insulator capacitor C_{ox} and the depletion layer capacitor C_D [29]:

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_D}} \tag{2.2}$$

where

$$C_D = \frac{\varepsilon_s}{x_d} \tag{2.3}$$

with ε_s being the permittivity of the semiconductor and x_d the depth of the depletion charge. This behaviour is indicated in Fig. 2.3 by the equal spacing between the illustrated negative charges in the conduction band. Keeping the influence of the depletion depth in mind, the equation for the capacitance can be written as:

$$C = \frac{C_{ox}}{\sqrt{1 + \frac{2 \cdot C_{ox}^2 \cdot V_G}{q \cdot N_a \cdot \varepsilon_s}}} \tag{2.4}$$

with V_G being the voltage applied to the gate, q the charge and N_a the p-type doping concentration [30].

Inversion:

Increasing the positive voltage applied at the gate results in a decrease in holes at the oxide boundary and consequentially, an increase in electrons. In the band diagram, it leads to a further downwards bending of the energy levels (see Fig. 2.2). The condition, where the surface electron concentration is equal to the bulk doping concentration is called the threshold. From this point forward, the semiconductor near the surface is in inversion. At the threshold condition the surface potential is

$$\Phi_s = 2\Phi_F = 2\frac{kT}{q} ln \frac{N_a}{n_i} \tag{2.5}$$

where ϕ_F is the electric potential at the Fermi energy, k is the Boltzmann constant, T is the temperature and n_i is the electron concentration. For $\phi_s \geq 2\phi_F$ the semiconductor surface is in strong inversion, beforehand, when the condition $\phi_F \leq \phi_s < 2\phi_F$ is met, the surface is in weak inversion [30].

Most commonly MOSFETs are operated in a state of strong inversion. However, for this research the state of weak inversion, more precisely the subthreshold region, is used to operate the piezoelectric field-effect transistor (see chapter 2.4).

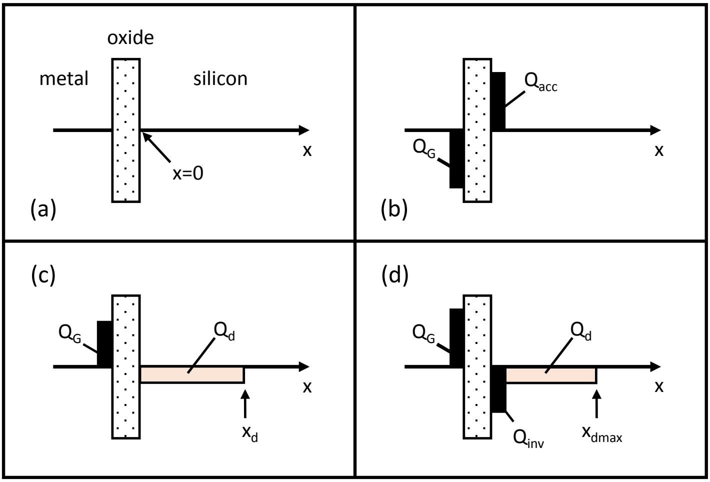


Figure 2.3 Charge distribution within a metal-oxide-semiconductor structure for the different conditions that can be achieved due to the applied bias. Conditions: (a) flat band, (b) accumulation, (c) depletion and (d) inversion. (adapted from [30])

The charges at the different states of the MOS capacitor are shown in Fig. 2.3. Additionally to accumulation (see Fig. 2.3 (b)), depletion (see Fig. 2.3 (c)) and inversion (see Fig. 2.3 (d)), Fig. 2.3 (a) shows the flat band condition. As the name suggests, in this case the energy bands are flat (not bend in any way). For a fictional metal with the same Fermi level as silicon, the flat band condition is reached when no external potentials are applied. The dependency of the charges that accumulate within the semiconductor on the voltage applied to the metal can also be displayed when looking at the space-charge density as a function of the surface potential (see Fig. 2.4 (a)).

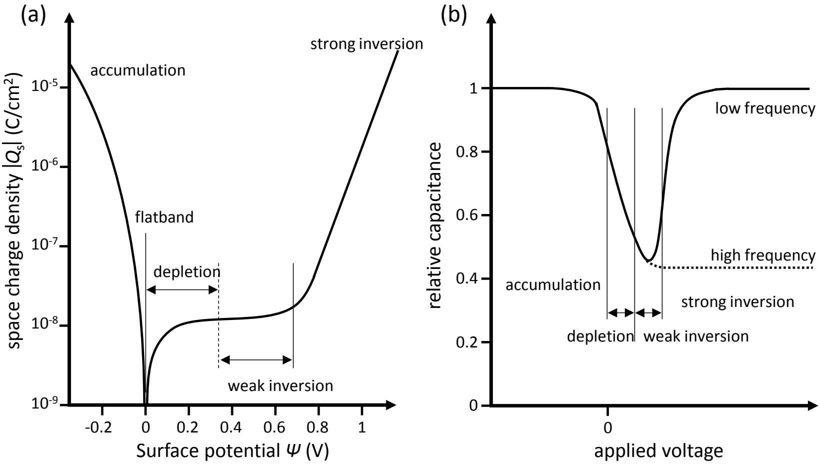


Figure 2.4 Variation of the space charge density in a metal-oxide-semiconductor structure and the corresponding capacitance voltage characteristic. (a) The modulus of the space charge density is displayed against surface potential in a metal-insulator-semiconductor structure. (b) The capacitance-voltage characteristics of an ideal metal-insulator-semiconductor structure for low and high frequencies. (adapted from [29], [30])

Consequently, the charge-voltage curve of a MOS capacitor is influenced by the potential dependent behaviour of the semiconductor electrode (see Fig. 2.4 (b)). For the semiconductor in accumulation and strong inversion, the capacitor reaches maximum capacity. Depletion, more specifically the depletion layer, results in a reduction of the capacity due to the former mentioned series connection of the insulator capacitor and the depletion layer capacitor. Moreover, a second effect on the CV-curve can be seen. The MOS capacitor in the inversion state is highly dependent on the measurement frequency. At a low frequency, electrons are directed towards the oxide boundary and form the inversion layer. The here mentioned electrons are generated inside the semiconductor through thermal generation. Increasing the measurement frequency results in a lower capacity, because thermal generation cannot create electrons fast enough to follow the frequency. Increasing the frequency further will result in a decrease of capacity down to the minimum. At this point, the electrons cannot follow the frequency with the depletion layer fully influencing the overall capacity.

In essence, the MOS capacitor is the base for the MOS field-effect transistor and the charge concentration in the semiconductor can be controlled by the application of different gate voltages, as described. Said gate voltage variations are used throughout this work to operate the devices at the optimal regimes.

2.1.2 MOSFET Operation

The basic modes of MOSFET operation have already been addressed. Here the MOSFET acts as a purely electrical switch. Additionally, the former mentioned “ON” state can be characterised more clearly. Particularly two characteristic curves are used to describe the transistor’s behaviour. Keeping the gate voltage constant and sweeping the drain voltage (V_D) results in the so-called “output curve”. In contrast, a constant drain voltage with a varied gate voltage leads to the “transfer curve”. For both measurements the source and bulk are grounded and the transfer curve is measured at a drain voltage where the MOSFET channel current is in saturation.

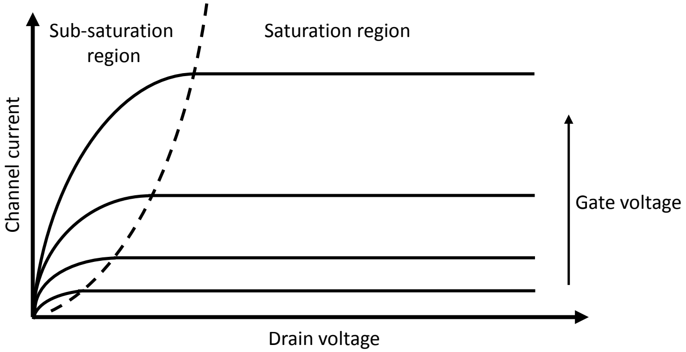


Figure 2.5 Output characteristics of an ideal MOSFET. The dotted line represents the pinch-off point at which V_{GS} - V_{Th} = V_{DS}.

The output characteristics of a MOSFET show the channel current for different levels of V_D at increasing gate voltages. Increasing the drain voltage leads to a (mostly) linear increase in channel current. From a certain point forward, increasing V_D no longer leads to a rise in channel current. These two variations in behaviour are shown in Fig. 2.5 and the dotted line separates the areas of occurrence. The region on the left side of the dotted line is called the "sub-saturation region", whereas the other is named "saturation region". For the sub-saturation region, the channel underneath the oxide is formed due to the applied V_G. Increasing V_D leads to a potential difference between the source (V_S = 0 V) and the drain. With this potential difference and the inversion layer in the semiconductor, electrons are free to move from the source to the drain (see Fig. 2.6 (a)).

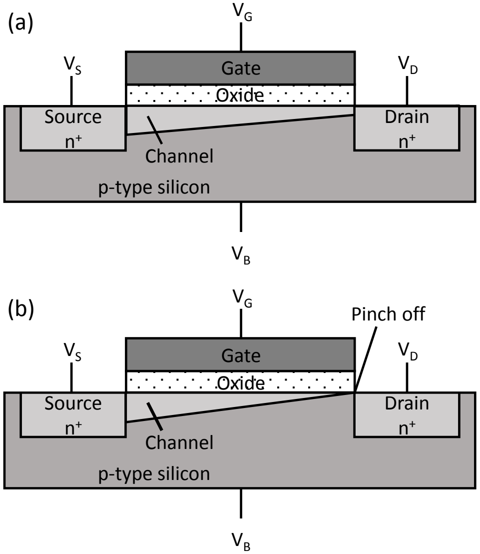


Figure 2.6 (a) Cross-sectional view of the formed channel in a MOSFET when driven in the sub-saturation regime. (b) Cross-sectional view of the channel behaviour at the "pinch off" point, where $V_D = V_G - V_{Th}$. Beyond this point, further increase of the drain voltage results in further reduction of the channel near the drain and a constant channel current.

Hence, the channel current is dependent on the gate voltage, the threshold voltage (V_{Th}) and the drain voltage, as shown in [38]:

$$I_D = \frac{W}{L} \mu_n C_{ox} \left(V_G - V_{Th} - \frac{V_D}{2}\right) V_D \tag{2.6}$$

where W is the channel width, L is the channel length, μ_n is the mobility of electrons. One of the most significant parameters is the threshold voltage, which is defined as:

$$V_{Th} = V_{FB} + 2\Phi_F \frac{\sqrt{2\varepsilon_s q N_A (2\Phi_F)}}{C_{ox}} \tag{2.7}$$

For the sub-saturation voltage regime, the channel current is directly influenced by the drain voltage. This explains why an increase in V_D leads to a higher channel current. However, at the point where the drain potential is equal to V_{Dsat} ($V_{Dsat} = V_G - V_{Th}$), the channel current saturates. The dotted line in Fig. 2.5 indicates this point, which is commonly known as the “pinch off”. Particularly, the name refers to the channel narrowing at the drain-channel boundary up to disappearing completely, therefore, being pinched off (see Fig. 2.6 (b)). Provided that the drain voltage is increased further, the pinch off point is moved along the channel towards that source region. In the output characteristic, this does not result in a decrease or discontinuation of the channel current. It rather leads to the former mentioned saturation current (I_{Dsat}), given by [38]:

$$I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} (V_G - V_{Th})^2. \tag{2.8}$$

Despite the lack of a conductive channel near the drain region, the potential difference between drain and source (V_{DS}) generates a sufficiently strong electric field for electrons to drift from the channel to the drain. In comparison to the sub-saturation region, the saturation current is no longer dependent upon the drain voltage. Hence, an increase in V_D results in a constant channel current.

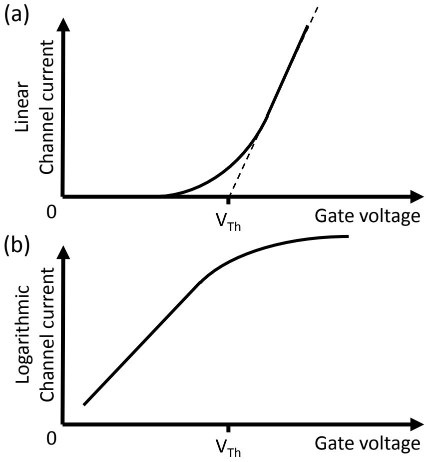


Figure 2.7 Comparison between the linear and logarithmic display of MOSFET transfer curves. (a) Transfer characteristic of an ideal MOSFET in linear representation. (b) Transfer characteristic of an ideal MOSFET in logarithmic representation. Since the subthreshold regime is used for the operation of the piezoelectric field-effect transistors, this logarithmic representation of the transfer curve is shown since it highlights the current increase in this region.

Similarly, the transfer curve reveals additional information about the transistor's behaviour. The threshold voltage can be derived from the transfer curve. To do so, the drain voltage is kept constant and the gate voltage is swept. The outcome of this measurement can be seen in Fig. 2.7 (a). The linear representation of the transfer curve suggests that in the subthreshold region the channel current is zero. Nevertheless, if the current is depicted on a logarithmic scale (as in Fig. 2.7 (b)) a steep increase in current is visible for this voltage regime. The so-called "subthreshold swing" (S_t) is defined as ΔV_G/decade I_D. Research shows an increase of 60 mV/dec as a minimum value for MOSFETs [39]. A lot of research effort is directed towards finding ways of lowering this value even further [39]–[43]. In this work, the piezoelectric field-effect transistor (see chapter 2.4 and 5.3) takes advantage of the relationship between a small change in voltage and a large change in current.

2.1.3 Bulk Potential

Up to this point, the substrate was assumed to be at the same potential as the source ($V_B = V_S = 0$ V) and thus, effectively grounded. However, for this work it is important to address the case of a bulk potential other than 0 V. Applying a negative voltage at the bulk connection leads to holes being pulled into the substrate, thus leaving negatively charged ions in the channel region. This increase in ions results in a lack of mobile electrons, which can contribute to the channel current. Consequently, this increases the gate voltage needed to form a channel. This effect is reflected in the threshold voltage [29]:

$$V_{Th} = V_{FB} + 2\Phi_F \frac{\sqrt{2\varepsilon_S q N_A (2\Phi_F - V_B)}}{C_{ox}} \tag{2.9}$$

For the previously discussed transistor characterisation, no bulk potential was needed because only positive drain voltages were applied. However, when negative drain voltages are used, a greater negative bulk potential ($V_B < V_D$) is needed. As shown in Fig. 2.8 the p-doped substrate and the n-doped source and drain regions form two pn-diodes. These diodes are forward biased when the bulk potential is more positive than the drain (or source) potential ($V_B > V_D$). To prevent a current flow from substrate to drain, the maximum negative potential has to be applied at the bulk for all measurements. Due to its operation scheme, the MemFlash configuration (see chapter 2.3.2) of an EEPROM cell (see chapter 2.2.2) requires a negative bulk potential.

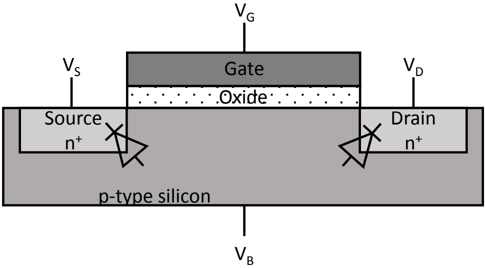


Figure 2.8 Cross-sectional view of a MOSFET, highlighting the diode structures within the device.

2.2 Floating Gate Devices

The literature distinguishes between two major classes of semiconductor memory devices: random access memory (RAM), which is a volatile type of information storage, and read-only memory (ROM), which is non-volatile [8], [29]. The first floating gate device for storage applications was proposed in 1967 [44]. Floating gate devices generally have a MOSFET base with two gates. The top gate is addressable from the outside and called the control gate (CG). The second gate is located between the channel and the control gate and is electrically floating, thus called the floating gate. A schematic view of a floating gate device is shown in Fig. 2.9 (a).

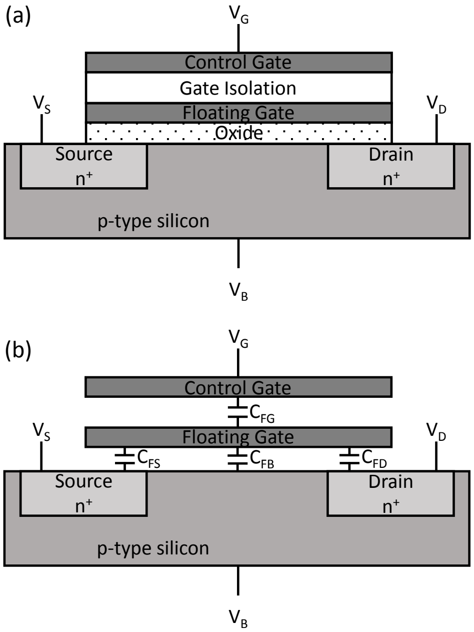


Figure 2.9 (a) Schematic cross-sectional view of a floating gate transistor. (b) The capacitive structures within a floating gate transistor highlighted in the cross-sectional view of an ideal device.

The first floating gate device that could be electrically programmed was the electrically programmable read-only memory (EPROM) [45]. As the name suggests, it can only be electrically programmed using hot-electron injection, but cannot be electrically erased. Instead UV light is used to erase an EPROM device. Even though each cell in an EPROM array may be programmed individually, the erasing procedure affects all cells equally. Evidently, the erasing procedure for EPROM devices using UV light is rather complex and has obvious drawbacks. The electrically erasable programmable read-only memory (EEPROM) solves many issues of the EPROM architecture. In an EEPROM device, programming and erasing can be done by electrical signals. The first EEPROM cell relying solely on Fowler-Nordheim tunnelling for programming and erasing was introduced in 1978 [46].

2.2.1 Fowler-Nordheim tunnelling

Fowler-Nordheim (FN) tunnelling is the main mechanism for programming and erasing in MOS memory devices [29], [47], [48]. The theory behind this concept states that electrons are able to tunnel through an insulator if an electric field is applied, provided that the insulator is thin enough for the given electric field strength. Tunnelling processes through different insulators have been studied extensively.

Applying the concepts of classical physics, an electron approaching a potential barrier will be reflected unless it has enough energy to clear said barrier. However, taking quantum mechanics into account, the possibility of an electron appearing behind the barrier is greater than zero [49]. This is generally explained by considering the electrons wave function, which enables the electron to tunnel through the potential barrier. Applying an electric field leads to a deformation of the potential barrier as can be seen in Fig. 2.10.

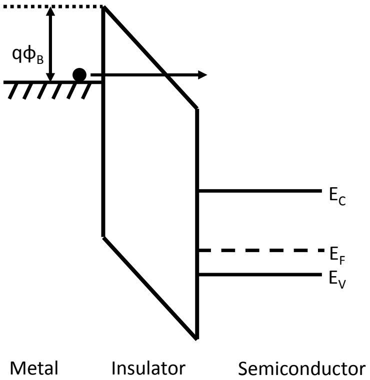


Figure 2.10 Energy-band diagram showing Fowler-Nordheim tunnelling in a metal-insulator-semiconductor structure.

At a certain field strength, the triangular shape of the potential barrier results in a smaller distance the electron has to tunnel trough. As the applied electric field leads to a barrier deformation at the material interface, FN tunnelling is classified as an "electrode-limited conduction mechanism". Generally, Fowler-Nordheim tunnelling is said to be the main conduction mechanism for 4 – 5 nm barrier thickness and above. In contrast, direct tunnelling accounts for the conduction in thinner barriers. The FN tunnelling current density is given by

$$J_{FN} = \pm \frac{q^3 E^2}{8\pi h q \Phi_B} exp\left[\frac{-8\pi(2qm_T^*)^{1/2}}{3hE} \Phi_B^{3/2}\right] \tag{2.10}$$

with J_{FN} being the current density, q the electronic charge, E the electric field applied across the dielectric, h being Planck's constant, $q\varphi_B$ the conduction band offset and m_T^* being the tunnelling effective mass in the dielectric [49], [50]. To eliminate thermal influences on electron conduction, the Fowler-Nordheim tunnelling current is ideally measured at low temperatures of 77 K or less.

2.2.2 FLOTOX EEPROM

In this work, different configurations of floating gate devices with a range of functionalities were fabricated. With respect to information storage, namely memory devices, the EEPROM cells are comparable to modern floating gate tunnelling oxide (FLOTOX) transistors (see Fig. 2.11). These devices allow programming and erasing by Fowler-Nordheim tunnelling through a thinned oxide tunnelling window above the drain region [51]. Therefore, charging and discharging the floating gate can be achieved by applying negative or positive potentials between the control gate and the drain.

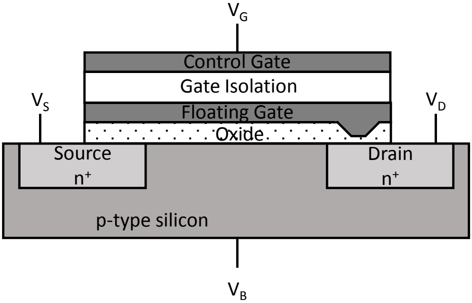


Figure 2.11 Schematic cross-sectional view of an ideal FLOTOX EEPROM cell. The reduced oxide thickness above the drain region distinguishes it from other EEPROM cell designs.

Introducing the floating gate into the regular MOSFET configuration changes the performance of the device. The behaviour changes, as if an additional capacitor has been added. This capacitor consists of the floating and control gate with the gate isolation as a dielectric. The charge on the floating gate is responsible for the development of a channel in the semiconductor. It affects the threshold voltage of the device by a factor of C_T/C_{FG}, where C_T is the total capacitance, with $C_T = C_{FG} + C_{FD} + C_{FS} + C_B$. C_{FG} is the capacitance between the floating gate and the control gate, C_{FD} is the capacitance between the floating gate and the drain region, C_{FS} is the capacitance between the floating gate and the source region and C_{FB} is the capacitance between the floating gate and the substrate (see Fig. 2.9 (b)). Compared to regular MOSFET performance, the presence of a floating gate results in a changed saturation current behaviour:

$$I_{Dsat} = \frac{W}{2L} \mu C_{ox} \left(\frac{C_{FG}}{C_T} (V_{CG} + \frac{C_{FD}}{C_{FG}} V_{DS} \right) - V_{Th})^2 \qquad (2.11)$$

In this case, V_{CG} is the voltage applied at the control gate and V_{DS} is the voltage applied between drain and source [30]. However, comparing the saturation current equation of the MOSFET and the EEPROM device shows that for the floating gate transistor there is still a dependency on the drain-source voltage.

Therefore, even though it is at this point referred to as a saturation current, the channel current does in fact not reach a maximum at $V_D = V_{Dsat}$ [6]. The result is an increase of the channel current even in the saturation region. This can most clearly be seen when comparing the characteristic output curves of an EEPROM cell, which are shown in Fig. 2.12, with those of an ideal MOSFET (see Fig. 2.5).

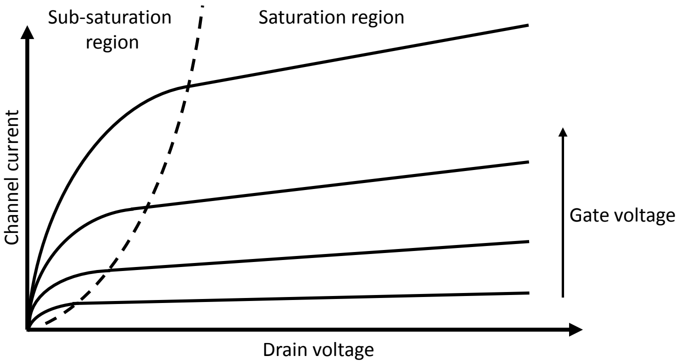


Figure 2.12 Output characteristics of a floating gate transistor. In comparison to a field-effect transistor without a floating gate, the current in the "saturation region" is dependent upon the applied drain voltage and therefore not constant beyond the pinch-off point.

The quality and the thickness of the oxide inside it the tunnelling windows are of great importance for the functionality of FLOTOX EEPROM devices. Depending on the thickness of the oxide, a larger electric field and therefore, more power is needed for charging and discharging the memory cell. Moreover, state-of-the-art memory devices are required to store information for a long time. The time it takes for the charge on the floating gate to reduce to 50 % of its original value is called the retention time [29]. For state-of-the-art memory devices a retention time of at least more than ten years is required [8]. Thus, a reduction of the tunnelling oxide thickness is a trade-off between power consumption and retention time.

2.3 Neuromorphic Engineering

For centuries, humankind has made use of phenomena observed in nature. The focusing via lenses in a camera is derived from the functionality of eyes and Velcro was invented by adaptation of the burdock plant seeds. Perhaps the most famous adaptation of nature is the development of human flight. Nowadays, in the twenty-first century, computers are an integral part of everyday life. As stated before, for the past decades the number of components on computer chips and the corresponding computing power has increased. This was achieved by a continuous decrease in feature size. However, with feature sizes reaching 5 nm and less, new ways have to be found to stay on this course, because physical limitations prohibit simple downscaling [52]. One approach to tackle performance and power consumption challenges in the future is neuromorphic engineering. The concept was first presented in 1990 by Carver Mead [53]. He showed that it was possible to mimic the behaviour of a part of the neuron, the so-called axon hillock [54]. Nowadays, various approaches to hardware implementation of neuron behaviour can be found in literature [55]. Furthermore, not only single devices mimicking selective behaviour are being developed, but large scale networks based upon neuromorphic architectures are being implemented, because they are highly connected and parallel and offer the possibility of combining processing and memory [56]. This approach could revolutionize the established von Neumann architecture used in computers. Even John von Neumann himself saw a possible link between brains and computers [57]. Computer architecture is based upon the separation of computation and storage, which leaves the connection between these two regions as the performance bottleneck of any system [58]. Accordingly, increasing the processing performance of a computer merely somewhat increases its overall performance. Moreover, traditional computer processors excel at calculations and logic operations. However, when it comes to e.g. image and voice recognition the human brain outshines them. Especially when taking the power consumption into account [59], [60]. Therefore, one approach to future computer architecture could be brain-inspired systems, where the memory is located within the processing unit. One example of such an implementation is IBM’s TrueNorth chip [61]. Unsurprisingly, increasing man’s understanding of the brain is another vital requirement in this research area. Up to this point, we do not have an absolute understanding of the brain and all its internal workings. However, research has revealed a lot of the brains secrets [62]–[64] and efforts are directed at understanding it even better. Especially in the age of big data, computer simulations and hardware implementations have the capability of improving our understanding of the brain and in return help reinvent the computer.

2.3.1 Memristive Devices

To attain the goal of a re-envisioned computer setup based upon the workings of mammalian brains, first the basic building blocks have to be identified. In state-of-the-art computer chips, transistors are the main components. However, since the architecture of computer chips and mammalian brains are not comparable, no equivalent for single devices can be defined. In the brain, the cells responsible for the transfer of information are the neurons. They consist of the soma, the nucleus, dendrites, the axon hillock and the axon. The soma is the neurons cell body and contains the nucleus, which stores the genetic information. Information is received by the neuron via its dendrites. The axon hillock evaluates the received information and, if sufficient, initiates a signal to other neurons along the axon. The signals sent between neurons are called action potentials. At the ends of the axon the action potential reaches the synapse, which connects the axon to a dendrite of a following neuron (the post-neuron) [62].

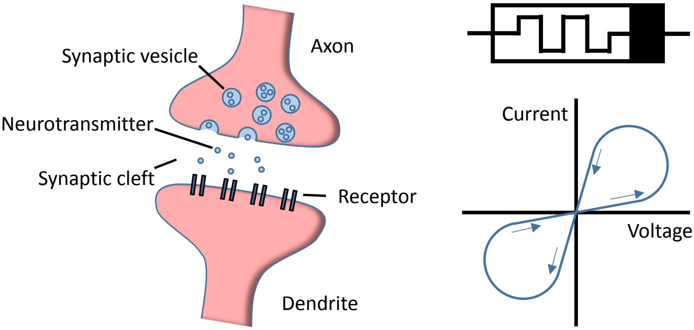


Figure 2.13 Illustration of a synapse found in the human brain (left) and its artificial equivalent, the so-called memristor (right). Underneath the wiring symbol of the memristors, the characteristic current-voltage behaviour of such devices is shown.

It is widely assumed, that the synapses in the brain play a vital role in information storage and therefore in human memory [65]. However, the exact mechanism with which humans store information is still intensely investigated [66]–[68]. Nevertheless, following the assumption that synapses are essential for information storage, researchers have invested great efforts into finding devices that mimic their behaviour [69]. The illustration in Fig. 2.13 shows a synapse and its artificial counterpart, a memristor. The memristor (memory + resistor) has the potential to meet the demands of such devices. It was first proposed by Leon Chua in 1971 [70]. The main characteristic of these two-terminal devices is the pinched-hysteresis I-V loop [71]. This current answer to a periodic voltage signal shows the analogue change in resistance which most closely compares to synaptic plasticity [72].The resistance of a memristive device is therefore dependent upon its charge history. Additionally, in contrast to other fields of application, memory devices for neuronal computing need to fulfil specific criteria [73]. A number of memristive devices have been developed over the years [74], [75]. In the following, the focus will not lie on differences, advantages and disadvantages of different types of memristive devices in general, but on one particular device: the MemFlash cell.

2.3.2 MemFlash

The MemFlash cell is an EEPROM device used in a diode configuration. Standard EEPROM cells are four-terminal devices. However, the diode configuration of the MemFlash operation turns them into (quasi) two-terminal memristive devices.

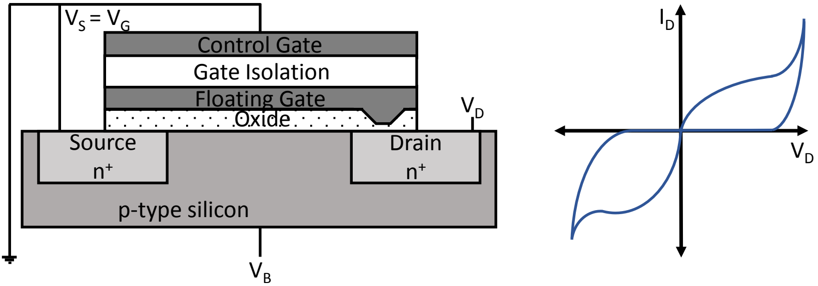


Figure 2.14 A FLOTOX EEPROM cell, as used in this work, wired in the MemFlash configuration, creating a (quasi) two-terminal memristive device. The corresponding device behaviour, the characteristic pinched current-voltage curve, is illustrated next to the schematic view of the device.

Fig. 2.14 shows a schematic cross-sectional view of an EEPROM cell in a MemFlash configuration. Here, the source and control gate are kept at ground potential (in this configuration: $V_S = V_G = 0$ V). Furthermore, the bulk connection is used to keep the substrate at the lowest potential to avoid a short within the device. This leaves the drain connection to control the device. Applying an increasing positive voltage at the drain will, at a certain point, result in an electric field strong enough to move electrons from the floating gate into the drain. Therefore, the floating gate becomes positively charged and an increase in current flow from source to drain is observed. The positive charge on the floating gate is not lost, once the voltage is lowered again (or completely switched off) and the *I*-*V* curve, therefore, follows an altered trajectory. The channel current decreases with decreasing drain voltage until both values are zero. The application of an increasing negative drain voltage results in a negative current flow. Again, at a certain voltage level, the potential difference between the drain region and the floating gate allows electrons to tunnel onto the floating gate. As a result, the floating gate becomes negatively charged and prohibits further current flow through the channel. Accordingly, the *I-V* curve of the MemFlash devices, once more, follows an altered trajectory when the negative drain voltage is reduced. The resulting pinched hysteretic *I-V* curve of an EEPROM cell in a MemFlash configuration is shown in Fig. 2.14.

Memristive devices usually are two-terminal devices. The MemFlash wiring configuration requires the bulk connection to be used as a third terminal as described above. For a single cell this makes any Memflash device a three-terminal memristive device. However, taking the scaling possibility of the device into account, with a growing number of MemFlash devices n in a network, the number of terminals would add up to $2n + 1$. This is due to the fact that all MemFlash devices in the network could be supplied with a constant negative bulk voltage. Therefore, even though a single Memflash device has three active terminals, the Memflash device may be considered as a two-terminal memristive device.

The MemFlash operation mode as an adaptation of standard EEPROM cells for neuromorphic applications was proposed by Ziegler et al. in 2012 [15]. It has the possibility to become a suitable alternative to other memristive devices, because it is compatible with current silicon technology. This was shown by Himmel et al. with an industrial SONOS cell [76]. Thus, some common problems of memristive devices, such as retention and parameter spread, potentially do not affect MemFlash cells. In addition to the memristive behaviour, further investigation into the MemFlash operation, possible design improvement and potential usage in networks have been undertaken [18], [77], [78]. Additionally, the neuromorphic performance of a MemFlash cell was compared to other memristive devices [17]. The power consumption and switching times are large compared to the ionic devices. However, the purely on electron movement based MemFlash device shows comparable performance, bearing the advantage of a well understood and simple model of how the device functions.

2.4 Piezoelectric Field-Effect Transistor

In accordance with the search for new and possibly better gate insulators for MISFETs, a number of materials have been introduced into transistor gate stacks [79]–[82]. Mostly these novel materials are used to replace the SiO_2 gate oxide. However, materials are also being introduced into the gate stack at other locations to include additional functionalities. Thin-film transistors, biomechanical CMOS and piezotronics are just a few fields of current research efforts [83]–[86]. As the name suggests, the piezoelectric field-effect transistor (PiezoFET) is an enhancement of the standard field-effect transistor (see Chapter 2.1). The addition of a piezoelectric layer in the gate stack enables the transistor to show a reaction to mechanical stress.

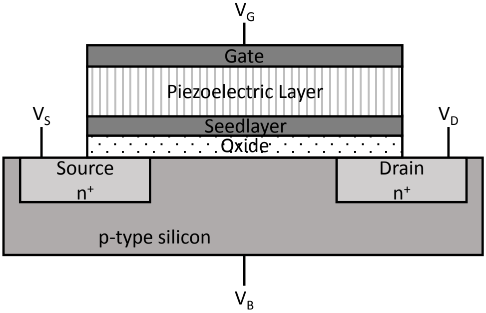


Figure 2.15 Schematic cross-sectional view of a piezoelectric field-effect transistor. The piezoelectric layer enables the transistor to react to stress applied across the device, since the charge generated due to the strain affects the channel current.

A schematic view of the cross section for a piezoelectric field-effect-transistor is given in Fig. 2.15. The structure resembles that of an EEPROM cell. In addition to the piezoelectric layer a seedlayer has to be included into the stack. This layer is necessary for the columnar, N-polar and (0001) oriented growth of the aluminium nitride (AlN), which is used as the piezoelectric material [87]–[89].

2.4.1 Piezoelectricity

The piezoelectric effect (and the inverse piezoelectric effect) is an indispensable effect in a number of applications, e.g. energy harvesting [90], [91] and medical imaging applications [92]. Starting from the Greek word for "to press", "piezo", it combines pressure and electricity and was first discovered by Pierre and Paul-Jacques Curie in 1880 [93], [94]. Only occurring in insulating materials, the piezoelectric effect shows itself in materials with unsymmetrical crystalline structures (e.g. PZT, AlN). When these crystalline structures are mechanically deformed, surface charges form. The deformation causes the molecular dipole moments inside the crystal to reorient and therefore move the centre of charge, leading to said surface charges. Applying an electric field across a piezoelectric crystal results in the opposite effect, called the invers piezoelectric effect. Here, the change in the shape of the dipoles results in a deformation of the crystal caused by the external electric field. These effects enable piezoelectric crystals to be used for the detection of stress or to produce soundwaves [92], [93], [95]. Both effects are illustrated in Fig. 2.16.

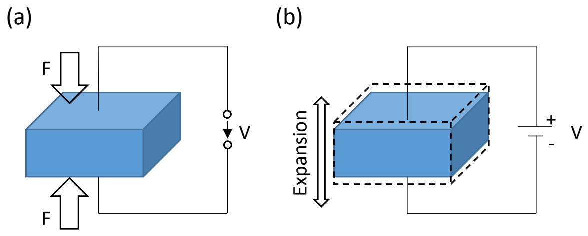


Figure 2.16 Reaction of an ideal piezoelectric crystal to (a) deformation and (b) an applied voltage.

A mechanical stress T leads to the displacement of charges within the crystal and therefore to a polarization P. This can be described using the electric displacement field D instead of the polarization.

$$D = d \cdot T + \varepsilon^T \cdot E \tag{2.12}$$

$$S = s^E \cdot T + d \cdot E \tag{2.13}$$

With S being the mechanical strain (deformation), d being the piezoelectric coefficient, ε^T being the permittivity, s^E being the elasticity constant and E being the electric field strength. For both formulas, the superscripted values are kept constant. Equation 2.12 is used to describe the direct piezoelectric effect, equation 2.13 for the invers piezoelectric effect. Additionally, it is important to note, that all equations given are describing the linear answer of the piezoelectric system to small disturbances.[96]

The strain S of a piezoelectric material in reaction to an externally applied electric field E is reflected in the piezoelectric coefficient d_{ij}.[97]

$$d_{ij,k} = \frac{\delta S_{ij}}{\delta E_k} \tag{2.14}$$

In the same way, the mechanical stress T on a piezoelectric material in reaction to an externally applied electric field E is reflected in the piezoelectric coefficient e_{ij}.[97]

$$e_{ij,k} = \frac{\delta T_{ij}}{\delta E_k} \tag{2.15}$$

Considering the application of the piezoelectric effect in this work, the important parameter is the piezoelectric coefficient e_{31}. It describes the relationship between a lateral stress and the electric field strength perpendicular to said stress. This effect is being utilized in this work in a way that stress applied across the piezoelectric layer results in an electric field able to influence the charge carrier density in the nearby semiconductor.

2.4.2 Cantilever Mechanics

To use a PiezoFET as a sensor for mechanical stress, a setup needs to be created where the application of a force leads to lateral stress across the transistor. In 2004 Wu et al. [27] presented a theoretical approach to a stress sensor based upon a field-effect transistor with a piezoelectric layer placed on a cantilever. A schematic view of this setup is shown in Fig. 2.17.

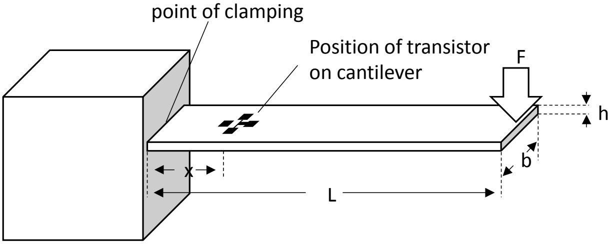


Figure 2.17 Simplified illustration of the stress sensor configuration consisting of a piezoelectric field-effect transistor on a Si cantilever.

Fig. 2.17 illustrates the important mechanical parameters of the setup. The free-standing length of the cantilever is given by *L*. The thickness of the beam is given by *h* and the width by *b*. Using these values, cantilever specific parameters such as the moment of inertia *I* can be calculated.

$$I = \frac{bh^3}{12} \tag{2.16}$$

This equation is valid for a rectangular beam only [98]. From this, the maximum deflection δ_{max} can be calculated in respect to a force F applied at the free end of the cantilever [99]:

$$\delta_{max} = \frac{FL^3}{3EI} \tag{2.17}$$

The additional parameter E needed for this calculation is the modulus of elasticity, or Young's modulus. It describes the relation between stress and strain in the cantilever.

Furthermore, the position of the transistor on the cantilever is highlighted in Fig. 2.17. The position of the transistor on the cantilever is vitally important because there are different magnitudes of tensile stress along the cantilever when a force F is applied at the tip. This stress σ is produced by the extension or compression of the cantilever surface. It results in a volume constant deformation and is given by

$$\sigma_x = \frac{M_x}{S_{b,x}} \tag{2.18}$$

Here, M_x describes the moment of bending at a point x along the cantilever and $S_{b,x}$ describes the section modulus at the same point x [100]. The values used in the calculation of the stress at a certain point along the length of the cantilever can be expressed as

$$M_x = F \times (l - x) \tag{2.19}$$

and

$$S_{b,x} = \frac{bh^2}{6} \tag{2.20}$$

for a beam with a rectangular shape as is used in this work [101].

3 Device Fabrication

This chapter describes all methods used during sample fabrication in this work. The methods are presented in order of appearance in the fabrication process. Parts of the process (i.e. oxidation and doping of the semiconductor) could not be done at the faculty of engineering at Kiel University and were therefore undertaken at the Fraunhofer Institute for Silicon Technology (ISIT) in Itzehoe. Afterwards the samples were transported to the “Kiel Nanolaboratory” at the faculty of engineering of Kiel University for further processing. At the end of this chapter, the different samples are presented, their specific characteristics highlighted and important details addressed.

The detailed use and the parameters for every step of the fabrication process are mentioned in this chapter when appropriate. In-depth fabrication flow charts, including processes and parameters can be found in the appendix (see chapters A.1 and A.2).

3.1 Oxidation

Local Oxidation of Silicon (LOCOS) is a common method of isolation in semiconductor fabrication. In an initial step, the active areas of the transistors are defined by applying a LOCOS oxide to the wafer surface. The basis for this work builds a boron doped 8-inch monocrystalline silicon wafer with a resistivity of 10 Ωcm, a crystal direction of <100> and a thickness of 725 µm. On said wafer, the future transistors were outlined and electrically separated using LOCOS.

In a first step of the LOCOS process, the areas in which the oxide is to be grown are defined. To do so, a layer of silicon nitride is deposited on the wafer and structured via photolithography (see chapter 2.5). To protect the underlying silicon from the White-Ribbon-Effect the nitride is deposited on top of a thin oxide layer [102], [103]. This thin thermal oxide layer is a sacrificial oxide and will be removed after the LOCOS growth and all ion implantation steps are completed. The purpose of this thin oxide layer is to keep stress exuded by the nitride layer from harming the bulk silicon underneath. In the defined areas, the LOCOS oxide is now thermally grown. This method assures less boundary layer effects than deposited oxide would. In a cross-sectional view, the edges of the LOCOS show a slowly narrowing progression which extends under the nitride protection layer. Due to its shape this phenomenon is called the “bird’s beak” and is regarded as a downside in industrial semiconductor fabrication. However, this effect is not of great importance in this work. On one hand, the size of transistors decreased dramatically in the last decades (following Moore’s Law [3]) and the distances between devices on a chip followed a similar path [104]. Therefore, having the passivating oxide migrate under the protecting nitride layer is a drawback in industrial fabrication. On the other hand, transistors with comparably large sizes are used in this work. Consequently, the bird’s beak effect is visible in the fabrication of the transistors used here, but has no limiting effects due to the device sizes.

3.2 Doping Techniques

As mentioned in chapter 2.1, a MOSFET has differently doped areas within the semiconductor device, which are crucial for the flawless operation of the device. Therefore, implanting the right number of dopants into the desired areas and at the most favourable depths is an important fabrication step.

In general, three different methods of doping are used in the industrial fabrication of semiconductor devices. Two of these methods (vapour-phase doping and doping from a doping-layer) may be further classified as thermal doping procedures. However, as they are not used for this work, here the focus lies on ion implantation.

3.2.1 Ion Implantation

In this work, four differently doped areas (source, drain, channel and bulk) have been defined during the implantation process. In the resulting n-channel field-effect transistors, the source and drain regions are n^+ doped with an As concentration of 5×10^{15} cm^{-3}. To allow a connection into the substrate, bulk regions are p doped with a B concentration of 5×10^{15} cm^{-3}. The channel regions are p doped with a B concentration of 2.1×10^{12} cm^{-3}.

For ion implantation, the doping gas is ionized, focused by electric field lenses and accelerated through a mass separator. Here, unwanted ions, which are by-products of the ionization process, are filtered out by deflecting them into covers behind the separator. Due to their different masses they do not follow the 90° trajectory and therefore do not pass through the covers. The ions are accelerated further and focused into a beam by lenses. Deflectors direct the ion beam to the sample, which is mounted onto the rotating sample holder. The beam strikes the sample at a small angle of about 7° to avoid channelling and therefore, assure the desired depth placement of the dopants. By rotating the wafer, a shadowing effect can be minimized as well.

The ions are accelerated with a voltage of about 100 kV. Therefore, by striking the wafer they do not only enter but damage the crystalline structure of the silicon. Additionally, they are not located at the lattice sites after being inserted. Consequently, the semiconductor has to be heated to a temperature between 500 to 1000 °C to restore the monocrystalline state of the material and include the dopants into the atomic lattice.

Despite ion implantation being the costliest method of doping, it is the most commonly used one. This is largely due to the fact, that ion implantation provides a great placement and dose accuracy. Additionally, dopants can be brought into defined depths of the wafer without having to dope the sample surface. Another advantage of ion implantation is, that standard resist masks for photolithography can be used [103]–[105].

3.3 Etching

Etching in semiconductor fabrication is used to remove entire layers of various oxides, nitrides, semiconductors and metals. Additionally, structures created by photolithography can be transferred into desired layers on the semiconductor surface. Two main groups of etching methods can be distinguished: Chemical etching and physical etching. Both fields of methods are explained in the following subchapters, however, at this point in the fabrication process only chemical wet etching is used. Ion beam etching is used in a later stage of the fabrication of piezoelectric field-effect transistors to structure the entire gate stack.

3.3.1 Chemical Etching

In this work, a 1:100 hydrofluoric acid (HF 48 %) solution is used to thin the silicon dioxide in a 2 x 2 µm window above the drain region and, using a second photoresist mask, remove remaining oxide from the drain, source and bulk regions. The reaction of HF with the SiO_2 is characterised by the following equation [106]

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{3.1}$$

However, even though both tasks are of importance for the finished device to work faultlessly, adjusting the thickness of the tunnelling oxide was the main objective of the HF solution. Therefore, the etch rate (about 1.6 nm/min) of the solution was adjusted to accurately thin the tunnelling oxide.

Chemical etching in general has the advantage of high selectivity. Thus, the etchant can be chosen in a way that merely the desired material is dissolved. This allows the use of etch stops, which are layers of different materials underneath or alongside the material to be etched. Consequently, with this method, materials can be completely removed without greatly harming adjacent layers and structures. However, most chemical etching methods are isotropic. This has to be taken into account if structures are to be transferred into a layer using masks. Depending on the material, its crystalline structure and the etchant, etching underneath the mask may be observed.

Chemical etching methods can be further split into the fields of chemical wet and dry etching. As no chemical dry etching was used during the fabrication of samples, from this point forward only chemical wet etching will be explained further.

Chemical wet etching solutions need to fulfil as many of the following requirements as possible [106]:

- the mask used in the process (most commonly photoresist) may not be attacked by the solution
- they need to exhibit high selectivity between the materials used in silicon technology
- no gas phase reaction products should be formed during etching, in order to limit the chance of local shadowing effects due to bubble formation in the surface
- to avoid particles in the solution, the reaction products need to liquidize immediately
- the etch rate needs to be constant over a long period of time and it needs to be in a manageable range, as to avoid extremely long or short etch times
- a defined etch stop has to be possible by watering down the solution
- (for industrial mass production) the etching solutions need to be harmless for the environment and easily disposable
- the solutions should work at room temperature to keep the instrument-based outlay as simple as possible.

3.3.2 Physical Etching

Physical etching methods are characterised by a lack of chemical components in the etching process. However, some physical dry etching methods may be expanded to include chemical components as well. In this work, solely physical ion beam etching (IBE) was used. As mentioned before, IBE was used to structure the gate stack of the piezoelectric field-effect transistors. An Oxford Instruments PC3000 was used in combination with a Hiden Analytical mass spectrometer.

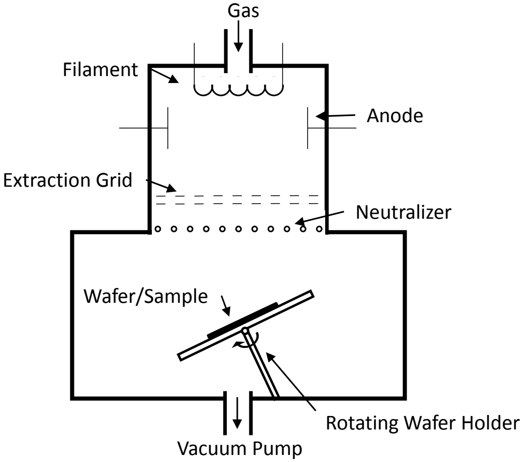


Figure 3.1 Illustration of an ion beam etching chamber, comprising the plasma generation in the top part, with ion extraction and acceleration for the ion beam generation and the rotatable and inclinable sample holder.

Ion beam etching takes place in a vacuum chamber in which an inert gas (e.g. Ar) is ionized (see Fig. 3.1). Applying a potential at the extraction grid accelerates ions towards the sample. The ions striking the sample will extract atoms from the surface [107]. As these detached atoms are not chemically bound, they are free to set at any surface. This includes the chamber walls and other parts of the sample itself. By tilting the sample holder and rotating it throughout the etching process, atoms that settle on the sides of etched structures are instantly removed. To compensate the charging of the sample surface the neutralizer emits electrons.

As in every method of etching, knowing when the desired depth is reached or a layer is completely removed, is an important part of the process. In industrial semiconductor fabrication, where maximum device uniformity is desired, processes are created, optimised and checked thoroughly, which makes manual supervision obsolete. With samples in a non-industrial setting, variations in layer thickness and process quality are common and result in a variation of endpoints. Therefore, the manual supervision of an etching process is critical. In chemical wet etching, visual monitoring may be enough to register changes in colour of the sample. For the ion beam etching processes, however, secondary-ion mass spectrometry (SIMS) was used to determine the endpoints. SIMS works in combination with any sputter-based etching process. It collects secondary ions ejected from the sample and analyses them using mass spectrometry. An exemplary measurement is shown in Fig. 3.2.

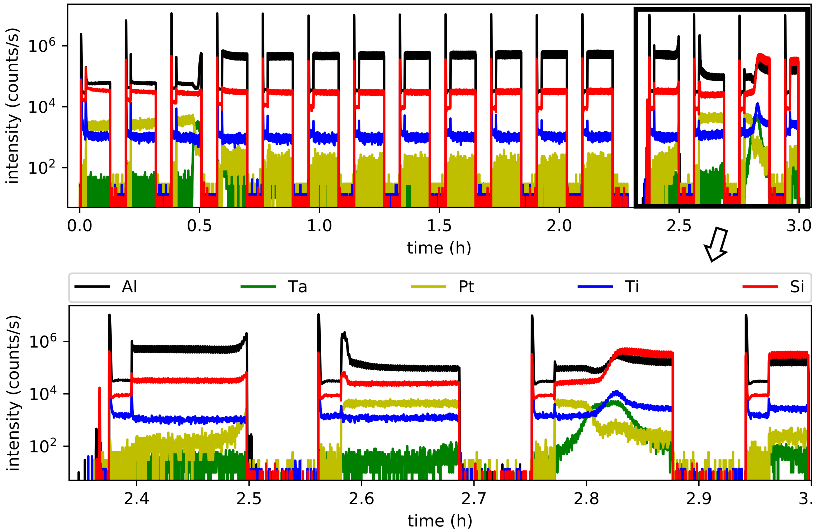


Figure 3.2 Exemplary secondary-ion mass spectrometry (SIMS) measurement results recorded during the ion beam etching process of a piezoelectric field-effect transistor's gate stack. The four final etching cycles are magnified in the bottom graph to show the intensity changes at the end of the etching process and from that determine the endpoint of the process.

Thus, the ratio between mass and charge of the ions is measured and the element determined. Once a layer is removed, the corresponding signal decreases and the signal for the layer underneath will increase. Consequently, with this method a live monitoring of the etching progress is possible. An exemplary etching process of the gate stack of a piezoelectric field-effect transistor is shown in Fig. 3.2. The intervals are due to the etching process itself. Since the sample heats up during the ion bombardment, after every 6 min of etching a 3 min cooling break is implemented. Of greater interest is the final phase of the etching process highlighted in the full scale representation (upper graph) and magnified in the lower graph. At this point, the AlN layer is almost completely etched and the corresponding Al signal (black) decreases. The underlying Pt layer signal (yellow) rises and decreases again when the layer is almost completely removed. At the point in time when this happens, the next layer, in this case Ta, starts to be etched, with the corresponding signal (green) rising. Since the Ta layer is merely a few nm thick, the increase in the signal is very short and a rise in the underlying signals start almost at the same time. These underlying layers are SiO2 (red) and Ti (blue). In order to ensure the complete removal of the Ta layer and therefore avoid unwanted connections in the wiring, the etching process was conducted for a short time after the Ta signal reached its initial value.

3.4 Lithography

This technique, as can be taken from the fact that it has already been mentioned a couple of times in this chapter, is one of the most important methods of fabrication for any semiconductor device. It is used as the basis for a number of structuring procedures, by allowing the transfer of a structure onto a mask of removable photoresist. These structures may in a following process be used as a deposition guide or a mark for etching processes.

The standard lithography process can be split into three parts: The application of the photoresist layer, the structuring of the photoresist layer and the removal of the photoresist mask.

For the application of a photoresist layer several methods can be used. In this work, photoresist (AZ 5214 E from Microchemicals GmbH [108]) is applied by spincoating. When using this technique, the sample is placed onto a rotatable holder and secured by vacuum. After 150 µl of the resist is applied to the surface of the sample, the holder is rotated for 60 s at 4000 rpm. Here, it is important that the speed of the rotation be slowly ramped up, to avoid an uneven dispersion of resist. Depending on the photoresists viscosity and the rotations per minute (rpm) of the sample holder, a defined thickness can be achieved. Following the application, the sample is heated for 50 s at 110 °C to evaporate the remaining solvents. With this method, a solid, easy to structure polymer layer of consistent thickness can be applied to the sample surface.

Depending on the desired properties of the final mask, different photoresists and therefore, structuring techniques have to be chosen. In general, we distinguish between two types of resist, positive and negative. Exposing a positive resist to UV-light will lead to a destruction of crosslinks within the resist, which makes the exposed areas dissolvable in standard developer. Exposing a negative resist to UV-light, however, leads to the opposite effect of further crosslinking within the resist. Consequently, these areas are harder to dissolve in developer.

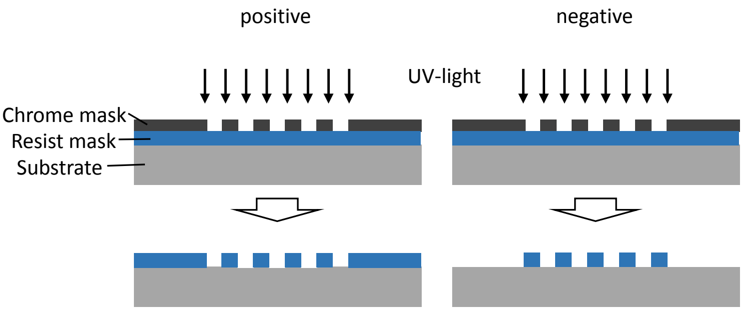


Figure 3.3 The differences between positive and negative photoresist. Exposing the negative resist to UV light crosslinks the polymer and results in the shown mask after development. In contrast, in positive resist the polymer chains are broken by UV light and development results in the shown mask.

In Fig. 3.3 the differences between the two types of resist are illustrated. Additionally, the chrome mask, which is necessary for the transfer of structures into the resist, is shown. This mask contains the final version of the desired structures in chrome on a UV-light transparent glass substrate. The chrome mask is placed onto the substrate, with the chrome layer being in contact with the sample. Thus, any shadowing or light scattering effects are minimized. In this work, the photoresist used is a reversal resist. Hence, it can be used as either positive or negative resist. For further processing with ion beam etching, the positive properties of the resist are used. Thus, the sample can at this point be placed in a developing agent to remove the unwanted resist. However, for the deposition and wet chemical etching steps, the negative properties are used. In order to do so, the resist needs to be heated (120 °C for 120 s) once more, following the first exposure. Furthermore, the resist has to be exposed to UV light again, this time for 7 s, in order to make the previously unexposed areas soluble. Following the exposure, the sample is placed in a developing agent to remove the unwanted resist. This leaves the sample with a defined mask of photoresist and ready for further processing [108]–[110].

3.5 Sputter Deposition

Sputter deposition is one of the main techniques used in silicon technology for the deposition of thin films [111]. Here, an inert gas (e.g. argon) is ionized and the ions are accelerated towards a target in order to eject surface atoms. Unlike other deposition techniques, like e.g. evaporation, sputtering is widely used because it allows the creation of a film with the same composition when sputtering alloys. Out of the many variations of sputtering processes, in this work direct current (dc) magnetron sputtering is used. The parameters for all thin films deposited with a Univex 450b system from Leybold are given in table 3.1.

material	Ti	Al	Al	Nb	AlN
power	300 W	100 W	100 W	360 W	150 W
time	15 s	10 s	10 s	3 s	50 s
gas (Ar)	15 sccm	40 sccm	40 sccm	25 sccm	-
gas (N_2)	-	-	-	-	8 sccm

Table 3.1 The parameters used in this work for the DC magnetron sputter deposition (in the Univex 450b system from Leybold) of thin layers.

The Ti was used in this work to provide contact to the semiconductor (source, drain and bulk regions) for all devices and as gate material for the fabricated MOSFETs. Al and Nb was used as the floating gate for the MemFlash cells. The AlN was deposited as an adhesive layer for the SiO MemFlash devices.

The piezoelectric field-effect transistors used 10 nm Ta as an adhesive layer for the following 100 nm Pt. Said Pt was needed to ensure the columnar growth of the piezoelectric AlN. The AlN layer had a thickness of 500 nm. As a top electrode (gate) 300 nm Pt were sputtered on a 10 nm Ta adhesion layer. These thin films were provided through a collaboration within the faculty and deposited using a Von Ardenne CS 730S magnetron cluster system with the parameters from Yarar et al. [87].

Fig. 3.4 shows a schematic view of a sputter chamber. The sample is placed on the sample holder underneath the target. A vacuum is created inside the chamber and a predefined amount of gas inserted. Following this, a plasma is ignited in the chamber and the resulting ions are accelerated towards the target by an electric field. The collision of the ion with the target surface results in a train of events that can lead to the ejection of atoms from the target. The ratio of the number of atoms ejected from the target to the number of ions striking the target is defined as the sputtering yield. However, the target surface might not be “clean”, a native oxide could have formed on the surface or other impurities might have settled there. Therefore, a shutter above the sample acts as an umbrella and prevents atoms from reaching the sample during the first part of the sputtering process. This initial part is used to clean the target and make sure only the desired metal is deposited. The shutter is than opened for a specific amount of time to reach the wanted layer thickness on the sample. Furthermore, when sputtering on resist the thermal balance has to be taken into account. The heating of the sample has to be limited to prevent the photoresist from burning. This could result in unwanted structures and problems when removing the resist.

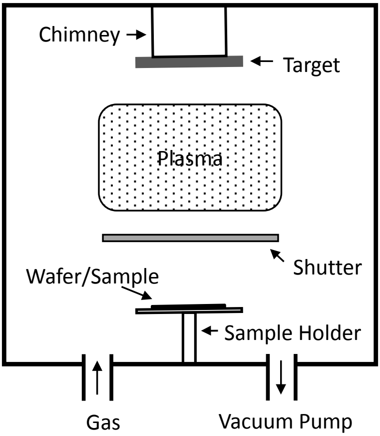


Figure 3.4 Schematic design of a sputter chamber used for the deposition of metallic thin films.

The free electrons created during the process are accelerated by the electric field and, if striking an atom on their way, contribute to sustaining the plasma by creating ions. To increase the distance the electrons have to travel, an arrangement of magnets is used to force the electrons into a helical orbit. This method increases the chance of ionization and prevents electrons from striking the chamber walls, where they could not contribute to sustaining the plasma [112].

Additionally, reactive sputtering was used during this work. It shows all the same characteristics of regular dc magnetron sputtering, with the variation of a reactive gas being used for the process. Typically, reactive gases (e.g. N_2 or O_2) have a lower atomic mass than argon, which results in a lower yield for reactive sputtering. This can be aided by adding argon in with the reactive gas. Either way, this form of sputtering relies on the reaction of the material with the gas to form a compound layer on the substrate surface [113], [114].

3.6 Fabricated Devices

Using the before mentioned techniques, six different sample types were fabricated. All devices were built on the same semiconductor base with the before mentioned doping concentrations and a 13 nm thick SiO_2 gate oxide. The devices can be split into three categories: MOSFET devices, MemFlash devices and Piezoelectric FET devices. The two different devices of the MOSFET type were a classical MOSFET and a MOSFET with a tunnelling window above the drain region. The two MemFlash devices differed in the material used for the isolation layer between the floating and the control gate. The two piezoelectric field-effect transistors were a floating gate transistor comprising a piezoelectric layer in the gate stack and a reference sample. The reference sample was fabricated alongside the PiezoFET, however it was built without a piezoelectric AlN layer in the gate stack.

Since the initial steps for all devices are similar they are given in the following overview. In the sub-sections, the device specific fabrication steps are stated and a diagram of each device is shown. These cross-sectional diagrams include the used materials and thicknesses. Additionally, a detailed process flow for all fabricated devices can be found in the appendix (see chapters A1 and A2).

The fabrication of all devices started with the structuring of the SiO_2 layer. The etching of the SiO_2 layer for either thinning of the tunnelling window oxide (MemFlash devices and the tunnelling window MOSFETs) and for the removal of the protective oxide above the source, drain and bulk regions (all devices), was done by chemical wet etching. For this, a 1:100 HF solution was used. To avoid the forming of an extensive native oxide layer at the drain, source or bulk regions, the Ti wiring was deposited immediately after the removal of the protective oxide. This was done to achieve the best connection into the doped regions. From this point forward, the fabrication of each device differs, therefore they are looked at individually. For each device a schematic cross-sectional view is displayed, showing the finished device with all materials used.

MOSFET

In the case of the MOSFET devices Ti was used for the gate electrode, deposited by sputtering and structures with a lift-off. An illustration of the resulting MOSFET devices with and without a tunnelling window are shown in Fig.3.5 and Fig. 3.6, respectively.

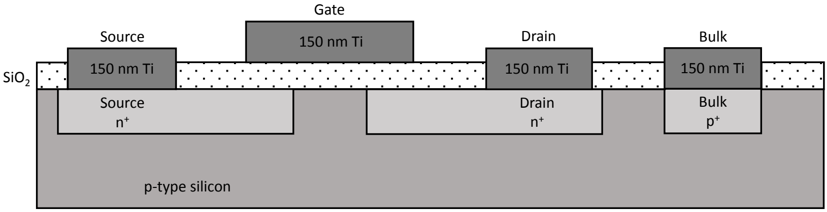


Figure 3.5 Cross-sectional view of the MOSFET layout used in this work, including the used materials and layer thicknesses.

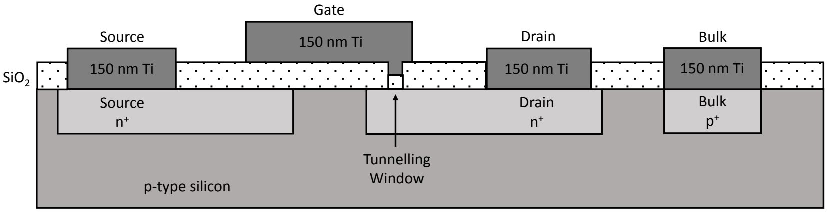


Figure 3.6 Cross-sectional view of the tunnelling window MOSFET layout used in this work, including the used materials and layer thicknesses.

MemFlash

Two types of MemFlash devices can be distinguished. The main distinguishable difference between the two device types is the dielectric material used to isolate the floating gate from the control gate. However, considering the differences in the fabrication process, both processes are presented briefly.

For silicon oxide MemFlash devices Al (with a thin Nb coating) was used for the floating gate. The Al and Nb were deposited by sputtering. The floating gate pattern was transferred onto the transistors by using standard UV lithography and removal of the excess Nb by plasma etching with SF_6. The Al was structured with a wet chemical etching process using TMAH. Following this, the gate isolation area was defined using lithography and a thin layer of AlN was deposited using reactive sputtering as an adhesion layer. Afterwards the gate isolation (SiO) was deposited with thermal evaporation. In a final step, the control gate area was defined using lithography and Ti deposited by sputtering.

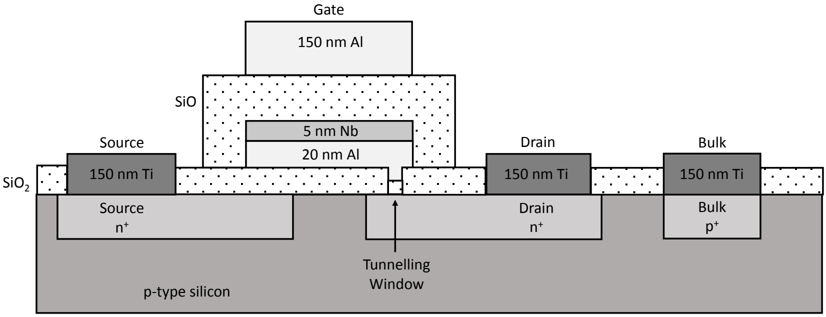


Figure 3.7 Cross-sectional view of the MemFlash device layout (comprising a SiO gate stack isolation layer) used in this work, including the used materials and layer thicknesses.

For polymer MemFlash devices Al was used for the floating gate, deposited by sputtering and structured with a wet chemical etching process. As an isolation between the floating gate and the control gate a polymer (AZ nLOF 2070 [115]) was used. This polymer was deposited by spincoating and easily structured using standard UV lithography. Hence, lithography was used to excavate the source, drain and bulk regions. This way, the polymer acted as an isolation across the entire sample, only the before mentioned regions were exposed and could be externally contacted. In a final step, the Al control gate was deposited by sputtering and structured with a chemical wet etching process. To remove the photoresist mask used for the final structuring step, acetone could be used, because the polymer was chosen specifically with a certain tolerance to acetone exposer in mind.

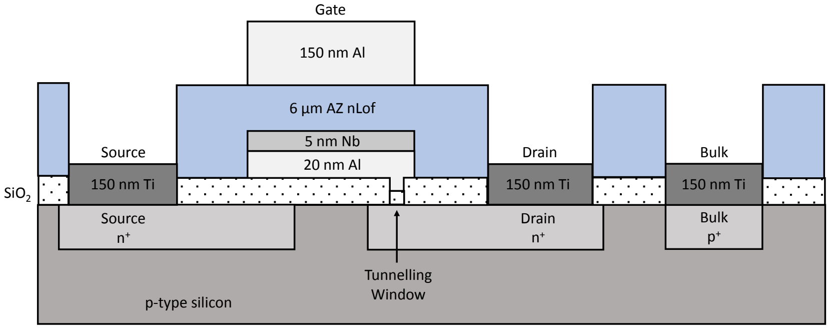


Figure 3.8 Cross-sectional view of the MemFlash device layout (comprising a polymer gate stack isolation layer) used in this work, including the used materials and layer thicknesses.

Piezoelectric FET

In the case of the piezoelectric FET, Ta was deposited by sputtering and used as an adhesion enhancing agent for the following deposition of Pt. Pt formed the seedlayer for the desired columnar growth of the AlN. The AlN was used as the piezoelectric layer in the gate stack and deposited using a low temperature sputtering process. This process was developed by Yarar et al. and the AlN was deposited by the chair of “Inorganic Functional Materials” [87]. For further information concerning the AlN and the deposition procedure this work is recommended. As a control gate, Pt was deposited on top of the AlN. The Pt was deposited in a thick layer of 300 nm to avoid any damages to the AlN in future bonding steps. To structure the entire gate stack, ion beam etching was used as a final step. An illustration of the resulting piezoelectric field-effect transistor is shown in Fig. 3.9.

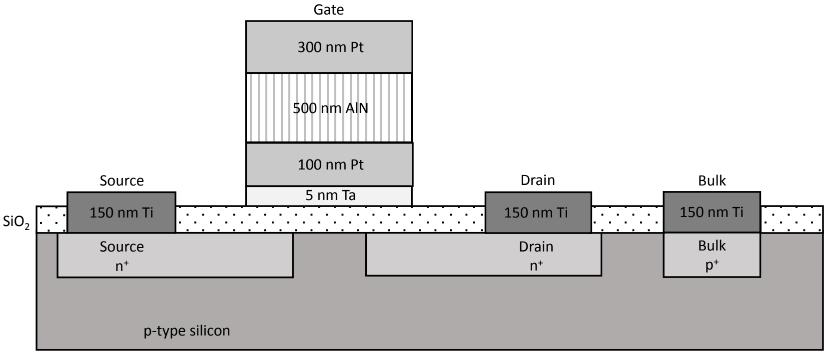


Figure 3.9 Cross-sectional view of the piezoelectric field-effect transistor layout used in this work, including the used materials and layer thicknesses.

For comparison the cross-sectional view of the reference sample layout is shown in Fig. 3.10. Reference samples were fabricated and analysed during this work as a way of confirming the piezoelectric field-effect transistors. All reference devices were fabricated alongside the piezoelectric FETs. The only difference is the lack of piezoelectric layer in the gate stack.

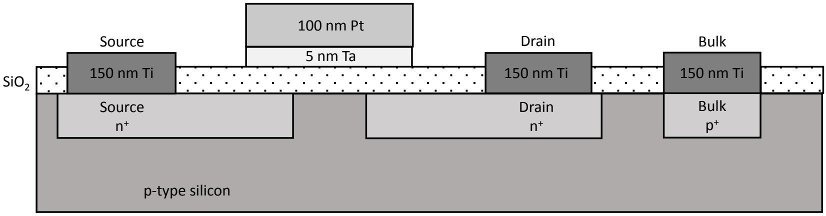


Figure 3.10 Cross-sectional view of the reference sample layout used in this work, including the used materials and layer thicknesses.

4 Characterisation Methods

This chapter highlights the methods used for the characterisation of the MOSFET, MemFlash and piezoelectric-FET devices. First the variations of all current-voltage measurements, including the measurement setups are shown. Further, the setup for the capacitance-voltage measurements is introduced. Finally, two variations of mechanical stress measurements are presented. Both setups, mechanical and magnetic, are used for the excitation of the piezoelectric-FETs. Paired with current-voltage measurements they are used to show the device behaviour.

4.1 Current-Voltage Measurements

For all variations of current-voltage measurements the Hewlett-Packard 4145A Semiconductor Parameter Analyzer was used. A connection to a computer was realized through general purpose interface bus (GPIB) and a graphical user interface (GUI) was created in Microsoft Visual Studio (see appendix A.3 for a description) to conduct measurements remotely.

The HP 4145A Semiconductor Parameter Analyzer has a total of four source measure units (SMUs). SMUs use a four-quadrant output and surpass standard programmable power supplies in precision. They are often used for the characterisation of devices that require low-level sourcing and measuring. The SMUs are connected via a triaxial cable and an adapter to the BNC connector of four micromanipulators. At the end of the positioning arm of each manipulator, a wolfram needle is used for the connection of the device. The micromanipulators are located inside a shielded wafer prober with a moveable sample holder stage. To aid the connection of the devices, a microscope is mounted inside the wafer prober above the stage.

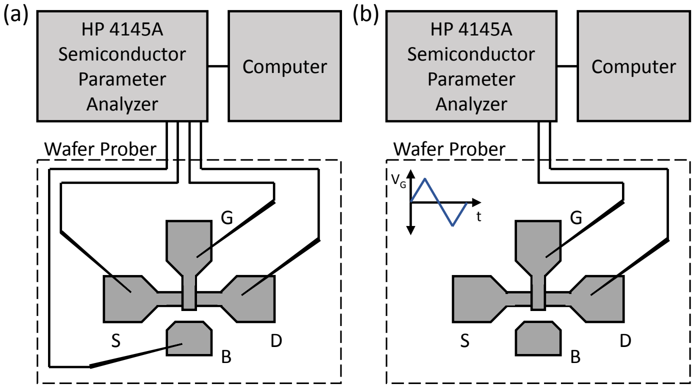


Figure 4.1 Measurement setups for the (a) MOSFET characterisation and (b) the tunnelling current measurements. The setup shown in (a) was further used for the current-voltage, pulse and retention measurements of MemFlash cells.

4.1.1 MOSFET Measurements

These measurements are used for the characterisation of MOSFET devices. Two types of current-voltage curves describe the behaviour of a field-effect transistor. To obtain said characteristics, the SMUs are connected to all four pads of the device. For the output measurements, the bulk and the source potentials are set to 0 V, the gate potential is kept at a constant value and a voltage sweep is applied at the drain. For the transfer measurement, bulk and source potential are again kept at 0 V, the drain potential is kept constant and the voltage sweep is applied at the gate. In both cases, a voltage sweep is defined as starting at 0 V and increasing at a defined step width to a chosen maximum voltage value. For every voltage applied during the sweep a corresponding current value is measured and stored in the internal storage of the Parameter Analyzer. Following the measurements, all acquired data is transferred to the computer. A schematic view of the experimental setup is shown in Fig. 4.1 (a).

4.1.2 Tunnelling Current Measurements

For the measurement of oxide thicknesses (primarily for the determination of the tunnelling oxide thickness within the tunnelling window of MemFlash cells) the measurement setup shown in Fig. 4.1 (b) was used. Two SMUs of the HP 4145A Semiconductor Parameter Analyzer were used. One SMU was defined as the ground potential and set to 0 V. The other SMU was used to sweep a defined voltage range. To aid comparison between all measurements, the ground potential was always applied at the drain (semiconductor) and the sweep was applied at the gate (metal). For this type of measurement, a sweep was specified as a voltage, starting at 0 V and increasing at the former defined step width to a chosen maximum voltage value. After reaching this value, the voltage was decreased in the same increments to a chosen minimum voltage value. Finally, the voltage was increased back to the starting value of 0 V. The applied voltage sweep is depicted in Fig. 4.1 (b). For every voltage applied during the sweep a corresponding current value was measured, sent back to the computer and depicted in a live view within the GUI.

4.1.3 Hysteresis Measurements

This measurement setup was used for the characterisation of MemFlash cells. In order to record the characteristic pinched-hysteresis loop of a memristive device, a quasi-two-terminal setup had to be used (see chapter 2.3.2). The micromanipulators were connected to the device as shown in Fig. 4.1 (a). The source and the gate potential were set to ground and the device was driven by a voltage sweep at the drain. The sweep was specified as a voltage, starting at 0 V and increasing with the before defined step width to a chosen maximum voltage value. After reaching this value, the voltage was then decreased in the same increments to a chosen minimum voltage value. Finally, the voltage was increased back to the starting value of 0 V. For every voltage applied during the sweep a corresponding current value was measured, sent back to the computer and depicted in a live view within the GUI. Additionally, due to the nature of the device, the mentioned minimum voltage value was negative to reset the device and therefore, record the entire hysteresis. With this in mind, the bulk potential had to be set to a greater negative value than the minimum voltage value applied at the drain (see chapter 2.1.3).

4.1.4 Pulse Measurements

To analyse the created memristive devices beyond the current-voltage pinched hysteresis loop pulse measurements were conducted. They were used to show the retention behaviour and the answer to pulse stimulation of the devices. For both measurement types source and gate were set to ground, the bulk was kept at a constant negative voltage (greatest negative voltage applied to the device) and pulses were applied at the drain. The micromanipulators were connected to the device as shown in Fig. 4.1 (a).

Two types of pulses can be classified: read pulses and write pulses. The former was used to determine the state of the device by applying a 60 ms voltage pulse. The magnitude was chosen in a way that it does not affect the device more than necessary. The latter was used to set and re-set a device. Consequently, no limitations on the magnitude of the voltage pulses were imposed.

Retention measurements were conducted by first applying a read pulse to get the initial state of the device. A number of write pulses were then used to set the device. Following every write pulse, a read pulse recorded the device’s state. The retention was then determined by applying read pulses in specified intervals.

Pulse measurements also started with a read pulse to determine the initial state of the device. Varying pulse trains were applied to the devices to examine charging and dis-charging behaviour when stimulated by pulses, not constant voltages. Using the GUI, pulse duration, magnitude of read and write pulses and the time interval between the pulses could be set. However, all pulse trains not only started with a read pulse, between every two write pulses a read pulse was applied. This way not only the initial state of the device, but the device’s state after every event was recorded.

4.2 Mechanical Stress Measurements

These measurements were used to record the current answer of piezoelectric field-effect transistors when submitted to mechanical stress. For this purpose, samples were thinned by grinding, to make them more flexible. Additionally, the samples were cut into cantilever structures to further improve flexibility. Applying stress across the devices was achieved in two ways, by mechanical or magnetic excitation. Both methods of recording the influence of mechanical stress required the same connection arrangement. However, in comparison to previous measurements, the devices were not directly connected with needles. Bond wires were used to connect the device to a printed circuit board (PCB). Micromanipulators with wolfram needles were than attached to connector plates on the PCB, to supply the needed voltages and measure the current. This ensured a stable link between the SMUs and the device, even when the cantilever was bent. In order to test this linkage and make sure the device was not damaged during bonding, the MOSFET measurements were conducted before and after bonding.

4.2.1 Mechanical Excitation

For the mechanical excitation of the cantilever the arrangement shown in Fig. 4.2 (c) was used. The cantilever was placed in the holder and a transistor was connected to the PCB via bonding. To measure the influence of mechanical stress on the cantilever and therefore the transistor, the source and bulk potentials were set to ground. At the gate and the drain constant voltages were applied to operate the transistor at a fixed point. The channel current was recorded permanently when all control-voltages were applied. Additionally, a micrometre screw was fixed to an electric motor and placed underneath the freestanding tip of the cantilever. The motor was driven via an H-Bridge setup and controlled with an Arduino Nano. This setup allowed an upwards bending of the cantilever (see Fig. 4.2 (b)) and the simultaneous recording of any chance in current through the field-effect transistor using a SMU.

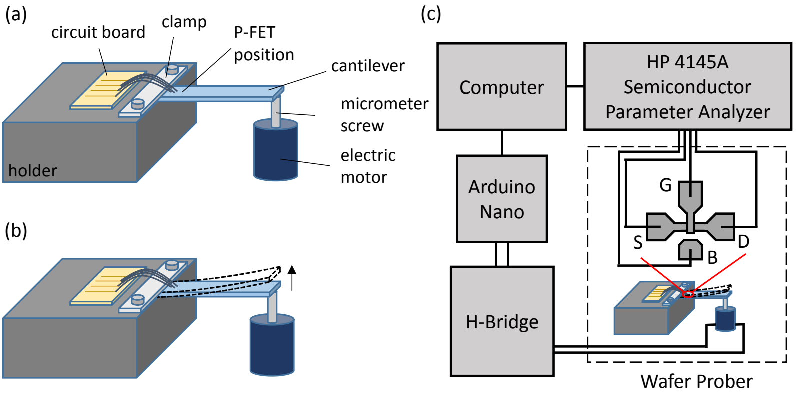


Figure 4.2 Measurement setup designed for the mechanical excitation and simultaneous data recording of cantilever based stress sensors. (a) Sample holder with attached stress sensor (cantilever + piezoelectric field-effect transistor) and the mechanical excitation unit, consisting of a micrometre screw and an electric motor. (b) The unilateral tip displacement possibilities of the proposed setup. (c) The external connection of the excitation mechanism and the connection scheme of the transistor inside the wafer prober.

4.2.2 Magnetic Excitation

This measurement setup was implemented because the purely mechanical excitation via the micrometre-screw only allowed unidirectional deformation of the cantilever. Additionally, the response time of the electric motor and the physical extension of the micrometre-screw only allowed the analyses of very low frequencies.

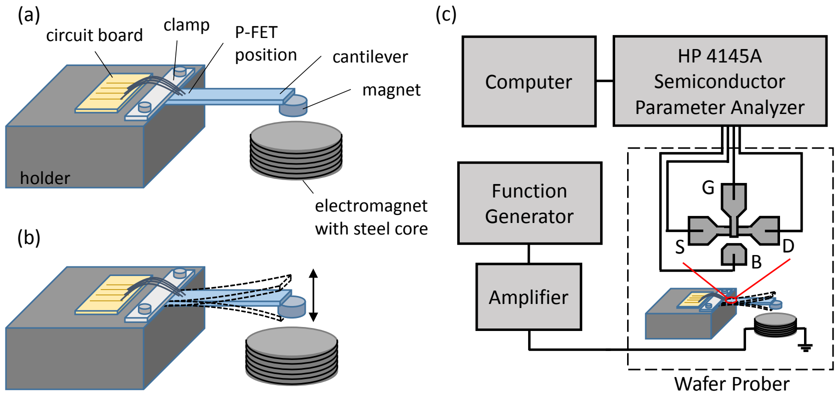


Figure 4.3 Measurement setup designed for the magnetic excitation and simultaneous data recording of cantilever based stress sensors. (a) Sample holder with attached stress sensor (cantilever + piezoelectric field-effect transistor) and the magnetic excitation unit, consisting of a round permanent magnet (material = NdFeB, height = 1 mm, diameter = 6 mm, weight = 0.21 g, magnetic flux density = 0.14 T) and an electromagnet. (b) The bilateral tip displacement possibilities of the proposed setup. (c) The external connection of the excitation mechanism and the connection scheme of the transistor inside the wafer prober.

With the setup shown in Fig. 4.3 (c), excitation in two directions was possible (see Fig. 4.3 (b)). Furthermore, a characterisation of the transistor under stress could be achieved without additional equipment. A permanent magnet was attached to the tip of the cantilever and an electromagnet placed underneath. The electromagnet was driven by a function generator, supported by a voltage follower. However, even though this setup allows the measurement of bi-directional cantilever displacement, it is still limited by the speed of the data recording setup of SMU and computer. It does not allow the measurement of high frequencies. A maximum recording rate of 100 mHz was possible. Even though the electromagnet, driven by the function generator, could create a higher frequency field and the cantilever would follow that field, the recording rate limits the maximum excitation frequency. Thus, this setup was used to check the piezoelectric functionality of the transistors after bonding and see its response to low frequency signals.

4.2.3 Periodic Excitation

In order to gain the technical potential to analyse the sensitivity of the sensor and therefore the piezoelectric transistors, an additional setup was used. Here, the electromagnet and the free-standing cantilever setup was expanded with faster data recording. Initially, the voltages needed for the operation of the transistor were no longer supplied by the SMU. Hence, a power supply was used to supply the drain voltage to the transistor. The second output of the function generator was used to supply the gate voltage. The source and bulk potentials were set to ground. This way, a constant voltage or a voltage sweep could be applied at the gate. The SMU was replaced with a lock-in amplifier which was synchronised with the frequency of the function generator. The channel currents exceeded the range of the lock-in amplifier and therefore, a resistor was used in series to the channel. This way, the voltage across the resistor could be recorded by the lock-in and the peak-to-peak amplitude recorded with an oscilloscope. Additionally, the gate and drain voltage were recorded with the oscilloscope to control the correctness of the applied voltages. Finally, the voltage signal across the resistor at the drain was not only fed to the Lock-In, but simultaneously recorded with the oscilloscope. This way, the live channel signal could be recorded in addition to the peak-to-peak amplitude measurement. In order to record the signal across the resistor, an instrumentation amplifier was used to supply sufficient voltages to the oscilloscope. All voltages recorded were displayed on and saved to the computer. In Fig. 4.4 the connection scheme is shown. To study the cantilever-transistor relationship and find the operating point at which the sensor is most sensitive, a periodic signal with constant amplitude and frequency was used to excite the cantilever, the drain voltage was kept constant and the gain voltage was ramped up. Using the Lock-In output, the point of highest sensitivity could be obtained.

Furthermore, the frequency behaviour of the cantilever was to be investigated, in order to determine the resonance frequency and the effect of higher excitation frequencies on the transistor behaviour. Hence, constant voltages were applied at the gate and the drain. The source and bulk potentials were set to ground. In order to ramp the frequency of the signal applied to the electromagnet, the function generator's modulation setting was used. As the second output was needed to do so, the gate voltage for this measurement was supplied by a power supply. The peak-to-peak amplitude was again recorded using the lock-in amplifier and transmitted to the oscilloscope. Further were the gate and drain voltages recorded with the oscilloscope, as well as the signal across the resistance at the drain.

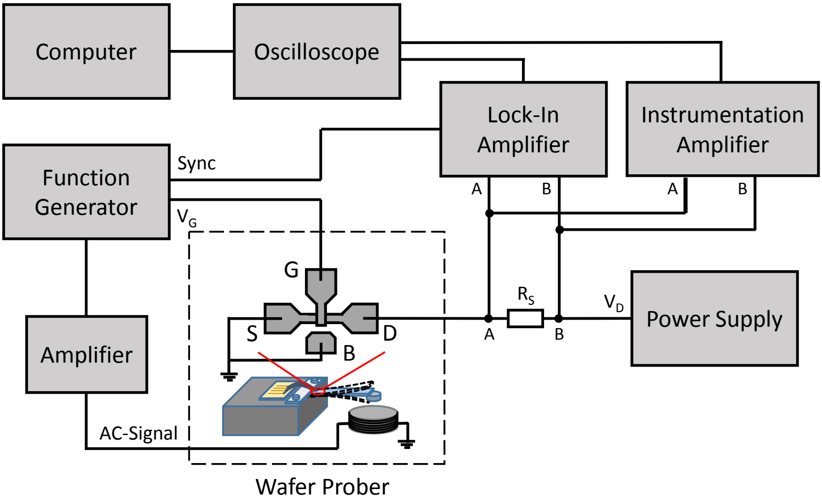


Figure 4.4 Measurement setup designed for the magnetic high frequency excitation and simultaneous data recording of cantilever based stress sensors. The external connection of the excitation mechanism and the connection scheme of the transistor inside the wafer prober. With the Lock-In amplifier the current delta of the transistor output in response to an AC excitation signal could be recorded. Simultaneously, the voltage signal across the serial resistance is amplified by an instrumentation amplifier and recorded.

5 Experimental Results and Discussion

In this chapter the previously described measurement setups were used to characterise the fabricated devices. Firstly, the MOSFET devices were investigated to show their functionality. Additionally, the tunnelling window oxide thickness was studied to provide the basis for the MemFlash cell fabrication. The charging and discharging of the floating gate of all MemFlash cells in this work was achieved by electron tunnelling. In order to optimise MemFlash device performance, the oxide barriers were chemically thinned and electrically investigated to determine their thickness and behaviour. Secondly, two types of MemFlash cells were fabricated and characterised. Both devices showed the same structures with a variation of the floating gate isolation material. With the silicon oxide based MemFlash devices showing reproducibility limitations, polymer based devices were created to allow the investigation of the oxide thickness dependent behaviour. This investigation consists of voltage dependent, frequency dependent and pulse measurements.

Finally, the characterisation of the piezoelectric field-effect transistor was undertaken. Here, different methods of cantilever excitation were reviewed in order to show the possibility of the device being used as a basis for stress sensors and other applications. The point of operation at which the transistor is most sensitive was determined, as well as the influence of operation at different excitation frequencies investigated. Lastly, a comparison between two different piezoelectric materials in regards to the influence of their different piezoelectric coefficients on device behaviour and sensitivity was conducted.

5.1 MOSFET

For the characterisation of the MOSFET devices, the methods and setup described in chapter 4.1.1 were employed. Initially, the output and transfer *I-V* characteristics of the MOSFETs were recorded. Since the fabrication process of MOSFETs was newly implemented in this work, these measurements were employed to determine the flawless functionality of the created devices. Furthermore, from these characteristics, device specific values, such as the threshold voltage could be obtained. In addition, these measurements allowed the comparison of devices with different channel dimensions.

In preparation of MemFlash device fabrication and characterisation, an additional MOSFET device type was fabricated. These MOSFETs had a tunnelling window with the size of 2 µm x 2 µm above the drain area and were the base for future MemFlash devices. Because the electrical charging and discharging of the MemFlash floating gate was achieved by thinning the gate oxide within the tunnelling window, it was crucial to determine the thickness of the thinned oxide and its voltage dependent behaviour.

5.1.1 Device Characterisation

All devices fabricated in this work are variations of MOSFET structures. The basic operation of an ideal MOSFET was described in chapter 2.1.2. The output and transfer characteristics of MOSFET devices fabricated during this work is shown in Fig. 5.1. They are in good agreement with the theoretically proposed behaviour of an ideal MOSFET. From these characteristics the threshold voltage of the fabricated MOSFETs can be deduced to be $V_{\mathrm{Th}} = 1.9$ V. Additionally, the process transconductance of the device was determined to be 120 $\mu A/V^2$, the subthreshold leakage current as $I_{\mathrm{sub}} \approx 200$ pA and the subthreshold swing as $S_{\mathrm{t}} = 400$ mV/dec. Based upon the recorded characteristics it can be assumed that the MOSFETs fabricated in this work are functional. The deduced parameters are within the normal range for devices with larger channel dimensions [116]. Therefore, any device created on the basis of these MOSFETs can be compared with other field-effect transistor based devices.

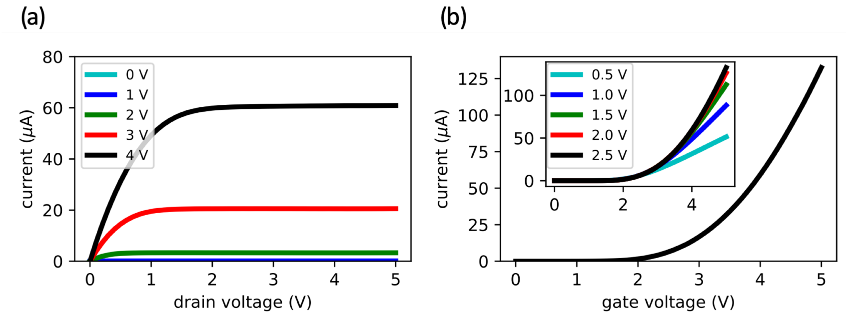


Figure 5.1 Characterising current-voltage curves of a representative MOSFET fabricated in this work. The output characteristics are presented on the left for gate voltages from 0 to 4 V. Additionally, in the right graph the transfer characteristics for a drain voltage of 2.5 V are shown. The inset shows the transfer characteristics for further drain voltages of 0.5 to 2.5 V.

The output curves of a standard MOSFET device can be seen in Fig. 5.1 (a). Since the current increase in the sub-saturation region and the constant current behaviour in the saturation region are most clearly visible in this voltage range, the characteristics were recorded for gate voltages of 0 to 4 V and in a drain voltage range of 0 to 5 V. It can be seen that an increase in gate voltage leads to a higher saturation current and a higher saturation voltage. As suggested by equation 2.8, the saturation current is not dependent upon V_{DS} after the channel pinch-off. This effect is shown here as well with the constant current beyond this point. Additionally, the spacing between the output curves suggests a constant mobility behaviour of the devices [29]. In Fig. 5.1 (b) the transfer curve for V_{DS} = 2.5 V is displayed. From this graph a threshold voltage of about 1.9 V can be determined. In addition, the inset shows the transfer characteristics of the device for further drain voltages. From this inset it can be seen that the transfer curves migrate towards a maximum (beyond pinch-off) at which there is no more change in the trajectory for higher drain voltages. To ensure functionality, these measurements were performed (when possible) for all devices fabricated during this work.

Furthermore, an investigation of the influences of channel size variation was done. From equation 2.6 it can be seen that the relation of channel width and length has a multiplicative effect on the channel current. Every chip had a total of 69 transistors with 10 different channel dimensions on it.

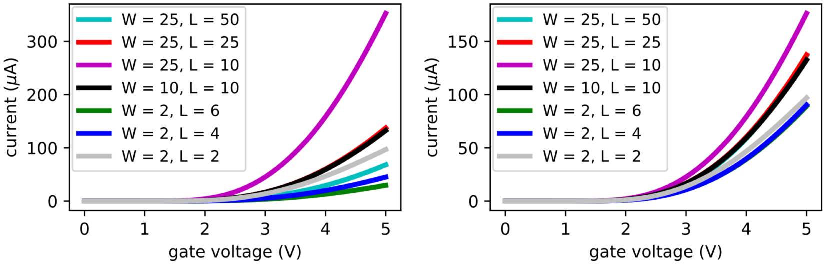


Figure 5.2 Transfer characteristics of several MOSFETs with varying channel dimensions recorded at drain voltages of 2.5 V is shown in the left graph. In the right graph the normalised transfer characteristics for the same MOSFETs are displayed.

As is visible in Fig. 5.2, 7 different channel dimensions were compared. The left graph shows the recorded transfer curves for the given channel widths and lengths. It can be seen, that the transistor with W/L = 2.5 (magenta) shows the highest current answer to the applied voltages. In accordance with this, the transistor with W/L = 1/3 (green) shows the lowest current answer. In this respect, the channel size variations result in the expected behaviour. However, the right graph of Fig. 5.2 shows the transfer curves after normalization (W/L = 1 for all transistor sizes). For ideal transistors, this normalization should result in all curves showing the same trajectory. However, three different trajectory groups were observed. Transistors with equal channel width tend to show similar behaviour. According to the Fraunhofer Institute in Itzehoe, where the semiconductor bases for the transistors were fabricated, the lithography process was optimised for the transistor with a channel width of 10 µm and a channel length of 10 µm (black) and amended for all other dimensions. This may result in a deviation from the stated sizes and explain the differences in channel current. However, even though these deviations are noticeable, they can be neglected because the general operation of all transistors is not affected.

5.1.2 Tunnelling Oxide Thickness Analysis

The initial oxide thickness above the drain region is 30 nm for all transistors. With the method described in chapter 3.3.1 the oxide was reduced within a 2 x 2 µm window. The determination of oxide thicknesses within these tunnelling windows of the fabricated devices was done by current-voltage measurements and mathematically confirmed. With the fabricated MOSFET devices (see Fig. 3.6) the current through the oxide could be recorded in respect to the voltage directly applied across the tunnelling barrier. The measurements of the different oxide thicknesses were done with the method and setup described in chapter 4.1.2. An exemplary measurement is shown in Fig. 5.3.

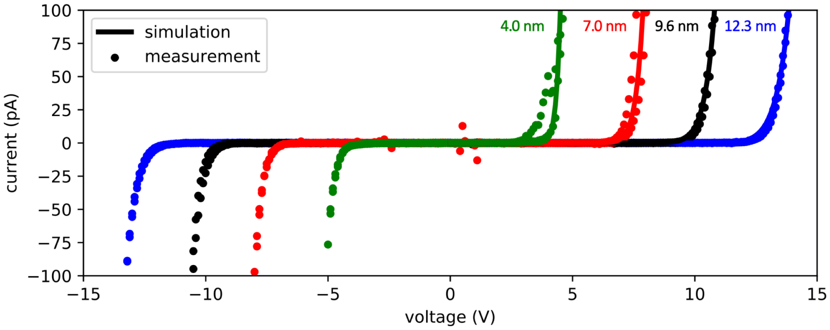


Figure 5.3 Fowler-Nordheim tunnelling currents recorded across a variation of oxide thicknesses. The solid lines show the corresponding calculated Fowler-Nordheim tunnelling currents, from which the thicknesses of the oxides were determined.

The measurements follow the exponential behaviour expected from Fowler-Nordheim tunnelling processes. Depending on the thickness of the oxide a greater voltage had to be applied. With the calculated results of equation 5.1 being in good agreement with the measurements, it can be shown that Fowler-Nordheim tunnelling seems to be the main tunnelling mechanism within the fabricated devices. Furthermore, this combination of measurements and simulation allows the determination of the oxide thicknesses.

Fig. 5.3 shows the measured values as dotted lines, with the fits displayed as solid lines. In accordance with Sze et al., equation 2.10 may be simplified as follows to determine the oxide thickness [29].

$$I_{FN} = AC_4E^2 \cdot \exp\left(\frac{-C_5}{E}\right) \tag{5.1}$$

In this equation, the area of the tunnelling window is given by A, C_4 and C_5 represent constants and E the electric field across the tunnelling barrier. For thermal oxides the constants are given at values of C_4 = 9.63 x 10^{-7} A/V^2 and C_5 = 2.77 x 10^8 V/cm [29]. The tunnelling window area for all transistors is A = 4 x 10^{-12} m^2. The oxide thickness d_{ox} can be calculated from the electric field with $E = d_{ox}/V$, where V is the voltage applied across the oxide. Using these parameters, oxide thicknesses for the given current-voltage tunnelling curves can be determined. Taking the etch rates for SiO_2 found in literature of 2.3 nm/min into account, the resulting thicknesses are in good agreement with the initial oxide thickness of 30 nm [117].

5.2 MemFlash

The investigations done here are based on the work of Riggert et al. in which the influence of varying tunnelling oxide thicknesses in MemFlash cells on the power consumption and learning behaviour are theoretically discussed [18]. This research states, that a reduction of the tunnelling oxide thickness of an EEPROM cell in a MemFlash configuration should result in reduced power consumption.

State-of-the-art memory cells work with large write and erase voltages to achieve the required long data storage times. However, high device resistance is required for memristive devices to bring power consumption of neuronal networks down to an acceptable level [118]. Furthermore, long data retention may not be needed in memristive devices. In order to study the proposed scaling effects, devices were fabricated that only vary in the thickness of the tunnelling oxide. The current-voltage sweeps for different devices are shown and characterised. The measurement method and setup described in chapter 4.1.3 were used to record the *I-V* characteristics.

Furthermore, in order to show the compatibility of the MemFlash device setup with pulse driven applications used in neuromorphic computing, pulse measurements were performed using the measurement methods and setup described in chapter 4.1.4.

5.2.1 Silicon Oxide Devices

CMOS compatible memristive devices would allow easy integration into any state-of-the-art semiconductor production process. The fabrication of memristive devices with modern silicon technology would allow low cost production, high density and high yield. Additionally, for some memristive devices the inner workings are not fully understood [73]. The MemFlash approach has the potential to combine well understood technology and devices with the advantages of neuronal computing [15]. Functional MemFlash operation was already shown for industrial SONOS cells by Himmel et al. [76]. In this work, silicon oxide based FLOTOX EEPROM cells were fabricated and driven in a MemFlash configuration.

5.2.1.1 Characterisation

The pinched hysteretic curve is an indicator of memristive operation of a device [75]. Consequently, the *I-V* loop was the first measurement conducted for any

MemFlash device in this work. The general operation of a MemFlash device is described in chapter 2.3.2.

Fig. 5.4 shows the hysteretic behaviour of two different silicon oxide MemFlash devices in a linear representation on the left and a semi-logarithmic representation on the right. Both devices have a channel width of *W* = 25 µm, a channel length of *L* = 10 µm and a 450 nm gate isolation consisting of thermally evaporated SiO. Here it is important to highlight, that both devices do not differ in structure or layer composition. However, even though both devices should behave very similarly, distinct differences are visible. Firstly, device A needs an applied voltage of about 10 V to reach a sufficient level of floating gate charge, whereas, device B needs 12 V to reach a comparable charge. Secondly, for device B a significant drop in floating gate charge is visible, indicated by the downward trajectory of the channel current for the voltage reduction towards 0 V. This effect is not seen for device A, which indicates the existence of a substantial leakage current. Considering the gate oxide and tunnelling window oxide are of industrial and therefore very good quality, it can be assumed that the SiO gate isolation is leaky. This assumption is aided further by the fact that a number of devices with a wide spread variation of SiO thicknesses was fabricated and only a small number showed the desired behaviour. Furthermore, even though increasing the thickness of the gate isolation did reduce the leakage current, no thickness of the isolation layer could be determined that would regularly result in the fabrication of functional devices. Therefore, it can be assumed that the quality of the used SiO under the conditions of deposition available is not high enough to yield reproducible results. However, even though a fabrication of CMOS compatible thin film MemFlash devices with a high yield was not achieved due to the fabrication conditions, a small number of devices could be fabricated nevertheless. These devices could not be used to investigate the initial premise, the influence of reduced tunnelling oxide thickness, since any change in behaviour could not be ascribed to the change in oxide thickness with absolute certainty. However, the fabricated devices could be used to show device behaviour when driven by pulse trains.

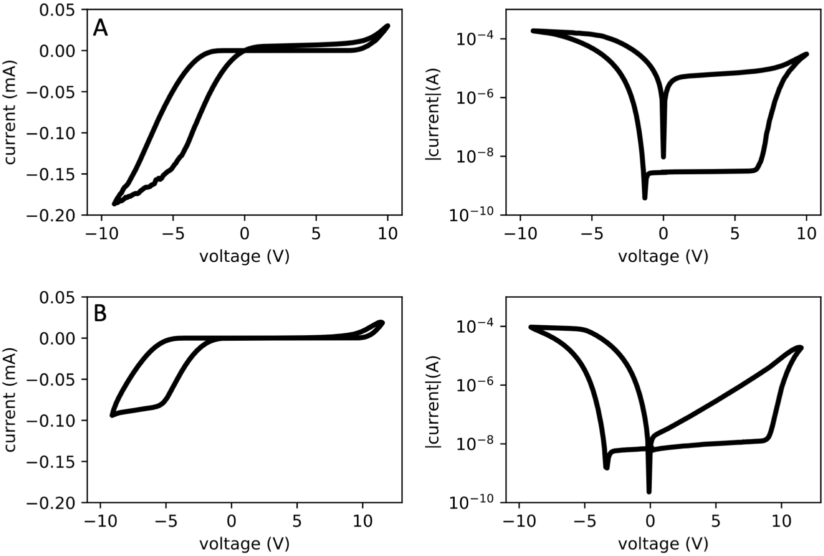


Figure 5.4 Hysteretic current-voltage characteristics of MemFlash cells comprising gate isolation of 450 nm SiO. For both devices the hysteresis are displayed on a linear scale (left) and a logarithmic scale (right) in order to highlight the electrical differences of identically fabricated silicon oxide based devices. All graphs display one cycle of the hysteresis.

5.2.1.2 Pulse Measurements

Taking the limitations of the fabricated samples into account, further investigations into the device performance were undertaken. The hysteretic functioning of an additional MemFlash device with a channel width of $W = 25$ µm, a channel length of $L = 10$ µm, an isolation between the floating and the control gate of 300 nm SiO and a 9.6 nm tunnelling window oxide thickness is shown in Fig. 5.5 (a). The hysteretic current-voltage loop is displayed on a linear and a logarithmic scale to allow further explanation of the chosen pulse train used for stimulation of the device.

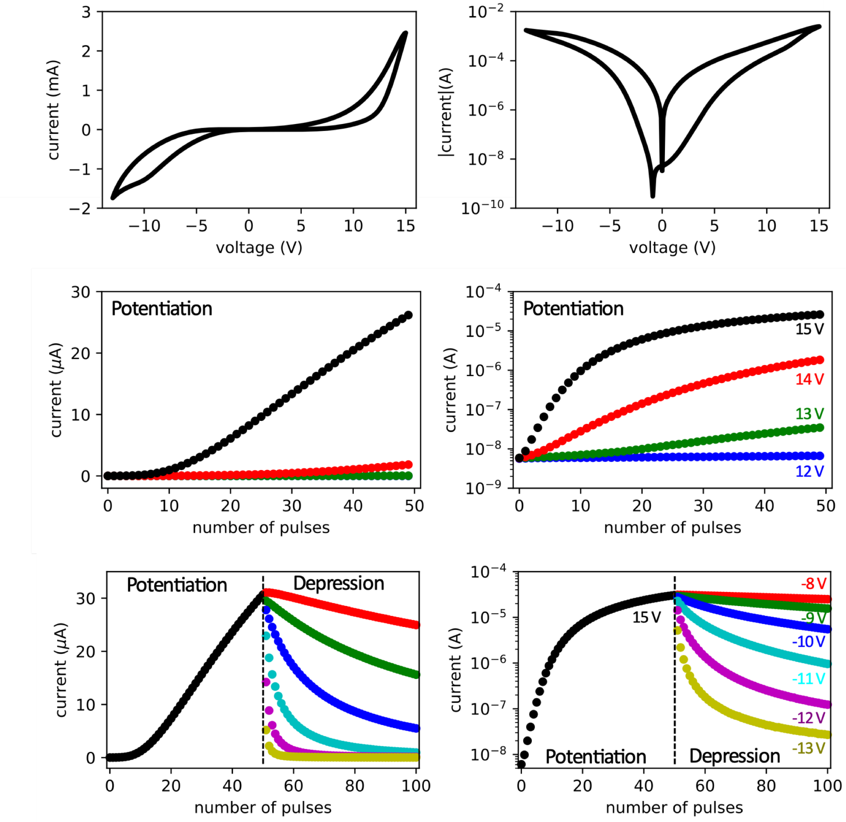


Figure 5.5 The hysteresis of a MemFlash cell comprising a 300 nm silicon oxide gate stack isolation is displayed in A. B shows the charging characteristic of the device for different magnitudes of voltage pulses. The discharging behaviour for different voltage pulse magnitudes, following the charging of the device, is shown in C. For A, B and C the measurements are displayed on a linear scale (left) and a logarithmic scale (right).

The pinched hysteresis current-voltage characteristic shown in Fig. 5.5 (a) is indicative for memristive devices. However, in comparison to the previously seen measurements (see Fig. 5.4), the device exhibits a smaller opening of the hysteresis in the positive and negative voltage regime. Furthermore, the channel current starts to increase at a significantly lower voltage. An explanation for this behaviour is given in chapter 5.2.2.1. This device shows good performance as a memristive device and is therefore used for further investigation.

In addition to the hysteretic behaviour, Fig. 5.5 (b) and (c) show the current responses to pulse stimulation of the memristive device. Synaptic plasticity, the change of the synaptic weight, is considered to play an important role in the way the brain stores information [119]. Often pulse trains are used to characterise the synaptic behaviour of memristive devices since the action potentials have similar characteristics [17]. Fig. 5.5 (b) highlights the device response to varying charging voltages, both on a linear (left) and a logarithmic (right) scale. Especially the logarithmic representation shows the differences between the applied voltages. Different pulse trains with charge voltages from 12 V to 15 V were applied to show the device behaviour for varying potentiation signal strength. From the logarithmic display of the current-voltage curve (see Fig. 5.5 (a)), the magnitude of the read voltage pulse was determined to be V_{read} = 1 V. At this voltage, an applied read pulse does not affect the floating gate charge and therefore the status of the device noticeably. This threshold effect may be considered beneficial for practical applications, since it allows an non-influential reading of the device status [120]. Furthermore, at this value the opening of the hysteresis is at a maximum and thus the difference between a charged and an uncharged status is maximised. The shapes of the applied pulse trains used to show the potentiation and depression behaviour of the MemFlash cell are shown in Fig. 5.6. A charge voltage pulse of V_{charge} = 12 V does not have any visible effect on the floating gate charge and therefore the channel current. However, increasing V_{charge} above 12 V results in an increasing current response of the device. In addition, a saturation effect can be noticed. For this reason, the number of charge pulses was set to be 50 for all further measurements. The charge voltages of 12 V and more are considered large for memristive devices, however, they are in the normal range for EEPROM memory. However, these measurements showed the need for a reduction of the power consumption for EEPROM based MemFlash devices.

In Fig. 5.5 (c) the behaviour of a charged device presented with a variation of discharging voltage pulses is presented. Again, this is shown on a linear (left) and a logarithmic (right) scale. For this, the device was charged using 50 charge pulses of 15 V magnitude. Following this, a variation of depression pulse trains was applied, ranging from -8 V to -13 V. As expected, greater discharge voltage pulses lead to a weaker current response after 50 pulses and to a stronger initial discharging of the floating gate. Whereas for a discharge voltage of -10 V a gradual decrease in the current is noticeable, a strong initial depreciation is visible for -13 V. Again, a saturation can be seen which is due to the decrease in floating gate charge and therefore reduces the potential difference between the drain and the floating gate. For a fully charged floating gate the potential difference across the tunnelling oxide is greater than for an uncharged or lower charged floating gate, when a discharge pulse is applied at the drain. Furthermore, since the current answer changes depending on the charge history of the device, the increase in channel current may be viewed as a decrease of the device resistance. Compared to other memristive devices, the device shows the expected behaviour under the application of invariant pulses [120]–[123].

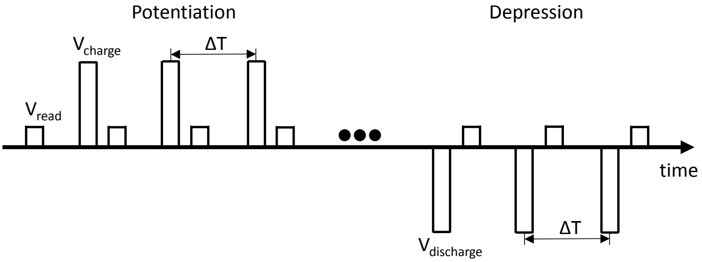


Figure 5.6 A schematic view of the pulse train used for the charging and discharging of the memristive devices created in this work. The V_{charge} pulses are used in the potentiation of the device, whereas $V_{\text{discharge}}$ pulses were used for depression. The device status was determined by applying V_{read} pulses. In order to characterise the devices, the potentiation and depression pulses could be applied with varying magnitudes and duration. Furthermore, the time between pulses ΔT could be adjusted.

In order to charge and discharge the device, while at the same time continuously reading the state of the floating gate charge through the channel current, the pulse train in Fig. 5.6 was used. The first read pulse was applied to record the initial state of the device and had the same magnitude as all read pulses at V_{read} = 1 V. The charging cycle consists of 50 positive charge pulses V_{charge}, each followed by a read pulse to record the changes in device status. The discharge cycle also consists of 50 pulses with a negative voltage $V_{\mathrm{discharge}}$ in order to reduce the positive charges on the floating gate and bring the device back to its initial status. Each discharge pulse is followed by a read pulse.

5.2.2 Polymer Devices

The polymer MemFlash devices are the result of a number of different approaches and the gradual improvement of the SiO devices discussed in the previous chapter. In an initial approach to the subject two aspects seemed of great importance for proper functionality: charging and retention. Charging refers to the charging of the floating gate by applying a positive voltage at the drain and have electrons tunnel through the tunnelling oxide of the floating gate, therefore charging it positively. Similarly, the opposite effect of discharging was investigated as well. Furthermore, retention is the time it takes for the charges on the floating gate to dissipate without external stimuli applied.

The addition of a control gate and gate isolation to a standard MOSFET results in the capacitive structure shown in Fig. 2.9 (b). In comparison to the direct effect of an applied voltage and the resulting FN-tunnelling current measured in chapter 5.1.2, this capacitive structure influences the voltage distribution inside the device. A voltage applied between the drain and the control gate does not solely fall off at the tunnelling barrier. Due to the capacitive voltage divider, only part of this voltage falls off across the tunnelling oxide. Accordingly, coupling coefficients for the amount of external voltage falling off across the tunnelling oxide are introduced [124], [125].

$$k_{charge} = \frac{C_{FG}}{C_{FG} + C_{FB} + C_{FD}} \tag{5.2}$$

$$k_{discharge} = \frac{C_{FD}}{C_{FG} + C_{FB} + C_{FD}} \tag{5.3}$$

The equations 5.2 and 5.3 describe the coupling coefficients for the charging and discharging of the floating gate, respectively. To reduce the needed voltages and therefore reduce power consumption of the device, the coupling coefficient should be as large as possible. Consequently, the capacitance between the floating and the control gate C_{FG} should be large. Moreover, keeping the tunnelling barrier thickness and the areas of all capacities constant for all devices, the thickness d_{FG} defines the magnitude of C_{FG} and therefore, directly influences the coupling coefficients. In accordance with the equation for a standard parallel-plate capacitor, d_{FG} should be kept small to increase the capacitance (see equation 2.1).

In order to further investigate the effect the size of the capacitance C_{FG} has on device performance, a MOSFET with a tunnelling oxide thickness of 9 nm was fabricated and driven with an external capacitor at the gate. The schematic cross-sectional view of the device with the used external wiring scheme is shown in Fig. 5.7 (a). Here the floating gate is not electrically floating, however it is nonetheless named floating gate to allow comparison to the capacitance structure within a thin film cell (see Fig. 2.9 (b)).

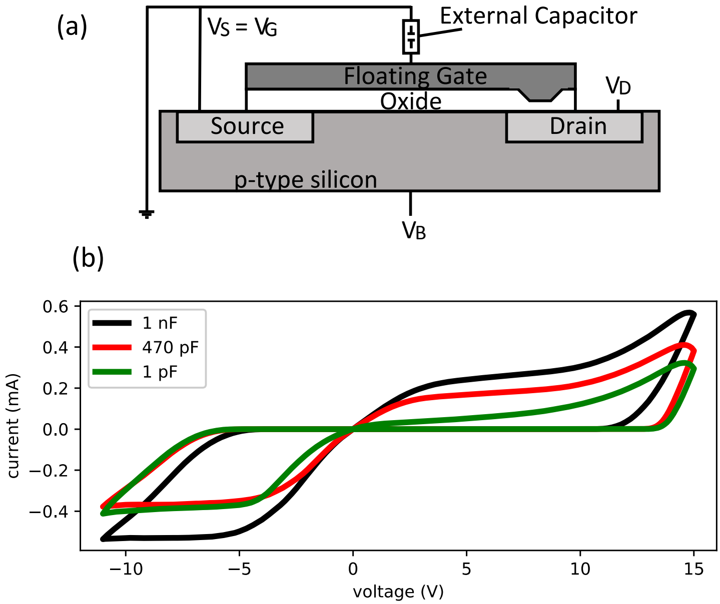


Figure 5.7 Schematic cross-sectional view of a MOSFET with a tunnelling window above the drain region. The external capacitor in combination with the MemFlash wiring scheme allows memristive behaviour. The hysteretic current-voltage characterisations for external capacitors of different sizes are shown in the graph below. The MOSFET used for these measurements had a channel width of W = 10 µm and a channel length of L = 10 µm.

The external capacitor allows a detailed analysis of different capacitor sizes in the gate stack. Any effect seen is solely based upon a difference in capacitance since the MOSFET is the same for all measurements. Three different capacitor sizes were used for these measurements: 1 nF, 470 pF and 1 pF. All capacitors were store bought and the capacitances were confirmed using an LCR-meter. The recorded hysteresis curves are displayed in Fig. 5.7 (b). A reduction in capacitance leads to a lower current answer and therefore a smaller hysteresis opening. Additionally, the rise in channel current sets in later for smaller capacitances. This is in accordance with equation 5.2, as a reduced C_{FG} would lead to a smaller coupling coefficient and therefore a larger external voltage is needed to achieve the same voltage drop across the tunnelling oxide. However, with the capacitor size being reduced by three orders of magnitude the resulting change in performance is relatively small. Therefore, even though these measurements reinforce the influence of the top capacitance on the device performance, they similarly show that an optimisation of the coupling coefficient alone does not by itself result in a working device. Instead, the ability to hold charges on the floating gate seems to be the main factor for a working device. Henceforth, the retention of the devices with external capacitances was investigated. Even though they showed hysteretic behaviour, they showed a retention of only a few seconds. Due to the fact that the floating gate was not isolated and thus not electrically floating, charges from the surrounding atmosphere may have been attracted and neutralised the stored charge. However, from these measurements, the importance of a reduced leakage current through the gate isolation between the floating and control gate was deduced. Calculations show that a leakage current of as low as a few fA could result in a neutralisation of the required floating gate charge.

With different thin film options being insufficient in providing the low leakage currents within the gate stack needed for device operation (see chapter 5.2.1.1), a polymer isolator was chosen. The leakage currents were measured with capacitor structures by application of a voltage across the capacitor and measuring the current response.

The current response of a parallel-plate capacitor with a Al bottom electrode, a 6µm thick AZ nLOF 2070 polymer [115] insulator and a Ti top electrode is shown in Fig. 5.8. The measurement was conducted at two different speeds. The first was a fast measurement with a step width of 250 mV and medium integration time (integration over 16 recorded values) for every recorded data point. This measurement resulted in a hysteretic current-voltage loop which indicates a well-insulated capacitor. The current response measured was a displacement current from the charging of the capacitor. Consequently, by setting a step width of 10 mV and using a long integration time (integration over 256 recorded values) the hysteresis disappeared. Due to the resolution of the SMU, no final value for the leakage currents within the polymer could be determined. However, any capacitor structures comprising a thin film, such as silicon oxide, showed significant leakage currents in the same range of applied voltage.

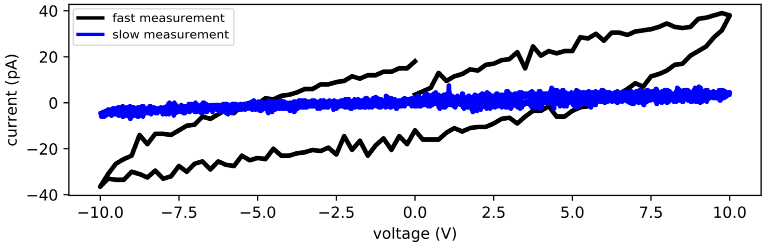


Figure 5.8 Leakage current measurements for a parallel plate capacitor structure comprising an Al bottom electrode, a Ti top electrode and 6 µm polymer isolation. Depending on the set size and integration time of the measurement, a hysteresis forms (black). Increasing the measurement duration decreases the opening of the hysteresis (blue), which suggests the currents recorded are displacement currents due to the charging of the capacitor structure, not leakage currents.

Ultimately, the leakage current through the gate isolator is the critical factor when creating a working MemFlash device based on this technology. With this knowledge is was possible to create a number of memory cells and assess their performance as MemFlash devices. In the following a variety of MemFlash devices will be presented, their structural differences highlighted and the influences of said differences evaluated. Furthermore, the impact of changing working conditions like a change in applied charge and discharge voltages or frequency was studied. Finally, the performance of the memristive devices when driven by voltage pulses was examined.

5.2.2.1 Characterisation

The polymer MemFlash devices created in this work were used to examine the influence a change in tunnelling oxide thickness has on the device performance in different aspects. The devices are all based on MOSFETs with a channel width of W = 10 µm and a channel length of L = 10 µm. One of the main concerns with the MemFlash approach to memristive devices is the comparatively high power consumption of the devices. However, due to the high scaling possibility of the underlying memory devices, this concern could be addressed through a general size reduction and power consumption reduced to the level of other state-of-the-art memristive devices. Additionally to the overall downscaling of the transistor, a reduction of the tunnelling oxide thickness of the devices could result in a decrease of power necessary for the operation of MemFlash devices [18]. First, the hysteretic behaviour of the devices is shown in Fig 5.9. In addition to the measurement results presented in this work, simulations were performed using the models of Ziegler et al. [57][15] and Riggert et al. [18]. The simulations are in good agreement with the measured data and support the conclusions drawn. The results of the simulations and a comparison to measurement data can be found in [19].

The hysteretic behaviour of the MemFlash devices with tunnelling oxide thicknesses of 7.4 nm, 6.4 nm and 4.0 nm is shown in Fig. 5.9. Both, the 7.4 nm and the 6.4 nm devices require charge voltages of 15 V, whereas the 4.0 nm device only requires 9 V to charge the floating gate. This shows a reduction in voltages needed to drive this memristive device can be achieved by reducing the tunnelling oxide thickness. Additionally, comparing the resistance ratios at a voltage of 1 V shows a reduction from $R_{\mathrm{off}}/R_{\mathrm{on}} = 3.3 \times 10^4$ (6.4 nm) to $R_{\mathrm{off}}/R_{\mathrm{on}} = 4.3 \times 10^3$ (4.0 nm). This reduction was expected, since the maximum current for the thin oxide device is lower. However, even though the reduction of the tunnelling oxide thickness reduces the channel current, the 4.0 nm device still shows satisfactory memristive behaviour. Lastly, the charging trajectories for the curves differ greatly. The devices with thicker tunnelling oxide (7.4 nm and 6.4 nm) show a rise in current at as little as 2 V. In comparison, the thin tunnelling oxide device (4.0 nm) shows a rise in the channel current at about 6 V. This effect may be caused by charges remaining on the floating gate, even after applying a sufficient discharging voltage.

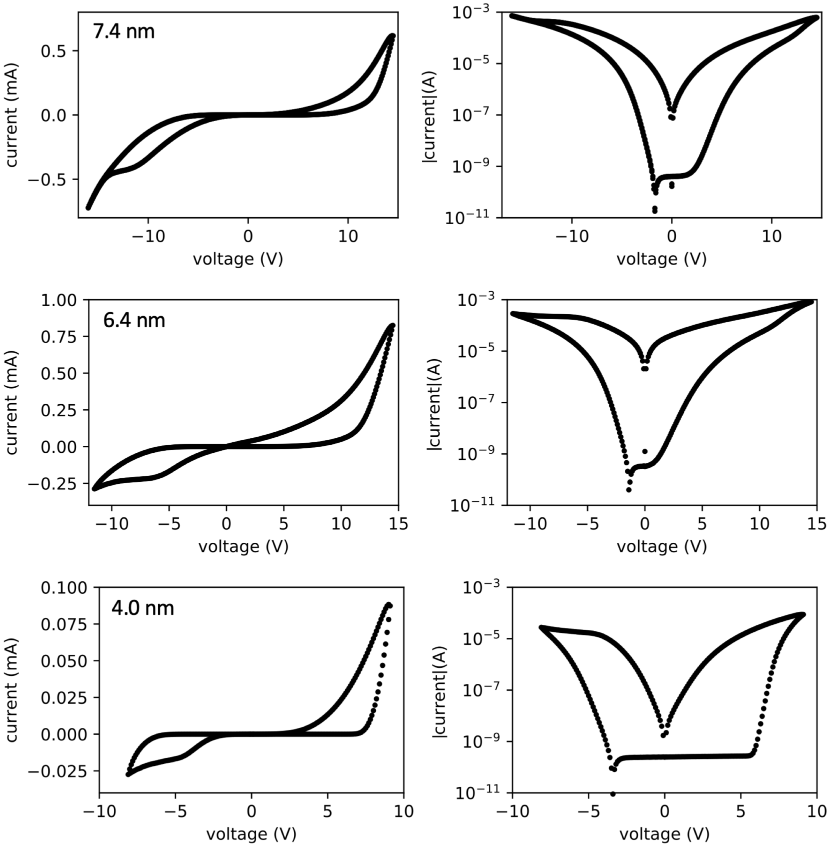


Figure 5.9 The characteristic current-voltage curves for the memristive devices comprising polymer gate isolation fabricated in this work are shown. l devices were fabricated identically with only the thickness of the tunnelling oxide varied. The resulting devices had oxide thicknesses of 7.4 nm, 6.4 nm and 4 nm. Additionally, on the right, the hysteretic behaviour of all devices is shown on a logarithmic scale.

When looking at the 7.4 nm device in Fig. 5.9, the opening of the hysteresis narrows with increasing negative voltage. Beyond -14 V no apparent opening is visible. This suggests, that the floating gate is fully discharged, since any difference in current answer is linked to charges remaining on the floating gate. However, the following charging (positive voltage) trajectory of the hysteresis suggests an increased conductance of the channel. In comparison, the 4.0 nm device does not experience the same behaviour. Considering the reduced tunnelling oxide thickness, lower voltage differences across the oxide are needed to move electrons onto and off the floating gate. Additionally, for devices with lower tunnelling oxide thicknesses, charges dissipate from the floating gate without any external influences at a higher rate, compared to devices with thicker oxides.

Due to the previously described forming process, the initial measurement of a MemFlash device differs from following current-voltage measurements. In a number of memristive devices, an electroforming process is used to cause initial structural changes to the electrolyte and aid future switching [73], [126]. Yet, within the MemFlash cell no structural changes occur during the first operation of the device. However, when looking at the charging and discharging process of the floating gate, the Fowler-Nordheim tunnelling current depends on the potential difference between the floating gate and the drain region and the tunnelling oxide thickness. If the floating gate is fully charged the potential difference to a negative voltage applied at the drain is large. The floating gate discharges to a minimum at which the potential difference is no longer able to move electrons through the tunnelling oxide. Therefore, the floating gate remains at this level of charge and influences any future current-voltage measurements. However, as stated previously, the effect depends on a number of factors, one being the tunnelling oxide thickness of the floating gate device. For this reason, the effect is not seen for MemFlash devices with thin tunnelling oxides. The effect the forming process can have on the hysteresis of a MemFlash cell is highlighted in Fig. 5.10.

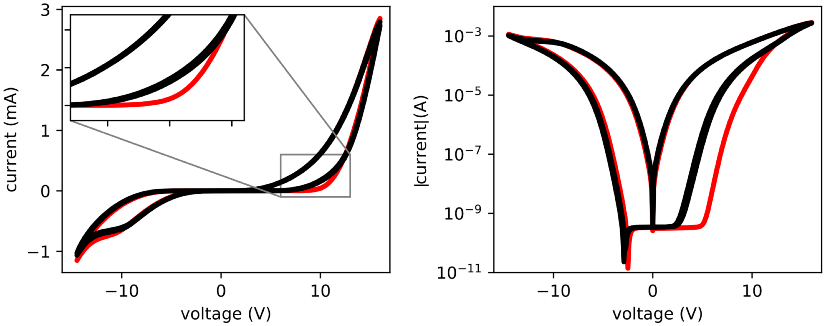


Figure 5.10 The forming process of the fabricated MemFlash cells is shown in the difference between the initial measurement (red) of a device and the following cycles (black). To highlight the full extent of the forming process and its influence on the electrical behaviour, the measurements are displayed on a logarithmic scale on the right.

The forming process mainly effects the charging of the device. Looking at the linear representation (left) of the initial (red) and the following measurement cycles (black), one can see a small decrease in the hysteresis opening. This change is highlighted in the inset. Moreover, comparing the trajectories in the logarithmic representation (right) shows the full extent of the forming process. The opening of the hysteresis is reduced, as well as the voltage needed (from 5 V to 2.5 V) for the channel current to increase. However, even though the forming process results in a significant reduction of the hysteresis opening, this does not affect the low voltage regime of the hysteresis. Additionally, the forming effect lessens for reduced tunnelling oxide thicknesses as these devices are less capable of holding charges on the floating gate. Therefore, after initial forming, meaningful measurements can still be performed using the fabricated devices.

5.2.2.2 Voltage Dependent Behaviour

All hysteresis curves presented until now show memristive behaviour of the MemFlash devices for optimised operational voltages. Here, optimised refers to the voltages at which the floating gate is charged as much as possible (and for negative voltages discharged respectively) without the internal field exceeding the breakdown point of the isolation or oxide. The optimal voltage regimes were derived from measurements where the swept voltage range was increased gradually until the hysteresis showed signs of saturation, such as a narrowing of the hysteresis opening at higher voltages. Ultimately any memristive device is required to work outside this optimal voltage range, therefore at lower voltages. In this chapter, device behaviour for voltages below the maximum charge and discharge voltages is investigated.

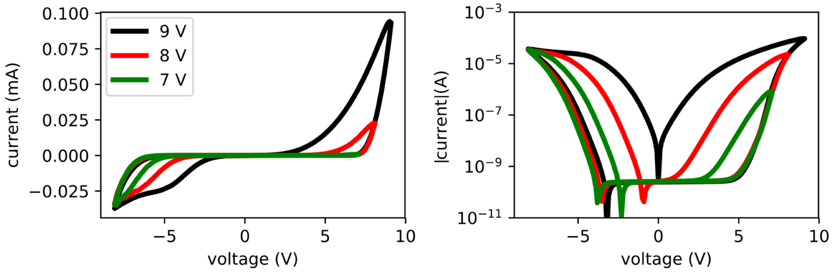


Figure 5.11 The influence of varied positive voltage ranges on the shape of the hysteretic current-voltage curve of a MemFlash device, displayed on a linear scale (left) and a logarithmic scale (right). The applied voltage ranges were varied from -8 V to 7 V, 8 V and 9 V.

Fig. 5.11 shows the linear (left) and logarithmic (right) representation of a change in the charge voltage for a MemFlash device with a thin tunnelling oxide (4.0 nm). The discharging voltage is kept at the optimal magnitude of $V_{\mathrm{discharge}}$ = -8 V for all measurements. This value was determined from the measurements conducted before (see Fig. 5.9). When the charging voltage is reduced, a narrowing of the hysteresis opening can be observed. Additionally, even though the linear representation does not show any hysteretic opening for the positive loop of the V_{charge} = 7 V (green) measurement, the opening is clearly visible in the right graph. This shows memristive behaviour of MemFlash devices is possible even when operated at less than ideal conditions. However, for every MemFlash device a certain voltage cannot be undercut for the device to show memristive behaviour. If the charge voltage falls below this value, no charge can be stored on the floating gate and no hysteresis will form, because the potential difference across the tunnelling oxide is less than required for electrons to tunnel onto the floating gate. This feature may be useful for future application, since reading the status of a device is an action that does preferably not affect its status.

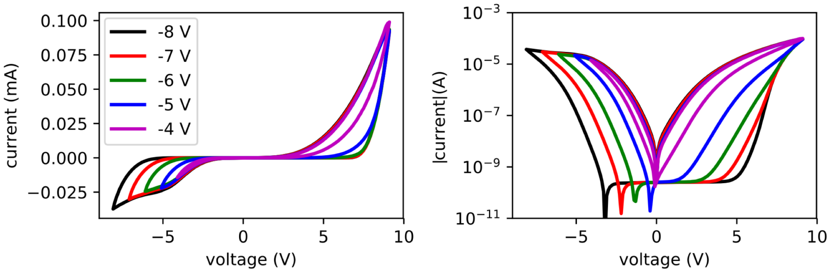


Figure 5.12 The influence of varied negative voltage ranges on the shape of the hysteretic current-voltage curve of a MemFlash device, displayed on a linear scale (left) and a logarithmic scale (right). The applied voltage ranges were varied from -4 V, -5 V, -6 V, -7 B and -8 V to 9 V.

Similarly, a change in discharge voltages was investigated and the resulting measurements are displayed in Fig. 5.12. Again, the charging voltage was kept at the optimal magnitude of V_{charge} = 9 V for all measurements. In accordance with the previous voltage measurements, a narrowing of the hysteresis opening was observed for reduced discharge voltages. However, due to the reduced discharging of the floating gate, the opening narrowed towards the low resistive trajectory.

Altogether, the voltage dependent measurements were performed for all MemFlash devices with varying tunnelling oxide thicknesses (4.0 nm, 6.4 nm and 7.4 nm). Since the general behaviour is comparable for all devices, the results are shown for the 4.0 nm MemFlash device representatively. Furthermore, the measurements show that MemFlash devices can be used as analogue memristive devices as they change their synaptic weight gradually in response to the applied voltage. However, charge voltages have to be kept in a certain regime in order to allow memristive behaviour and to not destroy the devices. One operational disadvantage of a “true” memristor is that every use alters its status [70]. When the human brain recalls information, it is legitimate to think of the synaptic weight changing during the process. However, for a number of computational applications, such as reading the information stored in the memory, reading the device status without any alteration is needed. The threshold demonstrated here allows reading the status of the memristive devices without altering the stored information.

5.2.2.3 Frequency Dependent Behaviour

Previously, the influence of charge and discharge voltage variation has been investigated. In addition to changing the voltage, adjusting the duration of the applied programming signal to a memristive device offers a further way of controlling the device resistance [126]. Therefore, the influence of the frequency of the voltage sweep applied to the MemFlash devices has been investigated. Fig. 5.13 shows the linear (left) and logarithmic (right) representation of the frequency dependent behaviour for the 4.0 nm MemFlash device. The current-voltage sweeps were performed at cycle frequencies of

3 mHz (black), 15 mHz (red) and 30 mHz (green). These frequencies were chosen because they most clearly show the behavioural changes of the current-voltage curve. Furthermore, since the behaviour of all MemFlash cells was equivalent, the results shown are representative.

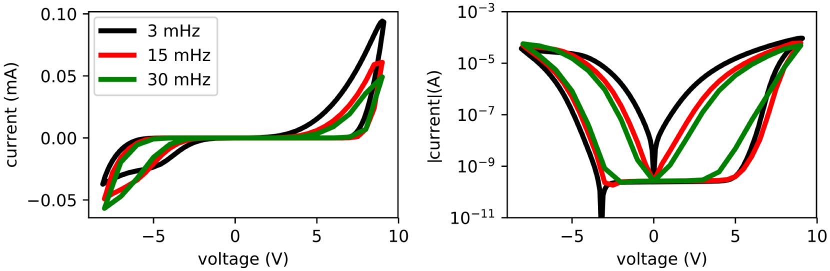


Figure 5.13 The influence of varied cycle frequencies on the shape of the hysteretic current-voltage curve of a MemFlash device, displayed on a linear scale (left) and a logarithmic scale (right). The applied sweep frequencies of 3 mHz, 15 mHz and 30 mHz are displayed.

An increase in cycle frequency results in a narrowing of the hysteresis opening. Additionally, the reduction of cycle duration leads to a decrease in the maximum current obtained in the positive voltage regime and an increase of the maximum current response in the negative voltage regime. This may be explained when taking the floating gate potential into account, which, in the positive voltage range, is higher for higher frequencies and, in the negative voltage range, is smaller when the cycle frequency is increased [19]. Since charging and discharging voltages are applied for a shorter amount of time, the number of electrons pulled off or pushed onto the floating gate, is reduced.

5.2.2.4 Pulse Measurements

Measurements to show how MemFlash devices work when they are driven by pulse trains have been discussed in chapter 5.2.1.2. In addition to this global inquiry, this chapter will focus on the influence of changing tunnelling oxide thicknesses. To do so, two devices will be compared: a MemFlash device with a 6.4 nm tunnelling oxide and a device with a 4.0 nm oxide.

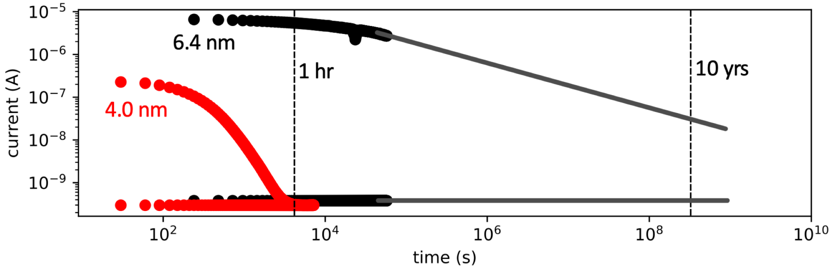


Figure 5.14 Investigation of the retention behaviour of MemFlash devices with different tunnelling oxide thicknesses of 4 nm (red) and 6.4 nm (black). Both devices were charged until a saturation of the floating gate charge could be seen. After this point only read pulses of V_{read} = 1 V were applied to determine the state of the devices. The solid grey lines are a linear extrapolation of the retention behaviour of the 6.4 nm device. (adapted from [19])

First, the impact of a reduction in tunnelling oxide thickness on the retention behaviour of the devices was investigated. The results of this comparison are shown in Fig. 5.14, with the 6.4 nm device represented in black and the 4.0 nm device in red. In order to measure the rate at which charge dissipates from the floating gate, the devices were charged and the current response read by the application of a voltage pulse V_{read} = 1 V. With this method the floating gate charge was influenced as little as possible while still getting frequent information about the charge level. From Fig. 5.14 the differences in retention are clearly visible, with the 4.0 nm device having lost all its initial charge after an hour. The 6.4 nm device, however, did only see a small drop in the current answer for the full measurement duration (about 16 hours). The grey lines show linear extrapolations of the expected development in the charge level. This shows that the fabricated devices do not meet industrial standards, but demonstrate a sufficient retention to allow meaningful research.

The use of memristive devices in neuronal computation architecture relies on the ability of the device to reliably work when driven by pulse trains. For MemFlash cells to be considered as possible synapses in neuronal networks they need to respond to the basic neuronal principles. For instance, the communication between neurons is achieved by spikes which, dependent on their frequency, change the synaptic weight of the synapse between the neurons [127], [128]. Therefore, memristive devices need to show a resistance change in relation to the applied pulse trains in order to work as an artificial synapse. Furthermore, using a spike based protocol would reduce the systems power consumption.

The permanent reduction in resistance of the memristive device can be considered to be the equivalent of long-term potentiation (LTP). LTP refers to an increase in the synaptic strength that persists over the duration of a few hours [129]. That being said, a mechanism that increases synaptic strength should not stand alone, as this could only lead to an eventual saturation of all synapses [130]. Therefore, the reverse effect, a reduction in the synaptic strength is called long-term depression (LTD). LTD shows itself as a permanent increase in the resistance of the memristive device. Comparatively, the change in current corresponding to potentiation and depression in the MemFlash devices is shown in Fig. 5.15.

The pulse train applied can be split into two sections: charging (potentiation) and discharging (depression). In Fig. 5.15 the charging of both devices is shown in the left graphs. Here the magnitude of the charge pulses was varied with the read pulse magnitude and the pulse intervals staying constant at V_{read} = 1 V and ΔT = 1 s, respectively. The general shape of the pulse train is shown in Fig. 5.6, displaying potentiation and depression differences. For the MemFlash device with a tunnelling oxide thickness of 6.4 nm the charging voltage was varied from 11 V to 14 V and for the 4.0 nm device from 7 V to 9 V. For both devices an increase in V_{charge} results in a larger maximum current reached after potentiation. Additionally, it leads to a faster charging of the floating gate which is reflected in a steeper increase in current response. Putting this in relation, the Memflash devices both show the expected behaviour with a decrease in device resistance for increased voltage magnitudes and pulse train duration.

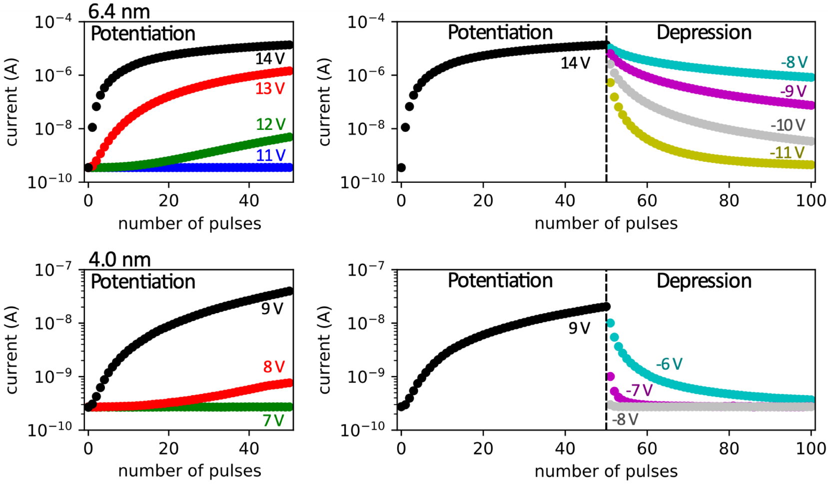


Figure 5.15 Comparison of the potentiation and depression behaviour of MemFlash devices with different tunnelling oxide thicknesses of 6.4 nm and 4 nm. The left graphs show the potentiation behaviour of the device for different charge pulse magnitudes. The right graphs show the depression behaviour of the devices for different discharge pulse magnitudes. In order to investigate the depression behaviour, the devices were charged with 50 positive voltage pulses before the depression measurements.

Furthermore, depression behaviour of the devices was investigated. The devices were charged using 9 V (4.0 nm) and 14 V (6.4 nm) charging pulses before applying a variety of discharge magnitudes. The 4.0 nm device was discharged using -6 V to -8 V voltage pulse magnitudes, whereas voltages from -8 V to -11 V were applied to the 6.4 nm device. Again, the pulse distances were kept constant at ΔT = 1 s and the read voltages at V_{read} = 1 V. The conductance decreases for both devices with every depression pulse applied. Further, a greater negative pulse magnitude leads to a lower final current response and a faster drop in the initial current. Altogether, both devices show the expected behaviour desired from artificial synapses [131]–[134]. Furthermore, the measurements conducted show the influence of a reduced tunnelling oxide thickness for charging and discharging of the floating gate. In consequence, this effect on the charging and discharging dynamics allows the implementation of a learning behaviour in MemFlash cells by the precise adjustment of the oxide thickness. With state-of-the-art silicon technology this precise adjustment is possible and results in a simple way to implement learning schemes within neuromorphic circuits [19].

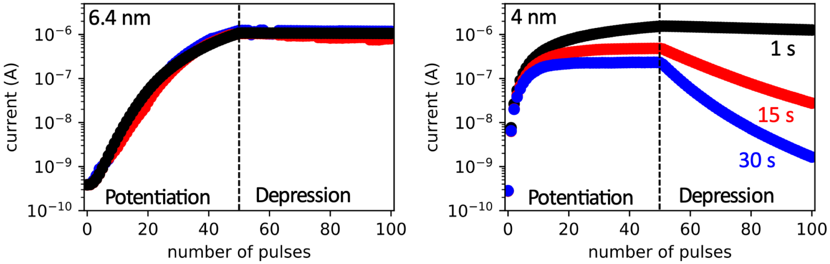


Figure 5.16 The influence of increasing time intervals between charging and discharging pulses for MemFlash devices with different tunnelling oxide thicknesses of 6.4 nm and 4 nm. The times between the pulses were changed from 1 s to 15 s and 30 s, in order to investigate the influence of retention on potentiation and depression in pulse driven memristive devices.

Moreover, with the 6.4 nm device holding charges for long periods of time, it can be assumed that the change in potentiation may be referred to as LTP. However, for the 4.0 nm device the charges on the floating gate dissipate within a much shorter period of time. With the much shorter timescale, this effect could be regarded as short-term potentiation (STP) [135]. The difference of STP and LTP is shown for two different MemFlash devices in Fig. 5.16.

In order to show the effect of the tunnelling oxide thickness on the charge storage more clearly, a frequency variation was included in the pulse train. While charging the devices with voltage pulses of unchanging magnitudes (V_{charge} = 10 V for the 4.0 nm device and V_{charge} = 14 V for the 6.4 nm device), the frequency at which pulses were applied was varied from ΔT = 1 s (black) to ΔT = 15 s (red) and ΔT = 30 s (blue). This showed, that the change in frequency does not affect the potentiation of the 6.4 nm device, but leads to a difference in the floating gate charge of the 4.0 nm device. A lowered pulse frequency results in a reduced maximum charge after the potentiation protocol for the thin oxide device. Additionally, after potentiation read pulses were applied at the same frequencies without any discharge pulses. In accordance with the retention measurements, the floating gate of the 4.0 nm device discharges over time, with the current response at high frequency (ΔT = 1 s) showing only a small drop after 50 read pulses and the lowest frequency (ΔT = 30 s) showing the greatest drop after the same amount of pulses. No drop in conductivity can be seen for the 6.4 nm device for either frequency. Again, this underlines the previously drawn conclusion that memory capabilities may be set by an adjustment of the tunnelling oxide thickness and could be fitted easily to the requirements of a neuromorphic system.

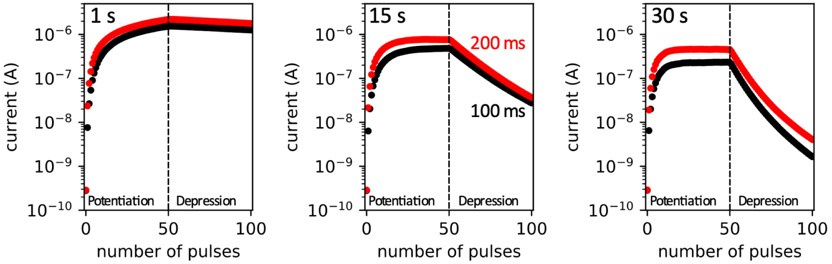


Figure 5.17 Investigation of the influence of pulse duration for a MemFlash device with a tunnelling oxide thickness of 4 nm. In addition to comparing pulse durations of 100 ms (black) and 200 ms (red), the time between pulses was changed as well. This way, retention influences in combination with pulse duration and time between the pulses could be studied.

Lastly, the influence of pulse duration in combination with the before studied effects was investigated. Fig. 5.17 shows the effects doubling the duration of potentiation pulses has on the MemFlash device with a tunnelling oxide thickness of 4.0 nm. The effects of a pulse duration change from 100 ms (black) to 200 ms (red) is depicted for different pulse distances of 1 s, 15 s and 30 s. The increase in pulse duration leads to a higher current response, regardless of pulse distance. The charge on the floating gate depends on the applied drain voltage $V_D(t)$ and the charge dissipation over time [15]. Thus, increasing the net charging time results in a higher floating gate charge at every point during potentiation, as was expected. The depression was measured in the same way as it was before, by applying read pulses at the mentioned frequencies without additionally discharging the floating gate. Here, as expected no difference showed, since the read pulse duration was not changed. The depression is solely due to charge dissipation from the floating gate over time.

In conclusion, it was shown that the magnitude of charge and discharge voltages has an effect on the resistance ratios of MemFlash devices. Likewise, the impact of changing the frequency of the applied voltage sweep was shown. These behavioural changes were found to be similar for all investigated devices and are therefore not dependent on the tunnelling oxide thickness. However, pulse measurements show a distinct dependency of device behaviour on the tunnelling oxide thickness. The charge storage ability of the device largely depends upon the thickness. Furthermore, changing charging and discharging voltage pulse magnitudes revealed the potential use of MemFlash devices as artificial synapses. In combination with frequency and pulse duration measurements, the devices showed LTP or STP behaviour, depending on the oxide thickness. These analyses show that a simple approach to implementing a basic memory scheme for MemFlash devices is possible by the simple adjustment of the tunnelling oxide thickness [19].

5.3 Piezoelectric Sensor

The piezoelectric sensor presented in this work is based upon a piezoelectric field-effect transistor (see chapter 2.4). The idea of using a piezoelectric material to detect forces is very common. However, most devices rely on a parallel plate layout, with the charge generated by an applied force directly recorded across the piezoelectric [136], [137]. These devices are often limited in respect to the range of measurable forces and their sensitivity. In order to condition a sensor output signal an amplifier is used as closely to the sensor as possible. The approach of placing the piezoelectric layer (sensing material) inside a field-effect transistor to use its internal amplification has been shown [138], [139]. However, these approaches use polymers like polyvinylidene fluoride (PVDF) as a piezoelectric layer. In this work, a CMOS compatible approach of such a device is presented comprising AlN in the gate stack. This approach would allow full processing within standard silicon technology fabrication lines, offer high scalability and the possibility of incorporating the sensor in integrated circuits.

In addition to polymer based devices, some concepts using CMOS compatible piezoelectric materials in combination with a field-effect transistor have recently been published. However, in comparison to the approach chosen in this work, the piezoelectric layers are positioned outside of the transistor [140], [141]. Thus, device scaling seems limited and the amplifying properties of the approach reduced.

For the characterisation of the proposed transistor, a two-part setup consisting of the external body to which a force is applied (silicon cantilever) and the sensing unit (piezoelectric field-effect transistor) was used. Piezoelectric field-effect transistors show a different behaviour when compared to conventional MOSFETs. Therefore, the characteristic output and transfer curves were recorded and compared to conventional MOSFETs. The investigation of the stress sensing capability was conducted with two different excitation setups. The first is described in chapter 4.2.1 and solely relies on mechanic excitation of the cantilever. The setup allowed the application of constant forces with different magnitudes for varying durations. To achieve higher precision of the excitation signals and reduce their magnitudes, the setup was extended to apply forces using magnets. The method and setup is described in chapter 4.2.2. Furthermore, the magnetic excitation setup was enhanced to handle high frequency excitation of the cantilever (see chapter 4.2.3). With this, the resonance frequency, sensitivity and limit of detection of the sensor was determined. Lastly, an approach of using the piezoelectric field-effect transistor in a neuronal force sensing setup will be presented.

5.3.1 Device Characterisation

Two different sample variations were created to show the validity of the used approach to stress sensing. The reference sample has no piezoelectric layer in the gate stack to act as control sample, as it should show no reaction to stress. The active sample comprises a piezoelectric AlN layer in the gate stack of the transistor, making it susceptible for applied stress. In order to allow columnar growth of the AlN, which is needed for the piezoelectric properties, a Pt seedlayer was also introduced underneath the AlN. This additional metallic layer within the transistors gate stack led to a change in characteristic output and transfer behaviour. The recorded output and transfer curves for a piezoelectric field-effect transistor were compared to those of an ordinary MOSFET (see Fig. 5.18). For both samples the output curves were recorded for different gate voltages and the transfer curves likewise for a variation of drain voltages.

The reference samples were fabricated alongside the sensing transistors; however, they were removed from the fabrication process after the deposition of the seedlayer. Hence, they behaved like an ordinary MOSFET with the added benefit of serving as references for all measurements. Here, they were used to demonstrate the behavioural differences caused by the altered gate stack. All samples used for the measurements presented in this and the following chapter comprise transistors with a channel width of $W = 25$ µm and a channel length of $L = 20$ µm.

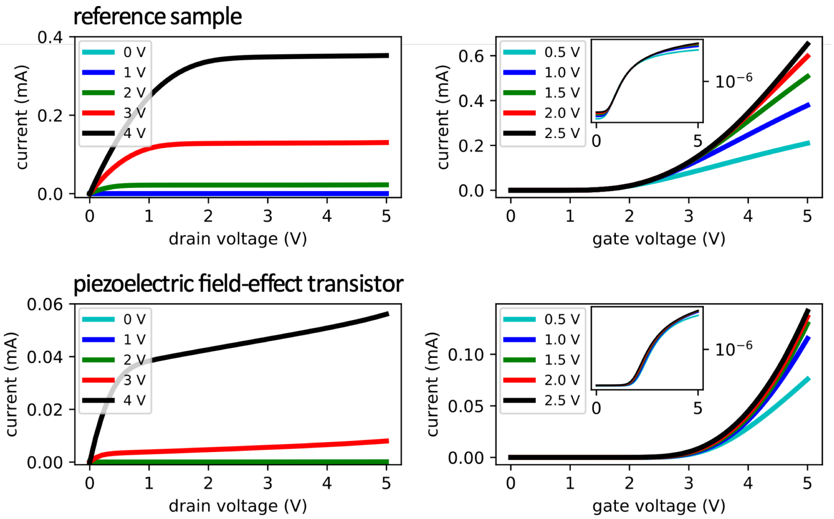


Figure 5.18 Output and transfer characteristics for a piezoelectric field-effect transistor (bottom) comprising AlN as a piezoelectric layer in the gate stack and a reference sample (top) without piezoelectric material. The output characteristics are shown for gate voltages of 0 V, 1 V, 2 V, 3 V and 4 V. The transfer characteristics are shown for drain voltages of 0.5 V, 1V, 1.5 V, 2 V and 2.5 V. The insets show the logarithmic representation of the transfer characteristics. (adapted from [28])

Fig. 5.18 shows the output and transfer characteristics of a piezoelectric FET (bottom) and a reference sample (top). The output curves of the reference sample show the trajectories expected from a MOSFET structure. In comparison, the output characteristics of the piezoelectric FET show no saturation for higher drain voltages. This was expected from this device, as its structure resembles this of an EEPROM device (see chapter 2.2.2). Additionally, the current response of the piezoelectric field-effect transistor is smaller than the channel current in the reference sample when the same external voltages are applied. Again, this behavioural change is expected since the channel is not only influenced by a single gate but a capacitive structure consisting of control and floating gate. Furthermore, when comparing the transfer characteristics of both devices a shift in the threshold voltage from 1.8 V (reference FET) to 2.8 V (piezoelectric FET) is noticeable. This shift is even more prominent when looking at the insets which show the logarithmic representation of the curves.

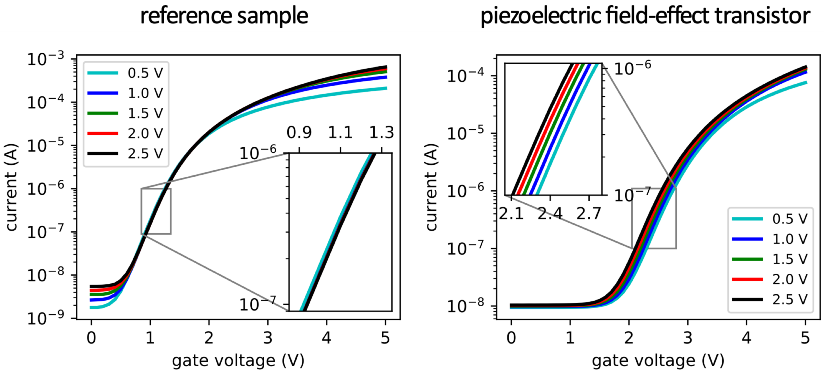


Figure 5.19 Logarithmic representation of the transfer characteristics of a reference sample (left) and a piezoelectric field-effect transistor (right). The piezoelectric field-effect transistor used AlN as a piezoelectric material in the gate stack, whereas the reference sample has no piezoelectric layer. The transfer characteristics for both devices were recorded for drain voltages of 0.5 V, 1 V, 1.5 V, 2 V and 2.5 V. The insets highlight the subthreshold swing, showing the change in gate voltage needed for the channel current to increase by one decade.

The semi-logarithmic representation is shown again in Fig. 5.19. When comparing the characteristics, the increase in threshold voltage for the PiezoFET (right) is again visible. Additionally, no great difference in the trajectories of transfer curves for different drain voltages can be seen in the reference device (left). The piezoelectric FET on the other hand, shows a spread of the transfer characteristics for the same region. These regions are highlighted within the corresponding insets. Furthermore, the subthreshold swing increases from about 400 mV/dec (reference FET) to 450 mV/dec (piezoelectric FET).

Considering the working principle of the stress sensor, the point of operation can be chosen on the basis of the transfer curves. It is reasonable to assume that the transistor is most sensitive at the point of the lowest subthreshold swing, since a change in gate voltage results in the greatest possible change of the channel current.

5.3.2 Mechanical Excitation

Following the investigation of the transistor characteristics, an examination of the full sensor setup was conducted. In order to study the sensor output signal in respect to a unidirectional force input, the setup in Fig. 4.2 was used. By extending the micrometre screw, a displacement of the cantilever tip was achieved. This displacement of the tip results in a stress across the cantilever surface. Bending the cantilever upwards leads to a compression of the top surface, where the bottom surface experiences an extension. This deformation was simulated using Agros2D, a finite element method allowing the structural analysis of the mechanical setup used in this work [142].

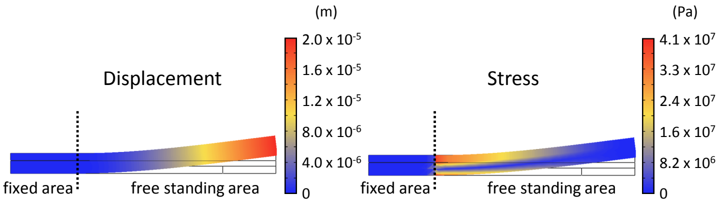


Figure 5.20 Simulation of the stress induced at the cantilever surfaces when applying a force to the tip of the cantilever. The stress generated by the deformation is displayed on the right, with the corresponding displacement shown on the left. The simulation was performed with Agros2D.

From this simulation two conclusions can be drawn with regards to the sensor operation. The first applies to the location of the piezoelectric transistor on the cantilever. In order to achieve a high stress across the AlN, it is important to position the sensing unit in close proximity to the point of clamping. The second conclusion is, that an approximation of the stress can be deduced. Hence, a tip displacement of 20 µm was simulated, which results in a von Mises stress seen on the right in Fig. 5.20 [143], [144]. The simulated magnitude of the stress experienced by the cantilever was confirmed using equations 2.18, 2.19 and 2.20, with all required values given in table 5.1.

variable	**value**
δ	20 µm
E	125 GPa [145]
b	2 mm
L	7.5 mm
h	485 µm
x	2.5 mm

Table 5.1 Geometric dimensions of the cantilever used in the finite element method simulation in order to determine the most suitable location of a piezoelectric transistor on the cantilever.

Building on these findings, a force of 330 mN was applied to both, the reference and the piezoelectric transistor samples. This force corresponds to a tip displacement of 20 µm and can be deduced using equations 2.16 and 2.17.

Fig. 5.21 shows the current responses for three different forces (330 mN, 670 mN and 1 N) applied to the tip of the cantilever. These forces correspond to tip deflections of 20 µm, 40 µm and 60 µm. Additionally, the times at which the forces are applied, as well as the durations of the force excitation are shown in the displacement graph. The current answer shows a sharp increase at the time of force application with an exponential decrease following this initial jump. Said jump seems to increase almost linearly for larger forces applied. Moreover, from the exponential decrease of the current the time constant can be derived. The time constant τ is defined as the time that passes as the voltage across a capacitor drops to about 37 % of its initial value [38].

$$\tau = RC \tag{5.4}$$

From the different excitation strengths, an average for the parallel resistance of the gate stack was calculated. Using the determined stress σ across the device, the piezoelectric constant g_{31} and the thickness of the AlN layer d_{AlN}, the voltage generated across the piezoelectric material V_{AlN} in respect to the applied force was calculated [87], [146], [147].

$$V_{AlN} = \sigma \cdot g_{31} \cdot d_{AlN} \tag{5.5}$$

On the basis of these calculations a leakage current of a few fA was deduced. The piezoelectric coefficient g_{31} can be deduced from the piezoelectric coefficient d_{31}, the relative permittivity ε_r and electric constant ε_0 [146].

$$g_{31} = \frac{d_{31}}{\varepsilon_r \cdot \varepsilon_0} \tag{5.6}$$

Since the value of the piezoelectric coefficient d_{31} was not measured in this work, the work of Yarar et al. was consulted [87]. The relative permittivity of the AlN used in this work was measured to be $\varepsilon_{r,AlN} = 10$. The additional charges Q_{AlN} generated by the excitation of the piezoelectric material were calculated using the capacitance of the gate stack C_{AlN} and V_{AlN}.

$$Q_{AlN} = C_{AlN} \cdot V_{AlN} \tag{5.7}$$

Considering that these calculations result in an additional gate stack charge of a few pC, the leakage current seems to be a good estimation. Furthermore, from this it may be assumed that the drop in current is a direct result of the leakage current across the piezoelectric layer and could largely be prevented by further improvement of the gate isolation.

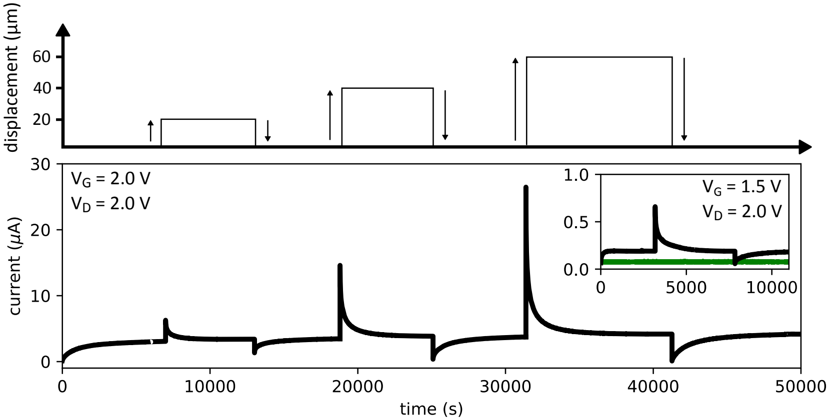


Figure 5.21 Investigation of the influence of different displacements of the tip of the cantilever based sensor setup, comprising the piezoelectric field-effect transistor, on the drain-source current. The displacements of the tip and their duration are shown underneath the measurement results. The current answer was recorded for about 14 h, in order to show the relaxation behaviour of the device, when excited by different signal strengths. In the inset, a comparison between a sensor with a piezoelectric field-effect transistor (black) and a reference sample comprising a transistor without a piezoelectric material (green) is shown. Both samples were excited with the same signal, with only the piezoelectric sample showing and change in channel current. (adapted from [28])

Furthermore, the inset of Fig. 5.21 shows the current response of a reference sample (green) in comparison to that of a piezoelectric sample (black). This measurement was conducted to make sure no additional effects originate in the MOSFET structure that influence channel conductivity [28], [148]. From this it can be presumed, that solely the deformation of the piezoelectric AlN layer influences the conductivity in the semiconductor.

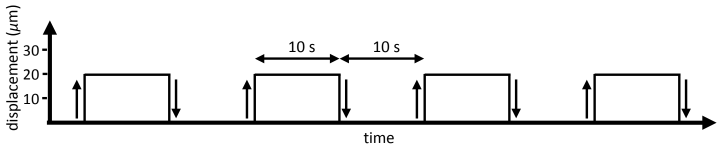


Figure 5.22 The excitation signal used for the periodic mechanical excitation of the cantilever based sensor setup comprising a piezoelectric field-effect transistor.

In addition to the single stimulus, a periodic signal was used to stimulate the cantilever and with that the transistor. The excitation is schematically shown in Fig. 5.22. The force was again exerted on the cantilever by the micrometre screw, which was extended 20 µm and kept at this position for 10 s before it was retracted. Every stimulus was followed by a period of 10 s in which no force acted on the cantilever. This action was repeated for 150 cycles. Periodic excitation of the cantilever with a frequency of 50 mHz results in the current answer displayed in Fig. 5.23. The device followed the input signal precisely, which can be seen even more clearly in the magnified view of the highlighted time period. However, for the first 10 pulses, a transient settling period is visible. This settling period can most likely be linked to an initial charging of traps in the isolation layers of the device. Such behaviour could be reduced or even eliminated with an annealing step at the end of the fabrication process. To further show this initial effect, all maximum and minimum current values were extracted from the measurement and displayed in the second inset (peak-to-peak). The channel current levels in the unexcited periods do not experience a large decrease over the time of stimulation. On the contrary, the device answer to excitation shows a higher level in the beginning. Consequently, the average over the difference between the two states (red) is also higher in the beginning. Most likely traps within the isolating materials in the gate stack (SiO_2 gate oxide or AlN piezoelectric layer) were charged during the first excitation cycles. However, this settling period only lasts a few pulses. From this point forward, the stimulation results in an unchanged current signal.

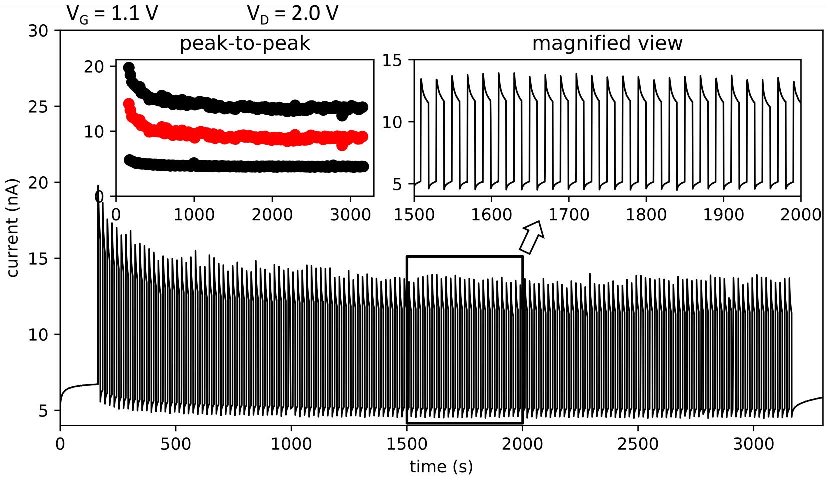


Figure 5.23 Current response of the cantilever based sensor setup comprising a piezoelectric field-effect transistor to a periodic mechanical excitation signal. In the inset "magnified view", the time period between 1500 s and 2000 s is highlighted. Furthermore, an analysis of the maxima and minima is given in the inset "peak-to-peak". Additionally, the oscillation amplitudes are shown in red to show the transient settling.

With these measurements it is safe to say, that the sensor device, consisting of a cantilever and a piezoelectric field-effect transistor, is able to detect a range of forces applied to it. Furthermore, from the current answer one can distinguish between the magnitude and duration of the force. Due to the fabrication process, most likely the ion beam etching used to structure the gate stack, the dielectric effectiveness of the AlN layer was reduced. This leads to the seen decrease in current over time, even though the force on the cantilever stays unchanged. However, this simple CMOS compatible sensor setup was successfully used to detect low frequency stimulation with constant and periodic excitation signals [28].

5.3.2.1 Simulation

In order to deduce the reasons for the previously shown decrease in the current answer over time, a numerical simulation was performed using Python. The channel current of a transistor in the subthreshold regime can be expressed using the following equation [38]:

$$I_D \approx I_{DSS} \cdot exp\left(\frac{V_{GS}}{mV_T}\right)\left[1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{5.8}$$

Here, I_{DSS} describes the subthreshold leakage current, m is the subthreshold ideality factor and V_T is the thermal voltage. With this, the relationship between the channel current and the applied gate voltage is described.

The application of a stress across the transistor induces additional charges in the piezoelectric material and therefore in the gate stack, resulting in a change of the gate voltage. With equation 5.5 this additional potential difference across the AlN created by the externally applied stress was deduced. Fig. 5.24 shows the measurement results in relation to the simulated values. The measurement values are the same as can be seen in Fig. 5.23. From Fig. 5.24 the good agreement of the simulated values with the recorded data can be seen. The calculated potential change V_{AlN} was used to determine the initial rise in current as a response to an applied force. The charge compensation was modelled with the leakage current, which compensates the charges on the floating gate and thus reduces the gate voltage over time.

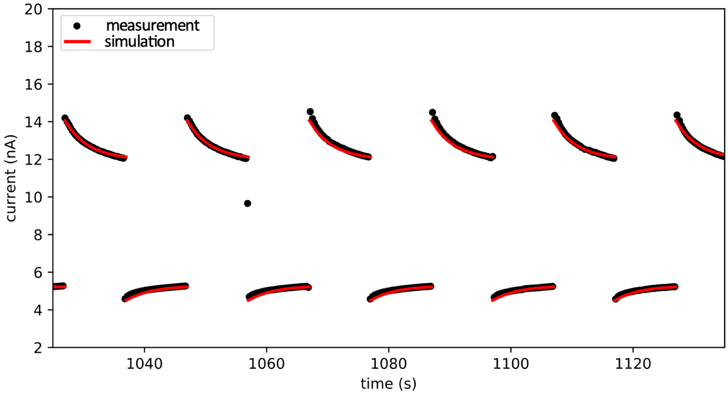


Figure 5.24 Simulation results (red) compared to a measurement (black) of the stress sensor based upon the created piezoelectric field-effect transistor. The measurements were performed at V_D = 2.0 V and V_G = 1.1 V for a transistor with a channel width of W = 25 µm and a channel length of L = 10 µm.

In order to calculate the leakage, the time constant τ was taken from the measurement and used to calculate the leakage resistance across the piezoelectric AlN layer using equation 5.4. Furthermore, from this the initial leakage current I_{leak} could be determined.

$$I_{leak} = \frac{V_{AlN}}{R_{AlN}} \tag{5.9}$$

The charge on the floating gate decreases based on the leakage current. Therefore, the change of the charge was modelled and the resulting change in V_{AlN} was determined with equation 5.7.

$$\mathrm{Q}(t) = Q_{\mathrm{AlN}} - \int_{0}^{t} I_{leak}\, dt \tag{5.10}$$

The floating gate charge decrease over time is modelled in equation 5.10. It was assumed that the leakage current across the AlN follows an exponential decrease.

Based on this simulation, it is reasonable to assume that a leakage current across the piezoelectric AlN is responsible for the current decrease over time. Said current behaviour was seen for all devices measured, independent from the method of excitation or the force applied to the cantilever. Since re-deposition of material during ion beam etching is a common phenomenon, it may be assumed that this fabrication step results in the seen device behaviour.

parameter	value
force on cantilever	108 mN
δ	8.3 µm
σ	10.75 MPa
V_{AlN} (initial)	206 mV
Q_{AlN} (initial)	3.3 pC
I_{leak} (initial)	3.3 fA
I_{DSS}	3.5 pA
m	8
V_{T}	26 mV

Table 5.2 Parameters used in the simulation of the channel current change in response to constant force applied to the cantilever.

5.3.3 Magnetic Excitation

The limitations of the previously discussed mechanical excitation setup were addressed as follows. Due to the setup utilising a micrometre screw, solely unidirectional displacement of the cantilever tip could be achieved. To allow bidirectional oscillation, the excitation method was changed to magnetic excitation. A permanent magnet was attached to the tip of the free standing cantilever. With an electromagnet positioned underneath the sensor, contactless excitation was realised. Two different setups were built around this method of excitation. In the first setup the data recording was done by a SMU and it was used to record low frequency oscillations for different excitation signals (the setup is shown in Fig. 4.2). In the second setup a lock-in amplifier allowed faster data recording and it was used to determine the optimal operation voltages of the transistor and to show the impact of the resonance frequency on the device output (the setup is shown in Fig. 4.3). Lastly, the possibility of using other piezoelectric materials with higher coefficients than AlN will be discussed.

5.3.3.1 Periodic Excitation

The measurements described here were conducted using the procedure defined in chapter 4.2.2. Since the SMU used for these measurements allows only limited resolution, merely low frequency signals could be used to excite the sensor. However, with this setup the precise force applied to the tip of the cantilever could be determined. The forces that act on the tip of the cantilever can be calculated using [149]

$$F = \frac{B_1 B_2 A_1 A_2}{4\pi r^2 \mu_0} \tag{5.11}$$

with $B_{1,2}$ being the magnetic flux density, $A_{1,2}$ being the areas of the magnet and the electromagnet, r being the distance between the magnet and the electromagnet and μ_0 being the vacuum permeability. In the previous chapter the device reaction to varied magnitudes of applied force was presented. Since the behaviour of the sensor does not fundamentally change, here the reaction to different input signals is shown. Using a function generator, the device was confronted with differently shaped magnetic field excitation signals and the corresponding output signals are shown in Fig. 5.25.

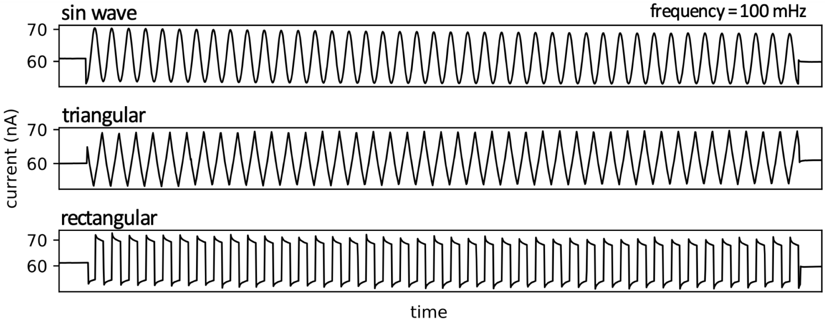


Figure 5.25 Current response of the piezoelectric sensor to excitation signals of different shapes (sin wave, triangle and rectangular). The measurements were performed at V_D = 1.5 V and V_G = 1.5 V for transistors with a channel width of W = 25 µm and a channel length of L = 50 µm.

In addition to the previously used rectangular mechanical excitation signal with a frequency of 50 mHz (see Fig. 5.22), a rectangular, a sine wave and a triangular magnetic excitation signal with frequencies of 100 mHz were used. Said signals were applied to the electromagnet via the function generator and the corresponding outputs from the transistor were recorded. Fig. 5.25 shows that every input signal can be clearly distinguished from the other shapes. For the signals used here, a maximum force of 8.4 mN was determined. Comparing this value to the forces applied before, the detection range of this sensor becomes apparent. During additional measurements, forces as low as 100 µN could be detected using the SMU for data recording. However, this value is limited by the dimensions of the cantilever and could easily be improved by further geometrical adjustment.

With the transistor used here, a maximum force of 8.4 mN (of the sine or triangular excitation signal) resulted in a change of 9 nA in the channel current, which corresponds to a 15 % increase compared to the initial current. Furthermore, the maximum channel current change increases even more, when sudden forces are applied to the cantilever. Replacing the gradual application of force of the sine or triangular signal with the pulse like stimulation (rectangular excitation signal) results is a 10 nA change in current. Due to the leakage current across the AlN, a gradual excitation would yield lower maximum output currents. This finding is supported by the corresponding principle of sharp excitation of piezoelectric crystals used in e.g. lighters to generate short high voltages.

5.3.3.2 Sensitivity Analysis

In the previous examination of the sensor device based on the created piezoelectric field-effect transistor, the reaction to forces applied to the tip of the cantilever was investigated. For these measurements it was assumed that the highest sensitivity is achieved when the transistor voltages are chosen in a way that a small change in gate voltage results in a correspondingly large increase in channel current. Therefore, drain and gate voltages that allowed the operation on the subthreshold swing were used to fulfil this requirement. However, since this was merely an assumption, this chapter is used to identify the optimal point of operation. Additionally, the influence of applying a stimulation signal at the resonance frequency is investigated. Operation at the resonance frequency of the cantilever should further increase the output signal of the transistor, since the amplitudes of the oscillations of the cantilever increase at this frequency. Furthermore, the limit of detection and the sensitivity of the sensor setup were determined and compared to sensor approaches with similar concepts. For all measurements presented in this chapter the setup presented in chapter 4.2.3 was used.

The resonance frequency f_R of the Si cantilever and therefore the sensor, was in a first step calculated in order to define the measurement resolution. The fact that the permanent magnet on the tip of the cantilever essentially acts as a weight was taken into account for the calculations [150].

$$f_R = \frac{1}{2\pi}\sqrt{\frac{3EI}{L^3 \cdot (M + 0.23 \cdot m)}} \tag{5.12}$$

The length of the free-standing part of the entire sensor setup (length of the cantilever with the magnet at the front) is given by *L*, the mass of the magnet is given by *M* and the mass of the cantilever by *m*, Young's modulus by *E* and the moment of inertia by *I*. The values for all parameters can be taken from table 5.3.

variable	**value**
E	125 GPa [145]
I	$2.4 \cdot 10^{-14}$ m^4
L	11.5 mm
M	210 mg
m	15.8 mg

Table 5.3 Values for the parameters used to calculate the resonance frequency of the proposed setup with equation 5.13.

With these values, a resonance frequency of $f_R \approx 820$ Hz was calculated. Here it is important to notice, that the length L is not solely the length of the cantilever. Since the magnet is not a point mass its length reaching out over the length of the cantilever adds to the total length of the sensor. To confirm this presumed resonance frequency, an excitation signal with a peak-to-peak force of $F_{PP} = 33.6$ mN was applied. The transistor voltages were chosen to operate the transistor near the presumed ideal point of operation. The output of the lock-in amplifier and the voltage over the serial resistance were recorded with an oscilloscope. The lock-in amplifier's output is the peak-to-peak value of the oscillating signal. Hence, if the output of the lock-in increases, the amplitude of the oscillations increased. Consequently, with the amplitude of the input signal being kept constant, an increase in the lock-in output suggests additional influences, namely resonance.

First, the frequency of the excitation signal was increased slowly from 200 to 900 Hz. This provided a rough overview over the device response to various frequencies and especially the calculated resonance frequency (see Fig. 5.26 inset).

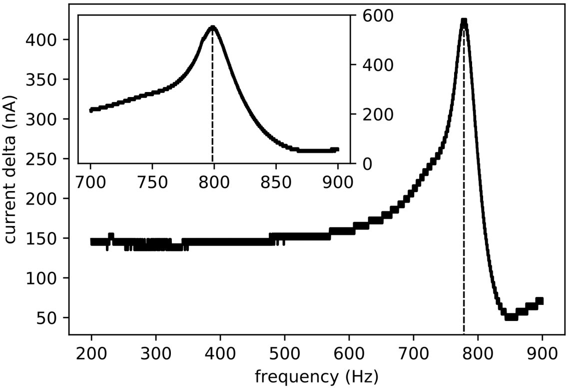


Figure 5.26 Frequency analysis of the current response of the cantilever based stress sensor. The current delta of the oscillations was recorded with a lock-in amplifier in order to show the response near the resonance frequency of the cantilever. Furthermore, the frequency dependent behaviour between 200 and 900 Hz is displayed in the inset. The measurements were performed at V_D = 1.0 V and V_G = 2.0 V for transistors with a channel width of W = 2 µm and a channel length of L = 6 µm.

In the inset in Fig. 5.26 the entire measured frequency range is shown. At about 800 Hz a peak in the lock-in output is visible. This peak suggests, that the resonance frequency lies somewhere near the calculated frequency. However, this first measurement merely gave an overview over the frequency dependency of the sensor. In order to determine the exact resonance frequency, the measurement was repeated with a finer resolution in the range of 700 to 900 Hz. The result of said measurement reveals the resonance frequency to be f_R = 798 Hz (see Fig. 5.26). This value is in good agreement with the calculation. However, it should be noted that the resonance frequency of every cantilever is unique and the value given here is an exemplary measurement result.

Nevertheless, knowing the effect of resonance on the channel current allows speculations on additional adaptations of the sensor. Adding a magnetostrictive layer to the cantilever, instead of the magnet on the tip, a thin film magnetoelectric (ME) sensor would be possible. A number of magnetic field sensor approaches with bilayer ME composites have been realised already and show promising results [151]–[154]. In comparison to other cantilever based magnetic field sensors, the addition of a magnetostrictive thin film to the sensor setup described in this work could achieve even better results, since the generated potential across the piezoelectric layer is used to drive the underlying field-effect transistor. Hence, the sensing element is positioned very close to an amplifier, which, in theory, would improve the signal to noise ratio and the sensitivity.

Moreover, the resonance frequency was used in this work to identify the operation point of the transistor that allows the sensor to have the highest sensitivity (see Fig. 5.27). Since the current signal is greatest at f_R, an excitation signal with this frequency was applied to the electromagnet, thus allowing maximum signal response and consequently reducing noise influences. The drain voltage was kept constant and the gate voltage swept. In addition to the lock-in amplifier output, the channel current was measured by recording the voltage over the serial resistance. The channel current signal (black) shown in Fig. 5.27 was subsequently processed with a band-pass filter and does therefore not show the oscillations of the current signal. However, it follows the trajectory of the transfer characteristics of the device. In addition, the lock-in output (red) is displayed. The signal reveals a maximum at a gate voltage of $V_G \approx 1.82$ V. When looking at the channel current signal and comparing the incline to the location of the maximum of the lock-in output, the peak is near the steepest part. The slight shift visible can be explained by the measurement delay of the lock-in amplifier.

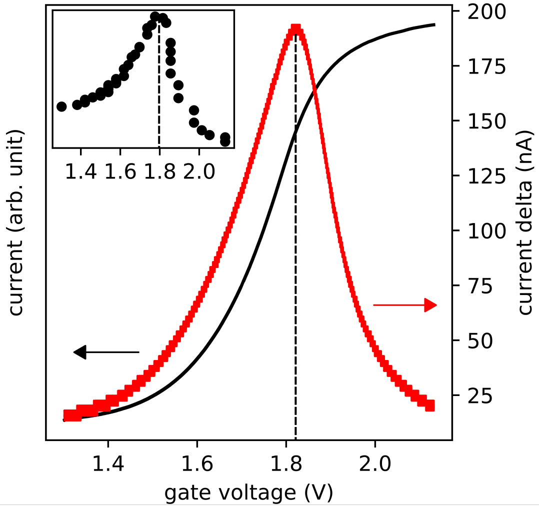


Figure 5.27 Sensitivity analysis of the piezoelectric stress sensor performed to find the ideal point of operation. The sensor characteristic (black) was derived directly from the sensor response, whereas the current delta (red) was recorded using a lock-in amplifier. The inset shows the derived incline of the recorded sensor response. All measurements were recorded for varying gate voltages and show the point of highest sensitivity. The measurements were performed at V_D = 2.5 V for transistors with a channel width of W = 10 µm and a channel length of L = 10 µm. The measurements were performed at V_D = 1.0 V for transistors with a channel width of W = 2 µm and a channel length of L = 6 µm.

To highlight the relationship between the subthreshold swing and the sensitivity, the differentiation of the current signal is displayed in the inset of Fig. 5.27. The steepest incline of the curve is at a gate voltage value that is very close to the maximum of the output signal oscillations. Therefore, the assumption that operating the device as closely to this point as possible to achieve the highest sensitivity was correct. Henceforth, by further optimising the operation voltages, it should be possible to achieve even better results for all forms of excitation, since the previously shown measurements were not performed at the transistors ideal operating voltages.

The limit of detection of a sensor gives the lowest value, which is possible to be recorded with the given measurement setup. For the presented sensor, based on the piezoelectric field-effect transistor, the limit of detection measurements were performed at the optimal operation voltages. The stress depended current change was recorded by applying force signals of varying amplitudes from 10 µN down to 900 nN at a constant frequency of 512 Hz. This frequency was not the resonance frequency of the cantilever. As a result, the stress across the piezoelectric transistor can be calculated directly from the force applied to the tip of the cantilever using equations 2.18, 2.19 and 2.20. In Fig. 5.28, the change in channel current is shown as a function of the stress across the transistor on the cantilever and the applied force. From these measurement results the sensitivity of the device was determined to be $S_F \approx 44.5$ nA/N. Additionally, the sensitivity can be given in respect to the corresponding stress created due to the cantilever setup: $S_\sigma \approx 0.565$ fA/Pa. Furthermore, the limit of detection is shown in this graph, representing the smallest force recognisable by this device at $LOD_F \approx 33$ nN. The corresponding limit of detection in respect to the stress generated across the transistor was calculated: $LOD_\sigma \approx 3$ Pa. Beyond this point the noise of the measurement setup and the sensor itself did not allow any detection of a force applied to the sensor. The LOD_F could be improved even further, since it is highly depended on the geometry of the cantilever. Increasing the length or reducing thickness of the cantilever would result in the displayed stress occurring at lower forces, moving the LOD_F to lower values. Thus, the LOD_σ in respect to the generated stress shows the limitation of the device most clearly.

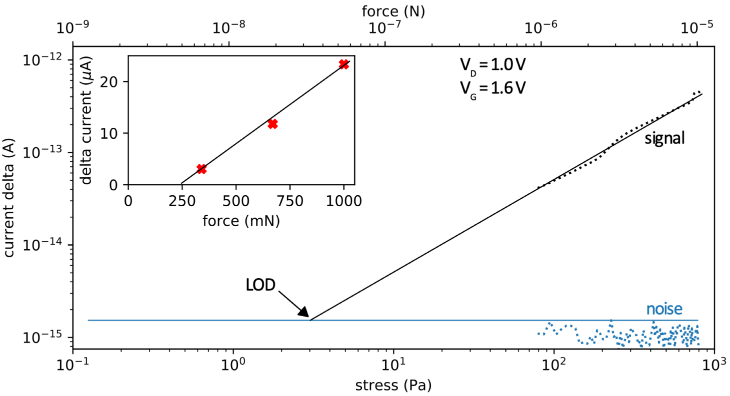


Figure 5.28 The point of lowest possible excitation of the piezoelectric field-effect transistor is displayed. The noise measurement determines the level of parasitic noise of the system and the signal shows the sensor response for various excitation strengths. Measurements are displayed as dots, whereas the solid lines show extrapolations of the recorded values. The measurements were performed for transistors with a channel width of $W = 25$ µm and a channel length of $L = 10$ µm.

Furthermore, it is important to note, that a number of transistors with different channel dimensions on various cantilevers with a range of different geometric dimension were investigated. The transistors were driven at different operating voltages. Consequently, the performance factors given show the potential of the piezoelectric field-effect transistor but it may not be the highest values reachable. In the inset of Fig. 5.28, the sensitivity for measurements not conducted with the noise reducing lock-in amplifier setup are displayed. The presented data was deduced from the mechanical excitation measurements presented previously (see Fig. 5.21). The sensitivity for the sensor was determined as $S_{SMU} = 10.6$ N^{-1}. Here it is important to note, that the underlying measurements were not performed at the optimal point of operation for the transistor. However, in a comparable force region the sensor shows competitive performance nevertheless [28], [138], [140]. Furthermore, no subsequent circuitry is used to amplify the signal further, keeping the setup clear and simple. This simplicity would help with future integration into measurement applications and circuitry. Moreover, it has to be taken into account, that the detected forces were strongly dependent on the cantilever geometry. Thus, optimising the geometry of the cantilever could greatly affect the sensor performance further.

5.3.4 Alternative Piezoelectric Materials

In addition to the optimisation of the operating voltages, other piezoelectric materials could be considered for the gate stack to further improve device performance [155]. A large number of materials (e.g. ZnO, BaTiO3, PZT) show higher piezoelectric coefficients compared to AlN [155]–[157]. Within the CMOS compatible piezoelectric materials, AlScN is showing promise to overtake AlN in micro-electro-mechanical system (MEMS) applications [158]–[160]. The piezoelectric coefficients shown for AlScN are considerably higher compared to AlN [159], [161]. Therefore, AlScN was chosen for a first comparison and to examine how introducing a material with a higher piezoelectric coefficient would affect the device.

The sensitivity in relation to the applied gate voltage was investigated by using the measurement setup described in chapter 4.2.3. Both samples used had the same geometrical parameters, with only a slight difference in thickness (h_{AlN} = 525 µm, h_{AlScN} = 500 µm). The main difference between both samples lay in the gate stack. Whereas the AlN sample had a gate stack comprised of 5 nm Ta, 100 nm Pt, 500 nm AlN and 300 nm Pt, the AlScN sample's gate stack was made of 5 nm AlN, 100 nm Pt, 500 nm AlScN and 300 nm Pt. Besides the different piezoelectric materials, the adhesive layers underneath the Pt seedlayer differed as well. However, no great performance reducing influences could be observed from either adhesive layer used. The AlScN layer was deposited by the chair of "Materials and Processes for Nanosystem Technologies", following the process presented by Fichtner et al. [160], [162].

For the measurement, the lock-in amplifier signal was recorded in relation to a change in the applied gate voltage. The resulting peaks shown in Fig. 5.29 indicate the points of highest sensitivity. For both measurements the same excitation signal was applied, driving the cantilevers at their corresponding resonance frequencies.

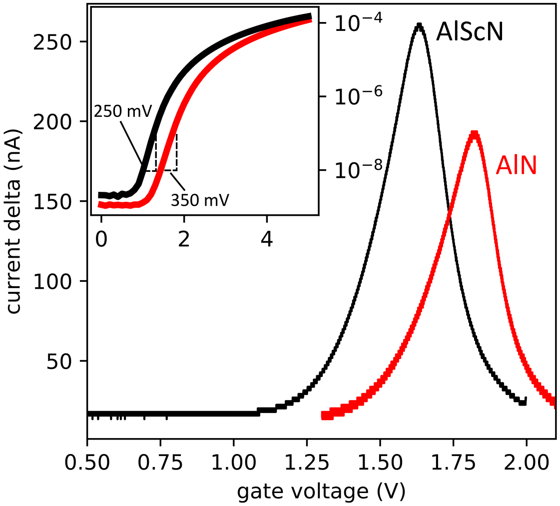


Figure 5.29 Comparison between two stress sensors comprising AlN (red) and AlScN (black) as piezoelectric sensing materials in the gate stacks of the piezoelectric field-effect transistors. The AlScN based sensor shows a higher current delta at a lower applied gate voltage for the same excitation signal. The inset compares the transfer characteristics of both transistor types, showing a smaller voltage change needed for an increase of one decade in current for the AlScN sample. The measurements were performed at V_D = 2.5 V for transistors with a channel width of W = 10 µm and a channel length of L = 10 µm.

The comparison between the sensors using AlN and AlScN as sensing materials in the piezoelectric field-effect transistors, demonstrates that AlScN comprising devices display a higher current output for the same input signal. The current answer of the AlN sensor oscillates at a maximum peak-to-peak value of 68 nA, whereas the AlScN device states a maximum of 92 nA. Additionally, for the AlScN device the maximum is reached at a gate voltage of 1.6 V. Compared to the AlN device, where the peak is reached at 1.8 V, the AlScN sensor shows a higher output signal at a lower applied voltage. The transfer characteristics are compared in the inset of Fig. 5.29. They underline the favourable behaviour of AlScN. Whereas the AlN device shows a subthreshold swing of 350 mV/dec, the AlScN sample only needs a gate voltage change of 250 mV to show an increase in channel current of one decade.

In conclusion, optimisation of the device in ways of sensitivity and power consumption is possible. One approach would be the introduction of other piezoelectric materials with higher piezoelectric coefficients, as shown. Another would be the optimisation of the underlying MOSFET. With a reduced gate oxide thickness, any charges introduced into the gate stack by deforming the piezoelectric layer would have a greater effect. Additionally, from the conducted experiments it appears beneficial to improve the subthreshold swings of the piezoelectric transistors. Creating devices with a subthreshold swing close to the modern silicon technology standard of 60 mV/dec would improve the performance of the sensor significantly.

5.3.5 Device Application

In the first chapter, a possible application of the piezoelectric field-effect transistor as a force or tactile sensor was introduced. Continuing to use the cantilever structure as a means of stress application across a transistor with an AlScN piezoelectric layer and a leaky integrate-and-fire circuit, a neuronal inspired force sensor was realised. The schematic of the proposed setup is illustrated in Fig. 5.30. By changing the charging current of the oscillator circuit, a pulse train was generated in response to a force stimulus.

This conversion of a constant input to a pulsed output signal is comparable to the way humans detect a force at their extremities [163]. The created force sensor was designed to copy the behaviour of Merkel's disks, which have been associated with the sensation of light pressures in humans. The Merkel's disks are characterised by their slow adaptation of output spike frequency when confronted with a constant stimulus [63]. Therefore, this simple setup is able to show similar behaviour as the human "sense of touch". However, the term "sense of touch" is based on a number of stimuli, including but not limited to mechanical stimulation [163].

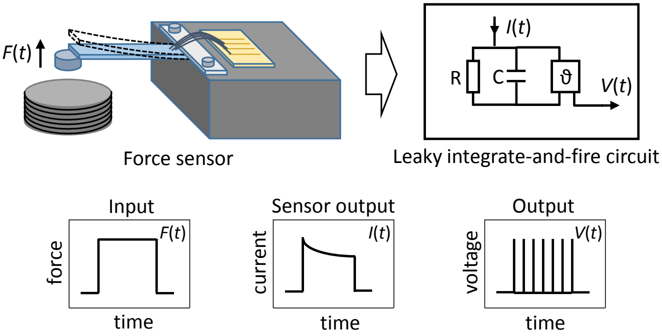


Figure 5.30 Schematic setup of a neuronal inspired force sensor comprising the created piezoelectric field-effect transistor. The force sensor schematic shows the magnetic excitation method used to apply defined forces to the sensor. The sensor output was used as a charging current in a leaky integrate-and-fire circuit. Underneath the setup, the input signal (force), the sensor output (current) and the circuit output (voltage pulses) are illustrated.

As Fig. 5.30 shows, the force stimulus $F(t)$ applied to the cantilever results in a change in the channel current of the transistor. The channel current $I(t)$ is used to charge the capacitance of the leaky integrate-and-fire circuit. At the point where the voltage across the capacitor is equal to the threshold θ, the capacitor is rapidly discharged which results in a voltage peak in the circuit output $V(t)$.

Consequently, a force applied at the sensor results in an increased charging current in the oscillator circuit and, depending on the threshold condition, a voltage pulse at the output.

Furthermore, as can be seen in the sensor output illustration in Fig. 5.30, the current *I*(*t*) shows the exponential decay for constant forces applied, introduced in chapter 5.3.2. However, considering the time scale of the current reduction, the sensor output to the leaky integrate-and-fire circuit results in a decrease in firing frequency of the oscillator circuit for the application of a constant force. Consequently, a prolonged sensor excitation force could be frequency coded in the output signal. Additionally, the magnitude of the applied force could also be coded in this way, with greater forces resulting in a higher frequency output. However, here the general approach of a force sensor based on the developed piezoelectric field-effect transistor is shown. Therefore, the described setup was implemented and a variation of forces applied to the sensor via the magnetic excitation introduced in the previous chapter. Fig. 5.31 shows the input signal with the corresponding output.

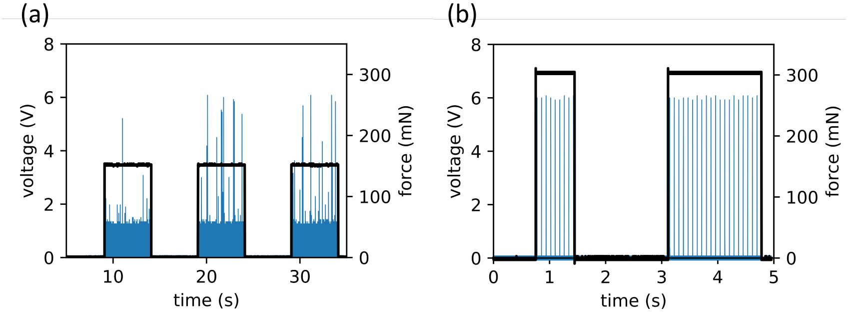


Figure 5.31 (a) Pulsed voltage output (blue) of the neuronal inspired force sensor in response to force pulses of 150 mN magnitude and a duration of 5 s. (b) Pulsed voltage output (blue) of the neuronal inspired force sensor in response to force pulses of 300 mN magnitude and varying durations.

For force pulses (black) of 150 mN magnitude and a duration of 5 s applied to the sensor, a pulse train output (blue) was generated. Additionally, as can be seen in Fig. 5.31 (a), at the times where no force was applied to the sensor, the system generated a constant output. Furthermore, from the first results different magnitudes for the output pulses are noticeable. These differences are due to the sampling rate of the oscilloscope used to record the input and the system output. Fig. 5.31 (b) highlights this, since here a higher sampling rate was chosen and all pulses have the same magnitude. In addition to showing the stability of the output signal, Fig. 5.31 (b) shows the system's response to an additional pulse train. This pulse train consists of force pulses with 300 mN and varying durations. The different pulses were applied to show the sensitivity and flexibility of the system. The magnitude changes allowed the verification of the previously postulated frequency change for different forces applied to the sensor. Furthermore, when a constant stimulus was applied to the sensor, a slow adaptation of the frequency of the generated output spikes was observed.

The presented results lead to the conclusion that the piezoelectric field-effect transistor can be used as a sensing element in a neuronal setup to emulate force sensing. Due to the assumed CMOS compatibility of the transistor based sensor, this simple setup could be implemented in an integrated circuit, making the system highly scalable and allowing the integration in state-of-the-art silicon technology fabrication lines. Furthermore, eliminating the cantilever from the setup and using a setup where the force is directly applied to the gate stack of the transistor would allow the creation of arrays. With such arrays not only force detection would be possible. Further, tactile sensing, the determination of sizes and shapes, and slipping detection could be realised - thus making the piezoelectric field-effect transistor a promising sensor for neuronal and robotic applications.

6 Conclusion

In this thesis, two different adaptations of the well-known metal-oxide-semiconductor field-effect transistor were created and characterised. Both devices have completely different fields of application, with the MemFlash cell acting as an artificial synapse and the piezoelectric field-effect transistor as a building block for sensor applications. However, even though the tasks the devices were created to accomplish are very different, both utilise the behaviour of an enhancement type MOSFET. Both devices investigated in this work show great potential as CMOS compatible MOSFET based concepts for memristive or sensor applications. The combination of state-of-the-art silicon technology with novel concepts allows high scalability and thus integration of the MemFlash cell and the piezoelectric field-effect transistor, alike.

The capability of memory devices based on the MemFlash cell concept to act as artificial synapses was shown in research prior to this work. The main drawbacks of the MemFlash approach are the high operating voltages and the corresponding high power consumption compared to other memristive devices. Based on a theoretical postulation, a tunnelling oxide thickness adjustment and its benefits to said operational concept was investigated. To do so, the MemFlash cell fabrication process was implemented in the cleanroom and a measurement setup, including a task-specific data recording software, was developed. The fabrication of the MemFlash cell involved the analysis of the underlying MOSFET and an analysis of the tunnelling current used for charging and discharging of the floating gate. During the investigation of the charging behaviour, it was deduced that the gate stack leakage current played a more important role for memristive device behaviour than optimised coupling factors.

The created memristive devices showed retention times of several years, which could be lowered by reducing the tunnelling oxide thickness. This enabled the analysis of the learning behaviour for MemFlash devices with different retention times. Furthermore, it allowed the investigation of the postulated fall in power consumption for tunnelling oxide thickness reduction. Alongside voltage and frequency dependent behaviour, device response to pulsed input signals was studied. While devices with varying oxide thicknesses showed similar behaviour when confronted with varying voltage and frequency signals during current-voltage measurements, pulsed operation showed significant differences. Devices with thinner tunnelling oxides showed a strong dependency upon the frequency, amplitude and duration of the applied pulses, whereas the output of devices with higher retention times was not affected by variation of these parameters. Therefore, it was shown that by carefully choosing the thickness of the tunnelling oxide for MemFlash cells the rate at which this artificial synapse learns can be tailored to fit the desired performance. Furthermore, the rate at which charge dissipates from the device can be adjusted by the same fabrication parameter. In learning neural networks, the ability to forget information, could be an asset, since not frequently used information does not occupy space needed for new information. Lastly, said reduction of the oxide thickness reduced the voltages needed to operate the MemFlash cells and thus the power consumptions. With the high power consumption being one crucial downside of the MemFlash approach, reducing it by the mere downscaling of the tunnelling oxide further shows the adjustment capabilities. Therefore, in this work, the implementation of simple learning behaviour adjustment by designing the tunnelling oxide thickness in EEPROM based MemFlash devices was presented. Additionally, it was experimentally shown, that the power consumption of MemFlash cells can be reduced not only by downscaling of the whole device, but also by reducing the thickness of the tunnelling oxide.

The second device introduced in this work was the piezoelectric field-effect transistor. This MOSFET based concept comprises a piezoelectric layer in the gate stack allowing the transistor to react to deformation. The deformation of the piezoelectric layer resulted in additional charges in the gate stack that led to a change in the transistors current answer. To maximise the sensitivity and output signal of this force sensing setup, the ideal position for the transistor on the cantilever was determined via finite-element method simulation. Following this, a fabrication process for piezoelectric transistors on cantilever structures was designed. The basic operation of the transistor was verified, revealing that it experienced the characteristic behaviour of a floating gate transistor. The piezoelectric transistor also showed an increase in threshold voltage and a reduction of channel current compared to a MOSFET structure without piezoelectric layer. This was expected due to the seedlayer needed for the columnar growth of the piezoelectric material. Furthermore, the transistors revealed subthreshold swings between 350 mV/dec and 450 mV/dec. A small subthreshold swing is desired, since a stress induced charge generation would result in a greater channel current change for a device with a steeper subthreshold swing.

The sensor setup of the transistor on the cantilever structure was excited by a variation of signals. Using different excitation methods, it was shown that the sensor was able to detect forces between 33 nN and 1 N. This detection range could be improved even further, since the geometry of the cantilever was the limiting factor. An indication of the potential of the piezoelectric field-effect transistor in such a sensor setup is given by the minimum stress of 3 Pa that could be detectable. Furthermore, it could be shown that the sensor output followed every excitation signal imposed on the cantilever, regardless of frequency and shape. The transistor was able to produce an output signal that followed excitation frequencies between 50 mHz and 1kHz. Furthermore, the point of operation at which device sensitivity is at its highest was identified, showing that the subthreshold regime is ideal for operation. In this region a small change in gate voltage leads to a large change in channel current. When taking the subthreshold swing of the created device into account and comparing it to the 60 mV/dec of modern silicon technology transistors, this work shows the improvement potential of the presented approach.

The AlN, used as the piezoelectric layer, allowed the CMOS compatible fabrication of the sensor while also allowing reasonable piezoelectric properties. However, other CMOS compatible piezoelectric materials with higher coefficients have emerged over the years. Thus, AlScN was introduced into the device to show the flexibility of the fabrication process and the possibility to increase device performance. The AlScN's higher piezoelectric coefficient allows the device to show a greater response compared to the AlN based devices at similar power consumption and excitation stimuli. Lastly, the presented sensor was implemented in a neural inspired force sensor in order to show possible device application. The sensor, in combination with a leaky integrate-and-fire circuit, was able to show frequency coded force detection. The setup did exhibit Merkel disk like behaviour and is therefore a good candidate to be used in neural force and tactile sensor applications.

A Appendix

A.1 Fabrication of Devices

Within this work a number of devices were fabricated. The complete device fabrication of all devices, including every single step is shown here. Firstly, the MOSFET devices, without and with tunnelling window, are presented. Secondly, the fabrication of both different MemFlash device configurations (silicon oxide and polymer based devices) are explained. Lastly, the piezoelectric field-effect transistor fabrication process is laid out.

For all devices the steps are described individually as presented visually in the corresponding figures.

MOSFET

In the following, all processes used in this work for the fabrication of MOSFET devices are presented along the visual representation in Fig. A.1.

(a) The initial device setup received from the Fraunhofer Institute in Itzehoe (ISIT). The devices were processed on an 8-inch wafer and cut into 10 mm x 10 mm chips after the photoresist layer was applied and structured. This resist layer includes the tunnelling window, which, due to its small size of 2 µm x 2 µm, was to fine for the mask aligner's resolution at Kiel University.

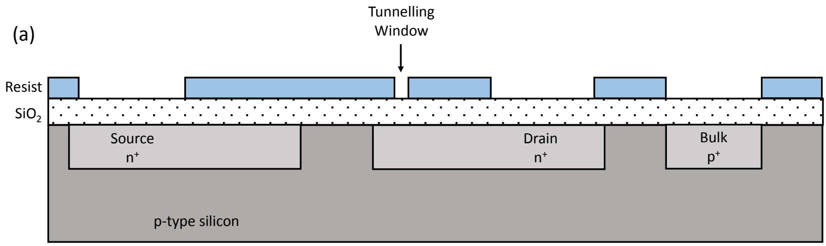
(b) Since the tunnelling window is not needed for the MOSFET device, the resist is removed in the first step. In order to resolve the resist, the chip is placed in acetone for 10 min.

(c) Application of a resist mask (AZ 5214E from Microchemicals) leaving the bulk, source and drain areas free.

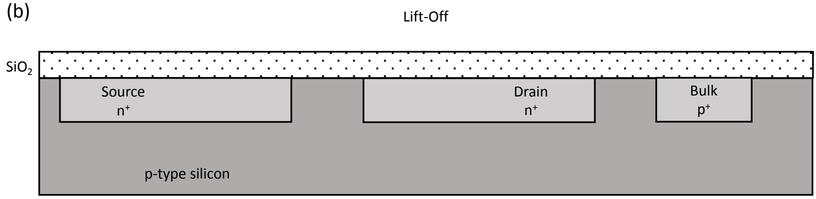
(d) Removal of the SiO_2 layer above the bulk, source and drain areas, using a 1:100 HF (48 %) solution for 15 min.

(e) Deposition of 150 nm Ti for the connection into the semiconductor (wiring) using DC magnetron sputtering.
(f) Removal of the resist mask to take away unwanted Ti and merely leave the wiring by placing it in acetone for 10 min.
(g) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate area.
(h) Deposition of 150 nm Ti to form a gate using DC magnetron sputtering.
(i) Final MOSFET device after removal of the resist mask and excess Ti.

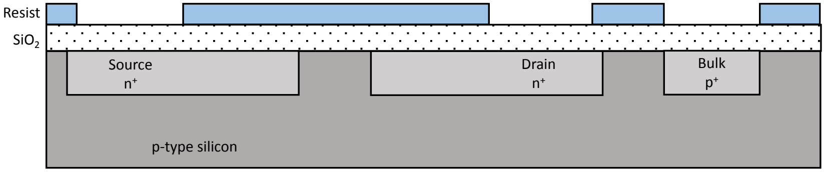
(a)


Tunnelling Window
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

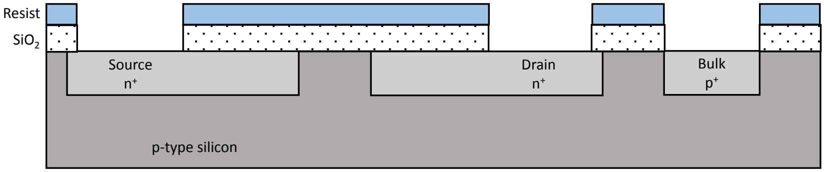
(b)


Lift-Off
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

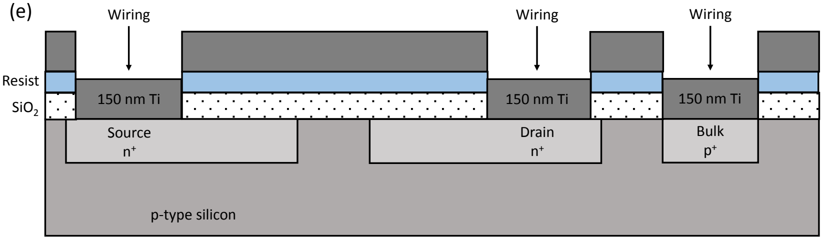
(c)


Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

(d)


Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

(e)


Wiring
Wiring
Wiring
Resist
SiO_2
150 nm Ti
150 nm Ti
150 nm Ti
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

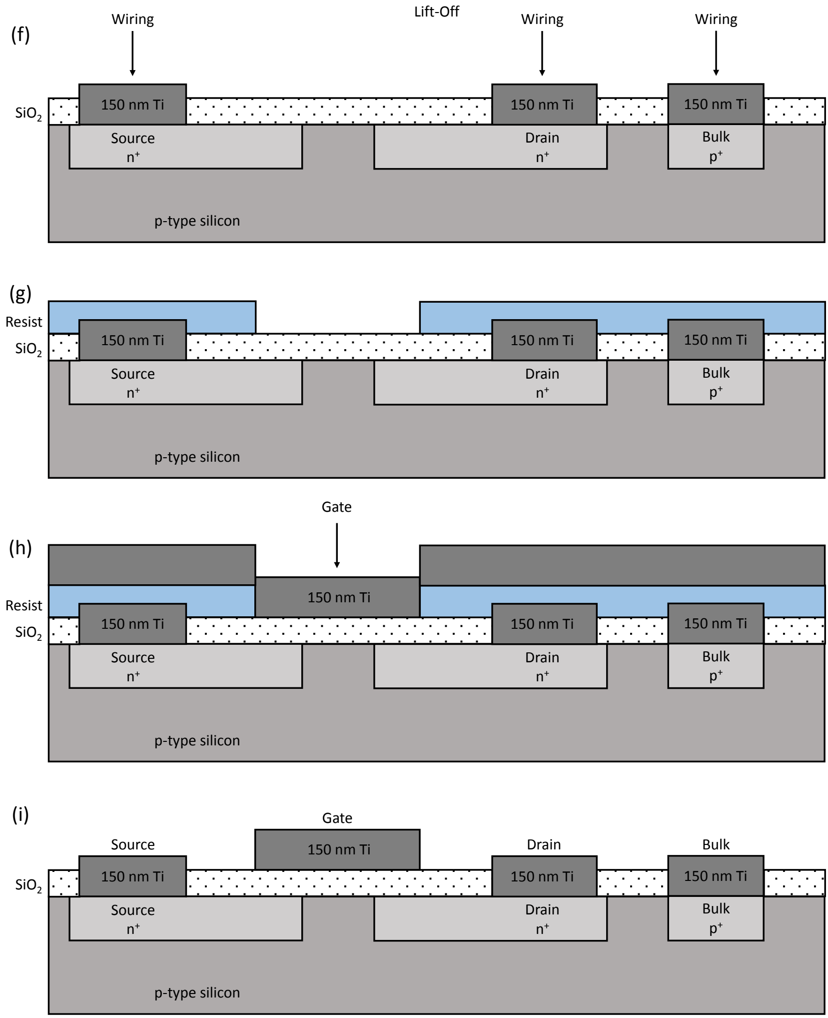
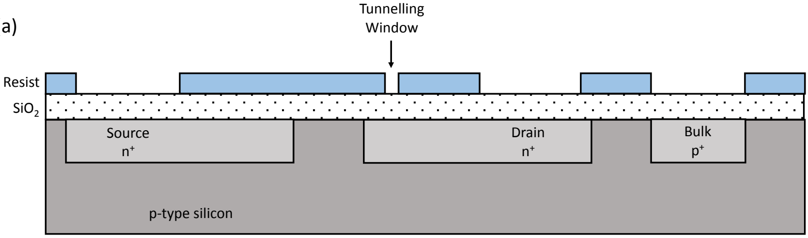


Figure A.1 Schematic cross-sectional view of all steps involved in the MOSFET fabrication process, with (a) showing the initial device received from the Fraunhofer Institute (ISIT) and (i) showing the final MOSFET created.

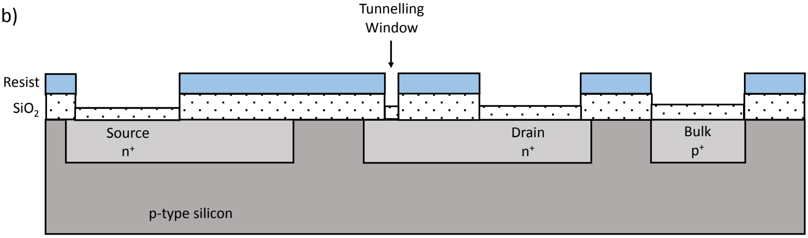
In the following, all processes used in this work for the fabrication of MOSFET devices with a tunnelling window are presented along the visual representation in Fig. A.2.

(a) The initial device setup received from the Fraunhofer Institute in Itzehoe (ISIT). The devices were processed on an 8 inch wafer and cut into 10 mm x 10 mm chips after the photoresist layer was applied and structured. This resist layer includes the tunnelling window, which, due to its small size of 2 µm x 2 µm, was to fine for the mask aligner's resolution at Kiel University.
(b) Thinning of the oxide within the tunnelling window using a 1:100 HF (48 %) solution.
(c) Removal of the resist mask by placing it in acetone for 10 min.
(d) Application of a resist mask (AZ 5214E from Microchemicals) leaving the bulk, source and drain areas free.
(e) Removal of the SiO_2 layer above the bulk, source and drain areas, using a 1:100 HF (48 %) solution. The chips were etched for a total time for 15 min (etch times from steps (b) and (d) combined).
(f) Deposition of 150 nm Ti for the connection into the semiconductor (wiring) using DC magnetron sputtering.
(g) Removal of the resist mask to take away unwanted Ti and merely leave the wiring by placing it in acetone for 10 min.
(h) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate area.
(i) Deposition of 150 nm Ti to form a gate using DC magnetron sputtering.
(j) Final MOSFET device with a tunnelling window after removal of the resist mask and excess Ti.

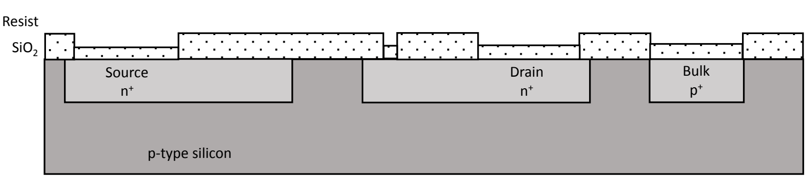
(a)


Tunnelling Window
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

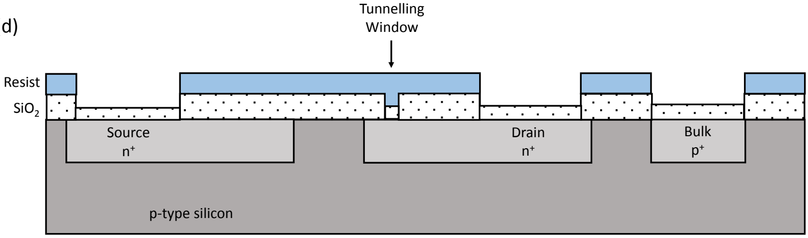
(b)


Tunnelling Window
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

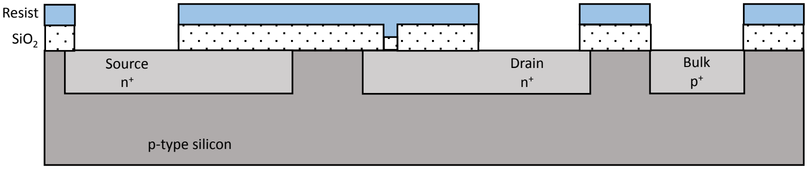
(c)


Lift-Off
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

(d)


Tunnelling Window
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

(e)


Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

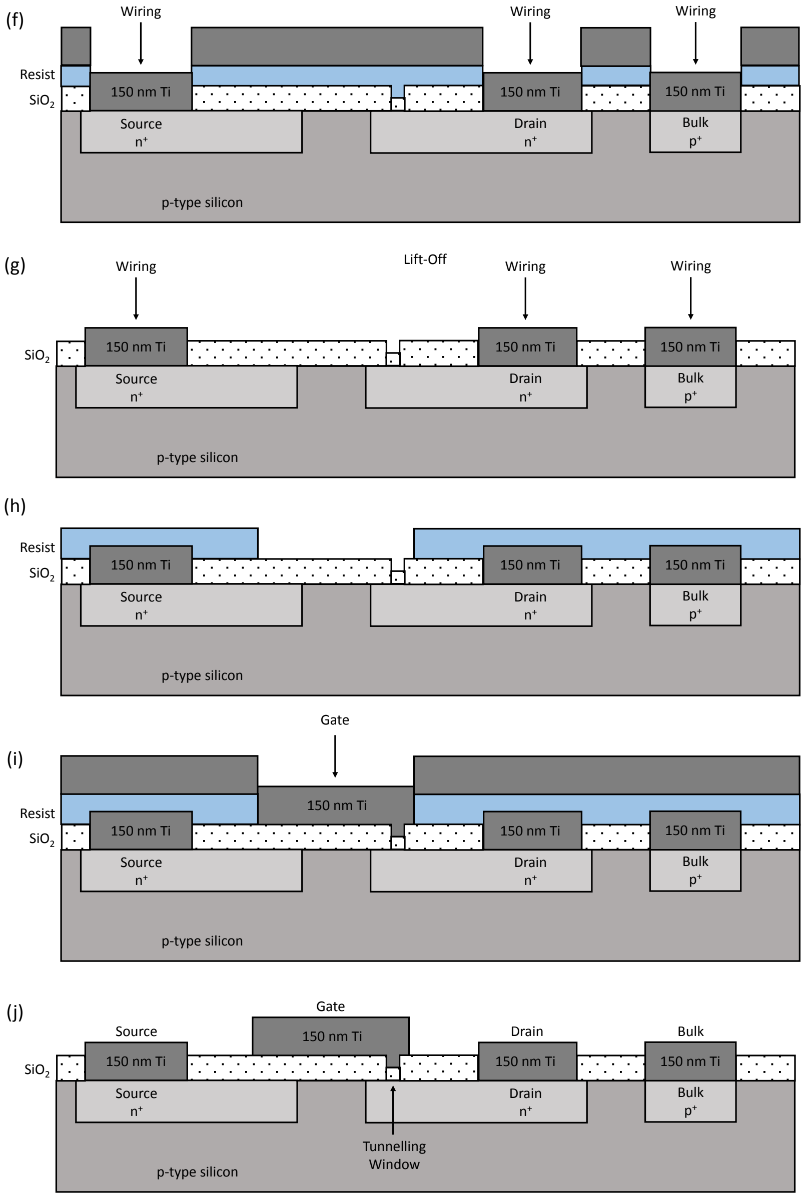
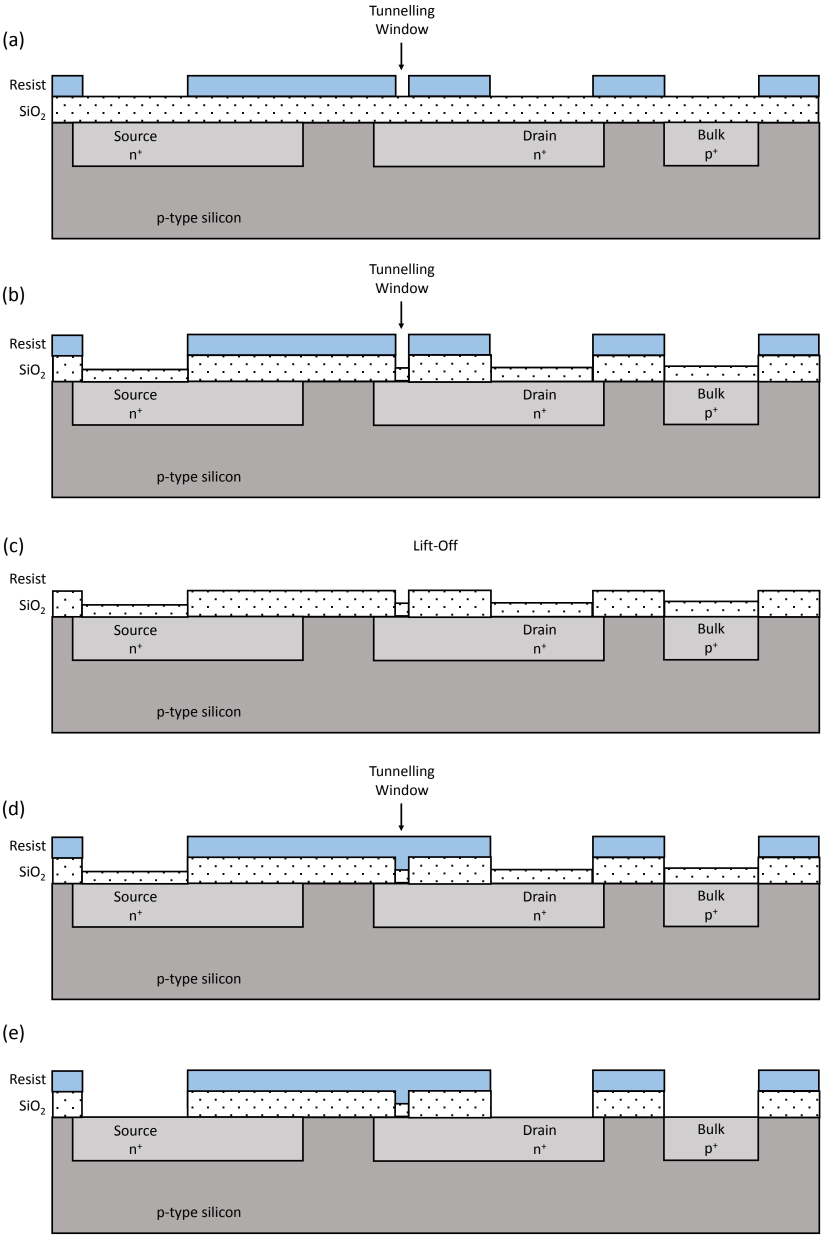


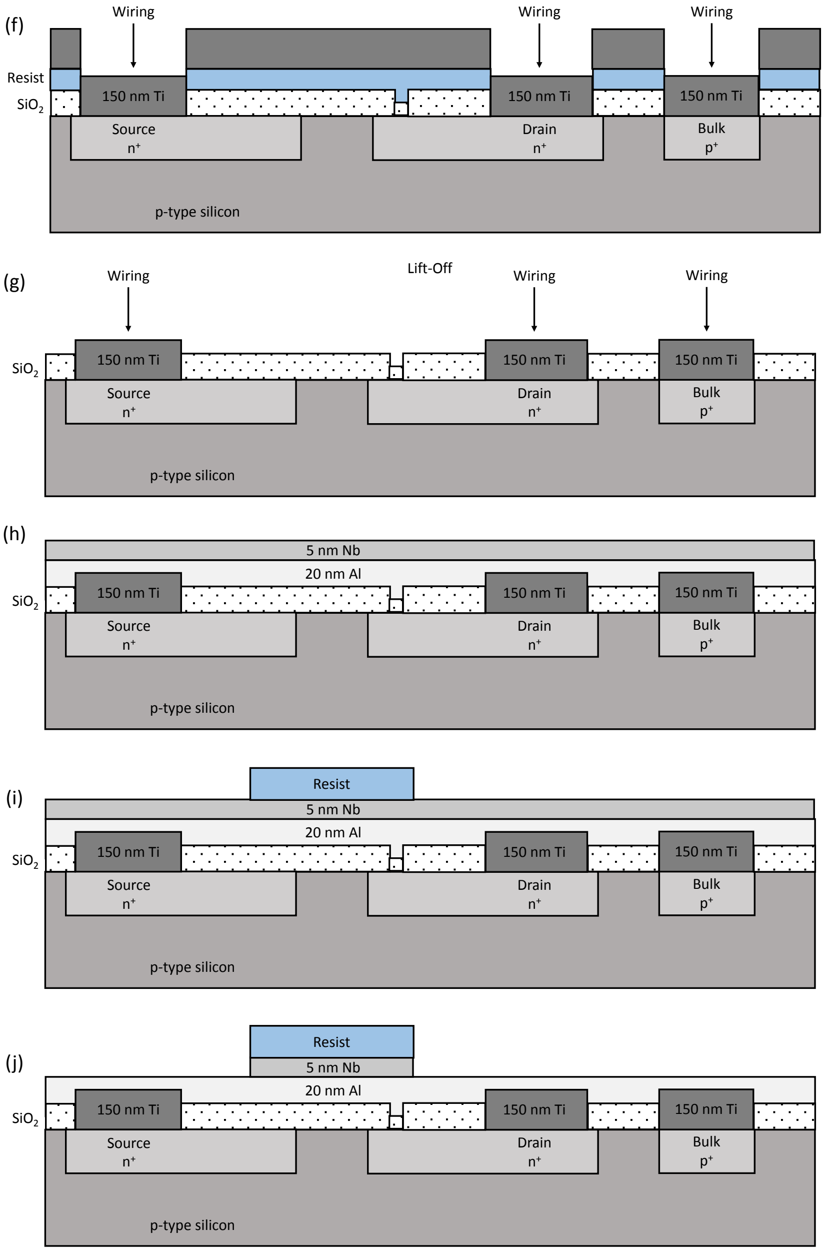
Figure A.2 Schematic cross-sectional view of all steps involved in the fabrication process of a MOSFET with a tunnelling window, with (a) showing the initial device received from the Fraunhofer Institute (ISIT) and (j) showing the final MOSFET created.

In the following, all processes used in this work for the fabrication of silicon oxide based MemFlash devices are presented along the visual representation in Fig. A.3.

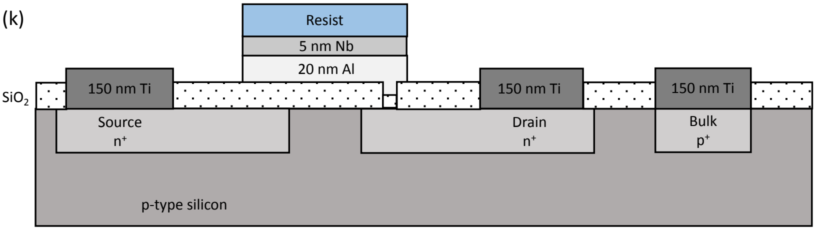
(a) The initial device setup received from the Fraunhofer Institute in Itzehoe (ISIT). The devices were processed on an 8 inch wafer and cut into 10 mm x 10 mm chips after the photoresist layer was applied and structured. This resist layer includes the tunnelling window, which, due to its small size of 2 µm x 2 µm, was to fine for the mask aligner's resolution at Kiel University.
(b) Thinning of the oxide within the tunnelling window using a 1:100 HF (48 %) solution.
(c) Removal of the resist mask by placing it in acetone for 10 min.
(d) Application of a resist mask (AZ 5214E from Microchemicals) leaving the bulk, source and drain areas free.
(e) Removal of the SiO_2 layer above the bulk, source and drain areas, using a 1:100 HF (48 %) solution. The chips were etched for a total time for 15 min (etch times from steps (b) and (d) combined).
(f) Deposition of 150 nm Ti for the connection into the semiconductor (wiring) using DC magnetron sputtering.
(g) Removal of the resist mask to take away unwanted Ti and merely leave the wiring by placing it in acetone for 10 min.
(h) Deposition of 20 nm Al and 5 nm Nb by DC magnetron sputtering.
(i) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate region.
(j) Removal of the Nb layer with plasma etching by placing the chip in a SF_6 plasma for 5 min.
(k) Removal of the Al layer with a TMAH containing solution (AZ 726 from Microchemicals). The duration of the etching process was visually supervised and stopped when the Al was completely dissolved.
(l) Removal of the resist mask by placing it in acetone for 10 min.

(m) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate region.
(n) Deposition of SiO isolation layer by thermal evaporation.
(o) Removal of the resist mask and excess SiO by placing the chip in acetone for 10 min.
(p) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate area.
(q) Deposition of 150 nm Ti to form a gate using DC magnetron sputtering.
(r) Final MOSFET device with a tunnelling window after removal of the resist mask and excess Ti.


(a)
Tunnelling Window
Resist
SiO$_2$
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(b)
Tunnelling Window
Resist
SiO$_2$
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(c)
Lift-Off
Resist
SiO$_2$
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(d)
Tunnelling Window
Resist
SiO$_2$
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(e)
Resist
SiO$_2$
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon

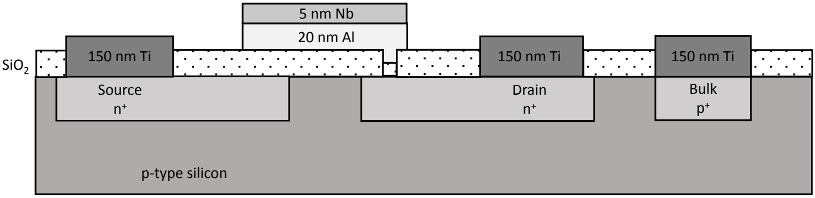

(f)
Wiring
Wiring
Wiring
Resist
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(g)
Wiring
Lift-Off
Wiring
Wiring
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(h)
5 nm Nb
20 nm Al
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(i)
Resist
5 nm Nb
20 nm Al
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon
(j)
Resist
5 nm Nb
20 nm Al
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon

(k)

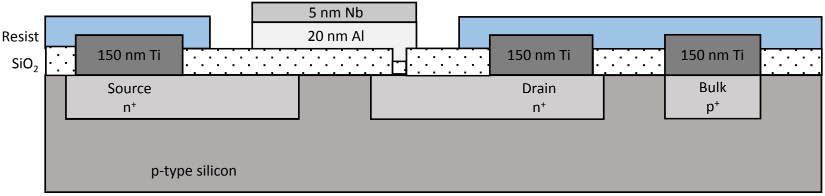


Lift-Off

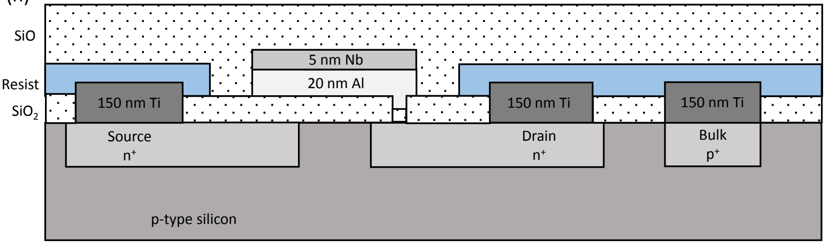
(l)



(m)

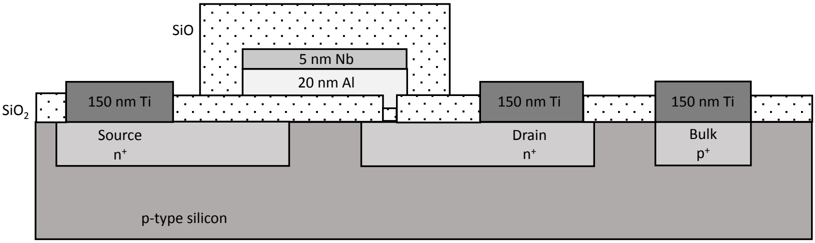


(n)



(o)

Lift-Off



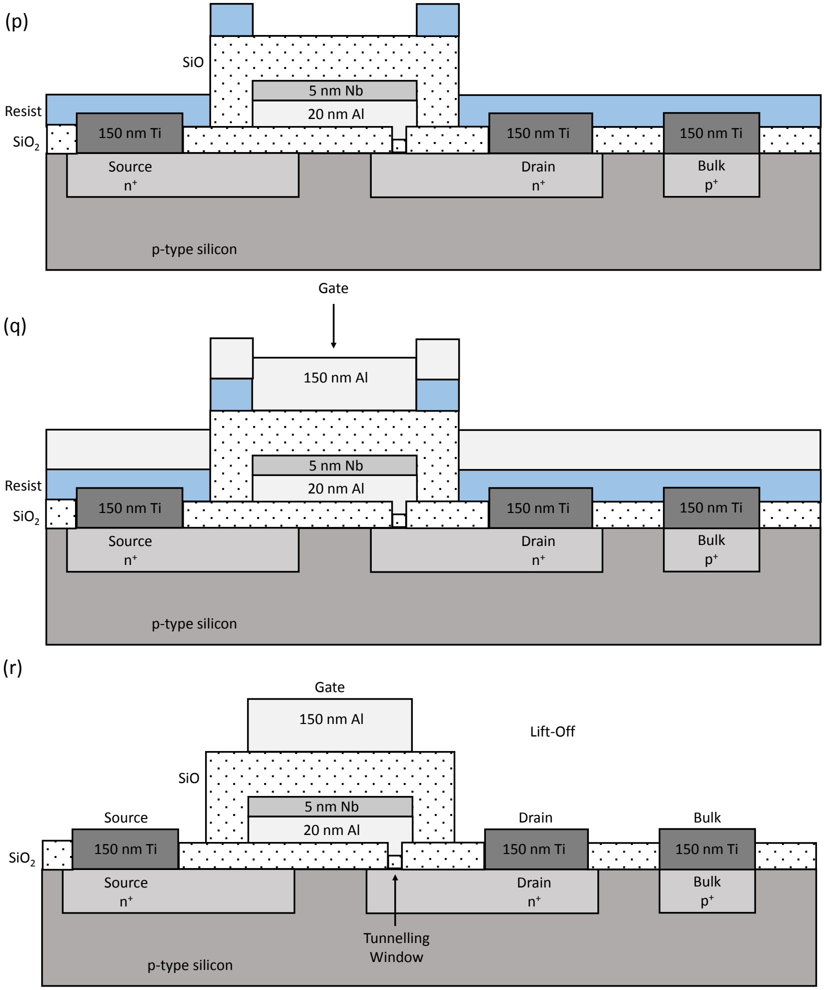


Figure A.3 Schematic cross-sectional view of all steps involved in the fabrication process of the silicon oxide MemFlash devices, with (a) showing the initial device received from the Fraunhofer Institute (ISIT) and (s) showing the final device created.

In the following, all processes used in this work for the fabrication of silicon oxide based MemFlash devices are presented along the visual representation in Fig. A.3.

(a) The initial device setup received from the Fraunhofer Institute in Itzehoe (ISIT). The devices were processed on an 8 inch wafer and cut into 10 mm x 10 mm chips after the photoresist layer was applied and structured. This resist layer includes the tunnelling window, which, due to its small size of 2 µm x 2 µm, was to fine for the mask aligner's resolution at Kiel University.

(b) Thinning of the oxide within the tunnelling window using a 1:100 HF (48 %) solution.

(c) Removal of the resist mask by placing it in acetone for 10 min.

(d) Application of a resist mask (AZ 5214E from Microchemicals) leaving the bulk, source and drain areas free.

(e) Removal of the SiO_2 layer above the bulk, source and drain areas, using a 1:100 HF (48 %) solution. The chips were etched for a total time for 15 min (etch times from steps (b) and (d) combined).

(f) Deposition of 150 nm Ti for the connection into the semiconductor (wiring) using DC magnetron sputtering.

(g) Removal of the resist mask to take away unwanted Ti and merely leave the wiring by placing it in acetone for 10 min.

(h) Deposition of 20 nm Al and 5 nm Nb by DC magnetron sputtering.

(i) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate region.

(j) Removal of the Nb layer with plasma etching by placing the chip in a SF_6 plasma for 5 min.

(k) Removal of the Al layer with a TMAH containing solution (AZ 726 from Microchemicals). The duration of the etching process was visually supervised and stopped when the Al was completely dissolved.

(l) Removal of the resist mask by placing it in acetone for 10 min.

(m) Application of AZ nLof 2070 polymer by spin coating at 5000 rpm for 60 s.

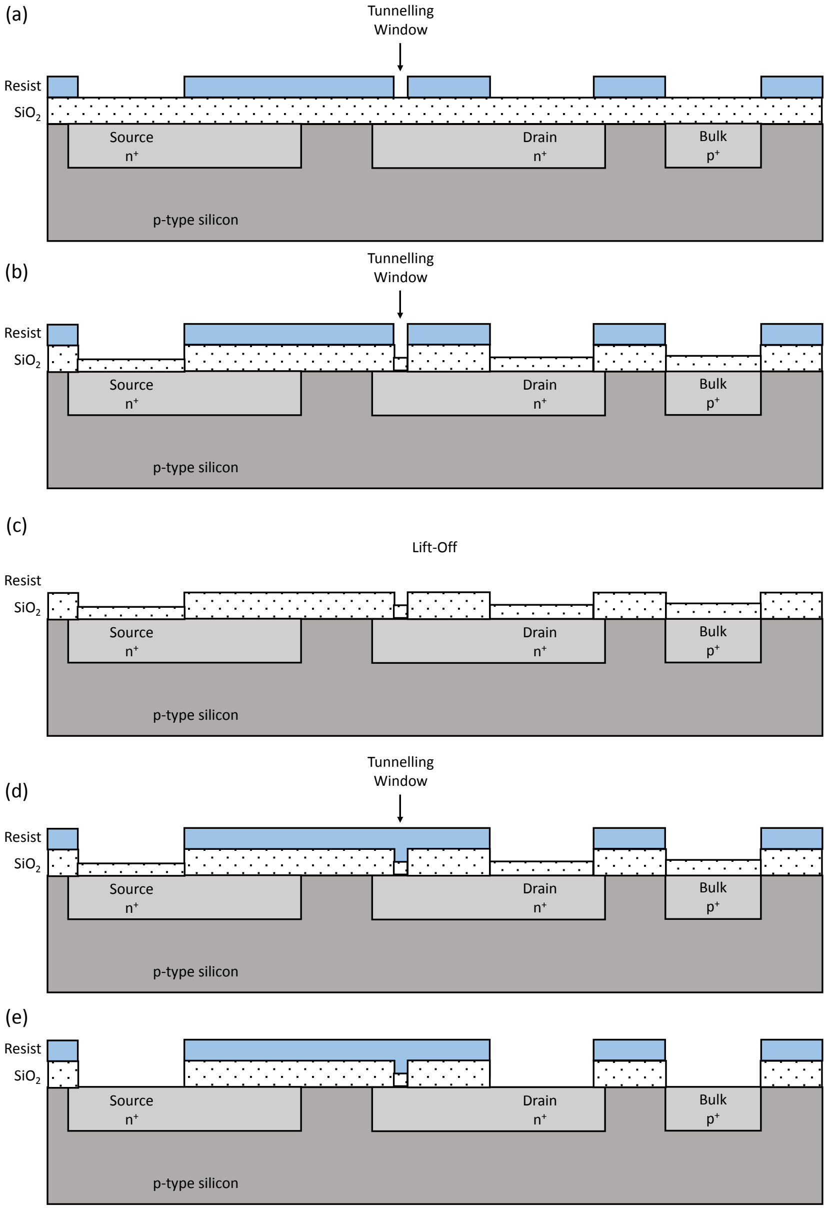
(n) Structuring the polymer to electrically isolate the gate stack with still allowing access to the drain, source and bulk regions.

(o) Deposition of 150 nm Al by DC magnetron sputtering.

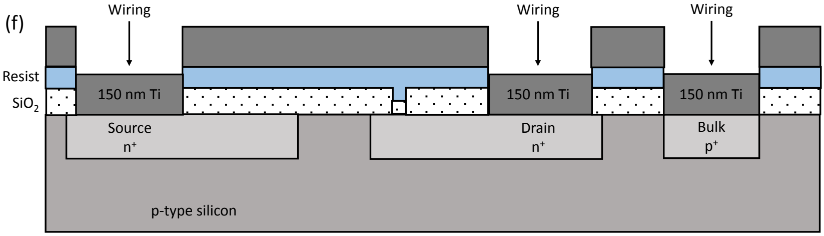
(p) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate area.

(q) Within the definition of the gate, the Al will be etched by the structuring of the resist with the AZ 726 developer. Therefore, in combination with the previous step the Al is structured as well.

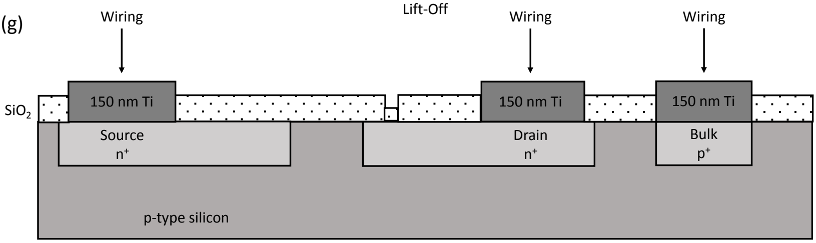
(r) The resist is removed by placing the chip in an acetone bath for a few seconds. The AZ nLof polymer withstands acetone longer than AZ 5214E. However, prolonged exposure damages the polymer.


(a)
Tunnelling Window
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon
(b)
Tunnelling Window
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon
(c)
Lift-Off
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon
(d)
Tunnelling Window
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon
(e)
Resist
SiO_2
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

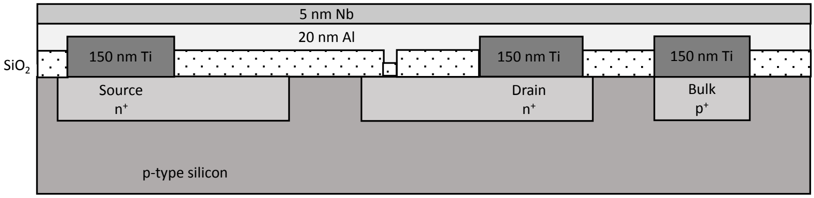
(f)


Wiring
Wiring
Wiring
Resist
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon

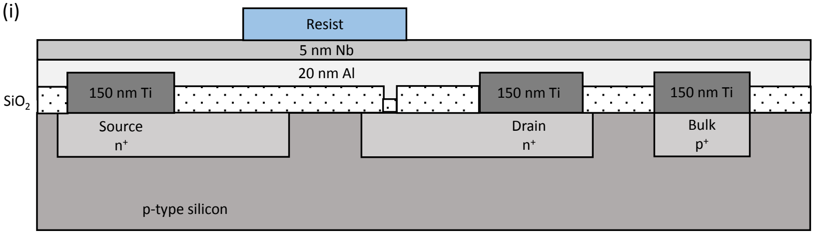
(g)


Wiring
Lift-Off
Wiring
Wiring
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon

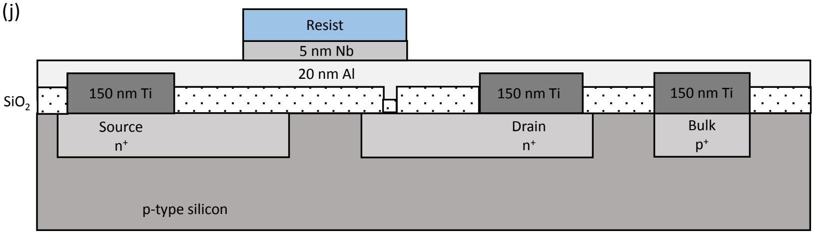
(h)


5 nm Nb
20 nm Al
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon

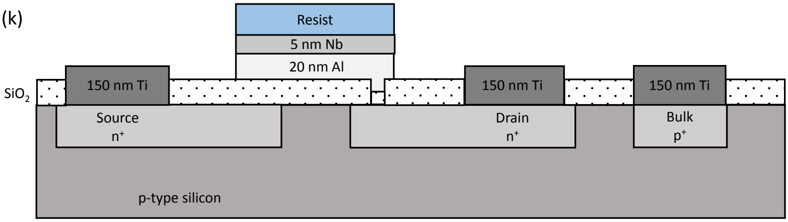
(i)


Resist
5 nm Nb
20 nm Al
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon

(j)

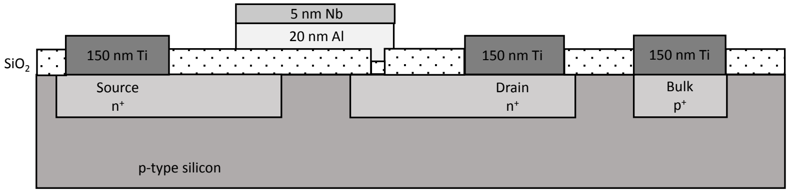

Resist
5 nm Nb
20 nm Al
SiO$_2$
150 nm Ti
150 nm Ti
150 nm Ti
Source
n$^+$
Drain
n$^+$
Bulk
p$^+$
p-type silicon

(k)

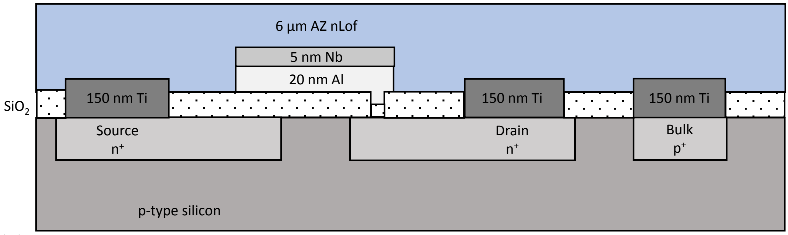


(l)

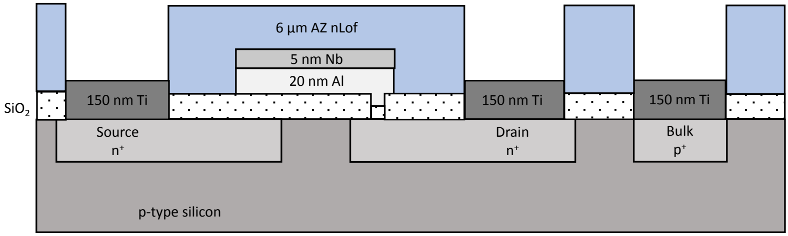
Lift-Off



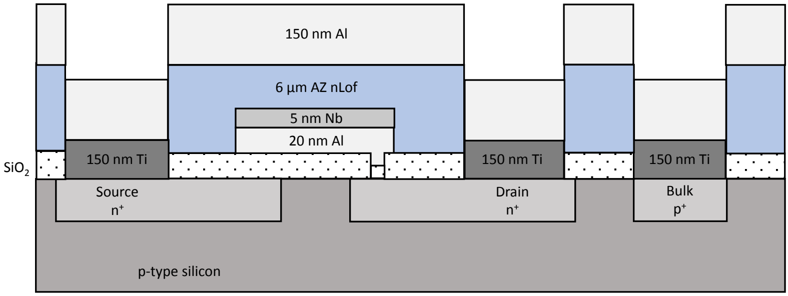
(m)



(n)



(o)



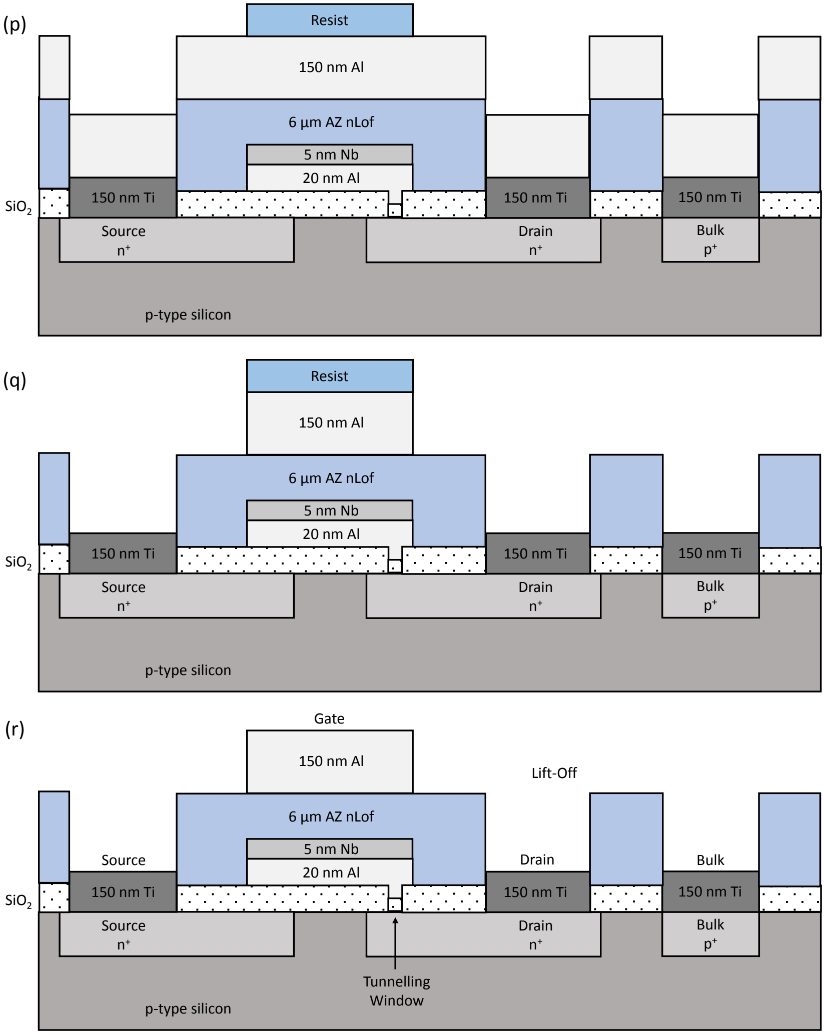


Figure A.4 Schematic cross-sectional view of all steps involved in the fabrication process of the polymer MemFlash devices, with (a) showing the initial device received from the Fraunhofer Institute (ISIT) and (t) showing the final device created.

In the following, all processes used in this work for the fabrication of piezoelectric field-effect transistor devices are presented along the visual representation in Fig. A.5.

(a) The initial device setup received from the Fraunhofer Institute in Itzehoe (ISIT). The devices were processed on an 8 inch wafer and cut into 10 mm x 10 mm chips after the photoresist layer was applied and structured. This resist layer includes the tunnelling window, which, due to its small size of 2 µm x 2 µm, was to fine for the mask aligner's resolution at Kiel University.

(b) Since the tunnelling window is not needed for the MOSFET device, the resist is removed in the first step. In order to resolve the resist, the chip is placed in acetone for 10 min.

(c) Application of a resist mask (AZ 5214E from Microchemicals) leaving the bulk, source and drain areas free.

(d) Removal of the SiO_2 layer above the bulk, source and drain areas, using a 1:100 HF (48 %) solution for 15 min.

(e) Deposition of 150 nm Ti for the connection into the semiconductor (wiring) using DC magnetron sputtering.

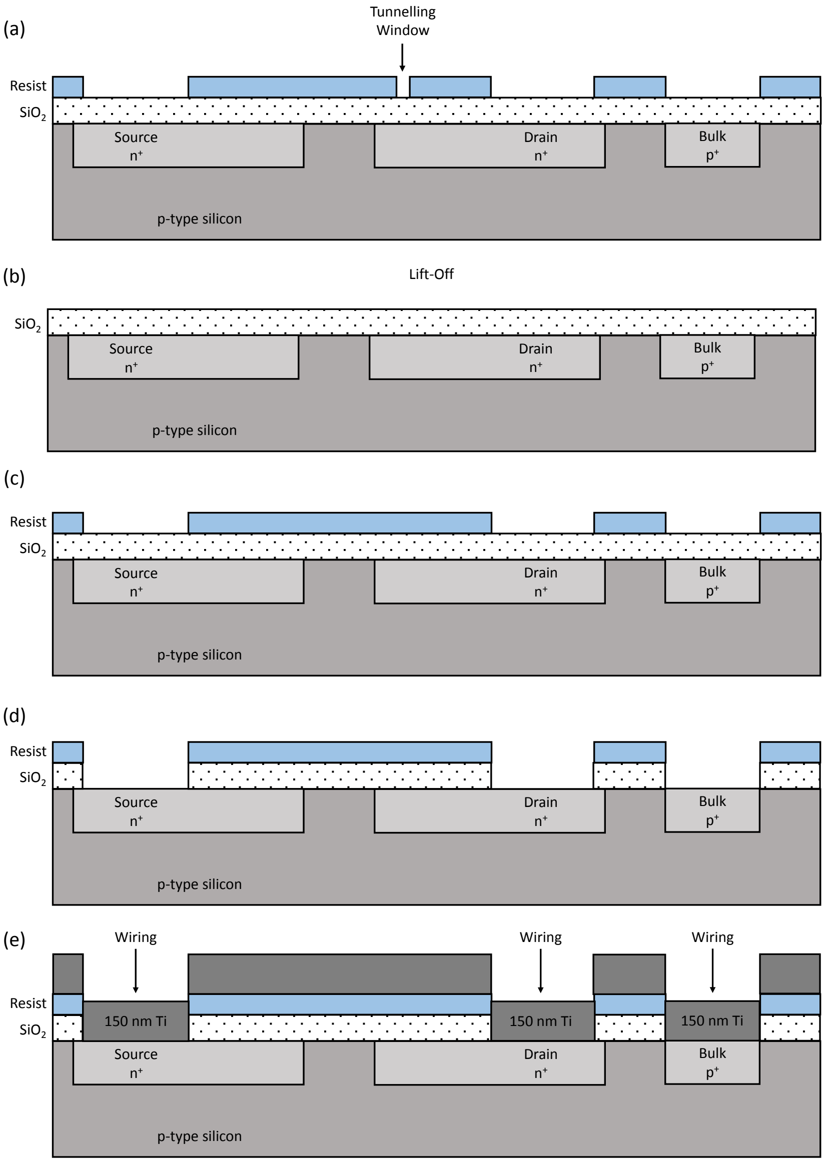
(f) Removal of the resist mask to take away unwanted Ti and merely leave the wiring by placing it in acetone for 10 min.

(g) Deposition of 5 nm Ta, 100 nm Pt, 500 nm AlN and 300 nm Pt. These depositions were performed with the method proposed and optimized by Yarar et al. [87].

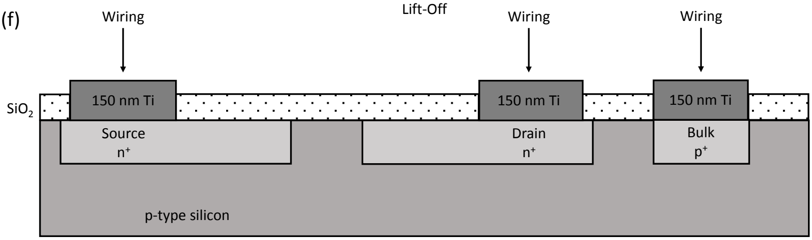
(h) Application of a resist mask (AZ 5214E from Microchemicals) defining the gate area.

(i) Structuring of the gate stack by ion beam etching.

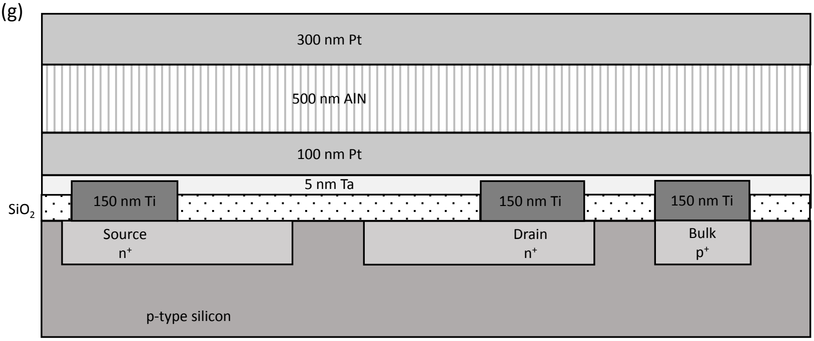
(j) Removal of the resist mask by placing it in acetone for 10 min.


(a)
Tunnelling Window
Resist
SiO2
Source
n+
Drain
n+
Bulk
p+
p-type silicon
(b)
Lift-Off
SiO2
Source
n+
Drain
n+
Bulk
p+
p-type silicon
(c)
Resist
SiO2
Source
n+
Drain
n+
Bulk
p+
p-type silicon
(d)
Resist
SiO2
Source
n+
Drain
n+
Bulk
p+
p-type silicon
(e)
Wiring
Wiring
Wiring
Resist
SiO2
150 nm Ti
150 nm Ti
150 nm Ti
Source
n+
Drain
n+
Bulk
p+
p-type silicon

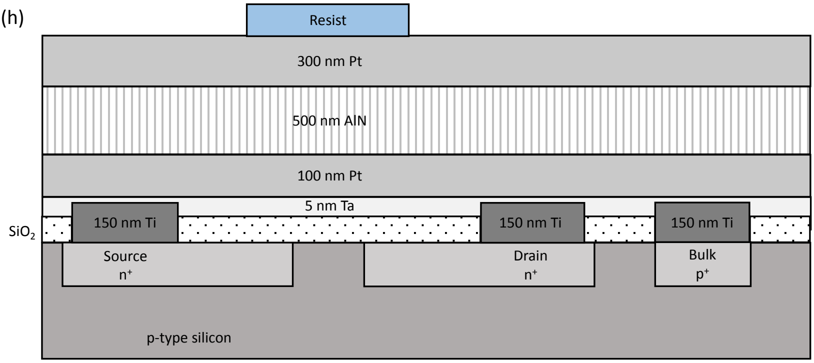
(f)


Wiring
Lift-Off
Wiring
Wiring
SiO_2
150 nm Ti
150 nm Ti
150 nm Ti
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

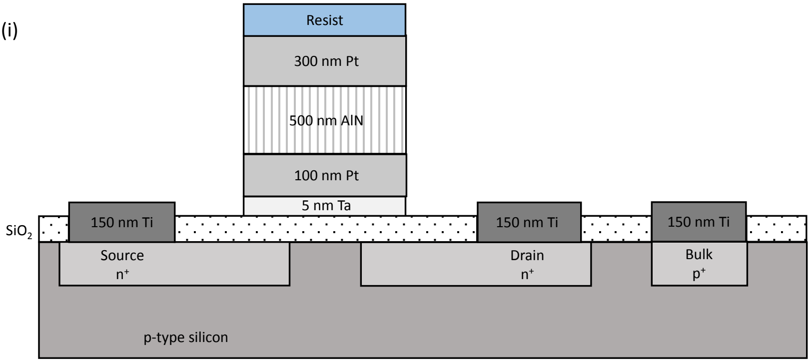
(g)


300 nm Pt
500 nm AlN
100 nm Pt
5 nm Ta
SiO_2
150 nm Ti
150 nm Ti
150 nm Ti
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

(h)


Resist
300 nm Pt
500 nm AlN
100 nm Pt
5 nm Ta
SiO_2
150 nm Ti
150 nm Ti
150 nm Ti
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

(i)


Resist
300 nm Pt
500 nm AlN
100 nm Pt
5 nm Ta
SiO_2
150 nm Ti
150 nm Ti
150 nm Ti
Source
n^+
Drain
n^+
Bulk
p^+
p-type silicon

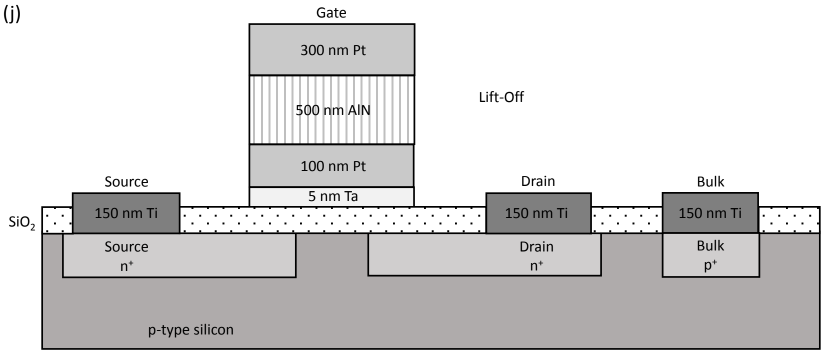


Figure A.5 Schematic cross-sectional view of all steps involved in the fabrication process of the piezoelectric field-effect transistors, with (a) showing the initial device received from the Fraunhofer Institute (ISIT) and (j) showing the final device created.

A.2 Process Parameters

Lithography:

resist	variable	value
AZ 5214E (positive)	coating	60 s @ 4000 rpm
	pre-bake	50 s @ 110 °C
	exposure	2.5 s
	developing	50 s in AZ 726
AZ 5214E (negative)	coating	60 s @ 4000 rpm
	pre-bake	50 s @ 110 °C
	exposure	2.5 s
	reversal bake	120 s @ 120 °C
	flood exposure	7 s
	developing	50 s in AZ 726
AZ nLof 2070	coating	60 s @ 5000 rpm
	pre-bake	300 s @ 100 °C
	exposure	6.5 s
	post-bake	60 s @ 110 °C
	developing	50 s in AZ 726
	hard-bake	120 s @ 125 °C

Table A.1 Parameters used during spincoating and lithography processes.

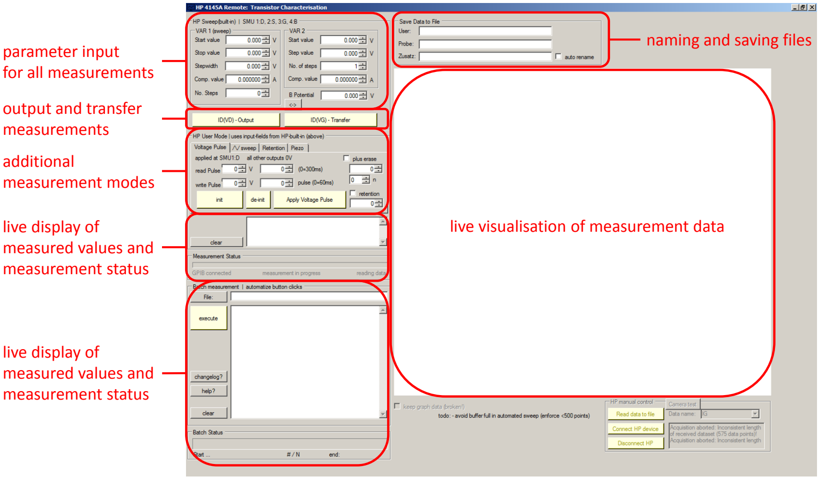
Ion Beam Etching:

	variable	value
plasma	pressure	8 torr
	power	1600 W
	gas	Ar 10 sccm
beam	current	350 mA
	voltage	400 V
neutralizer	gas	Ar 5 sccm
sample holder	rotation	8 rpm
	angle	30 °

Table A.2 Parameters used during ion beam etching processes.

A.3 Measurement Software

Within this work a custom software program was created. The program allows the measurement of all devices produced in this thesis. The graphic user interface (GUI) is shown in Fig. A.6.


HP 4145A Remote: Transistor Characterisation

HP Sweep(built-in) | SMU 1:D, 2:S, 3:G, 4:B

VAR 1 (sweep)
Start value 0.000 V
Stop value 0.000 V
Stepwidth 0.000 V
Comp. value 0.000000 A
No. Steps 0

VAR 2
Start value 0.000 V
Step value 0.000 V
No. of steps 1
Comp. value 0.000000 A
B Potential 0.000 V

HP User Mode | uses input-fields from HP-built-in (above)
applied at SMU1:D all other outputs 0V
☐ plus erase 0
read Pulse 0 V 0 (0=300ms)
write Pulse 0 V 0 pulse (0=60ms)
0 n
☐ retention 0

Measurement Status
GPIB connected measurement in progress reading data

Batch measurement | automatize button clicks

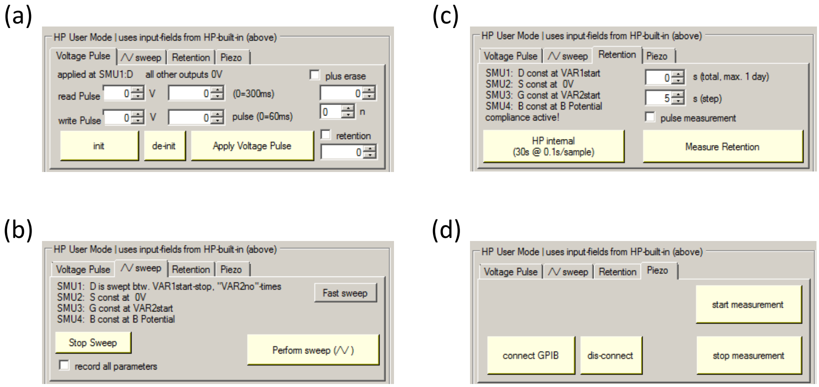
Save Data to File
User:
Probe:
Zusatz:
☐ auto rename

☐ keep graph data (broken!)
todo: - avoid buffer full in automated sweep (enforce <500 points)

HP manual control
Data name: IG
Acquisition aborted: Inconsistent length of received dataset (575 data points)! Acquisition aborted: Inconsistent length

Figure A.6 Graphic user interface created during this work and used for most measurements.

The measurement software enables the user to apply different measurement schemes to a device and record, display and save the measured data. Within the program, different measurement modes were implemented. For the characterisation of all transistors, the output and transfer measurements were used. Since these are the most commonly used modes, they are implemented on the front page of the GUI. Furthermore, the additional modes are a voltage pulse mode (see Fig. A.7 (a)), a voltage sweep mode (see Fig. A.7 (b)), a retention mode (see Fig. A.7 (c)) and a piezo mode (see Fig. A.7 (d)).



SMU1: D const at VAR1start
SMU2: S const at 0V
SMU3: G const at VAR2start
SMU4: B const at B Potential
compliance active!

SMU1: D is swept btw. VAR1start-stop, "VAR2no"-times
SMU2: S const at 0V
SMU3: G const at VAR2start
SMU4: B const at B Potential

Figure A.7 Different measurement modes implemented in the graphic user interface created during this work and used for most measurements.

Eidesstattliche Erklärung

Hiermit erkläre ich:

Diese Dissertation mit dem Titel "On field-effect transistor concepts beyond traditional application" habe ich noch nie, weder ganz noch teilweise im Rahmen eines anderen Promotionsverfahrens vorgelegt oder veröffentlicht. Ich habe mich bislang noch keiner mündlichen Prüfung im Rahmen eines Promotionsverfahrens unterzogen. Die vorliegende Arbeit habe ich ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt; die aus fremden Quellen direkt oder indirekt übernommenen Gedanken sind als solche kenntlich gemacht. Die Arbeit ist unter Einhaltung der Regeln guter wissenschaftlicher Praxis der Deutschen Forschungsgemeinschaft entstanden. Bei der Auswahl und Auswertung des Materials sowie bei der Herstellung des Manuskripts habe ich nur Unterstützungsleistungen meines Betreuers erhalten. Weitere Personen waren an der geistigen Herstellung der vorliegenden Arbeit nicht beteiligt. Insbesondere habe ich nicht die Hilfe eines Promotionsberaters in Anspruch genommen. Dritte haben von mir weder unmittelbar noch mittelbar geldwerte Leistungen für Arbeiten erhalten, die im Zusammenhang mit dem Inhalt der vorgelegten Dissertation stehen.

Kiel, den

____

Henning Winterfeld

Scientific Vita

Name:	Henning Winterfeld
Nationality:	German
Date of Birth:	15.04.1988
Place of Birth:	Kiel, Germany

2007 - 2014	Study of Electrical Engineering, Information Technology and Business Management at Kiel University, Germany
2015 - 2019	Research associate at the chair of Nanoelectronics at Kiel University

Publications:

N. Himmel, M. Ziegler, H. Mähne, S. Thiem, **H. Winterfeld** and H. Kohlstedt, ‘Memristive device based on a depletion-type SONOS field effect transistor’, *Semicond. Sci. Technol.*, vol. 32, 2017.

H. Winterfeld, M. Ziegler, H. Hanssen, D. Friedrich, W. Benecke, and H. Kohlstedt, ‘Technology and electrical characterization of MemFlash cells for neuromorphic applications’, *J. Phys. Appl. Phys.*, 2018.

H. Winterfeld, L. Thormählen, H. Lewitz, E. Yarar, T. Birkoben, N. Niethe, N. Preinl, H. Hanssen, E. Quandt, and H. Kohlstedt, ‘A stress sensor based on a silicon field effect transistor comprising a piezoelectric AlN gate dielectric’, J. Mater. Sci. Mater. Electron., 2019.

Patents:

H.Winterfeld, T. Birkoben and H. Kohlstedt, ‘Elektrisches Bauelement und Verfahren zur Sensierung einer mechanischen Verformung’, 5979-012 DE-1, (patent application submitted)

List of Figures

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