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Optimal Design of a Medium-Voltage Grid Analyzer

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Keywords

«High frequency power converter», «Design», «Multilevel converters», «Parallel operation», «Power quality»

Abstract

Much research has been done for medium-voltage applications, where multilevel inverters are challenging classical low-voltage inverters, connected by transformers. Although the decision is very crucial for system costs and performance, comparisons of both approaches are missing, being now introduced for the application of a medium-voltage grid analyzer.

Introduction

The Modular Multilevel Converter (MMC) has become a competitive solution for HVDC applications by using hundreds of IGBT modules to block the required voltages. For low-voltage (LV) applications, the requirements are much lower and two-level or three-level inverter solutions commonly sufficient. These classical solutions can also be easily applied for medium-voltage (MV) applications with the help of step-up transformers. On the other hand, the advanced MMC can be easily designed for MV grids by adapting the number of submodules (SMs). Although all important properties, such as costs, volume, performance and efficiency, are directly influenced by the choice of approach, studies are very scarce.

In this paper, the application of a MV grid analyzer is selected as a study case. The main goal of this application is the determination of the grid impedance depending on the frequency, also varying with the time due to changing conditions. Different to the analysis at LV grids [1, 2, 3], measurements and analysis for MV grids are very scarce [4, 5]. However, the effectiveness of grid services can be enhanced a lot by proper knowledge and analysis of the grid characteristics. The reactive power supply can be perfectly adapted to the exact impedance for effective voltage stabilization. Furthermore, active power filtering can be optimized by taking into account the online measurements [6]. In addition to this, resonance damping can be achieved by knowing the resonances of the grid for stable operation [7].

This paper provides a general design approach for classical and advanced solution and further comparisons to support the choice of the optimal solution.

Medium-Voltage Grid Analyzer

The basic principle of the MV grid analyzer is indicated in Fig. 1a. By the injection of monofrequent currents $I_{\text{exc}}(f)$, an excitation of the grid voltage $V_{\text{exc}}(f)$ is achieved. The relation between achieved voltage excitation and required current injection provides the frequency-dependent grid impedance $Z_{\text{grid}}(f)$. Beside the determination of the grid impedance, the system is able to provide reactive power supply and active power filtering for grid voltage stabilization and harmonic cancellation. The power consumption of the system will be fed from the MV grid.

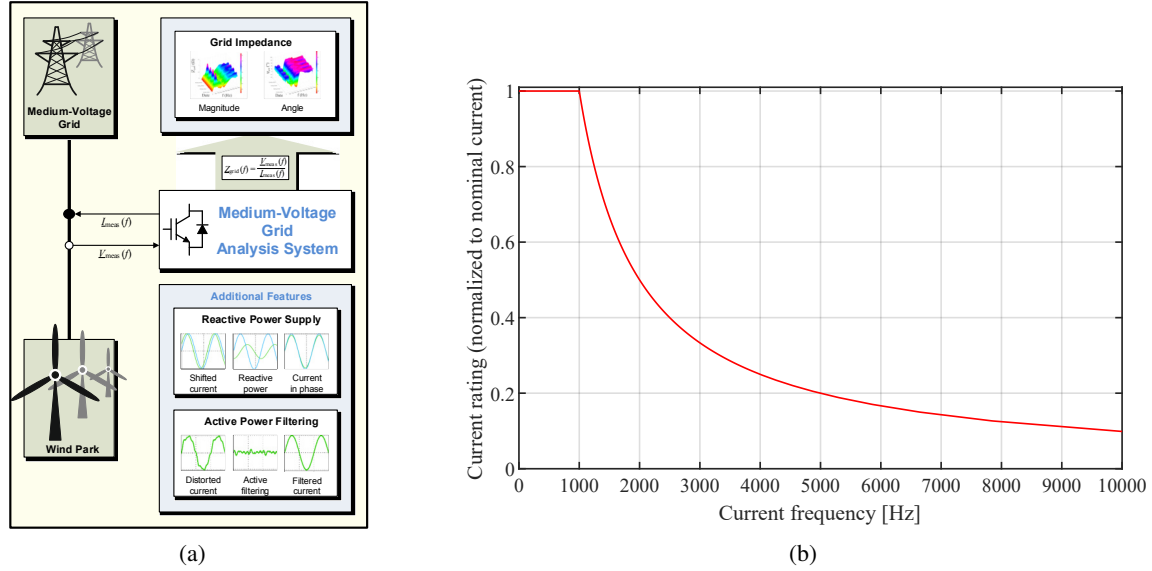


Figure 1: Medium-voltage grid analyzer: a) Scheme, b) Current rating profile.

With the goal of a proper signal to noise ratio based on previous experiences at LV grids [3], a grid voltage excitation of 1 % is aimed in a frequency range between 100 Hz and 10 kHz. MV grids are very stiff compared to LV grids, requiring much higher power for proper excitation. The basic grid characteristics for Germany, Russia and Brazil are summarized in Table I; with short-circuit powers up to 500 MVA. Accordingly, the minimum possible grid impedance is calculated with (1). For simplification an ohmic-inductive behavior is assumed up to $f = 100$ Hz. Accordingly, the angle $\Psi_{\min} = 50^\circ$ corresponds to the highest resistive part in (2) and thus to the lowest inductive part in (3), corresponding to the minimum grid impedance at 100 Hz in (4).

Table I: Basic data for 20 kV medium-voltage grid for the connection of decentralized energy systems [8].

	$V_{g,MV,\Delta}$ [kV]	S_k [MVA]	Ψ [°]
Range	20 ... 22	30 ... 500	50 ... 85

$$Z_{k,MV,\min}^{50\text{Hz}} = \frac{V_{MV,\Delta}^2}{S_{k,\max}} = \frac{(20\text{kV})^2}{500\text{MVA}} = 0.8\Omega \quad (1)$$

$$R_{k,MV} = Z_{k,MV,\min}^{50\text{Hz}} \cdot \cos \Psi_{\min} = 0.514\Omega \quad (2)$$

$$L_{k,MV} = \frac{Z_{k,MV,\min}^{50\text{Hz}} \cdot \sin \Psi_{\min}}{2\pi f_0} = 1.95\text{mH} \quad (3)$$

$$Z_{k,MV,\min}^{100\text{Hz}} = \sqrt{R_{k,MV}^2 + (2\pi f \cdot L_{k,MV})^2} = 1.33\Omega \quad (4)$$

This minimum impedance requires the maximum current injection to achieve a voltage excitation of 1 % and is calculated in (5). The final specifications are adapted to 0.55 % grid excitation, corresponding to 1 % grid excitation for short-circuit powers up to minimum 275 MVA. In this way, the required power injection is almost halved, by covering most of the MV grid connection points. An excitation of 0.55 %

in the worst case is still acceptable and reasonable to limit the costs. Accordingly, the MV grid analyzer has to be designed for a current injection of 47.78 A, corresponding to an injected power of $S_{g,n}^{55\%} = 1.655 \text{ MVA}$.

$$I_{MV,\max}^{100\text{Hz}} = \frac{\Delta V_{\text{exc},\Delta}}{Z_{k,MV,\min}^{100\text{Hz}}} = \frac{0.01 \frac{V_{MV,\Delta}}{\sqrt{3}}}{Z_{k,MV,\min}^{100\text{Hz}}} = 86.82 \text{ A} \Rightarrow I_{MV,\max}^{55\%} = 0.55 I_{MV,\max}^{100\text{Hz}} = 47.78 \text{ A} \quad (5)$$

Due to inductive behaviors of the grid, an increase of the grid impedance is assumed at higher frequencies. Since the frequency behavior of MV grids has not been investigated deeply and due to possible unknown resonances, the system will be designed for the rated current up to frequencies of 1000 Hz to ensure full flexibility. For frequencies higher than 1000 Hz, the current rating is decreasing according to Fig. 1b. The demand of high powers in a high frequency range is linked to different goal conflicts, being directly affected by the choice between classical transformer-connected LV inverters and advanced MV multilevel inverters.

Classical Solution

The connection of LV inverters to the MV grid by step-up transformers leads to very high converter currents, so that paralleling of power modules or inverters becomes useful at a certain point. The transformer needs to be designed for the full frequency range, whereas a low transformer impedance should be achieved to minimize undesired voltage drops especially at high frequencies. For this reason a short-circuit voltage of 2.5 % is aimed, realizable by leading transformer manufacturers. The transformer characteristics can be expressed by (6)-(8).

$$u = \frac{V_{g,LV,\Delta}}{V_{g,MV,\Delta}} \quad (6) \quad Z_{k,\text{trafo}} = u_k \cdot \frac{V_{g,LV,\Delta}^2}{S_{g,n}^{55\%}} \quad (7) \quad L_{k,\text{trafo}} = \frac{Z_{k,\text{trafo}}}{2\pi f_0} \quad (R_{k,\text{trafo}} \approx 0) \quad (8)$$

The generation of current frequencies up to 10 kHz is linked to very high switching frequencies. In this context, the dead time needs to be minimized by accepting fast switching transients. However, high voltage slopes result in high stress for the transformer windings. A du/dt filter will be included to decrease the voltage slope by a factor above 8. The filter design is oriented to the du/dt filter FN 5060 from Schaffner [9], corresponding to $L_{\text{filter}} = \frac{6.36 \mu\text{H}}{1000 \text{ A}} \cdot I_{LV,n}$, depending on the nominal current $I_{LV,n}$. The filter inductance also leads to a reduction of the current ripple. The overall cable inductance related to LV side is approximated by $L_{\text{cable}} = 0.7 \mu\text{H}$.

For the generation of currents up to 10 kHz, switching frequencies up to 30 kHz are demanded. The power unit and cooling system should be designed for switching frequencies of $f_{\text{sw}} = 15 \text{ kHz}$ at nominal current to limit occurring current ripples. For this purpose, 1700 V Si-based IGBT modules are not suitable due to very high switching energies. Even if silicon carbide technology would allow required switching frequencies at high voltage levels, the additional costs would not be reasonable at the present time. On the other hand the selection of 600 V Si-based IGBT modules would lead to huge currents on LV side for classical two- or three-level topologies. These are the reasons why the focus is put on standard 1200 V Si-based IGBT modules.

The amount of switching losses is not only affected by the voltage level but also by the inverter current. In order to reduce the current rating of each module and to allow harmonic cancellation by interleaved modulation, the paralleling of several inverters is recommended [10]. Particularly for interleaved operation the separation of dc capacitor banks is useful to suppress possible circulating currents between the inverters.

The voltage design of the inverters needs to be done carefully and is directly linked to the required winding ratio of the transformer. In general, the phase voltage amplitude of conventional inverters can be

expressed by (9), whereas third harmonic injection allows an increase of the modulation range according to (10). The maximum voltage decrease due to dead time generation is approximated by 5 % according to (11). The inverter needs to compensate the transformer input voltage and the voltage drops across transformer, filter and cable impedances. The transformer input voltage $v_{g,LV}$ can increase by 1 % due to the grid voltage excitation and also due to possible grid voltage variations, taken into account in (12). The voltage amplitude across the transformer impedance is expressed by (13). Furthermore, the voltage amplitude across the filter and cable inductance is provided in (14) and (15), respectively. In addition to the voltage drops, a voltage reserve for proper control and modulation is taken into account in (16), proofed by simulation.

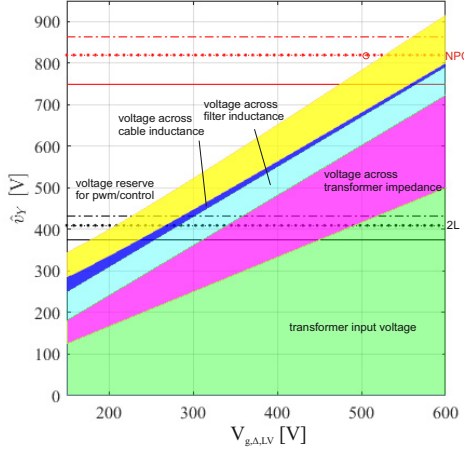


Figure 2: Voltage design for classical solution ($f = 1000\text{Hz}$).

Fig. 2 shows the occurring voltages at nominal operation with a current frequency of 1000 Hz. Two classical inverter topologies are considered, namely the two-level inverter and the three-level Neutral-Point Clamped inverter (NPC). The DC voltages are limited to 62.5 % for protection due to possible overvoltages in transient conditions, corresponding to 750 V for the two-level inverter and 1500 V for the NPC inverter.

The three-level NPC inverter allows a transformer input voltage of 510 V and is the preferred choice compared to the two-level inverter only allowing 200 V, corresponding to a reduction of more than 60 %. A transformer input voltage of 510 V corresponds to a LV current of 1873.74 A and a converter rating of 2985.79 kVA according to (17) and (18), respectively.

$$I_{LV,n} = \frac{V_{g,MV}}{V_{g,LV}} \cdot I_{MV,max} = 1873.74 \text{ A} \quad (17)$$

$$S_{conv,n} = \sqrt{3} \cdot 920 \text{ V} \cdot 1873.74 \text{ A} = 2985.79 \text{ kVA} \quad (18)$$

The dc capacitors need to be designed for the nominal current at minimum frequency. The ripple can be calculated by (19) whereas the capacitance of the system can be determined by (20). By defining a maximum voltage ripple of $\pm 10\%$, an overall capacitance of 28.36 mF is obtained for a grid frequency of $f_0 = 50\text{Hz}$.

$$\frac{\Delta V_{dc}}{2} = \frac{3V_{g,LV,\lambda} \cdot I_{LV}}{2\pi \cdot V_{dc,ref} \cdot C_{dc} (f - f_0)} \quad (19)$$

$$C_{dc} = \frac{3V_{g,LV,\lambda} \cdot I_{LV,n}}{2\pi \cdot V_{dc,ref} \cdot \frac{\Delta V_{dc}}{2} (f - f_0)} \quad (20)$$

For a current frequency of 1000 Hz the DC voltage can be approximated as constant since the oscillating energy is very low. Nevertheless, the injection of nominal current at 1000 Hz is the worst case for the

voltage design since voltage drops across the overall inductance L_{total} (transformer, inductor, cabling) are significantly higher, needed to be compensated by the inverter.

The described system has been realized with two parallel transformers and six parallel NPC inverters. Fig. 3a shows both containers with areas for inverters, transformers, measuring technique and MV switch gear. Furthermore, the cabinet of one NPC inverter and one MV transformer is depicted in Fig. 3b and 3c for further illustration.

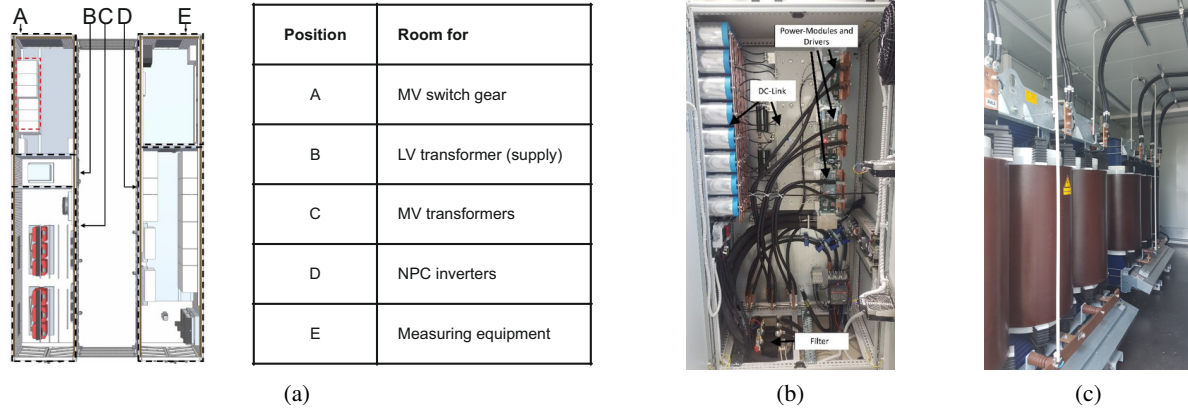


Figure 3: Final realization: a) Containers (length: 12.2 m), b) Cabinet of one NPC inverter, c) Medium-voltage transformer.

MMC-based MV Grid Analyzer

In contrast to conventional two- or three-level inverters, the MMC can be designed for MV connection by standard components. IGBT modules with 1700 V breakdown voltage can be selected to limit the number of components. In this case, the number of SMs is still high enough to allow very low switching frequencies. IGBT modules with 3.3 kV breakdown voltage are not further considered in this paper due to limited availability and high costs at the market.

The MMC design is oriented to [11], [12]. Different to the introduced design of the classical solution, the voltage design for the MMC needs to be done for nominal current at 100 Hz instead of 1000 Hz. This is caused by the maximum capacitor ripple at 100 Hz, being much higher than possible voltage drops at 1000 Hz, since the converter current is low on MV level. Due to the missing transformer, the converter needs to be able to block the MV grid, possible voltage variations of 1 % and additional possible 1 % due to the grid excitation, summarized in (21). Furthermore, voltage drops across the arm inductances, carefully selected with $L_{\text{arm}} = 3 \text{ mH}$, need to be taken into account, expressed in (22).

$$1.02 \hat{v}_{g, \text{MV}, \lambda} = 1.02 \cdot \sqrt{2} \cdot \frac{V_{g, \text{MV}, \Delta}}{\sqrt{3}} = 16656.53 \text{ V} \quad \hat{v}_{L, \lambda} = \sqrt{2} \cdot 2\pi f \cdot L_{\text{arm}} \cdot i_{\text{MV}, \text{max}} = 127.37 \text{ V} \quad (22)$$

(21)

For simplification, the effective cable inductance is assumed to be the same as for the classical solution according to (23). In contrast to the classical LV solutions, voltage drops across the cable impedance are not crucial issue at MV level with relatively low currents. Based on the converter voltage in (10), the minimum required dc link voltage can be calculated by (24).

$$\hat{v}_{\text{cable}, \lambda} = \sqrt{2} \cdot 2\pi f \cdot L_{\text{cable}} \cdot I_{\text{MV}, \text{max}} = 0.3 \text{ V} \quad V_{\text{dc}, \text{min}} = \sqrt{3} \cdot (1.02 \hat{v}_{g, \text{MV}, \lambda} + \hat{v}_{L, \lambda} + \hat{v}_{\text{cable}, \lambda}) = 29071.09 \text{ V} \quad (23) \quad (24)$$

The maximum capacitor voltage is selected by 62.5 % of the IGBT breakdown voltage, corresponding to $V_{C,\max} = 1062.5 \text{ V}$. For maximum $\pm 10\%$ capacitor voltage ripple, the minimum capacitor voltage is calculated in (25). The number of minimum SMs is calculated in (26).

$$V_{C,\min} = \frac{V_{C,\max}}{1.1^2} = 878.1 \text{ V} \quad (25)$$

$$n_{\min} > \frac{V_{DC,\min}}{V_{C,\min}} = 33.1 \quad (26)$$

In analogue to the classical solution, an increased voltage level of 14.7 % is provided for pwm and control, corresponding to 37.9 SMs. Thus, taking into account two additional SMs per arm for possible damages, the MMC is designed with 40 SMs per arm. A downscaled prototype with four SMs per arm has been realized, depicted in Fig. 4.

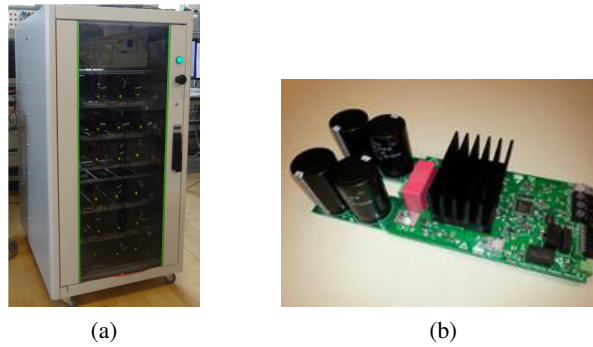


Figure 4: MMC prototype: a) Cabinet with 24 SMs, b) Board of one SM.

Comparison

The design properties for both presented solutions are summarized in Table II. On the one hand, six parallel NPC inverters are considered to reduce the current rating of one inverter to a reasonable value. On the other hand, the MMC is designed for the half grid current and an additional reserve of 10 % for the circulating current.

The MMC avoids the use of bulky transformers, however much more semiconductors are required to block the high grid voltages. Nevertheless, the overall power rating of semiconductors is lower than for the classical solution of NPC inverters, particularly valid for the diodes. This is especially caused by the high LV currents, resulting in high voltage drops linked to a significant converter overdesign.

Although the NPC inverters provide a line-to-line inverter voltage of 920 V, the transformer input voltage needs to be decreased to 510 V. Thus, only 55.4 % of the nominal power can be injected to the grid. The injection of lower frequencies would allow much higher transformer input voltage, nevertheless the transformer needs to be designed for the worst case (maximum voltage drops) due to its stiff characteristics.

On the other hand, the MMC only needs to compensate small voltage drops due to the very low current at MV level, almost non-relevant for the voltage design and the corresponding number of SMs. In addition to this, the MMC provides much more voltage levels in comparison to parallel NPCs due to the high number of SMs.

The MMC behavior is illustrated in Fig. 5, achieving a switching frequency of ca. 100 Hz with a capacitance of 1 mF per SM. The installed capacitance is significantly higher than for the classical solution, however can be reduced by applying a PWM method with more homogenous switching profiles at higher switching frequencies [13].

The performance of both solutions is illustrated in Fig. 6-8 for nominal current injections up to 10 kHz. Although filter effort and switching frequencies are minimized, the current waveforms are sufficient for both solutions due to the high number of available voltage steps.

Table II: Comparison of classical and advanced solution.

	Classical Solution	Advanced Solution
Transformer	yes	no
Breakdown voltage (semiconductors)	1200 V	1700 V
Nominal current (semiconductors)	312.29 A	26.28 A
Number of cells (per phase)	6 (NPC)	80 (Half-bridges)
Number of IGBTs	72	480
Number of Diodes	108	480
Number of Inductors (three-phase)	6	2
DC Capacitance of each inverter / each cell	4.73 mF	1 mF
Stored energy in capacitors	31.91 kJ	135.47 kJ
Power rating of IGBTs	26.98 MVA	21.44 MVA
Power rating of Diodes	40.47 MVA	21.44 MVA

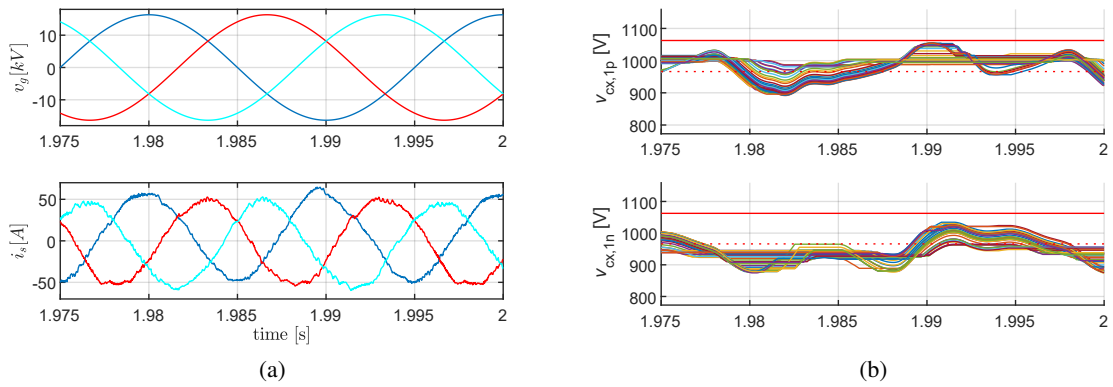


Figure 5: MMC simulations at 100 Hz (staircase modulation): a) Grid voltages and grid currents, b) Capacitor voltages in one leg.

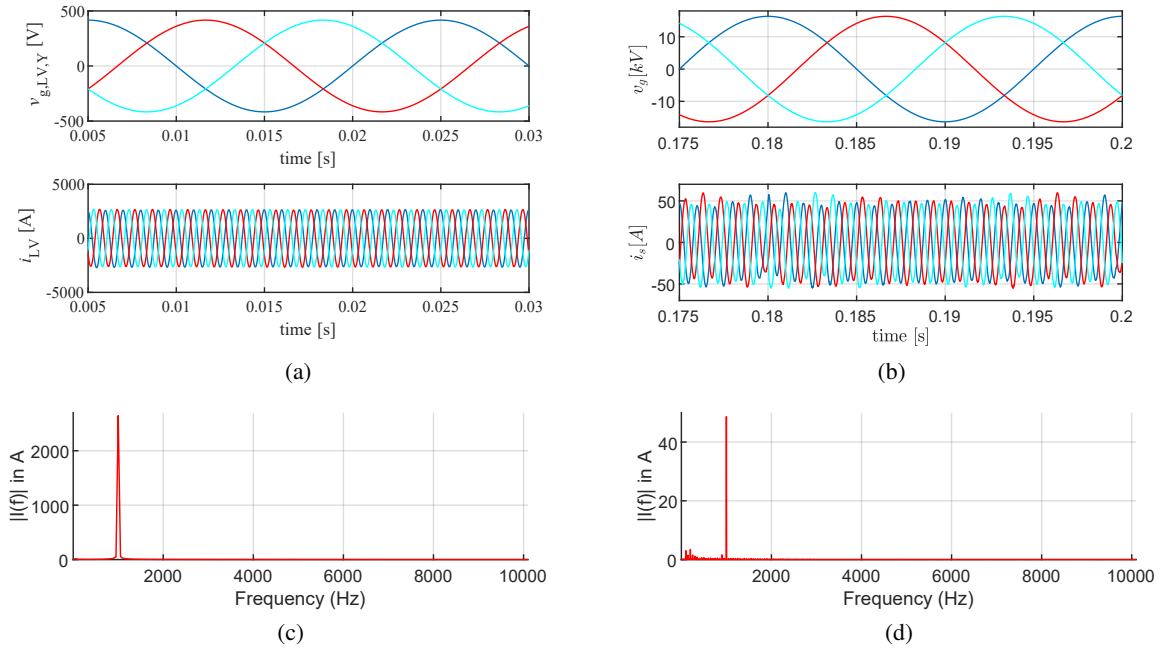


Figure 6: Current injection at 1000 Hz: a) Classical solution of parallel NPC inverters (phase-shifted PWM, $f_{carrier} = 15$ kHz), b) Advanced solution: MMC (staircase modulation).

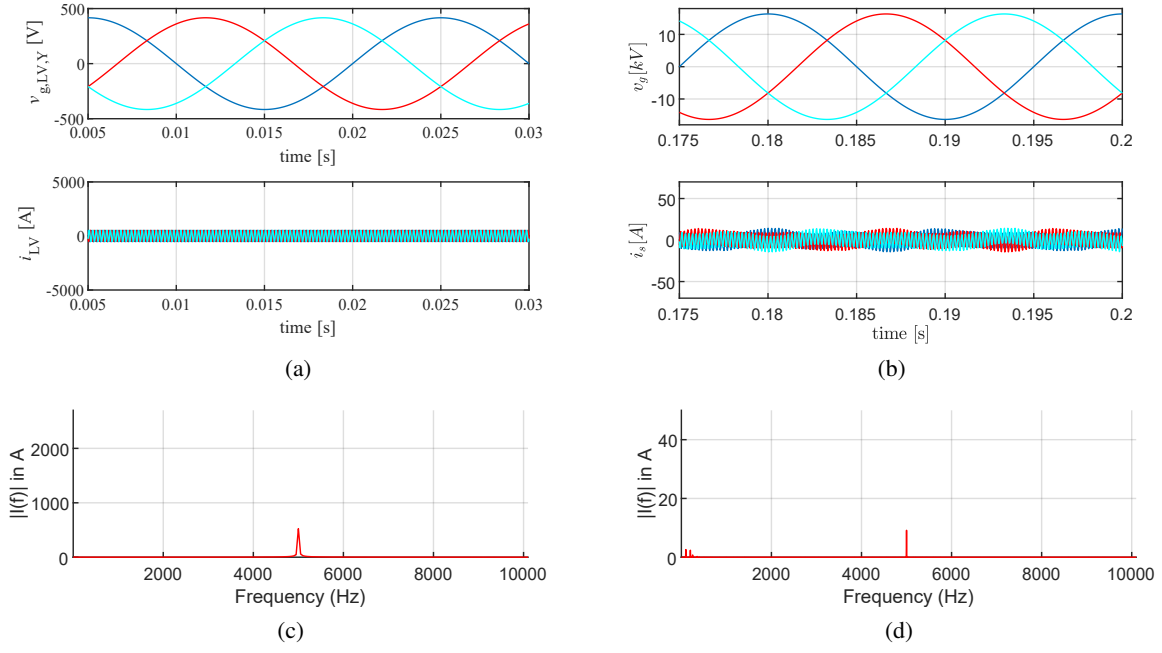


Figure 7: Current injection at 5000 Hz: a) Classical solution of parallel NPC inverters (phase-shifted PWM, $f_{\text{carrier}} = 30\text{kHz}$), b) Advanced solution: MMC (staircase modulation).

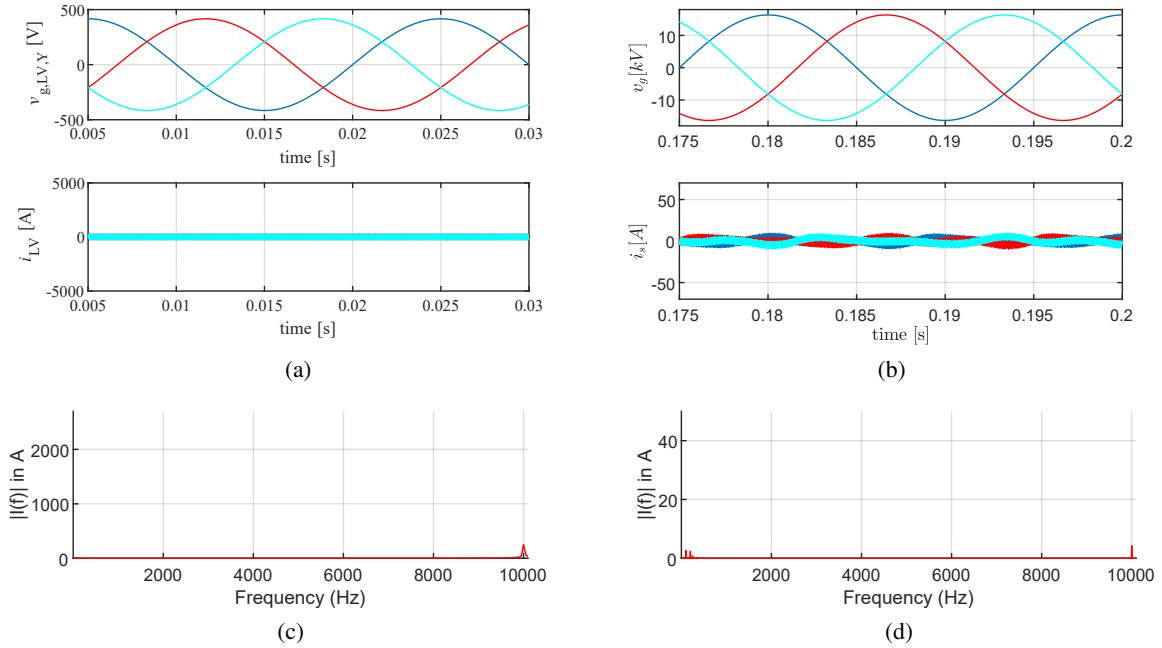


Figure 8: Current injection at 10000 Hz: a) Classical solution of parallel NPC inverters (phase-shifted PWM, $f_{\text{carrier}} = 30\text{kHz}$), b) Advanced solution: MMC (staircase modulation).

Conclusion

In this digest, a MV grid analyzer has been designed for both a classical solution and an advanced solution. Among the classical solutions with step-up transformers, it has been demonstrated that the three-level NPC inverter is the preferred choice. As advanced solution the MMC has been selected, providing excellent waveform qualities due to high number of voltage levels. Although the NPC can be designed with a much lower number of semiconductors, the overall semiconductor power rating can be

significantly reduced by an MMC due to limited voltage drops. In addition to this, the use of bulky and specially designed transformers can be avoided.

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