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# Current Limitation Strategy For Grid-Forming Converters Under Symmetrical And Asymmetrical Grid Faults

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***Abstract*— The potentials of grid-forming (GFM) converters in stabilizing a power system with high penetration of power electronics-based generation have been recently investigated. Due to their intrinsic behaviour of voltage source behind impedance, a crucial aspect of any GFM converter control strategy will be the handling of fault-ride through (FRT) scenarios. This paper proposes a FRT strategy for GFM converters, which respects the converter hardware limitations (i.e. current limitations) even under sever fault conditions, while maintaining GFM behavior before, during, and after the fault. The presented strategy addresses both symmetrical and asymmetrical faults, and is compliant with recently proposed draft grid codes requirements published by the British system operator NGESO. The issues related to FRT of GFM converters are first discussed in detail, and a comprehensive overview on the solutions proposed in the literature is reported. Then a proper strategy is presented, and its effectiveness is demonstrated by means of simulations and Power-Hardware-in-the-Loop (PHIL) measurements in a laboratory environment.**

## I. Introduction

STUDIES have investigated the potential benefits of GFM converters and their capability of stabilizing a power system with high penetration of power electronics-based generation [1]. The concept of GFM converters has been originally introduced for micro- and islanded grid applications [2], [3], and only recently this has been re-evaluated for applications in wide interconnected power networks. Discussions in different countries about the need for introducing additional converter performance requirements in future grid codes have been initiated in the last years. To cite few examples, the European Network of Transmission System Operators for Electricity (ENTSO-E) established a working group on High Penetration of Power Electronic Interfaced Power Sources (HPoPEIPS) [4] in 2017, while in early 2018 the British SO (NGESO) convened an Expert Group (EG) on virtual-synchronous machines (VSM) associated with the Grid Code Consultation (GC0100) [5], involving members from the wind, solar, and HVDC industry, consultants, and academia.

Differently from state-of-the-art grid-following (GFL) converters, which regulate active and reactive power injection by controlling active and reactive currents, GFM converters control power injection by regulating the magnitude and the phase of the voltage at the point of common coupling (PCC). Nowadays, several GFM control strategies can be found in the literature, whose common characteristic is the emulated behaviour of a voltage source behind impedance [6]-[8]. As a consequence, the response of GFM converters to grid faults is substantially different from the one of their counterpart GFL converters, due to the fact that the converter can react almost instantaneously to any grid event, without the need for detecting first the actual operating condition. Even though this prompt reaction is superior to the one of a GFL converter, and hence highly attractive for SOs, the rapid growth of converter currents caused by a severe fault might jeopardize the integrity of the converter hardware components.

To this extent, several FRT strategies for GFM converters have been proposed in the literature [8]-[25]. However, most of them either address only symmetrical fault conditions, or the proposed structures switch from GFM mode to standard vector current control mode at the occurrence of a fault, hence without fully utilizing the potentials of GFM converters under such operating conditions. This paper proposes a FRT strategy for GFM converters, which allows emulating the behaviour of a voltage source behind impedance before, during, and after the fault, while respecting the converter hardware limitations. Furthermore, the proposed control strategy complies with the most up-to-date draft grid codes elaborated by the EG established by NGESO, which require fully utilizing the potentials of GFM converters during faults [5].

The outline of the paper is the following: in Section II, the behaviours of GFM converters and of the state of-the-art GFL converters during grid faults are first compared, then the actual draft specifications regarding the FRT behavior of GFM converters are introduced, along with a comprehensive overview on the solutions already reported in the literature. A current limitation strategy for GFM converters complying with the actual draft specifications is presented in Section III, and the effectiveness of the proposed solution is verified first by means of simulations in Section IV, then in Section V through experimental tests in a laboratory environment. Finally, Section VI is dedicated to the conclusions.

## II. Behaviour of GFM converters during faults

Fig.1 (a) and (b) show the typical representations of GFL and GFM converters adopted in the literature [3]. The former is usually represented by means of a current source with a high

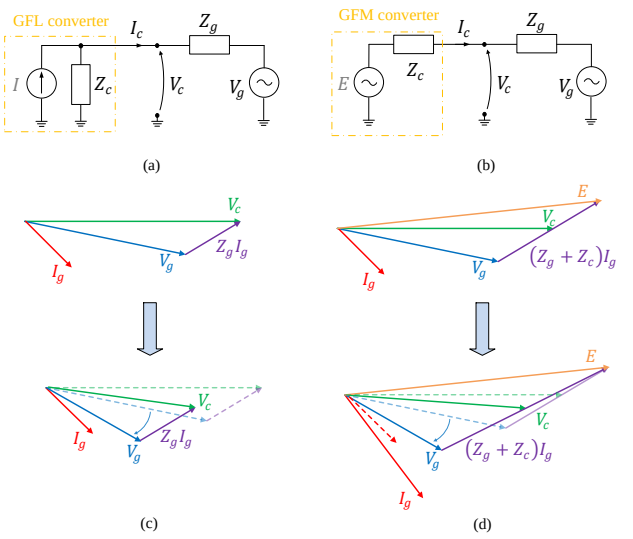



Figure 1: GFL converter: (a) simplified representation, (c) phasor diagram of the reaction to a grid voltage variation; GFM converter: (b) simplified representation, (d) phasor diagram of the reaction to a grid voltage variation [29].

parallel impedance, while the latter is commonly indicated as a voltage source with series impedance. Several studies have shown the beneficial effects of GFM converters compared to their counterpart in stabilizing a system with high penetration of converter-based generation [1]. Among their characteristics, the capability of providing damping of system oscillations [26], and the contribution to small-signal stability [27], [28], have been recently addressed in the literature. However, one of the crucial aspects identifying the differences between GFM and GFL converters is related to their behaviour during grid faults, and it is schematically explained in Fig.1 [29].

During normal operation, a GFL converter regulates active and reactive power injected into the grid by controlling active and reactive currents, requiring therefore a dedicated unit for the calculation of the phase displacement between the currents injected by the converter and the grid voltage measured at the PCC. The phasor diagram in Fig. 1 (c), shows the typical reaction of a GFL converter to a variation of the voltage, where due to its intrinsic current source behavior, it tries maintaining the current phasor $\mathbf{I}_g$ constant in terms of magnitude and phase, while a synchronization loop and an outer power loop calculate amplitude and phase of the new reference currents for the injection of the required amount of reactive power according to the grid codes. Just to have an idea about the time constants at stake, the actual German grid codes require reactive power injection within 30 *ms* after fault detection [30].

On the contrary, due to its intrinsic behavior of a voltage source behind impedance, the reaction of a GFM converter to the same grid event will be to maintain the inner voltage phasor $\mathbf{E}$ constant, causing therefore an almost instantaneous variation of the phasor current $\mathbf{I}_g$, as schematically indicated in Fig. 1 (d).

### A. *Actual status of the draft grid codes*

Upon performing system studies, the British system operator NGESO identified a number of potential challenges associated with increased penetration of power-electronics-based generation in the British power system. In April 2018, an EG has been set up, so as to discuss enhanced converter control strategies that would lead to performances of the converter emulating some characteristics of synchronous machines, among others fast fault current injection during faults. At the end of the second stage of the EG (December 2019), the following requirements were included in the draft GFM specifications for Great Britain (GFC-GB) [5]:

**(i)** The converter shall be capable of operating as a voltage source behind a reactance over a frequency band of 5 Hz to 1 kHz before, during, and after the fault.

**(ii)** The converter shall have a short-circuit current contribution of at least 1.5 pu of converter rating.

**(iii)** During a fault or voltage depression below 0.85 pu, the phase, magnitude and frequency of the voltage source will remain fixed at the pre-fault values. In the event that the resulting fault current would exceed 1.5 pu, a reduced fault current limited to 1.5 pu can be supplied, however its phase angle relative to the voltage source must be equivalent to the phase angle of the higher fault current.

**(iv)** In the event of a fault, the converter shall be able of supplying reactive power as soon as possible and within 5 ms of the voltage disturbance.

**(v)** The converter shall be capable of absorbing an unbalanced current of up to 2% without modifying the voltage source waveform.

### B. *Overview on FRT control strategies for GFM converters*

Various FRT strategies for GFM converters can be found in the literature. However, due to the lack of clear specifications regarding the behaviour of GFM converters during faults, several techniques have been proposed, which in most of the cases mainly focus on limiting converter currents and preventing from instability issues, yet without reproducing a GFM behaviour also during the fault. For example, the solutions adopted in [8], [9] is to switch to vector controlled mode as soon as a grid fault is detected. However, also in this case, a proper current limitation technique should be implemented, and is often achieved by saturating the PI controllers of the cascaded control loops [10]-[12]. As a consequence, appropriate techniques for avoiding the classical phenomena of ”wind-up” or ”latch up”, typical of such operating conditions should be adopted. A valuable alternative to such solution is represented by the use of virtual impedances, consisting of limiting the converter reference voltage according to fictitious variable impedance, in order to avoid the generation of excessively high current reference signals for the inner current control loop [13]-[15].

Early investigations of FRT strategies for virtual synchronous machines (VSMs) have been presented in [16], [17].

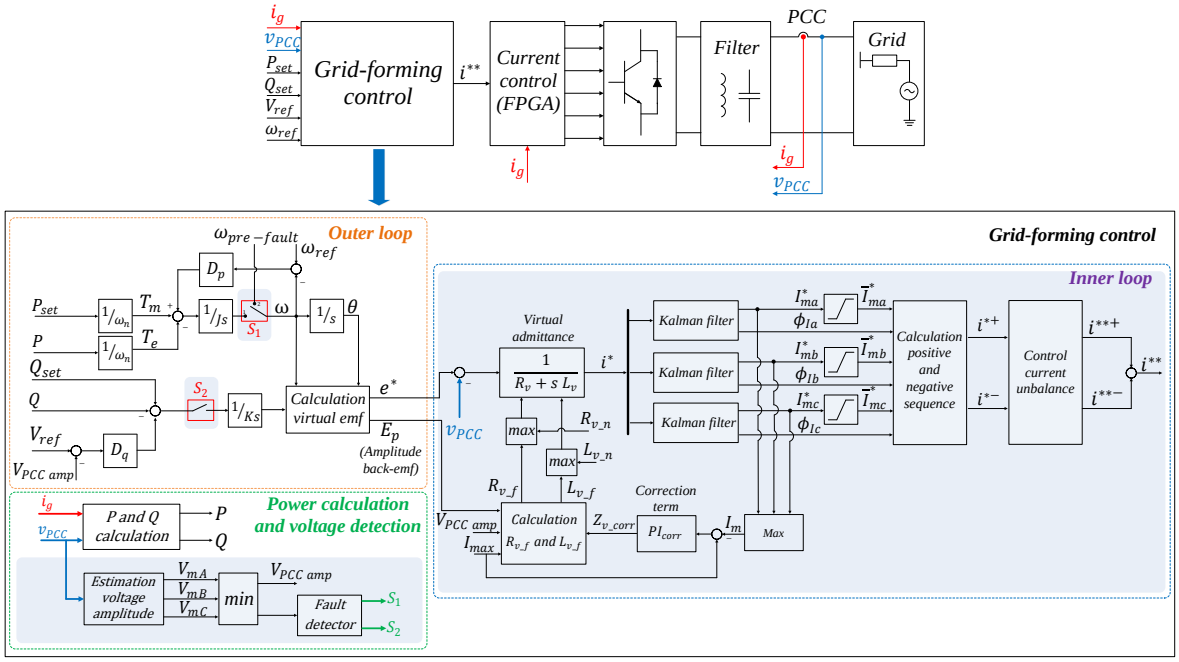



Figure 2: Scheme of the proposed control strategy.

The limitation of control states adopting non-linear control techniques has been proposed in [18] for the synchronverter, however without solving directly the issue related to converter overcurrents, but simply ensuring boundness of frequency and voltage without requiring saturation units. A comprehensive analytical calculation of the inrush currents of a synchronverter according to control parameters, and caused by symmetrical and asymmetrical grid faults has been presented in [19] and [20], respectively. The solution proposed in [19], consists of activating an inner current control loop, implemented by means of an hysteresis current controller as soon as the fault condition is detected. The reference converter currents are then calculated by means of a virtual impedance and active and reactive power setpoint are set so as to fulfill grid codes, however requiring detection of the grid angle. In [21], FRT and current limitation of GFM converters under asymmetrical grid faults are investigated. An auxiliary control for the negative sequence component is introduced at the occurrence of an asymmetrical fault, involving a dedicated unit for estimation of positive and negative sequence of the grid voltage. Nevertheless, only positive sequence injection is considered, making therefore the control inappropriate for fulfilling some stringent grid codes worldwide that require injection of negative sequence currents during asymmetrical faults [30]. To this extent, [22] proposes the modification of the standard synchronverter control structure by adding a cascaded inner current reference generator and an inner PI-based current control loop, in order to calculate proper converter currents according to the FRT strategies for GFL converters reported in [23], hence without fully utilizing the potentials of a GFM converter during faults.

In [24], the problems related to the saturation of the outer control loop of a GFM converter occurring when limiting converter currents are investigated, and a current limitation procedure, that prevents the converter from instability issues by means of a proper coordination between the outer and the inner control loops, is presented. Nevertheless, the proposed control does not deal with asymmetrical faults, which represents instead the most common condition in the field. Finally, current limitation by means of an adaptive virtual impedance is presented in [25], which limits the maximum amplitude of the converter currents by properly restraining positive and negative sequence current components. However, several filters are implemented in the control, degrading the dynamic response of the converter. Moreover, only simulation results are reported in the paper, missing an experimental proof of the proposed concept.

## III. Proposed FRT Strategy

In this section, a robust solution for preventing the converter from the risk of overcurrents and instability issues during faults is proposed. The core of the proposed control structure is the inner loop, which allows controlling directly converter currents, yet reproducing the behaviour of a voltage source behind impedance before, during, and after the fault, hence complying with the specifications listed in the previous section.

The structure of the proposed control is reported in Fig. 2. The outer loop shown in the figure, is represented by the well-known VSM implementation known as synchronverter [6], but it might be replaced by any other GFM control structure among the numerous already proposed in the literature, e. g. [7], [8]. A dedicated unit in charge of the estimation of the voltage amplitude at the PCC is introduced, which detects

a fault condition by considering each phase separately. A controller activates the switches indicated in the figure with $S_1$ and $S_2$, as soon as the lowest value among the three phases falls below the threshold defined by the specifications. As a consequence, the magnitude and the frequency of the reference back-emf voltage $e^*$ calculated by the outer loop are locked to their pre-fault values, as requested in **(iii)**. The pre-fault value of the frequency $\omega_{pre-fault}$ can be obtained either by means of a dedicated unit like a frequency-locked-loop (FLL) [23], or by a proper feedback of the internal quantity $\omega$.

A variable virtual admittance is implemented in the inner control loop [7], whose inductive and resistive components $L_v$ and $R_v$ are dynamically modified according to the operating conditions. The effects of virtual impedance on the robust stability of VSMs have been recently addressed in in [31], and the concept of virtual admittance represents a practical solution for virtually modifying the output impedance of a GFM converter without the need for performing the derivative of the measured currents, representing instead the commonly adopted solution in the literature [15]. Independent single-phase currents $i^*$ are calculated directly from the comparison between the instantaneous values of the measured voltages at the PCC ($v_{PCC}$) and the virtual back-emf voltages $e^*$ calculated in the outer loop, according to:

$$i^* = \frac{v_{PCC} - e^*}{R_v + s\ L_v}. \tag{1}$$

These would correspond to the currents flowing into the grid when the converter is replaced by ideal three-phase voltages sources behind resistive-inductive elements. Under normal operation, $L_v$ and $R_v$ are set to the nominal values $L_{v\_n}$ and $R_{v\_n}$, properly chosen during the design procedure [31]. According to the magnitude of the lowest single-phase measured voltage $V_{PCC\ amp}$ measured by the outer loop, a current limitation controller calculates the magnitude of the impedance $Z_{v\_f}$, necessary for limiting the highest single-phase reference current to the maximum value $I_{max}$ when the converter is replaced by three voltage sources reproducing the voltages $e^*$ calculated by the outer loop. This is obtained as follows:

$$\begin{cases} Z_{v\_f} = \left(E_p - V_{PCC\ amp}\right)/I_{max} + Z_{v\_corr}; \\ R_{v\_f} = Z_{v\_f}/\sqrt{X_{ratio}^2 + 1}; \\ L_{v\_f} = \left(X_{ratio} \cdot R_{v\_f}\right)/\omega_n; \end{cases} \tag{2}$$

where $L_{v\_f}$ and $R_{v\_f}$ respectively indicate the inductive and resistive components of the impedance $Z_{v\_f}$, $X_{ratio}$ indicates the $X/R$ ratio, and $\omega_n$ is the nominal grid frequency. At the occurrence of a fault, the highest value between the nominal quantities $L_v$ and $R_v$, and $L_{v\_f}$ and $R_{v\_f}$, are forwarded to the virtual admittance subsystem, so as to limit the output reference currents of the converter to the maximum allowed amplitude. However, since for the calculation of the virtual impedance $Z_{v\_f}$ only the amplitudes of the voltages $E_p$ and $V_{PCC\ amp}$ are taken into account, a correction term $Z_{v\_corr}$ compensates for the lack of exact information about the phase displacement between the two voltages, and is implemented by means of a PI controller. The discrete implementation of the variable virtual admittance is obtained according to the following equation:

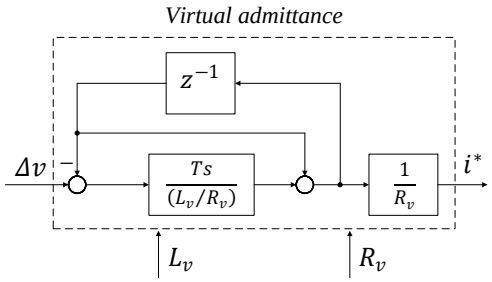


Figure 3: Discrete implementation of the virtual admittance.

$$Y_v(z) = \frac{T_s}{z\ L_v - (L_v + R_v T_s)}, \tag{3}$$

where $T_s$ represents the sample time, and a scheme of the discrete implementation of the virtual admittance is reported in Fig. 3, which allows easily modifying the parameters of the virtual admittance according to the operating condition.

A Kalman filter is implemented in order to detect the magnitude and the phase of each current separately [32]. These are indicated in the figure as $I_{mX}$ and $I_{\phi X}$, with $X = \{a,b,c\}$, and the filter equations are reported below:

$$\mathbf{x}(n+1) = \Phi(n)\mathbf{x}(n) + \mathbf{w}(n), \tag{4}$$

where $\mathbf{x}(n)$ is the state-vector and $\Phi(n)$ is the state transition matrix defined as:

$$\Phi(n) = \begin{bmatrix} \cos(\omega T_s) & -\sin(\omega T_s) \\ \sin(\omega T_s) & -\cos(\omega T_s) \end{bmatrix}, \tag{5}$$

with $\omega$ representing the frequency of the input signal and $T_s$ is the time step. The observation (or measurement) model is assumed to be of the form:

$$\mathbf{z}(n) = \mathbf{H}(n)\mathbf{x}(n) + \mathbf{v}(n), \tag{6}$$

where $\mathbf{H}(n)$ represents the measurement matrix, and $\mathbf{w}(n)$ and $\mathbf{v}(n)$ are the model and the measurement vectors, both assumed to be white sequence with known covariance matrices $\mathbf{Q}(n) = Q_0\mathbf{I}$ and $\mathbf{R}(n) = R_0\mathbf{I}$, respectively, and with $\mathbf{I}$ indicating the identity matrix. The filter is implemented by means of the following equations:

$$\widehat{\mathbf{x}}^-(n) = \Phi(n-1)\widehat{\mathbf{x}}(n-1), \tag{7}$$

$$\mathbf{P}^-(n) = \Phi(n-1)\mathbf{P}(n-1)\Phi^T(n-1) + \mathbf{Q}(n), \tag{8}$$

$$\mathbf{K}(n) = \mathbf{P}^-(n)\mathbf{H}^T(n)\left[\mathbf{H}(n)\mathbf{P}^-(n)\mathbf{H}^T(n) + \mathbf{R}(n)\right]^{-1}, \tag{9}$$

$$\widehat{\mathbf{x}}(n) = \widehat{\mathbf{x}}^-(n) + \mathbf{K}(n)\left[\mathbf{Z}(n) - \mathbf{H}(n)\widehat{\mathbf{x}}^-(n)\right], \tag{10}$$

$$\widehat{\mathbf{P}}(n) = \left[\mathbf{I} - \mathbf{K}(n)\mathbf{H}(n)\right]\mathbf{P}^{-}(n). \tag{11}$$

The notation $\widehat{\mathbf{x}}(n)$ indicates the estimation of $\mathbf{x}(n)$, $\mathbf{K}(n)$ represents the Kalman gain, and $\mathbf{P}(n)$ is the covariance matrix of the estimation error. The quantities indicated with $\widehat{\mathbf{x}}^{-}1(n)$ and $\mathbf{P}^{-}(n)$ represent estimations using information at the instant $n-1$.

The reference currents $i^{**}$ forwarded to the most inner current control loop are calculated reconstructing the three single-phase signals from the information about the respective magnitude and phase. First, the magnitude of each current is limited to the value $I_{max}$ by means of a saturation unit. Then positive and negative sequence components of the three-phase signals are calculated as follows [23]:

$$\begin{bmatrix}\mathbf{I}^{*+}\\ \mathbf{I}^{*-}\end{bmatrix} = \frac{1}{3}\begin{bmatrix}1 & \alpha & \alpha^2\\ 1 & \alpha^2 & \alpha\end{bmatrix}\begin{bmatrix}\bar{I}^{*}_{ma}e^{j\phi_{Ia}}\\ \bar{I}^{*}_{mb}e^{j\phi_{Ib}}\\ \bar{I}^{*}_{mc}e^{j\phi_{Ic}}\end{bmatrix}; \tag{12}$$

where $\alpha = e^{j2/3\pi}$ is the Fortescue operator [23], and $\bar{I}^{*}_{mX}$, with $X = \{a,b,c\}$, represents the saturated amplitude of the respective single-phase current. It can be noticed, that the calculation of positive and negative sequence current components is performed by means of algebraic equations, which do not involve any calculation time delay.

Further measures can be taken in order to limit the ratio between positive and negative sequence current component, as also indicated by the grid codes in **(v)**. These are introduced in the block indicated as "control current unbalance" indicated in Fig. 2, and can be simply implemented by limiting the magnitude of the negative sequence current to a certain percentage of the positive sequence component.

### A. Current control loop

According to the requirements on the control bandwidth specified in **(i)**, an extremely fast current control is necessary. In fact, considering that in order to reproduce the desired behaviour up to the required frequency range of 1 kHz, the inner current control loop should have a bandwidth in the range of 2-3 times higher than that, the time constant of the inner current control loop can be calculated considering the relation between rise-time and bandwidth of a first-order system [33]:

$$t_r = \frac{ln\ 9}{BW}, \tag{13}$$

with $t_r$ indicating the rise-time and $BW$ the bandwidth of the control. According to (13), the rise-time of the inner current control loop should be approximately in the range of $\approx 0.7ms$.

In order to reduce the time delay of the current control loop, different possible solutions can be adopted. Model predictive control based approaches, e. g. deadbeat control [23], might be good candidates [34]. However, due to the susceptibility of model predictive controllers to the knowledge of filter and grid parameters, an adaptive hysteresis current control has been implemented by means of an FPGA board [36]. This solution allows achieving extremely high bandwidth and ensures that the converter currents do not overcome the limitations imposed the hardware components, under the assumption that their reference values are properly generated. In the following, the results of a hardware-in-the loop (HIL) simulation campaign are reported.

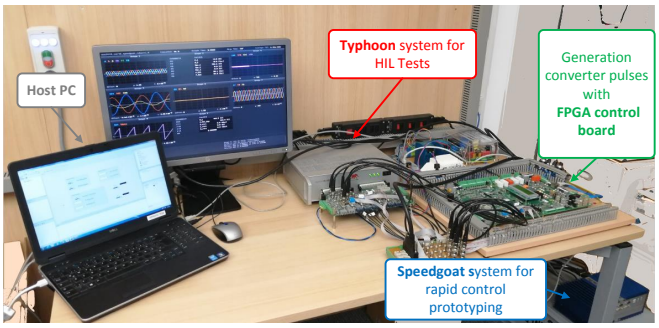



Figure 4: Picture of the HIL setup used for the tests.

Table I: System Parameters

| Description | Symbol | Value |
|---|---|---|
| Inverter rated power | $S_n$ | 1.55 kVA |
| Grid line-to-line voltage | $V_{LL}$ | 400 V (rms) |
| Rated grid frequency | $f_g$ | 50 Hz |
| Real filter inductance | $L_f$ | 0.15 pu |
| Real filter resistance | $R_f$ | 0.015 pu |
| Virtual filter inductance | $L_{v_n}$ | 0.26 pu |
| Virtual filter resistance | $R_{v_n}$ | 0.01 pu |
| Proportional gain correction term | $K_p$ | 30 |
| Integral gain correction term | $K_i$ | 1000 |
| Virtual inertia | $J$ | 4e-4 |
| Q-loop inverse integrator gain | $K$ | 800 |
| P-Droop coefficient | $D_p$ | 0.8 |
| Q-Droop coefficient | $D_q$ | 90 |
| Noise covariance factor | $Q_0$ | 0.05 |
| Measurement covariance factor | $R_0$ | 1 |

## IV. HIL SIMULATION RESULTS

In order to test the performance of the proposed control, simulation results have been performed by means of the HIL tests bench depicted in Fig. 4. A real-time digital simulator Typhoon HIL 602 simulates the converter and the grid with a time step of 1 $\mu$s, while the control structure shown in Fig. 2, is implemented on a Speedgoat real-time target machine running with a time step of 200 $\mu$s. An FPGA board produces the pulses of the IGBTs, in order to control the converter currents according to the reference signals $i^{**}$. The characteristics of the simulated system are reported in Table I.

Fig. 5 and Fig. 6 show the behaviour of the proposed control under symmetrical and asymmetrical fault conditions, respectively. Active and reactive power injection at the occurrence of the fault are reported in Fig. 5 (c), and Fig. 6 (c) for the two examined cases. As soon as the fault clearance condition is detected, the switches $S1$ and $S2$ of the outer

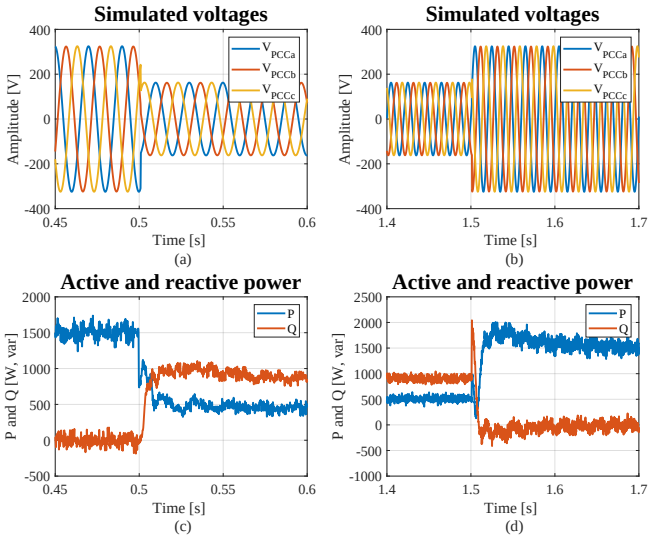



Figure 5: HIL simulations: behaviour of the converter according to a symmetrical grid fault. (a)-(b) Simulated PCC voltages, (c)-(d) active and reactive power.

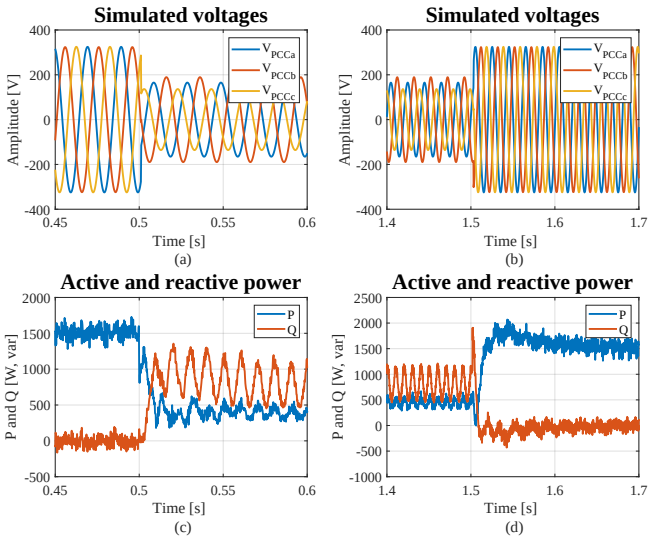



Figure 6: HIL simulations: behaviour of the converter according to an asymmetrical grid fault. (a)-(b) Simulated PCC voltages, (c)-(d) active and reactive power.

loop are set again to their original position, and the converter re-synchronizes itself automatically after a transient phase, as shown in Fig. 5 (d) and Fig. 6 (d). The dynamic performances in terms of reactive power injection will be further examined in the next section, while Fig. 7 highlights the process of reference currents $i^{**}$ generation from the signals $i^{*}$ calculated by the virtual admittance block in the two simulated fault cases. Following effects can be observed:

- The variable virtual admittance control dynamically modifies the amplitude of the reference currents so as to limit the highest peak among the three phases to the value specified in **(ii)**.

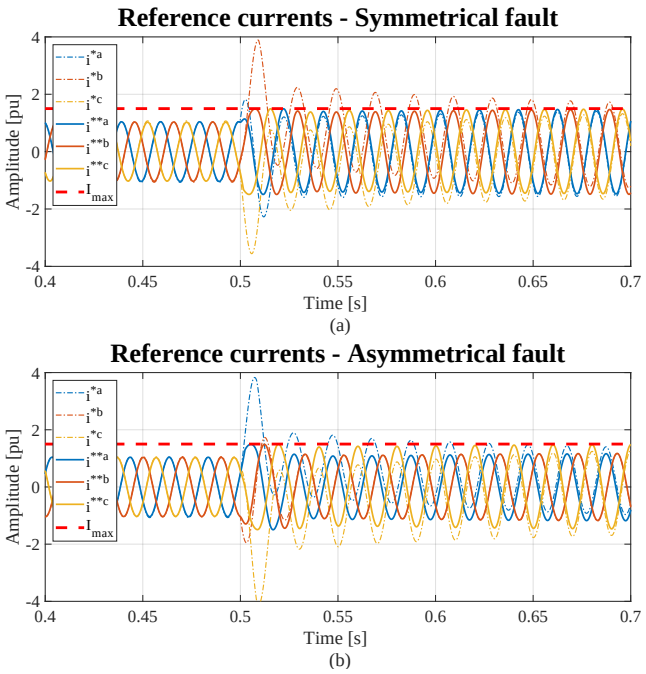


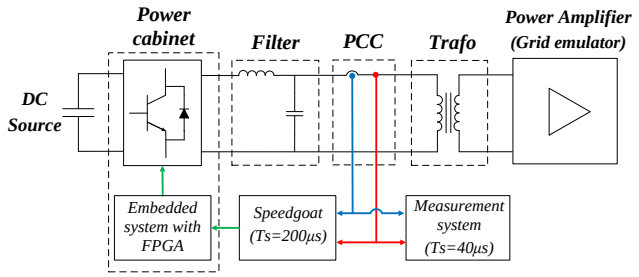

Figure 7: Reference currents generation: (a) symmetrical fault, (b) asymmetrical fault.

- According to **(iii)**, when the amplitude of the currents $i^{*}$ exceeds the specified maximum value, the inner current control loop calculates reference currents $i^{**}$, these having the same phase of the corresponding $i^{*}$, but limiting the amplitude to the highest allowable value $I_{max}$.
- The reference current calculation process effectively removes the DC-component of the short-circuit current typical of SMs, and generally of *RL* circuits [35], which does not contribute to active or reactive power injection, but it would rather saturate the transformer.

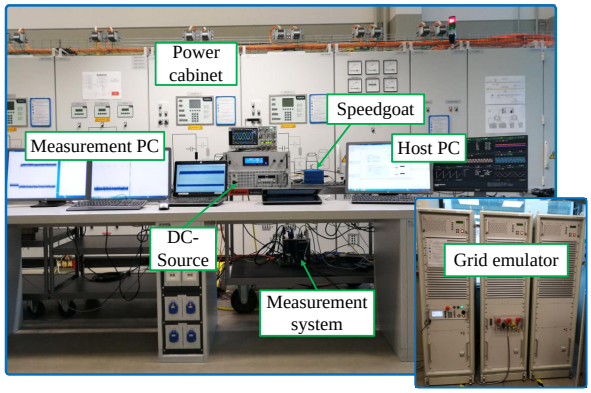
## V. Experimental Results

Experiments in a laboratory environment have been performed in order to test the performances of the proposed control. Fig. 8 (a) and (b) respectively show a scheme of the experimental setup, and a picture of it. A two-level converter with 1.5 kW rated power equipped with an output filter and isolation transformer, has been connected to a 4-quadrant linear power amplifier PAS 15000 from Spitzenberger & Spies. This is used as a grid emulator, and allows varying instantaneously the voltage at the connection point of the converter, hence emulating fault conditions. The setup composed of the Speedgoat real-time target machine combined with the FPGA board used for the HIL tests have been used to control the converter, while an IMC measurement system sampling voltages and currents at 25 kHz has been used for monitoring purposes.

Fig. 9 shows the reaction of the converter according to a symmetrical fault. In order to emulate the condition that the converter can inject a fault current up to 1.5 pu, active and reactive power setpoints prior the fault have been set




(a)




(b)

Figure 8: (a) Scheme of the laboratory setup used for the tests, (b) picture of the laboratory setup.

to $P_{set}$ =1 kW, and $Q_{set}$ =0 kvar, respectively. The prompt reaction of the converter in terms of reactive power injection can be appreciated in Fig. 9 (a), where the response within the first 5 ms after fault occurrence is highlighted. Current setpoints, along with the measured currents are shown in Fig. 9 (b), while in Fig. 9 (c) two vector diagrams compare voltages and currents previous and during the fault. Fig. 10 shows the behaviour of the converter under an asymmetrical fault condition. In this case, the amplitudes of the three voltages are suddenly reduced, and a phase shift in two phases is also reproduced. Similar considerations concerning the reaction time of the converter as for the previous case are valid.

It is finally worth to emphasize that, in both examined cases, the phase shift between voltages and currents during the fault are automatically resulting from the chosen virtual impedance, being the calculation of a reference reactive power setpoint according to the magnitude of the voltage depression and the type of fault not necessary.

## VI. Conclusion

This paper presents a FRT strategy for GFM converters ensuring current limitation independently on the type of the fault, and on the magnitude of the voltage dip. Regarding the behaviour during faults, the main advantage of GFM converters compared to their counterpart GFL converters consists on the almost instantaneous injection of reactive current without the need for tracking first the grid voltage angle and estimating the magnitude of the voltage dip. Even though this prompt reaction is surely beneficial for system stability, and highly attractive for SOs, the occurrence of a severe grid fault might easily provoke converter overcurrents and consequent hardware damages, if the fault condition is not properly handled. The proposed strategy directly controls the converter currents, yet it allows reproducing the required behaviour of a voltage source behind impedance before, during, and after the fault. Simulation results as well es experimental tests in a laboratory environment prove the effectiveness of the proposed strategy during symmetrical and asymmetrical fault conditions, showing a reactive power injection within few milliseconds after the occurrence of the fault, hence complying with the most up-to-date draft specifications elaborated within the EG convened by the British system operator NGESO.

## References


[1] H2020 MIGRATE Project, https://www.h2020-migrate.eu

[2] R. Lasseter, "Microgrids," in *Power Engineering Society Winter Meeting, 2002. IEEE* , vol. 1, pp. 305-308, 2002.

[3] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodriguez, "Control of power converters in AC microgrids," *IEEE Trans. Power Electron.*, vol. 27, no. 11, Nov. 2012, pag. 4734, 4749.

[4] ENTSO-E. (2017), High Penetration of Power Electronic Interfaced Power Sources (HPoPEIPS), [Available Online].

[5] NGESO, *"Expert workgroup on fast fault current injection - terms of reference,"* https://www.nationalgrideso.com

[6] Q.-C. Zhong, P.-L. Nguyen, Z. Ma, and W. Sheng, "Self-synchronized synchronverters: inverters without a dedicated synchronization unit," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 617-630, Feb. 2014.

[7] P. Rodriguez, C. Citro, I. Candela, J. Rocabert, and A. Luna, "Flexible grid connection and islanding of SPC-based PV power converters," *IEEE Transactions on Ind. Appl.*, vol. 54, no. 3, pp. 2690-2702, May-June 2018.

[8] L. Zhang, L. Harnefors, and H. P. Nee, "Power synchronization control of grid-connected voltage source converters," *IEEE Trans. Power Systems*, vol. 25, no. 2, pp. 809-820, May 2010.

[9] M. Ndreko, S. Rberg, and W. Winter, "Grid forming control for stable power systems with up to 100% inverter based generation: a paradigm scenario using the IEEE 118-bus system," *in Proc. 17th International Workshop on Large-Scale Integration of Wind Power into Power System (LSI)*, Sweden, Feb. 2018.

[10] M. A. Zamani, A. Yazdani, and T. S. Sidhu, "A control strategy for enhanced operation of inverter-based microgrids under transient disturbances and network faults," *IEEE Trans. on Pow. Deliv.*,vol. 27, no. 4, pp. 1737-1747, Oct. 2012.

[11] N. Bottrell and T. C. Green, "Comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up," *IEEE Trans. on Pow. Electr.*, vol. 29, no. 7, pp. 3786-3797, July 2014.

[12] W. Du, R. H. Lasseter and A. S. Khalsa, "Survivability of autonomous microgrid during overload events," *IEEE Trans. on Smart Grid*, vol. 10, no. 4, pp. 3515-3524, July 2019.

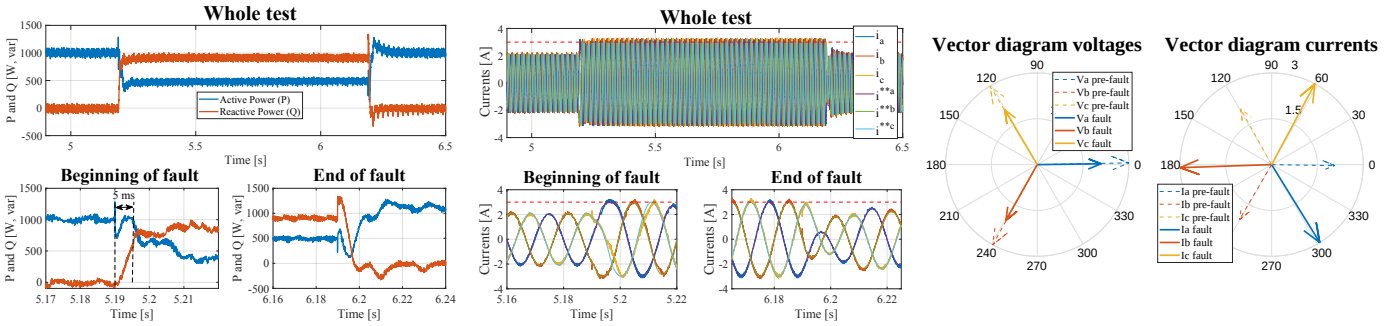
[13] J. He and Y. W. Li, "Analysis, design, implementation of virtual impedance for power electronics interfaced distributed generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 25252538, Nov./Dec. 2011.

[14] A. D. Paquette, and D. M. Divan, "Virtual impedance current limiting for inverters in microgrids with synchronous generators," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, Mar./Apr. 2015.

[15] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-impedance-based control for voltage-source and current-source converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 70197037, Dec. 2015.

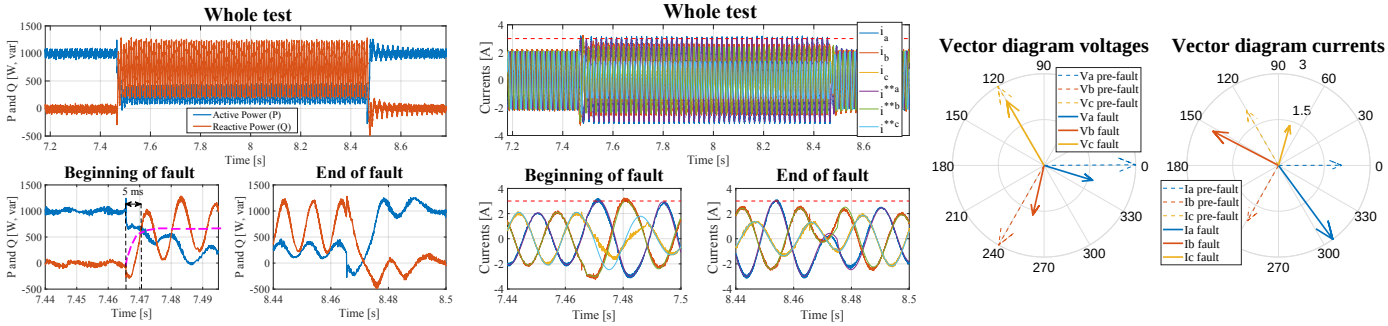
[16] J. Alipoor, Y. Miura, and T. Ise, "Voltage sag ride-through performance of virtual synchronous generator," *in Proc. International Power electronics conference*, 2014.

[17] H. Lin, C. Jia, J. M. Guerrero, "Angle stability analysis for voltage-controlled converters," *IEEE Trans. on Ind. Electr.*, vol. 64, no. 8, pp. 6265-6275, Aug. 2017.




(a) (b) (c)

Figure 9: Experimental results for a symmetrical fault: (a) active and reactive power, (b) converter currents, (c) vector diagrams of voltages and currents before and during the fault.




(a) (b) (c)

Figure 10: Experimental results for an asymmetrical fault: (a) active and reactive power, (b) converter currents, (c) vector diagrams of voltages and currents before and during the fault.


[18] Q.-C. Zhong, G. C. Konstantopoulos, B. Ren, and M. Krstic, "Improved synchronverter with bounded frequency and voltage for smart grid integration," *IEEE Trans. on Smart Grid*, vol. 9, no.2, pp. 786-796, March 2018.

[19] Z. Shuai, W. Huang, C. Shen, J. Ge, and Z. John Shen, "Characteristics and restrain method of fast transient inrush fault currents in synchronverters," *IEEE Trans. on Ind. Electr.*, vol. 64, no. 9, Sep. 2017.

[20] H. Lili, Z. Xin, L. Xuan, L. Zuyi, and S. John, "Transient characteristics of synchronverter subjected to asymmetric faults," *IEEE Trans. Power Delivery*, vol. 34, no. 3, pp. 1171-1183, Mar. 2019.

[21] P. Piya, M. Ebrahimi, M. Karimi-Ghartemani, and S. A. Khajehoddin, "Fault ride-through capability of voltage-controlled inverters," *IEEE Trans. on Ind. Electr.*, vol. 65, no. 10, Oct. 2018.

[22] T. Zheng, L. Chen, Y. Guo, S. Mei, "Comprehensive control strategy of virtual synchronous generator under unbalanced voltage conditions," *IET Gener. Transm. Distr.*, 2018, vol. 12, Iss. 7, pp. 1621-1630.

[23] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*, NJ, USA: Wiley-IEEE Press, 2011.

[24] M. G. Taul, X. Wang, P. Davari and F. Blaabjerg, "Current limiting control with enhanced dynamics of grid-forming converters during fault conditions," *in IEEE Journal of Emerging and Selected Topics in Power Electronics.*, doi: 10.1109/JESTPE.2019.2931477.

[25] S. F. Zarei, H. Mokhtari, M. A. Ghasemi, and F. Blaabjerg, "Reinforcing fault ride through capability of grid forming voltage source converters using an enhanced voltage control scheme," *in IEEE Trans. on Power Delivery*, vol. 34, no. 5, Oct. 2019.

[26] R. Lasseter, Z. Chen, and D. Pattabiraman, "Grid-forming inverters: a critical asset for the power grid," *IEEE Trans. JESTPE*, Invited paper.

[27] R. Rosso, J. Cassoli, G. Buticchi, S. Engelken, and M. Liserre, "Robust stability analysis of LCL filter based synchronverter under different grid conditions," *IEEE Trans. Power Electr.*, vol. 34, no. 1, pp. 46-52, Jan. 2019.

[28] R. Rosso, S. Engelken, and M. Liserre, "Robust stability investigation of the interactions among grid-forming and grid-following converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 991-1003, June 2020.

[29] R. Rosso, X. Wang, M. Liserre, X. Lu, and S. Engelken, "Grid-forming converters: an overview of control approaches and future trends," *in Proc. IEEE Energy Conversion Congress and Exposition (ECCE) 2020*, Detroit, Michigan, October 2020.

[30] VDE-Technische Anschlussregel Hochspannung (VDE-AR-N-4120).

[31] R. Rosso, S. Engelken, and M. Liserre, "Robust stability of synchronverters operating in parallel," *IEEE Trans. Power Electron.*, 2019, vol. 34, no. 11, pp. 11309-11319, November 2019.

[32] R. Grover Brown, *An introduction to random signal analysis and Kalman filtering*, John Wiley and Sons, 1983.

[33] D. Schroeder, "Elektrische Antriebe - Regelung von Antriebssystemen," Springer-Verlag, 2015.

[34] J. Rodriguez, and P. Cortes, *Predictive control of power converters and electrical drives.* Piscataway, NJ, Wiley-IEEE Press, 2012.

[35] P. Kundur, *"Power system stability and control"*, McGraw-Hill, Inc. 1994.

[36] S. Buso, S. Fasolo, L. Malesani, and P. Mattavelli, "A dead-beat adaptive hysteresis current control," *IEEE Trans. Ind. Application*, vol. 36, no. 4, pp. 1174-1180, Aug. 2000.