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A multiport partial power processing converter with energy storage integration for EV stationary charging

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Abstract—Battery storage system (BSS) integration in fast charging station (FCS) is becoming popular to achieve higher charging rates with peak-demand shaping possibility. However, the additional conversion stage for integrating the BSS increases the system losses, size and cost. The concept of partial power processing converter (PPPC), can mitigate this effect. Compared to conventional used full power processing converter, PPPC reduces the amount of transferred power from the BSS to the electric vehicle by the converter. As a consequence, the power losses generated by the converter are reduced, leading to lower sized converters and higher system efficiencies. This paper proposes a DC/DC multiport converter which allows the integration of battery storage in FCS based on a partial power processing concept, while maintaining the specific requirements in terms of isolation for FCS. The proposed three-port partial power processing converter (3P-PPPC) is derived from the commonly used triple active bridge (TAB) converter. The resulting design trade-offs, the dynamic behavior and limitations of the topology are investigated. Furthermore, the round-trip efficiency of the 3P-PPPC for integrating BSS in FCS is compared with conventional full power processing converter solutions, highlighting the superiority of the proposed topology. A prototype has been built to validate the 3P-PPPC.

Index Terms—DC/DC Converter, Multiwinding Transformer, Partial Power Processing, Battery Storage, EV Charging Stations

I. INTRODUCTION

In fast charging stations (FCS), the integration of battery storage system (BSS) is becoming of particular interest because of the peak power reduction during the charging process [1]–[3]. Furthermore, the use of BSS reduces the required grid connection capacity. This is especially important for locations where the local electricity infrastructure may not be sufficient for reaching high powers at the FCS. Without a BSS in the FCS, a cost-intensive upgrade of the existing electricity grid infrastructure is required [3], which might be not cost effective. Two factors mainly make the integration of BSS in FCS to an economical viable solution. Firstly, the continuously falling costs for battery storage and secondly the availability of so-called second life batteries, which are eventually removed from the electric vehicle (EV) when the capacity is below 80% of its initial value [4], [5].

Different solutions for BSS integration in FCS are discussed in literature. A common approach is the integration of the BSS in the DC Link via an additional DC/DC converter [Fig. 1 (a)]. Solutions that integrate BSS via a multiport converter [Fig.

1 (b)] are increasingly being investigated due to their high conversion efficiency and power density [6]–[11]. Particularly with regard to round trip efficiency, the multiport converter approach shows advantages due to the reduced number of conversions, as shown in Fig. 1. However, prevalent solutions are based on a full power processing converter (FPPC) structure. As a consequence, the DC/DC converter is sized for the maximum transferred power by the BSS.

In order to reduce the converter rating and further improve the efficiency, apart from the FPPC, the concept of partial power processing converter (PPPC) topologies has been proposed [12]–[15]. This concept aims to arrange an energy source as a series or a parallel element with the load, and allows that only a fraction of the total power is transferred through the converter. As a consequence, the power losses will be reduced, leading to a higher power density and efficiency. Furthermore, the reduced rating of the power converter will result in cost savings [16]. Different PPPC architectures have been proposed in literature, mainly considering the terms PPPC and differential power processing converter [13], [17]–[19]. The concept was mainly applied in the field of PV in order to compensate for the mismatch between series-connected PV panels [20], [21]. Nevertheless, due to the direct connection between source and load in PPPC, the feature of galvanic isolation is lost [16].

In the field of BSS integration in FCS, there are specific

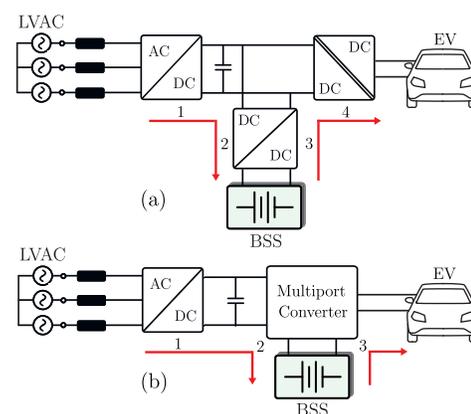


Fig. 1. Architectures for BSS integration with required number of conversions for recharging the BSS from grid and charging the EV from BSS: (a) BSS integration in DC link, (b) BSS integration with multiport converter.

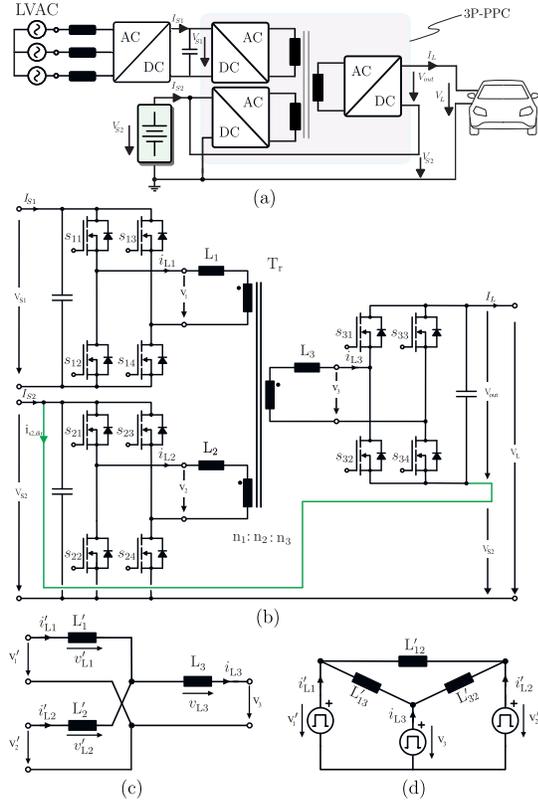


Fig. 2. Proposed 3P-PPC: (a) Concept with grid port voltage (V_{S1}), BSS port voltage (V_{S2}), EV port voltage (V_{out}) and charging voltage (V_L) which is sum of V_{S2} and V_{out} , (b) Detailed circuit, (c) Y-type referred to EV port equivalent circuit, (d) Δ -type equivalent circuit.

restrictions because of the required isolation between the electric vehicle (EV) and the electric grid, according to the IEC 61851-23:2014 standard. A way to benefit from partial power processing concept in FCS would be to integrate the BSS with a PPPC to the DC-Link [22]. However, due to the isolation requirement, the complete BSS power must be transferred through the adjacent full power processing isolated DC/DC converter. Another approach was presented in [23]: a multi-stage architecture for a FCS with multiple charging spots. The BSS is integrated after the required isolated DC/DC converter through a FPPC and then followed by PPPC, distributing the power to the different charging spots. However, from the system perspective, the high number of conversion stages and the related control effort are not beneficial.

This paper proposes a centralized DC/DC converter [Fig. 2 (a)], which combines the concept of multiport converter with the concept of PPPC, while reducing the number of required conversion stages to a minimum and maintaining galvanic isolation between specific ports of the converter, as required by the IEC 61851-23:2014 standard. Compared to other PPPC, the proposed multiport approach ensures galvanic isolation, which is normally lost when using the partial power processing concept. The magnetic coupling of the ports leads to certain design peculiarities in terms of power sharing capability between the different ports, which are investigated. Furthermore, the resulting limitations of the proposed 3P-PPC [Fig. 2 (a)] are analyzed. Finally, design guidelines are provided and high

efficiency operation is validated experimentally.

The paper is organized as follows: Section II provides a brief overview of the operation principle with the possible operation modes of the 3P-PPC. Furthermore, the equations describing the power transfer characteristic are derived. In Section III, the related design trade-offs are analyzed. A comparison with the conventional triple active bridge (TAB) converter is performed, highlighting the advantage of the 3P-PPC. The experimental validation is realized in Section IV, and followed by the conclusion in Section V.

II. OPERATION AND ANALYSIS OF 3P-PPC TOPOLOGY

The proposed 3P-PPC topology consists of three active full bridges which are linked with a three winding single core medium-frequency transformer (MFT) T_r , as shown in Fig. 2 (b). The topology is derived from the well known TAB converter, belonging to the class of multiport converter. As described above, the multiport approach [Fig. 1 (b)] shows advantages when round trip efficiency is considered, compared to conventionally used DC link integration of BSS [Fig. 1 (a)]. To quantify this advantage, round trip efficiency (grid to BSS, BSS to EV) for the depicted case in Fig. 1 is considered. In the following, the focus is on the analysis of the power electronic conversion stages. As a consequence, the resulting battery losses due to the electrochemical processes during charging and discharging are not considered in the round-trip efficiency. By assuming common efficiencies for the sub-systems (AC/DC: $\eta_{AC/DC} = 98\%$ [24], Non-isolated DC/DC: $\eta_{DC/DC} = 98\%$ [25], isolated DC/DC: $\eta_{iso,DC/DC} = 97\%$ [25],

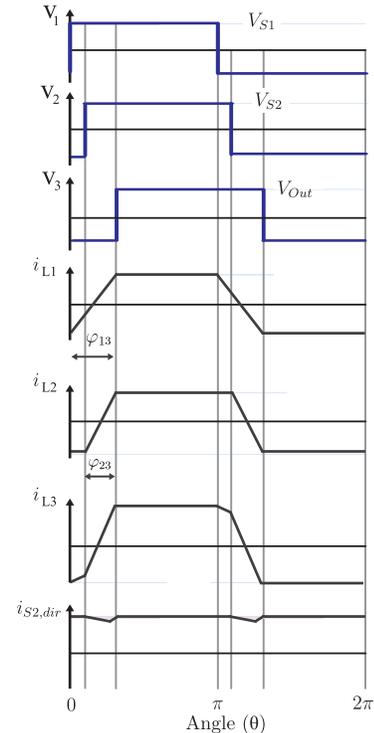


Fig. 3. Basic waveforms of 3P-PPC in steady state operation in which ϕ_{13} shows the relative phase shift between grid (port 1) and EV (port 3). ϕ_{23} depicts the relative phase shift between BSS (port 2) and EV (port 3).

multiport DC/DC: $\eta_{iso,mp} = 97\%$ [26]), it follows for the round trip efficiency of DC link integration ($\eta_{rt,1}$) and multiport approach ($\eta_{rt,2}$):

$$\eta_{rt,1} = \eta_{AC/DC} \cdot \eta_{DC/DC}^2 \cdot \eta_{iso,DC/DC} = 91.3\% \quad (1)$$

$$\eta_{rt,2} = \eta_{AC/DC} \cdot \eta_{iso,mp}^2 = 92.21\% \quad (2)$$

The superiority of the multiport approach can be further enhanced by the specific connection between the BSS port and the EV port of the proposed 3P-PPPC topology, which enables partial power processing operation, as shown next.

A. Operation principle and operation mode description

The proposed 3P-PPPC converter can be classified to the group of serially connected PPPC [15], because it adds a direct power transfer path between the BSS port and the EV port, depicted in green in Fig. 2 (b). As a consequence, the required voltage V_{out} at the EV port of the converter is reduced, since the total EV charging voltage V_L is the sum of the converter output voltage V_{out} and the direct applied BSS voltage V_{S2} . This reduction enables the use of lower rated devices with improved operation characteristics. Furthermore, the primary side BSS current i_{L2} through T_r is reduced. Although the galvanic isolation between the BSS and the EV is lost, the required galvanic isolation between the grid and the EV is fulfilled.

The general operation principle is similar to conventional TAB converter, whose equivalent circuits are depicted in Fig. 2 (c) and (d) [27], [28]. By using phase shift modulation (PSM), the active power between the ports can be adjusted [26]. Fig. 3 depicts the basic operation waveforms of the 3P-PPPC, showing a positive phase shift (ϕ_{13} and ϕ_{23}) from the grid (port 1) and the BSS (port 2) with respect to the EV (port 3) and hence transferring power to the EV port. For describing the power flow equations, the Y-type circuit [Fig. 2 (c)] in which the inductances, voltages and currents of the different ports are referred to a common port is transformed to Δ -type equivalent circuit [Fig. 2 (d)]. The power flow between two different ports (i,j) can be expressed with [28]:

$$P_{i,j} = \frac{v_i v_j}{2\pi f_s L_{i,j}} \phi_{i,j} \left(1 - \frac{\phi_{i,j}}{\pi}\right) \quad (3)$$

In which f_s defines the switching frequency. $\phi_{i,j}$ defines the relative phase shift between two ports and $L_{i,j}$ the inductance between the two ports. v_i and v_j depict the port voltages.

The converter can operate in different operation modes which are depicted in Fig. 4. The first scenario results when the EV is recharged by the combination of LVAC grid and the BSS [Fig. 4 (a)]. Thus, both active bridges are feeding at the same time the load. To control individually the power flow from the grid and BSS to the EV, each bridge is modulated independently. This mode will be the focus in this paper. In Fig. 4 (b) only the BSS is providing power to recharge the EV. Hence, in this scenario, the converter is operating as a dual active bridge (DAB) in partial power processing configuration. Finally, scenario three occurs when the BSS is recharged from

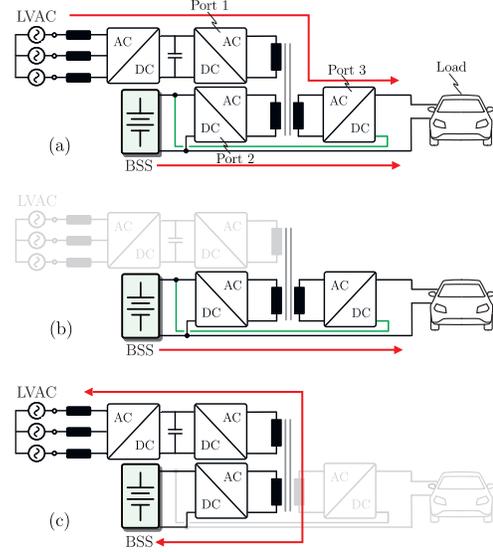


Fig. 4. Different operation modes of 3P-PPPC; (a) Grid (port 1) and BSS (port 2) transferring power to EV battery; (b) BSS is transferring power to EV battery; (c) Power transfer between grid and BSS port.

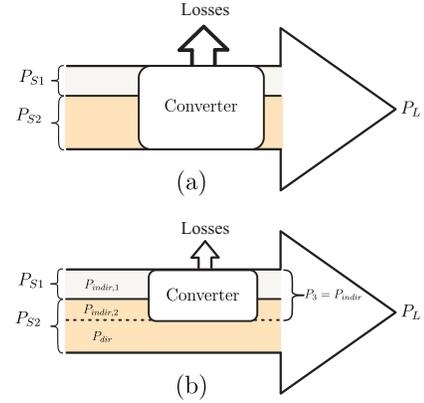


Fig. 5. Schematic of power sharing capability for: (a) conventional FPPC with two source ports and (b) proposed 3P-PPPC with direct power flow path from source port 2 to the load.

the grid or providing ancillary services for the grid, so that the 3P-PPPC operates like a DAB [Fig. 4 (c)].

B. Power transfer characteristic and power sharing capability of 3P-PPPC

Fig. 5 highlights the difference between a FPPC and the proposed 3P-PPPC. In a FPPC [Fig. 5 (a)], the complete power of the grid and BSS source ports (P_{S1}, P_{S2}) is processed through the converter. The 3P-PPPC [Fig. 5 (b)] allows that a fraction of the BSS port source power (P_{S2}) can be transferred directly (P_{dir}) to the load which reduces the power processed through the converter. The remaining power is transferred indirectly through the converter ($P_{indir,1}, P_{indir,2}$). For the transferred power of the source ports follows with (3):

$$P_{S1} = P_{12} + P_{13} \quad (4)$$

$$P_{S2} = -P_{12} + P_{23} + P_{dir} \quad (5)$$

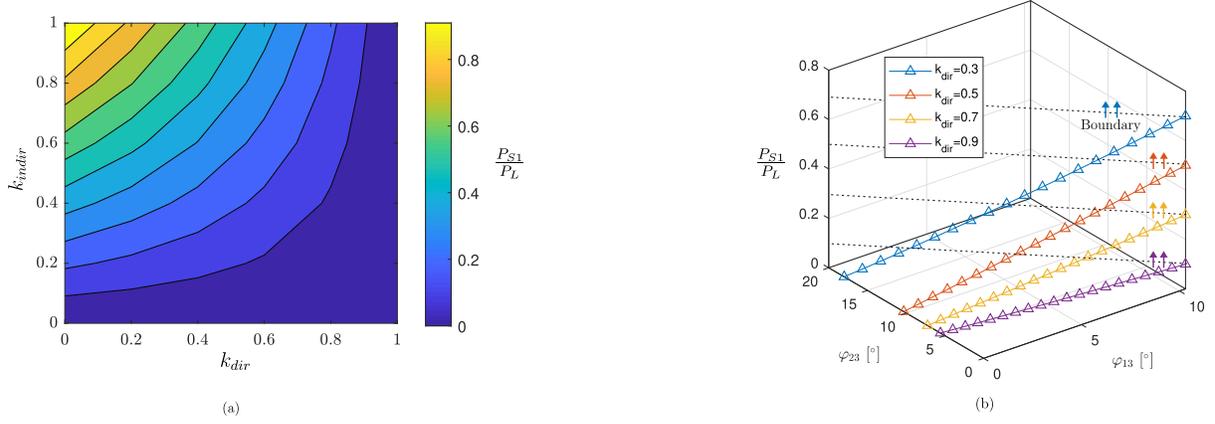


Fig. 6. Power sharing capability of 3P-PPPC: (a) Proportion of the transferred power from the grid port (P_{S1}) compared to the total charging power (P_L) in dependency of $k_{dir} = \frac{P_{dir}}{P_L}$ and $k_{indir} = \frac{P_{indir,1}}{P_{indir,1} + P_{indir,2}}$; (b) Required phase shift in order to achieve the desired power sharing ratio between the grid power and the total power in dependency of k_{dir} .

In which P_{S1} , P_{S2} depict the source power from the grid and BSS. With the series connected configuration in Fig. 2 (a), the charging voltage (V_L) is the sum of the converter output voltage (V_{out}) and the series connected BSS port (V_{S2}):

$$V_L = V_{out} + V_{S2} \quad (6)$$

The load power P_L is the total available charging power at the output and is composed by the indirect processed power (P_{indir}) through the converter to the load port and the direct transferred power (P_{dir}) from the BSS port.

$$P_L = P_{S1} + P_{S2} = P_{dir} + P_{indir} \quad (7)$$

With P_{dir} resulting from BSS voltage (V_{S2}) and the charging current (I_L) and P_{indir} being:

$$P_{dir} = V_{S2}I_L \quad (8)$$

$$P_{indir} = P_{indir,1} + P_{indir,2} \quad (9)$$

The 3P-PPPC has a design peculiarity compared to existing works on PPPC, due to its multiport configuration. The main parameter which defines the performance of a conventional two-port PPPC is the ratio between the direct processed power (P_{dir}) and the indirect processed power (P_{indir}). In general, designs with a larger proportion of direct processed power lead to higher efficiencies [16], [23]. In the proposed 3P-PPPC, additionally the ratio of the processed indirect power by the different feeding ports needs to be defined. Therefore, a two stage evaluation is required, as shown next.

In the first step, the power allocation between the direct transferred power P_{dir} and the indirect transferred power P_{indir} through the converter is defined. The amount of direct processed power with respect to the output power can be expressed with the factor k_{dir} and with (8) follows:

$$k_{dir} = \frac{P_{dir}}{P_L} = \frac{V_{S2}I_L}{V_L I_L} = \frac{V_{S2}}{V_L} \quad (10)$$

In a second step, the remaining indirect processed power which needs to be transferred through the converter is allocated to the feeding ports ($P_{indir,1}$, $P_{indir,2}$). The fraction of the indirect power between the feeding ports can be expressed with k_{indir} :

$$k_{indir} = \frac{P_{indir,1}}{P_{indir,1} + P_{indir,2}} \quad (11)$$

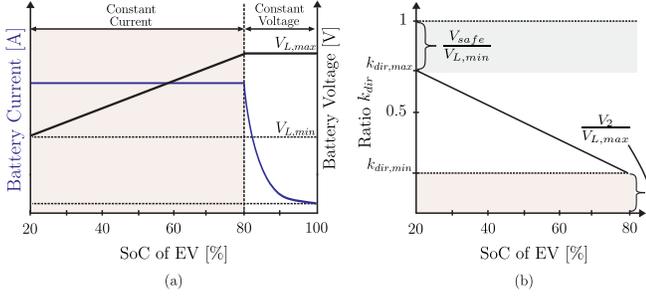
With (3) the equations can be further defined by:

$$k_{indir} = \frac{\frac{V_{S1} \frac{V_{out}}{n_1}}{\frac{n_3}{2\pi f L_{13}}} \Phi_{13} (1 - \frac{\Phi_{13}}{\pi})}{\frac{V_{S1} \frac{V_{out}}{n_1}}{\frac{n_3}{2\pi f L_{13}}} \Phi_{13} (1 - \frac{\Phi_{13}}{\pi}) + \frac{V_{S2} \frac{V_{out}}{n_2}}{\frac{n_3}{2\pi f L_{23}}} \Phi_{23} (1 - \frac{\Phi_{23}}{\pi})} \quad (12)$$

From (10), the proportion of the direct processed power is set by the choice of the BSS voltage level V_{S2} . The closer the BSS voltage V_{S2} reaches the load voltage V_L , the higher will be the direct transferred power to the load. A higher direct power transfer ratio k_{dir} limits the proportion of the transferred power from the grid port ($P_{S1} = P_{indir,1}$), compared to the total charging power (P_L). This relationship is shown in Fig. 6 (a), which depicts the proportion of the transferred power from the grid port (P_{S1}) compared to the total charging power (P_L) in dependency of k_{dir} and k_{indir} .

For designs with a small amount of direct processed power (low k_{dir}), large values for P_{S1} are possible with a high value of k_{indir} . In contrast, the larger the direct processed power (high k_{dir}), the smaller is the possible proportion of the power from the grid port (P_{S1}). The main part of the total power (P_L) is transferred directly from the BSS port (P_{S2}). Fig. 6 (b) illustrates this correlation by showing the required phase shifting combination, in order to achieve the desired power sharing ratios. Depending on the choice of k_{dir} , the maximum value of P_{S1} is limited.

The particularity, that the choice of the BSS voltage V_{S2} influences the the possible power sharing ratio, needs to be considered in the choice of the battery and the design process.



operation range: (a) Exemplary SoC curve of Li-Ion battery for EV charging, (b) Dynamic change of k_{dir} for relevant SoC range.

III. DESIGN AND COMPARISON OF 3P-PPPC WITH CONVENTIONAL USED TAB

The previous section revealed the general characteristics of the proposed 3P-PPPC. In the following, the design peculiarities of the 3P-PPPC are presented. Afterward, a specific design is verified and the 3P-PPPC is compared with the TAB in conventional configuration, highlighting the advantages of the 3P-PPPC.

A. Choice of the direct power transfer ratio k_{dir} and k_{indir}

In the application field of battery charging, the dynamic change of the load voltage V_L leads to a varying ratio of k_{dir} during operation. Exemplary Fig. II-B (a) shows a typical CC/CV charging curve, in which the CC stage (20% - 80% SoC) is the relevant area for fast charging applications [10]. The selection of the BSS voltage V_{S2} and the charging voltage V_L defines the ratio k_{dir} . As a constraint, the BSS voltage V_{S2} is not allowed to exceed the minimum charging voltage $V_{L,min}$, otherwise the required converter output voltage V_{out} becomes negative. Hence it follows:

$$V_{S2} \leq V_{L,min} \quad (13)$$

Assuming a linear voltage rise in the CC phase, Fig. II-B (b) depicts the range of the ratio k_{dir} across the SoC under the

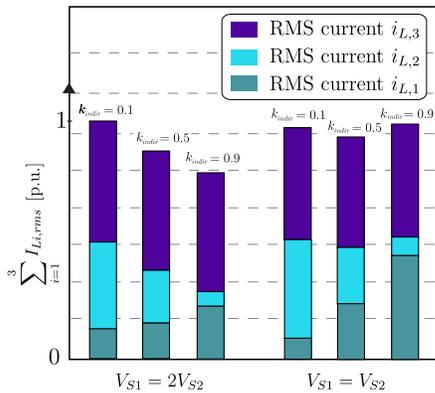


Fig. 7. Allocation of indirect processed power to feeding ports and effects on currents; Sum of transformer rms currents for different values of k_{indir} normalized to maximum value. Two cases are considered: (1) BSS voltage lower than grid voltage port ($V_{S1} = 2V_{S2}$), (2) Equal input voltage of the feeding ports ($V_{S1} = V_{S2}$).

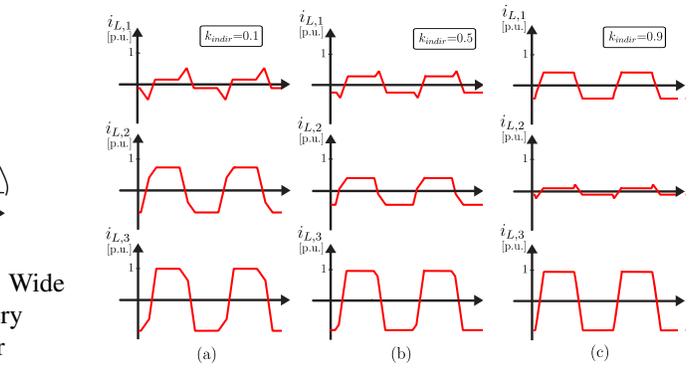


Fig. 8. Allocation of indirect processed power: (a)-(c) Transformer currents for case (1) of Fig. 7 for $k_{indir} = \{0.1, 0.5, 0.9\}$.

assumption of a constant voltage V_{S2} . At the beginning of the SoC curve the highest value of k_{dir} can be achieved:

$$k_{dir,max} = \frac{V_{S2} - V_{safe}}{V_{L,min}} \quad (14)$$

Theoretically a value of $k_{dir,max} = 1$ is feasible. However, due to safety reasons and the possibility of transient overvoltages, a buffer voltage V_{safe} is recommended [23]. Increasing the SoC will increase the required power through the converter and hence k_{dir} is decreasing and reaches its minimum at the maximum charging voltage ($V_{L,max}$):

$$k_{dir,min} = \frac{V_{S2}}{V_{L,max}} \quad (15)$$

As a consequence, the converter must be rated for the operation point in which the the direct transferred power is at its minimum ($k_{dir,min}$). In particular, the output voltage of the load port V_{out} reaches its maximum and hence determines the required semiconductor rating of the load port in terms of blocking voltage.

The ratio k_{indir} , which allocates the required indirect transferred power through the converter from the grid and BSS port, can be chosen arbitrarily. In general, the choice of k_{indir} depends on the individual scenario and the optimization target. Exemplary, Fig. 7 shows for different feeding port voltages (V_{S1}, V_{S2}) the sum of transformer rms currents for different ratios of k_{indir} . For instance, if transformer rms current minimization is the optimization target, it is beneficial in the first case of Fig. 7, in which the BSS voltage (V_{S2}) is lower compared to the grid port voltage (V_{S1}), to transfer more power through the grid port. Consequently a high k_{indir} should be chosen. This scenario is validated in Fig. 8 (a)-(c), which depict the resulting transformer current waveforms of each port. For this specific case a high value of $k_{indir} = 0.9$ reduces the sum of transformer rms currents.

B. Choice of transformer turns ratio and port inductances

The large output voltage range and the magnetic coupling between the ports require a careful selection of the turns ratios (n_1, n_2, n_3) and the port inductances (L_1, L_2, L_3) for the different transformer windings, as depicted in Fig. 2 (b).

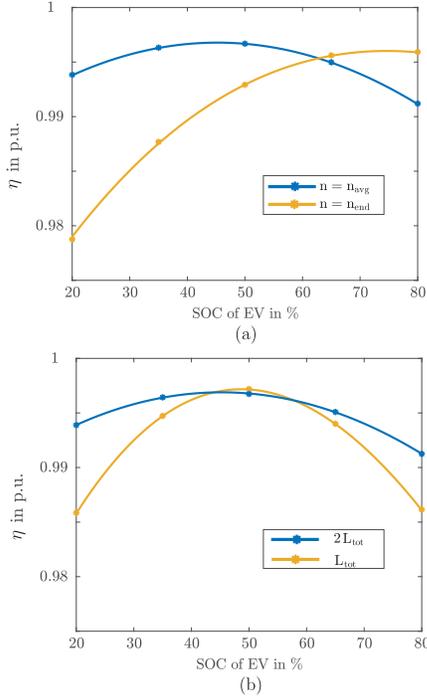


Fig. 9. Effect of transformer parameters on the efficiency of the 3P-PPPC for a complete SoC; (a) Effect of transformer turns ratio choice for matched voltage operation, (b) Effect of the port inductance choice assuming matched voltage operation at the average voltage of the EV port ($n = n_{avg}$)

In general, TAB based converters achieve the lowest current device stresses for operation scenarios with similar port voltages [10]. Unmatched port voltages lead to higher current stresses due to buck/boost operation. Depending for which operation point the turns ratio is chosen for the matched voltage operation, the efficiency curve will vary. Fig. 9 (a) depicts this issue for two exemplary designs. In the first approach, the matched voltage operation is set to the end of the CC stage, e.g. at 80% SoC ($n = n_{end}$). In a second case, where $n = n_{avg}$ the topology is designed based on the average voltage at the EV port, which occurs at 50% SoC. The latter maintains optimal current waveforms, when the voltage is at 50% SoC. As a consequence, the relative voltage difference will be lower and hence it diminishes the effect of the voltage variation at the EV port on the efficiency drop occurring during the charging process compared to the case where $n = n_{end}$.

At the same time the large output voltage range leads to a trade-off in the choice of the port inductances (L_1, L_2, L_3). In general, higher port inductances are more beneficial for operation scenarios with large unmatched port voltages. Whereas, for the operation scenario with matched voltages, a lower total inductance leads to less reactive currents due to smaller required phase shifts. Fig. 9 (b) evaluates this trade-off for two different designs. In the first design with a small value for the total inductance L_{tot} , which is the sum of the port inductances referred to port 3, the efficiency reaches its peak performance at the operation point with matched voltages (50% SoC). For operation points away from the matched voltage, the efficiency decreases significantly. In contrast, the second design with the larger L_{tot} achieves better efficiencies for operation points with

unmatched voltages.

However, its peak efficiency is slightly lower in the operation point with matched port voltages. In order to maintain a constant high efficiency across the charging curve, rather than having one optimized point, the design case two with higher L_{tot} is favored. The previous consideration highlighted the design aspects for the transformer parameters.

The specific operating conditions, such as battery discharge depth, affect the efficiency and therefore make it difficult to find generally applicable optimum values for the inductances. The best practice to design, is an iterative approach which evaluates the analytical equations. Based on the waveforms provided in Fig. 3, the transformer currents (I_{L1}, I_{L2}, I_{L3}) can be section-wise defined and composed. The resulting analytical equations for the currents allow to define an optimization routine (e.g. maximum efficiency, minimum peak currents and minimum rms currents).

Exemplary the procedure for the optimization target to minimize rms currents through the ports is depicted in Fig. 10 (i as running index). In a first step, the system specifications are determined. Furthermore, it is assumed that the port inductance are equal ($L = L_1 = L_2 = L_3$). Now the sum of the transformer winding rms currents of all three ports ($I_{L1,rms}, I_{L2,rms}, I_{L3,rms}$) are evaluated. In a next step the port inductance is increased incrementally (ΔL) and the currents are evaluated again. The port inductances are increased until the sum of the rms current is increasing compared to the previous running index ($i-1$).

As described before, the choice of the port inductance is critical in operation scenarios with large voltage deviations [29]. Therefore this approach is especially suitable for such scenarios to avoid high rms currents. Here it should be noted, that the analysis can be performed for several operation points during charging. This allows to obtain the best average value for the optimization target.

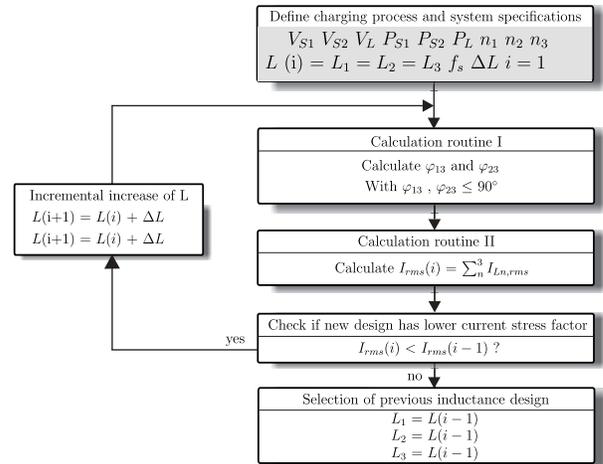


Fig. 10. Exemplary design guideline for choosing port inductance values with the target to minimize rms currents with i as running index and equal port inductances.

C. Storage battery peculiarities

Section (II-B) indicated the relation between the BSS voltage and the direct power transfer capability of the topology,

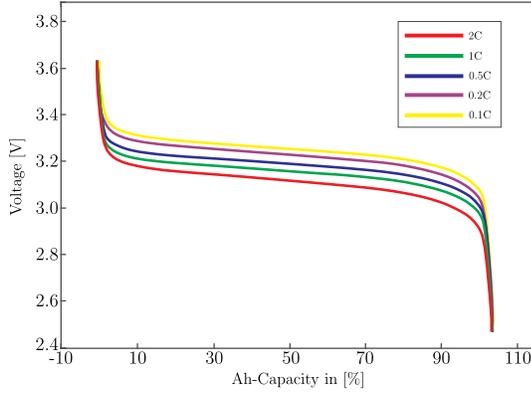


Fig. 11. Typical discharge curves for lithium iron phosphate (LiFePO4) battery for different C-rates [30].

which needs to be considered in the design process. A fast discharge of the BSS would lead to larger values of Δk_{dir} since the voltages V_L and V_{S2} "run" in opposite directions during the charging process which would reduce the k_{dir} . Furthermore, the larger operation range deteriorates the converters performance due to unmatched voltage operation.

As a consequence, the BSS voltage should be kept in a narrow range. In general, the nominal voltage and the voltage range during operation depend on the battery technology (e.g. cell chemistry). Fig.11 shows exemplary the discharge characteristic of a lithium iron phosphate battery for different discharge rates (C-rates). The larger the C-rate, the larger will be the voltage range. One strategy would be to choose a larger battery capacity which enables the operation at moderate C-rates and hence decrease the voltage range at the BSS port during the discharge process. Another strategy would be to operate not in the complete SoC range of the BSS. By limiting the depth of discharge the operation voltage range decreases. From the converter perspective, another strategy would be to operate the converter in a way, that a fraction of the grid power is used to recharge the BSS, in order to stay in the desired voltage range. This fact leads to the preliminary assumption of this paper, that the voltage of the supporting BSS is approximately constant as given in Table I.

D. Comparison with conventional used TAB

In order to validate the advantageous characteristics of the 3P-PPPC, a comparison with a TAB converter is performed. The TAB, in its conventional implementation as a FPPC, is widely used for integrating BSS [31].

For the comparison, a scenario with a charging current $I_L = 50$ A during the CC stage is assumed. The voltage of the EV battery V_L is assumed to increase linearly from 260 V to 340 V during charging from 20% to 80% SoC. This voltage range approximately corresponds to a battery pack consisting of 83 series connected Li-Ion Panasonic CGR18650AF [32] cells, when using the generic battery model based on the Shepherd's model in the MATLAB/Simulink environment [33], [34]. Based on the operation range, Table I shows the different designs for both converters. The maximum charging power $P_{L,max}=17$ kW is reached at the end of the CC stage

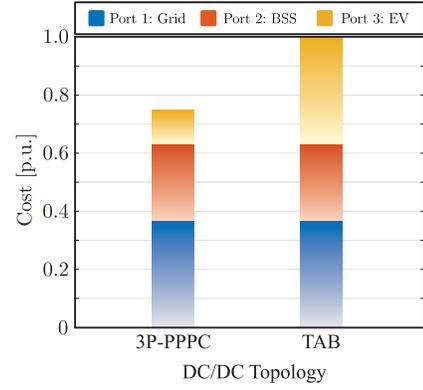


Fig. 12. Cost comparison between 3P-PPPC and TAB. Prices from www.digikey.com accessed at 28.09.2020.

Table I
CASE STUDY: 3P-PPPC VS. FPP-TAB FOR 20 kHz.

Parameter	3P-PPPC	TAB
Input voltage V_{S1} Grid Port	400 V	400 V
Input voltage V_{S2} BSS Port	200 V	200 V
Output voltage V_{out} EV Port	60-140 V	260 V - 340 V
Charging voltage V_L	260 V - 340 V	260 V - 340 V
CC charging current I_L	50 A	50 A
Maximum charging power $P_{L,max}$	17 kW	17 kW
Converter rated power	7.1 kW	17 kW
Turns ratio $n_{avg} = \{n_1, n_2, n_3\}$	{4, 2, 1}	{4, 2, 3}
Switching frequency f_s	20 kHz	20 kHz
Devices Grid Port	C2M0040120D	C2M0040120D
Devices BSS Port	C3M0030090K	C3M0030090K
Devices EV Port	IRF250P224	C2M0040120D

(80% SoC), which is the required power rating of the full power processing TAB.

On the other side, with (10) it becomes obvious, that for the 3P-PPPC the direct power transfer ratio k_{dir} is changing from $k_{dir} = 0.75$ (20% SoC) to $k_{dir} = 0.58$ (80% SoC). The remaining power which needs to be transferred through the converter in the operation point with the lowest k_{dir} depicts the required converter rating. As a consequence, the 3P-PPPC enables the reduction of the converter rating from 17 kW to 7.1 kW. Furthermore, the reduction of the converter output voltage V_{out} allows the use of lower rated semiconductor devices at the output port which leads to cost advantages. In the considered case study, the semiconductor cost can be reduced by around 25 % (c.f. Fig. 12).

Apart from the cost advantage due to the lower rated devices, the currents in the feeding ports (i_{L1} and i_{L2}) can be reduced with the partial power processing configuration due to the lower required output power and the resulting turns ratios of the transformer. In order to quantify this effect on the efficiency, the losses for a complete SoC curve have been analyzed. Fig. 13 (a) depicts the operation trajectory of the required phase shifts for reaching the different operation points on the SoC curve. The resulting DC voltages are shown in

Fig. 13 (b).

As a result Fig. 13 (c) shows the efficiency for both converters over the complete SoC. It can be seen, that the 3P-PPPC outperforms the FPP-TAB by around 1.9%, which results in 73 % of loss reduction for the 3P-PPPC.

E. Overall comparison, challenges and optimization potential of 3P-PPPC

The previous analysis has demonstrated the advantages of the proposed 3P-PPPC for the operation mode in which the Grid (port 1) and BSS (port 2) transferring power to EV battery [Fig. 4 (a)]. For an extended evaluation, the concept of overall round-trip efficiency is a useful method for the comparison of systems containing an energy storage as an intermediate step.

In the investigated scenario, the round-trip efficiency considers the energy transfer from the grid to the EV and as an intermediate step the charge and discharge of the BSS. The power electronic losses that occur during the required energy transformations are considered. As stated before, the losses which result from the chemical reactions from the battery represent another loss-component which are neglected in the analysis, since the BSS is used equivalent in all architectures.

The concept of round-trip efficiency was briefly introduced in Fig. 1. In this scenario all the energy is transferred in a first step to the battery and then to the EV. For a more general view, the analysis is extended for different fractions of the BSS power (P_{S2}) to the total charging power (P_L). Therefore, the factor k_{bat} is introduced, which defines the fraction of the BSS power to the total charging power:

$$k_{bat} = \frac{P_{S2}}{P_L} \quad (16)$$

The round trip efficiency for the 3P-PPPC is evaluated in dependency of k_{bat} and compared with the round trip efficiency for a classical battery integration with a non-isolated dc/dc converter in the DC link [Fig. 14 (a)] and a TAB converter in full power processing configuration [Fig. 14 (b)]:

$$\eta_{rt,DC-link} = k_{bat} \cdot \eta_{AC/DC} \cdot \eta_{DC/DC}^2 \cdot \eta_{iso,DC/DC} + (1 - k_{bat}) \cdot \eta_{AC/DC} \cdot \eta_{iso,DC/DC} \quad (17)$$

$$\eta_{rt,TAB} = k_{bat} \cdot \eta_{AC/DC} \cdot \eta_{iso,mp}^2 + (1 - k_{bat}) \cdot \eta_{AC/DC} \cdot \eta_{iso,mp} \quad (18)$$

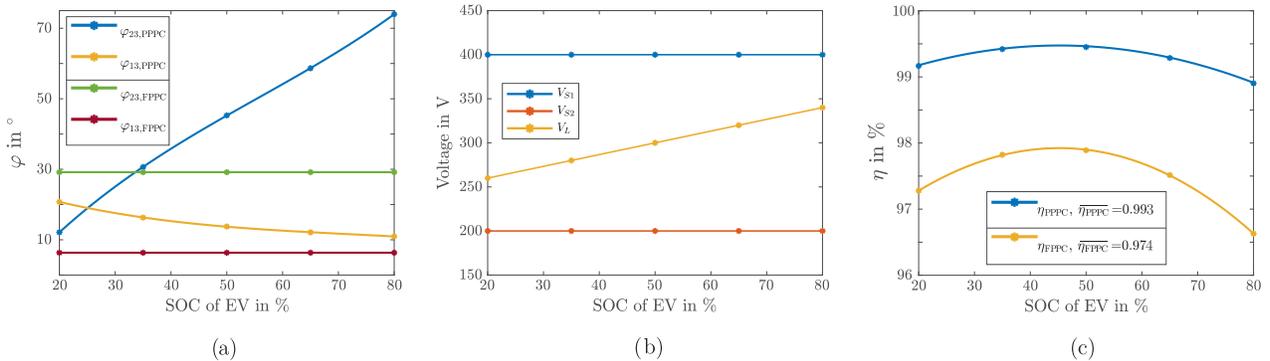


Fig. 13. Comparing TAB (FPPC) with proposed 3P-PPPC (a) the phase shifts for the 3P-PPPC topology, (b) different voltage trajectories over the complete SoC according to Table I and (c) the resulting efficiency for both converters over the complete SoC.

$$\eta_{rt,PPPC} = k_{bat} \cdot \eta_{AC/DC} \cdot \eta_{iso,mp} \cdot \eta_{ppp} + (1 - k_{bat}) \cdot \eta_{AC/DC} \cdot \eta_{iso,mp} \quad (19)$$

The values for the efficiencies of the subsystems have been defined Section II. The efficiency for the partial power process from the BSS to the EV is depicted with η_{ppp} and is assumed in this analysis to be $\eta_{ppp} = 98.5\%$. The results for the round-trip efficiency for the integration with non-isolated dc/dc converter in the DC link ($\eta_{rt,DC-link}$), for a FPP-TAB ($\eta_{rt,TAB}$) and for the 3P-PPPC ($\eta_{rt,PPPC}$) are shown in Fig. 14 (c). Regardless of the fraction of the BSS power with respect to the total charging power, the 3P-PPPC outperforms the other two approaches.

In order to exploit the full potential of the proposed topology, some aspects must be taken into account. The application-related wide operating range of the power converter leads to unequal port voltages. As described in Section III, a larger total inductance can counteract the impact of unmatched port voltages (e.g. higher current stresses of the devices). However, it should be ensured that the selected inductor enables the desired power transfer. Furthermore, the lack of isolation between the BSS and the EV port results in special functional safety requirements for field use. Further, the overall round trip efficiency can be increased by optimizing the BSS operation. For example, the battery efficiency and discharge loss effect is strongly correlated with the number of charging cycles, the depth of discharge and the C-rate, which also effects the temperature during charging/discharging. Limiting the system to a maximum C-rate of 1C will even reduce the loss of system efficiency because of the battery. The C-rate can be adjusted with the choice of the BSS capacity. Another optimization potential is the variable adaption of k_{indir} during different operation stages. For the initial analysis k_{indir} was kept constant during the complete SoC.

F. Dynamic modeling of 3P-PPPC

The dynamic behavior of the 3P-PPPC can be analyzed with a small signal model of the 3P-PPPC. As described in Section II B., the phase shifts φ_{13} and φ_{23} are available as control variables. If the DC-voltage at each port is constant, the system can be considered as a two-input system (φ_{13} and φ_{23}) and a two-output system (P_{S2} and P_L). The average active

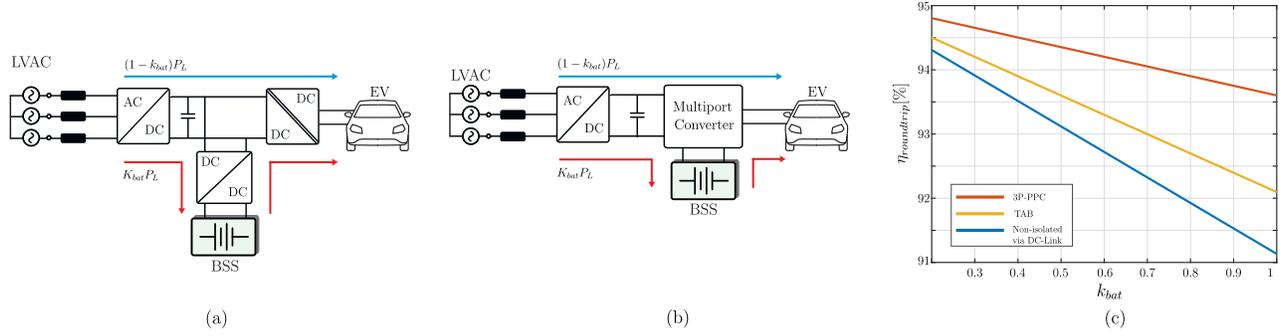


Fig. 14. Investigated scenarios for round-trip efficiency: (a) BSS integration via non-isolated dc/dc converter in DC-link, (b) Integration via multipoint converter in TAB configuration or 3P-PPPC configuration, (c) Resulting round-trip efficiencies for investigated systems.

power equations can be expressed with the Δ -representation [Fig. 2 (d)] and (4), (5) and (7):

$$P_{S1} = f_1(\varphi_{13}, \varphi_{23}) \quad (20)$$

$$P_{S2} = f_2(\varphi_{13}, \varphi_{23}) \quad (21)$$

$$P_L = f_3(\varphi_{13}, \varphi_{23}) \quad (22)$$

Consequently the net power from the feeding/sinking ports can be expressed with the port inductances and voltages referred to the EV port (port 3):

$$P_{S1} = \frac{V_1' V_2'}{2\pi f L_{13}'} (\varphi_{13} - \varphi_{23}) \left(1 - \frac{\varphi_{13} - \varphi_{23}}{\pi}\right) + \frac{V_1' V_3}{2\pi f L_{13}'} \varphi_{13} \left(1 - \frac{\varphi_{13}}{\pi}\right) \quad (23)$$

$$P_{S2} = -\frac{V_1' V_2'}{2\pi f L_{12}'} (\varphi_{13} - \varphi_{23}) \left(1 - \frac{\varphi_{13} - \varphi_{23}}{\pi}\right) + \frac{V_2' V_3}{2\pi f L_{23}'} \varphi_{23} \left(1 - \frac{\varphi_{23}}{\pi}\right) + V_2' I_L \quad (24)$$

$$P_L = P_{S1} + P_{S2} \quad (25)$$

(24)-(25) are large signal and non-linear equations, which need to be perturbed and linearized around an operating point.

$$\begin{aligned} G_{11} &= \left. \frac{\partial P_{S2}}{\partial \varphi_{13}} \right|_{\varphi_{13o}, \varphi_{23o}} & G_{12} &= \left. \frac{\partial P_{S2}}{\partial \varphi_{23}} \right|_{\varphi_{13o}, \varphi_{23o}} \\ G_{21} &= \left. \frac{\partial P_L}{\partial \varphi_{13}} \right|_{\varphi_{13o}, \varphi_{23o}} & G_{22} &= \left. \frac{\partial P_L}{\partial \varphi_{23}} \right|_{\varphi_{13o}, \varphi_{23o}} \end{aligned} \quad (26)$$

It follows:

$$G_{11} = \frac{V_1' V_2'}{2\pi f (L_{12}')^2} \left(1 - \frac{2(\varphi_{13o} - \varphi_{23o})}{\pi}\right) + \frac{V_1' V_3}{2\pi f L_{13}'} \left(1 - \frac{2\varphi_{13o}}{\pi}\right) \quad (27)$$

$$G_{12} = -\frac{V_1' V_2'}{2\pi f L_{12}'} \left(1 - \frac{2(\varphi_{13o} - \varphi_{23o})}{\pi}\right) \quad (28)$$

$$G_{21} = \frac{V_1' V_3}{2\pi f L_{13}'} \left(1 - \frac{2\varphi_{13o}}{\pi}\right) \quad (29)$$

$$G_{22} = \frac{V_2' V_3}{2\pi f L_{23}'} \left(1 - \frac{2\varphi_{23o}}{\pi}\right) \quad (30)$$

$$\begin{bmatrix} \tilde{P}_{S2} \\ \tilde{P}_L \end{bmatrix} = G \begin{bmatrix} \tilde{\varphi}_{13} \\ \tilde{\varphi}_{23} \end{bmatrix} \quad \text{with} \quad G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \quad (31)$$

In the proposed application of the 3P-PPPC, the control of the charging/discharging current of the storage battery (I_{S2}) and the electric vehicle battery (I_L) is desirable. The currents can be controlled directly via the relationship ($I_{S2} = P_{S2}/V_{S2}$, $I_L = P_L/V_L$).

However, from (31) the coupled nature of the control variables requires a measure for decoupling of these variables. A common method used in multipoint converters is a decoupling network. The resulting decoupling matrix is the inverse of the converter gain matrix G [28].

Besides using a decoupling matrix to cope with the cross-coupling between equations of the transfer matrix G , another approach is to use a Look-up table (LUT) to control the currents at both battery ports. Look-up tables are already used to address nonlinear behavior and to combine different modulation strategies.

The LUT table is constructed in advance from the hardware values (i.e., the port inductances) and the derived equations for the power transfer. Based on a set of linearly interpolated input vectors (V_{S2} , I_{S2} , V_L , I_L) the control variables φ_{13} and

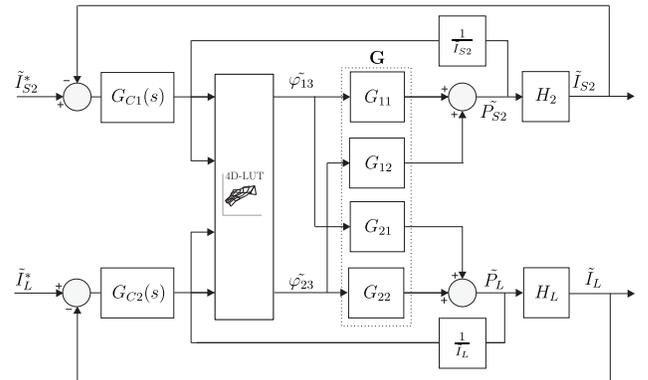


Fig. 15. Control loop block diagram of proposed 3P-PPPC, with look-up table (LUT) control approach.

φ_{23} are calculated and stored in a LUT (note that not only the power references, but also the information of the stiff voltages is used). During operation, the LUT evaluates the required phase shifts φ_{13} and φ_{23} . With this method, the phase shifts are impressed defined by the LUT to achieve the desired power flow between the ports dynamically during the charging process. If now the inputs of the LUT are controlled by a PI-controller using feedback from the real system, the currents and powers at the TAB ports can be regulated. The complete control loop block diagram is shown in Fig. 15.

H_L and H_2 represent the output filter to attenuate the current fluctuations. The fact that the series inductor and resistor of the battery are too small and almost they do not filter high frequency, the use of a low pass filter is required. Furthermore, it enables to set dynamics by the internal model control. It follows:

$$H_2 = H_L = \frac{1}{1 + \frac{s}{\omega_0}} \quad (32)$$

For the controllers G_{C1} and G_{C2} follows:

$$G_{C1}(s) = K_{C1} \frac{\tau_1 s + 1}{\tau_1 s} \quad (33)$$

$$G_{C2}(s) = K_{C2} \frac{\tau_2 s + 1}{\tau_2 s} \quad (34)$$

With K_{C1} and K_{C2} as the proportional gains. τ_1 and τ_2 are the time constants. The system dynamics of each terminal can be set independently by internal model control basic rules. For the practical controller design it is suggested to adjust the dynamics of the BSS current control loop (I_{S2}) to be different from the EV battery current (I_L) to cope with the coupling between the phase shifts and the non-linear transfer behavior of the 3P-PPPC. The dynamics of the EV current control (I_L) are adapted to prioritize CC operation at the EV port.

It should be noted, that the scope of this control analysis is the CC stage of the charging curve, which is more relevant for the fast charging. However, the control structure can be adjusted by including a switch which changes the control mode from CC to CV control depending on the current SoC value. In the CV stage a reference voltage needs to be provided, since the target of the controller is to supply constant voltage until the output current decrease to zero.

Table II
LABORATORY TEST CONDITIONS.

Parameter	3P-PPPC
Input voltage V_{S1} Grid Port	400 V
Input voltage V_{S2} BSS Port	200 V
Output voltage V_{out} EV Port	60 - 140 V
Charging voltage V_L	260 - 340 V
CC Charging current I_L	8 A
Turns ratio $n = \{n_1, n_2, n_3\}$	{4, 2, 1}
Port Inductance $L = \{L_1, L_2, L_3\}$	{ 80 μ H, 80 μ H, 40 μ H }
Switching frequency f_s	20 kHz

IV. EXPERIMENTAL VERIFICATION

The operation of the proposed 3P-PPPC has been tested with the specifications provided in Table II and the laboratory set up is depicted in Fig. 16 (a). Three power supplies have been used for validating the operation mode in which the grid and BSS transferring power to EV battery. The BSS port and the EV port have been operated with a bidirectional power supply (EA-PSB 9750-40 3U), enabling to emulate battery charging and discharging behavior. Both BSS and Grid port are operated with constant voltage. The bidirectional power supply of the EV acts as the sinking port and reproduces the charge curve with a constant charging current (CC phase in Fig. II-B (a)).

The converter has been tested for a complete charging cycle of the CC stage (20%-80% SoC). Different operation points of the SoC curve are depicted in Fig. 16(b)-(d). The converter is operating in steady state, where the transformer current of the charging port i_{L3} and the grid port i_{L1} and the related transformer voltages (v_3 and v_1) are presented. Based on the analysis provided in Section II-B, the power sharing coefficient of $k_{indir} = 0.8$ has been chosen for the operation of the converter. It can be seen that the converter operates in buck mode until a SoC of 50 % (Fig. 16 (b)-(c)). Above a SoC of 50 %, the converter operates in boost mode until the maximum voltage is of the charging curve is reached [Fig. 16 (d)-(f)].

Additionally, Fig. 18 (a)-(b) show the DC quantities in terms of charging voltage (V_L) and charging current (I_L) for two charging points with a SoC of 30 % and 50 %. Furthermore, Fig. 19 (a)-(b) validate the issue of higher current efforts from a wrong selection of the port inductance in operation cases for varying port voltages. Fig. 19 (c) depicts the resulting efficiency for both designs from Fig. 19 (a)-(b). The larger current stresses due to the wrong selection of inductance reduces the efficiency.

Finally, the efficiency across one charging cycle has been measured with the power analyzer Yokogawa WT1800. It can be seen that peak efficiency of $\eta = 98.7\%$ can be achieved for the operation case in which the port voltages are matched (Fig. 17). For unmatched port voltages, the converter will operate in buck ($V_L \leq 300V$) or boost mode ($V_L \geq 300V$) leading to a reduced efficiency. The average measured efficiency across a complete charging cycle is $\eta = 98.15\%$.

V. CONCLUSION

The proposed 3P-PPPC combines the concept of multiport converter with the concept of PPPC. As a consequence, the central integration of the BSS through a multiport converter enables a minimum of conversion stages while the PPPC concept leads to high efficient operation and a reduction of the required converter rating. Compared to other existing works on PPPC, a key feature of the proposed 3P-PPPC is its possibility to maintain the required galvanic isolation between the grid and the EV port.

The general design-Trade offs and limitations regarding power sharing between the feeding ports of the 3P-PPPC has been analyzed. Considering the peculiarities with respect to

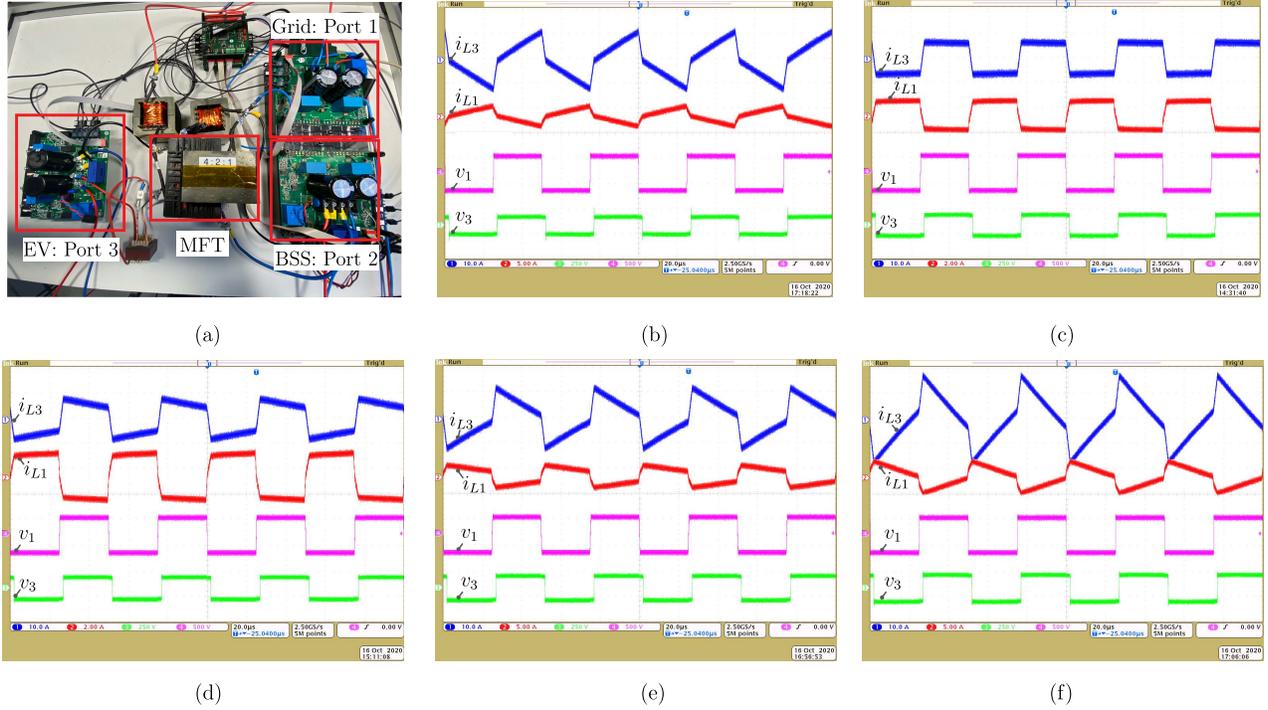


Fig. 16. Experimental validation of 3P-PPPC for different values of SoC curve: (a) Laboratory set-up, (b) Waveforms for operation point at 30 % SoC, (c) Waveforms for operation point at 50 % SoC, (d) Waveforms for operation point at 55 % SoC, (e) Waveforms for operation point at 60 % SoC, (f) Waveforms for operation point at 70 % SoC.

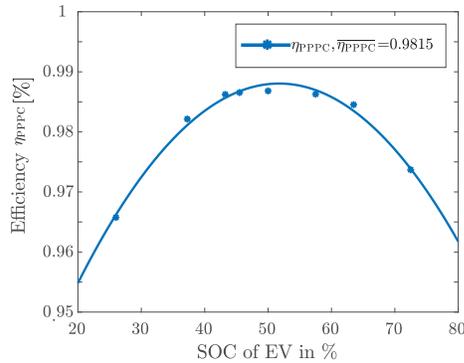


Fig. 17. Measured efficiency of 3P-PPPC across a complete SoC curve.

the power sharing capabilities, the proposed 3P-PPPC outperforms conventional used architectures for BSS integration. A comparison with the widely used TAB converter has shown a cost advantage around 25 % and an efficiency gain of 1.9 %, which results in 73 % of loss reduction, during the charging process. The converter operation has been validated with a laboratory prototype for a complete charging cycle of the CC stage (20%-80% SoC).

In summary, it can be stated that the 3P-PPPC is a promising alternative compared to the conventional FPP-based architectures. The 3P-PPPC performs particularly well in scenarios where a large part of the charging power has to be buffered via the BSS. However, due to the elimination of galvanic isolation between the BSS and the EV, appropriate safety precautions must be taken in terms of detecting ground fault leakage

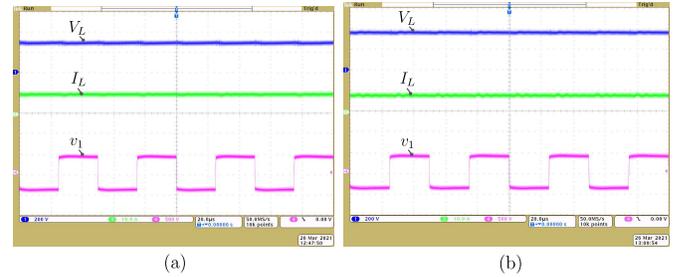


Fig. 18. DC quantities in terms of charging voltage (V_L) and constant charging current (I_L) for two points of SoC curve: (a) 30 % and (b) 50 % SoC

current. From the control perspective, the 3P-PPPC has similar requirements compared to conventional TAB. Existing control approaches can be also used for 3P-PPPC.

Future optimization potential for the 3P-PPPC lies in the choice of port inductances and transformer turns ratios in order to achieve the most efficient operation possible over the entire SoC. Further potential for optimization lies in the dimensioning of the BSS. Based on the available BSS capacity, optimal discharge depths can be controlled with regard to the losses and aging processes occurring in the battery, increasing the overall round-trip efficiency.

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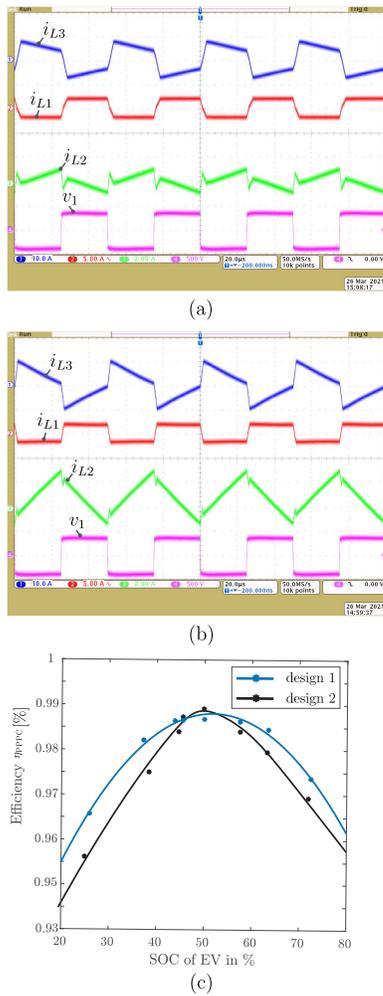


Fig. 19. Impacts of wrong port inductance design on current efforts in operation cases for varying port voltages (operation point at 55 % SoC): (a) Design 1 as suitable port inductances (design from Table II), (b) Design 2 where port inductances are too small (50% of value in Table II), resulting in high current efforts, (c) measured efficiencies for both designs across a complete SoC curve.

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