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Digital Object Identifier [10.1109/CPE-POWERENG50821.2021.9501174](https://doi.org/10.1109/CPE-POWERENG50821.2021.9501174)

2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering

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Suggested Citation

J. -H. Jung, S. Pugliese, M. Langwasser and M. Liserre, "Analysis and Suppression of Zero-Sequence Circulating Current in Multi-Parallel Converters," 2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), 2021.

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Abstract— The use of a multi-parallel converter system has many advantages in increased scalability, better maintenance, scheduling, and improved output current quality. However, a periodic zero-sequence circulating current (ZSCC) may occur due to the asymmetry of parallel-connected converters. ZSCC produces additional losses and possible instability of the system. Therefore, proper control must be applied to suppress this harmful ZSCC. In order to design an effective controller for suppressing ZSCC, it is necessary to analyze the circulating current. However, most of the studies conducted so far have applied the controller without detailed analysis. This paper mathematically analyzes the ZSCC spectrum by using the Fourier series to identify which harmonics are included in ZSCC. From the results of the analysis, the necessity of multi-resonant controllers to suppress the ZSCC at specific harmonics is demonstrated. Simulation and experiments are conducted to validate the analysis results and necessity of multi-resonant controllers.

Keywords—parallel PWM converter, zero-sequence circulating current, PR controller.

I. INTRODUCTION

In recent years, the power capacity of power conversion systems is increasing as the demand for electrical energy in the industry increases. Grid-connected AC-DC PWM converters have been widely used in the industry due to their advantages, such as high power factor, high efficiency, and low current distortion, compared to conventional rectifiers [1]. Nevertheless, the PWM converter cannot be used alone in large power systems due to the current limit of power devices. For this reason, studies on parallel PWM converters have been conducted in many papers. The parallel PWM converters have many advantages in terms of capacity scalability, maintenance, thermal management, and improved quality of the output current with interleaved PWM strategies [2, 3].

One of the main issues in parallel converters is the generation of the circulating current, which flows through them. The circulating current is created by asymmetry between converters in terms of output voltage and hardware. Although this current does not affect the quality of the three-phase current output from the entire system, it produces additional losses and can result in control instability. Therefore, the circulating current must be suppressed.

The circulating currents can be classified into two types depending on the frequency ranges that occur. In the high-

frequency region, the difference of the common-mode voltage (CMV) caused by each converter creates the circulating current at the switching frequency. So, it is defined as switching frequency circulating current (SFCC). If the interleaved PWM is applied to the parallel converter, the occurrence of SFCC is even worse. This SFCC can be reduced by applying modified PWM techniques [4-6].

On the other hand, in the low-frequency region, a low-frequency circulating current is generated by the difference in the zero-sequence voltage (ZSV) output from each converter [7-10]. This current is defined as a zero-sequence circulating current (ZSCC). In general, ZSCC can be suppressed using only a proportional-integral (PI) controller if the converter is controlled under the symmetry condition [8]. However, when the parallel converter is operated under the unbalanced load condition, such as a power routing in [11], a large periodic ZSCC occurs due to the difference in ZSVs. Since the PI controller is not adequate to suppress the periodic ZSCC, several papers have studied the application of proportional resonant (PR) controllers to reduce the ZSCC harmonic content [9, 10]. Although the PR controller reduces the ZSCC oscillation corresponding to the 3rd harmonic, the other low-frequency current oscillation remains. Therefore, it is necessary to design the controller more accurately so that even the remaining current ripple can be suppressed.

Previous studies have analyzed ZSCC about 1st and 3rd order harmonics [9, 10] or SFCC [4-6]. The PR controller for only the 3rd harmonics is designed and applied without a clear basis for ZSCC caused under the unbalanced load conditions. This is because it is possible to intuitively confirm that the 3rd harmonic is the dominant component in ZSCC and obtain relatively good reduction results by applying the PR controller for the 3rd harmonic. In order to effectively suppress ZSCC under unbalanced load conditions, it is necessary to design an accurate controller by analyzing and defining ZSCC in detail. Therefore, in this paper, ZSCC is analyzed and defined using the Fourier series for a precise and optimized controller design. As mentioned above, since the difference in ZSV output from each converter generates a ZSCC, the ZSV is at first mathematically generalized by using the Fourier series. The ZSV difference between one converter and the other converter is obtained, and then the ZSCC can be calculated by integrating the voltage difference and taking into account the inductance on the current loop. From the analytical results, it has been proved that the circulating current includes the current ripple at the 3rd harmonic

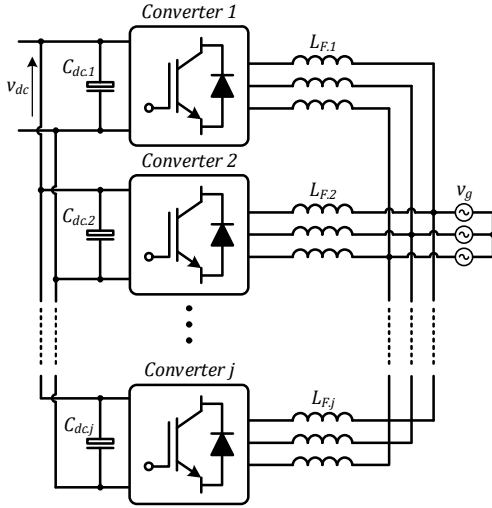


Fig. 1. Grid-connected multi-parallel three-phase PWM converters.

as well as at other harmonics, and described the necessity of applying additional resonant controllers to reduce these harmonics. The analysis of ZSV and ZSCC conducted in this paper is verified through simulation and experimental results. Moreover, it is validated that controllers must be added for suppressing a number of harmonics included in ZSCC.

II. PARALLEL-CONNECTED PWM CONVERTER SYSTEM

Fig. 1 shows a grid-connected multi-parallel three-phase PWM converter system. Each PWM converter shares the same DC-link voltage (v_{dc}), and each phase of all converters is connected to a corresponding phase of the grid voltages (v_g) through a harmonic filter (L_{Fj}). This parallel converter system is suitable for high-power applications because the capacity of the system can be increased by adding more power converters in parallel. Also, the modularity of the converter facilitates easy repair and maintenance, and the quality of the output phase current can be improved by applying the interleaved PWM method to each converter.

Although the parallel converter has many advantages as mentioned above, the circulating current (CC) flowing between the parallel converters can be created as shown in Fig. 2 due to asymmetry between the converters. This current does not flow into the grid but only inside the system. However, CC must be suppressed because it causes additional losses in the converter and instability of the control system, in the worst case.

In general, CC can be defined as the sum of the three-phase currents expressed in (1), where j indicates the j -th converter. Besides, the current can be classified into switching-frequency CC (SFCC) and zero-sequence CC (ZSCC) according to the frequency region where it occurs. Between them, ZSCC is generated by the difference in ZSV (v_{zs}) of each converter. For example, in a two-parallel converter system, ZSCC flowing between converter '1' and '2' can be defined (2).

$$i_{cc,j} = \frac{i_{A,j} + i_{B,j} + i_{C,j}}{3} \quad (1)$$

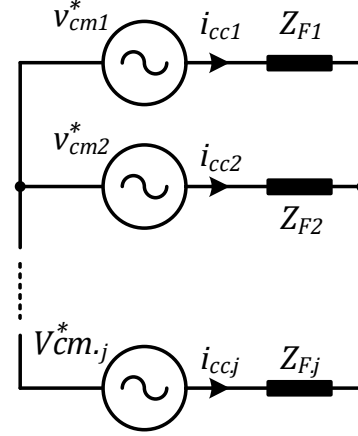


Fig. 2. Equivalent circuit of multi-parallel three-phase PWM converters.

$$i_{cc,1} = -i_{cc,2} = \frac{1}{L_{F,1} + L_{F,2}} \int (v_{zs,1}^* - v_{zs,2}^*) dt \quad (2)$$

Usually, the parallel-connected PWM converters are designed and controlled symmetrically to each other. In this case, the ZSV output from each converter is almost the same. It means there is little voltage difference in ZSV and this voltage difference only causes some ZSCC. Thus, it is possible to sufficiently suppress ZSCC to zero current by applying only a conventional P or PI controller to the converter [8]. However, if each parallel-connected converter operates under different load conditions, such as the power routing [11], ZSV output from each converter no longer overlaps with each other. The ZSV difference generates a periodic ZSCC, as shown in Fig. 3.

Since the conventional P and PI controller is not suitable for suppressing a periodic error, these controllers are not effective in reducing periodic ZSCC when the parallel converter is controlled under unbalanced conditions. In several papers, a PR controller like in (3), designed with a bandwidth around resonant frequency equal to triple of fundamental operating frequency, is applied to suppress the ripple of ZSCC [9, 10].

$$G_{PR}(s) = K_p + \frac{K_R s}{s^2 + \omega_0^2} \quad (3)$$

However, the design criterion or basis for the PR controller only highlights the 3rd harmonic. In addition, The ZSCC ripple at higher frequency remains even though the ZSCC ripple corresponding to the dominant component, the 3rd harmonic, is reduced. Therefore, it is necessary to analyze which harmonics are included in ZSCC to design a more accurate ZSCC suppression controller.

III. MATHEMATICAL ANALYSIS OF ZSCC

Since ZSCC occurs by the difference in ZSV as presented in (2), it is required to generalize the equation of ZSV before the analysis of ZSCC. ZSV can be given as (5) by using a mid-value (v_{mid}) among three-phase voltage references in (4) [1].

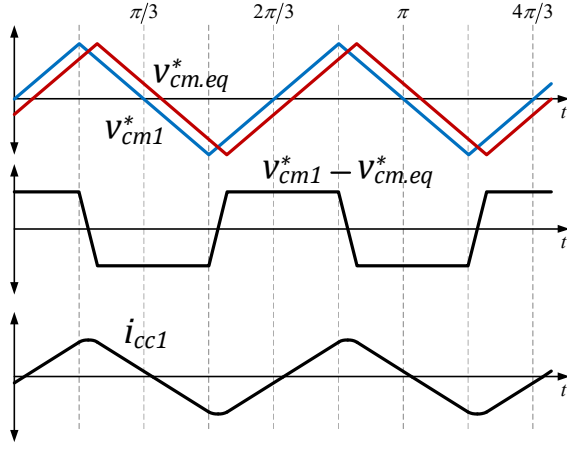


Fig. 3. ZSV, ZSV difference and ZSCC under unbalanced load conditions.

$$\begin{cases} v_{A,j}^* = V_j \cos(\theta) \\ v_{B,j}^* = V_j \cos(\theta - 2\pi/3) \\ v_{C,j}^* = V_j \cos(\theta + 2\pi/3) \end{cases} \quad (0 < \theta \leq 2\pi) \quad (4)$$

$$v_{zs,j}^* = -\frac{v_{\max,j}^* + v_{\min,j}^*}{2} = \frac{v_{\text{mid},j}^*}{2} \quad (5)$$

As shown in Fig. 3, the ZSV is a periodic function with a period of $2\pi/3$, and it can be obtained as (6) in case the phase angle ranges from $0 < \theta < 2\pi/3$. The ZSV is relevant with the voltage reference of a phase 'B' in a range of $0 < \theta < \pi/3$ and a phase 'A' in range of $\pi/3 < \theta < 2\pi/3$.

$$v_{zs,j}^*(\theta) = \begin{cases} \frac{1}{2} V_j \cos(\theta - 2\pi/3) & (0 < \theta < \pi/3) \\ \frac{1}{2} V_j \cos(\theta) & (\pi/3 < \theta < 2\pi/3) \end{cases} \quad (6)$$

The Fourier series of a function $f(\omega t)$ with a period T is given as follow:

$$f(\theta) = a_0 + \sum_{n=1}^{\infty} \left\{ a_n \cos\left(\frac{2\pi n \theta}{T}\right) + b_n \sin\left(\frac{2\pi n \theta}{T}\right) \right\} \quad (7)$$

Where a_0 , a_n , and b_n are Fourier coefficients.

The Fourier coefficient a_0 for the ZSV can be defined as (8) considering (6).

$$\begin{aligned} a_0 &= \frac{1}{T} \int_0^T v_{zs,j}^*(\theta) d\theta \\ &= \frac{3V_j}{4\pi} \left\{ \int_0^{\pi/3} \cos\left(\theta - \frac{2\pi}{3}\right) dt + \int_{\pi/3}^{2\pi/3} \cos(\theta) dt \right\} = 0 \end{aligned} \quad (8)$$

The coefficient a_n and b_n can be expressed as (9) and (10), respectively.

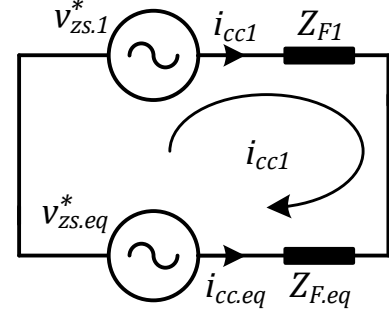


Fig. 4. Simplified equivalent circuit of the parallel converter from the viewpoint of the converter '1'.

$$a_n = \frac{2}{T} \int_0^T v_{zs,j}^*(\theta) \cos\left(\frac{2\pi n \theta}{T}\right) d\theta \quad (9)$$

$$b_n = \frac{2}{T} \int_0^T v_{zs,j}^*(\theta) \sin\left(\frac{2\pi n \theta}{T}\right) d\theta \quad (10)$$

a_n and b_n can be obtained as (11) and (12) considering (6) in the same way as (8).

$$\begin{aligned} a_n &= \frac{3V_j}{2\pi} \left\{ \int_0^{\pi/3} \cos\left(\theta - \frac{2\pi}{3}\right) \cos(3n\theta) d\theta + \int_{\pi/3}^{2\pi/3} \cos(\theta) \cos(3n\theta) d\theta \right\} \\ &= -\frac{3\sqrt{3}V_j}{\pi(9n^2 - 1)} \quad (n = 1, 3, 5, \dots, 2m-1) \end{aligned} \quad (11)$$

$$\begin{aligned} b_n &= \frac{3V_j}{2\pi} \left\{ \int_0^{\pi/3} \cos\left(\theta - \frac{2\pi}{3}\right) \sin(3n\theta) d\theta + \int_{\pi/3}^{2\pi/3} \cos(\theta) \sin(3n\theta) d\theta \right\} \\ &= 0 \end{aligned} \quad (12)$$

Finally, the ZSV can be given as (13) by substituting the three Fourier coefficients of (8), (11), and (12) in (7).

$$v_{zs,j}^* = -\sum_{n=1}^{\infty} \frac{3\sqrt{3}V_j}{\pi(9n^2 - 1)} \cos(3n\theta) \quad (13)$$

From (13), it can be confirmed that the ZSV contains only $3n$ ($n=1, 3, 5, \dots, 2m-1$) order harmonics, and the magnitude of the voltage decreases as the order 'n' increases.

As presented in Fig. 3 and (2), the ZSCC is created by the difference in ZSV of each parallel-connected converter. From the converter '1' viewpoint, if the remaining parallel-connected converters are represented equivalently as shown in Fig. 4, ZSCC flowing through converter '1' and equivalent converter model can be expressed as (14).

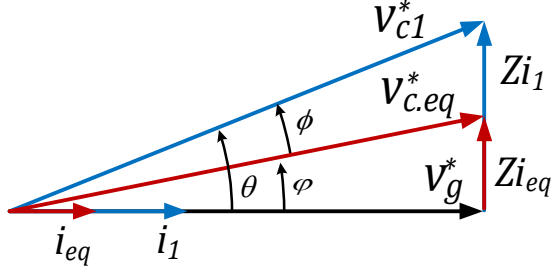


Fig. 5. Relationship of voltage references between converter '1' and the equivalent converter.

$$i_{cc,1} = \frac{1}{L_{F,1} + L_{F,eq}} \int (v_{zs,1}^* - v_{zs,eq}^*) dt \quad (14)$$

Where $L_{F,eq}$ is an equivalent inductance, and $v_{zs,eq}$ means ZSV output from the equivalent converter.

Assuming that the voltage reference of the equivalent converter model lags behind that of the converter '1' by ϕ . $v_{zs,eq}$ and $v_{zs,1}$ are given as (15) and (16), respectively, and the difference between two voltages can be evaluated as (17).

$$v_{zs,1}^* = -\sum_{n=1}^{\infty} \frac{3\sqrt{3}V_1}{\pi(9n^2 - 1)} \cos(3n\theta + \phi) \quad (15)$$

$$v_{zs,eq}^* = -\sum_{n=1}^{\infty} \frac{3\sqrt{3}V_{eq}}{\pi(9n^2 - 1)} \cos(3n\theta) \quad (16)$$

$$\begin{aligned} v_{zs,1}^* - v_{zs,eq}^* &= -\sum_{n=1}^{\infty} \frac{3\sqrt{3}}{\pi(9n^2 - 1)} \{V_1 \cos(3n\theta + \phi) - V_{eq} \cos(3n\theta)\} \\ &= V_1 \sin \phi \sum_{n=1}^{\infty} \frac{3\sqrt{3}}{\pi(9n^2 - 1)} \{\sin(3n\theta) - \tan \phi \cos(3n\theta)\} \end{aligned} \quad (17)$$

The relationship between V_1 and V_{eq} is given as (18), based on Fig. 5.

$$V_{eq} = V_1 (\cos \phi - \tan \phi \sin \phi) \quad (18)$$

Where ϕ is the phase angle between the grid voltage (v_g) and the voltage reference of the equivalent converter.

If the converter system is appropriately designed and controlled with a unity power factor, ϕ is relatively small. Since a term corresponding to tangent and cosine affects the phase shift for the sine function, (17) is approximated (19).

$$v_{zs,1}^* - v_{zs,eq}^* = V_1 \sin \phi \sum_{n=1}^{\infty} \frac{3\sqrt{3}}{\pi(9n^2 - 1)} \sin(3n\theta - \phi) \quad (19)$$

As expressed in (14), ZSCC flowing through the converter '1' can be obtained by integrating the voltage difference in (20)

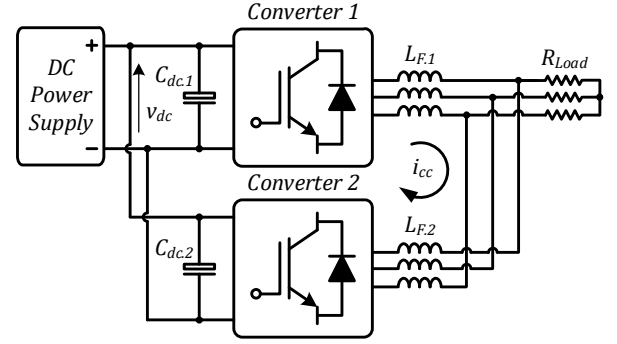


Fig. 6. Circuit configuration for the simulation and experiment.

TABLE I. SIMULATION AND EXPERIMENTAL CONDITIONS

Parameters	Value
DC-link voltage	600 [V]
Inductance of filter	3.6 [mH]
Resistance of load	15 [Ω]
Switching frequency	10 [kHz]
Fundamental operating frequency	50 [Hz]

and dividing by the sum of the inductance on the current loop. The phase angle θ is replaced by ωt , which is about a term for the angular speed. For reference, the resistance of the loop is neglected because it is very small.

$$i_{cc,1} = -\frac{V_1 \sin \phi}{\omega(L_{F,1} + L_{F,eq})} \sum_{n=1}^{\infty} \frac{\sqrt{3}}{n\pi(9n^2 - 1)} \cos(3n\omega t - \phi) \quad (20)$$

In conclusion, it is proved by (20) that the ZSCC includes $3n$ ($n=1, 3, 5, \dots, 2m-1$) order harmonics, and it is generated when the parallel-connected converters are operated under the unbalanced load conditions. This means that P and PI controllers, which is not suitable for reducing the periodic error, cannot be applied to the system, and since the PR controller used in [9] and [10] is applied for the purpose of reducing only the 3rd harmonic, ZSCC ripple such as 9th and 15th order harmonics still remain.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experiments are conducted to validate the analysis results of ZSCC. As shown in Fig. 6, two parallel-connected PWM converters with DC power supply, single-phase harmonic filters ($L_{F,j}$), and resistive load (R_{Load}) are used. The conditions and specifications for simulation and experiment are presented in Table I.

Fig. 7 shows the simulation results about the ZSVs of the two converters, the difference in ZSV, and ZSCC when the two converters are equally controlled with a constant current of 10A. As a ZSCC suppression controller, a PI controller is used for each converter. ZSVs of each converter are almost the same as each other, and their difference is less than 2V, as presented in Fig. 7(a) and (b). So, it can be seen from Fig. 7(c) that almost

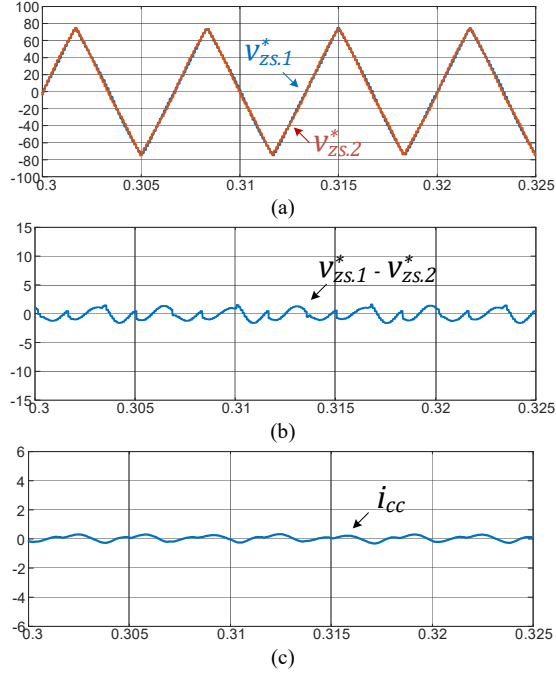


Fig. 7. Simulation results under balanced conditions (a) ZSVs of two converters, (b) ZSV difference, (c) ZSCC.

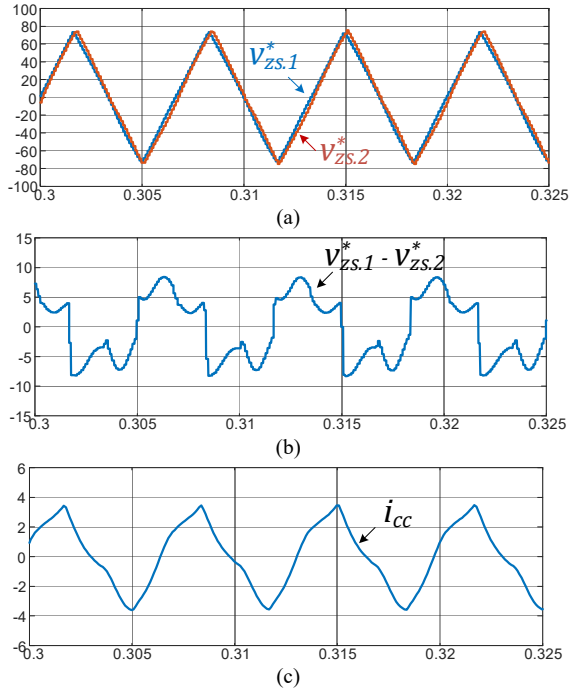


Fig. 8. Simulation results under unbalanced conditions. (a) ZSVs of two converters, (b) ZSV difference, (c) ZSCC.

zero ZSCC flows. This means that sufficient suppression results can be obtained with only conventional PI controller when the converters operate under balanced conditions.

On the other hand, Fig. 8 presents the results under the unbalanced conditions, that converter '1' and '2' are controlled with the constant current of 15A and 5A, respectively. As shown

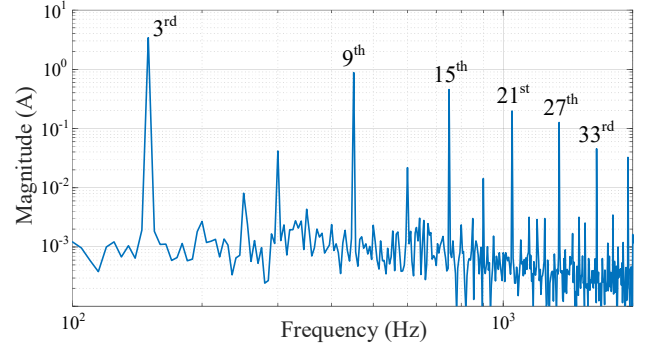


Fig. 9. Simulation result about FFT analysis of ZSCC.

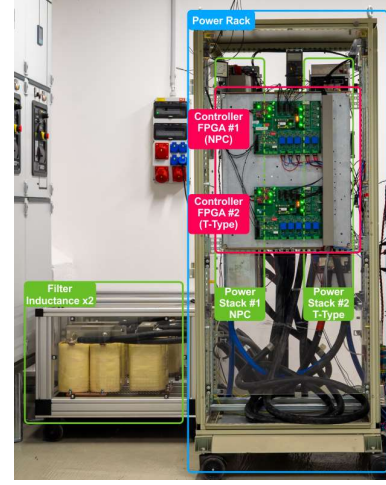


Fig. 10. Experimental setup.

in Fig. 8(a), two ZSVs do not entirely overlap each other compared to the result in Fig. 7(a), and voltage difference up to 8V is shown in Fig. 8(b). As a result, it can be confirmed from Fig. 8(c) that a triangular waveform of ZSCC occurs as analyzed in this paper. An FFT analysis is conducted in simulation to identify the harmonics in ZSCC, as shown in Fig. 9. The results show that $3(2m-1)$ order harmonics occur as described in Section III.

Fig. 10 shows the developed experimental setup, consisting of two parallel-connected three-level NPC converters with inductive filters. The experiments are carried out within the Table I conditions. In Fig. 11, experimental results about ZSCC and its FFT analysis according to the ZSCC controller conditions are shown. Similar to the results of Fig. 8(c), Fig. 11(a) shows that a triangular ZSCC with $3n$ harmonics component is generated (with $n=1, 3, 5, \dots, 2m-1$). A peak value of the ZSCC is about 4A, and the 3rd harmonic of up to 4.3A is measured. Considering the phase current conditions for two converters, this current is about 28% and 86%, respectively. This ZSCC may produce losses that cannot be ignored. This ZSCC ripple can be suppressed by applying the PR controller corresponding the 3rd harmonic, as shown in Fig. 11(b). The 3rd harmonic is reduced to 0.5A, but the 9th harmonic is instead increased from 1A to 1.6A. This is due to the characteristic of the PR controller. From this result, it is necessary to suppress not

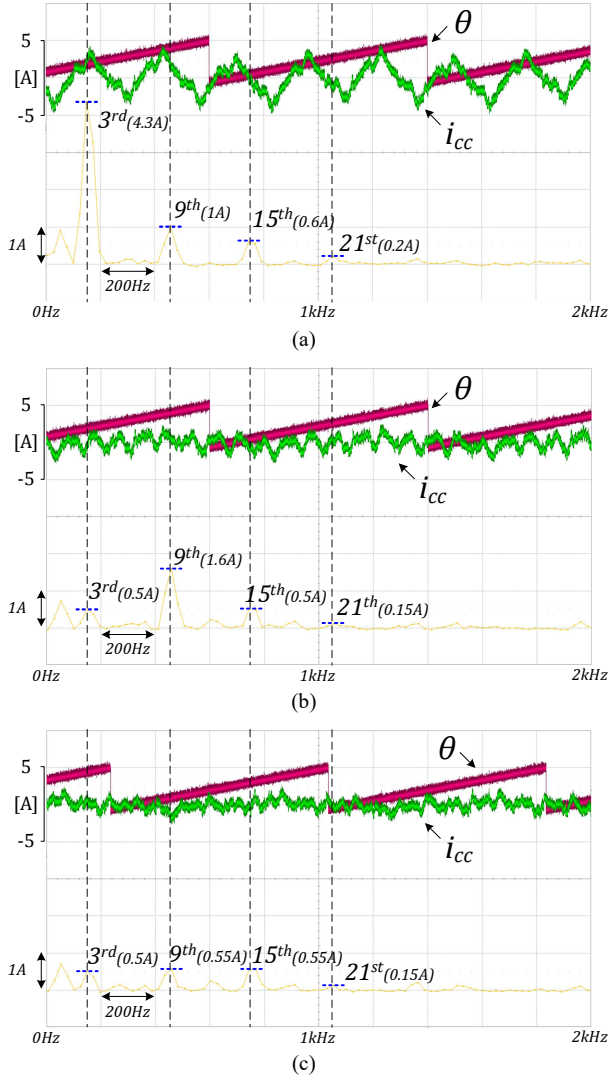


Fig. 11. Experimental results about ZSCC and its FFT analysis (a) P-controller (b) PR controller for 3rd harmonics, (c) PR controller for 3rd and 9th harmonics.

only the 3rd harmonic but also the remaining harmonics, including at least the 9th harmonic. So, a resonant controller for suppressing the 9th harmonic needs to be added to the existing PR controller used in the result of Fig. 11(b). As a result, the 9th harmonic is also reduced to about 0.55A like the 3rd harmonic. In conclusion, in order to reduce ZSCC more accurately and effectively, it is required to apply the controller such as multiple resonant controller to suppress the 3(2m-1) order harmonics as the result analyzed in this paper.

V. CONCLUSION

This paper analyzed ZSCC mathematically for the precise and optimized design of the ZSCC suppression controller.

Conventionally, a single-frequency PR controller is used for suppressing the ZSCC at the 3rd harmonic in parallel converter systems under the unbalanced load condition. However, in this paper, it has been shown that the ZSCC contains not only the 3rd harmonic and other 3(2m-1) order harmonics, such as the 9th and 15th, from the mathematical analysis based on the Fourier series. In the simulation results, it was validated that the ZSCC contains 3(2m-1) order harmonics, when the parallel converters are operated under the unbalanced load conditions. In addition, the necessity of applying additional resonance controllers as well as the controller for the 3rd harmonic was verified by the experimental results.

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