Management and Protection of High-Voltage Direct Current Systems Based on Modular Multilevel Converters

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M. Sc. ***Marius Langwasser***

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Kiel, den 25. Mai 2021

Marius Langwasser
Olshausenstraße 77
24106 Kiel

1. Gutachter:	Prof. Marco Liserre, Ph.D.
2. Gutachter:	Prof. Antonello Monti, Ph.D.
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To my wife Jasmin

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Deutsche Kurzfassung der Arbeit

Das Stromnetz erfährt in Folge der Integration von Erneuerbaren Energien und der Elektrifizierung des Verkehrs- und Wärmesektors tiefgreifende Veränderungen. Diese neuen Ressourcen sind typischerweise nicht planbar und abhängig von externen Faktoren (z. B. Wetter, Nutzerverhalten). Beide Aspekte führen zu schwerer vorhersehbarer Energieerzeugung und -bedarf und begünstigen so eine erhöhte Leistungsvariabilität. Folglich werden Störungen und das Aufrechterhalten der Versorgungsqualität herausfordernder, da schon geringe Leistungsungleichgewichte zu großen Frequenzschwankungen mit schnellen Transienten führen. Um diese Probleme zu bewältigen, benötigt das Energiesystem ein Infrastrukturupgrade sowie ein verbessertes Regelungssystem. In dieser Hinsicht können Hochspannungsgleichstromübertragungssysteme (HGÜ) die Regelbarkeit des Stromnetzes erhöhen und so die Integration zuvorgenannter Technologien fördern.

Diese Arbeit erweitert den Stand der Technik für HGÜ, indem die Modellierung, Regelung und der Schutz von HGÜ basierend auf modularen Multilevelumrichtern mit Fokus auf die Erbringung von Netzdienstleistungen für das Übertragungsnetz adressiert werden.

Studien zu HGÜ-Regelungs- und Schutzkonzepten erfordern eine akkurate Modellierung in stark voneinander abweichenden Zeitbereichen. Diese Arbeit stellt daher als ersten Schritt eine Richtlinie zur Bestimmung des notwendigen Modellierungsdetailgrads leistungselektronischer Komponenten in Abhängigkeit des betrachten Stromnetzphänomens vor.

Ausgehend von der geeigneten Modellierung für Stromnetzstudien, präsentiert diese Arbeit einen Ansatz zur HGÜ-basierten Primärfrequenzregelung, welcher den Lastbedarf flexibler, spannungsabhängiger Lasten mittels kontrollierter Blindleistungseinspeisung und entsprechender Netzspannungsregelung anpasst. Diese Lösung ermöglicht eine schnelle und akkurate Leistungsbalancierung und minimiert so die Frequenzschwankungen im Übertragungsnetz sowohl in der asynchronen als auch in der netzintegrierten HGÜ-Anwendung.

Eine zentrale Herausforderung für HGÜ ist eine geeignete Auslegung des Schutzsystems und insbesondere der Gleichstromschutzschalter, welche eine Analyse der Fehlerströme für eine Vielzahl an Netzzuständen und Parametern erfordern. Diese Arbeit nutzt das erworbene Wissen zu Modellierung und Regelung der HGÜ, um eine schnelle und akkurate Methodik zur Fehlerstromschätzung für modulare Multilevelumrichter-basierte HGÜ zu entwickeln. Unter Einbeziehung der HGÜ-Regelung ermöglicht der Algorithmus akkurate Prognosen des Maximalwerts sowie der Steilheit der Stromtransiente mit im Vergleich zu simulationsbasierten Verfahren stark verkürzter Rechenzeit.

Zuletzt wird in dieser Arbeit ein weiteres HGÜ-Schutzkonzept basierend auf einer hybriden Mischzellenumrichtertopologie ohne zusätzliche Schutzschalter untersucht, welches mit der minimal notwendigen Anzahl bipolarer Zellen eine mit Schutzschaltern vergleichbare Fehlerklärung und tolerierbare Zellüberspannungen erzielt.

English Summary

The electrical grid is undergoing large changes due to the massive integration of renewable energy systems and the electrification of transport and heating sectors. These new resources are typically non-dispatchable and dependent on external factors (e.g., weather, user patterns). These two aspects make the generation and demand less predictable, facilitating a larger power variability. As a consequence, rejecting disturbances and respecting power quality constraints gets more challenging, as small power imbalances can create large frequency deviations with faster transients.

In order to deal with these challenges, the energy system needs an upgraded infrastructure and improved control system. In this regard, high-voltage direct current (HVdc) systems can increase the controllability of the power system, facilitating the integration of large renewable energy systems.

This thesis contributes to the advancement of the state of the art in HVdc systems, addressing the modeling, control and protection of HVdc systems, adopting modular multilevel converter (MMC) technology, with focus in providing services to ac systems.

HVdc system control and protection studies need for an accurate HVdc terminal modeling in largely different time frames. Thus, as a first step, this thesis presents a guideline for the necessary level of deepness of the power electronics modeling with respect to the power system problem under study.

Starting from a proper modeling for power system studies, this thesis proposes an HVdc frequency regulation approach, which adapts the power consumption of voltage-dependent loads by means of controlled reactive power injections, that control the voltage in the grid. This solution enables a fast and accurate load power control, able to minimize the frequency swing in asynchronous or embedded HVdc applications.

One key challenge of HVdc systems is a proper protection system and particularly dc circuit breaker (CB) design, which necessitates fault current analysis for a large number of grid scenarios and parameters. This thesis applies the knowledge developed in the modeling and control of HVdc systems, to develop a fast and accurate fault current estimation method for MMC-based HVdc system. This method, including the HVdc control, achieved to accurately estimate the fault current peak value and slope with very small computational effort compared to the conventional approach using EMT-simulations.

This work is concluded introducing a new protection methodology, that involves the fault blocking capability of MMCs with mixed submodule (SM) structure, without the need for an additional CB. The main focus is the adaption of the MMC topology with reduced number of bipolar SM to achieve similar fault clearing performance as with dc CB and tolerable SM over-voltage.

Used symbols and abbreviations

General symbols

General symbols

$u(t)$, u	Time-variant variable
$\hat{u}$	Peak value
U	Constant value, average value
$\tilde{u}$	Phasor
$\mathbf{U}$	Matrix
Δ	Variation
(s)	Laplace domain operator
(t)	Time domain operator

Superscripts

$*$	Reference
^{i}	i-th component

Subscripts

0	Initial value
a, b, c	Phase a, b, c
ac	Alternating current
b	Base value for power, voltage, and current
dc	Direct current
d, q	Rotating dq-reference frame components
l	Lower arm component
ll	Line-to-line component
max	Maximum value
min	Minimum value
nom	Nominal value
n	Negative pole component
p	Positive pole component
ph	Phase-to-neutral component
SM	Submodule
u	Upper arm component

Special symbols

$\alpha_{c,ac}$	MMC output current controller closed-loop bandwidth
$\alpha_{i,ac}$	MMC output current controller integral part bandwidth
α_{Wdc}	MMC dc bus energy controller proportional part bandwidth
$\alpha_{i,Wdc}$	MMC dc bus energy controller integral part bandwidth
β	Phase constant
χ	Load active power to voltage sensitivity
δ	Angle between sending and receiving end voltages
$\delta\theta$	PWM carrier phase shift between the upper and the lower arm in the MMC
$\phi_{m,ac}$	MMC output current controller phase margin
θ_x	Generators rotational angle of the x-th area
θ^i	PWM carrier phase shift of i-th submodule
ρ_f	Frequency droop per unit decrement of the active power
ΣR_{on}	Sum of submodule IGBT on-state resistances
τ_{line}	Time constant of transmission line pi-section representation
τ_x	Internal dynamic state of the turbine transfer function of the x-th area
ω	Angular grid frequency, nominal angular speed of rotation
ω_1	Angular grid frequency in area 1
ω_2	Angular grid frequency in area 2
ω_{g1}	MMC angular grid frequency fundamental component
ω_r	Rotor speed of synchronous generators
ω_s	MMC angular sampling frequency
ξ	Traveling wave reflection coefficient
ζ	Traveling wave refraction coefficient
a	Symmetrical optimum dynamic coefficient
$\mathbf{A}$	Updated network incidence matrix without virtual nodes
$\mathbf{A}_t$	Network incidence matrix
$\mathbf{A}_{t1}$	Real node columns of network incidence matrix
$\mathbf{A}_{t2}$	Virtual node columns of network incidence matrix
$\mathbf{A}_z$	Bipolar network incidence matrix
$\mathbf{A}_{z1}$	Real node columns of bipolar network incidence matrix
c_{line}	Equivalent line capacitance per unit length
C_{arm}	Equivalent MMC arm capacitance of series connected FBSM
C_c	MMC dc side equivalent capacitance
C_{dc}	HVdc bus capacitor
C_{eq}	Equivalent MMC capacitor (of simplified MMC average value model)
C_{line}	Lumped equivalent line capacitance
C_{par}	Parasitic cable capacitance
C_{SM}	MMC submodule capacitance

$d_{\Delta dc}$	Differential power controller proportional gain
d_{ω}	Virtual friction constant
$d_{\omega 1}$	Area 1 power oscillation damping controller proportional gain
$d_{\omega 2}$	Area 2 power oscillation damping controller proportional gain
d_{dc}	V_{dc}-P-droop control proportional gain
d_{f}	V_{dc}-f-droop control proportional gain
d_{idc}	V_{dc}-I_{dc}-droop control proportional gain
d_{IE}	Emulated inertia controller proportional gain
d_{p}	P-f-droop control proportional gain
D	Load damping constant
E_{r}	Receiving end grid voltage
E_{s}	Sending end grid voltage
f	Grid frequency
F_{HP}	Turbine power fraction of high pressure section
F_{LP}	Turbine power fraction of low pressure section
g_{x}	Internal dynamic state of the governor transfer function of the x-th area
G	Isochronous governor proportional gain
G_{ac}	MMC output current controller electrical plant transfer function
$G_{c,ac}$	MMC output current controller closed-loop transfer function
G_{cir}	MMC circulating current controller electrical plant transfer function
G_{delay}	Modulation and computation delay transfer function
$G_{PI,ac}$	MMC output current PI-controller transfer function
$G_{o,ac}$	MMC output current controller open-loop transfer function
G_{Wdc}	MMC dc bus energy controller electrical plant transfer function
G_{x}	Governor transfer function of the x-th area
H	System inertia constant
H_{IE}	Emulated system inertia constant
i_{bij}	Branch current from node i to node j in negative pole of multi-terminal HVdc model
i_{c}	Circulating current MMC
i_{ci}	Injected current from i-th MMC in multi-terminal HVdc model
i_{d}	MMC output current d-component
i_{dc}	DC current
$i_{dc,bus}$	DC bus input current
i_{ij}	Branch current from node i to node j in positive pole multi-terminal HVdc model
i_{l}	Lower arm current MMC
i_{par}	Current through parasitic cable capacitors
i_{q}	MMC output current q-component
i_{trip}	Converter fault current trip threshold

i_s	Phase (output) current MMC
i_{SM}	MMC submodule current
$i_{sMMC,i}$	Source current from i-th MMC in multi-terminal HVdc model
i_u	Upper arm current MMC
i_x	Internal dynamic state of the rotor inertia and load damping transfer function of the x-th area
I_r	Receiving end current
I_s	Sending end current
I_x	Rotor inertia and load damping transfer function of the x-th area
J	Moment of inertia of rotating masses
k_{bal}	Decentralized MMC submodule balancing controller proportional gain
$k_{i,ac}$	MMC output current controller integral gain
$k_{i,cir}$	MMC circulating current controller integral gain
$k_{i,Wdc}$	MMC dc bus energy controller integral gain
$k_{p,ac}$	MMC output current controller proportional gain
$k_{p,cir}$	MMC circulating current controller proportional gain
$k_{p,Wdc}$	MMC dc bus energy controller proportional gain
k_{Vdc}	Droop-constant of the P_{dc}-V_{dc}-droop control
k_{Vdci}	Droop-constant of the I_{dc}-V_{dc}-droop control
$\mathbf{K}$	Network capacitance matrix
K_{fp}	Load active power to frequency dependency
K_p	Load active power to voltage dependency
l_{fault}	Fault distance to terminal
l_{line}	Equivalent line inductance per unit length
$\mathbf{L}$	Updated network inductance matrix without virtual nodes
L_{arm}	Arm inductance MMC
L_c	MMC dc side equivalent inductance
L_{dc}	DC current limiting inductance
L_{eq}	Equivalent inductance of simplified MMC average value model
L_f	MMC ac-side filter inductance
L_{line}	Lumped equivalent line inductance
$\mathbf{L}_t$	Network inductance matrix
L_{sc}	Short circuit path inductance
m	Modulation index
m_{dc}	MMC dc modulation index
m_{MOV}	Number of bypassed dc CB main breaker modules
m_o	MMC over-modulation index
M	Equivalent system inertia
n_{cd}	Number of CDSM in one MMC arm
n_{cs}	Number of CSSM in one MMC arm

n_{f}	Number of FBSM in one MMC arm
$n_{\mathrm{f,n}}$	Number of negative state FBSM in one MMC arm
n_{h}	Number of HBSM in one MMC arm
n_{i}	i-th node in multi-terminal HVdc model
n_{l}	MMC lower arm insertion index
n_{l}^{i}	MMC insertion index of i-th submodule in lower arm
n_{MOV}	Number of dc CB main breaker modules
n_{mt}	Number of converter terminals in multi-terminal HVdc system
n_{SM}	Total number of MMC submodules per arm
n_{u}	MMC upper arm insertion index
n_{u}^{i}	MMC insertion index of i-th submodule in upper arm
p_{i}	Per unit share of constant current load
p_{p}	Per unit share of constant power load
p_{x}	Proportional share of frequency support in the x-th area
p_{z}	Per unit share of constant impedance load
P	Active power
P_{39bus}	HVdc active power set-point in IEEE 39-bus system
P_{Δ}	Differential power in multi-terminal HVdc systems
P_{cm}	Common power in multi-terminal HVdc systems
$P_{\mathrm{dc,bus}}$	DC bus input power
P_{e}	Synchronous generators' electrical power
P_{kundur}	HVdc active power set-point in Kundur benchmark system
P_{L}	Load active power consumption
P_{m}	Synchronous generators' mechanical power
P_{o}	Terminal output power in multi-terminal HVdc systems
P_{r}	Receiving end active power
Q	Reactive power
Q_{r}	Receiving end reactive power
r_{line}	Equivalent line resistance per unit length
R	Governor frequency droop constant
$\mathbf{R}$	Updated network resistance matrix without virtual nodes
R_{arm}	Arm resistance MMC
R_{c}	MMC dc side equivalent resistance
R_{eq}	Equivalent resistance of simplified MMC average value model
R_{f}	MMC ac-side filter resistance
R_{line}	Lumped equivalent line resistance
$\mathbf{R}_{\mathrm{t}}$	Network resistance matrix
R_{sc}	Short circuit path resistance
S	Apparent power
S_{i}	i-th switch of MMC submodule

S_{rated}	Nominal power rating of synchronous generators
t	Time
t_{d}	Communication delay of primary frequency regulation
t_{op}	DC CB operating time
T	Fundamental period
T_{ac}	MMC output current controller electrical plant time constant
T_{CH}	Turbine main inlet volume time constant
T_{delay}	Modulation and computation delay time constant in MMC
T_{e}	Synchronous generators' electrical torque
T_{G}	Governor time constant
$T_{\text{i,ac}}$	MMC output current controller time constant
$T_{\text{i,cir}}$	MMC circulating current controller time constant
$T_{\text{i,Wdc}}$	MMC dc bus energy controller time constant
T_{m}	Synchronous generators' mechanical torque
T_{p}	Load recovery time constant
T_{RH}	Turbine reheater time constant
T_{s}	MMC sampling period
T_{x}	Turbine transfer function of the x-th area
v_{ac}	AC voltage, grid voltage
v_{arm}	MMC arm voltage
$v_{\text{arm,dc}}$	MMC dc-side arm voltage
v_{c}	Inner voltage MMC
v_{ci}	Voltage across equivalent capacitor of i-th MMC in multi-terminal HVdc model
v_{dc}	DC voltage
v_{par}	Voltage across parasitic cable capacitors
v_{l}	Lower arm voltage MMC
$v_{\text{ll,ab}}$	Line-to-line voltage between phase a and phase b
v_{ldc}	Lower arm dc voltage
v_{n0}	Voltage between ac neutral point and dc side ground
v_{s}	Output side emf MMC
v_{u}	Upper arm voltage MMC
v_{udc}	Upper arm dc voltage
$v_{x\text{n}}$	Phase-to-neutral voltage of phase x
V_{ac}	MMC output current controller electrical plant proportional gain
V_{SM}^{Σ}	Sum capacitor voltage MMC
$V_{\text{c,i}}$	MMC submodule capacitor voltage of i-th capacitor
V_{L}	Load voltage at point of connection
V_{PL}	Arrester protection voltage level
V_{o}	MMC submodule output voltage

V_{SM}	Nominal MMC submodule voltage
W_{ac}	Effective AAC ac-side energy
W_{dc}	Effective MMC/AAC dc bus energy
W_{MMC}	MMC energy equilibrium
x	Position at the line
x_{fault}	Fault position at the line
X_{ac}	Lumped equivalent transmission line impedance
Y	Turbine control valve position
Y_{line}	Lumped equivalent admittance of transmission line pi-section representation
Z_c	Characteristic line impedance
Z_l	Equivalent wave impedance of transmission line
Z_{line}	Lumped equivalent impedance of transmission line pi-section representation
Z_x	Equivalent wave impedance at point x

Abbreviations

AAC	alternate arm converter
ac	alternating current
ADSM	asymmetrical double submodule
AFCE	analytical fault current estimation
ASB	auxiliary semiconductor breaker
AVR	automatic voltage regulation
BESS	battery energy storage system
CB	circuit breaker
CCSM	cross-connected submodule
CIGRE	Conseil International des Grands Reseaux Electriques
CDSM	clamp double submodule
CSSM	clamp single submodule
dc	direct current
DBSM	diagonal bridge submodule
DSO	distribution system operator
EMT	electro-magnetic transient
ENTSO-E	European Network of Transmission System Operators for Electricity
ESS	energy storage system
FACTS	flexible ac transmission system
FB	full-bridge
FC	flying capacitor

FF	feed forward
FRT	fault ride through
HB	half-bridge
HCMC	hybrid cascaded multilevel converter
HMMC	hybrid modular multilevel converter
HA-MMC	hybrid arm modular multilevel converter
HV	high-voltage
HVac	high-voltage alternating current
HVdc	high-voltage direct current
IE	inertia emulation
IEEE	Institute of Electrical and Electronics Engineers
IGBT	insulated gate bipolar transistor
LCC	line commutated converter
LV	low-voltage
LVRT	low-voltage ride through
MMC	modular multilevel converter
MMCC	modular multilevel cascade converter
MOSFET	metal oxide semiconductor field-effect transistor
MOV	metal oxide varistor
MSB	main semiconductor breaker
MTdc	multi-terminal high-voltage direct current
MV	medium-voltage
NPC	neutral point clamped
OHL	overhead line
OLTC	on-load tap changer
PCC	point of common coupling
P2G	pole-to-ground
P2N	pole-to-neutral
P2P	pole-to-pole
PE	power electronics
PFR	primary frequency regulation
PI	proportional-integral
PLL	phase-locked loop
POD	power oscillation damping
PR	proportional-resonant
PV	photo-voltaic
RCB	residual current breaker
RES	renewable energy system
RoCoF	rate of change of frequency
SCDSM	series connected double submodule

SM	submodule
ST	Smart Transformer
STATCOM	static synchronous compensator
TIV	transient interruption voltage
TSO	transmission system operator
U-FBSM	unipolar full-bridge submodule
UFMS	ultra-fast mechanical switch
VDE	Verband der Elektrotechnik Elektronik Informationstechnik e. V.
VDL	voltage-dependent loads
VSC	voltage source converter

1. Introduction

The European Network of Transmission System Operators for Electricity (ENTSO-E) state in 2019 [1]:

> **High voltage direct current (HVdc) is an increasingly important technology for transferring electrical power in the European transmission grid.**

In this sense, HVdc systems play a key role in the future development of the European (see Fig. 1.1) and worldwide power system [2]. System operators all over the world see HVdc systems as a possibility to tackle the current and future challenges in the electrical grid (compare worldwide installed capacity in Fig. 1.2), which are introduced by the global trends towards decarbonization, large scale integration of renewable energy systems (RES) with fluctuating power generation, and electrification of transport and heating sectors [1]. The decommissioning of conventional rotating power plants, moreover, leads to low system inertia and the agglomeration of the RES power plants in remote grid areas requires bulk power transfer over large distances. In this scenario, the HVdc's advanced functionalities are considered essential for the secure and efficient grid operation in the future. In addition, from a non-technical perspective, HVdc can help to establish a transnational energy market, potentially also combining different synchronous areas [1].

To date, HVdc systems are mostly applied to connect two asynchronous, non-embedded ac systems or for bulk power transfer through overhead transmission lines and submarine ca-

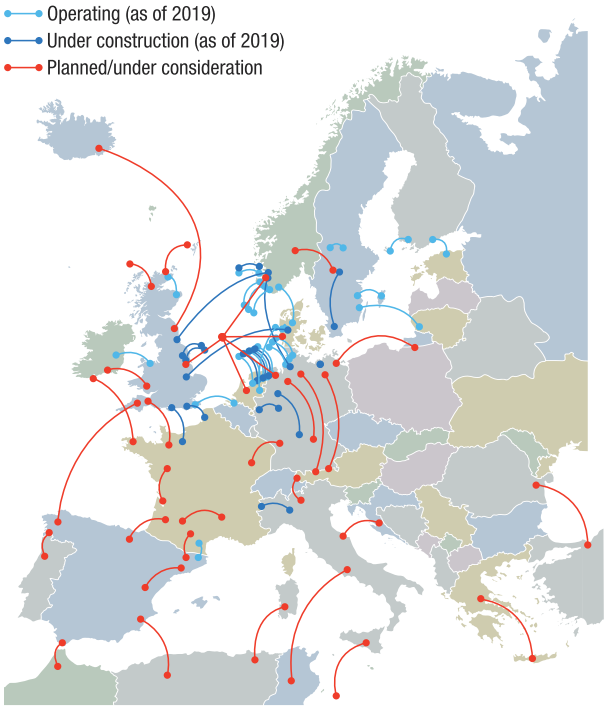


Fig. 1.1: HVdc installations in Europe (Status 2019/2020) [2].

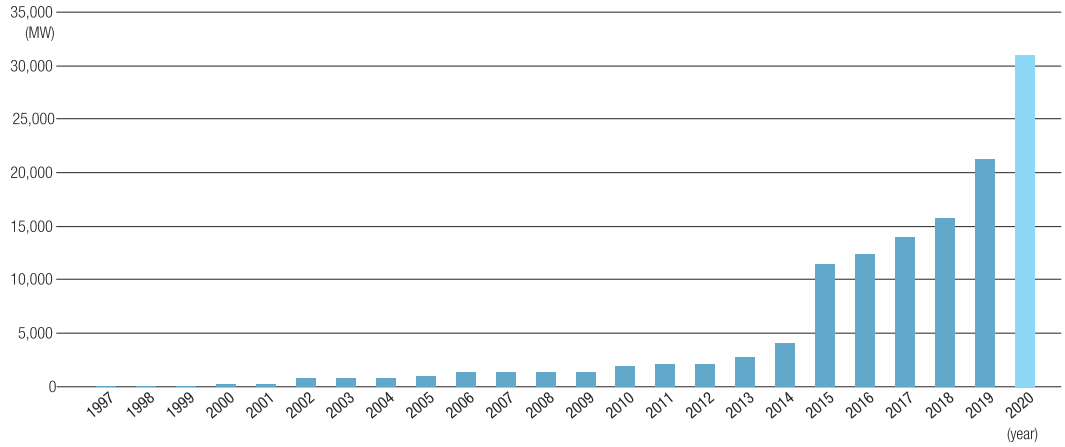


Fig. 1.2: Global trend of total MW capacity of HVdc installations 1997-2020 [2].

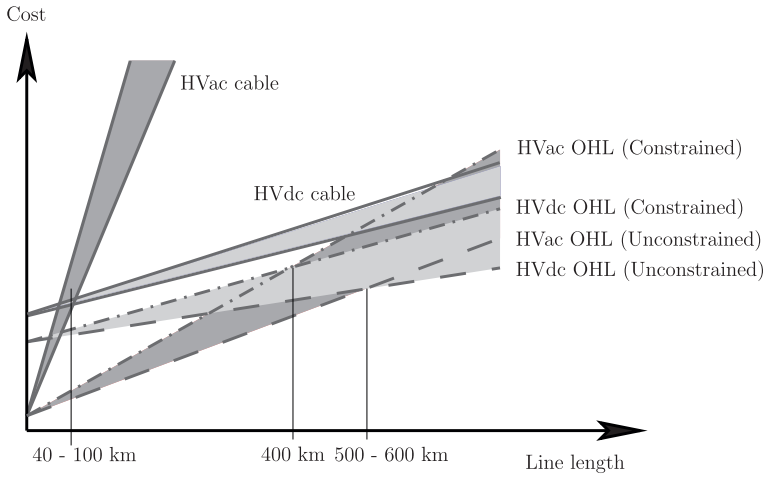


Fig. 1.3: Cost breakdown for HVac and HVdc systems (adapted from [4]).

bles [1]. In these applications, HVdc systems present a number of advantages over their high-voltage alternating current (HVac) counterpart. First, HVdc systems eliminate the reactive power requirement and reduce the operational losses, which enables long-distance power transmission through cables or overhead lines. Also, the power transfer capability of a single conductor is higher and the HVdc can be installed with reduced right of way, since only a maximum of two instead of the three ac conductors are required [2, 3]. Moreover, the HVdc systems enable asynchronous active power transfer and independent reactive power provision, which prevents cascading failures and can help to stabilize the grid. However, due to the much more complex system equipment, such as transformers, circuit breakers and protection components and especially the high costs of the power electronics parts, HVdc systems are only economically rational beyond a certain break-even distance [1]. The break-even distance varies with technical and non-technical constraints (e.g. easier permitting process, more open space to place transmission lines), so that the two technologies compete within a certain range as indicated in Fig. 1.3.

1.1. Motivation of advanced HVdc-based grid services

Especially the growing technology readiness of modular multilevel converter (MMC)-based HVdc systems, which to date reach voltage levels of up to ±500 kV and power transmission capacity of up to 3000 MW per terminal, facilitates the provision of grid services to guarantee power supply continuity and grid stability under the future grid scenario. Depending on the application of the HVdc system, it is more suited for active power related services, which is the case for long HVdc corridors or interconnectors, or the provision of reactive power related services, valid for embedded HVdc systems in highly meshed ac grids [5]. Many different services have been proposed in the last couple of years to address classical power system problems, such as power flow control and curative congestion management [5, 6], voltage and reactive power control both in steady-state [7] and dynamic condition [8, 9], and damping of power oscillations to increase the rotor angle stability [10, 11, 12]. Moreover, HVdc systems are also highly suitable to support the active power and frequency control [13, 14, 15] and emulate virtual inertia [16, 17, 18], especially under low inertia conditions, which result from the de-commissioning of conventional power plants [19], and can act as a black-start resource for grid restoration purposes [20, 21].

However, the provision of frequency services with HVdc systems, such as primary frequency regulation and inertia emulation, has one common drawback: If no additional source of energy by e.g. either wind farms or battery energy storage systems is provided, unwanted disturbances occur in the supporting grid areas [15]. Moreover, embedded HVdc systems, which by definition inhabit both terminals in the same synchronous area and thus the two terminal frequencies are strongly coupled [22], are to date not suitable to damp frequency oscillations by simple active power modulation, as the HVdc itself is not a source of energy [5].

Flexible, voltage-dependent loads have already been considered in the balancing of load demand and power generation as well as for the provision of services for a couple of years [23] and shaping their power consumption by controlled grid variation has seen several applications with static var compensators [24], synchronous condensers [25], and smart transformers [26]. Thus, it is a logical consequence to extend this concept to HVdc systems to fully exploit their potential in frequency service provision. What has to be noted, is that the necessary change in the grid voltage to shape the loads' power consumption by HVdc systems is restricted by the current grid codes of ENTSO-E [27] and technical requirements for HVdc connection of the German association Verband der Elektrotechnik Elektronik Informationstechnik e. V. (VDE) [28]. Thus, further potential is seen in multi-terminal HVdc systems, in which the power flow can be controlled flexibly [29, 30] and the frequency support can be provided from different loads in the different connected areas.

1.2. Motivation of analytical design methods for HVdc circuit breakers

One key challenge since the beginning of HVdc systems is their protection in the event of a short circuit fault. While in ac systems the current naturally crosses through zero, in dc systems an artificial zero crossing must be created to avoid large arc and to guarantee save fault current interruption. Moreover, the low line impedance of dc systems leads to high fault currents with fast transients, which poses additional challenges to the protection system [31].

Depending on the chosen protection philosophy, i.e. if it is allowed to shut down the whole HVdc system (non-selective), subparts of it (partially-selective) or just the faulted line (fully-selective), the primary protection scheme can be based on ac circuit breakers (CB), integrated in converters with fault blocking capability, or based on dc CB, which form the only fully-selective solution [32]. Several different types of dc CB have been proposed, which are passive resonant mechanical breakers [33], active current injection mechanical breakers [33], solid-state breakers [34] or the most-promising technology: hybrid dc CB [35]. While the mechanical breakers suffer from comparably long opening times of the mechanical switch, pure solid-state breakers are to date not commercially available and introduce high on-state losses. Thus, the current focus lays on the development of hybrid dc CB, which combine the high efficiency of mechanical switches with the fast switching properties of solid-state devices. To date only a few hybrid dc CB designs are commercially available [36, 37, 38]. The requirements on dc CB are manifold [31, 39, 40] and it is of utmost importance to evaluate the performance of newly introduced designs as well as the proven ones in a large number of different grid scenarios considering different parameters related to the breaker design itself, as well as the grid operating condition, and secondary technology such as communication infrastructure.

For such purpose, analytical fault current estimation methods are introduced, which can facilitate and speed up the design process of dc CB and hence already save costs in the initial stage of development of dc CB. The recent methods to estimate fault currents in multi-terminal HVdc (MTdc) systems can be classified in three types, which are to simulate (e.g. using EMT-simulations) all the possible fault conditions and then evaluate the worst-case scenario [41], the classical analytical approach based on traveling wave analysis [31, 42], and lastly an analytical estimation based on circuit analysis through coupled linear differential equations [43, 44]. However, EMT-simulation based methods are very time consuming and rely on detailed models of converters and transmission systems, which require data not always available due to property restrictions. Indeed, traveling wave analysis is seen as the potential standard in fault current estimation. Nevertheless, it requires the solution of lengthy equations to obtain the exact time-domain solution, which are also valid only in the temporal and spatial proximity of the fault, and thus the approach might be impractical to analyze the individual parameter's impact on the protection design [42]. In contrast, using mesh

analysis based on linear differential equations is regarded as a simple yet accurate approach to determine the most relevant design parameters, fault current slope and maximum peak current, and gives the possibility to investigate multiple parameter variations in short time. However, a clear drawback of existing methods in this field is that they are either applicable only to conventional voltage source converter systems [43] or use oversimplified models of the MMC, which leads to inaccurate estimation results in multi-terminal systems [44].

Hence, it has been identified as an of yet open research field, an analytical fault current estimation method for modular multilevel converter-based MTdc systems, which facilitates parameter variation analysis with reasonable computational effort and is also applicable not only to a single fault scenario or HVdc system configuration, but can be extended to analyze different ones, such as pole-to-pole and pole-to-neutral faults in symmetrical monopole and bipolar HVdc configurations.

The HVdc CB - being a component of relatively high costs - can be not only applied for its conventional purpose, the fault clearing process, but can also be involved in the reclose and restart function after a temporary fault happened. In order to achieve a faster restoration and to avoid multiple reclosing attempts in the event of permanent faults, recently adaptive auto-reclosing strategies have been proposed [45], which identify the fault type prior to initiating the reclosing operation using either the MMC [46] or a hybrid dc CB based on full-bridge architecture in the main breaker path [47]. Thus, it is interesting to investigate, if the same functionality can be also implemented in different dc CB designs, for example in the modular dc CB presented by ABB [36].

1.3. Motivation of modular multilevel converter-based HVdc protection

Despite using additional protection equipment such as dc CB, another possible protection method is to embed the dc fault blocking in the converter station [48]. The conventional MMC using half-bridge submodules (SM) is vulnerable to dc faults, because it behaves as an uncontrolled diode rectifier in the blocked state feeding the fault point [49].

Thus, MMCs, which inhabit the fault blocking feature, must provide reverse-biased voltage in the blocked state in order to prevent uncontrolled current flow from the ac to the dc side during the fault [50]. This requires special considerations in the SM, for which several designs, among others the full-bridge SM [50], clamped-double SM [50], or cross-connected SM [49] have been developed. However, these bipolar or asymmetric SM, due to their higher number of switches, increase the converter losses in normal operation and involve higher investment costs than the cost-efficient half-bridge SM.

Hence, new converter architectures have been proposed, which combine the SM with fault blocking ability with half-bridge SM. If both SM types are used in both converter arms, the

topology is known as hybrid MMC [49, 51] and if the SM types are only used in separate arms, e.g. the bipolar SM in the upper arm and the half-bridge SM in the lower arm next to the ground pole, it is defined as hybrid arm MMC [52]. The hybrid arm topology is beneficial compared to the hybrid MMC due to its superior performance under ac faults [53].

For the hybrid MMC, it has already been shown that the fault blocking function can be also enabled with a reduced number of bipolar SM in order to further reduce the costs of the system [51], which is vital, since the industry involved in the operation of HVdc systems is very cost-sensitive, so that even fractions of a percent in efficiency improvements are important [54]. It is left to be demonstrated, what is the minimum number of SM in a hybrid arm MMC - from an operational perspective - to obtain the fault blocking capability, while maintaining high efficiency.

1.4. Research proposal

The aim of the thesis is to investigate the services HVdc systems can provide to the ac grid and to analyze the protection concepts of MTdc systems. Control solutions to implement frequency regulation with minimum impact on the power system and the HVdc system itself are developed. Moreover, the fault currents in HVdc systems are analyzed in order to determine and evaluate criteria for the design of HVdc CB under different grid conditions. Lastly, an adapted design of the hybrid arm MMC is presented to achieve fault blocking capability with increased efficiency in normal operation.

Target I: Development of a control solution for HVdc-based primary frequency regulation and inertia emulation

The first objective is the development and design of an HVdc-based primary frequency regulation and virtual inertia emulation scheme, which has minimum impact on the supporting ac areas in terms of frequency and voltage disturbances. Moreover, the scheme should be effective in suppressing frequency oscillations in both asynchronous HVdc interconnectors and embedded HVdc systems forming parallel, hybrid connection with an existing HVac grid.

It is proposed to shape (upward and downward) the power consumption of voltage dependent loads in the proximity of the HVdc terminals by varying the grid voltage amplitude in order to raise additional source of energy for the frequency support, which is independent from the synchronous generators and thus does not affect the supporting area's frequency. The effectiveness of the proposed control scheme is analyzed for both asynchronous HVdc interconnectors and embedded HVdc systems considering also the limitations imposed by the current grid codes and power system condition. Furthermore, the control scheme is expanded to MTdc systems, in which the focus is laid on the optimal selection of the frequency

support share. Adjusting the droop coefficients relative to the estimated load voltage dependence (also known as sensitivity), allows the provision of the same frequency service with less impact on the grid voltage in the supporting areas and lower reactive power injection.

Target II: Analytical fault current estimation in multi-terminal HVdc systems for HVdc circuit breaker design

The second research objective is to investigate the fault current behavior in MMC-based MTdc systems and suitable dc CB designs to protect such systems. A generalized list of criteria is developed from the numerous existing studies to evaluate the suitability of hybrid HVdc CB designs for a given grid scenario. The assessment of these criteria requires the development of a fault current estimation method for dc CB design purposes, which allows complex parameter variation analysis with limited computational effort for various fault scenarios in an MMC-based MTdc system. Mesh analysis with linear differential equations and modified average value model of the MMC is targeted to estimate the fault currents. In order to overcome the limitations of existing methods, the power flow in the converter during the fault time is included by considering the outer control loops. Moreover, it is analyzed how the fault current estimation can be extended to bipolar HVdc configuration, in which both pole-to-pole and pole-to-neutral faults can be investigated. Detailed parameter analysis is presented, which allows the evaluation of the suitability of recent dc circuit breaker designs for given grid and fault conditions. Additionally, adaptive auto-reclosing schemes are analyzed and the modular hybrid dc CB shall be exploited to inject active dc voltage pulses in the grid, in order to analyze the fault type by means of traveling wave analysis. In case of permanent faults, the same approach can be used to locate the fault position and in case of temporary faults, a smooth dc voltage build-up is presented by sequentially switching the dc CB main breaker modules off.

Target III: Analysis of the fault blocking capability of hybrid arm modular multilevel converter with reduced number of bipolar submodules

As the third research contribution, the fault blocking capability of MMC will be analyzed and an adapted topology of the hybrid arm MMC is targeted, which includes the minimum required number of bipolar SM, here the established full-bridge SM are chosen, to achieve acceptable fault clearing performance in terms of clearing time and SM over-voltage and reduced on-state losses. The minimum number of SM as well as the worst-case SM over-voltage will be derived analytically based on the fault operation sequence of the hybrid arm MMC.

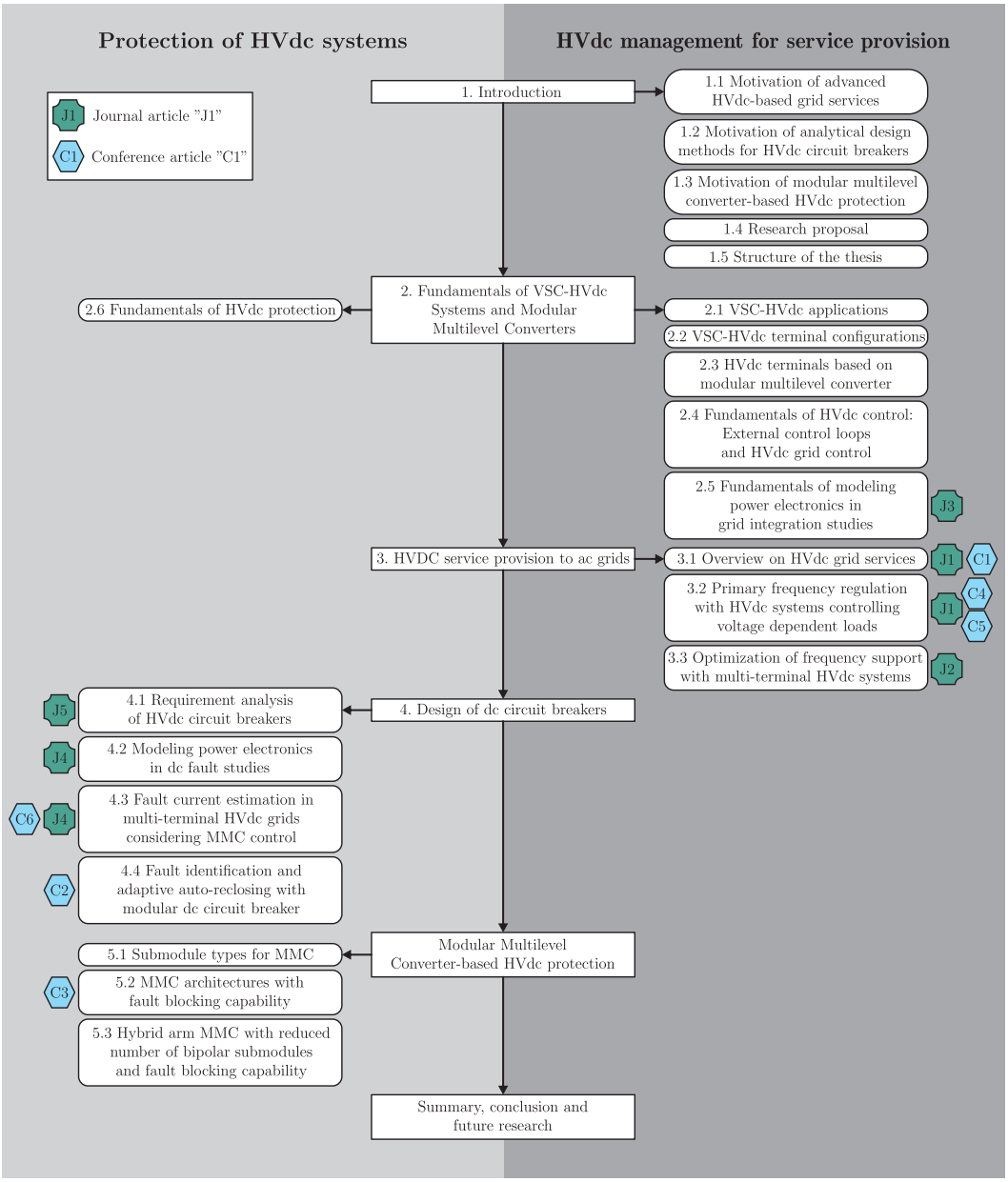


Fig. 1.4: Structure of the thesis and related publications.

1.5. Structure of this thesis

The topics investigated in this thesis are organized into six chapters as depicted in Fig. 1.4 along with their associated publications.

Section 2 provides the necessary theoretical basis for the presented work. HVdc system applications and configurations are explained, as well as the different possibilities to control and protect (multi-terminal) HVdc systems. Additionally, the fundamental operation of the MMC in HVdc terminals and its basic controller design is presented, which is used in the simulation models throughout this thesis. Moreover, a guideline to model power electronics in power system studies is presented, which deals with power system stability problems and is used to define the necessary deepness of modeling for the primary frequency regulation

method presented in **Section 3**.

In **Section 3**, at first, an overview on HVdc grid services is given, which focuses on the control implementation and highlights the shortcomings of existing methodologies, especially referring to frequency regulation aspects. In the following, a HVdc-based primary frequency regulation method is presented, which is based on the control of voltage dependent loads and thus overcomes the limitation of undesired frequency disturbances in supporting areas, which are present in the state of the art methodologies, and is applicable not only to asynchronous but also to embedded HVdc systems, which is demonstrated analytically and proven with PSCAD/EMTDC simulations. Necessary fundamentals on load modeling and control as well as the power system representation for frequency control studies are given. Finally, a combination of primary frequency regulation and inertia emulation (referred to as enhanced frequency support) is proposed for MTdc systems, considering optimized share of the frequency support respecting the estimated load power to voltage sensitivity.

Section 4 deals with design requirements of HVdc CB and analytical fault current estimation methods to evaluate those. It is proposed an analytical fault current estimation method based on coupled differential equations and mesh analysis, which accurately determines the current slope and maximum fault currents for pole-to-pole and pole-to-neutral faults in symmetrical monopole and bipolar HVdc configurations. The section is concluded by proposing an adaptive auto-reclosing strategy and fault type identification using the modular hybrid dc CB.

HVdc systems can be protected either by using dc CB as presented in **Section 4** or by employing fault blocking capability of the MMC in the HVdc terminals. A new perspective is put on the design of hybrid arm MMC, for which the minimum number of bipolar SM to achieve fault blocking capability with increased on-state efficiency is evaluated analytically from the converter's fault operation sequence in **Section 5**.

Finally, **Section 6** is dedicated to the summary of this thesis, followed by the conclusion and future research.

1.6. List of publications

The list of scientific papers associated with this thesis are given as follows:

Journal publications

J1 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Primary Frequency Regulation Using HVDC Terminals Controlling Voltage Dependent Loads," in *IEEE*

Transactions on Power Delivery, vol. 36, no. 2, pp. 710-720, April 2021, doi: 10.1109/TPWRD.2020.2990565.

J2 **M. Langwasser**, G. De Carne, M. Liserre, and M. Biskoping, "Enhanced grid frequency support by means of hvdc-based load control," in *Electric Power Systems Research*, vol. 189, p. 106552, December 2020, doi: 10.1016/j.epsr.2020.106552.

J3 G. De Carne, **M. Langwasser**, M. Ndreko, R. Bachmann, R.W. De Doncker, R. Dimitrovski, B.J. Mortimer, A. Neufeld, F. Rojas and M. Liserre, "Which Deepness Class Is Suited for Modeling Power Electronics?: A Guide for Choosing the Right Model for Grid-Integration Studies," in *IEEE Industrial Electronics Magazine*, vol. 13, no. 2, pp. 41-55, June 2019, doi: 10.1109/MIE.2019.2909799.

J4 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Fault Current Estimation in Multi-Terminal HVdc Grids Considering MMC Control," in *IEEE Transactions on Power Systems*, vol. 34, no. 3, pp. 2179-2189, May 2019, doi: 10.1109/TPWRS.2018.2887166.

J5 **M. Langwasser**, G. D. Carne, M. Liserre, and M. Biskoping, "Requirement analysis of hybrid direct current breaker in multi-terminal high-voltage direct current grids," *Journal of Engineering*, vol. 2018, no. 15, pp. 1066-1071, October 2018, 10.1049/-joe.2018.0267.

Conference publications

C1 **M. Langwasser**, K. Schoenleber, A. Wasserrab, M. Thiele, and M. Liserre, "Online estimation of dynamic capacity of vsc-hvdc systems: Power system use cases," *Internationaler ETG-Kongress 2021*, 2021.

C2 H. Iman-Eini, **M. Langwasser**, L. Camurca and M. Liserre, "Modular Hybrid DC Breaker-based Adaptive Auto-Reclosing Method for MMC-HVDC Systems," *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1-P.9, doi: 10.23919/EPE20ECCEEurope43536.2020.9215743.

C3 **M. Langwasser**, H. Imaneini, G. De Carne and M. Liserre, "Estimation and Interruption of Short Circuit Currents in HVDC Systems," *2019 IEEE Power & Energy Society General Meeting (PESGM)*, 2019, pp. 1-5, doi: 10.1109/PESGM40551.2019.8973517.

C4 **M. Langwasser**, M. Biskoping, G. D. Carne and M. Liserre, "Frequency support provision by parallel, hybrid HVDC-HVAC system with Voltage-based Load Control," *2019 IEEE Milan PowerTech*, 2019, pp. 1-6, doi: 10.1109/PTC.2019.8810519.

C5 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Voltage-Based Load Control for Frequency Support Provision by HVDC Systems," *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 311-316, doi: 10.1109/IECON.2018.8592709.

C6 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Improved Fault Current Calculation Method for Pole-to-Pole Faults in MMC Multi-Terminal HVDC Grids Considering Control Dynamics," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 5529-5535, doi: 10.1109/ECCE.2018.8557979.

2. Fundamentals of VSC-HVdc systems and modular multilevel converters

Modern HVdc systems can be classified in line-commutated converter HVdc (LCC-HVdc) using thyristor bridges in current source converter topology and voltage-source converter HVdc (VSC-HVdc) using forced-commutated power electronic switches such as high-voltage IGBTs [1]. A typical arrangement of a LCC-HVdc converter terminal using the 12-pulse thyristor bridge is shown in Fig. 2.1.

VSC-HVdc systems exist with three-different converter topologies (see terminal arrangement in Fig. 2.2). While the first commercial VSC-HVdc applications were built adopting two-level converters (like the Gotland HVdc project installed by ABB in 1997 [55]), also three-level neutral point clamped (NPC) converters are in use (MurrayLink Australia [4]). To date, most new VSC-HVdc installations are based on variants of the MMC. What differs among the manufacturers is the basic SM configuration. The technology of ABB, also known under the brand name HVdc Light, is based on series-connected insulated gate bipolar transistors (IGBT) in a double SM configuration, while Siemens and General Electric (formerly Alstom) use the MMC in its conventional structure without serialization in half-bridge (Siemens, known as HVdc Plus) and full-bridge (GE/Alstom, known as HVdc MaxSine) SM configuration [56, 4].

Table 2.1 summarizes the comparison between LCC- and VSC-HVdc systems.

As can be seen, VSC-HVdc systems present a number of advantages in comparison to their LCC counterpart [57], which are

- Independent active and reactive power control (no reactive power compensation is required)
- AC voltage support either in STATCOM mode or also while transmitting active power

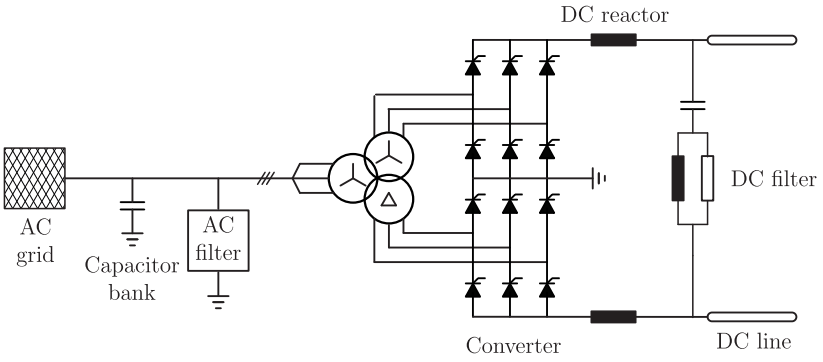


Fig. 2.1: Typical arrangement of 12-pulse LCC-HVdc terminal (modified from [1]).

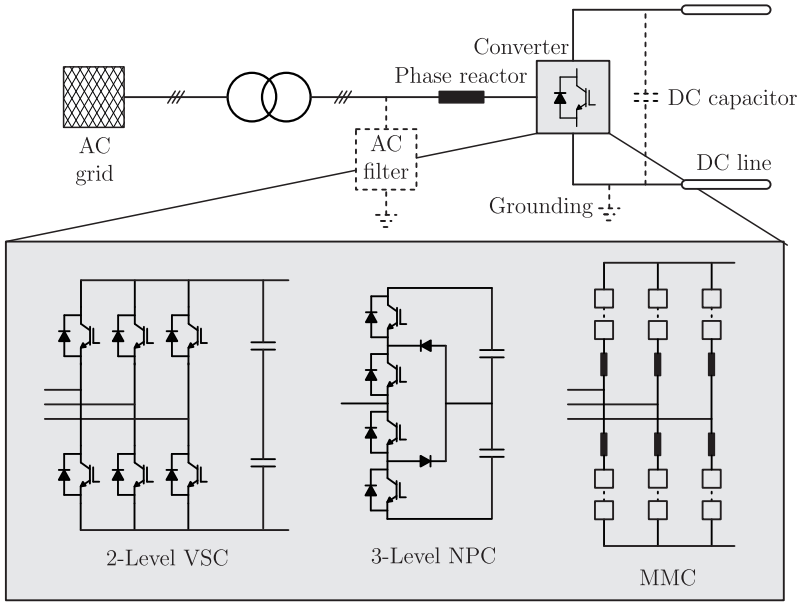


Fig. 2.2: Typical arrangement of VSC-HVdc terminal with 2-Level VSC, 3-Level NPC (single phase representation), and MMC.

- Fast active power reversal by reversing the current direction (dc voltage polarity is kept the same)
- Reduced filtering requirement and thus smaller footprint
- Service provision to the ac grid, such as black-start capability, low-voltage ride through (LVRT), fast frequency and damping support through power modulation
- Possibility to operate in grid-forming mode and thus enabling the transition from grid-connected to islanded operation
- Construction of multi-terminal grids because of constant voltage polarity and enhanced control functions

Nevertheless, both technologies will co-exist in the future, each with its specific application. The classic LCC-HVdc systems, due to their technological readiness, higher efficiency and lower operational costs will be applied at very higher power and voltage ratings, whereas the VSC-HVdc will be used in applications, in which the higher controllability and flexibility to provide services to the ac grid is of greater value [54].

The focus of this thesis, on one hand lies on the services HVdc systems can provide to the ac grid (which are only realizable with VSC-HVdc) and on the other hand on the protection using dc CB and MMC. That is why in the remainder of this section only the fundamentals of VSC-HVdc systems, their terminal configuration based on MMC, their control schemes, and protection are explained.

Table 2.1: Comparison between LCC- and VSC-HVdc systems [56, 1].

	LCC-HVdc	VSC-HVdc
Power electronic technology	Thyristor, turn on capability only	IGBT, turn on/turn off
Commercially established since	1954	1997
Power rating	$\leq 10,000$ MW	$\leq 4,500$ MW
Voltage rating	$\pm 1,100$ kV	± 500 kV
Filtering requirement	High, due to low-order harmonics (e.g. 11^{th} and 13^{th})	Low (kHz-range)
Footprint	Very high (dominated by harmonic filters)	Lower
Control	2-quadrant operation (always consumes reactive power)	4-quadrant operation (independent P/Q control)
AC network requirements	strong ac network (SCR>3)	Possibility to operate with weak or islanded network
AC faults	Commutation failure, Loss of power transmission for several hundred ms	Fault ride through capability and maintains active power transfer
DC faults	Can extinguish dc faults by control action	Depends on converter topology (fault blocking or feeding)
Losses	0.7%	2-Level: 1.5%, MMC: <1%
Dynamic overload capability	High	Low
MTdc operation	Difficult (power flow reversal requires voltage polarity change)	Easier (power flow reversal involves current polarity change)

2.1. VSC-HVdc applications

In the following section, the different existing VSC-HVdc applications are introduced to give a basis for the later study cases regarding HVdc protection and service provision to the ac grid. In the European network development plan [58], a threefold of HVdc systems, namely

- Asynchronous HVdc interconnector
- Embedded HVdc
- HVdc offshore wind integration

has been considered as possible solution towards a more controllable and reliable grid (see Fig. 2.3). MTdc grids, with respect to several point-to-point-connections, can dispatch the power flexibly among the terminals without limitations imposed by the ac power flow and thus are foreseen to become inevitable for the control and operation of the future power transmission system. Fig. 2.4 summarizes the schematic illustration of the different HVdc applications, while in the first case the ac areas can be either a meshed ac system or an

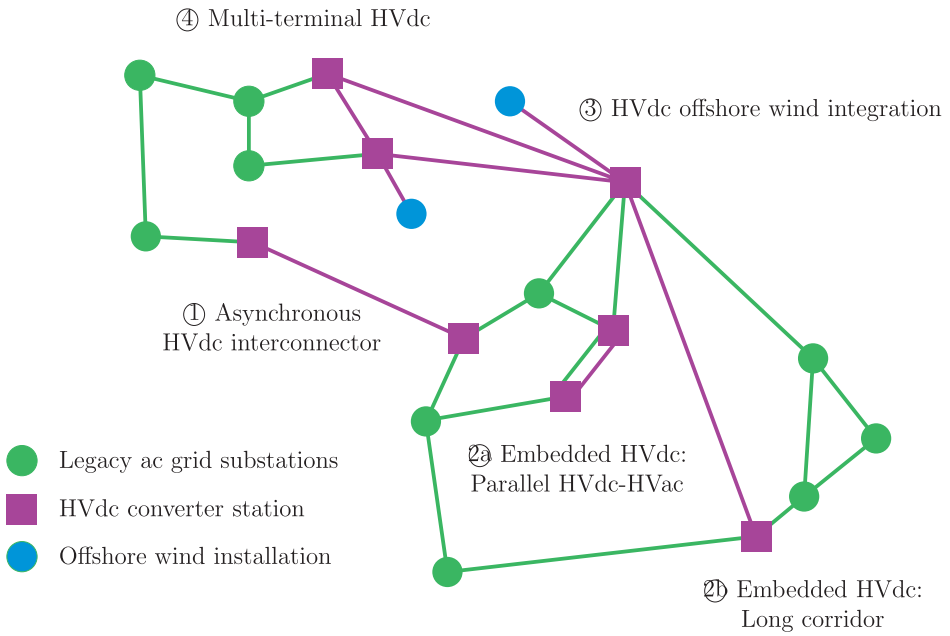


Fig. 2.3: HVdc applications in power system (modified from [5]).

isolated ac system (e.g. for offshore wind), the other cases always represent a meshed ac grid.

Asynchronous HVdc interconnector The most prominent application of HVdc to date are asynchronous HVdc interconnectors, which are used to transmit bulk power between two (strong) asynchronous ac grids. A practical example is given by the asynchronous HVdc interconnector between Germany and Denmark in Fig. 2.5(a). The flexibility, compactness and dynamic performance of VSC-HVdc makes it a favorable solution of transmission system operators worldwide to meet the growing challenges of network development [5]. Typical future applications are seen in megacities power infeed and the connection of remote islands [5].

Embedded HVdc The Joined CIGRE Working Group C4/B4/C1.604 [22] gives the following definition of an embedded HVdc system:

> An embedded HVdc system is defined as a dc link with at least two ends being physically connected within a single synchronous ac network. With such a connection, it can perform not only the basic function of bulk power transmission, but also, importantly, some additional control functions within the ac network such as power flow control, voltage control, system stability improvement and the mitigation of system cascading failure.

In [5], three applications of embedded HVdc systems are defined:

The first case, embedded HVdc forming a hybrid parallel HVdc-HVac interconnection (schematic shown in Fig. 2.4(b)) is used to increase the transmission capacity of the combined corridor and to enhance the grid controllability with limited right of way for new infrastructure.

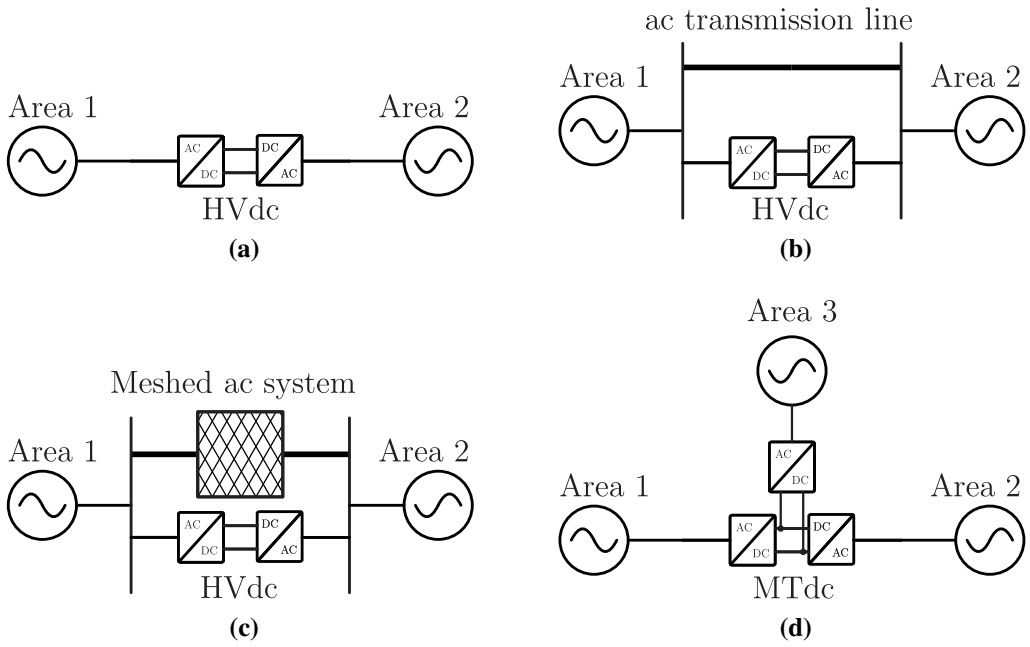


Fig. 2.4: Schematic illustration of HVdc applications: (a) Asynchronous HVdc interconnector (or HVdc offshore wind integration), (b) Embedded HVdc: Parallel, hybrid HVdc-HVac, (c) Embedded HVdc: Long HVdc corridor, (d) Multi-terminal HVdc.

An additional power transfer increase is achieved, since the HVdc can control the reactive power and ac voltage at both ends and thus allows the operation of the HVac line closer to its limits. Shorter HVdc lines in grids with higher degree of meshing and parallelism are better suited for reactive power based grid services, while active power-based support has only marginal influence due to the strong synchronous coupling between the two terminals [5].

The second case, schematically illustrated in Fig. 2.4(c), are long distance corridors to connect remote renewable energy generation or remote load centers within the same synchronous area. This scheme is best suited for bulk power transmission and active power related grid services, because it effectively reduces the power flow in any ac line, which residues between the two HVdc terminals [5]. A practical example of embedded HVdc is given by the planned HVdc corridors in Germany in Fig. 2.5(b).

The third case shows that embedded HVdc can be applied as back-to-back HVdc schemes to mesh grids and provide high power flow controllability. Thus, embedded back-to-back HVdc schemes can be seen as an alternative to phase shifting transformers or FACTS devices in an overall power flow management of an interconnected grid, particularly because of their independent active and reactive power controllability [22].

HVdc offshore wind integration In offshore wind application, a large amount of electric power aggregated from the wind turbines must be fed to the on-shore power system. The

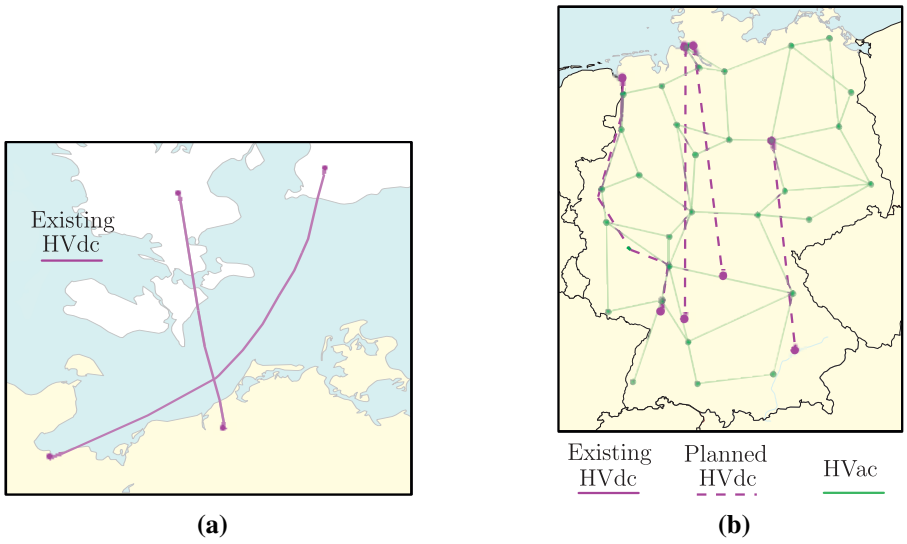


Fig. 2.5: Examples of HVdc applications: (a) Asynchronous HVdc interconnector (Germany - Denmark), (b) Embedded HVdc links in Germany.

focus of this connection are cable systems (for submarine transmission and limited right of way on-shore), for which HVac suffers from the excessive reactive power drawn by the cable capacitances. Thus, the maximum length of HVac cables is restricted (usually to about 200 km for the typical 150 kV [59]). HVdc instead is suitable for bulk power transmission over long distances. Moreover, the HVdc decouples the offshore from the onshore grid, preventing cascading failures, and offers independent control of active and reactive power, which enables a variety of control objectives in both the offshore and onshore grid and allows a flexible configuration of the offshore wind farm grid irrespective of the wind turbine type [59]. In [60], a technical and economical analysis has proven the benefits of HVdc offshore wind integration with respect to its HVac counterpart.

Multi-terminal HVdc The development and construction of MTdc grids is mainly driven by the large-scale integration of renewable energy into the existing ac power system and the potential of international energy markets in the context of so-called supergrids [61]. Supergrids based on HVdc technology can form a new additional backbone for the power system [62]. One can distinguish two main types of MTdc: MTdc systems, which comprise of more than two terminals without dc meshes and real MTdc grids, which denote a dc transmission system based on more than two converters with at least one meshed dc path and hence providing multiple power-flow paths between two grid terminals [61]. MTdc systems will likely grow organically from existing HVdc links and offshore wind integration [61, 63].

A recent realization of MTdc is the Zhangbei HVdc power transmission project in China, which utilizes MMC at a rated voltage of $\pm$500 kV to form a ring network of four interconnected converter stations. The system is designed for a total transmitted power of 4.5 GW [64].

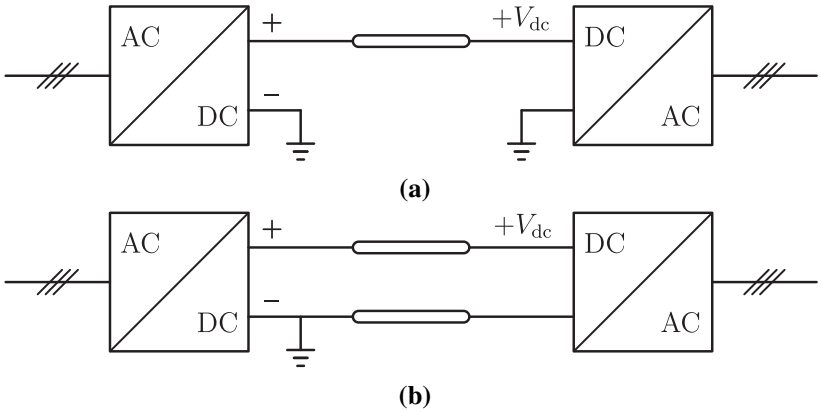


Fig. 2.6: Asymmetrical monopolar HVdc configurations: (a) with ground electrode return, (b) with metallic return conductor.

2.2. VSC-HVdc terminal configurations

To date, three main terminal configurations of VSC-HVdc systems are installed, which are asymmetrical monopole, symmetrical monopole and bipolar configurations [4].

2.2.1. Asymmetrical monopole configuration

The asymmetrical monopole configuration for a point-to-point HVdc link is shown in Fig. 2.6. This scheme consists of one high voltage conductor (cable or overhead line) and eventually one neutral conductor. In normal operation, the current flows through the high voltage conductor. The return path is formed by either the ground or sea electrodes (Fig. 2.6(a)) if substantial ground currents are allowed and the HVdc link is grounded at both terminals or the metallic ground conductor (Fig. 2.6(a)), which is usually grounded at a single end [4].

In most cases, the ground return currents are not allowed due to environmental concerns. The neutral conductor avoids the ground currents, however, involves higher losses compared to the ground return configuration. The neutral conductor must be rated for the full current, but can have - especially for submarine installations - lighter insulation, since it does not require to withstand the full dc voltage, but only the voltage drop along the conductor and the temporary over-voltage in case of failure. Thus, the costs and also the probability of dielectric failures are lower as compared to the high voltage conductor. In overhead transmission line systems, a possibility to reduce the corona-effects, is to choose the high voltage conductor with negative polarity [4].

Two major drawbacks are present in asymmetrical monopole HVdc configuration. On one hand, the dc side of the HVdc link is grounded (dc voltage is asymmetric) and therefore the ac side transformer must withstand continuous dc stress of half the rated dc voltage and special transformer designs have to be applied. On the other hand, in case of failure (e.g.

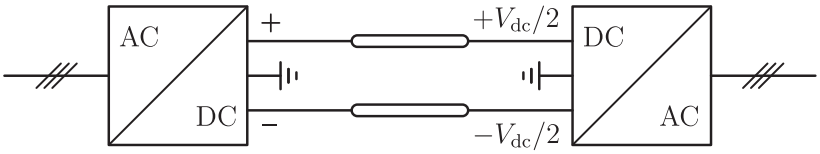


Fig. 2.7: Symmetrical monopole HVdc configuration

short circuit or component outage) or maintenance, the whole HVdc system must be shut down and the power transfer is completely disrupted [4].

2.2.2. Symmetrical monopole configuration

Fig. 2.7 shows the symmetrical monopole configuration of a point-to-point HVdc system, which is the commonly used configuration for VSC-HVdc systems nowadays. The two dc terminals of the converters are connected to the positive and negative pole. The dc voltage potential of both poles is equal, i.e. $\frac{V_{\mathrm{dc}}}{2}$, but with opposite polarity. So, in contrast to the asymmetrical monopole configuration, the dc voltage is symmetrical in this case and no steady-state dc voltage stress is applied on the ac transformers and standard transformer design can be used. Various grounding options (e.g. high impedance grounding) can be used to ground the system on the dc side at the midpoint of the shunt capacitors. The grounding configuration has large impact on the fault currents in case of pole-to-ground faults [4].

Even though the two high voltage conductors are rated at full current and isolated to the full dc voltage, in case of failure, similar to the asymmetrical monopole, the system cannot remain in operation by using the earth as return path. The critical drawback, is that in case of pole-to-ground faults, the healthy pole voltage can - in theory - raise to a maximum voltage of 2 times the pre-fault voltage. To be noted that the pole-to-pole voltage will stay constant at V_{dc} but with a displacement between the poles. To avoid the heavy over-voltage and potential insulation breakdown in the healthy pole, the whole system must be shut down in case of fault, resulting in complete loss of power transfer [4].

2.2.3. Bipolar configuration

In Fig. 2.8, the two possibilities of bipolar HVdc point-to-point configuration are depicted, with ground electrode return (Fig. 2.8(a)) or with metallic return conductor (Fig. 2.8(b)). In general, the bipolar structure is the connection of two asymmetrical monopoles sharing the same ground pole, which is the midpoint of the two converters. On the ac side, each converter is connected to a separate transformer and thus the two converters are operated in parallel from the ac grid perspective. Similar to the asymmetrical monopole configuration, the two transformers will experience steady-state dc stress and hence special transformer designs are required [4].

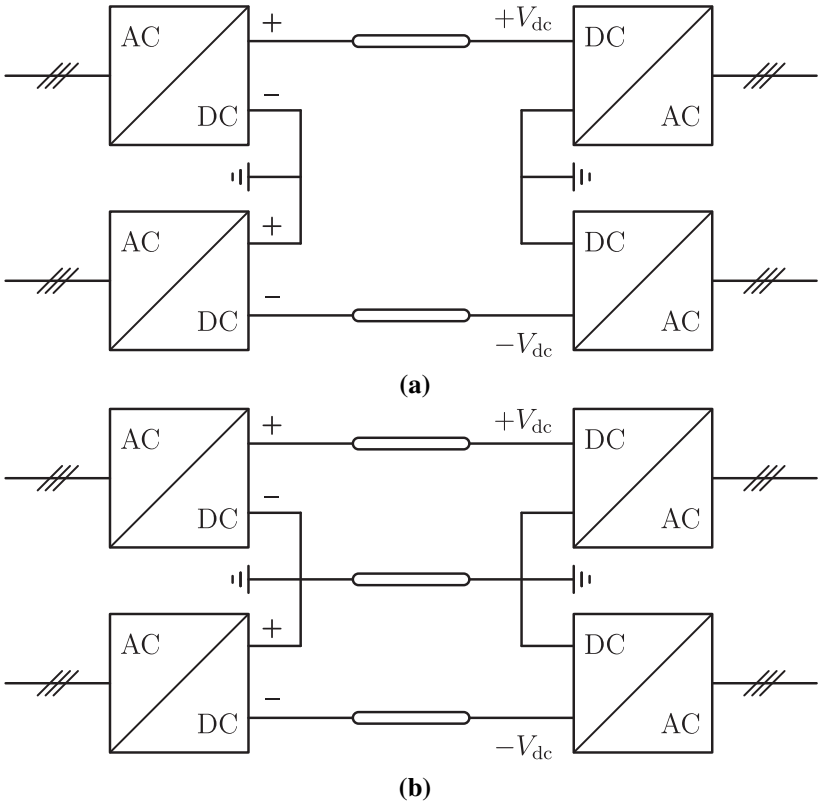


Fig. 2.8: Bipolar HVdc configurations: (a) with ground electrode return, (b) with metallic return conductor.

The bipolar HVdc configuration uses two high voltage conductors with equal dc voltage rating of V_{dc} of opposite polarity. One converter is connected to the positive pole, while the other is connected to the negative pole. In normal operation, the two poles are balanced and the current is circulating among them. The pole currents have equal amplitude, but opposite flow direction, e.g. by convention forward in the positive pole and backward in the negative pole (return path). Hence, in normal operation, no current is flowing through the neutral conductor or the ground electrodes. This configuration is also referred as rigid bipolar. As shown in (Fig. 2.8(b)), a metallic neutral conductor can be used to connect the two ground poles (of rectifier and inverter end of the HVdc link) in order to avoid substantial ground currents. This can be either necessary due to environmental reasons or also to avoid degradation of the ground electrodes, which occurs for long term use of the ground path in conduction state [4].

In bipolar systems, the two converters can be operated independently. Thus, if one converter or pole is under fault or maintenance, in order to increase the system's reliability, the system can be continuously operated with half power transmission capacity using the remaining pole and the neutral conductor (or where it is allowed the ground electrodes) as return path for the current. In this case, the system continues to operate as asymmetrical monopole with half power rating. The high expenditures for bipolar systems limit their application to HVdc systems of very high power rating, where the capacity of a single monopole is not sufficient.

Table 2.2: HVdc terminal configurations.

		Asymmetrical monopole		Symmetrical monopole	Bipolar	
		ground return	metallic return		ground return	metallic return
Costs		low	medium	medium	medium	high
Environmental impact	Earth current	high	low	low	high	low
	No. of conductors	low	medium	medium	medium	high
Transmission capacity		1 p.u.	1 p.u.	1 p.u.	2 p.u.	2 p.u.
DC voltage polarity		$-V_{dc}/0$	$-V_{dc}/0$	$+\frac{V_{dc}}{2}/-\frac{V_{dc}}{2}$	$V_{dc}/0/-V_{dc}$	$V_{dc}/0/-V_{dc}$
Redundancy		No	No	No	Yes (1 p.u.)	Yes (1 p.u.)

Bipolar HVdc configuration can also be seen as a future extension of existing monopole configurations. In that case, the two monopoles can also be operated fully independently using the metallic ground as return path in normal operation as well [4].

Table 2.2 provides a comparison among the presented terminal configurations.

2.3. HVdc terminals based on modular multilevel converter

The application of conventional two- or three-level converters in HVdc systems has several disadvantages. The low number of discrete output voltage levels leads to significant harmonic content in the ac waveform around the switching frequency and multiples of it [65]. In low-voltage systems, a high switching frequency is used to mitigate lower order harmonics in the spectrum and reduce the effect on the ac waveform quality. However, due to the relatively high blocking voltage of several kilo-volts for each individual semiconductor device (e.g IGBT), the high switching frequency in HVdc systems leads to high switching losses. Hence, to prevent negative effects of the harmonics on system, excessive filter equipment has to be installed. The second drawback is that the maximum blocking voltage of currently available semiconductor devices is limited, thus, a series connection of hundreds of semiconductors is required to realize a high-voltage converter for HVdc. The principle of operation of two-level converters is to switch the output phase voltage between the two poles of the dc side, which implies a high voltage difference in case of HVdc systems. Moreover, in order to keep the switching losses low, the commutation time must be kept small, which, in consequence, results in high $\frac{dv}{dt}$ and significant stress on the insulation [65].

Employing MMC in the terminals of VSC-HVdc transmission systems instead, has several advantages. In the MMC, the modular structure, i.e. connecting multiple SM with low rated voltage in series in stacks, eases scalability to different voltage and power ratings and offers

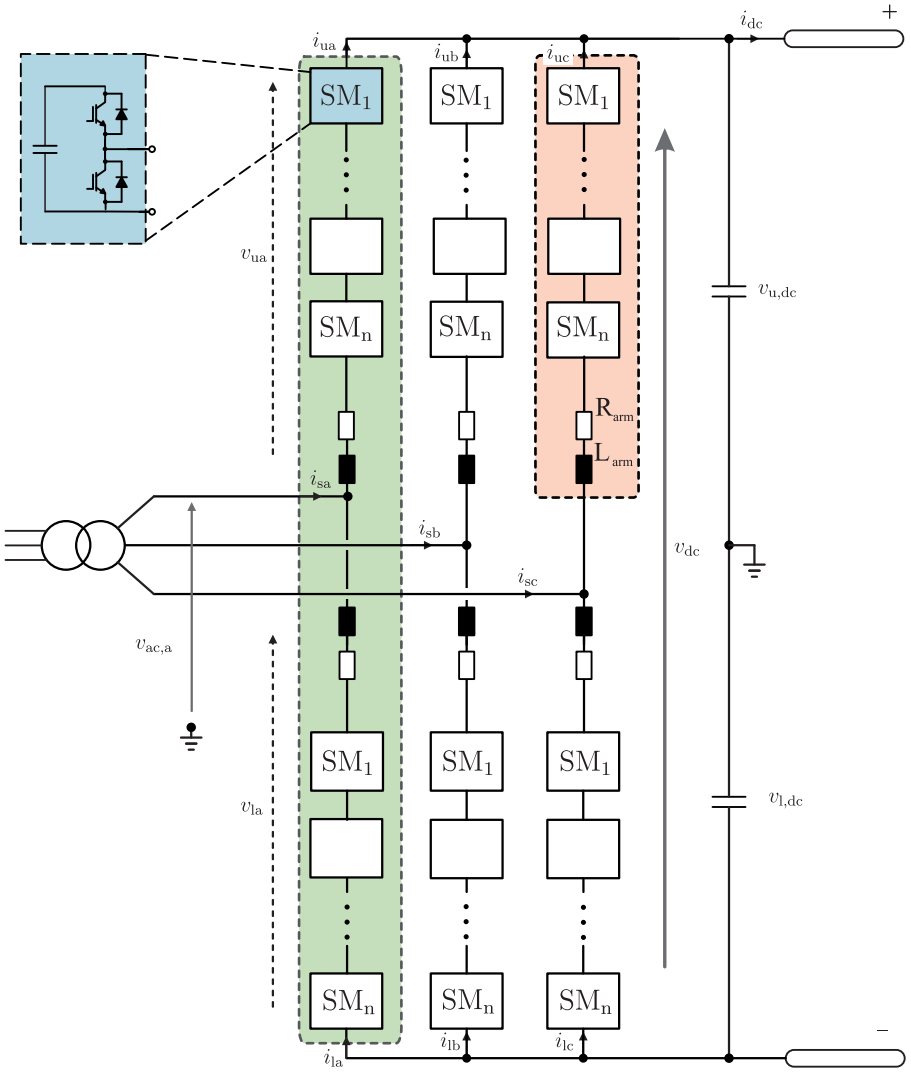


Fig. 2.9: Three-phase topology of MMC based on half-bridge submodules in symmetrical monopole HVdc configuration.

high power efficiency. In fact, due to the higher level of discrete voltage steps in the output voltage, the amplitude of harmonics is reduced. The second effect is that not every switch is involved in every transition of the output voltage. Consequently, the pulse frequency (of the modulation) by which the output voltage is changed can be increased without increasing the effective switching frequency of the semiconductor devices. Likewise, the harmonic spectrum is shifted towards higher harmonic frequencies, which results in high quality waveforms at the ac side and a significant reduction of the ac filter size [66], while keeping the switching losses of the converter low [65].

2.3.1. Fundamental operation of the MMC

Fig. 2.9 shows the three-phase MMC topology based on half-bridge SM in symmetrical monopole configuration, in which the dc midpoint is grounded. This topology is also known as modular multilevel cascade converter (MMCC) as defined by Akagi or more precisely

considering the employment of half-bridge SM (which are also known as chopper cells) and the circuit configuration as modular multilevel cascade converter based on double-star chopper cells (MMCC-DSCC) [67]. Nevertheless, Akagi states that using the general term MMC is allowable [67] and hence, will be used in the remainder of this thesis.

The circuit consists of three phase legs (green) with a midpoint connection between the two arms (red). These midpoints are the ac terminal of the converter. In each arm a number n of SM is connected in series, in which the commutation is performed internally. In each arm a small arm inductor is implemented, which avoids unreasonably large switching harmonics in the arm currents [65]. The arm resistance represents the losses in the arm inductors (and the SM) and is usually small. The capacitors connected at the dc side are a lumped model representation of the pole-to-neutral capacitance of the positive and negative dc pole cables or OHL. In steady state, the dc bus is assumed to be balanced between the two poles [65].

The principle operation of the MMC is based on the control of the SM, in such a way that the combination of voltages inserted by the SMs form the desired ac and dc side voltage of the converter. The sum of the upper and lower arm voltage is approximately maintained at the pole-to-pole dc side voltage, while the difference of upper and lower arm voltage results in the alternating voltage at the ac side [65]. To fulfill such requirements the upper and lower arm voltages in the MMC in steady state are given by

$$\begin{aligned} v_\mathrm{u} &= \frac{v_\mathrm{dc}}{2} - \hat{v}_\mathrm{s}\cos(\omega t) \\ v_\mathrm{l} &= \frac{v_\mathrm{dc}}{2} + \hat{v}_\mathrm{s}\cos(\omega t) \quad , \end{aligned} \tag{2.1}$$

where v_dc represents the dc side voltage and $v_\mathrm{s} = \hat{v}_\mathrm{s}\cos(\omega t)$ the output-side emf of the converter, since there is no explicit ac-side voltage in the MMC [65]. It has to be noted that symmetrical voltages are assumed, so that the three output phases are shifted by 0 rad, $\frac{-2\pi}{3}$ rad, and $\frac{2\pi}{3}$ rad in the phase, respectively. Thus, the converter operation can be expressed on a phase-by-phase basis and the equations are given without the explicit phase notation. The arm currents in steady state are obtained by

$$\begin{aligned} i_\mathrm{u} &= i_\mathrm{c} + \frac{\hat{i}_\mathrm{s}}{2}\cos(\omega t) \\ i_\mathrm{l} &= i_\mathrm{c} - \frac{\hat{i}_\mathrm{s}}{2}\cos(\omega t) \quad , \end{aligned} \tag{2.2}$$

where i_c represents the circulating current and $i_\mathrm{s} = \hat{i}_\mathrm{s}\cos(\omega t)$ the ac phase current. The mean value of the three phase arm currents adds up to the dc side current i_dc [65]. Assuming balanced ac bus voltages v_ac and purely dc circulating current (i.e. the second order circulating current is ideally controlled to zero) it follows

$$i_\mathrm{u} = \frac{i_\mathrm{dc}}{3} + \frac{\hat{i}_\mathrm{s}}{2}\cos(\omega t)$$

$$i_{\mathrm{l}} = \frac{i_{\mathrm{dc}}}{3} - \frac{\hat{i}_{\mathrm{s}}}{2}\cos(\omega t) \quad . \tag{2.3}$$

From the KVL at the upper and lower arm of the MMC and assuming a balanced dc bus, the following can be obtained

$$\begin{aligned} v_{\mathrm{ac}} &= \frac{v_{\mathrm{dc}}}{2} - v_{\mathrm{u}} - R_{\mathrm{arm}} i_{\mathrm{u}} - L_{\mathrm{arm}} \frac{\mathrm{d}i_{\mathrm{u}}}{\mathrm{d}t} \\ v_{\mathrm{ac}} &= -\frac{v_{\mathrm{dc}}}{2} + v_{\mathrm{l}} + R_{\mathrm{arm}} i_{\mathrm{l}} + L_{\mathrm{arm}} \frac{\mathrm{d}i_{\mathrm{l}}}{\mathrm{d}t} \quad . \end{aligned} \tag{2.4}$$

Adding and subtracting these terms leads to the dynamics of output and circulating current, respectively [65]:

$$\begin{aligned} \frac{L_{\mathrm{arm}}}{2}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} &= \underbrace{\frac{-v_{\mathrm{u}} + v_{\mathrm{l}}}{2}}_{v_{\mathrm{s}}} - v_{\mathrm{ac}} - \frac{R_{\mathrm{arm}}}{2} i_{\mathrm{s}} \\ L_{\mathrm{arm}}\frac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t} &= \frac{v_{\mathrm{dc}}}{2} - \underbrace{\frac{v_{\mathrm{u}} + v_{\mathrm{l}}}{2}}_{v_{\mathrm{c}}} - R_{\mathrm{arm}} i_{\mathrm{c}} \quad . \end{aligned} \tag{2.5}$$

Following the definitions of the output-side emf v_{s} and internal voltage v_{c} in (2.5), the maximum output voltage is obtained, when all SM in the lower arm are inserted and all SM in the upper arm are bypassed, while the minimum is obtained for the opposite, i.e.

$$\begin{aligned} v_{\mathrm{u}} = 0, \quad v_{\mathrm{l}} = v^{\Sigma}_{\mathrm{SM,l}}, \quad \Rightarrow v_{\mathrm{s}}^{\mathrm{max}} &= \frac{v^{\Sigma}_{\mathrm{SM,l}}}{2} \\ v_{\mathrm{u}} = v^{\Sigma}_{\mathrm{SM,u}}, \quad v_{\mathrm{l}} = 0, \quad \Rightarrow v_{\mathrm{s}}^{\mathrm{min}} &= -\frac{v^{\Sigma}_{\mathrm{SM,u}}}{2} \quad . \end{aligned} \tag{2.6}$$

To keep the circulating current in average at a pure dc value, the internal voltage must be chosen equal to $v_{\mathrm{c}} \approx \frac{v_{\mathrm{dc}}}{2}$ [65]. Thus, in order to maximize the ac voltage magnitude according to (2.6), the sum of capacitor voltages in the SM string in both arms in average should be equal to the dc-side voltage:

$$V^{\Sigma}_{\mathrm{SM}} = V_{\mathrm{dc}} \quad . \tag{2.7}$$

The sum capacitor voltage should usually be equally distributed among the SMs, so that

$$V_{\mathrm{SM}} = \frac{V^{\Sigma}_{\mathrm{SM}}}{n_{\mathrm{SM}}} = \frac{V_{\mathrm{dc}}}{n_{\mathrm{SM}}} \quad . \tag{2.8}$$

It should be noted that this is the ideal case. In practice, the insertion of the SM will lead to charging and discharging processes of the SM capacitors depending on the current direction, which reflect in capacitor voltage ripple around the nominal value given by (2.8) [65].

In the following, the averaged dynamic model of the MMC will be derived based on [65].

The fundamental operation of the MMC implies that at each time instant the appropriate number of SM is inserted to generate the desired voltage waveform and apply the control laws. At each time instant, the SM insertion indices can only attain two different values, whereas $n^i_{\mathrm{u,l}} = 1$ inserts the ith capacitor in the upper/lower arm and $n^i_{\mathrm{u,l}} = 0$ bypasses it [65].

Thus, the upper and lower arm voltages can be obtained with:

$$v_{\mathrm{u,l}} = \sum_{i=1}^{n_{\mathrm{SM}}} n^i_{\mathrm{u,l}} v^i_{\mathrm{SMu,l}} \ . \tag{2.9}$$

The mean value of all capacitor voltages is considered equal. To ensure that the individual differences in the capacitor voltages are balanced, a decentralized SM energy balancing controller can be implemented. Hence, the individual differences can be neglected in the dynamic model of the converter and can be replaced with their common mean value as in (2.8):

$$v_{\mathrm{u,l}} = \sum_{i=1}^{n_{\mathrm{SM}}} n^i_{\mathrm{u,l}} v^i_{\mathrm{SMu,l}} \approx \sum_{i=1}^{n_{\mathrm{SM}}} n^i_{\mathrm{u,l}} \frac{V^{\Sigma}_{\mathrm{SM}}}{n} = \frac{V^{\Sigma}_{\mathrm{SM}}}{n} \sum_{i=1}^{n_{\mathrm{SM}}} n^i_{\mathrm{u,l}} \ . \tag{2.10}$$

The individual SM insertion indices can be averaged for one arm, which results in the per-arm insertion indices:

$$n_{\mathrm{u,l}} = \frac{1}{n_{\mathrm{SM}}} \sum_{i=1}^{n_{\mathrm{SM}}} n^i_{\mathrm{u,l}} \ . \tag{2.11}$$

The per-arm insertion indices can obtain $n_{\mathrm{SM}} + 1$ discrete values. However, assuming n_{SM} is a sufficiently large number, the insertion indices can be assumed continuous in the range $[0 \ldots 1]$ [65]. Thus, the upper and lower arm voltages can be expressed with:

$$v_{\mathrm{u,l}} = n_{\mathrm{u,l}} V^{\Sigma}_{\mathrm{SMu,l}} \ . \tag{2.12}$$

Substituting (2.12) in (2.5) results in:

$$\begin{aligned} \frac{L_{\mathrm{arm}}}{2} \frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} &= \underbrace{\frac{-n_{\mathrm{u}} V^{\Sigma}_{\mathrm{SMu}} + n_{\mathrm{l}} V^{\Sigma}_{\mathrm{SMl}}}{2}}_{v_{\mathrm{s}}} - v_{\mathrm{ac}} - \frac{R_{\mathrm{arm}}}{2} i_{\mathrm{s}} \\ L_{\mathrm{arm}} \frac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t} &= \frac{v_{\mathrm{dc}}}{2} - \underbrace{\frac{n_{\mathrm{u}} V^{\Sigma}_{\mathrm{SMu}} + n_{\mathrm{l}} V^{\Sigma}_{\mathrm{SMl}}}{2}}_{v_{\mathrm{c}}} - R_{\mathrm{arm}} i_{\mathrm{c}} \ . \end{aligned} \tag{2.13}$$

Adding and respectively subtracting the underbraced expressions in (2.13), the per-arm insertion indices can be solved based on the output and internal voltage of the MMC. Replacing the output and internal voltage with their respective references (available from the phase current and circulating current controller output, respectively) finally results in the ideal per-arm

insertion indices [65]:

$$n_{\mathrm{u}} = \frac{v_{\mathrm{c}}^{*} - v_{\mathrm{s}}^{*}}{V_{\mathrm{SMu}}^{\Sigma}} \tag{2.14}$$

$$n_{\mathrm{l}} = \frac{v_{\mathrm{c}}^{*} + v_{\mathrm{s}}^{*}}{V_{\mathrm{SMl}}^{\Sigma}} \ . \tag{2.15}$$

Despite the output and circulating currents, the SM capacitors add $2n$ more state variables to the MMC dynamic model by their capacitor voltages. In high-voltage systems, the large number of SM in the MMC would result in immense computational effort to solve a set of differential equations with such a high order [65]. However, under the assumption of continuous per-arm insertion indices, it is possible to average the individual SM voltages

$$C_{\mathrm{SM}} \frac{\mathrm{d}v_{\mathrm{SMu,l}}^{i}}{\mathrm{d}t} = n_{\mathrm{u,l}}^{i} i_{\mathrm{u,l}} \ \text{,for} \ i = 1, 2, \ldots, N \tag{2.16}$$

by one sum capacitor voltage per arm [65]:

$$C_{\mathrm{SM}} \underbrace{\sum_{i=1}^{n_{\mathrm{SM}}} \frac{\mathrm{d}v_{\mathrm{SMu,l}}^{i}}{\mathrm{d}t}}_{\mathrm{d}v_{\mathrm{SMu,l}}^{\Sigma}/\mathrm{d}t} = \sum_{i=1}^{n_{\mathrm{SM}}} n_{\mathrm{u,l}}^{i} i_{\mathrm{u,l}} \ . \tag{2.17}$$

The equation (2.17) can be simplified to:

$$\frac{C_{\mathrm{SM}}}{n_{\mathrm{SM}}} \frac{\mathrm{d}v_{\mathrm{SMu,l}}^{\Sigma}}{\mathrm{d}t} = n_{\mathrm{u,l}} i_{\mathrm{u,l}} \ . \tag{2.18}$$

Substituting the arm currents in (2.18) with the output and circulating current, finally results in:

$$\frac{C_{\mathrm{SM}}}{n_{\mathrm{SM}}} \frac{\mathrm{d}v_{\mathrm{SMu}}^{\Sigma}}{\mathrm{d}t} = n_{\mathrm{u}} \left(\frac{i_{\mathrm{s}}}{2} + i_{\mathrm{c}} \right) \tag{2.19}$$

$$\frac{C_{\mathrm{SM}}}{n_{\mathrm{SM}}} \frac{\mathrm{d}v_{\mathrm{SMl}}^{\Sigma}}{\mathrm{d}t} = n_{\mathrm{l}} \left(-\frac{i_{\mathrm{s}}}{2} + i_{\mathrm{c}} \right) \ . \tag{2.20}$$

2.3.2. MMC-HVdc terminal inner control loops and controller design

Fig. 2.10 provides an overview of an MMC control system applied to the terminals of the HVdc system, where the controllers marked in green are further elaborated on in the following.

Phase (output) current controller The phase or output current controller will operate in the dq-reference frame, to enable decoupled control of active and reactive power. The first

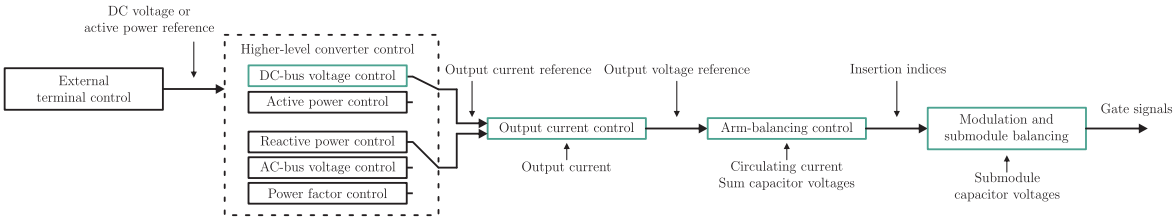


Fig. 2.10: Overview of the inner MMC-terminal control system [65].

part of the control plant of the phase current controller evolves from the dynamics of the output current controller in (2.5) and considering an additional ac side filter it follows:

$$G_{\mathrm{ac}}(s) = \frac{i_{\mathrm{s}}(s)}{v_{\mathrm{s}}(s) - v_{\mathrm{ac}}(s)} = \frac{2}{s\,(2L_{\mathrm{f}} + L_{\mathrm{arm}}) + (2R_{\mathrm{f}} + R_{\mathrm{arm}})} \ , \tag{2.21}$$

in which the transfer function from $v_{\mathrm{s}}(s)$ to $i_{\mathrm{s}}(s)$ is the reference transfer function and the grid voltage $v_{\mathrm{ac}}(s)$ is a disturbance, which can be (partially) canceled using a feed-forward (FF) term. The FF term has to be filtered by a first-order low-pass filter to avoid the propagation of high order harmonics in the control. It should be remarked that the output voltage follows its reference with a certain delay

$$v_{\mathrm{s}}(s) = e^{-sT_{\mathrm{delay}}} v_{\mathrm{s}}^{*}(s) \approx \underbrace{\frac{1}{1 + sT_{\mathrm{delay}}}}_{G_{\mathrm{delay}}(s)} v_{\mathrm{s}}^{*}(s) \ , \tag{2.22}$$

which is introduced by the computation delays in digital signal processors, field-programmable gate arrays, and in the analog-to-digital conversion process (summing up to the sample period T_{s}), and the switching delay of the pulse-width modulation (PWM) equal to $\frac{T_{\mathrm{s}}}{2}$, thus $T_{\mathrm{delay}} = \frac{3T_{\mathrm{s}}}{2}$.

Thus, the overall control plant has second-order dynamic behavior, i.e. PT_2-behavior. However, the time constant of the filter and arm inductors is much larger than the time constant introduced by the delay between output voltage and its reference (in the order of one hundred). For such a system in [68], the use of proportional-integral (PI)-controller

$$G_{\mathrm{PI,ac}}(s) = k_{\mathrm{p,ac}} + \frac{k_{\mathrm{i,ac}}}{s} \tag{2.23}$$

tuned with the technical optimum is proposed. The aim of the technical optimum is to keep the magnitude of the closed-loop frequency response at one and the phase of the closed-loop frequency response at zero for frequencies as high as possible. Likewise, a small overshoot in the step response and fast reference tracking are ensured.

As the first condition, the time constant of the controller is set equal to the larger time constant of the control plant (the one of the filter) to compensate it and guarantee high dynamics,

i.e.

$$T_{\mathrm{i,ac}} = T_{\mathrm{ac}} = \frac{L_{\mathrm{f}} + \frac{L_{\mathrm{arm}}}{2}}{R_{\mathrm{f}} + \frac{R_{\mathrm{arm}}}{2}} \ . \tag{2.24}$$

The control gain is selected, such that the magnitude of the reference transfer function is kept at one for frequencies as high as possible, from which the second condition evolves:

$$k_{\mathrm{p,ac}} = \frac{T_{\mathrm{ac}}}{2V_{\mathrm{ac}}T_{\mathrm{delay}}} \ , \tag{2.25}$$

with $V_{\mathrm{ac}} = \frac{1}{R_{\mathrm{f}}+\frac{R_{\mathrm{arm}}}{2}}$ being the gain of the control plant. The integral gain of the controller follows from (2.24) and (2.25):

$$k_{\mathrm{i,ac}} = \frac{k_{\mathrm{p,ac}}}{T_{\mathrm{i,ac}}} \ . \tag{2.26}$$

The open-loop transfer function is achieved with the product of controller and control plant transfer functions:

$$G_{\mathrm{o,ac}}(s) = G_{\mathrm{PI,ac}}(s) \cdot G_{\mathrm{ac}}(s) \cdot G_{\mathrm{delay}}(s) \ . \tag{2.27}$$

The closed loop transfer function can be obtained accordingly with

$$G_{\mathrm{c,ac}}(s) = \frac{G_{\mathrm{o,ac}}(s)}{1 + G_{\mathrm{o,ac}}(s)} \ . \tag{2.28}$$

In [65], an alternative controller design is presented to achieve higher control bandwidth at the cost of a lower stability margin. First, it is assumed that the time constant of the filter and arm inductors is much larger than the time constant introduced by the delay between output voltage and its reference, so that the control plant can be approximated as first-order transfer function. To design the PI-controller, first, only the proportional part is considered. A further simplification is made by neglecting the impact of the usually small arm and filter resistances (which is valid since the circuitry shows almost inductive behavior at high frequencies). Consequently, the closed loop transfer function results in a first-order system with bandwidth equal to $\alpha_{\mathrm{c,ac}} = \frac{k_{\mathrm{p,ac}}}{L_{\mathrm{f}}+\frac{L_{\mathrm{arm}}}{2}}$, i.e. the closed loop transfer function's magnitude equals $|G_{\mathrm{c,ac}}(j\alpha_{\mathrm{c,ac}})| = \frac{1}{\sqrt{2}}$ and it holds $G_{\mathrm{c,ac}}(0) = 1$. The closed-loop bandwidth is an important parameter of the control tuning, since it determines the exponential convergence rate of the system, i.e. how the variable (in this case the phase current) will react to a reference step. In fact, the time constant of the reference tracking is the inverse of the closed-loop bandwidth.

Even though in the first consideration the total time delay of computation and modulation was neglected, this is not generally valid, which constraints the maximum closed-loop bandwidth, which should be chosen according to $\alpha_{\mathrm{c,ac}} \leq \frac{\omega_{\mathrm{s}}}{10}$, in which ω_{s} is the angular sampling frequency.

Taking into account the beforehand neglected total time delay of computation and modula-

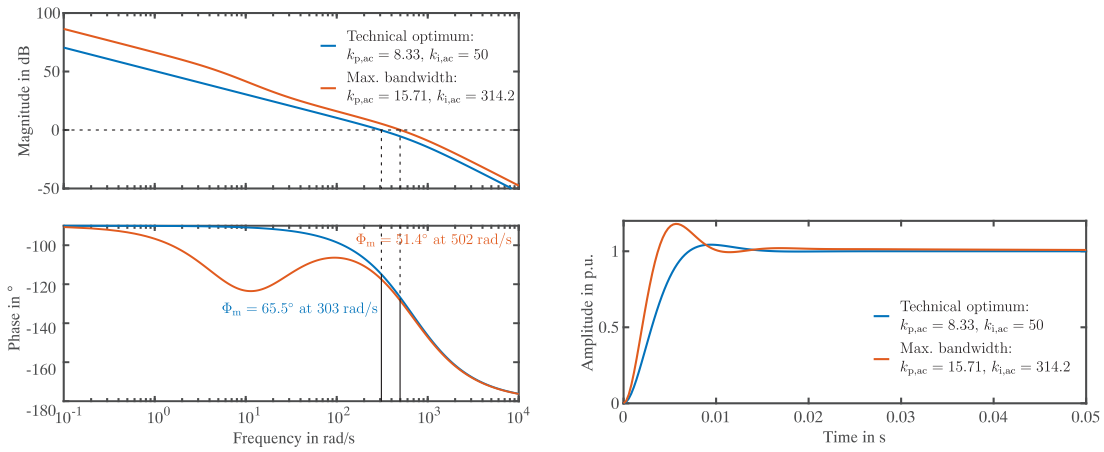


Fig. 2.11: Phase (output) current controller design: (a) Open-loop Bode-plot, (b) Closed-loop step response.

tion, the open loop transfer function (assuming pure P-control) can be expressed by

$$G_{o,ac}(s) = \frac{k_{p,ac}}{s\left(L_f + \frac{L_{arm}}{2}\right)} \cdot \frac{1}{1+sT_{delay}} = \frac{\alpha_{c,ac}}{s} \cdot \frac{1}{1+sT_{delay}} \quad . \tag{2.29}$$

The cross-over frequency is determined as the value of ω, for which the magnitude of the open loop transfer function is equal to one (i.e. $|G_{o,ac}(j\omega_c)| = 1$), which evaluating (2.29) is obviously $\alpha_{c,ac}$. Then, the phase margin can be calculated as

$$\phi_{m,ac} = \pi - \arg G_{o,ac}(j\omega_c) = \pi - \arg G_{o,ac}(j\alpha_{c,ac}) = \frac{\pi}{2} - \alpha_{c,ac}T_{delay} \quad . \tag{2.30}$$

Choosing the bandwidth at the upper limit $\alpha_{c,ac} = \frac{\omega_s}{10}$, the phase margin results in $\phi_{m,ac} = 36°$, which according to [65] is small but often still acceptable.

The bandwidth of the integral term in the controller $\alpha_{i,ac}$ determines the exponential convergence rate of the adjustments made by the integral-part to obtain accurate reference tracking with zero steady-state error. According to [65], the bandwidth of the integral term should be chosen much smaller than the bandwidth of the proportional control term, so that the closed-loop system will be dominated by the proportional control part. A typical selection shall be smaller than the fundamental frequency (e.g. in the range of tens or hundreds of rad/s). Finally, the integral gain is then obtained from

$$k_{i,ac} = 2\alpha_{i,ac}k_{p,ac} \quad . \tag{2.31}$$

The resulting open-loop Bode-plots and closed-loop step responses of controller designs with technical optimum and upper limit design are shown in Fig. 2.11(a) and Fig. 2.11(b), respectively.

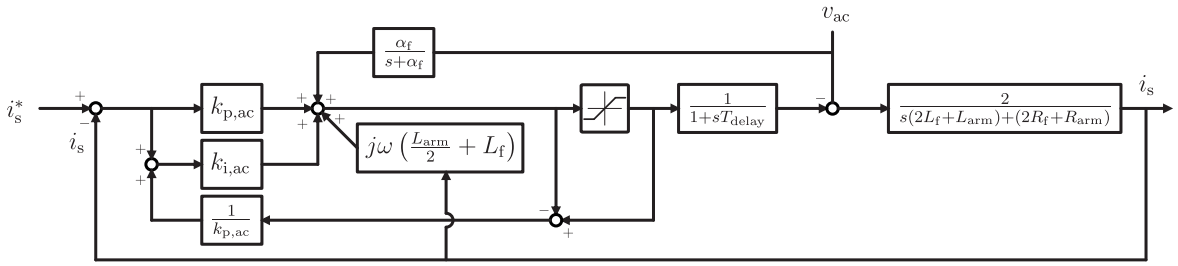


Fig. 2.12: Phase (output) current controller in dq-reference frame [65].

The overall control structure of the phase (output) current controller is depicted in Fig. 2.12, in which in addition to the controller, plant and aforementioned feed-forward with filter, a de-coupling term to diminish the cross-coupling effects between the d and q-components introduced by the current derivative in the control plant is considered. Moreover, the ac voltage reference must be limited (e.g. to $\frac{V_{\mathrm{dc}}}{2}$), which in turn requires an anti-wind-up. The shown anti-wind-up structure is of the back-calculation type, so that the difference between the saturated reference minus the ideal reference is multiplied with $\frac{1}{k_{\mathrm{p,ac}}}$ and fed-back to the input of the integral part of the controller.

Arm-balancing (internal) control The arm-balancing or internal control of the MMC comprises of the control of the sum-capacitor voltages (i.e. the arm voltages) and the circulating current controller. The aim of the sum-capacitor voltage control is to ensure that the sum-capacitor voltages in each arm converge to their desired mean value V_{dc}. The circulating current controller is implemented to control the charging and discharging process of the SM capacitors and depends on the chosen type of sum-capacitor voltage controller.

In the following, direct voltage control, which is also known as direct modulation, is applied. The goal is to find the upper and lower arm insertion indices as in (2.15). For direct voltage control the sum capacitor voltages in the upper and the lower arm are replaced with their ideal mean value V_{dc}:

$$n_{\mathrm{u}} = \frac{v_{\mathrm{c}}^{*} - v_{\mathrm{s}}^{*}}{V_{\mathrm{dc}}} \tag{2.32}$$

$$n_{\mathrm{l}} = \frac{v_{\mathrm{c}}^{*} + v_{\mathrm{s}}^{*}}{V_{\mathrm{dc}}} \ . \tag{2.33}$$

The benefit of the direct voltage control is that it results in an inherently asymptotic stable system and has low computational complexity. On the other hand, parasitic components (at twice the fundamental frequency) appear in the output and internal voltages, which have to be suppressed by the output and circulating current controllers [65].

The control plant of the circulating current controller can be obtained from the current dy-

namic equations given by (2.5). It follows:

$$G_{\mathrm{cir}}(s) = \frac{1}{s \cdot L_{\mathrm{arm}} + R_{\mathrm{arm}}} \quad . \tag{2.34}$$

Similar to the output of the phase current controller, the internal voltage also equals its reference with a delay. In addition, a parasitic component Δv_{c} is considered, which implies switching harmonics and for direct voltage control includes a component of twice the fundamental frequency (i.e. a second order harmonic):

$$v_{\mathrm{c}} = e^{-sT_{\mathrm{delay}}} v_{\mathrm{c}}^{*} + \Delta v_{\mathrm{c}} \approx \underbrace{\frac{1}{1 + sT_{\mathrm{delay}}}}_{G_{\mathrm{delay}}(s)} + \Delta v_{\mathrm{c}} \quad . \tag{2.35}$$

Thus, the circulating current controller should be designed to act on the second harmonic, which can be either achieved with a proportional-resonant (PR) controller with resonant part at the second harmonic acting on the phase quantities like in [65] or with a PI-controller in dq-reference frame, rotating at twice the fundamental frequency to cancel the second harmonic and ensure accurate reference tracking. The control law is given by

$$v_{\mathrm{c}}^{*} = \underbrace{\frac{V_{\mathrm{dc}}}{2} - R_{\mathrm{arm}} i_{\mathrm{c}}^{*}}_{\mathrm{FF}} - k_{\mathrm{p,cir}} \left(1 + \frac{1}{sT_{\mathrm{i,cir}}}\right) \left(i_{\mathrm{c}}^{*} - i_{\mathrm{c}}\right) \quad , \tag{2.36}$$

in which a FF term can be applied, which compensates for the resistive voltage drop and the dc voltage term in order to increase the control dynamics. The reference of the circulating current is set to one third of the desired dc current value. The plant structure is very similar to the phase current control plant and thus, the technical optimum is applied to tune the circulating current control parameters as well. The resulting open-loop bode-plot and closed-loop step response are shown in Fig. 2.13(a) and Fig. 2.13(b), respectively.

Fig. 2.14 and Fig. 2.15 summarize the control circuits of the circulating current controller and the direct voltage control, respectively.

DC voltage (dc energy) control The model for the dc bus (assuming that no additional dc bus capacitor is installed and the shunt capacitors of the cable or overhead line are neglected, thus, only the equivalent contribution of the SM capacitors is considered) results in:

$$\underbrace{\frac{6C_{\mathrm{SM}}}{n_{\mathrm{SM}}}}_{C_{\mathrm{eq}}} \frac{\mathrm{d}v_{\mathrm{dc}}}{\mathrm{d}t} = i_{\mathrm{dc,bus}} - \underbrace{\frac{P}{v_{\mathrm{dc}}}}_{i_{\mathrm{dc}}} \quad . \tag{2.37}$$

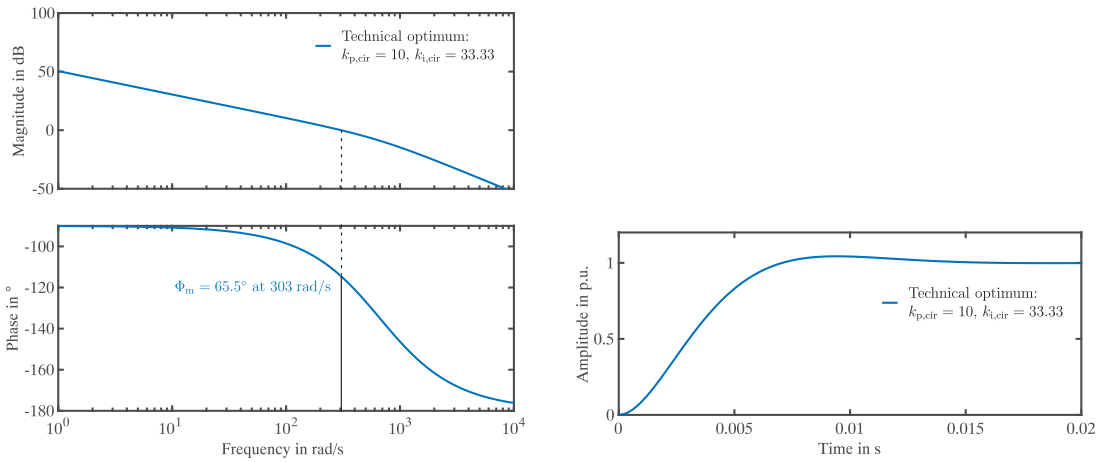


Fig. 2.13: Circulating current controller design: (a) Open-loop bode-plot, (b) Closed-loop step response.

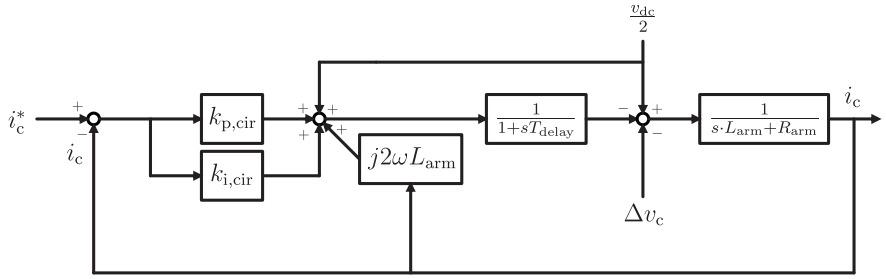


Fig. 2.14: Circulating current controller in dq-reference frame rotating at twice the fundamental frequency [65].

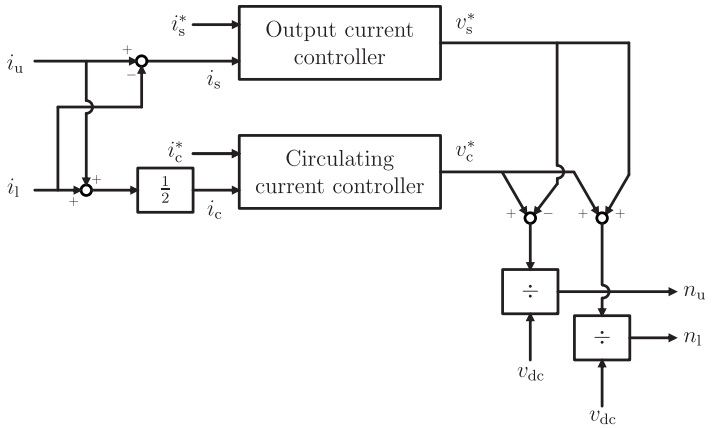


Fig. 2.15: Direct voltage control [65].

Multiplying both sides of (2.37) with v_{dc} delivers

$$C_{eq} v_{dc} \frac{dv_{dc}}{dt} = v_{dc} i_{dc,bus} - P \Rightarrow \frac{C_{eq}}{2} \frac{dv_{dc}^2}{dt} = \underbrace{v_{dc} i_{dc}}_{P_{dc,bus}} - P \ , \tag{2.38}$$

where $i_{dc,bus}$ and $P_{dc,bus}$ are the dc bus input current and power, respectively (e.g. to account for the incoming power flow of other converters in MTdc systems). Considering the

definition of the effective dc bus energy $W_{\mathrm{dc}} = \frac{C_{\mathrm{eq}} v_{\mathrm{dc}}^2}{2}$ it results in:

$$\frac{\mathrm{d}W_{\mathrm{dc}}}{\mathrm{d}t} = P_{\mathrm{dc,bus}} - P \Rightarrow W_{\mathrm{dc}}(s) = \left(P_{\mathrm{dc,bus}}(s) - P(s)\right) \cdot \frac{1}{s} \ . \tag{2.39}$$

The dc bus current and power can be regarded as disturbance variables and thus neglected in the reference transfer function. The closed-loop transfer function of the inner output current control loop tuned with the technical optimum can be approximated with

$$G_{\mathrm{c,ac}}(s) \approx \frac{1}{1 + s \cdot 2T_{\mathrm{delay}}} \ . \tag{2.40}$$

Thus, the transfer function of the control plant can be obtained with

$$G_{\mathrm{Wdc}}(s) = G_{\mathrm{c,ac}}(s) \cdot \frac{1}{s} \tag{2.41}$$

and has an IT_1 behavior. Considering a PI-controller to ensure zero static gain under the presence of a disturbance (e.g. the dc bus power), in total, it results in an open-loop transfer function with two integral parts (one of the controller and one of the electrical plant), which according to [68] requires the control parameter tuning with the symmetrical optimum to remain stable. The aim of the symmetrical optimum is to obtain the maximum phase margin at the cut-off frequency and similar to the technical optimum to keep the magnitude of the reference transfer function at one for frequencies as high as possible. The general tuning is then obtained with

$$T_{\mathrm{i,Wdc}} = a^2 \cdot 2T_{\mathrm{delay}} \tag{2.42}$$

and

$$k_{\mathrm{p,Wdc}} = \frac{1}{a} \cdot \frac{1}{2T_{delay}} \ . \tag{2.43}$$

The parameter a can be tuned to account for the trade-off between stability (high a) and dynamic performance (low a), where $a = 2$ is the standard choice. Iterative tuning in the simulation has revealed that $a = 5$ is better suited in the specific case of the dc energy control of the MMC under study to provide better damping performance, which results in control parameters $k_{\mathrm{p,Wdc}} = 66.67$ and $k_{\mathrm{i,Wdc}} = 888.9$. Fig. 2.16 depicts the open-loop bode-plot and closed-loop step response for standard symmetrical optimum and tuning with $a = 5$. The control structure is shown in Fig. 2.17.

An alternative controller design has been presented in [65]. Starting from equation (2.39) it has been assumed that the inner current control loop is significantly faster and thus that the power instantaneously follows the reference. Hence, combining the control law

$$P^* = \alpha_{\mathrm{Wdc}} \left(1 + \frac{\alpha_{\mathrm{iWdc}}}{s}\right) (W_{\mathrm{dc}} - W_{\mathrm{dc}}^*) \tag{2.44}$$

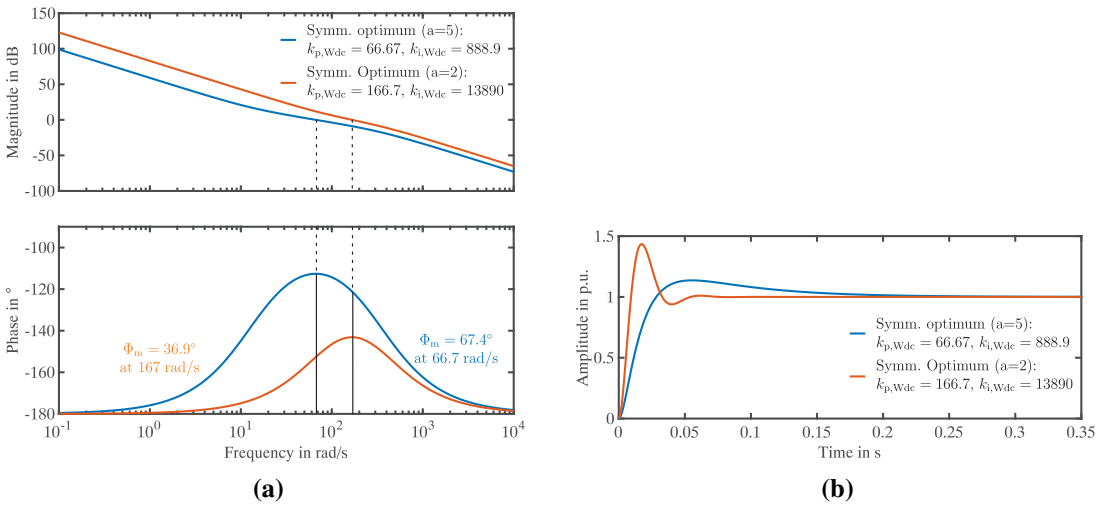


Fig. 2.16: DC bus energy controller design: (a) Open-loop bode-plot, (b) Closed-loop step response.

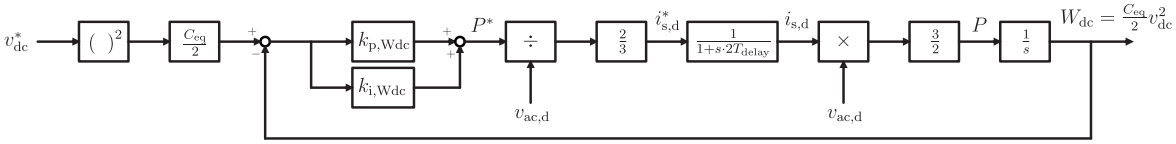


Fig. 2.17: DC voltage (dc energy) controller [65].

with (2.39) results in the closed loop transfer function

$$W_{dc} = \frac{\alpha_{Wdc}\left(s+\alpha_{iWdc}\right)}{s^2+\alpha_{Wdc}s+\alpha_{Wdc}\alpha_{iWdc}} W_{dc}^* + \frac{s}{s^2+\alpha_{Wdc}s+\alpha_{Wdc}\alpha_{iWdc}} P_{dc,bus} \quad . \tag{2.45}$$

The term related to the dc bus power has zero static gain in the closed loop transfer function, if the integral gain of the controller is larger than zero, and thus the dc voltage can still follow its reference with zero static error [65].

At first, pure P-control is assumed. Thus, the closed-loop transfer function is of high-pass character and it is sufficient to choose the P-bandwidth below the grid fundamental angular frequency, i.e. $\alpha_{Wdc} < \omega_{g1}$ [65]. Assuming as second step a PI-control, the poles in the closed-loop transfer function exist at

$$s = \frac{\alpha_{Wdc}}{2}\left(-1 \pm \sqrt{1-\frac{4\alpha_{iWdc}}{\alpha_{Wdc}}}\right) \quad . \tag{2.46}$$

To ensure sufficient damping, the imaginary part should be kept smaller than the real part, which results in the requirement for the I-part bandwidth $\alpha_{iWdc} < \frac{\alpha_{Wdc}}{2}$. A possible parametrization for a test converter similar to the converter under study in this thesis is given in [65] with $\alpha_{Wdc} = 50$ rad/s, which is close to the symmetrical optimum design with higher damping coefficient ($a = 5$).

Modulation and submodule balancing For simplicity's sake, it is assumed that the MMC in this thesis uses a phase-shifted carrier modulation. The multilevel waveform is based on n_{SM} two-level PWM waveforms, whose carriers are symmetrically phase shifted to allow for harmonic canceling within the phase arms [65]. The phase shift can be obtained from

$$\theta^i = 2\pi\frac{i-1}{n_{\mathrm{SM}}}, \quad \text{where} \quad i = 1,\ldots,n_{\mathrm{SM}} \ . \tag{2.47}$$

The phase shift of the upper arm carriers with respect to the lower arm carriers differs by an offset $\Delta\theta$, which can be chosen depending on the desired harmonic suppression in either ac or dc side. While an offset of $\Delta\theta = 0$ is suitable to obtain lowest harmonic distortion on the ac side, in the case of an odd number of SM and $\Delta\theta = \frac{\pi}{n_{\mathrm{SM}}}$ in the case of an even number of SM. To reduce the dc side harmonic content in any case, the offset should be chosen to $\Delta\theta = \pi$ [65].

Using a phase-shifted carrier modulation, the switching pattern is fully defined by the modulation scheme and no additional SM selection is required. However, there is no inherent balancing function in this modulation scheme, which makes individual (distributed) SM energy balancing necessary [65]. The goal of the balancing is to achieve equal power distribution among the SM. Distributed and centralized balancing methods exist [69]. The centralized balancing scheme is directly combined with the modulator and can be combined with nearest-level modulation, which - for practical HVdc systems - is the preferred solution due to their extremely high number of SM, which makes distributed balancing schemes complex. In the centralized scheme, the modulator provides the necessary number of inserted SM, which are in the second step selected depending on the capacitor voltage and arm current direction (sorting algorithm). As mentioned in [70], a possible drawback of centralized balancing schemes is that additional switching actions may be required. The distributed SM energy balancing is based on a closed-loop control of the individual SM voltages. Thus, a modification in the modulation signal is caused, which requires a sufficiently high switching frequency [69, 70].

The per-arm insertion indices, which are computed by the internal arm balancing and phase current control, are offset by an additional term proportional to the normalized deviation of the ith capacitor voltage $v^i_{\mathrm{SMu,l}}$ from its ideal value $\frac{V_{\mathrm{dc}}}{n_{\mathrm{SM}}}$:

$$n^{*i}_{\mathrm{u,l}} = n^i_{\mathrm{u,l}} + k_{\mathrm{bal}}\frac{\frac{V_{\mathrm{dc}}}{n_{\mathrm{SM}}} - v^i_{\mathrm{SMu,l}}}{\frac{V_{\mathrm{dc}}}{n_{\mathrm{SM}}}} \ . \tag{2.48}$$

The proportional gain k_{bal} is dimensionless and its sign must be chosen equal to the sign of the corresponding arm current in order to allow the convergence of the individual capacitor voltages. In order to avoid the introduction of disturbances in the modulation, the propor-

tional gain must be chosen small. A general rule is $k_{\text{bal}} << 1$ and the tuning can be made iteratively [65].

2.4. Fundamentals of HVdc control: External control loops and HVdc grid control

The main objective in HVdc networks is to control the node dc voltage in order to dictate the power flow through the dc lines. This does not only include the normal operating condition, in which small deviations due to different voltage drops across the lines have to be adjusted, but also disturbance conditions, in which larger imbalances in the dc voltage as a consequence of e.g. converter outages shall be compensated. Usually, the dc voltage control is based on local dc voltage measurements. However, a common system voltage feedback can also be used as modification. At first, the reference direction of HVdc power and current have to be defined. It is assumed that the power and current in inverter mode are positive, while in rectifier mode they are negative. In consequence, regular ac frequency droop curves have a negative slope and regular dc voltage droop curves have a positive slope.

In [71], a general classification of the control dependent on the control base of the outer loop controller has been made: Current-based and power-based control approach.

The current-based approach makes use of a I-V-characteristic, thus, a linear relationship between the dc voltage and current and consequently a non-linear relationship between power and dc voltage is considered. The advantage of this kind of control is that the control behavior is linear, i.e. a voltage deviation will reflect in equivalent current deviation, which is intuitive as the droop in this case has similar relation as the dc line impedance. The control in this case is the same for all voltage deviations from any reference value [4].

In contrast, the power-based approach makes use of linear P-V-characteristic and hence power-voltage relation is linear. From a power system point of view this control approach, even though the control characteristic is non-linear, is more intuitive, since it resembles the frequency regulation in ac grids. Moreover, the main advantage of the power-based approach is that it can easily be integrated with the existing vector control strategies with outer voltage or power loop and fast inner current loop.

The control is imposed by three different limits related to the converter and dc system, which are 1) dc voltage limits, 2) power limits and 3) dc current limits. The dc voltage is restricted on the upper limit by the insulation of the switching components and the equipment (such as cables) connected to the dc side. The lower limit is determined by the limitation of the converter's modulation signal, which depends on the converter topology and the converter control implementation. The maximum power is limited by the semiconductor ampacity, which limits the ac current flowing through the converter and hence the power, if constant ac

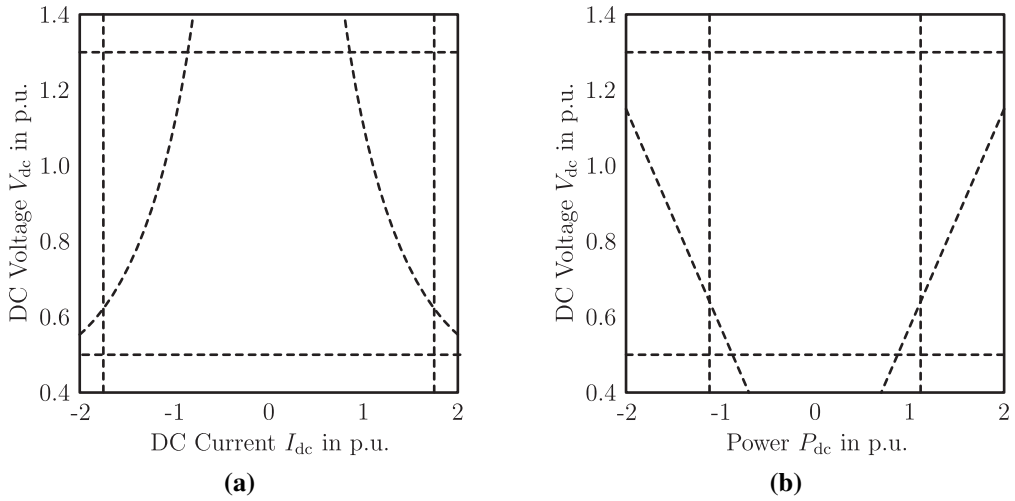


Fig. 2.18: Converter and system limits (Power limit: dashed, dc voltage limits: dashed-dotted, dc current limits: dotted): (a) I-V curve, (b) P-V curve.

voltage is assumed. The third limitation is imposed by the maximum dc current limit, which is based on the current ratings of dc connected equipment.

Fig. 2.18 demonstrates the three limitations in the I-V and P-V curves, where the limits shown are valid for both control approaches: current- and power-based. The limits values have been selected for illustrative purposes and do not necessarily represent realistic HVdc converter limits.

2.4.1. HVdc converter external control strategies

In the following, first, the main external converter control strategies [72, 4] are described, from which afterward the grid control strategies of MTdc systems are derived. The external converter control strategy defines the control set-points, either dc voltage or active power, of the before described inner converter control loops.

Voltage droop control In the voltage droop control a linear relationship between the dc voltage and the control base (current or power) is used (see Fig. 2.19), which can be mathematically expressed by

$$\Delta P_{\mathrm{dc}} = \frac{1}{k_{\mathrm{vdc}}} \Delta v_{\mathrm{dc}} \tag{2.49}$$

$$\Delta i_{\mathrm{dc}} = \frac{1}{k_{\mathrm{vdc,i}}} \Delta v_{\mathrm{dc}} \ . \tag{2.50}$$

The droop constants k_{vdc} and $k_{\mathrm{vdc,i}}$ define the slope of the I-V or P-V characteristic, respectively [4]. Droop coefficients can be adapted considering limited converter ampacities and the operating condition [30]. The droop constant is the inverse of the actually implemented

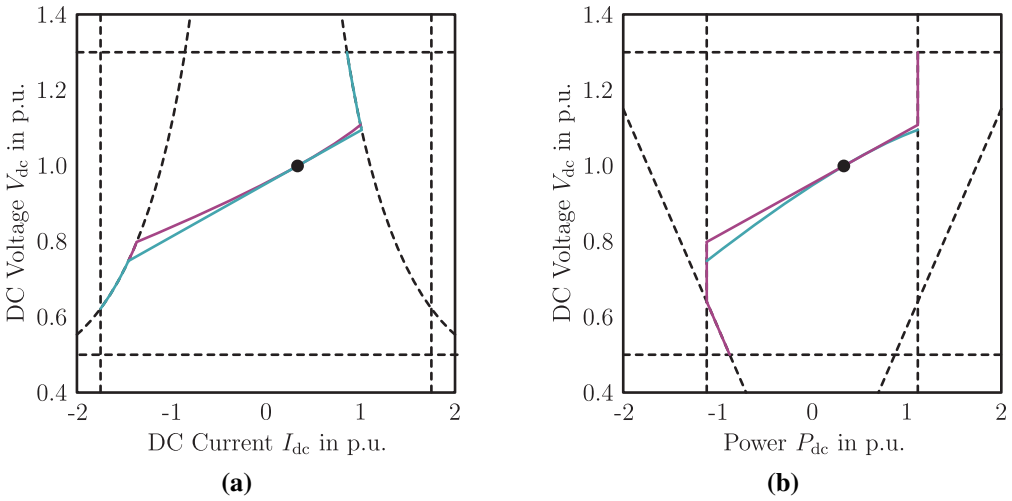


Fig. 2.19: Droop control (I-droop: green, P-droop: purple): (a) I-V curve, (b) P-V curve.

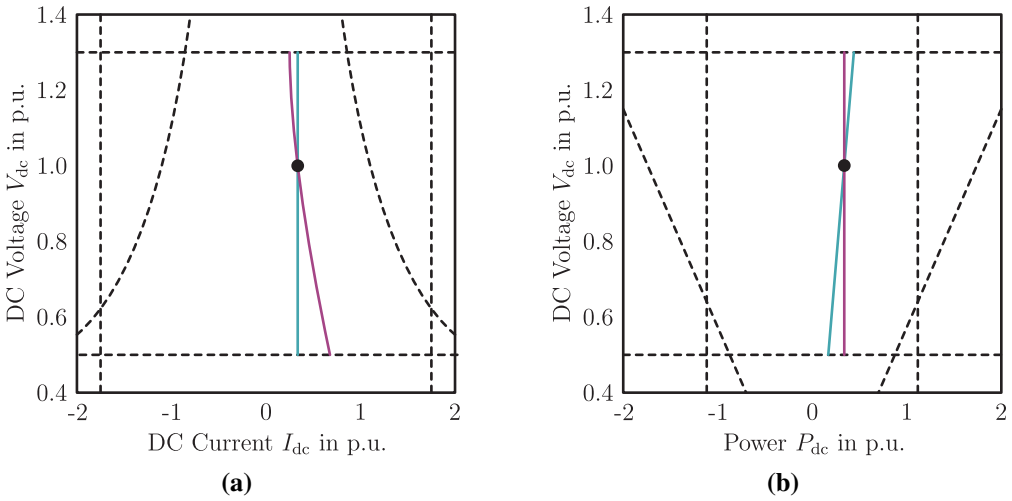


Fig. 2.20: Constant current (green) and constant power (purple) control: (a) I-V curve, (b) P-V curve.

proportional controller d_{vdc} or $d_{\text{vdc,i}}$, respectively. It has to be noted that in this section, the notation based on the droop constant is used, in order to stay consistent with the usual definitions of the general control strategies, while in the following sections the notation based on the proportional gain is applied to refer to the practical implementation.

Constant current/power control The constant current/power control depicted in Fig. 2.20 can be regarded as a special case of the droop control, with infinite droop constant (or zero proportional gain). This is represented with vertical line in the I-V or P-V curve, which indicates that the current or power do not change, whenever the dc voltage changes. The usual implementation is done with PI controller tracking the respective control reference (current or power) [4].

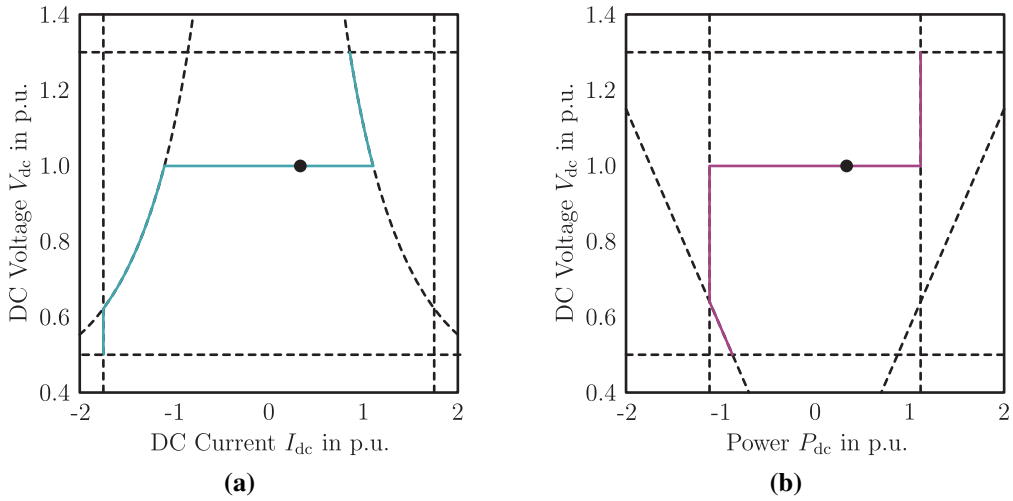


Fig. 2.21: Constant voltage control: (a) I-V curve, (b) P-V curve.

Constant voltage control The constant voltage control represents the case of the droop control with zero droop constant (see Fig. 2.21). It is obvious that an implementation with infinite proportional gain would result in instability and hence is unrealistic. Usually this converter control is based on PI controller to keep the dc voltage constant at its reference value. This is also known as dc slack bus control. In the I-V and P-V curves, this control is represented by a horizontal line, which indicates the same control behavior irrespective of the control base, current or power [4].

Voltage margin control The voltage margin control as presented in [56] is a combination of constant current/power control and constant voltage control as shown in Fig. 2.22. In the normal operating state, i.e. if the voltage is within the normal operating margin, the converter is controlled in constant current or power mode. If the voltage reaches the limits of the voltage margin, the control is switched to constant voltage control mode, clamping the voltage at the limit of the voltage margin to prevent further voltage deviation.

Deadband droop The deadband droop control is based on a similar operating principle as the voltage margin control, such that in normal operation condition the converter controls the current or power to a constant reference and switches its control mode, if the voltage exceeds the predefined margin [4]. However, in contrast to the voltage margin control, outside the normal operating voltage margin, a droop control is applied (see Fig. 2.23). Thus, the voltage margin control can be seen as special case of the deadband droop with zero droop constant.

Undeadband droop The most general form is the undeadband droop control, which applies two different droop control constants in normal and disturbed operating condition [4]. This gives rise to the possibility to independently optimize the droop constant for normal

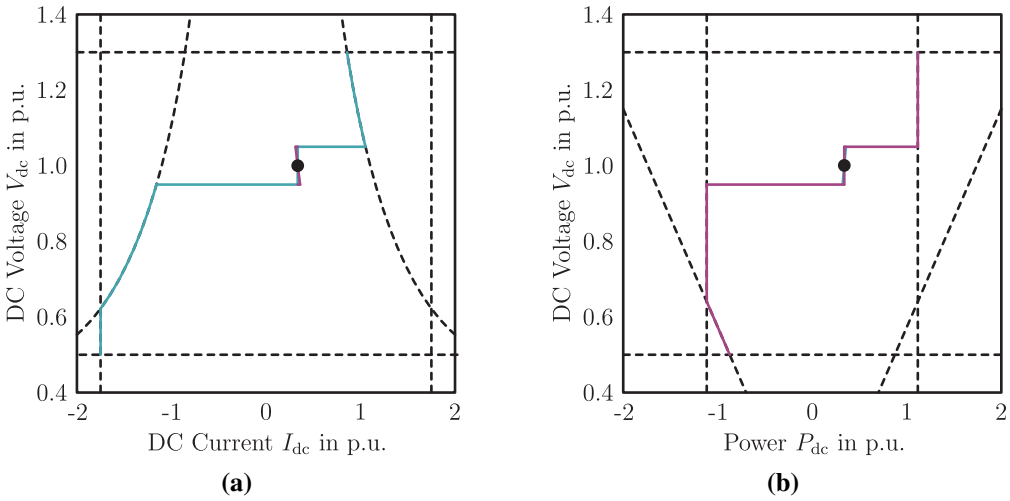


Fig. 2.22: Voltage margin control: (a) I-V curve, (b) P-V curve.

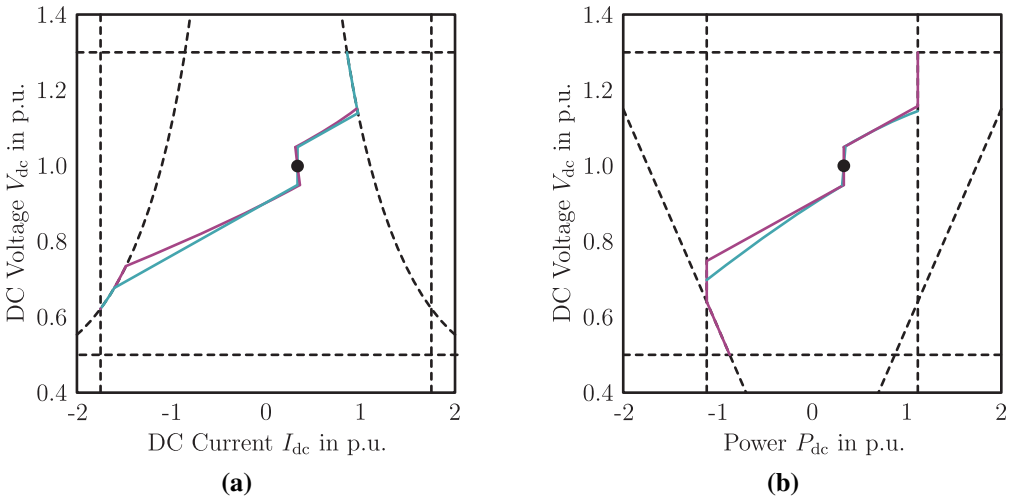


Fig. 2.23: Deadband-Droop control (I-droop: green, P-droop: purple): (a) I-V curve, (b) P-V curve.

and disturbed operation. Indeed, it is desirable to increase the voltage control contribution of remaining converters, if another converter fails, such that higher droop constants are chosen outside the voltage margin as shown in Fig. 2.24. The undeadband droop control improves the control dynamic performance [73]. From this consideration, the deadband droop control is the special case with infinite droop under normal condition and the voltage margin control is an undeadband droop with infinite droop under normal and zero droop in disturbed operation.

2.4.2. HVdc grid control strategies

Based on the converter control strategy definitions in Subsection 2.4.1, the following dc grid control strategies can be established for MTdc grids.

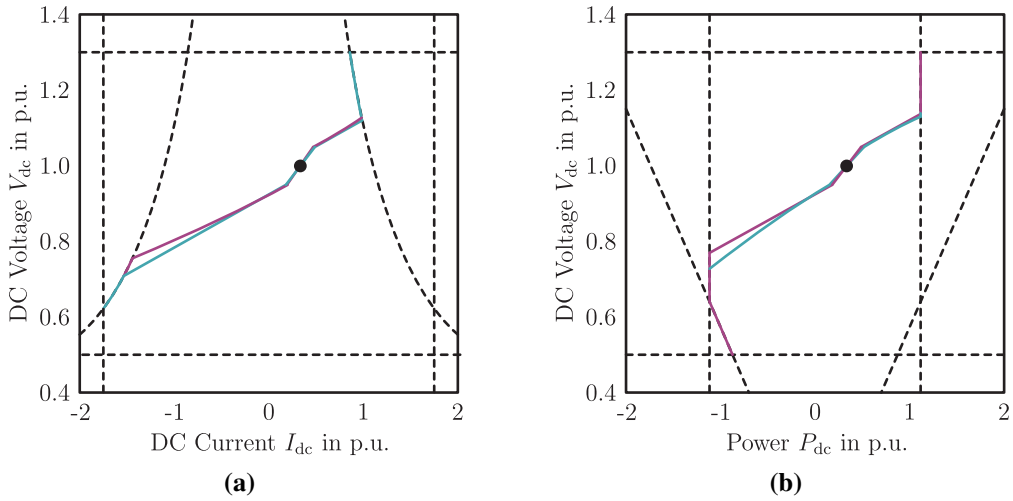


Fig. 2.24: Undeadband-Droop control (I-droop: green, P-droop: purple): (a) I-V curve, (b) P-V curve.

Centralized voltage control The centralized voltage control is also known as master-slave control or dc slack control, referring to the definition of the main converter control modes applied in this case. One converter - the master or dc slack bus - operates in constant voltage control mode. Usually, the converter connected to the strongest grid is chosen as master converter having to compensate the active power mismatch of the whole grid. The other converters - the slave or power control bus - control the current or power exchange with the ac grid constant to its nominal value, which is similar to the control strategy applied in HVdc point-to-point connections. The main drawback of the centralized voltage control is the fact that only one converter has to account for all changes in the power flow. Thus, this control strategy is generally only applicable to small multi-terminal networks, also because the slack converter has to compensate all losses in the network, which increase for large networks. No back-up control is foreseen in this control approach, if the master converter fails [4].

Distributed voltage control In the distributed voltage control, the droop control is applied to several converters in the network [4]. It is not necessary that all converters participate in the voltage control, indeed droop-controlled converters can be combined with constant current or power-controlling converters (e.g. if the respective converter terminal is connected to offshore wind-farms and tries to supply the maximum available power to the grid). A combination with dc voltage controlling converters is usually not feasible. This is due to the fact that the power is shared among the different droop-controlled converters based on their droop constant relative to the others. A small droop constant leads to a large power share. The constant dc voltage control, in fact, represents a droop constant of zero, which counteracts the principle of the distributed voltage control, since the main power flow is directed towards the voltage controlling converter and the power distribution effect of the droop control will be limited. Only the voltage drops across the lines (i.e. the losses) determine the

operating points of the droop-controlled converters in this case, which results in small control contribution [4].

Centralized voltage control with centralized back-up This grid control approach needs a replacement of the constant power control in at least one converter by voltage margin control. If the voltage deviates significantly, i.e. if the master converter fails, it will hit the voltage margin, which switches the control of the respective converter from constant power control to constant dc voltage control at the limit of the voltage margin. The task to control the dc voltage can be handed back and forth between different converters. In large networks, the risk for contingencies also in normal operation is comparably high, which results in frequent changes of the control modes and highly non-linear system behavior. In consequence, the local dc voltage measurements does not longer give valid insights on the general system state [4]. Moreover, the approach is limited by the dc voltage operating range, which is usually approximately $\pm 10\%$ around the nominal voltage value and thus in the number of converters in the system. This is necessary on one side to avoid adverse control interactions between two terminals introduced by too small voltage margins [56], and on the other side, to avoid that the total voltage deviation in the end might become too large if high voltage margins are chosen [4].

Centralized voltage control with distributed back-up Being the deadband droop control implemented in several formerly constant current / power controlling converters instead of the voltage margin control, the back-up control can be distributed among several converters. If the master converter fails, the voltage control is not given to a single converter as in the case before, but to all deadband droop-controlled converters. Nevertheless, the centralized voltage control with distributed back-up is also not applicable for large systems, where the individual converter rating is much smaller than the system rating. In this case, the operation outside the deadband is likely to appear very frequently, if the master converter hits its limits [4].

Distributed voltage control with distributed back-up In order to distribute the voltage control in both normal and disturbed conditions, the undeadband droop control can be applied. Even though, a distributed voltage control does not necessarily require an additional back-up control scheme, the different droop constants can be beneficial, since it allows the converter to maintain an operation close to its reference in normal condition (small droop) and increase the voltage control contribution during large disturbances by applying higher droop outside the normal operating margin [4].

Table 2.3 summarizes the presented grid and converter control strategies.

Table 2.3: HVdc grid control strategies.

Grid control		Centralized		Distributed	
Back-up	None	Centralized	Distributed	None	Distributed
Converter control	Master-slave	Voltage margin control	Deadband droop	Droop	Undeadband droop
Applicable grid size	Point-to-point / Small	Small	Small / Medium	Large	Large
Disturbance security	None	Low	Low / Medium	Medium	High

2.5. Fundamentals of modeling power electronics in grid integration studies

Studying power electronics (PE) in grid integration studies is a non-trivial task due to the complexity of the devices, especially in HVdc systems, where the number of switches in equipment is large, and due to non-linear behavior such as saturation, limits and tripping, and the different control layers involved. On one hand, the need for large network studies affects the computational time, which is especially relevant in the commissioning and design stage of new equipment, when intensive analysis is required. On the other hand, PE-related phenomena, such as reduced inertia and reduced transient stability margin due to the constant power behavior and resonances between cables and PE as well as the participation of PE-based generation and controllable loads in service provision, must be represented well in grid integration studies. Thus, the way of modeling a power converter is important to account for the trade-off between the risk of under/overestimation of the system response to certain phenomena and computational effort of too detailed simulation models, which would limit the application especially in real time simulations and thus delay projects already in the design and planning stage.

This thesis incorporates studies of different time scales of the involved phenomena, ranging from less than *ms*-range for dc fault phenomena to several seconds for the frequency regulation and virtual inertia emulation. For this reason, in the following, a guideline to accurately model power electronics in grid integration studies is presented based on [74], which differentiates the power electronics models in terms of complexity and typology, in order to tackle correctly the addressed problems.

In the following, three main aspects are used to define the complexity of power electronics-based resources in the grid, which are

- Power converters (topologies, thermal characteristic)
- Hardware (dc link, ac filters)
- Control (inner and outer loops, phase-locked loop (PLL))

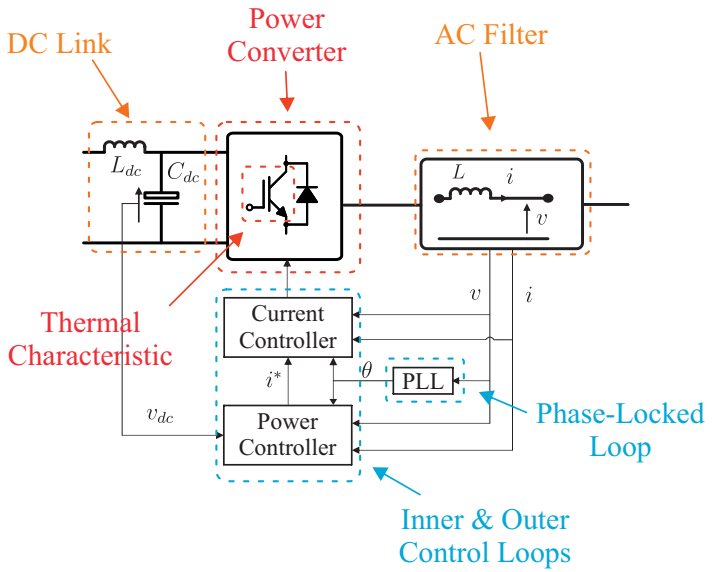


Fig. 2.25: Complexity of a power electronics-based resource: power converter (red), hardware (orange), control (blue).

As Fig. 2.25 shows, the modeling of the power converter can involve the representation of the semiconductor switches with their detailed model, optionally expanded by their thermal behavior, or the simplified equivalent model by means of controlled voltage and current sources. The hardware part is related to the passive components, such as inductors, resistors and capacitors in the dc link and ac filter, which can be represented in detail, considering e.g. their damping and temperature effects, or simply by equivalent ideal inductance, resistance and capacitance. Models with higher degree of deepness respect the controllers design (e.g. proportional, integral, derivative, resonant, etc) and the transient tracking of the error between the reference and measured variable, while simplifying approximations (e.g. first-order transfer functions) can be used in large timescales to include only the controller dynamic.

The proposed scale describes for each stage, which component has to be represented and with which necessary degree of deepness it has to be represented with consideration of the power systems model to be adopted. The scale ranges from A+ being the most accurate model, in which the switching and thermal behavior of the converter is respected to F being the least complicated model with steady-state constant voltage constant impedance modeling (see Fig. 2.26).

To describe the scale the following parts have to be evaluated:

Power converter representation: The most accurate representation of the power converter is its switching model, in which different semiconductor technologies (e.g. IGBT, Thyristors or MOSFETs) can be considered. In the average value model, the converter is condensed to controllable voltage (ac) and current sources (dc) with equivalent filter, which can emulate the converter's harmonic behavior up to the half of the switching frequency. The simplest

Deepness	Converter							Power System
	Power converter representation	Thermal Model	Inner control loop	Outer control loop	PLL	Filter	DC link capacitor	
A+	Switching Model	Included	Detailed model	Detailed model	Detailed model	Included	Included	Physics component modelling
A	Switching Model	Not included	Detailed model	Detailed model	Detailed model	Included	Included	Physics component modelling
B	Average model	Not included	Detailed model	Detailed model	Simplified Model	Simplified Model	Included	Multi-machine
C	Average model	Not included	Simplified Model	Detailed model	Simplified Model	Not included	Included	Multi-machine
D	Average model	Not included	Simplified Model	Detailed model	Simplified Model	Not included	Not included	Multi-machine
E	Phasorial Model	Not included	Simplified Model	Detailed model	Not included	Not included	Not included	Multi-machine
F	Phasorial Model	Not included	Not included	Simplified Model	Not included	Not included	Not included	Infinite bus

Fig. 2.26: Modeling deepness scale for power electronics grid-integration studies.

representation is the phasorial model of the converter, in which only a current source with slowest control dynamics is included.

The *thermal model* characterizes the thermal behavior of semiconductors and passive components in the converter. Only if the highest level of detail in the converter is needed, for example in reliability analysis, it has to be considered.

The converter control is defined by the *inner and outer control loop*. While the fast inner loop is usually implemented as current controller, for the outer loop, which provides the current reference for the inner loop, various control schemes can be implemented depending on the targeted application and service. Examples of the outer loop are among others: Active or reactive power control, dc voltage controller, ac rms voltage controller and the droop controller in HVdc systems. The control loops can be represented in full detail, including the actual control scheme with proportional, integral (or resonant) and derivative (e.g. for the current controller in HVdc systems [57]) terms or with simplified models, which take into account only the control loops' dynamic, representing it for example as first order transfer function. This model type is particularly relevant for linear analysis of the converter plant and stable and robust outer loop controller design (e.g. then applied for the optimally tuned inner current controller). If necessary, more complex control structures can involve also multiple resonant controller at harmonic frequencies of interest to study the harmonic rejection capability or multi-frequency power transfer [75].

A detailed representation of the *PLL* is requested, only if the impact of non-synchronous phenomena such as unbalances or harmonics is considered. To include the contribution of the PLL in the converter dynamics, a simplified model can be used, approximating the PLL with a second order equivalent transfer function. This approach includes the PLL bandwidth in the converter control and stability study, without increasing the complexity of the simulation.

Problem	Sub-Problem	Voltage range			Frequency range	
		HV	MV	LV	From	to
Electromagnetic Transients (EMT)	High frequency harmonics/resonances	A+	A+	A+	DC	kHz
Small-signal stability	Harmonic stability	A	A	A	55 Hz	kHz
	Sub-synchronous resonances	B	B	NA	5 Hz	55 Hz
	Inter-area oscillations	C	NA	NA	0,1 Hz	5 Hz
	DC Voltage stability	C	C	C	DC	Hundreds Hz
Transient stability	Angle and voltage stability	E	D	C	0,2 Hz	1,2 Hz
Frequency stability	Primary frequency control	E	D	C	DC	1,2 Hz
Scheduling & Optimization	Load flow	F	F	F	DC	DC

Fig. 2.27: Grid-integration studies and sub-problem modeling deepness classification depending on the voltage level.

Passive elements like *filters and dc capacitors* only have to be modeled, if their bandwidth falls into that of the phenomenon under study. In general, it can be concluded that the ac filter should be included, if the current controller is represented in detail and high frequency interactions are considered (above 1 kHz). For dynamics higher than a few Hz (e.g. 2^{nd} harmonic power variation in three-phase unbalanced or single phase systems) the dc link capacitor detailed model is required.

In the last column, the modeling of *power system* is considered, which has to be adapted depending on the deepness of the PE model itself. A detailed model of the power system (frequency-dependent and high order modeling of devices) is only needed, if a detailed representation of the PE with full switching model is foreseen. For phenomena involving low frequency (< 50 Hz) interactions, the system can be represented with less details as multi-machine model. Static models, which contain just the system constraints and limits, can be only applied in grid planning studies.

The scale benefits from its modularity, which allows the model allocations to be changed in the future. New scientific trends and results can be incorporated by scaling up or down the respective entry. The idea behind the presented guideline is to link a specific modeling deepness to the power system problem or phenomenon under study. As depicted in Fig. 2.27, the process starts with the definition of the general problem and then targets the sub-problem under investigation with respect to its frequency range.

The most detailed model is required by *electromagnetic transient (EMT) simulations*, which use time-steps in the order of hundreds of nanoseconds up to tens of microseconds. The aim of EMT-simulations is to investigate phenomena from dc up to tens of kHz with very

fine resolution, such as semiconductor switching harmonics, modulation strategies or fault blocking of multi-level converters (e.g. in HVdc terminals) and lightning impact on the power system. If reliability studies are carried out, the thermal model of the components can optionally be included.

Small-signal analysis investigates the system's response to small perturbations in order to analyze unstable or under-damped modes as a result of control interactions or resonances [76]. Specific sub-problems of the small-signal analysis are given by harmonic stability, which is mostly related to control interactions of the inner current controllers and PLL with the passive components in the grid [76, 77], sub-synchronous resonances [78, 79], and inter-area oscillations. Harmonic stability studies require the highest level of details, i.e. detailed models of the fast acting inner current controller, PLL and outer power or voltage control loops are necessary [80]. Additionally, to investigate the whole harmonic frequency range, even the converter switching properties have to be included [81]. In sub-synchronous resonance studies, the phenomena frequency range ($5 - 55$ kHz) may interfere with the bandwidth of the inner current or voltage controller, which have to be considered in the model accordingly. Inter-area oscillations studies, instead, due to the slower transients to be analyzed ($0.1 - 5$ Hz), need to incorporate only the outer control loops. PLL synchronization and dc-link capacitor must be taken into account due to their dynamics with similar bandwidth to the inter-area oscillations [82]. A special case is the MMC-HVdc system, which also requires more details in the converter model itself due to the more complex structure and control involving different inductor and capacitor interactions with different sub-synchronous dynamic responses. Another reason for detailed modeling is that simplifications in the circulating current suppression and voltage balancing control can change the sub-synchronous characteristic of the MMC model [83, 84].

DC voltage stability also relates to small-signal stability, in the sense of interactions between the interface ac/dc-converters and their controllers themselves and the converters and passive components in the grid [85]. Suitable examples in high voltage grids, are point-to-point [85] or multi-terminal VSC-HVdc systems [86], in which the injection of a large amount of power by the dc voltage controlling converter leads to negative values of the converter's power dependent equivalent admittance. If this coincides with the dc cable grid resonance, poorly damped oscillation modes result. This poses a risk of instability. DC instabilities are located mostly in the harmonic frequency range, but well below the switching frequency. Thus, small-signal methods, such as frequency domain impedance analysis [87] or time-domain modal analysis of the linearized system model [86] can be applied. In these models, average value models of the converter can be used, neglecting the PWM switching transients or representing them by first order delay transfer function [85, 88]. In the article [74], it is shown that in dc stability studies (here related to control instability phenomena induced by the dc voltage controller) the full-switching model gives only marginal accuracy improvements in the transients, while oversimplification (e.g. fixed dc voltage source instead of controlled

current source and equivalent dc capacitor for a two-level converter) ignores the effect at all. Thus, accurate representation of the outer loop (dc voltage or droop) controllers is of special importance, while the optimally tuned inner current controller can be approximated with first order transfer function. The inclusion of the PLL is important, because otherwise low-frequency modes may be overlooked [86].

Transient stability studies (for example LVRT studies and short circuits) refer to the power system's capability to remain stable after certain disturbances, such as faults or imbalances. In these studies usually large networks with high number of buses and machines are considered, which requests reduced modeling complexity in each component to avoid large computational effort compared with EMT simulations. Moreover, EMT simulations suffer from the difficulty to initialize the model for a given load flow scenario [89]. An example for HVdc system transient stability modeling is given in the CIGRE B4.57 technical brochure [90]. The models can be divided into phasor domain and average value models [91]. Power system stability studies using phasor domain models, by default, assume fundamental frequency and are based on the assumption that the small time constant of inner current control loops is irrelevant and thus only the outer loop is considered, while the inner loop is replaced with the current reference. Hence, to study transient stability with fast phenomena in the order of tens or hundreds of milliseconds, generic average value models have to be used, in which despite the outer loop, the inner current loop is represented at least with its first-order approximation. In contrast to HV system simulations, in which the inclusion of outer control loops (e.g. power loop) is sufficient to achieve satisfactory accuracy, in medium-voltage (MV) or low-voltage (LV) systems, the synchronization loop should be additionally included to account for the possible source of instability caused by slow (or too fast) PLL bandwidth [92]. This increased modeling accuracy, however, may have an impact on the computational time of large simulations, in which a large number of ac/dc converters are considered.

In *frequency stability* analysis, the capability of the power system to react on frequency disturbances and control the system frequency is studied. Frequency control (here: primary frequency regulation) involves dynamics in the order of seconds. Studies related to frequency control often take only into consideration the mechanical equations of the generation units and the power control loop of the power sources [93]. Thus, detailed model of the PE converter outer loop control (active power flow) is necessary to verify its impact on system frequency, while the inner control loops and the hardware modeling do not necessary ask for additional complexity due to their fast dynamics (tens or hundreds of milliseconds). Considering this, HVdc systems, which interconnect two different ac areas, can be approximated only with the frequency-power-droop curve, while the dynamics of turbines and governors are regarded for the generators as representation of the power system. This simplification allows the analysis of the HVdc-based primary frequency regulation in very short time (few seconds) without losing accuracy compared to rms phasor models or EMTDC simulations. In contrast in low-voltage grids, particularly in microgrids, the frequency control involves

much faster dynamics, which requires a detailed representation of PLL and dc link capacitor [94].

Scheduling and optimization involve a steady-state view on the system, i.e. the load flow, which is used in system planning or to initialize other, more complex simulations like EMT or transient stability simulations. Thus, accurate models of the power converters are not needed, and each component can be represented as current injection at the connection bus. In order to decrease the problem size, the resources, such as local loads and renewable generation, are usually grouped as unique active load. In this case, the generated power by the renewable energy system (RES) is subtracted from the loads' power consumption. However, problems arise if the load has a voltage-dependent power consumption [95]. Especially in LV grids, as simplification of the outer loop controllers, the active and reactive power dependence on grid voltage variations of specific loads can be added, to account for the difference in the power variation of the equivalent bus, when it is subject to voltage variations.

2.6. Fundamentals of HVdc protection

The general philosophy of the protection in HVdc grids coincides with the one in ac grids. However, the constraints that are imposed by the equipment in dc and ac grids are fundamentally different. In ac grids, the protection equipment has to ensure that the fault is cleared before the large synchronous generators lose synchronism during severe disturbances. In HVdc grids, instead, the protection times are constrained by the power electronics equipment, which is much more vulnerable and hence requires much faster protective action. DC grids also impose smaller line impedance and hence the fault propagates rapidly through the HVdc grid, which makes a fast fault identification and clearing necessary in order to avoid large outages and as consequence long restoration time. Another reason for fast clearing is the minimization of the effect of dc faults on the ac transmission grid. HVdc system are usually included in the power flow management and to provide services to the grid. Thus, the temporary loss of the converter controllability in the blocked state during the dc side fault should be kept as small as possible to not interfere with the save operation of the transmission grid and avoid cascading failures [4].

In the following subsection, the fundamentals of HVdc grid protection are briefly summarized. First, it is given an overview of typical fault types in HVdc grids, which is followed by brief explanations of the protection methodologies (more details can be then found in the respective sections on dc circuit breaker (Section 4) and MMC-based protection (Section 5)). Finally, different HVdc grid protection philosophies are explained in order to classify the protection methodologies from a power system point of view.

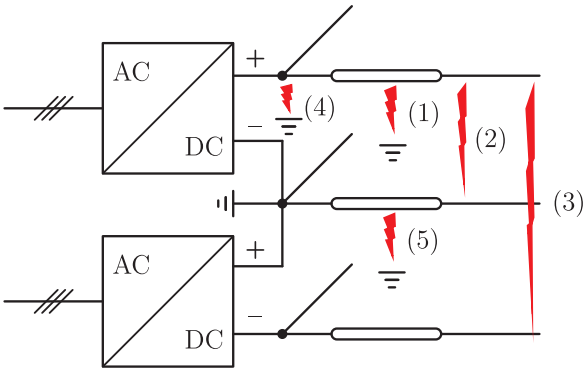


Fig. 2.28: Fault types in HVdc grids.

2.6.1. Fault types in HVdc grids

The fault types in dc grids can be divided into the following categories [4]:

- Pole-to-ground faults
- Pole-to-neutral faults
- Pole-to-pole faults
- Bus faults
- Neutral-to-ground faults

Fig. 2.28 shows the fault types' location at one terminal of a generalized bipolar HVdc configuration.

In the case of pole-to-ground faults (Type (1) in Fig. 2.28), one pole is connected to the ground through a specific fault impedance. The steady-state overcurrent and undervoltage greatly depends on the grounding circuit in this case. In low-impedance grounded asymmetric or bipolar systems, the pole-to-ground fault results in large overcurrents through the grounding electrodes, while the pole voltage is clamped to low value. In high-impedance grounded symmetrical or bipolar systems the steady-state fault current is theoretically zero. However, the pole-to-ground fault defines a new ground reference, such that on the healthy pole an overvoltage of up to twice the nominal value can occur [4].

Pole-to-neutral faults (Type (2) in Fig. 2.28) can occur in bipolar systems or symmetrical monopole systems with metallic return path. This fault type presents similar characteristics as a pole-to-ground fault [4].

The pole-to-pole faults (Type (3) in Fig. 2.28) refer to a connection of the positive and the negative pole through a specific fault impedance. The fault response for both low- and high-impedance grounded systems is similar in this case, because for all configurations a direct path for the fault current exists. This leads to very high overcurrent and low undervoltage, which makes the pole-to-pole fault the most severe fault type in HVdc systems [4].

Bus faults (Type (4) in Fig. 2.28) exist in all above mentioned types and show similar general characteristics as the equivalent pole fault. The difference is that not only a single transmission line, but the whole bus, potentially involving multiple lines in a multi-terminal HVdc system, is lost. Thus, the impact of bus faults is considered to be more severe [4].

Neutral-to-ground faults (Type (5) in Fig. 2.28) generally do not involve large overcurrents or undervoltages [4].

2.6.2. HVdc grid protection methodologies

The existing HVdc grid protection methodologies to interrupt and clear the dc-side short-circuit fault of an MMC-HVdc system can be summarized as follows.

- AC CB-based
- DC CB-based
- Converter-blocking based

In the protection methodology using ac CB, mechanical ac CBs are installed at each converter to interrupt and clear the dc fault [96]. Additionally, slow dc side disconnectors are employed to finally isolate the faulted line, whose location can be determined during the opening time of the ac CB. This protection methodology is particularly slow, due to the delay introduced by the mechanical breakers, which take several cycles (e.g. 2- 3 cycles) of the fundamental frequency to interrupt the fault. During the opening time of the ac CB, the freewheeling diodes of the MMC form an uncontrolled rectifier circuit in the blocked state of the converter. Hence, these diodes should be designed to tolerate the high fault current for a few fundamental cycles, or additional measures, such as thyristor-based bypass circuits, have to be considered to avoid large over-dimensioning of the diodes. In consequence of this protective action, the whole HVdc grid has to be de-energized, resulting in an outage of several cycles. Modular multilevel converters, which submodule capacitors remain charged during the blocked state, can help to regain the proper operation of the HVdc grid after fault clearance. Due the total loss of power transfer and the relatively long outage time, this protection methodology is only applicable for small scale multi-terminal HVdc grids or point-to-point HVdc interconnectors [4].

Employing dc CB in the grid protection, allows the splitting of the HVdc grid into different protection zones. In each zone a primary protection should clear the fault first and back-up protection schemes are considered in the case of primary protection failure. Fast acting dc CB must be installed at each end of a protection zone (inside the protection zone any of the three described methodologies can be applied), or in case full selectivity is desired (defining each transmission line as single protection zone) at each end of a transmission line or cable [32]. Planning the protection system, the trade-off between number of dc CB (and

thus cost and coordination complexity) and the impact of the disturbance on the dc grid has to be carefully solved. Different dc CB concepts have been presented in the literature, i.e. the passive or active resonant mechanical dc CB, the solid-state dc CB (whose technology is not sufficiently mature to date) and the hybrid dc CB, which combines the mechanical and solid-state devices to achieve fast fault clearing and low on-state losses. More details on the different dc CB designs and the general requirements can be found in Section 4. Besides the dc CBs, converters with fault blocking capability, superconducting fault current limiters, or isolated dc/dc converters also can be used to isolate the faulted grid section [4].

The third protection methodology is to embed the dc-fault blocking in the HVdc converter station. Therefore, MMC with fault blocking capability have to be used. A detailed overview on suitable MMC architectures and submodule topologies can be found in Section 5. Interrupting the converter fault current at the dc side, results in a temporary loss of the whole dc power flow, unless options to split the grid in different protection zones and sub-grids are considered. The main advantage of this methodology is that the converter can block almost instantaneously once the fault is detected, which ensures extremely fast fault interruption [4].

2.6.3. HVdc grid protection philosophies

In general, as presented in [4] the HVdc protection system should fulfill three main objectives:

- Minimize the impact of faults in the grid functioning
- Avoid damage of faults to components
- Ensure safe operation of the system

From this general consideration, the article [97] has gathered six criteria to describe an HVdc grid protection philosophy.

1. Reliability: The reliability of the protection system is defined by two factors. First, the dependability of the protection system, which means that the protection system should apply the correct action to faults, which require this kind of protective action. Second, the protection system should be secure, thus should not act, if the situation does not require protective action.
2. Speed: The HVdc protection has to act particularly fast to avoid damage on the components and to limit the impact of disturbances on the grid operation. Moreover, it must be guaranteed that the protection system limits the fault current to the maximum interruptable current.

3. Sensitivity: The HVdc protection system must be sensitive, hence, must be able to detect every fault in the HVdc grid. Special demand is imposed by high-impedance faults.
4. Selectivity: The protection system should be preferably split in protection zones, in order to allow only the faulted zone to be isolated. A protection zone can be either a single transmission line or cable or also a dc subgrid.
5. Robustness: The protection system must be able to react in degraded condition. Indeed, if the primary protection fails, the back-up protection must be able to successfully clear the fault and isolate the faulted zone. Redundancy in the protection equipment, such as additional modules in the breaker or MMC, aid to increase the robustness of the protection system.
6. Stability: The stability is related to the speed of the fault recovery process and is mainly determined by the system outage time after fault. The system must reach stable operation condition in acceptable time after the fault.

The fundamental difference in the HVdc grid protection philosophy is defined by the selectivity criterion. It has to be noted that it must not be confused with the selectivity of the protection equipment, which has to be able to correctly identify the fault section and fault location even in the case of non-selective protection philosophy in order to facilitate a re-start of the healthy remaining part of the grid. Three HVdc grid protection philosophies have been defined in [32] and are shown in Fig. 2.29:

- Non-selective
- Partially selective
- Fully selective

The non-selective fault detection and clearing philosophy defines the complete HVdc system as one single protection zone. Hence, in case of a dc side fault, from the moment of the fault detection, the whole HVdc grid will be de-energized. Before the HVdc grid is de-energized, the faulty line (or faulty subgrid) is identified and after de-energization, slow mechanical disconnectors can be applied to isolate the line. Finally, the remaining healthy part of the HVdc grid is restored to normal operation reestablishing the converters' pre-fault operation [32].

In the partially selective protection philosophy, the HVdc grid is divided into several smaller protection zones or sub grids in order to limit the impact of the disturbance on the dc grid and avoid losing the entire HVdc grid. Therefore, the healthy zones are quickly isolated from the faulty part and the major part of the HVdc system stays in operation. Suitable devices to split the dc grid are HVdc circuit breakers, fault current limiters (e.g. superconducting fault current limiters) and isolated dc/dc converters. Within the faulted subgrid any of the above presented protection methodologies can be adopted [32].

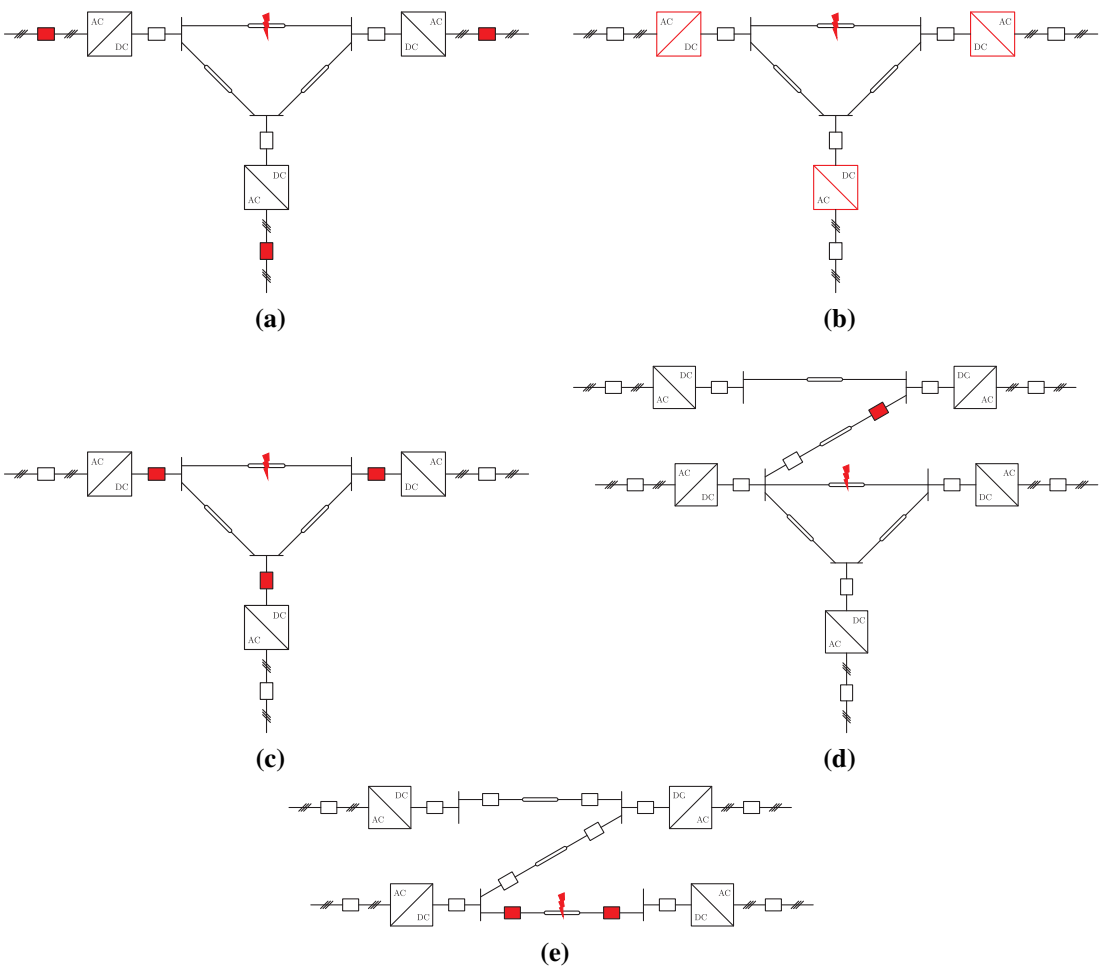


Fig. 2.29: Overview on HVdc grid protection philosophies: (a) Non-selective with ac CB, (b) Non-selective with converter blocking, (c) Non-selective with dcCB, (d) Partially selective,(e) Fully selective.

In the fully selective protection philosophy, the protection zones are defined such that each individual dc branch or node can be protected. To achieve full selectivity, HVdc CBs must be installed at each lines' end. The HVdc CB must be capable to trip immediately and isolate the line, if the fault happens at the specific line (primary protection) and additionally serve as back-up protection for faults in adjacent lines. The fully selective protection philosophy has the lowest impact on the dc system and the ac grid stability due to comparably low loss of power transmission and short outage time. However, at the expense of high costs for the high number of individual HVdc CBs and high coordination effort [32].

A preferred protection philosophy cannot be generally defined, since it is highly dependent on the considered HVdc grid design and the HVdc's desired functionality to the overall transmission system [32].

2.7. Summary and conclusions of the section

The section has provided - in a comparative manner - the fundamental knowledge on HVdc applications, configurations, control and protection. Regarding the preferred control and protection concept for HVdc grids, no general recommendation can be given, and both the control as well as the protection must be chosen case by case. Special focus has been given to the operation of the MMC in the HVdc terminal and the design of the inner terminal controllers, i.e. the converter control, which will be used in the detailed simulation models throughout this thesis, has been presented. Thus, this section forms the theoretical basis for the following research contributions on HVdc grid services and HVdc system protection using dc CBs and MMC. Moreover, a guideline for modeling power electronics (e.g. in the terminals of an HVdc system) in various grid integration studies for wide frequency band (from high frequency ac harmonic stability to steady-state load-flow studies) has been proposed, in which the model complexity differs by factors such as power converter representation, inner and outer control loops, PLL and passive components (ac filters, dc capacitors). The scale is highly modular, such that the respective entry for each power system problem or sub-problem can be scaled up or down to account for new trends in power electronics modeling. The guideline can serve as a reference for future power electronics studies and is used as a reference for the frequency control studies in Section 3.

3. HVdc service provision to ac grids

The landscape of the German power system is changing. Large-scale installation of wind power generation in the North, while the relevant industrial loads still being in the South near the de-commissioned large conventional power plants, raises the need for a grid infrastructure upgrade to maximize the bulk power transfer over large distances and to increase the controllability of the power system. HVdc systems, both point-to-point (interconnectors and embedded) and multi-terminal grids, are foreseen as possible solution to enable a more controllable and reliable power system [58].

The following section aims to introduce the services the HVdc systems can provide to the ac grid. First, an overview of conventional grid services is given with insights on the implementation benefits and challenges. It is revealed that frequency services, such as primary frequency regulation and inertia emulation, cause unwanted disturbances in the supporting ac areas, if no other source of energy is included. Then, to avoid the large-scale implementation of batteries for that reason, this work proposes the HVdc-based control of voltage-dependent loads to participate in the frequency regulation and to relief the burden of supporting areas generators as originally presented in [98]. The concept is applied in HVdc interconnectors and embedded HVdc systems. Finally, based on [99], a control approach is developed, to optimally share the frequency support among the different areas of a multi-terminal HVdc system.

3.1. Overview of HVdc grid services

Grid services or also known as ancillary services are all services, which the grid operator needs, to guarantee a certain level of power supply continuity and which are beneficial for the grid [4]. In the following section, the grid services, which HVdc systems can conventionally provide to the ac grid to preserve its integrity and stability are summarized and their implementation challenges and opportunities are explained. According to [4] these are:

- Power flow control and congestion management
- (Steady-state) voltage control / reactive power control
- Black start and restoration
- Rotor angle stability control and power oscillation damping
- Active power/frequency control and reserves
  - Primary frequency regulation
  - Secondary frequency regulation
- DC transmission reserve

A special focus is laid on the provision of primary frequency regulation and virtual inertia emulation as part of the active power control.

3.1.1. Power flow control and congestion management

In the future power grid, large-scale wind and solar implementation far-off the load centers will require a bulk transmission of the renewable power over large distances [6]. This scenario of relatively fast-changing power generation landscape and delayed grid expansion measures increases the risk for congestion, i.e. the scheduled generated power cannot be transferred to the demand centers due to overloading of specific grid areas or assets. In consequence, the dispatched active power of the power plants must be adjusted, resulting in so called re-dispatch costs [5]. These conventional measures to avoid congestion in the power grid are of preventive nature.

In contrast, employing HVdc systems in the grid increases the control flexibility with low reaction times and hence provides the option for easy and secure curative actions after the congestion occur. This curative approach enables higher loading in normal operation, reducing the costs of preventive measures like re-dispatch [100]. The main feature of the HVdc system is to increase the power flow capability between two remote points. Especially long links can effectively reduce the loading of the parallel ac lines and hence increase the overall power transfer [5]. As an example, in [6] it is shown that by replacing an overloaded ac line with long distance HVdc corridor the system operating limit can be boosted by up to 70 %. It is clear, that the location of the HVdc system in the network is of utmost importance to increase its effects on the power flow controllability. The article [6] introduces a ranking for the HVdc location in the power system based on so-called distribution factors, which determine the influence of an ac line replacement by HVdc system on the loading of the most critical line in the grid.

The fast power flow controllability of the HVdc system - also with the capability to reverse the power flow - supports preventive measures as well as the system's curative response to contingencies and helps to avoid cascading failures in the power system [5]. This dynamic congestion management gains in importance with increasing amount of renewable and distributed power generation, whose fluctuating nature essentially requires the high dynamic management of the power flow to relieve congestion in the network [101].

3.1.2. Steady-state grid voltage support and fault ride through

In conventional ac systems, the charging current of ac lines (either overhead or cables) must be compensated and to enable a stable power transfer, reactive power compensation may be needed depending on the length of the ac line. In the German case, the primary sources of

reactive power are large nuclear and coal-fired power plants, which are intended to be shut down in the near future.

In consequence, to avoid reactive power deficit and following voltage limit violations in specific geographic areas, HVdc systems should participate in the steady-state grid voltage support by reactive power provision. Not only that the HVdc power transmission itself does not require any reactive power, but the stations can operate in STATCOM mode to compensate reactive currents independently at both connection points to further boost the power transfer capacity of the ac grid [7]. This STATCOM requirement is already included in the grid codes for integrating HVdc systems into the power system depending on the voltage and power level [5].

As stated in [5], the efficiency of the reactive power support in contrast to the efficiency of the active power provision (as explained in Subsection 3.1.1) is higher for short HVdc links. Hence, it is more favorable to employ e.g embedded HVdc in systems with high degree of parallelism and meshing, where the short length of the link allows reactive power provision from both sides. A long link instead, since the voltage can be only locally influenced by reactive power, has limited impact on the voltage control in remote parts of the ac system far away from the terminals.

The HVdc systems are providing a large share of the power supply and a disconnection would result in serious power stability problems. Thus, it is important that they stay connected and operational during temporary grid voltage disturbances (such as faults or large load changes) and provide continuously the system support [5, 8]. This feature, known as fault ride through (FRT) (or in the particular case of a voltage dip: LVRT), shall be combined with controlled fast fault current injection as stated in recent grid codes. In this case, the control priority is shifted from active power to reactive power and - if needed - the active power transmission can be reduced. Thus, the HVdc converter terminal can support the grid by injecting positive sequence reactive currents during and after voltage sags and negative sequence currents during unbalanced faults [9]. Grid faults result in low voltage conditions at the converter terminal. Hence one requirement is to support the grid voltage recovery by injecting positive reactive current proportionally with the grid voltage deviation from 0.9 pu. Another task is the injection of negative sequence currents, which, despite reducing the voltage negative sequence during the asymmetric fault, facilitate the operation of protection relays. Provision of reactive currents during fault ride through would be needed in time ranges of 150 ms to trigger protection schemes and support the voltage of the ac grid. Dynamic voltage support after the FRT continues the support up to approximately 1s [100].

3.1.3. Black start and system restoration

In extreme cases, a power mismatch between load and generation can result in large under- or over-frequency deviations potentially triggering a cascade of failures, which finally can result in regional or national blackouts. In the recent example of the Italy blackout in 2003 [102], several interconnection lines tripped resulting in a generation deficit of 6400 MW and generators disconnection due to under-frequency conditions. After such kind of wide-area power outage, which affects several control areas and might not give the possibility of voltage and power provision from neighboring transmission system operators (TSO), a black-start of the power system must be performed, i.e. restarting the power plants and connecting the loads under the condition of zero power supply. Typically the black-start is initiated by pump storage hydro power plants, whose large generators are started by smaller diesel generators beforehand. However, providing a large amount of standby capacity (up to 10 % of the station power is typically required) is costly. In this conventional black-start process, first the voltage is established by synchronous generators in the black-start facilities, which are operated with excitation system and automatic voltage regulation (AVR). Second, the power balance during the connection of loads or generators and hence the frequency control is assured by the governor control acting on the prime mover of the turbine.

Instead, two different VSC-HVdc applications, i.e. HVdc asynchronous interconnector between two areas [20] or HVdc for offshore wind connection [21], can be used as black-start facility. The asynchronous HVdc interconnector also functions as firewall of the system against the failure propagation. The HVdc system in black start mode works in grid-forming control mode (e.g. as a voltage controlled oscillator) to provide effective voltage and frequency stabilization in the affected ac grid, while the dc voltage is maintained by the terminal connected to the non-affected area. In [20], it has been proven by field tests in Estonia, that the HVdc can provide the electrical auxiliary power to start-up dead thermal power stations and synchronize the established island grid with the HVdc converter station being the only ac supply. If the black-start procedure is finished (i.e. the ac voltage is established and other assets in the dead grid, such as transformer, ac lines, loads and generators are re-energized), the HVdc control switches back to the grid-following mode. As reported in [20], a smooth transition can be achieved by applying the measured active and reactive power as initial set-points.

The article [103] summarizes the black-start sequence of the HVdc system as follows: Originally, the HVdc system is in standby mode and the ac breakers in both terminals are open. Then, the ac breakers of the non-affected terminals are closed and the converter is switched on to energize the dc line and build up the dc voltage. The affected terminal converter is energized from small battery energy storage systems (BESS) or in specific cases from the dc line itself. Afterward, the ac CB between the terminal and the transformer in the affected

area is closed and the voltage is ramped up to smoothly energize the transformer. Finally, the ac breaker to the busbar is closed, which re-energizes the dead main ac grid.

Applying the HVdc as standby facility for black-start and ac grid restoration is beneficial in terms of the following aspects [20]: 1) HVdc provides direct control on the voltage, instead of relying on the excitation system with slow dynamics in the generators, which additionally involves under- or overexcitation problems. 2) The HVdc grid forming controller allows a gradual ac voltage increase, which avoids high transformer inrush currents. 3) After the black-start procedure, the HVdc can smoothly balance the power mismatch upwards and downwards to assist during the loads' pick-up and hence speed up the restoration process and avoid the risk of under-frequency load tripping [21]. Moreover, it is not longer necessary to adapt the governor control during the initial phase of the restoration in small island network. 4) Instead of the large standby capacity, the HVdc system only requires small BESS to be installed next to the converter terminal to initially re-start the control and protection equipment.

In [21], the black start support with HVdc system interconnecting a large offshore wind farm with the main power grid is analyzed. In this case, the on-shore converter stations builds up the voltage to establish the electrical island, from which the mainland power grid can be resupplied. The auxiliary power for the start-up process of thermal power plants is in this case provided by the offshore wind farm, which requires changes in the control strategy of the offshore converter station to match the power generation of wind turbines with the onshore network demand.

3.1.4. Power oscillation damping

Traditionally, power system stability problems are related to the synchronous operation of the large synchronous generators, which is determined by the generator rotor angle and the power-angle relationship [104]. In this sense, the rotor angle stability is the ability of the synchronous machines of a power system to remain in synchronism. The rotor angle stability can be further split into transient stability (which is related to the power system's behavior after severe disturbances, such as three-phase faults) and small-signal stability (which is related to minor changes in load or generation) [104]. Following a disturbance in the system, it is as an example assumed that one generator runs faster than another, which results in a difference in their angular positions. In consequence, part of the power is transferred from the slow to the fast machine, which equalizes the angles (stable operation). However, if the angle separation becomes too large, the power transfer can be reduced and the angles further separate, which causes loss of synchronism and hence instability.

The change in the electrical torque (in power system stability analysis the terms torque and power are used simultaneously, as their *per unit* values are almost equal [104]) following

the disturbance can be expressed with two terms, one related to the angle difference, which is called synchronizing torque and another one related to the frequency difference, which is referred as damping torque. While a too small synchronizing torque leads to an aperiodic drift (i.e. steady increase) of the rotor angle, a lack of damping torque results in oscillatory instability (i.e. rotor oscillations of increasing amplitude). As stated in [104], the main small-signal stability problem in today's power systems is related to the insufficient damping of oscillations.

This effect can occur either between one machine and the rest of the system or between groups of machines. The swinging of one generation station with respect to the rest of the system is referred as local (or intra-area) modes, while swinging of groups of machines against machines in other parts of the power system are known as inter-area modes, which are usually caused by two or more groups of closely coupled machines, which are interconnected by weak lines.

As result low-frequency electro-mechanical oscillations occur (i.e. intra-area and/or inter-area oscillations), which are mainly dependent on the system inertia and damping (of the rotating masses of turbines and alternators), the governor control and synchronous generators' excitation system and the power system topology itself. These oscillations usually occur in a frequency range from a fraction to a couple of Hertz, e.g. $0.1 - 0.7$ Hz for inter-area modes and $0.7 - 2$ Hz for intra-area modes. The conventional approach is to use power system stabilizers in the large synchronous generators [104]. However, with the replacement of conventional power plants with renewable ones and a decreasing system inertia, new solutions must be found to provide adequate damping and avoid growing oscillations as possible result of disturbances (faults, loss of a line, etc.) and also in normal operating condition.

HVdc systems often bridge large distances and hence have strong influence on the dominant power system modes, which makes them an excellent choice for power oscillation damping (POD). POD can be achieved with active and reactive power modulation, and a variety of different approaches have been presented in the last years. In the following only a brief description of the general implementation in HVdc links and multi-terminal HVdc systems is provided. For further details refer for example to the review on POD controllers in [10].

The power flow of HVdc systems can be modulated in proportion to the observed frequency deviation between the two ends of the line [11] or also implemented as decentralized control relying only on the local frequency measurement [11, 12]. Another possibility is to use real-time wide area measurements available from the growing number of installed phasor measurements units [10].

The article [11] introduces a concept called 'virtual friction' as POD control based on active power modulation in asynchronous HVdc interconnectors, which couples two lightly damped ac transmission systems. The control is based on the principle of differential and

common power, which allows the POD control action to be decoupled from the HVdc grid voltage regulation. The differential power is defined as

$$p_{\Delta} = \frac{p_{o1} - p_{o2}}{2} \tag{3.1}$$

and describes the power transmission across the HVdc line from one terminal to the other. The common power is given by

$$p_{cm} = -(p_{o1} + p_{o2}) \tag{3.2}$$

and is proportional to the energy stored in the dc capacitors and hence used for the dc voltage control. The two terminal output powers p_{o1} and p_{o2} can be obtained from (3.1) and (3.2) by

$$p_{o1} = p_{\Delta} - \frac{p_{cm}}{2} \tag{3.3}$$

$$p_{o2} = -p_{\Delta} - \frac{p_{cm}}{2} \quad . \tag{3.4}$$

To provide the damping of power oscillations, a droop control is added to the steady-state reference of the differential power $P^*_{\Delta 0}$ as in:

$$P^*_{\Delta} = P^*_{\Delta 0} + d_{\omega}(\omega_1 - \omega_2) \quad , \tag{3.5}$$

in which d_{ω} is the virtual friction constant acting on the difference of the two area frequencies. This control concept is based on communication between the two terminals to exchange the frequency and power references. To avoid control instabilities introduced by a potential communication delay, in [11] it is proposed to use only the local frequency measurement and add additional dc voltage droop term with proportional gain $d_{\Delta dc}$ in the differential power controller as in

$$P^*_{\Delta} = P^*_{\Delta 0} + 2d_{\omega}(\omega^*_1 - \omega_1) - d_{\Delta dc}(V^*_{dc} - v_{dc}) \quad . \tag{3.6}$$

Thus, the mismatch in the differential power references (and consequently in the grid frequencies) can be observed by the local dc voltage deviation from its reference.

In [12], the POD is implemented in a multi-terminal HVdc system. The preferred choice of POD control implementation in this case is the pairing of two terminals of the MTdc system. Thus, the identical reference for the power modulation is applied to two different terminals, but with opposite sign. The power reference for this control scheme is obtained from a superior wide area control system. Pairing two terminals has several advantages, which are: decoupling the POD control from the HVdc voltage control (i.e. the power transmission for the POD does not influence the droop-based HVdc voltage control and the dc voltage is kept approximately constant) ; offering the possibility to predefine different pairing options

and pre-calculate their references for several contingencies and offering the possibility for redundant pairings and thus increasing the reliability of the control. Moreover, it is shown in [12] that pairing results in the highest power oscillation damping effect.

The implementation of the POD controller is as follows, taking into account that proportional controllers are deemed sufficient assuming instantaneous response of the HVdc system to observed frequency deviations [12]:

$$P^* = P_0^* + d_{\omega 1}\omega_1 + d_{\omega 2}\omega_2 \ . \tag{3.7}$$

It has been revealed in [12] that the feedback of the machine offering the smallest inertia and hence is opposed to the largest frequency swing can be sufficient (hence $d_{\omega 2} = 0$ can be assumed in (3.7)). In larger interconnected systems with multiple machines, also the location of the machine with respect to the MTdc system must be considered [12].

The article [12] compares different pairing options depending on the transmission grid structure, in which the MTdc system is embedded. It has been found, that in symmetric networks (i.e. two areas with similar load/generation profile) parallel damping should be used, which means that two terminals, of which one is located in each of the respective areas, are paired and the energy to damp the oscillations is exchanged between the two areas. In contrast, in asymmetric networks, in which a large discrepancy exists between the load/generation profile, perpendicular damping is preferred, i.e. pairing one terminal in the network in which the disturbance is observed with one terminal in a network, which is not directly coupled with the disturbed one. In this case, the energy to damp the power oscillations is obtained from this asynchronously connected network.

3.1.5. Primary frequency regulation

Directly connected prime movers of conventional generation contribute directly with their rotating energy to the system inertia [105]. In fact, the system inertia constant H is proportional to the prime movers' speed of rotation squared and hence proportional to the stored rotating energy in the system, which can be mathematically expressed by

$$H = \frac{\frac{1}{2}J\omega^2}{S_{\text{nom}}} \ , \tag{3.8}$$

where J is the moment of inertia in kgm^2 of the rotating mass, ω is the nominal speed of rotation in $\frac{\text{rad}}{\text{s}}$ and S_{nom} is the nominal power rating of the machine in MVA. Typical values of the inertia constant lie between 2 and 9 s. The inertia determines the system's reaction to a power mismatch between generation and load following either of three causes:

- Loss of generation (generator, importing HVdc, ...)

- Loss of load
- Normal variations in load and generator output

The system dynamic response can be expressed by the Rate of Change of Frequency (RoCoF) [105]:

$$\frac{\mathrm{d}f}{\mathrm{d}t} = \frac{\Delta P}{2H} \ , \tag{3.9}$$

which in turn influences the minimum (or maximum) frequency nadir.

In the last years, an ongoing trend can be observed shifting the energy production share from large conventional generators to renewable ones, such as wind and solar power plants. Due to their power electronics grid interface, those resources do not provide rotational inertia contribution to the grid. Consequently, the system's damping during power unbalances is reduced and faster and larger frequency transients occur, compared to before, when the energy was uniquely produced by conventional generators. Recently, the two major frequency incidents in Continental Europe [106] and UK [107] have placed special emphasis on this issue.

In [19], a practical example of the German transmission grid is given, in which the conventional generators offer an aggregated inertia H=6 s, which is dropping to H=3-4 s during the wind and photovoltaic (PV) plant production peaks. In consequence, the power imbalance occurring after a specific disturbance in the ac grid (such as loss of infeed from RES or large generator or load (dis)connect) or in a possible dc grid or connection (such as converter outage) will lead to increased frequency deviation from the nominal value [15], e.g. from 400 mHz to more than 550 mHz [19].

Conventionally, the primary frequency regulation (PFR) is provided by the governors of synchronous machines adapting their power output linearly with the frequency deviation during the disturbance. However, the effectiveness of the control action is constrained by the turbine's slow dynamic (tens of seconds range). The same service can be provided using VSC based HVdc systems. Those systems can increase the controllability of the grid, varying their power output rapidly (within hundreds of ms) following a frequency disturbance. The frequency support with HVdc systems can be provided from three main sources of energy, which are energy from de-loading of wind turbines (mostly large offshore wind farms), energy from another asynchronous area (only in case of HVdc interconnector or multi-terminal HVdc) or energy from the dc capacitors of the HVdc converter and line. As explained with more details in Subsection 3.2, especially the energy provision from another area is limited due to the impact on the power balance and hence grid frequency in supporting areas. Therefore, in this thesis another source of energy to provide the primary frequency regulation, i.e. energy from voltage dependent loads is considered. An existing field application of the primary frequency regulation by HVdc systems is the Caprivi Link Interconnector HVdc Light, connecting weak grids such as the Namibian and Zambian ones [55, 108].

The implementation of the primary frequency regulation in the HVdc controller can be classified in two main types: 1) Power-frequency (P-f)-droop in the power-dc voltage (P-V_{dc})-droop control and 2) dc voltage-frequency (V_{dc}-f)-droop in the dc voltage-power V_{dc}-P-droop control of multi-terminal HVdc systems. In this thesis, the first case will be adapted for the slave converter's active power control in an HVdc interconnector. Special cases of the PFR are its implementation in power-synchronization controller of HVdc interconnector and in the MMC arm energy controller of an MMC-HVdc system.

Power-frequency (P-f)-droop in the power-dc voltage (P-V_{dc})-droop control Multi-terminal HVdc systems can be controlled with P-V_{dc}-droop to share the burden of dc voltage control and enhance the system resilience towards converter overload or outages. More details on the converter and grid control in multi-terminal HVdc systems can be found in Subsection 2.4.1 and Subsection 2.4.2, respectively. The power reference of the active power controller is linearly adjusted based on the observed dc voltage deviation at the respective terminal [109]. The article [13] extends this control concept to a dual droop controller to enable the PFR option as shown in Fig. 3.1:

$$P^* = P_0^* - d_{\mathrm{vdc}}\left(V_{\mathrm{dc}}^* - V_{\mathrm{dc}}\right) + d_{\mathrm{p}}\left(f^* - f\right) \quad . \tag{3.10}$$

The dual droop controller requires special attention to control stability, since the frequency and voltage droop constants act in opposite directions on the active power reference and hence could cause undesired oscillation degrading the control performance in both dc voltage and frequency. As a solution, the paper proposes to rescale the proportional gain of the frequency droop controller $d_{\mathrm{p,i}}$ of respective converter i with respect to the ratio of the inverse of the voltage droop parameter $d_{\mathrm{vdc,i}}$ of respective converter i to the average of the inverse of voltage droop of the n_{mt} other converters in the MTdc system, which prioritizes the frequency control over the dc voltage control and hence allows the MTdc control system to meet the system operator requirements:

$$d_{\mathrm{p,i}} = d_{\mathrm{p,i0}}\left(1 - \frac{d_{\mathrm{vdc,i}}}{\sum_{j=1}^{n_{\mathrm{mt}}} d_{\mathrm{vdc,j}}}\right) \quad , \tag{3.11}$$

where $d_{\mathrm{p,i0}}$ is the original proportional gain of the frequency droop control.

In [29], this concept, also referred as selective power routing, is extended to the case, where certain areas connected to the MTdc system cannot participate in the provision of inertial and primary frequency support, due to e.g. operation rules, limited power capabilities of the converter terminal or economic constraints. In this case, only a limited number of terminals adapt their power set-points (away from the agreed market set-point) to provide the frequency support, while the other - non-participating - terminals change their control from (P-V_{dc})-droop to constant power control to ensure a proper transition to emergency mode. This is

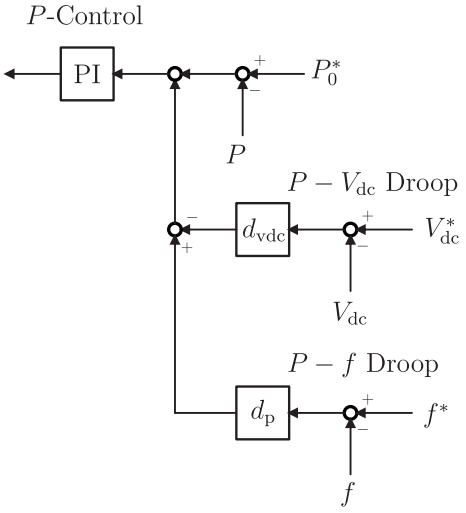


Fig. 3.1: Primary frequency regulation with power-frequency (P-f)-droop in the power-dc voltage (P-V_{dc})-droop control [13].

due to the fact that the change in the MTdc power flow following the frequency support action will also affect the losses in the MTdc system. If all converters remain in (P-V_{dc})-droop mode, the additional losses are shared by all converters, potentially endangering the constrained ones. The droop-control based implementation can be carried out with minimal communication.

In [110], the primary frequency regulation effectively acts in a similar way as in above described methods. However, in this case the necessary change in active power reference is computed with model predictive control (respecting e.g. the limits of the dc voltage and converter ampacity). The model predictive control changes the active power reference along a trajectory from its original agreed set-point to the new set-point with balanced frequency in a finite number of steps.

DC voltage-frequency (V_{dc}-f)-droop in the dc voltage-power V_{dc}-P-droop control Another possible - although with reference to [4] not conventional - way to operate a converter station in an HVdc system is based on the V_{dc}-P-droop control. In [14], it is proposed to use the dc voltage as global measurement to determine power balance of dc terminals in the same way as frequency is used for power balancing in ac systems. In this case, the dc voltage set-point is linearly adjusted with the deviation of the active power from its reference. However, this control strategy decouples the dc grid from the surrounding ac power grids, as the droop-controlled converter terminals behave as constant power node in the ac grid. In [14], it is proposed to combine the V_{dc}-P-droop with an V_{dc}-f-droop to exchange primary reserves within the MTdc system and provide frequency regulation to the ac system (see Fig. 3.2). The dc voltage control set-point of the respective controller V_{dc}^* is derived as follows:

$$V_{\mathrm{dc}}^* = V_{\mathrm{dc},0}^* - d_{\mathrm{dc}}\,(P^* - P) - d_{\mathrm{f}}\,(f^* - f) \quad , \tag{3.12}$$

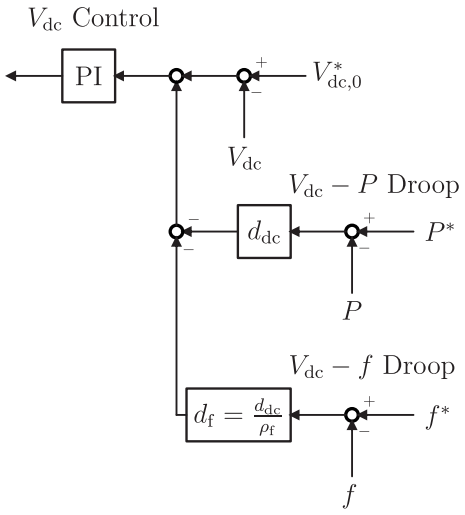


Fig. 3.2: Primary frequency regulation with dc voltage-frequency (V_{dc}-f)-droop in the dc voltage-power V_{dc}-P-droop control [14].

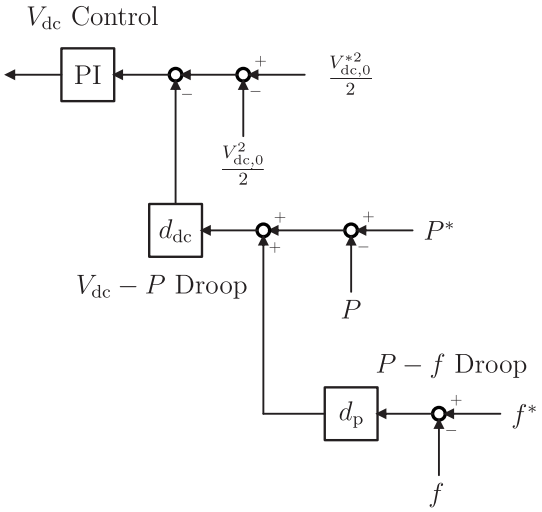


Fig. 3.3: Alternative primary frequency regulation with power-frequency (P-f)-droop in the dc voltage-power V_{dc}-P-droop control [15].

with $V^*_{\mathrm{dc},0}$ being the nominal dc voltage set-point, and d_{dc} and d_{f} the proportional gains of the V_{dc}-P-droop and the V_{dc}-f-droop controller, respectively. The control parameter d_{f} can be obtained with $d_{\mathrm{f}} = \frac{d_{\mathrm{dc}}}{\rho_{\mathrm{f}}}$, whereas ρ_{f} represents the desired amount of frequency droop per unit increment of the active power.

A similar control concept has been developed in [15] as shown in Fig. 3.3, emphasizing the constraints of the autonomous power sharing for primary frequency regulation. It is revealed that the dc voltage set-point variation must be limited to e.g. ± 5 % and that sharing the burden of frequency support results in a distribution of the frequency deviation amongst the formerly asynchronous ac areas, which in turn requests for an optimal tuning of the individual droop parameters in order to reduce the import/export of power by the HVdc converters in the surrounding ac systems.

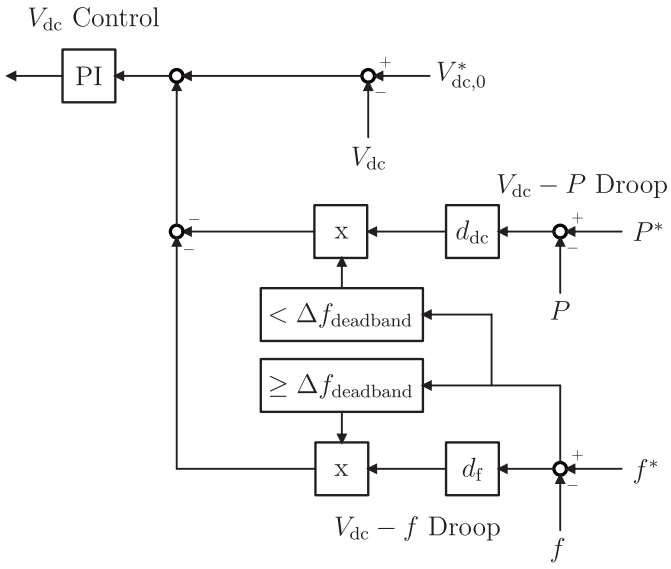


Fig. 3.4: Primary frequency regulation with dc voltage-frequency (V_{dc}-f)-droop in the dc voltage-power V_{dc}-P-droop control with firm control switching [111].

In the case of MTdc systems interconnecting a large offshore wind farm with the onshore ac grid, a cascading control mechanism can be implemented to transfer the energy from rotating mass of wind turbines [111] or de-loading of wind turbines through the MTdc system to provide frequency service in the onshore ac grid [112]. As mentioned in [13] for the case of (P-V_{dc})-droop controlled systems, a parallel operation of multiple droop controllers acting on the same quantity, will result in control interactions and degradation of both controllers' performances. Hence, to give priority to the frequency support in case of emergency, the grid side converters change the dc voltage control with respect to the frequency, i.e. the V_{dc}-P-droop is deactivated and discretely switched to V_{dc}-f-droop mode as shown in Fig. 3.4. The wind side converters change the frequency of the offshore ac grid depending on the dc voltage variation (resulting from the grid side converters' control action), where the wind turbine controllers are equipped with de-loading control responding to the frequency deviation and time derivative of the frequency deviation to provide primary frequency regulation and emulated inertia simultaneously. In [111], additional energy is extracted from non-affected asynchronously-connected onshore ac areas operating also in V_{dc}-f-droop mode during the contingency. After the frequency resettlement, the control of converters connected to non-faulty supporting onshore areas is switched to an active power-frequency droop control to provide the necessary wind turbine recovery power and to avoid a further frequency drop in the affected onshore area. However, similar to the frequency support provision from asynchronous areas, this causes undesired frequency drop in the non-affected areas.

As alternative to firm switching of the control mode, in [30], an adaptive droop control is proposed, which adjusts the dc voltage droop constant and as consequence its reference autonomously depending on the frequency deviation, resulting in a redistribution of the MTdc power flow to provide the PFR (see Fig. 3.5). In this case, a V_{dc}-I_{dc}-droop control is im-

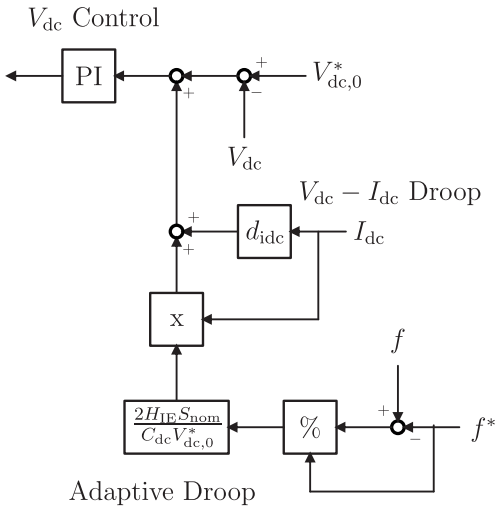


Fig. 3.5: Primary frequency regulation with adaptive V_{dc}-I_{dc}-f-droop control [30].

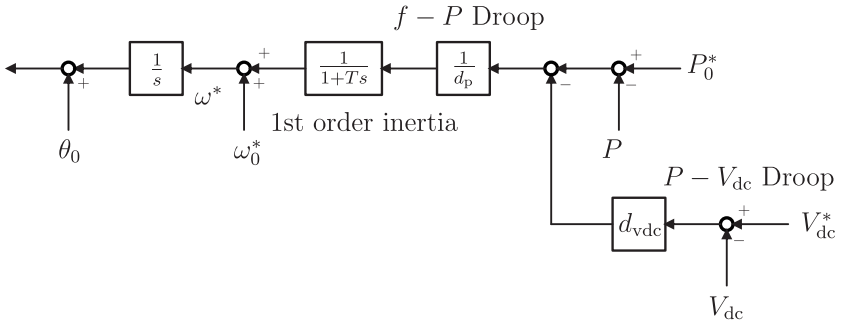


Fig. 3.6: Primary frequency regulation with synchronous generator emulation control [113].

plemented. The gain of the adaptive droop controller is calculated based on a linearization (first-order approximation) of the inertia emulation controller (as presented in [16]), which is referred to as V_{dc}-I_{dc}-f-droop:

$$V^*_{\mathrm{dc}} = V^*_{\mathrm{dc},0} + (d_{\mathrm{idc}} + d_{\mathrm{fi}})\, I_{\mathrm{dc}} \ , \tag{3.13}$$

with $d_{\mathrm{fi}} = \frac{2H_{\mathrm{IE}}S_{\mathrm{nom}}}{C_{\mathrm{dc}}V^*_{\mathrm{dc},0}} \cdot \frac{f-f^*}{f^*}$ being the proportional gain of the adaptive droop controller, which varies depending on the frequency deviation.

Special cases In [113], an HVdc interconnector between two asynchronous areas is assumed. The HVdc system is operating in synchronous generator emulation control (a kind of power synchronization control) with the aim to share the spinning reserve responsibility of the conventional generators, i.e. to provide primary frequency regulation (see Fig. 3.6):

$$\omega^* = \omega^*_0 - \frac{1}{1+Ts}\frac{P - \left(P^*_0 - d_{\mathrm{vdc}}\left(V^*_{\mathrm{dc}} - V_{\mathrm{dc}}\right)\right)}{d_{\mathrm{p}}} \ , \tag{3.14}$$

with T being the time constant of the first-order inertia element. In steady state, the synchronous generator emulation control resembles a (f-P)-droop (i.e. the frequency deviation from its reference is proportional to the active power deviation from its reference).

To avoid frequent changes of the control set-points under small and routine load variations, a sample-and-hold unit with a certain frequency deadband is implemented. The (f-P)-droop is implemented in both converters of the HVdc system, however, with opposite sign of the droop constant. It has to be noted that in order to maintain a stable dc voltage also a (P-V_{dc})-droop is implemented in both converters in parallel with the PFR controller. Since, the active power is a local measurement variable, the control implementation can be considered communication free. As a result, the HVdc system behaves like an ac line interconnecting the two areas, which synchronizes the two (formerly asynchronous) grids and lets the supporting grid frequency experience a large drop. As possible solution, it is proposed a firm under frequency load shedding and a limitation of the maximum admissible active power, which constraints the PFR performance.

A special case for primary frequency regulation of HVdc systems is the embedded HVdc system, which residues in one synchronous ac area and hence no energy is available from asynchronous systems interconnected with the HVdc, since the frequencies at both HVdc terminals are coupled and the simple power transfer does not have an impact on the frequency in this case. Instead in [114], it is proposed to use the capacitive energy of the MMC-terminal stations to provide simultaneous support of primary frequency regulation and system inertia emulation. The energy is extracted by changing the set-point of the MMC arm energy controller and hence varying the dc voltage level of the MMC SM within an acceptable range and exchanging their energy with the faulty ac grid.

Implementation in active power loop In this thesis, following the state of the art, an external droop controller is applied for the HVdc-based primary frequency regulation, which adapts the power set-point of the slave terminal (i.e. the active power controlling terminal) of the HVdc interconnector to an ac frequency variation. The frequency is extracted from the grid voltage measurements through PLL. Without loss of generality it is assumed that the faulty area is labeled with 1 and the supporting area with 2. Assuming a frequency disturbance $\Delta f_1 = f_1^* - f_1$ at the HVdc terminal 1 in Area 1, the measurement signal is send to terminal 2, where the active power reference of the HVdc terminal 2 controller is varied following a droop curve with slope $\frac{1}{d_{\mathrm{p}}}$, with P_{20}^* being the agreed market power set-point:

$$P_2^* = P_{20}^* + \Delta P_1 = P_{20}^* + d_{\mathrm{p}}\left(f_1^* - f_1\right) \ . \tag{3.15}$$

In order to prevent the controller from acting on small and routine load/generation unbalances, where only small deviations around the frequency nominal value occur, a dead-band

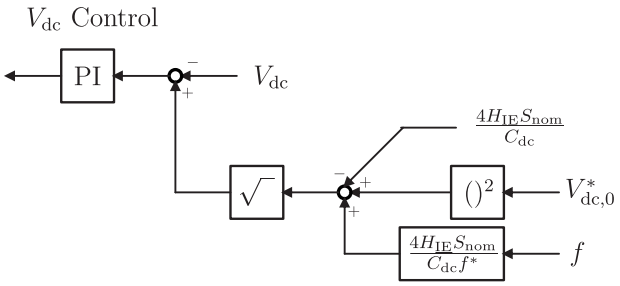


Fig. 3.7: Inertia emulation implemented in dc voltage controller [16].

droop-control is used for the primary frequency regulation. During the control a communication delay has to be considered, which is caused by the distance between the two terminals (e.g. $t_{\mathrm{d}} = 5\,\mathrm{ms}$).

The same controller can be implemented also with Area 2 frequency deviation as input [55, 108]. The control principle will remain the same, such that a frequency deviation would cause a linear change of active power reference. However, the sign of the droop constant will be opposite to the PFR acting on Area 1 frequency.

3.1.6. Inertia emulation

Due to the lack of synchronous inertia in the grid, HVdc systems have to support not only the primary frequency regulation but could also improve the system's initial response emulating virtual inertia. Considering the conventional master-slave control of HVdc interconnector, the inertia emulation control can be implemented either in the dc voltage controlling terminal (master) or in the power controlling terminal (slave).

The article [16] proposes the inertia emulation control implementation as dc voltage set-point variation in the master terminal of point-to-point HVdc (see Fig. 3.7). The energy to support the RoCoF in the grid in this case only comes from the dc capacitance of the HVdc connection (and not from the connected ac areas), which could require significant oversizing of the capacitors [17] to increase the available virtual inertia limited by the maximum permissible dc voltage variation. The approach in [16] computes the relation between the dc voltage set-point and frequency based on the similarity of dynamics of synchronous machine (frequency dynamics) and dc capacitor (dc voltage dynamics) equalizing their respective power equations

$$\frac{2H_{\mathrm{IE}}}{f_0} \cdot \frac{\mathrm{d}f}{\mathrm{d}t} = \frac{C_{\mathrm{dc}} V_{\mathrm{dc}}}{S_{\mathrm{nom}}} \cdot \frac{\mathrm{d}V_{\mathrm{dc}}}{\mathrm{d}t} \quad . \tag{3.16}$$

H_{IE} denotes the emulated virtual inertia, f_0 the nominal grid frequency, V_{dc} the dc voltage and S_{nom} the rated apparent power of the HVdc system.

The measurement of the frequency derivative $\frac{\mathrm{d}f}{\mathrm{d}t}$ is sensitive to noise amplification and can cause control instabilities. Hence, [16] proposes to cancel the dependence on the frequency

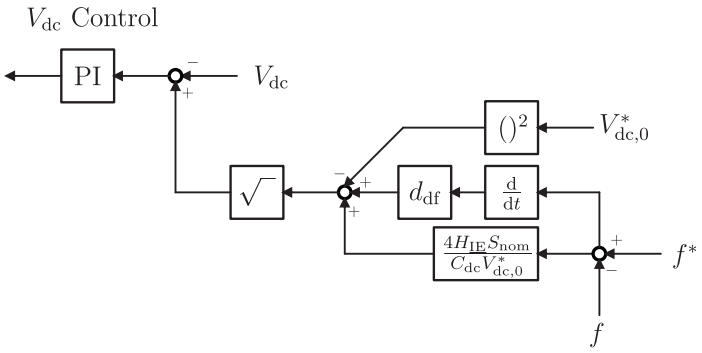


Fig. 3.8: Derivative-based inertia emulation implemented in dc voltage controller [17].

derivative by integrating both sides of (3.16):

$$\frac{2H_{\mathrm{IE}} \cdot f}{f_0} = \frac{C_{\mathrm{dc}} V_{\mathrm{dc}}^2}{2S_{\mathrm{nom}}} + K_1 \ , \tag{3.17}$$

with K_1 being the integration constant, which can be obtained inserting the nominal operating point of frequency f_0 and dc voltage $V_{\mathrm{dc},0}$ in (3.17):

$$K_1 = \frac{2H_{\mathrm{IE}} \cdot f_0}{f_0} = \frac{C_{\mathrm{dc}} V_{\mathrm{dc},0}^2}{2S_{\mathrm{nom}}} = 2H_{\mathrm{IE}} \ . \tag{3.18}$$

The time constant of the emulated virtual inertia with inserting (3.18) in (3.17) and mathematical manipulation results in:

$$H_{\mathrm{IE}} = \frac{\frac{1}{2}\frac{C_{\mathrm{dc}} V_{\mathrm{dc},0}^2}{S_{\mathrm{nom}}} \left[\left(\frac{\Delta V_{\mathrm{dc}}}{V_{\mathrm{dc},0}} + 1 \right)^2 - 1 \right]}{2\frac{\Delta f}{f_0}} \ . \tag{3.19}$$

Finally, the control set-point of the dc voltage controller can be obtained with:

$$V^*_{\mathrm{dc}} = \sqrt{\frac{4S_{\mathrm{nom}}H_{\mathrm{IE}}}{C_{\mathrm{dc}} f_0} \cdot f - \frac{4S_{\mathrm{nom}}H_{\mathrm{IE}}}{C_{\mathrm{dc}}} + V^2_{\mathrm{dc},0}} \ . \tag{3.20}$$

A similar control strategy is applied in [17] in the master terminal of a multi-terminal HVdc system with the extension of a dc voltage set-point variation depending on the frequency derivative. This method requires the measurement of the frequency derivative. However, it is demonstrated a further improvement of the RoCoF. As alternative to the capacitor oversizing, it is proposed to implement a droop controller in the slave terminals, which adapts the power set-points proportionally to the requested change in the dc voltage. However, this would cause a temporary power mismatch in the ac areas connected to the slave terminals similar to the effect of conventional droop-based primary frequency regulation as explained in more details in Section 3.2.

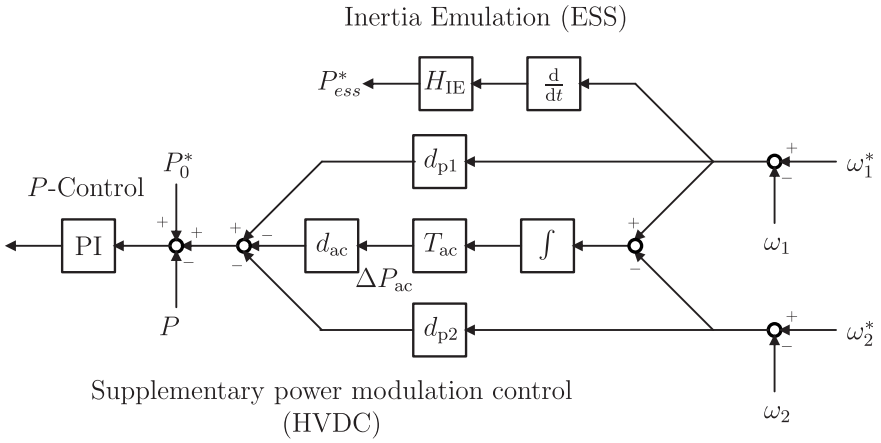


Fig. 3.9: Derivative-based inertia emulation implemented in power controller of ESS and primary frequency regulation by supplementary power modulation control in HVdc [18].

In contrast to the above mentioned methods, [18] presents a derivative control based inertia emulation, which acts on the power set-point of additionally installed energy storage system (ESS). The active power set-point of the ESS is changed proportionally to the frequency derivative (i.e. the RoCoF) with a droop constant. The HVdc system in this case is working with the supplementary power modulation control in parallel with an HVac transmission line and the HVdc active power is varied proportionally to the grid frequencies in both areas and the ac power flow to provide frequency service as shown in Fig. 3.9.

Similar to the behavior of a synchronous generator and following the inertia emulation strategy in [18], an additional power reference term can be also added in the slave control of the HVdc system itself, which is proportional to the derivative of the frequency variation in one area. Without loss of generality the supported area is labeled as Area 1 and the supporting area as Area 2 in the following:

$$P^*_2 = P^*_{20} + d_{\mathrm{p}} \cdot \Delta f_1 + d_{\mathrm{IE}} \frac{\mathrm{d}}{\mathrm{d}t} \Delta f_1 \ , \tag{3.21}$$

being P_{02} the agreed market set-point and d_{p} the proportional gain of the primary frequency regulation.

The proportional gain of the emulated inertia controller d_{IE} is selected to add the desired virtual inertia H_{IE} based on the following equation

$$d_{\mathrm{IE}} = H_{\mathrm{IE}} P_{1,\mathrm{nom}} / f_{1,\mathrm{nom}} \ . \tag{3.22}$$

The article [115] provides a comparison of virtual synchronous machine implementation (i.e. emulated swing equation) in the power controlling slave terminal and inertia emulation based on the dc-bus capacitor dynamics (implemented in the dc voltage controlling master terminal). The inertia emulation control in the master terminal is referred to as virtual syn-

chronous control (i.e. self-synchronization mechanism utilizing the similarities between the dynamics of dc capacitor and machine).

The article [116] compares the inertia emulation implementation with $\frac{\mathrm{d}f}{\mathrm{d}t}$-droop and three types of virtual synchronous machines by Power-Hardware-in-the-Loop experiments carried out with small-scale emulation of MMC-based point-to-point HVdc interconnector of two asynchronous ac areas. It is evaluated in particular the inertia emulation control performance with respect to the equivalent grid inertia (i.e. strong and weak or islanded grid condition). It is revealed that all evaluated implementations can provide the similar inertial response in the weak grid, while differences in the dynamic response and stability properties are obtained in strong grid conditions.

3.1.7. Research questions

The power flow of HVdc systems between two remote asynchronous areas can be adjusted to provide primary frequency regulation during disturbances (e.g. load/generator disconnect or loss of RES power infeed) in order to reduce the required amount of spinning reserve, to diminish the operating costs and increase the penetration of RES. While this action reduces the power deviation in the area affected by the disturbance, it causes a temporary power imbalance in the other healthy ac area, leading to a frequency variation of up to 500 mHz [15] and endangering the system stability. Industrial documents [55, 108] showed that this represents a huge restriction in frequency regulation depending on the strength of the supporting grid.

Moreover, the existing control strategies are mostly applied in case of asynchronous areas connection, giving the possibility to extract energy from one area and transmit it to the other or offshore wind farm connection, in which the energy can be extracted from the de-loading of the wind turbines to provide the frequency support. However, modern power systems, being limited in building new infrastructure, embed HVdc systems in ac grids, forming hybrid HVdc-HVac interconnections within a single synchronous control area [117]. Practical examples are the SuedLink and SuedOstLink projects in Germany [118], both 2 GW underground cable HVdc links. These links are designed to transmit the energy from the wind power plants in the north of Germany toward the southern industrial load centers, to compensate the missing energy from decommissioned nuclear and gas power plants. Both projects are co-operated by two different TSOs, demonstrating that HVdc applications are not only limited to single-operator systems.

To overcome these limitations, an HVdc based primary frequency regulation strategy should be designed, which minimizes the impact on supporting ac areas and can be generalized to both asynchronous HVdc interconnectors (e.g., between Germany and Denmark - Fig. 2.5(a)

and embedded HVdc systems forming a parallel, hybrid connection with existing HVac grid (in green in Fig. 2.5(b)), such as planned HVdc corridors in Germany (in pink in Fig. 2.5(b)).

3.2. Primary frequency regulation with HVdc systems controlling voltage dependent loads

In the following section, a primary frequency regulation with HVdc terminals controlling voltage dependent loads (PFR-VDL), e.g. industrial aluminum or steel plants or HV substations [119], is proposed. The HVdc terminal connected to the healthy area exploits the loads' voltage-power characteristic [23] and varies the grid voltage amplitude to shape (upward and downward) the loads' active power consumption in order to balance the power variation required by the fault-affected area. The PFR-VDL extracts the needed energy for the frequency support, not from the generators (with following frequency deviation) but from the voltage-dependent loads in the healthy area.

This technique has seen several applications with static var compensators [24], synchronous condensers [25], Smart Transformers [26] and load tap changers. The latter, however, seem more suitable for secondary/tertiary frequency control, due to their relatively slow dynamic that is more appropriate for conservation voltage reduction [120].

First, the general background of the loads voltage-power characteristic and the implementation of PFR-VDL approach by HVdc-terminals are explained. Afterward, the PFR-VDL performance (i.e. its application benefits and limitations) in both asynchronous HVdc interconnector and embedded HVdc (simplified with a parallel, hybrid connection with HVac) is evaluated analytically with a state-space representation of a simplified two-area system. The results are verified by means of PSCAD EMTDC simulations of the two-area system and finally validated with large interconnected IEEE 39 bus system.

3.2.1. Fundamentals of primary frequency regulation controlling voltage dependent loads

Load modeling In dynamic power system analysis, the load modeling, i.e. the mathematical representation of the load power to voltage (or frequency) dependency is a critical task. Even though the individual load data might be available, the estimation of the aggregated load characteristic is challenging. In [121], an industry survey among the TSO and Distribution System Operators (DSO) in Europe has been conducted to identify conventionally applied load models. Results show that the load active power consumption is modeled in 43% of the cases with a static constant power, current or impedance behavior. 21% of the

loads are modeled combining the three polynomials (called ZIP-model), 10% use static exponential load modeling, 16% ZIP plus induction machine and 8% detailed composite model. The more complex models including the simplified representation of induction machines or the load recovery, however, are not suitable for real-time application.

The exponential load model describes the load active (and reactive power) dependency on the voltage variation with a reduced number of parameters. In the following, only the equations for active power are presented, since the focus of the primary frequency regulation is the balance of active power consumption and generation. The load active power consumption P with respect to the grid voltage variation is given by

$$P = P_0 \cdot \left(\frac{V}{V_0}\right)^{K_\mathrm{p}} \quad , \tag{3.23}$$

where V is the rms value of the grid voltage, P_0 is the active power consumption at the nominal rms voltage V_0 and K_p is the active power to voltage dependency coefficient. The advantage of the exponential load model is its simplicity, since only one parameter for the active power (and another one for the reactive power) have to be identified. The simplicity can, however, also lead to less accurate results, if large power variations are measured [122].

The polynomial ZIP-model is an aggregate load model that combines different responses of the load power variation on voltage changes, including the static constant power, current and impedance terms:

$$\frac{P}{P_0} = p_\mathrm{z} \cdot \left(\frac{V}{V_0}\right)^2 + p_\mathrm{i} \cdot \left(\frac{V}{V_0}\right)^1 + p_\mathrm{p} \cdot \left(\frac{V}{V_0}\right)^0 \quad , \tag{3.24}$$

where p_z, p_i and p_p are the constant impedance, constant current and constant power *per unit* share of the total nominal aggregated load, thus $p_\mathrm{z} + p_\mathrm{i} + p_\mathrm{p} = 1$. The main drawback is that dependencies higher than constant impedance are difficult to be represented with the ZIP model and higher order equations become necessary. A possible example is the transformer dependency to reactive power, which can reach values up to 4 p.u. to 7 p.u. [123].

Applying the Taylor expansion, polynomial ZIP-models (including the static constant power, current and impedance models) can be expressed by their equivalent exponential parameters following the relation given in [121]:

$$K_\mathrm{p} = \frac{p_\mathrm{p} \cdot 0 + p_\mathrm{i} \cdot 1 + p_\mathrm{z} \cdot 2}{p_\mathrm{p} + p_\mathrm{i} + p_\mathrm{z}} \quad . \tag{3.25}$$

The main advantage in using the exponential model over the polynomial model is the reduced number of parameters and hence a simpler representation of the loads' behavior without losing in accuracy, normally. In total, static exponential load modeling can express more

than 70% of all used dynamic load models and hence is best suited as unified model to represent aggregate loads [119].

Load voltage sensitivity In general, the load power consumption can be expressed as

$$P = P(V, f, t, P_0) \tag{3.26}$$

which indicates the load consumption dependence on the rms voltage and frequency (in *per unit*). The term t is the time dependency due to load restoration and P_0 is the nominal condition at a given grid voltage, which depends on the amount and type of connected equipment. To be noted that in the following the load dependence to frequency, which can be expressed with the linear coefficient K_{fp} as follows

$$P = P_0 \cdot \left(K_{\mathrm{fp}} \frac{f - f_0}{f_0} \right) \tag{3.27}$$

is neglected and it is considered that the frequency (at the load's point of connection) is left unchanged at its nominal value f_0 in the remainder of this section.

A general expression for the load active power to voltage sensitivity, i.e. the deviation of the load consumption dP following a variation in the grid voltage rms value dV from its nominal value, can be found with

$$\chi = \frac{\frac{\mathrm{d}P}{P_0}}{\frac{\mathrm{d}V}{V_0}} \ . \tag{3.28}$$

To calculate the load sensitivity to voltage for the exponential model, the power expression in (3.23) has to be differentiated with respect to the voltage. It follows

$$\frac{\mathrm{d}P}{\mathrm{d}V} = K_{\mathrm{p}} \cdot P_0 \cdot \left(\frac{V}{V_0} \right)^{K_{\mathrm{p}}-1} \cdot \frac{1}{V_0} \ . \tag{3.29}$$

Evaluating (3.29) in the nominal voltage, i.e. $V = V_0$ results in

$$\frac{\frac{\mathrm{d}P}{P_0}}{\frac{\mathrm{d}V}{V_0}} = K_{\mathrm{p}} \ . \tag{3.30}$$

And thus, in case of exponential load model, the load active power to voltage sensitivity is equal to the respective dependency exponent. It can be easily found that

$$\frac{P_{\mathrm{i}}}{V_{\mathrm{i}}^{K_{\mathrm{p}}}} = \frac{P_0}{V_0^{K_{\mathrm{p}}}} \tag{3.31}$$

and consequently

$$\frac{\frac{\mathrm{d}P}{P_\mathrm{i}}}{\frac{\mathrm{d}V}{V_\mathrm{i}}} = K_\mathrm{p} \tag{3.32}$$

for any arbitrary operating point i. From (3.32), it can be concluded that the active power to voltage sensitivity is independent of the initial operating point condition.

For ZIP-model instead the power derivative over voltage from (3.24) follows as

$$\frac{\mathrm{d}P}{\mathrm{d}V} \cdot \frac{1}{P_0} = p_\mathrm{i} + p_\mathrm{z}\frac{V}{V_0} \ . \tag{3.33}$$

Again evaluating it in the nominal operating point $V = V_0$ results in

$$\frac{\frac{\mathrm{d}P}{P_0}}{\mathrm{d}V} = p_\mathrm{i} + p_\mathrm{z} \ . \tag{3.34}$$

Even considering $p_\mathrm{p} + p_\mathrm{i} + p_\mathrm{z} = 1$, the mathematical problem given by (3.34) is underdefined, since three parameters must be identified from which two are independent. Hence, to estimate the load sensitivity at least one parameter must be assumed known a priori or dependent on the other ones. However, as stated above, each ZIP-model can be transformed into an exponential model, for which the single parameter can be easily identified.

The load power to voltage sensitivity generally depends on the loading conditions, such as weather, season or day-time [119, 124], and the composition of the aggregated load, which represents hundreds or thousands of individual devices connected to the same substation. Table 3.1 summarizes the results of several studies - industry surveys in Europe and America [119, 121] and measurements in Serbian medium voltage (MV) grids [124] and Guadeloupe island [125] - which have been carried out with the aim to identify the sensitivity of aggregated and large individual power system loads. As reported in [119], residential loads exhibit a sensitivity (expressed with equivalent exponential parameter K_p) varying between $K_\mathrm{p} = 0.9$ in summer and $K_\mathrm{p} = 1.7$ in winter and commercial loads lay in the range of $K_\mathrm{p} = 0.5 \ldots 0.8$. The world median is assumed to be $K_\mathrm{p} = 1$, which represents constant current behavior. Independent of the voltage level, the authors of [121] have concluded from an industry survey among Americas network operators, that the equivalent sensitivity is between $K_\mathrm{p} = [1 \ldots 1.5]$. These assumptions are confirmed by measurements in medium voltage grids [124], where the aggregated load (dominated by residential loads) shows a mean value of $K_\mathrm{p} = 1.35$. In [24], the average load active power to voltage sensitivity in transmission grids is equal to $K_\mathrm{p} = 1.3$, while measurements in Guadeloupe island showed a sensitivity $K_\mathrm{p} = 1.5$ for primary substations [125].

This thesis considers active power to voltage sensitivity $K_\mathrm{p} = 1.8$, in line with the results of [119], where the highest share of load participating in frequency services (59 %) are industrial aluminum plants with average load sensitivity $K_\mathrm{p} = 1.8$. However, the general positive

Table 3.1: Real grid load sensitivities K_p.

Load type	Equivalent K_p	Reference
Commercial (summer/winter)	0.5 / 0.8	[119]
Residential (summer/winter)	0.9 / 1.7	[119]
America HV average	1.0 - 1.5	[121]
HV aggregated load	1.3	[24]
MV aggregated load	1.35	[124]
Primary substations	1.5	[125]
Steel mills	0.6	[119]
Industrial aluminum plants	1.8	[119]

effects involving the loads in the frequency support provision by HVdc systems are not impeded by a lower load sensitivity. It only reduces the operation margin of the frequency support provision, since the same active power contribution requires larger voltage variations.

Load identification and control Two approaches have been adopted to identify the load sensitivity, namely the measurement-based and component-based approach. The measurement-based approach relies on the field data available from e.g. phasor measurement units [126] and digital fault recorders at representative substations and feeders [121, 127]. The main benefit is the availability of a large set of data due to its worldwide application. However, the measurements can only be conducted for specific grid disturbances (with limited grid impact) [128] and require a relatively long data history to provide general results. Afterward, the obtained data is fitted to the actual load models. As mentioned in [129], another drawback is the confidentiality of the obtained data of the load itself. Instead, it is proposed to estimate the voltage sensitivity by instantaneous measurements of load active and reactive power and frequency deviations at the grid connection point of the load and neighboring buses. In the component-based approach, the response of individual load components in the laboratory is collected and aggregated in (sub-)classes of models, which take into account different loading conditions [124, 130]. The aggregation is performed with weighted averaging or curve fitting techniques.

In average over 50% of load identification is performed based on offline measurement data processing. While this is suitable for load identification in steady-state or dynamic studies, the missing capability to provide real time information on the load status limits their application in determination of proper corrective actions in grid disturbance situation.

Flexible, voltage-dependent loads have been considered as a valid contributor to the balancing of load demand and power generation. During contingency situations, an additional power reserve can be raised, which reduces the need for energy storage systems and limits the degradation effects on synchronous generators. The loads power consumption can be

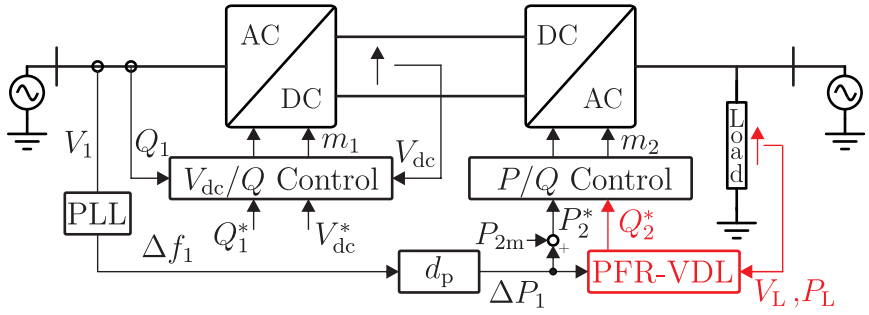


Fig. 3.10: HVdc control scheme with additional PFR-VDL.

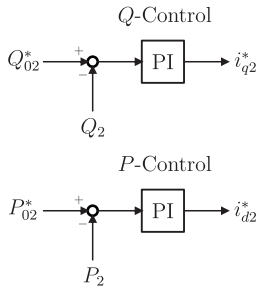


Fig. 3.11: HVdc slave-converter control: Outer control loops.

shaped through controlled voltage variations, a service that can be considered for economic dispatch, primary frequency regulation and contingency reserves [131].

PFR-VDL algorithm implementation As starting point, it is assumed a point-to-point HVdc system (see Fig. 3.10), in which one converter - the master - is controlling the dc voltage constant (in Fig. 3.10 it is the converter connected to area 1) and the second converter - the slave - is operating in constant active power control mode (in Fig. 3.10 it is the converter connected to area 2) to exchange the active power with the ac grid. In both converters the reactive power can be controlled independently using decoupled vector control in the dq-reference frame.

In the following, as depicted in Fig. 3.10, the PFR-VDL algorithm is implemented in the slave converter of the point-to-point HVdc. For simplicity, only the outer loops of the slave converter control are shown in Fig. 3.11, while inner current loop, PLL and the modulation are neglected in the following figures and explanations.

The first step of the PFR-VDL algorithm is the implementation of the primary frequency regulation introduced in Subsection 3.1.5 and repeated in Fig. 3.12. A dead-band droop control with proportional gain d_p and a dead-band of e.g. 100 mHz is applied for the PFR to prevent frequent control actions for small deviations around the nominal frequency value resulting from small and routine load variations. Both the active power P_2^* and reactive power set-points Q_2^* are limited by the maximum converter ampacity.

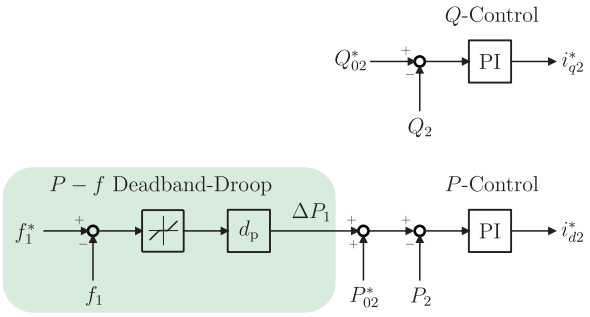


Fig. 3.12: HVdc primary frequency regulation in slave-converter control.

For a proper integration of voltage dependent loads in the primary frequency regulation of HVdc systems, it is vital to obtain real time knowledge on the actual status of the load. Hence, the online load active power sensitivity to voltage identification as originally proposed in [132] is used. The concept is based on the measurement of the loads reaction in terms of active power consumption P_L following a controlled voltage disturbance in the grid (see Fig. 3.13). In this case, the HVdc terminal applies a controlled reactive power injection to the grid that influences the load voltage amplitude V_L. This methodology allows the load power sensitivity to voltage K_p estimation in real-time, whenever it is needed or at regular time intervals (e.g. every few minutes see Fig. 3.16). The discretization of (3.30) gives:

$$K_\mathrm{p} = \frac{\frac{P_\mathrm{L}(t_k)-P_\mathrm{L}(t_{k-1})}{P_\mathrm{L}(t_{k-1})}}{\frac{V_\mathrm{L}(t_k)-V_\mathrm{L}(t_{k-1})}{V_\mathrm{L}(t_{k-1})}} \ , \tag{3.35}$$

where $P_\mathrm{L}(t_k)$, $P_\mathrm{L}(t_{k-1})$, $V_\mathrm{L}(t_k)$, and $V_\mathrm{L}(t_{k-1})$ are the active power and voltage measurement at a certain time step t_k and its previous one t_{k-1}. Focusing on the application in high voltage grids, in this study, it can be assumed that the load sensitivity does not vary substantially within the chosen time resolution (minutes range). Following the results of [133], in which it is demonstrated that in MV grids the load sensitivity varies in tens of minutes or hours, in HV grids a slower variation can be expected. The approach only relies on local measurements collected during the voltage and power variation at the interested HV substation (i.e. the controlled load), where the load sensitivity value is evaluated and sent to the HVdc controller with a specific time stamp. Hence, a fast communication is not required, but the conventional communication infrastructure (e.g. using Ethernet technology with data transmission rate of 100kSamples/s and speed in the range of hundreds of microseconds for sampled values [134]) can be employed, which is to a large extent vendor specific and in the future can potentially adopt similar structure as defined by the IEC 61850 for digital substations [134].

Knowing this sensitivity, the load active power consumption can be influenced varying the

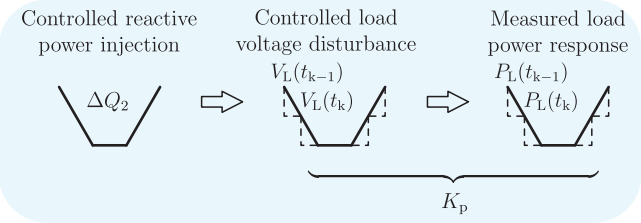


Fig. 3.13: HVdc-based load sensitivity identification.

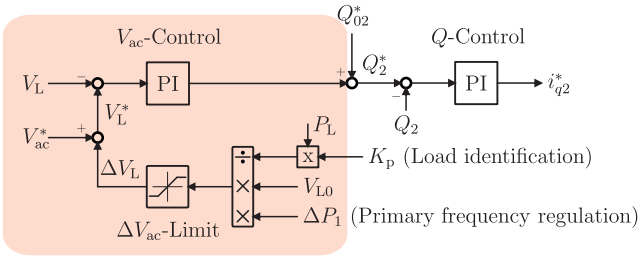


Fig. 3.14: HVdc-based control of voltage dependent loads.

voltage in Area 2 in *per-unit* by $\Delta V_L/V_0$:

$$\frac{\Delta V_L}{V_0} = \frac{\Delta P_1}{P_L K_p} = \frac{d_p \cdot \Delta f_1}{P_L K_p} \quad , \tag{3.36}$$

where ΔP_1 is the power variation requested by the droop controller d_p to compensate the frequency error Δf_1 in Area 1.

As shown in Fig. 3.14, the HVdc terminal 2 injects a controlled amount of reactive power Q_2^* in order to provoke a variation in the load voltage ΔV_L and consequently a change of the loads active power consumption:

$$Q_2^* = (\underbrace{V_{ac}^* + \Delta V_L}_{V_L^*} - V_L)\left(k_{p,V} + k_{i,V}\frac{1}{s}\right) \quad , \tag{3.37}$$

where V_L and V_L^* represent the load voltage actual and reference value, respectively.

In order to handle the power quality challenge, the grid voltage variation in the PFR-VDL is only applied as short-term action and is activated as additional reference only in abnormal frequency conditions. After frequency resettlement, the grid voltage and HVdc reactive power reference are restored to their pre-fault nominal values. Moreover, grid voltage variation limits of current ENTSO-E network codes for secure grid operation ($0.9-1.118$ pu) [27] or the stricter constraints of maximum voltage step-change due to reactive power injection in the technical requirements for grid connection of high voltage direct current systems (i.e. ± 0.02 p.u. [28]) are respected and due to the real time identification of the load sensitivity, it is known beforehand the requested voltage variation at the load point and the compliance with the grid voltage constraints can be checked in advance.

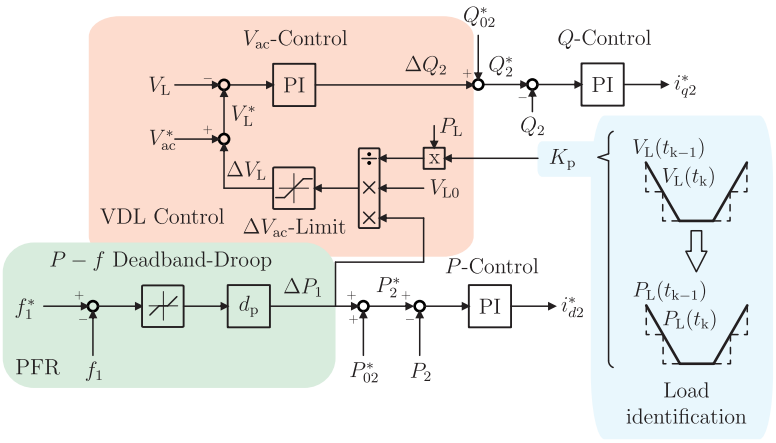


Fig. 3.15: HVdc PFR-VDL control loops in slave-converter control.

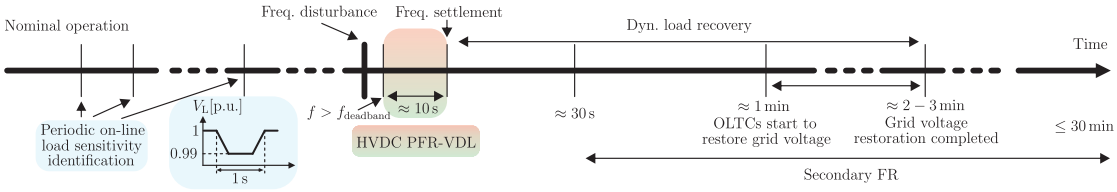


Fig. 3.16: Timeline of HVdc PFR-VDL application in frequency disturbance case.

The overall control scheme of the PFR-VDL algorithm is shown in Fig. 3.15 and its implmentation timeline with respect to conventional grid frequency control in Fig. 3.16.

After some time, the automatic generation control (secondary frequency control) slowly restores the ac frequencies to their nominal or scheduled values, i.e. by that time the load difference is entirely balanced by the generators [113]. In case the two interconnected grids residue in different control areas also the HVdc voltage and interchange power between the control areas are brought back to the original contracted value, while in the case the interconnected grids are considered as one control area only the dc voltage is restored.

Load recovery After the disturbance and control action of PFR-VDL, certain loads will slowly recover and on-load tap changers (OLTC) will restore the voltage. Typically, this action starts one minute after a drop in voltage occurred and the voltage restoration is completed within another one or two minutes [119]. Measurements in medium voltage distribution network in Serbia have confirmed a load recovery time constant around $T_p = 398.1$ s for voltage step up and $T_p = 221.5$ s for voltage step down [124].

The PFR-VDL is a short-term action applied for approximately the first ten seconds after the disturbance (see Fig. 3.16), which leads to the conclusion that the load recovery phenomenon can be neglected and the use of static exponential modeling is justified.

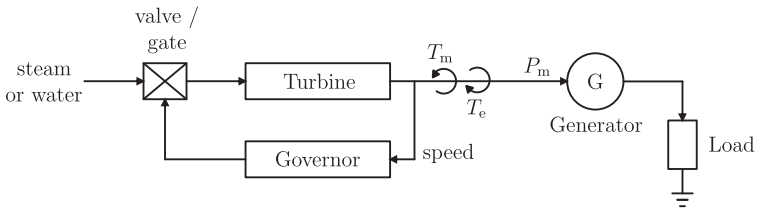


Fig. 3.17: General structure of generating unit.

3.2.2. Analytical results of primary frequency regulation with HVdc systems controlling voltage dependent loads

To evaluate the HVdc PFR-VDL performance analytically and ease the results replication, the simplified transmission grid benchmark with two areas and two machines presented in [104] is considered. This model is an accurate representation of the system with the minimum required level of details for frequency control studies [74].

Model derivation: Equivalent ac area modeling In each area there is assumed one generating unit, which has the general structure depicted in Fig. 3.17. A load change in this system, will cause an instantaneous change in the electrical torque of the generator, resulting in a mismatch between the electrical T_e and the mechanical generator torque T_m, which in turn results in a variation of the rotor speed $\Delta\omega_r$ determined by the equation of motion:

$$\Delta\omega_r = (T_m - T_e)\frac{1}{2Hs} \quad . \tag{3.38}$$

To study the frequency control in power systems, it is preferred to express the generator dynamic relationship in terms of power rather than torque:

$$P = \omega_r T \quad . \tag{3.39}$$

Now considering a small deviation around the nominal operating point gives:

$$P = P_0 + \Delta P \tag{3.40}$$

$$T = T_0 + \Delta T \tag{3.41}$$

$$\omega_r = \omega_{r0} + \Delta\omega_r \quad . \tag{3.42}$$

Inserting (3.42) in (3.39) gives:

$$P_0 + \Delta P = (\omega_{r0} + \Delta\omega_r)(T_0 + \Delta T) \quad . \tag{3.43}$$

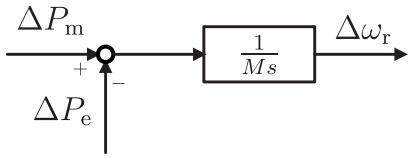


Fig. 3.18: Equivalent model of generators frequency response to a load change.

Neglecting higher order terms in (3.43) results in

$$\Delta P = \omega_{\mathrm{r}0}\Delta T + \Delta\omega_\mathrm{r} T_0 \ . \tag{3.44}$$

Evaluating (3.44) for the difference between the mechanical and electrical power leads to:

$$\Delta P_\mathrm{m} - \Delta P_\mathrm{e} = \omega_{\mathrm{r}0}\left(\Delta T_\mathrm{m} - \Delta T_\mathrm{e}\right) + \Delta\omega_\mathrm{r}\left(T_{\mathrm{m}0} - T_{\mathrm{e}0}\right) \ . \tag{3.45}$$

Considering that in steady-state the electrical and mechanical torque are equal and assuming the angular frequency in *per unit*, i.e. $\omega_{r0} = 1$, (3.45) simplifies to

$$\Delta P_\mathrm{m} - \Delta P_\mathrm{e} = \Delta T_\mathrm{m} - \Delta T_\mathrm{e} \ . \tag{3.46}$$

And thus the generators frequency response to a load change (summarized in Fig. 3.18) can be expressed with:

$$\Delta\omega_\mathrm{r} = \left(\Delta P_\mathrm{m} - \Delta P_\mathrm{e}\right)\frac{1}{Ms} \ , \tag{3.47}$$

where $M = 2H$ represents the equivalent system inertia created by the rotating machines.

Resistive loads (such as lighting) are independent of frequency changes, while the electrical power of motor loads (such as pumps) changes with the frequency due to changes in the rotor speed. In aggregate the load response to frequency deviation can be expressed with

$$\Delta P_\mathrm{e} = \Delta P_\mathrm{L} + D\Delta\omega_\mathrm{r} \ , \tag{3.48}$$

where ΔP_L is the non-frequency sensitive load change and D is the load damping constant, which expresses the percent change in the load for one percent change in the frequency and typically obtains values of $D = [1...2]$. Thus, in absence of a speed governor the system response to power variation is determined by the equivalent system inertia constant and the damping constant, which is summarized in Fig. 3.19.

If two or more generators are connected to the same system, an isochronous governor (ideal integral plant with gain G, which restores the frequency automatically back to its nominal value following a disturbance) cannot be used anymore, since all generators had to have exactly the same speed settings [104]. Hence, an additional droop feedback must be considered as shown in Fig. 3.20. The governor dynamic is simulated with a first order low pass filter representation with time constant $T_\mathrm{G} = \frac{1}{GR}$. The constant $-\frac{1}{R}$ represents a proportional

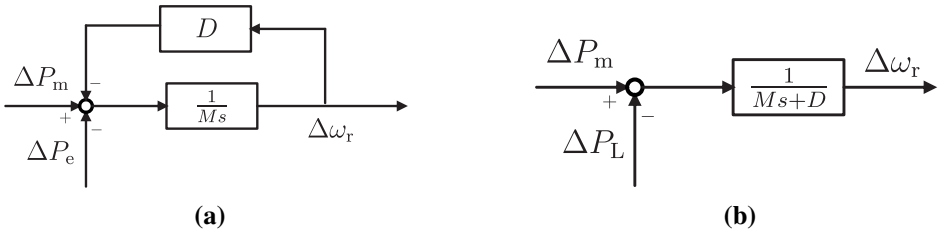


Fig. 3.19: Equivalent model of load response to frequency deviation: (a) Structure, (b) Transfer function.

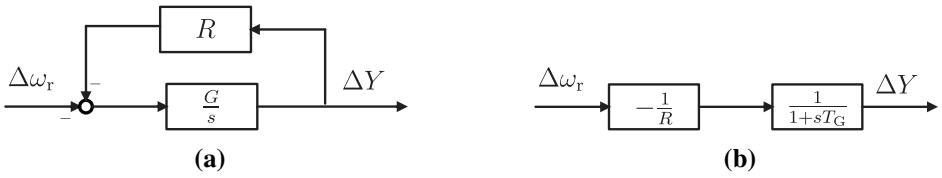


Fig. 3.20: Equivalent model of governor with frequency-droop characteristic: (a) Structure, (b) Transfer function.

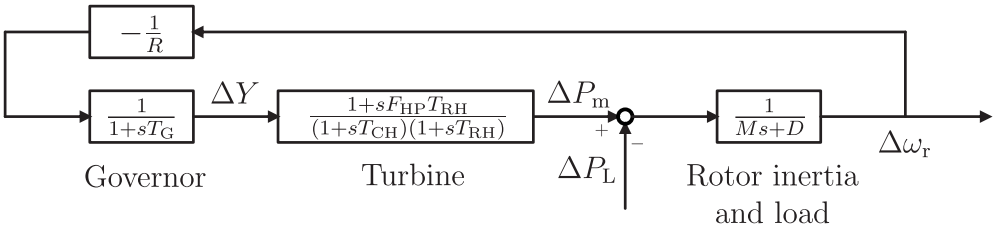


Fig. 3.21: Representation of one area with equivalent machine and load, reheat steam turbine and governor.

frequency controller, in which the frequency droop R determines the steady-state frequency-load characteristic of the generating unit. It has to be noted that usually in load frequency control studies, the inter-machine oscillations are neglected and all machines in one area are aggregated in one equivalent machine.

Considering now the relative response rate of the reheat steam turbine by its transfer function between the turbine torque (or power, if $\omega_{r0} = 1$) and the control valve position Y:

$$\frac{\Delta P_\mathrm{m}}{\Delta Y} = \frac{1 + sF_\mathrm{HP}T_\mathrm{RH}}{(1 + sT_\mathrm{CH})(1 + sT_\mathrm{RH})} \quad . \tag{3.49}$$

T_RH, F_HP, F_LP and T_CH represent the reheater time constant, power fraction of high and low pressure section and time constant of the main inlet volume of the turbine, respectively. This study only focuses on reheat steam turbine generator systems, while there exist several different types of turbines with different time constants and transients, resulting in smoother or more oscillating frequency behavior. However, it can be assumed that the general impact of HVdc frequency control will not differ substantially from case to case. The overall representation of one area with equivalent machine can be expressed as in Fig. 3.21.

Model derivation: Equivalent transmission system modeling The second step of the model derivation is the transmission line representation. Assuming a loss-less line, the voltage phasor at the sending end $\tilde{E}_\mathrm{s}$ with respect to the voltage and current phasor at the receiving end $\tilde{E}_\mathrm{r}$ and $\tilde{I}_\mathrm{r}$, respectively, the characteristic line impedance Z_c and $\theta = \beta x$, where β is the imaginary part of the wave propagation constant, also known as phase constant, and x is the position at the line, according to [104], can be expressed with

$$\tilde{E}_\mathrm{s} = \tilde{E}_\mathrm{r}\cos\theta + \mathrm{j}Z_\mathrm{c}\tilde{I}_\mathrm{r}\sin\theta \ . \tag{3.50}$$

Let δ be the angle, by which the sending end voltage $\tilde{E}_\mathrm{s}$ is leading the receiving end voltage $\tilde{E}_\mathrm{r}$. This angle is also known as load or transmission angle and represents the angular separation between the machines of two areas. Assuming $\tilde{E}_\mathrm{r}$ as reference phasor, the sending end phasor can be also expressed with:

$$\tilde{E}_\mathrm{s} = \hat{E}_\mathrm{s}\cdot e^{\mathrm{j}\delta} = \hat{E}_\mathrm{s}\left(\cos\delta + \mathrm{j}\sin\delta\right) \ . \tag{3.51}$$

Expressing the receiving end current phasor in (3.50) by the active and reactive power and the receiving end voltage leads to:

$$\tilde{E}_\mathrm{s} = \tilde{E}_\mathrm{r}\cos\theta + \mathrm{j}Z_\mathrm{c}\sin\theta\frac{P_\mathrm{r} - \mathrm{j}Q_\mathrm{r}}{\tilde{E}_\mathrm{r}^*} \ , \tag{3.52}$$

where $\tilde{E}_\mathrm{r}^*$ is the complex-conjugated voltage phasor. By equating the real and imaginary parts of (3.51) and (3.52) it can be obtained:

$$\hat{E}_\mathrm{s}\cos\delta = \hat{E}_\mathrm{r}\cos\theta + Z_\mathrm{c}\sin\theta\frac{Q_\mathrm{r}}{\hat{E}_\mathrm{r}} \tag{3.53}$$

$$\hat{E}_\mathrm{s}\sin\delta = Z_\mathrm{c}\sin\theta\frac{P_\mathrm{r}}{\hat{E}_\mathrm{r}} \ . \tag{3.54}$$

Rearranging (3.54) results in the active power expression

$$P_\mathrm{r} = \frac{\hat{E}_\mathrm{s}\hat{E}_\mathrm{r}}{Z_\mathrm{c}\sin\theta}\sin\delta \ . \tag{3.55}$$

For short lines, it can be assumed $\sin\theta = \theta$ and thus it follows

$$Z_\mathrm{c}\sin\theta = Z_\mathrm{c}\theta = Z_\mathrm{c}\beta x = \sqrt{\frac{l_\mathrm{line}}{c_\mathrm{line}}}\cdot\omega\cdot\sqrt{l_\mathrm{line}c_\mathrm{line}}\cdot x = \omega l_\mathrm{line}\cdot x = X_\mathrm{ac} \ , \tag{3.56}$$

with l_line and c_line being the equivalent line parameters per unit length of the frequency dependent line model. Thus, in general the power transmission across a transmission line can be expressed with

$$P_\mathrm{r} = \frac{\hat{E}_\mathrm{s}\hat{E}_\mathrm{r}}{X_\mathrm{ac}}\sin\delta \ , \tag{3.57}$$

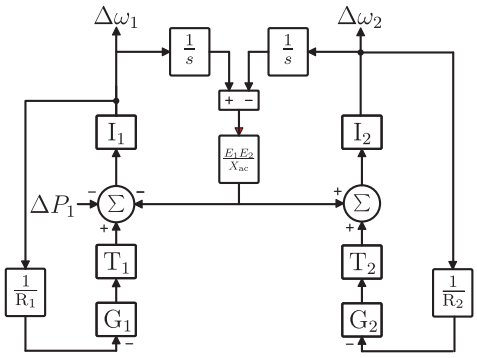


Fig. 3.22: Two-area system scheme with HVac interconnection.

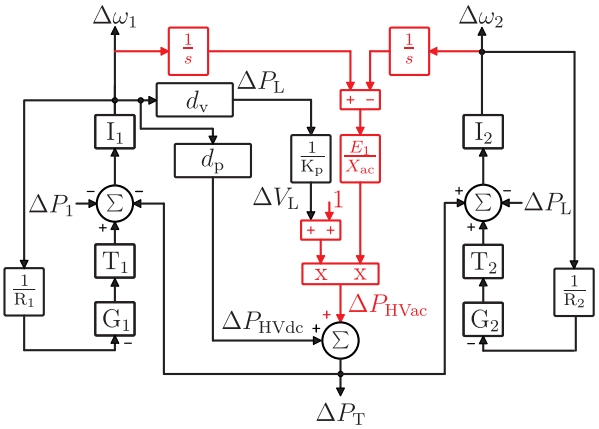


Fig. 3.23: Two-area system scheme with single HVdc interconnection (black), and parallel, hybrid HVdc-HVac interconnection (red) and PFR-VDL.

Table 3.2: Parameters of two-area grid.

R	T_G	F_{HP}	T_{RH}	T_{CH}	F_{LP}
0.05	0.2 s	0.3	7 s	0.3 s	0.7
M	D	K_p	E_1	X_{ac}	
13 s	1	1.8	1	0.022	

and assuming small angular separation between the two areas' machines $\sin\delta = \delta$

$$P_r = \frac{\hat{E}_s \hat{E}_r}{X_{ac}} \delta \,, \tag{3.58}$$

Combining two areas with their representation given by Fig. 3.21 with the ac transmission line model obtained in (3.58), leads to the overall system scheme shown in Fig. 3.22.

State-space model In the following, instead of the original 2 HVac tie lines, the two ac areas are interconnected with the HVdc cases under investigation: asynchronous HVdc interconnector (black) and embedded parallel HVdc-HVac lines (red) as in Fig. 3.23, in which

$\hat{E}_1$ is the amplitude of the voltage phasor at the sending end and it is assumed for the receiving end voltage $\hat{E}_2 = 1$ with an optional variation introduced by the HVdc control of voltage dependent loads. The two areas system parameters are listed in Table 3.2.

The dynamics of fast transient HVdc power electronics part and inner control circuits have time constants much smaller than the mechanical time constants relevant for the frequency analysis in the power system [18]. Hence, it is fair to assume the HVdc power control ideal, which results in simplified representation of the HVdc system only respecting its outer loop frequency power droop gain d_p. A similar assumption is valid for the dynamics of the control of voltage dependent loads, which are well outside the bandwidth of frequency control studies [74]. Thus, a linear relationship between frequency and load voltage can be assumed, which is added by the control gain of voltage dependent loads d_v and load voltage sensitivity K_p additionally in this scheme.

In order to account for different grid connection and control schemes in the theoretical analysis of the system frequency response to a power variation ΔP_1 (input of the system), a state space model of the test system in Fig. 3.23 has been developed.

Recapitulating the transfer function of each x-area system:

$$I_\mathrm{x}(s) = \frac{1}{M_\mathrm{x} s + D_\mathrm{x}} \tag{3.59}$$

$$G_\mathrm{x}(s) = \frac{1}{1 + sT_\mathrm{G,x}} \tag{3.60}$$

$$T_\mathrm{x}(s) = \frac{1 + sF_\mathrm{HP,x}T_\mathrm{RH,x}}{(1 + sT_\mathrm{CH,x})(1 + sT_\mathrm{RH,x})} \quad , \tag{3.61}$$

where $I_\mathrm{x}(s)$ represents the rotor inertia and load damping, $G_\mathrm{x}(s)$ the governor and $T_\mathrm{x}(s)$ the turbine transfer functions.

The state-space model of the overall scheme results to be (3.62):

$$A = \begin{bmatrix}
-\frac{1}{T_{\mathrm{G},1}} & 0 & -\frac{1}{M_1 R_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{T_{\mathrm{G},2}} & 0 & -\frac{1}{M_2 R_2} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\frac{d_\mathrm{p}+D_1}{M_1} & 0 & -\frac{1}{X_\mathrm{ac}} & \frac{1}{X_\mathrm{ac}} & \frac{F_{\mathrm{HP},1}}{T_{\mathrm{CH},1}} & \frac{1}{T_{\mathrm{CH},1}T_{\mathrm{RH},1}} & 0 & 0 \\
0 & 0 & \frac{d_\mathrm{p}-d_\mathrm{v}}{M_1} & -\frac{D_2}{M_2} & \frac{1}{X_\mathrm{ac}} & -\frac{1}{X_\mathrm{ac}} & 0 & 0 & \frac{F_{\mathrm{HP},2}}{T_{\mathrm{CH},2}} & \frac{1}{T_{\mathrm{CH},2}T_{\mathrm{RH},2}} \\
0 & 0 & \frac{1}{M_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{M_2} & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{T_{\mathrm{G},1}} & 0 & 0 & 0 & 0 & 0 & -\frac{T_{\mathrm{CH},1}+T_{\mathrm{RH},1}}{T_{\mathrm{CH},1}T_{\mathrm{RH},1}} & -\frac{1}{T_{\mathrm{CH},1}T_{\mathrm{RH},1}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & \frac{1}{T_{\mathrm{G},2}} & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{T_{\mathrm{CH},2}+T_{\mathrm{RH},2}}{T_{\mathrm{CH},2}T_{\mathrm{RH},2}} & -\frac{1}{T_{\mathrm{CH},2}T_{\mathrm{RH},2}} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0
\end{bmatrix} \tag{3.62}$$

$$B = \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \qquad C = \begin{bmatrix} 0 & 0 & \frac{1}{M_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{M_2} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \qquad D = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

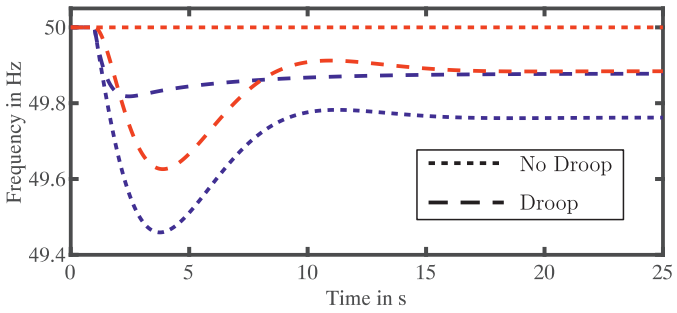


Fig. 3.24: Case I: Analytical calculation of frequency variation in Area 1 (blue) and Area 2 (red) w/ ('Droop') and w/o ('No Droop') HVdc primary frequency regulation for 10% active power load step in Area 1.

The dynamic state vector and the output vector are composed respectively of:

$$x = \left[g1 \;\; g2 \;\; i_1 \;\; i_2 \;\; \Theta_1 \;\; \Theta_2 \;\; \frac{d\tau_1}{dt} \;\; \tau_1 \;\; \frac{d\tau_2}{dt} \;\; \tau_2 \right]^T \tag{3.63}$$

$$y = \left[\Delta\omega_1 \;\; \Delta\omega_2 \right]^T \quad , \tag{3.64}$$

with $\Delta\omega_x$ being the frequency variation induced by load/generation mismatch, Θ_x the rotational angle and g_x, i_x and τ_x the internal dynamic states of the governor, rotor inertia and turbine of the respective area x.

Case I: Asynchronous connection with single HVdc interconnection The first study case is an asynchronous HVdc interconnector (depicted in black in (3.62)). After $t = 1\,\mathrm{s}$, a disturbance is created in Area 1 by applying an active power load step of $\Delta P_1 = 10\%$. With the conventional control (e.g. master-slave), the HVdc system works at constant power mode to keep the exchanged power between the two ac systems constant at its contracted value irrespective of the disturbance (marked with 'No Droop' in Fig. 3.24). In contrast, as Fig. 3.24 shows, the implementation of primary frequency regulation control by using a frequency-power-droop characteristic, allows the HVdc system to react on the detected frequency disturbance and to change its power request accordingly (marked with Droop). In constant power mode, the HVdc decouples the two ac areas and does not participate in the frequency regulation. The power mismatch in Area 1 leads to a large frequency drop below 49.5 Hz, while the Area 2 is unaffected in this case. On the contrary, implementing a frequency-power droop curve (proportional gain $d_\mathrm{p} = 20$) enables the HVdc system to modify its power demand proportionally with the frequency variation, which limits the frequency nadir to 49.8 Hz. However, as can be noticed from Fig. 3.24, increasing the transmitted power of the HVdc system as primary frequency regulation measure causes a temporary power imbalance and frequency variation of up to 49.6 Hz in Area 2, which is a critical drawback of the droop control action.

As solution to the above mentioned problem, the primary frequency regulation through con-

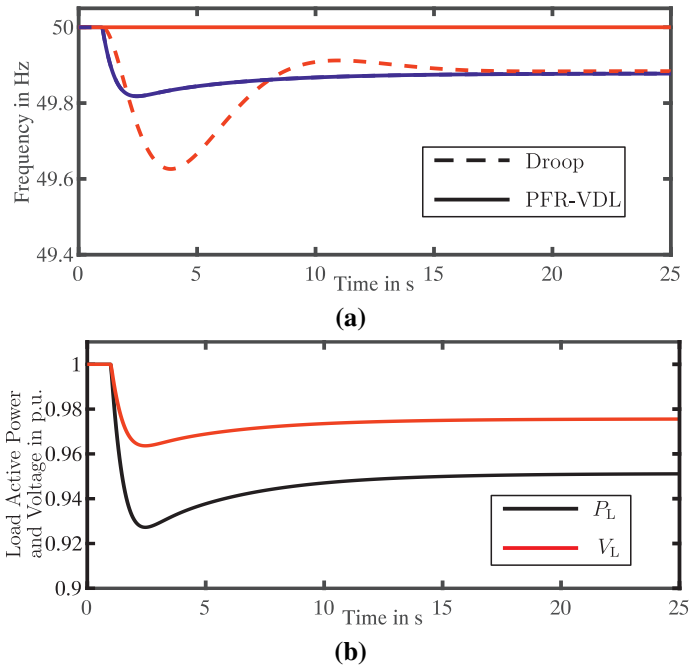


Fig. 3.25: Analytical calculation of (a) frequency variation in Area 1 (blue) and Area 2 (red) and (b) load active power and voltage variation with droop frequency regulation and with HVdc PFR-VDL in HVdc interconnector (Case I) for 10% active power load step in Area 1.

trol of voltage dependent loads as described in Subsection 3.2.1 can be additionally implemented in the HVdc terminal controller. The HVdc system can shape the voltage at the loads' point of coupling with the power system and consequently vary the active power consumption in order to partially balance the power variation request coming from the HVdc PFR. It is obvious that by extracting the same amount of power from the loads in Area 2 as requested by the HVdc PFR in Area 1, the HVdc terminal power can be completely balanced. Since the spinning reserve burden in this case is shared between the local generators and the nearby voltage dependent loads, additional operational reserve is raised and the frequency regulation service is made independent from the network inertia. As result, the frequency in Area 2 remains unchanged during the whole transient window (Fig. 3.25(a)). In order to guarantee a correct variation of load power consumption (see Fig. 3.25(b)), the load active power to voltage sensitivity K_p is estimated beforehand and the load voltage is changed accordingly (see Fig. 3.25(b)). This is vital to limit the load voltage drop (here to only 4 %), which gives high operational margin of the PFR-VDL application.

Case II Embedded HVdc forming a hybrid parallel HVdc-HVac interconnection As second use case, an embedded HVdc forming a hybrid parallel HVdc-HVac interconnection is considered. The additional equations to describe this implementation scheme are depicted in red in (3.62).

In the embedded scenario, the two grid frequencies are not independent due to the synchronous coupling by the parallel ac line through E_1/X_{ac}. Hence, a simple power transfer

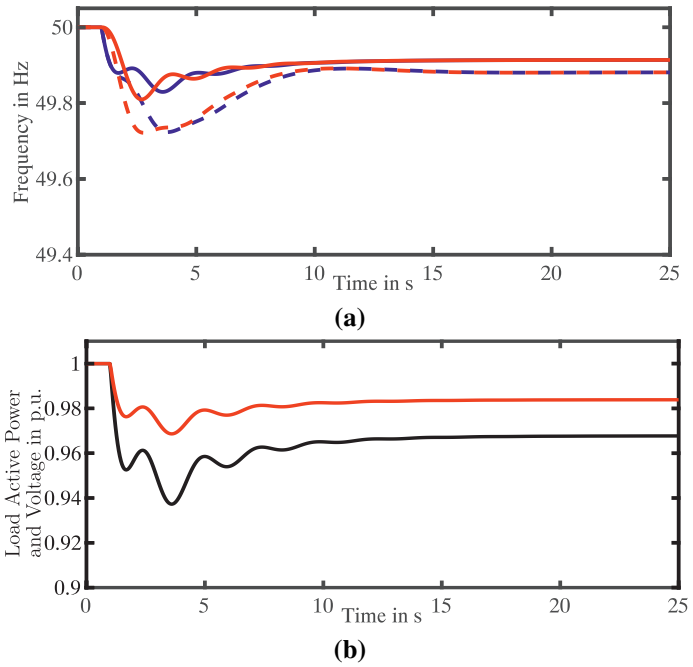


Fig. 3.26: Analytical calculation of (a) frequency variation in Area 1 (blue) and Area 2 (red) and (b) load active power and voltage variation with droop frequency regulation and with HVdc PFR-VDL in parallel, hybrid HVdc-HVac (Case II) for 10% active power load step in Area 1.

in droop mode has only limited impact on the frequency in both areas, which is dropping to 280 mHz. As can be concluded from Fig. 3.26(a) and Fig. 3.26(b) the PFR-VDL instead is effective also in embedded HVdc keeping the frequency oscillation in both areas above 180 mHz. In contrast to asynchronous HVdc interconnectors, not only the HVdc power, but the overall HVdc and HVac contribution affects the frequency in both areas.

In Fig. 3.27 the effect of increasing share of VDL control action d_v is analyzed. From the trajectory of the poles of the transfer function from active power load step ΔP_l to frequency variation $\Delta\omega_l$ three effects can be observed for high d_v: 1) a pole movement toward the imaginary axis, corresponding to a marginally reduced system stability, 2) a pole movement away from the real axis, indicating a reduction in system damping at higher frequencies (around 0.5Hz), and 3) a pole movement toward the real axis, with an increase of the damping at lower frequencies (around 0.1Hz). This results effectively in a reduced frequency nadir in both areas.

Discussion on the load sensitivity Effectively, the loads' power consumption variation by the PFR-VDL results in additional, virtual damping in the power system. The available spinning reserve from the loads for a given change in the voltage depends on the loads' sensitivity towards voltage variations K_p and as consequence, the maximum frequency deviation in Area 2 varies linearly with K_p. In Fig. 3.28, three different inertia cases have been considered: $H = 6.5$ s of conventional generators in Kundur benchmark; $H = 5$ s with mixed gen-

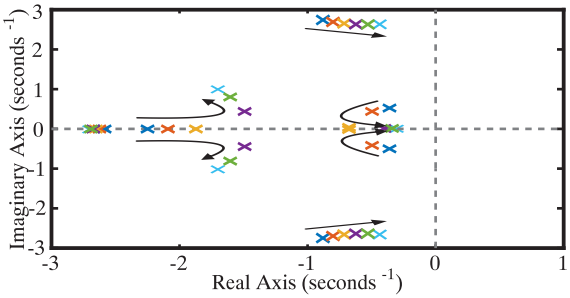


Fig. 3.27: Case II: Pole-Map of the closed-loop transfer function from active power load step ΔP_1 to Area 1 frequency variation $\Delta\omega_1$ with increasing VDL control gain $d_v = [0\%d_p \ldots 100\%d_p]$.

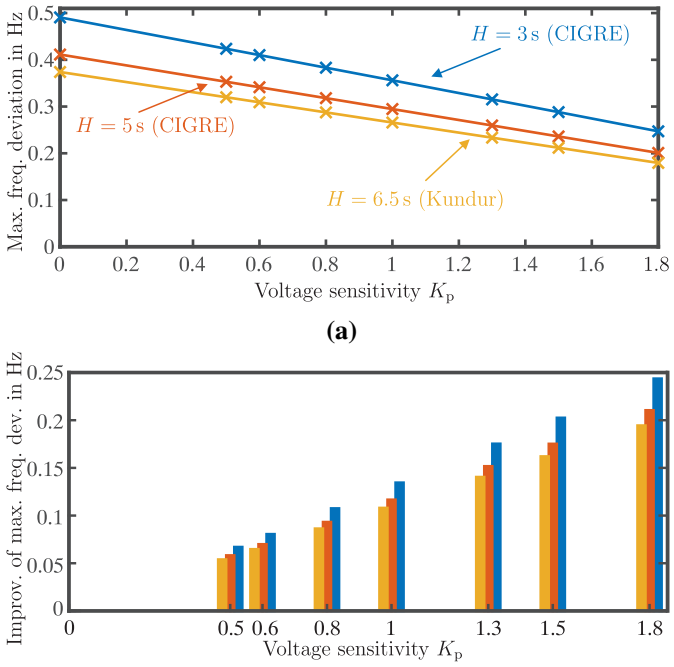


Fig. 3.28: Analytical calculation of (a) Maximum frequency deviation in Area 2 with PFR-VDL and (b) Improvement of PFR-VDL compared to Droop control with varying load voltage sensitivity and grid inertia for 10% active power load step in Area 1 and ± 0.02 p.u. voltage constraint.

eration (as reported in [135]) for North American and European HV transmission network benchmark; and $H = 3$ s during wind and PV plant production peaks [19]. A tight constraint on the grid voltage (e.g. ± 0.02 p.u. as requested by the current technical requirements for grid connection of high voltage direct current systems, [28]) limits the efficiency of the PFR-VDL in suppressing the undesired frequency deviation in supporting area 2. In Fig. 3.28(b) as best-case example, primary aluminum plants offer highest sensitivity of $K_p = 1.8$, which results in frequency oscillation damping by 180 mHz (high inertia) to 250 mHz (low inertia). However, as Fig. 3.28(b) shows, even for low-sensitivity loads (such as commercial loads in summer with a sensitivity of $K_p = 0.5$), improvements in frequency nadir of up to 50 mHz compared to conventional droop-based primary frequency control can be observed.

A future grid scenario with nearly 100% power electronics interfaced loads, may result in

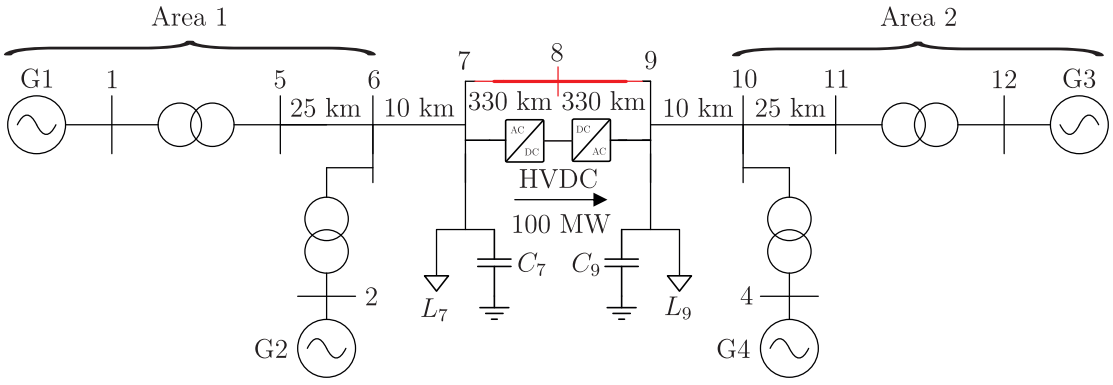


Fig. 3.29: Two-area four-generator system with single HVdc (black) and parallel, hybrid HVdc/HVac (red) interconnection.

close to zero load active power to voltage sensitivity. These constant-power loads, however, exhibit a negative incremental impedance [136], which reduces the system damping and results in instability or unacceptable oscillatory response [137]. Hence, modifications in the load dynamic characteristics (e.g. parallel resistive loads [137]) or changes in the load control are likely to be required, which results in average voltage sensitivity $K_\mathrm{p} > 0$ also in nearly 100% power electronics interfaced grids.

3.2.3. Simulations results: Simplified test system - HVdc interconnector

In the following, simulation results of EMTDC simulations in PSCAD environment are presented to verify the PFR-VDL improvements in HVdc-based frequency support. In order to simplify the results replication, the two-area benchmark transmission grid model established in [104] has been adopted, replacing the two original ac lines with single asynchronous HVdc interconnector (Case I) or with parallel, hybrid HVdc-HVac line (Case II) as shown in Fig. 3.29. The system's and HVdc's nominal parameters are listed in Table 3.3 and Table 3.4, respectively.

Each ac grid area consists of two machines, which include mechanical-hydraulic governor, steam turbine, synchronous generator and Ac2A-type exciter, and cable connections, which are represented with single PI-equivalent. The shunt capacitors of the cables are included in the dc capacitors of the converter equivalent model. The loads in this simulation are modeled as static exponential loads [104]. Following [74], a common modeling approach for power electronics in grid control studies is to use their average value model, in which the transient switching behavior of the converter is averaged within one switching interval. Consequently, both the inverter and rectifier of the HVdc system are modeled with controlled voltage source with series ac filter on the ac side. The source reference input is defined by the modulation waveform calculated by the HVdc controller. To represent the power flow from ac to dc, assuming a loss-less converter, a controlled current source with parallel dc capacitor is implemented in the dc side of the average value model.

Table 3.3: Initial set-points of generating units and loads of the two-area grid.

G1:	$P_1 = 530\,\text{MW}$	$Q_1 = 185\,\text{MVar}$	$E_{t1} = 1.03\angle 20.2°$
G2:	$P_2 = 530\,\text{MW}$	$Q_2 = 235\,\text{MVar}$	$E_{t2} = 1.01\angle 10.5°$
G3:	$P_3 = 550\,\text{MW}$	$Q_3 = 176\,\text{MVar}$	$E_{t3} = 1.03\angle -6.8°$
G4:	$P_4 = 560\,\text{MW}$	$Q_4 = 202\,\text{MVar}$	$E_{t4} = 1.01\angle 17.0°$
Bus 7:	$P_{L7} = 967\,\text{MW}$	$Q_{L7} = 100\,\text{MVar}$	$Q_{C7} = 200\,\text{MVar}$
Bus 9:	$P_{L9} = 1,167\,\text{MW}$	$Q_{L9} = 100\,\text{MVar}$	$Q_{C9} = 350\,\text{MVar}$

Table 3.4: Parameters of HVdc system.

Length	$V_{dc,nom}$	$V_{ac,nom}$	S_{nom}	P_{kundur}	P_{39bus}
660 km	400 kV	220 kV	500 MVA	100 MW	270 MW

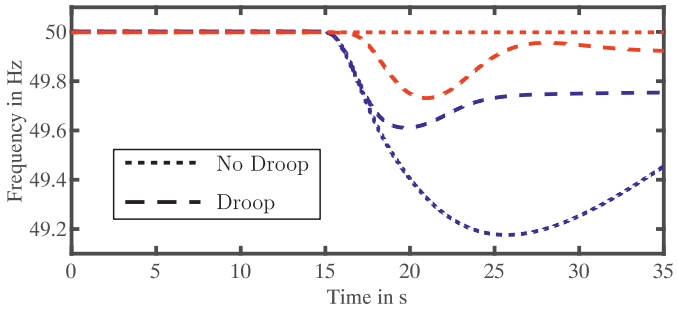


Fig. 3.30: Case I: Simplified test system: System frequency in Area 1 (blue) and Area 2 (red) w/ (Droop) and w/o (no Droop) HVdc frequency regulation.

In Fig. 3.30, at $t = 15$ s, a load step of 300 MW / 90 MVAr, which corresponds to around 8 % of the system rating (3600 MVA), is applied in area 1 to validate the PFR-VDL performance in HVdc systems. Two possible control modes of the HVdc system are considered: keeping the power transmission constant at the contracted value (indicated with 'No Droop' in Fig. 3.30); or frequency-power droop control mode (as depicted in Fig. 3.10) to linearly adapt its power output following the frequency disturbance (marked with 'Droop' in Fig. 3.30).

If the HVdc system operates in constant power mode, it does not participate in the frequency regulation and hence a large frequency deviation of up to 49.2 Hz occurs in the affected area 1. Instead, adapting the HVdc output power linearly with the frequency deviation, limits the negative frequency peak (i.e. frequency nadir) to 49.6 Hz as shown in Fig. 3.30. As consequence of the increased HVdc power transfer (Fig. 3.31(b)), the supporting area 2 experiences a temporary power imbalance and following frequency disturbance of 49.7 Hz, which forces the generators to ramp up to restore the power balance and stabilize the frequency.

Voltage-dependent loads can serve as additional power reserve in order to decrease the impact of the HVdc primary frequency regulation on the supporting area 2. The presented PFR-VDL algorithm is based on two steps. First, the load active power sensitivity to voltage is identified (at $t = 5$ s). Therefore, the HVdc terminal modifies the load voltage along

a pre-defined profile by controlled reactive power injection (Fig. 3.31(b)) and the change in the loads' power consumption is recorded. The load voltage and active power measurement data are sampled in the same place (e.g. at HV substation) and synchronized, which implies no communication delay. Once the sensitivity is known, as second step, the HVdc system applies the PFR-VDL control action, if the detected frequency deviation exceeds the dead-band of 100 mHz. The a-priori knowledge of load power to voltage sensitivity ensures that the load voltage variation, shown in Fig. 3.31(c), provokes a change in the load active power consumption matching exactly the required active power for the HVdc-based primary frequency regulation in area 1. Since the high voltage grid is mainly inductive, the voltage is sensitive to reactive power, which allows PFR-VDL control also with limited ampacity of the HVdc converter.

The effect of PFR-VDL action is shown in Fig. 3.31(a). The support on area 1 frequency is similar to the conventional droop control approach. However, the essential benefit of PFR-VDL application is that the frequency oscillation in supporting area 2 is reduced and the generators' primary frequency control is supported with high dynamics. Taking additional energy from nearby voltage dependent loads, reliefs the burden of the generators $G3$ and $G4$ to balance the energy deficit in area 2 as demonstrated with the generators' active power plots with and without load participation in Fig. 3.31(d). It is visible that in both transient and steady-state conditions the increase in the output power is smaller. Although only marginal improvements with respect to the pre-disturbance condition can be noticed in steady-state, the transient power overshoot (i.e., 3 %) can be avoided and a smoother governor control action can be applied.

In Fig. 3.32, the two area frequencies are depicted for the case of parallel, hybrid HVdc-HVac line assuming the same disturbance condition as before. In accordance with the findings of [15], it can be observed an inter-area mode in the two coupled frequencies, which was not triggered in the isolated, asynchronous interconnection. The PFR-VDL has an impact on the frequencies in two ways. First, the initial frequency drop is reduced by 80 mHz. Second, the post-disturbance inter-area oscillations are damped and steady-state conditions are reached earlier.

It can be argued that the proposed PFR-VDL approach can be only applied to voltage dependent loads in the proximity of the HVdc terminal. In the following, the PFR-VDL performance depending on the electrical distance between the load and the PFR-VDL control point is analyzed. Therefore, additional transmission lines of 0 km, 25 km and 50 km are introduced at the load bus in the benchmark simulation model. In order to get a fair comparison, the steady-state voltage and frequency condition at the load point is equalized for the different transmission line cases by adapting the generators initial set-points and the capacitor value at bus 9 of the Kundur grid. First, it can be noticed from Fig. 3.33 that the HVdc active power transmission and area 1 grid frequency are unchanged in all cases, indicating

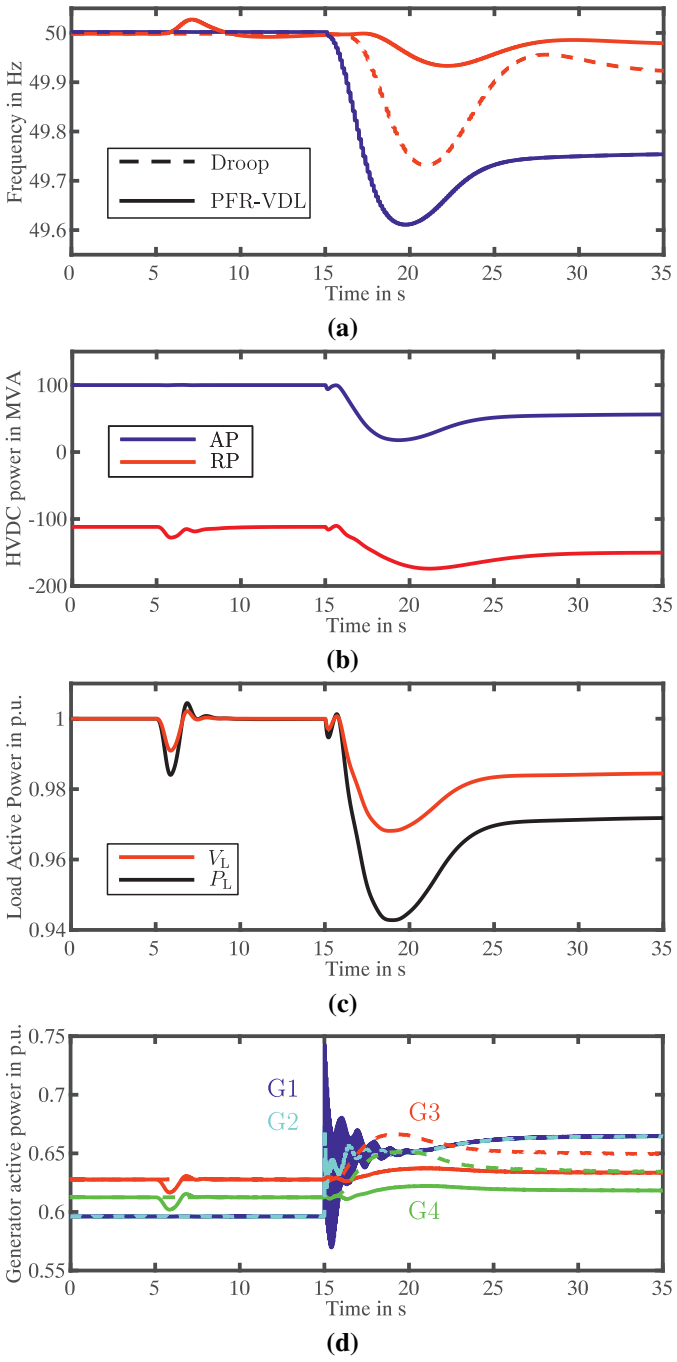


Fig. 3.31: Simulation results of PFR-VDL application in HVdc interconnector (Case 1) in the simplified test system: (a) Grid frequency in Area 1 (blue) and Area 2 (red), (b) HVdc active and reactive power, (c) Load active power and voltage and (d) Generator active power.

that the same primary frequency support can be provided to the affected area 1. However, two differences can be seen, if the line length changes. To compensate for the voltage drop across the transmission line, a small increase in the reactive power needed to influence the voltage amplitude can be observed. Moreover, the frequency nadir is slightly improved with longer lines. The reason can be found in higher losses in longer lines that decrease for a reduced load consumption. Hence, the total power mismatch to be compensated by the generators is reduced compared to the case with no transmission line.

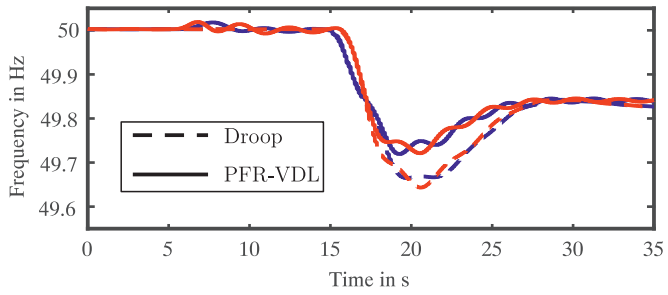


Fig. 3.32: Case II: Simplified test system: System frequency in Area 1 (blue) and Area 2 (red) with and without HVdc PFR-VDL.

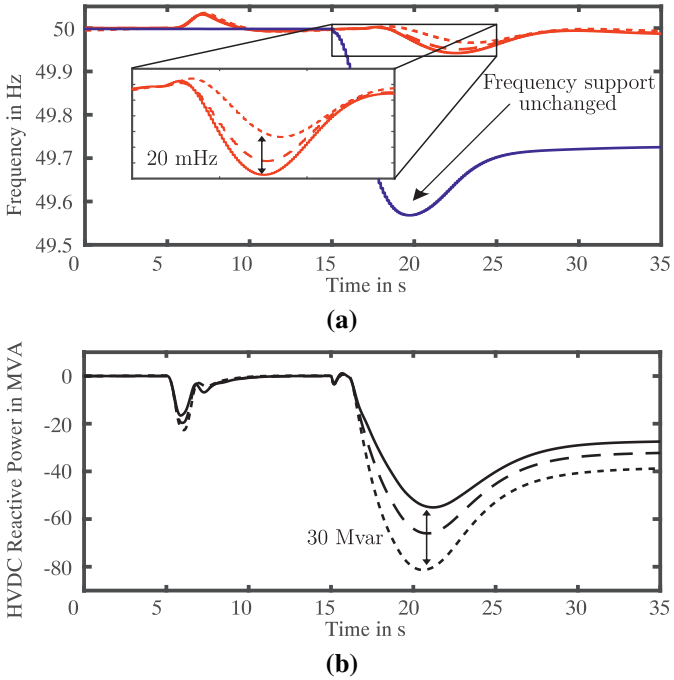


Fig. 3.33: Electrical distance variation between HVdc terminal and load: (a) Grid frequency in Area 1 (blue) and Area 2 (red) and (b) HVdc reactive power variation with 0km (solid), 25km (dashed) and 50km (dotted) transmission line.

3.2.4. Simulations Results: Large interconnected system - IEEE 39 bus system

The following section aims to validate the PFR-VDL application in embedded HVdc in a large interconnected system. Simulations results in modified IEEE 39-bus network [138] are carried out. As shown in Fig. 3.34, the HVdc replaces the ac line between bus 27 (terminal 1) and bus 26 (terminal 2) with identical active power flow of -270.4 MW. While the generators and HVdc system use the same type of modeling as in the simplified Kundur benchmark, the transmission lines in this case are represented with the Bergeron-model.

At $t = 35$ s a disturbance is created in the network by disconnecting the bus 39 from the main system, including the generator G_1, the connected load and the lines $1-39$ and $9-39$, which results in a grid-wide over-frequency event. The PFR-VDL application in embedded HVdc system is analyzed for two different study cases. First, in Fig. 3.35, it is assumed that

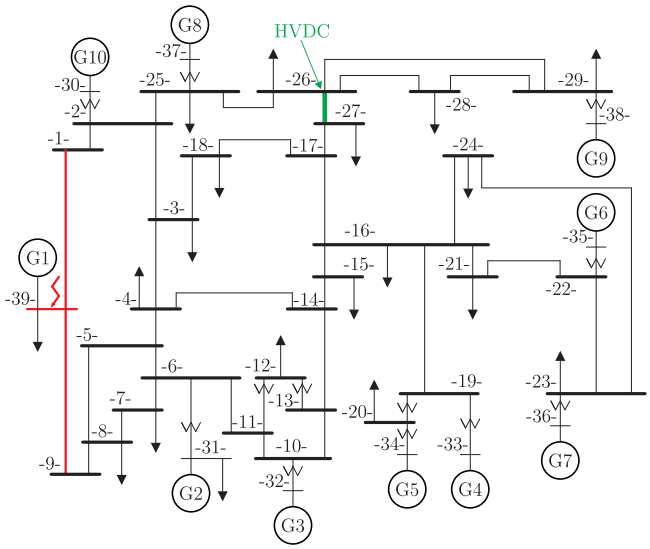


Fig. 3.34: Modified IEEE 39 bus system with HVdc system replacing the ac line between bus 27 (terminal 1) and 26 (terminal 2).

the system is dominated by conventional generators and hence offers the comparably high nominal inertia of $H = 6$ s. The second case (Fig. 3.36) considers higher penetration of RES (wind and PV) and consequently reduced aggregated inertia of $H = 3$ s.

By definition, in embedded HVdc systems, the two connection points residue in the same synchronous area and hence their frequencies are strongly coupled [139]. Consequently, a change in the active power transfer is ineffective to damp the frequency oscillation and an additional source of energy is required. Thus, in the following only the HVdc-based control of voltage dependent loads is analyzed.

Without the control of voltage dependent loads (indicated with no support in Fig. 3.35 and Fig. 3.36) the grid frequency in Fig. 3.35(a) increases up to 50.11 Hz in the case of $H = 6$ s, due to the sudden load/generation active power mismatch. If the control of voltage dependent loads is activated, the HVdc injects reactive power (Fig. 3.35(b)) to vary the voltage at the loads point of common coupling (PCC) (Fig. 3.35(c)). As consequence of the voltage variation, in Fig. 3.35(c) results an observable increase in the active power consumption of the controlled load at bus 26, which raises additional operational reserve for the frequency support. The PFR-VDL action does not only reduce the drop in frequency by 30 mHz, corresponding to a 30 % frequency nadir improvement with respect to the case without PFR-VDL, but, as theoretically analyzed in Subsection 3.2.2, also increases the system damping, leading to a reduced post-disturbance oscillation in the frequency (Fig. 3.35(a)).

Since the voltage is a local parameter, the HVdc system can directly influence only the voltage at its PCC through the reactive power injection. Assuming multiple voltage dependent loads connected in the proximity of the HVdc terminal, the change in voltage will not only control a single particular load, but will also partially affect the active power consumption of other voltage dependent loads at connected buses (28 and 29, Fig. 3.35(c)). In contrast to

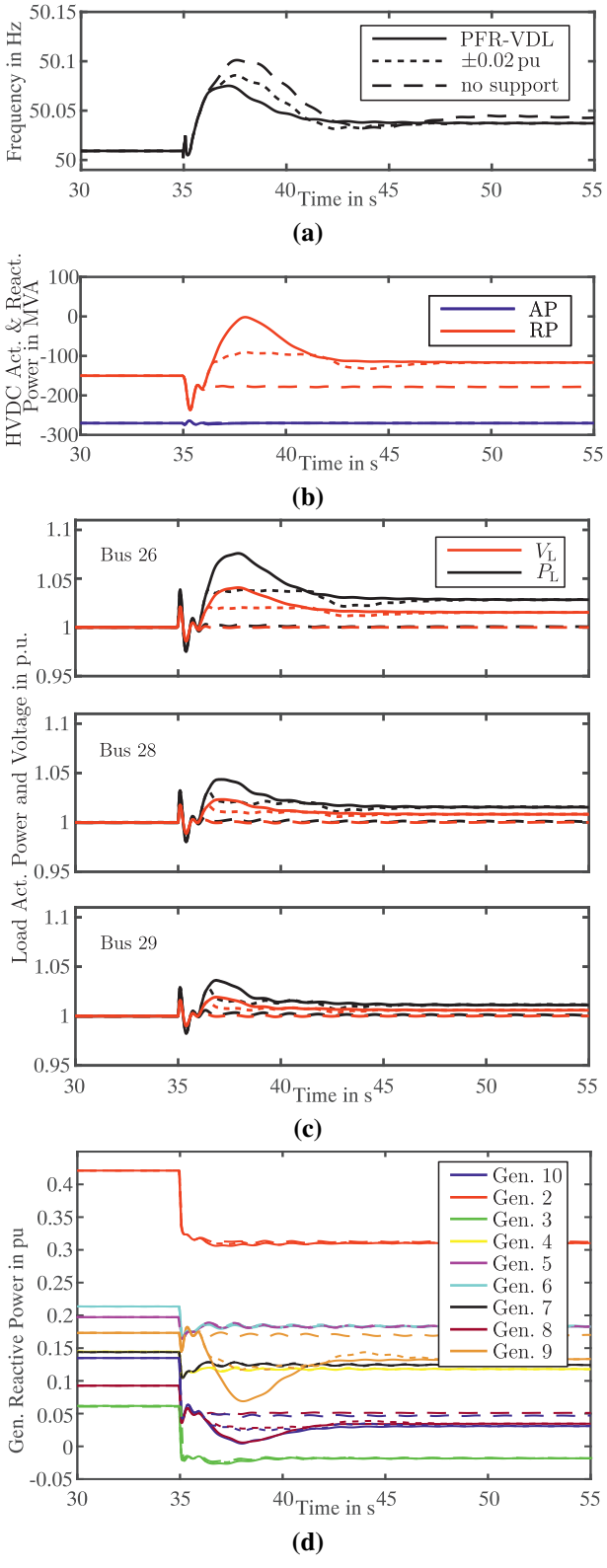


Fig. 3.35: Frequency event in IEEE 39-bus system in high inertia condition ($H = 6$ s) w/o ('no support') and w/ PFR-VDL with $0.9 - 1.118$ pu ('PFR-VDL') and ± 0.02 pu voltage limitation ('± 0.02 pu'):(a) Grid frequency, (b) HVdc active and reactive power, (c) Load active power and voltage and (d) Generator reactive power.

[113], in which the additionally requested energy for frequency support is obtained through firm load shedding, the proposed algorithm only requires soft load reduction, making the

participation of multiple voltage dependent loads actually beneficial for PFR performance. Moreover, the PFR-VDL control is a short-term action, activated only for few seconds to stabilize the frequency after the disturbance. As soon as the frequency resettles, the automatic voltage regulation (AVR) of the generators restores the voltage by reactive power injection as depicted in Fig. 3.35(d).

The HVdc grid voltage controller in the terminal 2 is active in all cases independent of the PFR-VDL action to support the grid voltage. Since, the grid voltage in the entire system experiences a sudden change following the frequency disturbance, in the first seconds after the fault, small HVdc reactive power injection can be noticed also with deactivated PFR-VDL.

A high renewable energy penetration reduces the system inertia and hence causes faster and larger frequency deviation after the disconnection of bus 39 (see Fig. 3.36(a)). Nevertheless, the HVdc PFR-VDL is effective in reducing the frequency nadir from original 50.14 Hz to 50.10 Hz, which corresponds to $\approx 30\,\%$ reduction also in low inertia condition. However, in absolute values the HVdc system must compensate a larger imbalance requiring higher grid voltage variation, i.e. 5.5 % in Fig. 3.36(c) compared to 4 % in the high inertia case in Fig. 3.35(c)) and hence higher reactive power injection (i.e. plus 50 MVAr in Fig. 3.36(b)).

The maximum-step change in voltage through reactive power injection is constrained by ± 0.02 pu as stated in the current technical requirements for grid connection of HVdc systems. This scenario is analyzed in Fig. 3.35 and Fig. 3.36 with dotted lines for the same two study cases, conventional high inertia grid and renewable generation dominated low inertia grid. Although a constraint on the permissible grid voltage variation will reduce the PFR-VDL influence on the frequency nadir, Fig. 3.35 and Fig. 3.36 demonstrate that still a positive damping effect on the frequency is obtained for both cases. If the inertia is low, the frequency oscillation is reduced by ≈ 30 mHz compared to 40 mHz in the unlimited case, and if the inertia is high ≈ 20 mHz compared to 30 mHz damping are achieved. Since lower amount of reactive power is injected by the HVdc, the generators reactive power response is released (see Fig. 3.35(d) and Fig. 3.36(d)).

3.3. Optimization of frequency support with multi-terminal HVdc systems

Multi-terminal HVdc systems connect multiple ac areas and allow for improved power flow control, which in turn provides multiple sources of energy and higher flexibility for both the primary frequency regulation and the inertia emulation.

In MTdc systems, the droop characteristic of the individual terminals can be tuned to optimally share the burden of frequency support among the terminals. Hence, in the following it

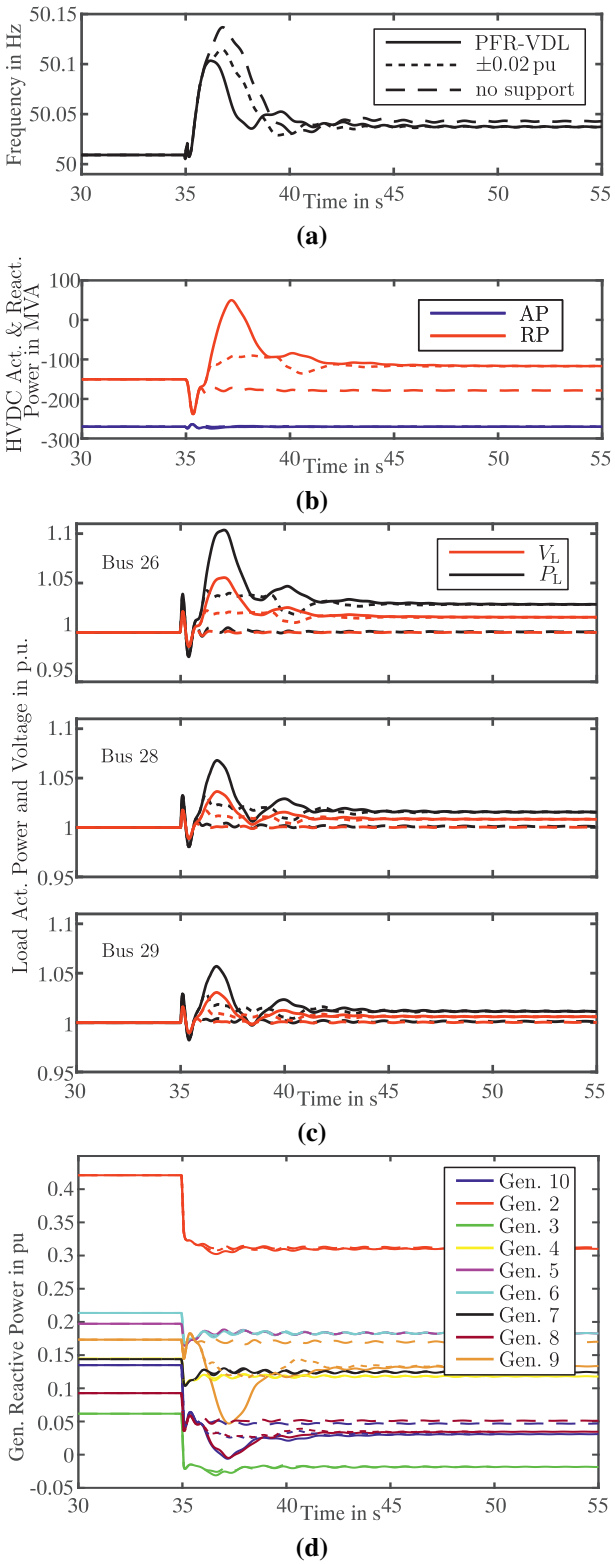


Fig. 3.36: Frequency event in IEEE 39-bus system in low inertia condition ($H = 3$ s) w/o ('no support') and w/ PFR-VDL with $0.9 - 1.118$ pu ('PFR-VDL') and ± 0.02 pu voltage limitation ('± 0.02 pu'):(a) Grid frequency, (b) HVdc active and reactive power, (c) Load active power and voltage and (d) Generator reactive power.

is evaluated, how the MTdc can optimally provide primary frequency regulation and inertia emulation with minimal impact on the frequency and voltage in connected areas by means

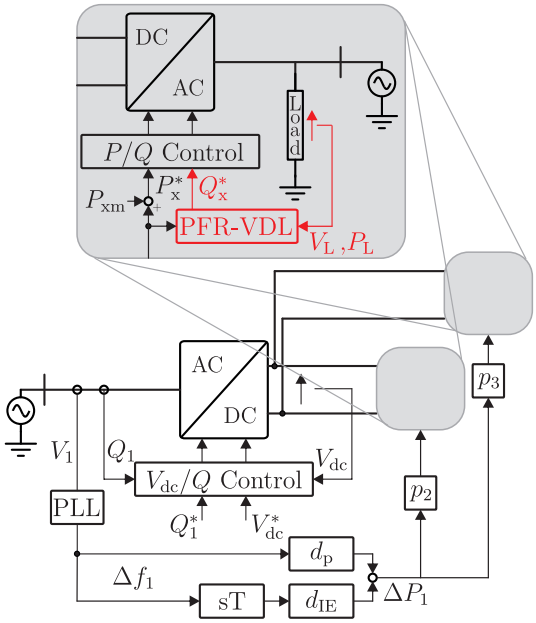


Fig. 3.37: MTdc master-slave control scheme with additional primary frequency regulation and inertia emulation controlling voltage dependent loads.

of adapting the droop coefficients.

In fact, it is proposed to optimally share the frequency support respecting the estimated load sensitivity in each connected area. This implies that terminals connected to loads with the highest sensitivity provide the highest share of frequency support. Consequently, the control margin for both upward and downward frequency support is increased and the voltage deviation in the supporting areas as well as the reactive power injection of the HVdc terminal are reduced without delimiting the frequency damping in the faulty area.

3.3.1. Analytical results of optimized frequency support in MTdc systems

In the following section, the analytical investigation of enhanced frequency support with MTdc systems is performed. It is assumed that the MTdc system is controlled in master-slave mode, hence one terminal - the master - controls the dc voltage and the other (in this case two) terminals - the slaves - control their active power exchange with the ac grid (more details in Subsection 2.4.2). Additionally, the slave terminals are equipped with droop-based primary frequency regulation and derivative term based inertia emulation as explained in Subsection 3.1 and shown in Fig. 3.37. In red is shown the control of voltage-dependent loads as additional operational reserve as explained in Subsection 3.2.1.

The analysis is carried out in an adapted model of the Kundur benchmark [104], extending it to a three-area, three-machine system with MTdc interconnection (Fig. 3.38). While by using simplified benchmark systems the results can be more easily replicated, this model maintains the necessary accuracy for frequency stability studies [74]. The detailed model

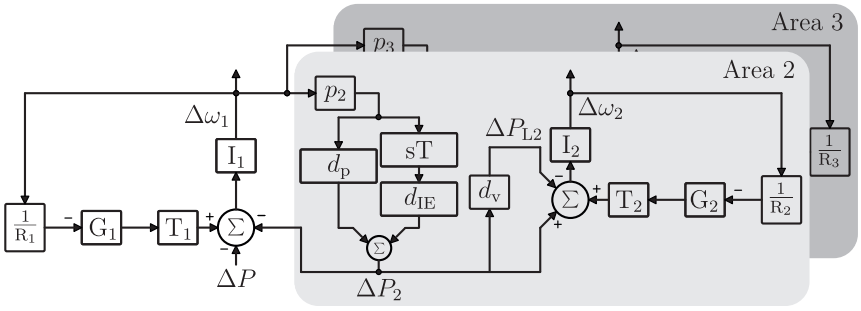


Fig. 3.38: Three-area three-generator system scheme with MTdc grid.

parameters are given in Table 3.2. For sake of simplicity, it is assumed that the two areas connected to the slave terminals show the same dynamics and damping and vary only in terms of their load power to voltage sensitivity. Area 2 contains low-sensitive loads (i.e. commercial loads in winter, $K_{p2} = 0.8$) and area 3 is assumed to include high-sensitive loads (industrial aluminum plants, $K_{p3} = 1.8$ [119]).

In the first study case, the improvements in frequency disturbance response of primary frequency regulation by MTdc compared to the case in which no support is given are analyzed with the assumption of equal power sharing between the two supporting terminals. The main objective of the analysis is the determination of power support share (also compared to cases where only one terminal is allowed to participate). Hence, it is assumed that the total amount of power provided by the (maximum two) supporting areas equals the power provision, which was assumed in the previous section by only one area.

The MTdc system is effective in limiting the frequency nadir in area 1 (from 49.4 Hz to 49.8 Hz) by applying the PFR control action. However, two challenges can be observed in Fig. 3.39(a). The initial RoCoF cannot be improved, since no inertia contribution is provided by the droop control and similar to the study cases before, the supporting areas suffer from large transient power mismatch and frequency deviation.

To tackle the first problem, the HVdc controllers' power reference is adapted proportionally (gain d_{IE}) to the derivative of the frequency variation, which emulates virtual inertia in the faulty system (for further details refer to Subsection 3.1). In Fig. 3.39(b), the emulated inertia H_{IE} is changed from 0 to 10 s, resulting in a RoCoF improvement of $0.15\frac{\text{Hz}}{\text{s}}$.

Although, this control action leads to noticeable improvements in the initial frequency response in area 1, a further deterioration of the frequency dip in supporting areas can be observed (dotted lines in Fig. 3.39(c)).

However, applying additionally the control of voltage dependent loads with the method established in Subsection 3.2.1 and represented with parameter d_v in Fig. 3.38, the power mismatch and consequently the frequency in the supporting areas can be balanced, while the same frequency regulation is achieved in the faulty area 1 (solid lines in Fig. 3.39(c)).

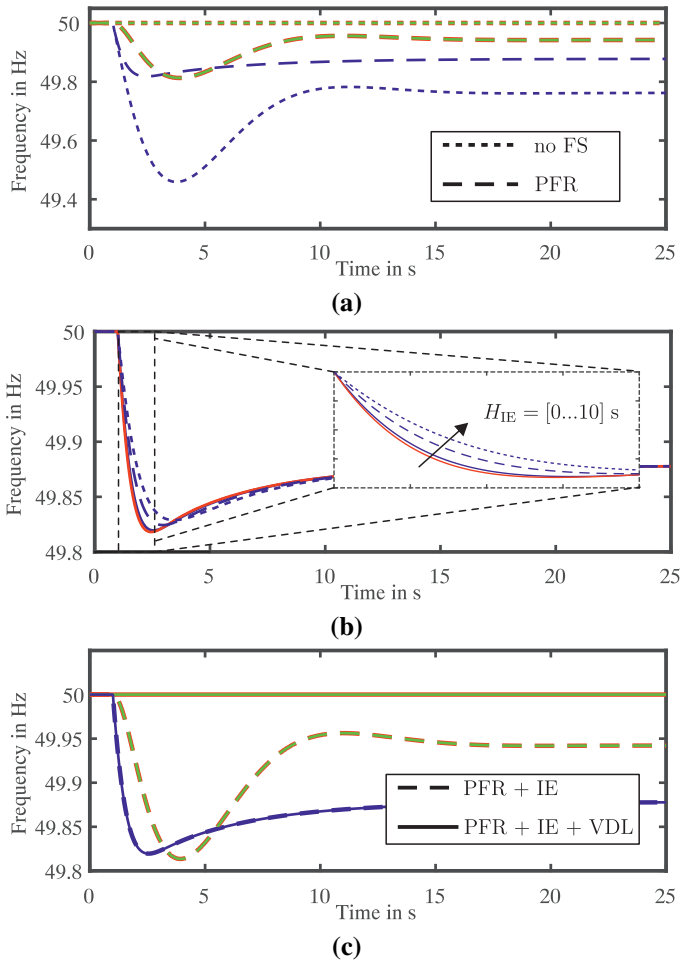


Fig. 3.39: Analytical results of grid frequency variation in the three areas 1 (blue), 2 (red) and 3 (green):(a) with and without MTdc primary frequency regulation (PFR), (b) with mtdc PFR and varying inertia emulation (IE), (c) PFR + IE with or without control of voltage dependent loads.

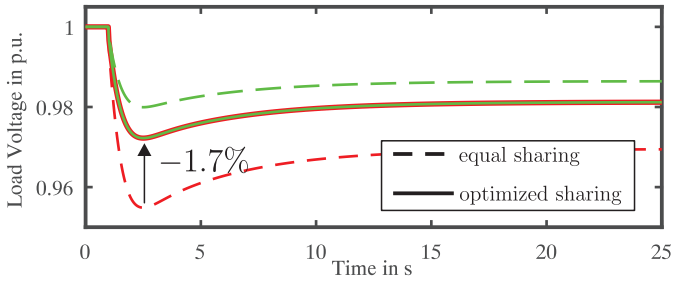


Fig. 3.40: Load voltage variation in the two supporting areas 2 (red) and 3 (green) with MTdc PFR-VDL and IE with and without optimal power sharing.

The optimization of the MTdc control providing frequency support has two main objectives. First, the minimum frequency deviation in supporting areas should be achieved (by using voltage-dependent loads) and second, being the focus of the following derivation, the voltage deviation in the two supporting areas originating from the load control action should be minimized. Obviously, the global minimum is obtained, if the grid voltage in both areas is varied by the exact same amount $\Delta V_{L2} = \Delta V_{L3}$. Hence, applying the control law (3.36) for

both areas results in

$$\frac{p_2 \cdot \Delta P_1 \cdot V_{02}}{P_{\mathrm{L}2} K_{p2}} = \frac{p_3 \cdot \Delta P_1 \cdot V_{03}}{P_{\mathrm{L}3} K_{p3}} \Rightarrow \frac{p_2}{p_3} = \frac{\frac{V_{03}}{V_{02}}}{\frac{P_{\mathrm{L}3}}{P_{\mathrm{L}2}} \cdot \frac{K_{p3}}{K_{p2}}} \ , \tag{3.65}$$

with p_2 and p_3 being the proportion of frequency support given by the areas 2 and 3, respectively. The basic optimization constraint is that full frequency support can be provided in area 1. Mathematically, this translates into $p_2 + p_3 = 1$. Thus, from (3.65) it follows

$$\frac{p_2}{p_3} = \frac{1 - p_3}{p_3} = \frac{\frac{V_{03}}{V_{02}}}{\frac{P_{\mathrm{L}3}}{P_{\mathrm{L}2}} \cdot \frac{K_{p3}}{K_{p2}}} \Rightarrow p_3 = \frac{1}{1 + \frac{\frac{V_{03}}{V_{02}}}{\frac{P_{\mathrm{L}3}}{P_{\mathrm{L}2}} \cdot \frac{K_{p3}}{K_{p2}}}} \ . \tag{3.66}$$

Assuming equal initial load active power and voltage, (3.66) simplifies to

$$p_3 = \frac{K_{p3}}{K_{p2} + K_{p3}} \tag{3.67}$$

and thus

$$p_2 = \frac{K_{p2}}{K_{p2} + K_{p3}} \ . \tag{3.68}$$

Fig. 3.40 depicts the effect of the optimal sharing. While in the case, the power share is kept equal, the low sensitive area experiences a voltage dip of more than 4 %, the optimal sharing results in an limitation by 1.7 % and hence overall minimized grid voltage deviation, which also reduces the needed reactive power injection of the HVdc station.

3.3.2. Simulation results of optimized frequency support in MTdc systems

In the following, PSCAD/EMTDC simulations in a multi-terminal three-area adaption of the benchmark grid established in [104] and shown in Fig. 3.41 are conducted to prove the effectiveness of the proposed optimization for MTdc primary frequency regulation and inertia emulation controlling nearby voltage dependent loads. The same modeling as explained in Subsection 3.2.3 is used and the system's parameters can be found in Table 3.3 and Table 3.4, assuming area 2 and area 3 being equal, except for the aggregated load active power to voltage sensitivity. It is supposed that area 2 comprises loads with low voltage sensitivity (e.g. commercial loads in winter, $K_{\mathrm{p2}} = 0.8$), while area 3 consists of high-sensitive loads, such as primary aluminum plants with $K_{\mathrm{p2}} = 1.8$, thus, in total, going in line with the average sensitivity in high-voltage grids as stated in Table 3.1.

The following control actions are studied:

- Case A: no MTdc frequency support

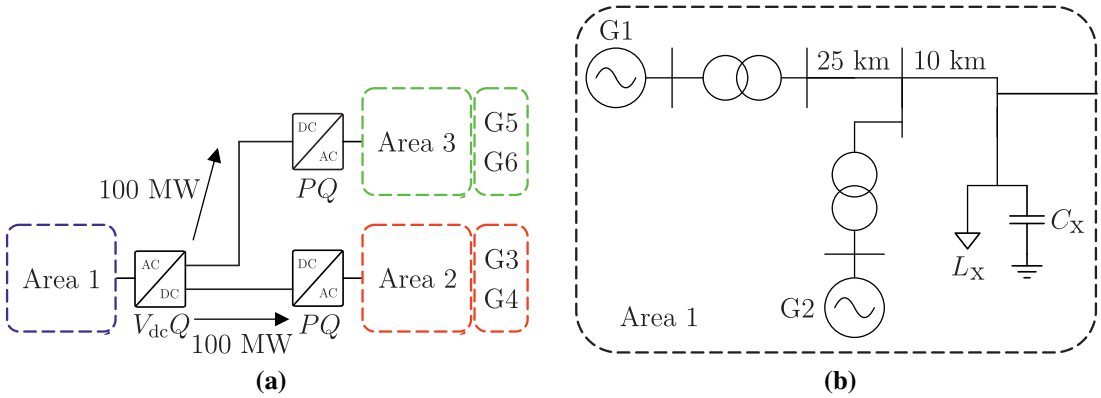


Fig. 3.41: Three-area six-generator system with MTdc grid:(a) System representation and (b) Representation of one area.

- Case B: MTdc PFR ($d_p = 100$), no IE
- Case C: MTdc PFR and IE ($H_{IE} = [1, 5, 10]$ s)
- Case D: MTdc PFR, IE and control of VDL (terminal 2, low load sensitivity $K_p = 0.8$)
- Case E: MTdc PFR, IE and control of VDL (terminal 3, high load sensitivity $K_p = 1.8$)
- Case F: MTdc PFR, IE and control of VDL equally shared among terminal 2 & 3
- Case G: MTdc PFR, IE and control of VDL optimally shared among terminal 2 & 3 depending on estimated load sensitivity

The system is disturbed by a 300 MW / 90 Mvar load step at the time $t = 15$ s, which corresponds to around 8% of the 3600 MVA system rated power. If the MTdc system continues to supply the same power as before the disturbance (Case A), the frequency in affected area 1 cannot be supported and hence drops to 49.3 Hz. Equipping the MTdc terminals with the primary frequency droop regulator (Case B) and varying the power flow linearly with the frequency deviation, supports the affected area damping and improves the frequency nadir by 300 mHz. It has to be noted that a dead-band of 100 mHz has been implemented, to prevent the MTdc system from acting under small and regular frequency variations. However, the droop control action cannot emulate virtual inertia in the grid and hence can only improve the frequency nadir but not the RoCoF. Moreover, as already stated in Subsection 3.2.2, the supporting areas 2 and 3 suffer from transient power mismatch and large frequency deviations of 130 mHz.

To emulate inertia, in the MTdc active power controllers an additional term proportional to the frequency gradient is included (Case C). As Fig. 3.43 demonstrates, the inertia in faulty area 1 can be increased virtually (additional inertia varied stepwise from 0 s to 10 s), which limits the RoCoF and also helps to further reduce the frequency nadir by up to 50 mHz.

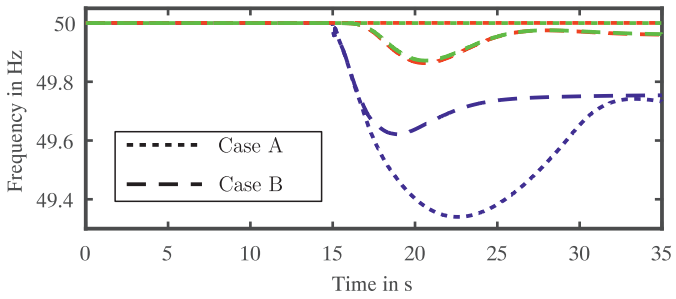


Fig. 3.42: System frequency in the three areas 1 (blue), 2 (red) and 3 (green) with and without MTdc primary frequency regulation.

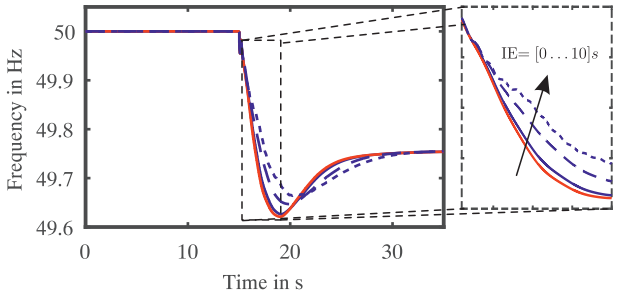


Fig. 3.43: System frequency in area 1 with emulated inertia $H_{\mathrm{IE}} = 0$ s (red), $H_{\mathrm{IE}} = 1$ s (solid blue), $H_{\mathrm{IE}} = 5$ s (dashed blue) and $H_{\mathrm{IE}} = 10$ s (dotted blue).

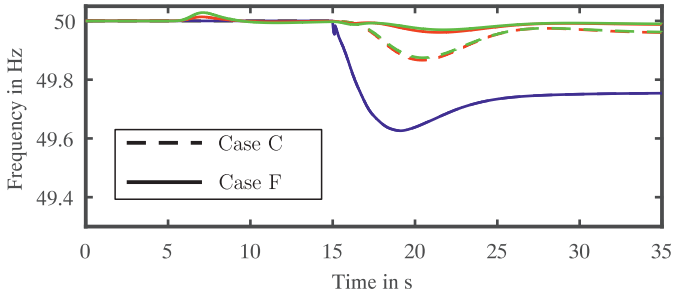


Fig. 3.44: System frequency in the three areas 1 (blue), 2 (red) and 3 (green) with MTdc frequency support (FS) and with or without control of voltage dependent loads (VDL).

The MTdc system can control the grid voltage at its terminals to shape the power consumption of nearby voltage dependent loads (e.g. industrial aluminum plants or primary substations). The control action involves two steps: First, the load active power to voltage sensitivity is estimated at $t = 5$ s. This knowledge guarantees a proper adjustment of the grid voltage to extract the exact required amount of power for the frequency support in the second step (Case F). What differs compared to conventional primary frequency regulation or inertia emulation (Case C), is the fact that the energy reserve is no longer given exclusively by the generators, but also by the nearby voltage dependent loads, which maintains the power balance in supporting areas and the frequency variation can be limited to < 50 mHz, while the same frequency support (PFR + IE) can be provided to area 1 (see Fig. 3.44). Moreover, a smoother governor control action can be applied, since the transient overshoot in the generators active power after the disturbance can be relieved by 1.5 % in both areas assuming equal machine rating (Fig. 3.45).

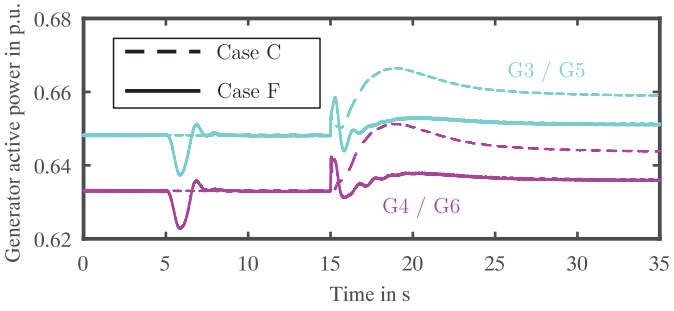


Fig. 3.45: Generators active power in the two supporting areas 2 and 3 with MTdc frequency support (FS) and with or without control of voltage dependent loads (VDL).

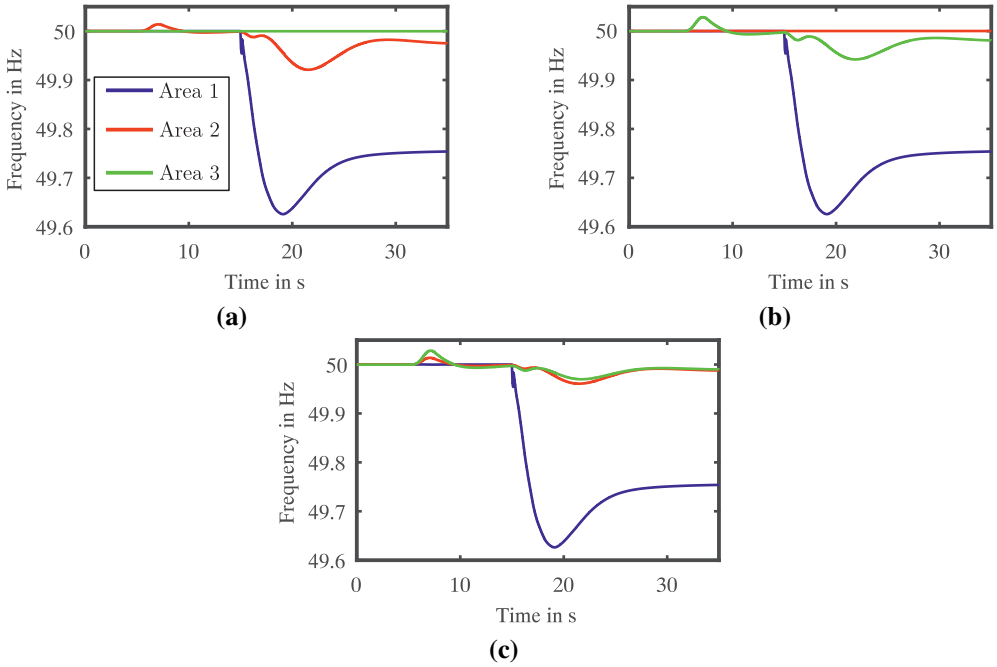


Fig. 3.46: System frequency in the three areas with FS-VDL:(a) Case D, (b) Case E and (c) Case F.

So far, the support is shared by the two terminals equally. However, MTdc systems offer the possibility to route the power flow and hence give additional degree of freedom for the frequency support. In Fig. 3.46, the frequency in the three areas is depicted, while area 1 is supported only from area 2 (Case D), area 3 (Case E) and equally from both areas (Case F). In all cases, 80 MW total active power is transmitted to area 1 (Fig. 3.47) to guarantee the same support in the affected area. Despite small changes, which are related to the losses in the ac grids, the average frequency disturbance is also equal.

However, a remarkable difference in the three cases exists in the required grid voltage change (Fig. 3.48) to create the load power consumption variation (Fig. 3.49) and hence in the HVdc reactive power injection to the grid (Fig. 3.50).

In cases D and E, it is assumed that only one area can participate in the frequency support, due to technical or economic constraints. It is obvious, that supplying the full power request from only the low-sensitive area, requires the biggest variation in the voltage of 6 %

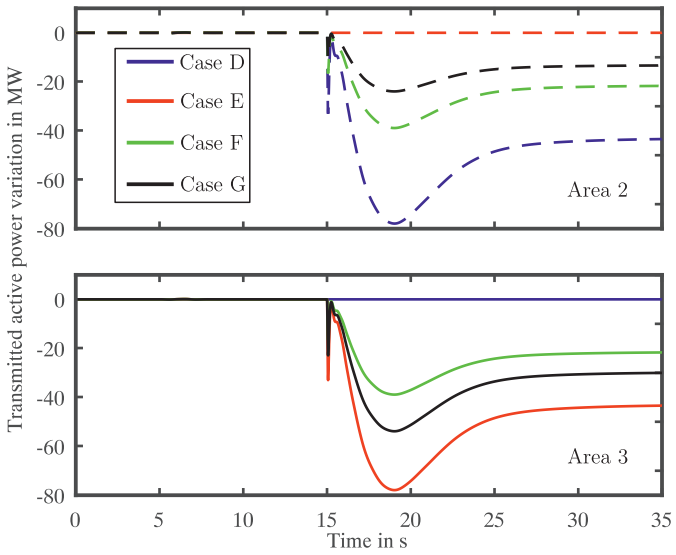


Fig. 3.47: MTdc active power variation with frequency support and control of voltage dependent loads (FS-VDL) in the two supporting terminals.

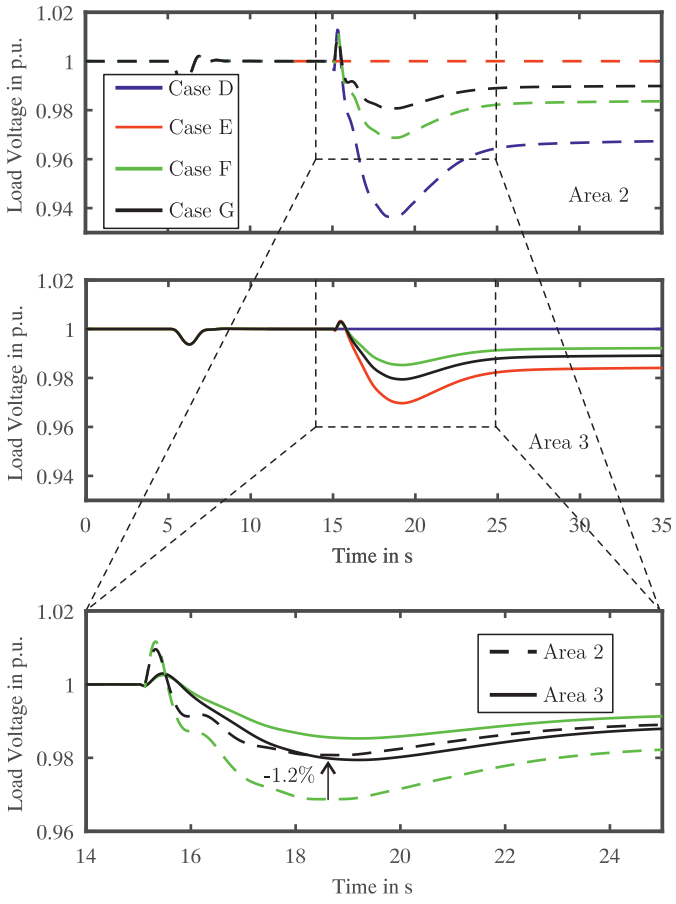


Fig. 3.48: Load voltage variation with FS-VDL in the two supporting areas and zoomed view of Cases F (green) and G (black).

and highest reactive power injection of 140 Mvar. On the contrary, high sensitive loads can provide the same amount of power with 3 % voltage variation and 60 Mvar reactive power injection. The second optimization goal, was to reduce the frequency deviation. In the aforementioned two cases, only the generators and loads of one area are used to compensate the

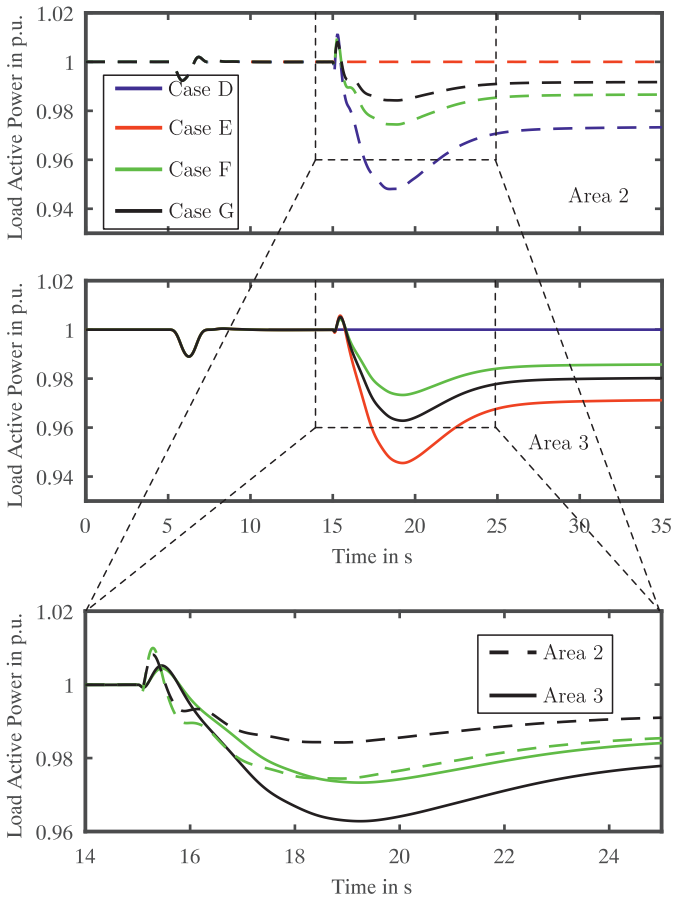


Fig. 3.49: Load active power variation with FS-VDL in the two supporting areas and zoomed view of Cases F (green) and G (black).

MTdc power request, which leads consequently to larger frequency oscillations in the supporting area also in the presence of load control (Fig. 3.46). Hence, it is favorable to share the frequency support among the areas, also because each individual load has to provide less power and hence the maximum grid voltage variation of each area will be kept smaller. Nevertheless, under the assumption of equal support sharing ($p_2 = p_3 = 0.5$), the low-sensitive loads still have to provide comparably high amount of active power and thus suffer from voltage variation of around 3 %, which leaves room for optimization. Moreover, the relatively large variation in the voltage requires unnecessary high reactive power injection.

As derived in Subsection 3.3.1, using the estimated value of load active power to voltage sensitivity, the frequency support can be optimally distributed among the supporting terminals (Case G). The goal is to achieve the same total active power reserve with the lowest overall grid voltage disturbance and lowest total amount of reactive power, such that compliance with local voltage constraints set by the grid operator and terminal converter ampacity limits can be guaranteed. If the support is shared with the ratio given by (3.67) and (3.68) (i.e. $p_2 = 0.3077$, $p_3 = 0.6923$), the maximum voltage variation that occurs in the supporting areas is limited by 1.2 % compared to the equal load power extraction as shown in Fig. 3.48. This results in reactive power saving of 20 Mvar, i.e. 25 % in comparison with

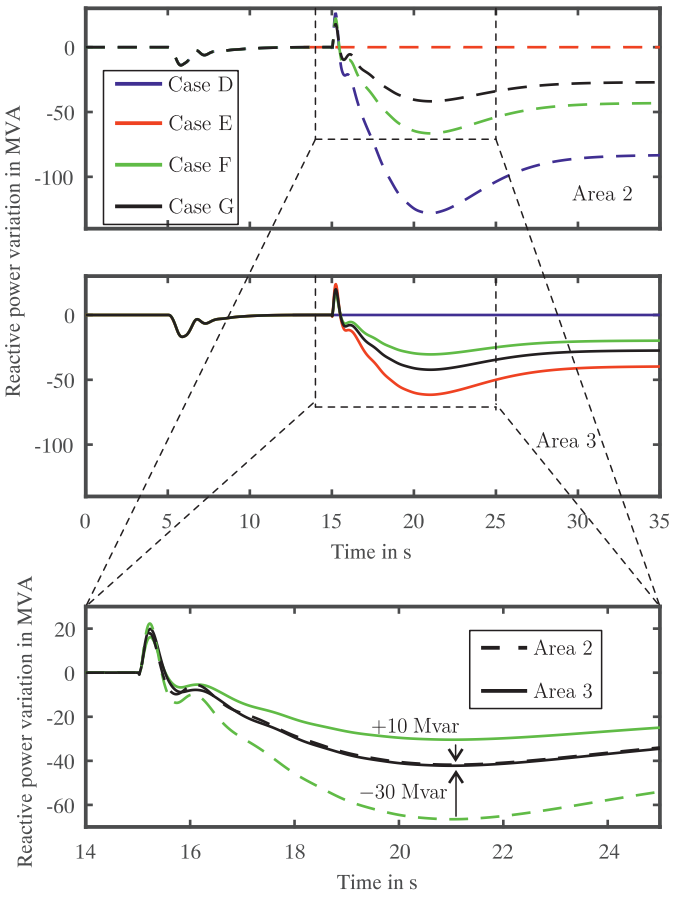


Fig. 3.50: Mtdc reactive power variation with FS-VDL in the two supporting terminals and zoomed view of Cases F (green) and G (black).

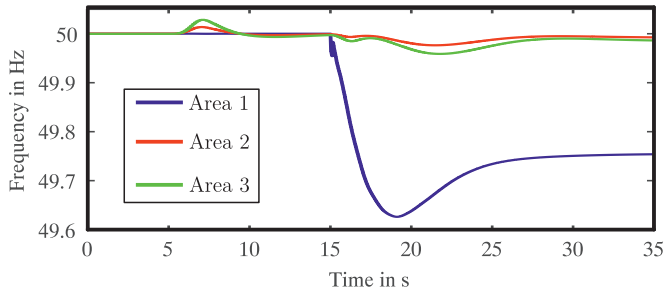


Fig. 3.51: System frequency in the three areas with FS-VDL for Case G ($p_2 = 0.3077$, $p_3 = 0.6923$).

case F (Fig. 3.50). As depicted in Fig. 3.51, the frequency oscillation damping in affected and supporting areas, respectively, remains unchanged.

3.4. Summary and conclusions of the section

HVdc systems can provide a variety of services to the ac grid, which are congestion management, reactive power provision for steady-state voltage support and fault ride through, black-start capability, primary frequency regulation and virtual inertia emulation. In this section, possible benefits and challenges of the respective control implementation in the HVdc

systems are discussed with special emphasize on the frequency related grid services.

Indeed, HVdc systems can vary their dc power flow proportionally with the frequency deviation or with the gradient of the frequency deviation to contribute with high dynamics to primary frequency regulation and emulate virtual inertia in the grid, respectively. However, as a consequence of the fast control action temporary active power imbalances and frequency deviations in the supporting areas arise. Instead of installing costly energy storage systems as reserve capacity, this work proposes an HVdc-based primary frequency controller acting on voltage-dependent loads as solution to overcome the conventional controller limitations and relief the burden on the supporting areas' generators. Only applied as a safety measure in the case of a frequency contingency, the HVdc terminal is controlled to inject reactive power in order to influence the grid voltage and consequently shape the power consumption of nearby voltage-dependent loads (e.g. HV substation, industrial aluminum or steel plant). As consequence, while the area 1 frequency is still adequately damped, the frequency oscillation in area 2 is limited, compensating the local power imbalance.

Taking the energy not only from the generators but also from the loads of the supporting area enables additional upward and downward operational reserve. Hence, embedded HVdc system, which otherwise, due to the synchronous coupling of the areas at both sides of the link, cannot participate in the primary frequency regulation, are enabled to support the grid frequency nadir also in case of strict grid voltage constraints.

While the load control action improves the grid's post-disturbance frequency behavior, it can possibly interfere with maximum permissible voltage variations given by the current technical requirements for grid connection of HVdc systems. In this section, it is demonstrated, that in the case of multi-terminal systems, the share of the frequency support can be optimally adjusted considering the areas' load power sensitivity to voltage. This results in minimum impact on the grid voltage (and hence minimum required reactive power injection), while providing the same additional damping to the affected and supporting grid.

The improvements of the load control application have been analyzed theoretically using state-space models and validated in PSCAD/EMTDC simulations considering asynchronous HVdc link and embedded HVdc systems in large interconnected grid.

The primary frequency regulation controlling voltage dependent loads has been only applied in the active power controlling terminals of HVdc system with the master-slave control approach by now. However, multi-terminal HVdc systems are likely to be controlled with dc-voltage or active power droop to enhance the supply security in case of converter or line outages. Hence, in the future, it is important to investigate the load control implementation in droop-controlled MTdc systems, also considering the possible interferences with the dc voltage droop controller, which were already mentioned for the conventional primary frequency regulation in [13]. Also, the load control in the affected area itself, which does not

involve any change in the HVdc power transmission and hence does not require participation of other connected areas can be included in the future scenario.

The primary frequency regulation controlling voltage dependent loads has been considered as application case for the dynamic capacity of HVdc systems [100]. VSC-HVdc systems have the capability to operate temporarily outside their nominal active and reactive power (P/Q) specification under certain conditions. The usage of the HVdc dynamic capacity is intended to provide grid services and ensure a more efficient and secure grid operation, which should be studied in more details also considering real field data as intended in the Kopernikus-project ENSURE "New ENergy grid StructURes for the German Energiewende" [140].

While the HVdc-based control of voltage dependent loads has been already investigated for primary frequency regulation in asynchronous interconnectors and embedded HVdc, another interesting application can be foreseen in offshore wind farm connections. As stated in [111], after the frequency support, the wind turbine recovery can cause temporary power imbalance and noticeable frequency deviations in the offshore grid, which can be potentially compensated extracting the required energy from the voltage dependent loads.

4. Design of dc circuit breakers

In HVdc systems, breaking the current in a short circuit event is challenging. In contrast to ac grids, in the dc equivalent a natural zero crossing of the fault current does not exist. Hence, a dc circuit breaker must create an artificial zero crossing to interrupt the fault current safely and to avoid large arc. Moreover, the dc grid offers low line impedance, which leads to high fault currents with fast transients. In this regard, the design and development of suitable dc CBs is seen as a pivotal step towards future MTdc grids. In the following section, first a generalized list of requirements for dc CB is developed and recent dc CB designs are reviewed. These findings are based on [141]. Then, to evaluate dc CB designs with the proposed criteria, an accurate and computational efficient fault current estimation method based on coupled linear differential equations and modified average value model of the MMC considering its control is presented based on [142]. The third subsection introduces the use of modular hybrid dc CB for fault identification and adaptive auto-reclosing as presented in [143].

4.1. Requirement analysis of high voltage dc circuit breakers

The basic requirement of HVdc CB is the capability to create a local current zero at the rated fault current without a re-strike of the mechanical interrupters or thermal overload of power electronic components [31]. Following this assumption, the main design criteria as reported in [31] are

- the maximum current the breaker can interrupt
- the interruption time
- the generation of sufficient counter voltage to initiate the fault current suppression
- the energy absorption capability
- the capability to withstand the rated dc voltage for a certain duration after the fault current interruption
- the dielectric withstand to ground

The rated fault clearing sequence, i.e. the possibility of auto-reclosing and frequent switching, is determined by the capability to withstand the current, voltage, or energy stress multiple times before thermal runaway or insulation breakdown.

4.1.1. Generalized qualitative criteria to evaluate high-voltage dc circuit breaker

The most important design parameters that a test routine should proof are the rated short circuit current (for instance, up to 11 kV as stated in [31]) with adequate $\frac{\mathrm{d}i}{\mathrm{d}t}$, the voltage stress after fault current interruption that the dc CB has to withstand (i.e. the rated system voltage, for instance, up to 320 kV [31]) and the energy stress (i.e. the energy the dc CB has to dissipate in the worst case fault condition; as example, in [31] it is mentioned 18.5 MJ for 150 mH dc side inductance and 11 kA maximum current), which under test conditions should be equivalent to the energy stored in the current limiting inductance as well as the energy supplied from the rest of the system in real operation condition [31]. Therefore, fault current envelopes, which are used in standardized dc CB testing, require in their simplest form the knowledge about peak fault current and maximum current derivative [39].

The article [34] states as main dc CB requirements the operating time, maximum current interruption capability, and absorbed energy and defines dc CB operational graphs to visualize the interdependence of these parameters. The dc CB design is not only influenced by the capability to clear the fault, but also by the chosen protection philosophy. As stated in Subsection 2.6.3, HVdc protection philosophies are clustered in fully selective, partially selective and non-selective, which sets the fault ride through scenario of the MMC [34]. A fully selective protection system, which is the focus of this section, does not allow any converter to be blocked, since the power flow in the remaining part of the grid as well as the ac grid support (in the sense of continuous ac voltage and reactive power support, i.e. STATCOM functionality as explained in Subsection 3.1.2) must be maintained. A partial selective protection would allow the temporary blocking of local converters, e.g. those connected to the faulted grid protection zone, while a non-selective protection allows temporary shutdown of the whole HVdc system and hence allows for blocking of both local and remote converters. The design parameter, which is mostly influenced by the choice of protection philosophy, is the size of fault current limiting devices (e.g. inductors). If temporary blocking of local converters is allowed, the fault current limiting requirement is reduced, which could save costs and enhance the dynamic controllability of the HVdc system [144]. In this case, the size of the minimum inductor is set to prevent the converter with the lowest rating from blocking and other inductors in the grid are scaled down inversely to other converters' power rating [34].

In [145], the influence of the protection philosophy on the energy dissipation requirement is studied also under the consideration of the maximum current rating and the time from fault occurrence to interruption. In addition, this work lists as important requirements the commutation time and sufficient counter voltage capability of the arrester to demagnetize the grid inductance and drive the short circuit current to zero.

The article [40] discusses grid integration aspects of high-voltage dc CB. As main aspects,

Table 4.1: Criteria and measures to evaluate the dc CB concepts.

Criteria	Description	Assessment measure
Interruption time	Time from beginning of detection to current zero (including detection time, trip signal communication, breaking and clearing time)	Analytical fault current estimation (AFCE), EMT-simulation (grid + ICT)
Voltage rating	Nominal arrester voltage	Specification
Current rating	Max. current conduction in normal operation	Specification
Max. fault switch-off current	Peak fault current (higher than converter trip threshold current)	AFCE, EMT-simulation (grid)
Transient interruption voltage (TIV)	Peak counter-voltage across dc CB after current interruption	EMT-simulation (stand.)
Max. $\mathrm{d}v/\mathrm{d}t$	Rate of rise of TIV	EMT-simulation (stand.)
Max. $\mathrm{d}i/\mathrm{d}t$	Rate of rise of fault current	AFCE, EMT-simulation (grid)
On-state power losses	Accumulated losses of the main current path	Calculation (semiconductor design)
Chip area	Accumulated area of used Silicon in semiconductors	Calculation (semiconductor design)
Energy absorption capability	Max. fault energy absorbed by the varistor	AFCE, EMT-simulation (stand.)
Dielectric withstand to ground	Insulation in blocked state	EMT-simulation (stand.)
Need for fault current limiter	Additional active or passive devices to limit the fault current rise (in case of limited current capability or large interruption times)	AFCE, EMT-simulation (grid)
Switching sequence	Auto-reclosing function and no. of switching events until thermal runaway or (in case of single switch-off) restoration time and effort	Specification
Bi-directional current breaking capability	Capability of conducting and breaking the fault current in case of reversed current flow	Specification, AFCE, EMT-simulation (grid)
System level delay times	Time from fault occurrence to interruption start (algorithm detection time and communication time for the trip signal)	EMT-simulation (grid + ICT)

the energy absorption capability of the arrester and the minimum size of dc current limiting inductance are analyzed considering the impact of the ac grid, dc lines, and also the delay time of the breaker to initiate a first negative $\frac{\mathrm{d}i}{\mathrm{d}t}$, i.e. to start the fault clearing period. The articles [73] and [146] describe the main design requirements on the basis of a generic mechanical dc circuit breaker considering pole-to-pole (P2P) and pole-to-ground (P2G) faults: arrester voltage rating, peak fault current, dc inductance, dc CB opening time and energy absorption. Moreover, the on-state power losses are mentioned, but - due to the simplicity of the dc CB model - not analyzed.

To facilitate a performance evaluation of future and new dc CB designs from the variety of

different criteria in the literature, a generalized list of qualitative criteria is established in Table 4.1. These criteria focus on hybrid dc CB, as it is the most promising CB technology for future high voltage dc grids. Additionally, measures to assess the suitability of a dc CB design in a given network are proposed.

4.1.2. High-voltage dc circuit breaker topologies

In this subsection different HVdc circuit breaker topologies will be classified and a brief description of their fault interruption principle will be presented.

Passive resonance mechanical circuit breaker Most practically realized HVdc CB consist of three branches: nominal current branch, commutation branch and energy absorption branch [147]. In the passive resonance mechanical CB the commutation branch is a series resonance circuit of capacitor and inductor (Fig. 4.2(a)), in which the arcing voltage of the mechanical switch excites a current with increasing amplitude oscillating at the natural frequency. If this oscillating current exceeds the system fault current, a current zero crossing occur in the nominal branch and the mechanical switch can interrupt the fault. The current continues to flow in the commutation branch, charging the capacitor until the threshold value of the energy absorbing element is reached. Finally, the current flows only in the resistive branch and decreases to zero. Preferably, metal oxide varistors (MOV) are used, which start to conduct only after a certain threshold voltage is exceeded and hence do not require an additional insertion device [147]. This CB topology generally requires 20-40 ms to interrupt the fault current [33], whereas the required interruption time for a HVdc grid should be significantly lower.

Active resonance mechanical circuit breaker Alternatively, the active resonance mechanical CB, also known as active current injection circuit breaker (see Fig. 4.2(b)), uses in the commutation branch a pre-charged capacitor in series with a reactor and thyristor switch to inject instantly a high frequency oscillating counter current (several kHz), that creates a local current zero in the mechanical interrupter of the normal current branch much faster than in the passive resonance CB. The energy absorption branch consists of several parallel stacks of metal oxide surge arresters, which are designed to clamp the peak TIV (hence, limiting the CB's recovery voltage) and to absorb the fault inductive energy. This scheme can typically interrupt dc faults within 8-10 ms [33].

Solid-State circuit breaker The solid-state CB is comprised of series connected power semiconductors in the main current path with parallel energy absorption arrester Fig. 4.2(c). The high dynamics of the power electronic switches provide excellent fault clearing times (in

microseconds range) without an electric arc [34]. However, due to the large series number of semiconductors in the main current path, the on-state losses of pure solid-state circuit breakers are extremely high, reaching up to 30 % of the converter losses [35] and hence making this topology unattractive for practical HVdc applications to date.

Hybrid circuit breaker To comply with the requirements of minimum on-state losses and minimum interruption time, the most recent approaches use a combination of mechanical switch and solid-state devices to clear the short circuit current. These hybrid CB generally consist of three branches to guarantee zero-current switching and hence no arc creation: a low impedance main current branch with ultra-fast mechanical switch (UFMS) in series with a bidirectional auxiliary semiconductor breaker (ASB), a commutation path with main semiconductor breaker (MSB), and an energy absorption path with MOV (see Fig. 4.3). All hybrid dc breakers are equipped with a mechanical residual current breaker (RCB) in series with the main CB to interrupt the residual current (i.e. leakage current flowing through the MOV) and to isolate the faulted system from HVdc grid, if the fault is identified to be permanent.

The auxiliary switch has lower voltage rating (in the range of the on-state voltage of the main switch) than the main breaker, resulting in lower on-state resistance and lower losses (i.e. 0.01% of the converter losses) in comparison with a solid-state dc CB during normal operation. This is possible due to the decoupling of the auxiliary switch from the line by means of the UFMS, which carries the TIV.

In recent literature, main breaker switches are comprised of either series connections of IGBTs with anti-parallel diodes (Hybrid 1) [36], series stacks of H-bridges (Hybrid 2) [38] (Fig. 4.3(a)), or bi-directional thyristors [37] (Hybrid 3, Fig. 4.3(b)). The first two have building block-based designs, which makes them easily scalable to higher system voltages without design changes in the semiconductor part. In [36] each main breaker segment is parallel connected with an individual MOV bank (so called modular hybrid CB). Due to the pure semiconductor MSB and modular MOV this topology offers adaptive auto-reclosing function and multiple fault interruptions.

After detection of the fault, the ASB opens first, avoiding the electrical arc creation across the mechanical switch when opening it, and the current commutates in the main breaker path. As proposed in [36], in order to reduce the impact of the mechanical switch opening delay (usually around 2 ms), the fault detection can be proactive, i.e. the first signal is sent to the ASB when a current increase is noted and the final trip signal to open the MSB is sent if e.g. a predefined overcurrent is reached. If the final trip signal is sent and the contacts of the UFMS are fully separated, the MSB opens, finally conducting the current to the arrester path, where the energy is absorbed (operational principle in Fig. 4.1).

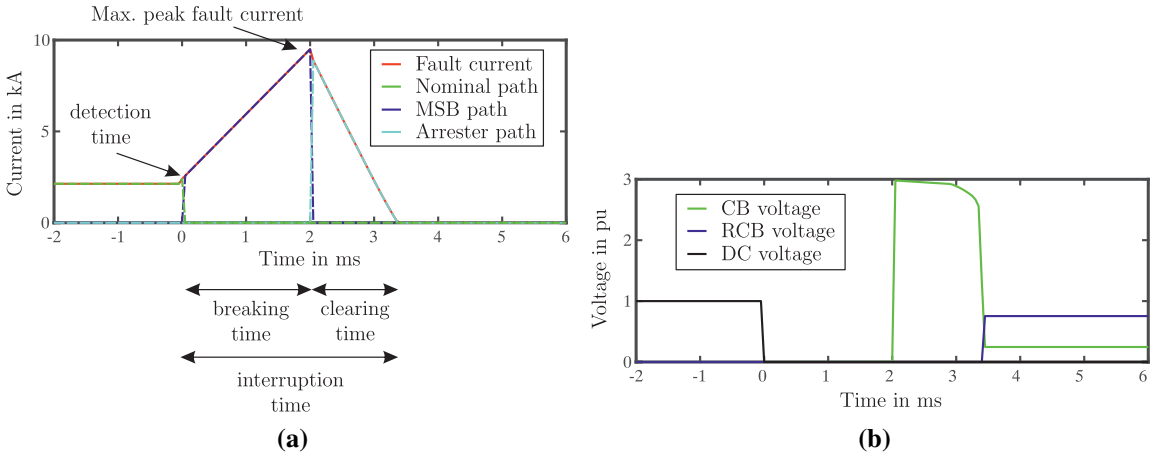


Fig. 4.1: Schematic operational principle of proactive hybrid dc CB (Hybrid 1) [36]: (a) Hybrid dc CB currents, (b) Hybrid dc CB voltages.

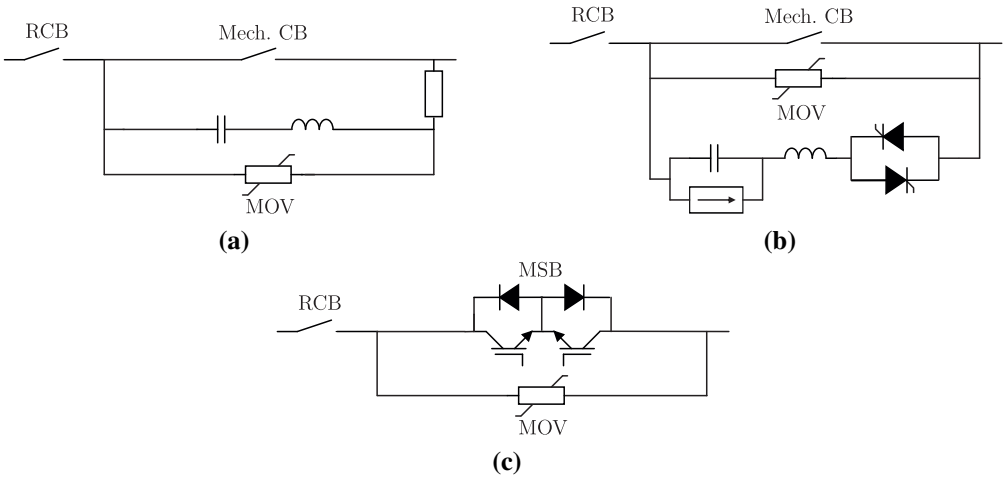


Fig. 4.2: Schematic topologies of dc circuit breakers: (a) Passive resonance mechanical CB, (b) Active current injection CB and (c) Solid-state CB.

In [38] the counter-voltage to conduct the current to the commutation path is created by charging the SM capacitor after turning off the SM IGBTs, instead of using a snubber circuit as in [36]. The counter voltage to initiate the current commutation in the topology presented in [37] is generated by charging series connected capacitors in the MSB path. Each stage is charged to a lower opposing voltage than the previous one, so that a counter current is injected in the previous stage to form current zero for mechanical switch and thyristors switch-off, respectively. Although this thyristor-based topology is equipped with passive components in the MSB path, multiple fault interruptions without noticeable restoration time are achievable as well. Indeed, the capacitors are charged and immediately discharged during the commutation process.

As a basis of following analysis, the proposed ratings of recent HVdc CB solutions in terms of main evaluation criteria are shown in Table 4.2. The values of solid-state (anticipated, since to date, no commercial design is available) and active resonant dc CB have been taken

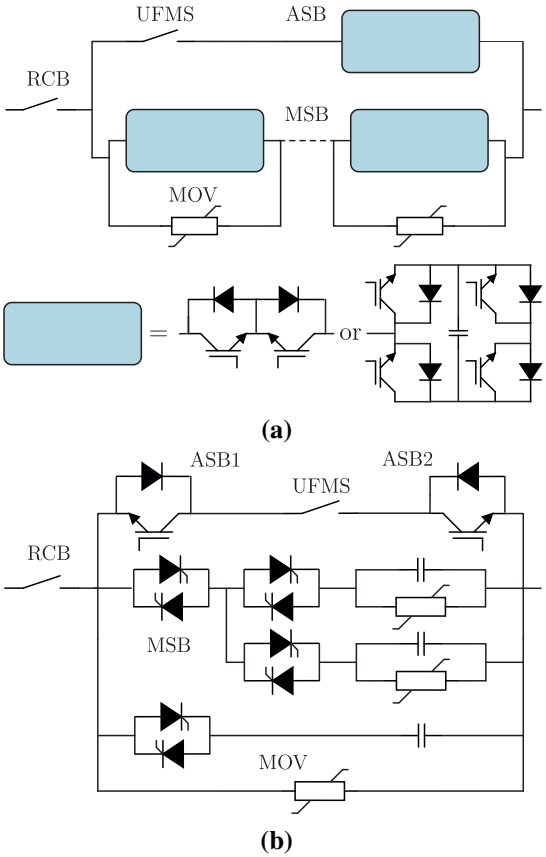


Fig. 4.3: Topologies of hybrid dc circuit breakers: (a) Modular IGBT-based hybrid CB (left: Hybrid 1, right: Hybrid 2), (b) Thyristor-based hybrid CB (Hybrid 3).

Table 4.2: DC breaker technologies comparison. (– indicates no available information.)

	Hybrid 1	Hybrid 2	Hybrid 3	Solid-State	Active Res.	Passive Res.
Interruption time in ms	3.5	≤ 4	5	1 - 3.3	8 - 10	20 - 40
Voltage rating in kV	320	200	120	≤ 800	≥ 320	–
Max. fault switch-off current in kA	test. 9 exp. 16	17	test. 5.3 exp. 7.5	5	10	–
TIV in p.u.	≥ 1.8	1.6	1.35	–	–	–
Losses in % of converter losses	0.01	0.01	0.01	30 - 40	negligible	

from [148] to demonstrate the need for hybrid dc CB solutions.

4.2. Modeling power electronics in dc fault studies

This subsection aims to introduce the necessary models of transmission systems (overhead lines and cables) and the MMC for the analytical fault current estimation.

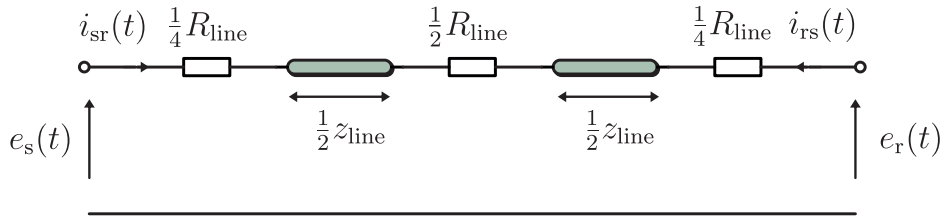


Fig. 4.4: Bergeron model of single-phase transmission line system.

4.2.1. Transmission system modeling

Overhead transmission lines and underground cables are highly non-linear in nature because of the conductors' frequency dependency (e.g. skin effect). To model these systems in EMT simulations, three main approaches are present in the literature [149]:

- Frequency dependent model
- Bergeron-model
- Pi-section model

The frequency dependent model and the Bergeron-model are more accurate, especially for long lines, since they are based on distributed parameters. In contrast to the lumped parameter pi-section model, distributed parameters allow for incorporating the traveling wave effect, so that a voltage disturbance will travel along the conductor with a certain propagation speed (approximately the speed of light), until it is reflected at the other end.

In the frequency dependent model (also known as universal line model), the full frequency dependence of the transmission system is included, which means that the equivalent line parameters are solved in many frequency points within a user defined scope. The full frequency dependence is represented with the telegraphers equation using two matrix transfer functions: the propagation transfer function and the characteristic admittance [150]. This requires long computational time, however, these models are most accurate for studies involving a wide frequency-range and due to the fact that despite the inductance and capacitance the line resistance is also a distributed parameter, provide more accurate results of the traveling waves' attenuation.

The Bergeron model as shown in Fig. 4.4 is in fact based on an ideal, that means loss-less, model of the transmission system, represented by distributed inductance and capacitance. To approximate the system losses, lumped resistance of $\frac{1}{4}R_{\mathrm{line}}$ is included at each end of the line model and $\frac{1}{2}R_{\mathrm{line}}$ in the middle [151]. The Bergeron model is a simplified distributed parameter model, which is evaluated only at a single frequency, usually the nominal grid frequency of 50 or 60 Hz for ac systems and 0.001 Hz as approximation of a steady-state signal for dc systems [149]. Thus, all calculated parameters, such as the characteristic impedance, are calculated at the single specific frequency. Nevertheless, the Bergeron model can be

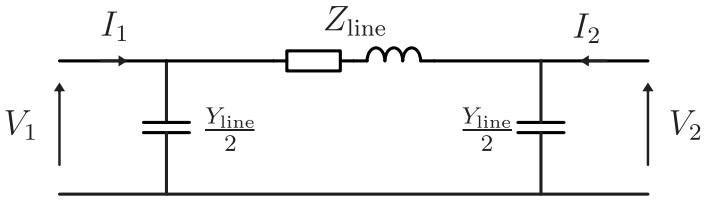


Fig. 4.5: Pi-section model of single-phase transmission line system.

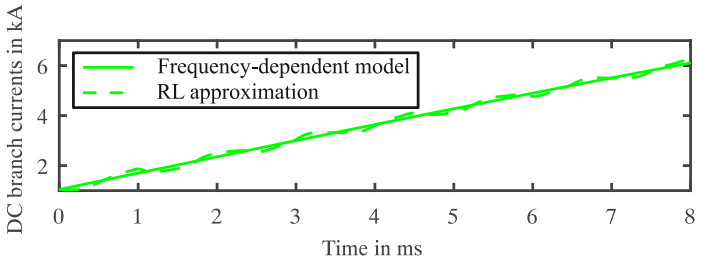


Fig. 4.6: Validation of RL-model for overhead lines.

used for time-domain studies, in which indeed all frequencies are present, with the restriction that only results at the chosen frequency are meaningful. Generally, this makes the Bergeron-model suitable for studies with one main frequency of interest, such as load flow and protection studies. Essentially, the Bergeron-model equals an infinite number of series connected pi-sections (the most simple form of transmission system representation) except that the total system resistance is concentrated at the end and the middle of the line model [149].

The pi-section model is the simplest form of transmission line representation, which makes use of lumped parameters for series line inductance and resistance and the shunt line capacitance [152]. The impedance values are only correct at the fundamental frequency, unless a high number of series connected pi-sections is used, which is impractical from a computational point of view. Thus, this kind of model is incapable of representing the traveling wave phenomena and is - in EMT simulations - just usable for electrically short lines, in which the propagation delays are negligible. The pi-section model as shown in Fig. 4.5 is a simple electrical circuit, in which the series impedance represents the inductance and resistance of the line and the shunt admittance the line capacitance, which is usually halved and placed at each end of the circuit with the series-impedance in between.

A sub-case of the pi-section model is the series RL approximation, in which the shunt capacitance to ground is either neglected or combined with the converters' equivalent dc capacitors. This assumption is valid for overhead transmission line systems, in which the line capacitance is usually small [104].

Fig. 4.6 proves the validity of RL-modeling approach for overhead lines by comparison with frequency dependent overhead line model in PSCAD$^{\text{TM}}$ EMT-simulations. It shows the fault current, which is directly flowing through the faulted line. The RL-approximation accurately

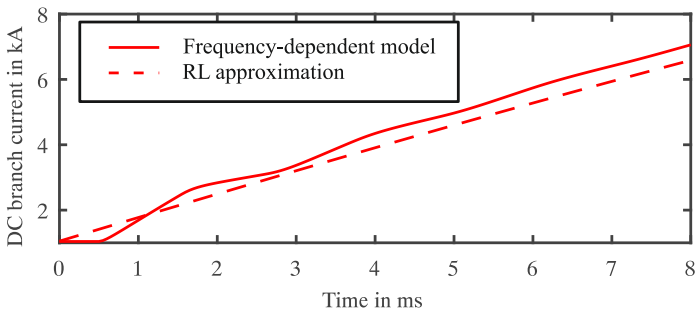


Fig. 4.7: Validation of RL-model for cables.

represents the maximum current (which is mostly determined by the line resistance) and the slope of the current (which is mainly determined by the time constant $\tau_{\text{line}} = \frac{R_{\text{line}}}{L_{\text{line}}}$), while the frequency dependent traveling wave effect and the attenuation along the line are neglected. It provides accurate average estimation of the frequency dependent characteristic, which is suitable for fault current estimation.

It needs to be remarked that the RL-approximation is only valid for overhead lines, in which the capacitance is usually small and thus can be either combined with the dc capacitors of the terminal or neglected at all. In Fig. 4.7 it is shown that using RL-model for cable systems leads to a growing modeling error with increasing time after the fault. If a cable has to be represented, the pi-modeling including shunt capacitors to ground is more suitable in the analysis.

4.2.2. Modular multilevel converter modeling

DC faults include electromagnetic transients, which are in the timescale of the switching frequency of the MMC (order of ms). Thus, to accurately model the effects of dc faults on the converter and also the effects of the converter design on the fault behavior of the dc grid, detailed converter models are usually necessary, which consider the individual switches of the MMC and also consider non-linear switching events.

In [153], the most detailed representation is the full-physics based model, in which complex IGBT sub-circuits are derived from partial differential equations. This modeling type accurately represents the physical behavior and losses of the individual IGBT, but due to its complexity and computational effort it is usually not used in power system studies.

The most detailed model in power system studies is the detailed non-linear IGBT-based model. The IGBT valves are modeled using an ideal control switch, two-non-ideal diodes - one series and one anti-parallel - and a snubber circuit. Non-linear modeling refers to representing the diodes with non-linear resistances using the classical V-I-curve of the diodes [153]. The main advantages of these detailed models are the high accuracy in representing

Table 4.3: General MMC model types for EMT simulations presented in [4].

Model	Nonlinear switching model	Linear switching model	Continuous model	Passive RLC
Detail	Each SM, each switch	Each SM, each switch	Each arm, no switches	Averaged dc side
Accuracy	Exact dc discharge	Approx. dc discharge	Approx. dc discharge	Approx. dc discharge
Simulation speed	Slowest	Faster than nonlinear	Faster than linear	Fastest

the switching and conduction losses and their ability to account for special switching states, like the blocked state in fault operation of the MMC or unbalanced conditions [154]. However, these models are very time consuming in simulations due to the very large number of switches in MMC especially for high-voltage applications and from the power system perspective not all details are necessarily required [154, 153]. Hence, this kind of model should be mostly adopted as accuracy reference for validating simplified models.

Reduced-order models, which accurately replicate the behavior of switches, converters, and control through simplified functions and controlled sources, have been developed to study the MMC in EMT-simulations of large grid studies. Table 4.3 gives a brief overview on general model types for MMC in EMT simulations [4].

Reduced converter models, such as the one presented in [155], aim to simplify the switching behavior of the converter by treating them as two-state resistive devices. The ON-state (or conduction state) of the switch is modeled as small resistance, while for the OFF-state a large resistance is applied. The parallel connection of IGBT and anti-parallel diode can be considered as one device in these models, since essentially the two devices act as one bi-directional switch and only one device is conducting at a given time instance. The SM capacitor in this model can be represented as an equivalent voltage source and resistor by applying numerical integration methods. In order to speed up the simulations, the MMC circuit can be reduced by eliminating internal intermediate nodes and creating Thevenin equivalents for each arm of the MMC [155]. So, in the main network equations the number of nodes is significantly reduced, while in the subsystem the detailed representation of the SM is still considered and each individual capacitor voltage can be obtained.

Further reduction can be achieved, if the individual SM themselves are not longer considered, but the whole converter arm is represented with a controlled voltage source as in [156]. The voltage source is given by the total arm voltage, which equals the sum of all SM voltages. In this kind of model, a blocking feature can be included, which makes it suitable for dc fault studies. However, this continuous model does not include each level of the MMC independently, and therefore does not allow for analyzing abnormal conditions such as device failure or SM control failure.

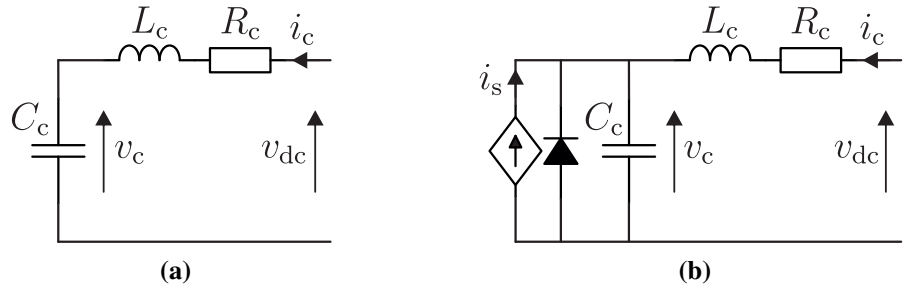


Fig. 4.8: Average Value Model of the Modular Multilevel Converter: (a) Passive RLC, (b) Modified AVM.

Finally, averaged value models (AVM) may be considered, which offer the fastest simulation speed but lack in accuracy especially for discrete events such as the converter blocking. In the simplest form the dc side of the AVM is a purely passive RLC circuit, which however, as it is demonstrated in Subsection 4.3, is not sufficient to accurately represent the fault currents in all parts of the multi-terminal network. Therefore, the classical AVM as in [157] with the improvements mentioned in [158] is considered.

In the classical AVM, the switching elements (IGBTs and diodes) are not explicitly displayed and the MMC behavior is modeled using controlled current and voltage sources [157]. Based on the principle of power balance and assuming a loss-less converter, i.e. equal power at the ac and dc side of the converter, the dc side of the AVM can be derived as a series RLC-equivalent circuit with controlled current source. Following the energy conservation principle [154]

$$W_{\mathrm{MMC}} = 6 \cdot \frac{1}{2} C_{\mathrm{SM}} \sum_{k=1}^{n_{\mathrm{SM}}} V_{\mathrm{SM}_k}^2 = \frac{1}{2} C_{\mathrm{c}} V_{\mathrm{dc}}^2 \ , \tag{4.1}$$

and assuming that all SM have the same voltage V_{SM}, the equivalent capacitor value can be obtained from the detailed model parameters by

$$C_{\mathrm{c}} = \frac{6 C_{\mathrm{SM}}}{n_{\mathrm{SM}}} \ , \tag{4.2}$$

where C_{SM} is the SM capacitor and n_{SM} is the number of SM per arm. On average, it can be assumed that one third of the dc current flows in each arm of the MMC and the dc current flow in the upper and lower arm is equal. Thus, the equivalent inductance is given by

$$L_{\mathrm{c}} = \frac{2 L_{\mathrm{arm}}}{3} \ . \tag{4.3}$$

The total MMC conduction losses can be found with

$$R_{\mathrm{c}} = \frac{2 \left(R_{\mathrm{arm}} + \sum R_{\mathrm{ON}} \right)}{3} \ , \tag{4.4}$$

where R_{arm} and L_{arm} are the arm resistance and inductance, respectively and $\sum R_{\mathrm{ON}}$ is the

sum of the on-state resistances of all IGBT modules.

The article [7] confirms the suitability of this modeling approach for time-domain MMC dc cable fault analysis. Using EMT-simulations of pole-to-pole faults, it is demonstrated that the AVM accurately mimics the slope and peak values of the dc fault current after the fault occurrence until a discrete event occurs (i.e. blocking of the converters' IGBTs) [157]. Improved accuracy of the dc currents can be achieved through more accurate loss modeling as introduced in the MAVM, which has been developed in [158] and is shown in Fig. 4.8. In comparison to the standard AVM, the diode replaces the ideal switch and serves as approximation of the blocked state. The current source reference in blocked state has to be set to zero. However, common to all AVM is that they mimic the converter's behavior during a dc fault correctly only before the converter's IGBTs blocking, which corresponds to the time frame of capacitor discharge. The representation of the fault periods after converter blocking (freewheeling diode conduction period and ac in-feed period) can be improved by adding more complex retro-fit blocking modules [158].

4.3. Fault current estimation in multi-terminal HVdc grids considering MMC control

The choices for a certain protection strategy and the involved protection components, i.e. MMC or dc CB, depend on the fault current that the protection system shall interrupt few milliseconds after the fault occurrence. Before the field implementation, different hardware limitations and requirements (see 4.1) must be evaluated for each protection system. However, it is challenging to estimate all the possible fault conditions in the grid, due to the many involved variables. This calls for an analytical estimation of the fault current in MTdc grids, which links system related parameters with dc CB requirements and provides, in accordance with minimum standards of testing envelopes, the knowledge about maximum fault current and fault current derivative.

4.3.1. Review of fault current estimation methods

The reviewed methods to estimate fault currents in multi-terminal HVdc systems and to analyze grid parameters' impact on those can be classified in three types: A straightforward approach is to simulate (e.g. EMTDC) all the possible fault conditions and then evaluate the worst case scenario, which in the following is referred as EMT-simulation-based fault current estimation. Second, a classical analytical estimation based on traveling wave theory can be used. And lastly, the analytical estimation can be performed based on average converter models and circuit or mesh analysis through coupled linear differential equations.

This thesis concentrates on VSC-based HVdc systems (including the sub-category of MMC-based HVdc systems). Consequently, the fault current estimation in LCC-HVdc systems, which has been studied in works such as [159], is excluded in the following.

Generally, the natural fault current response in VSC-HVdc systems can be grouped in three stages. While for two or three-level VSC-converters the dc capacitor discharge, free-wheeling diode, and ac in-feed stage are reported [41], [31] lists for MMC-based HVdc systems the capacitor discharge, arm current decay, and ac in-feed stage.

In HVdc systems, approximately the first ten milliseconds are dominated by dc capacitor discharge and adjacent line capacitor discharge, which show highest contribution to the fault current and hence are most relevant for the protection system design. After the fault incident, voltage waves are traveling along the lines in both directions of the fault discharging the line capacitors. While the majority of the wave is reflected at the current limiting reactors, part of the wave is transmitted to the converter, where it propagates into the three phase legs of the MMC and partially discharges the SM capacitors resulting in a rapidly increasing current until the converter threshold for converter blocking is reached [31]. The capacitor discharge period ends when the fault current reaches the converter threshold and the converter is blocked. Before converter blocking, the dc components of the arm currents in the MMC increase. After blocking, the arm currents cannot be switched off instantly and are feeding the fault through the freewheeling diodes. The dc current decays with the arm currents until the currents in three of the arms reduce to zero. At this moment, the fault is entirely contributed from ac in-feed (which depends on the strength of the ac network). In the two- or three-level VSC-HVdc system, due to the large dc capacitance, the fault current is expected to be higher [160].

The general benefit of the EMT-based fault current estimation is that it makes use of the fully detailed frequency-dependent model for cables and OHLs and fully detailed switching model of the converter and eventually the breaker. This does not only lead to the most accurate results, but also allows to study the blocked converter behavior and hence to analyze the fault periods after converter blocking (i.e. arm current decay or free-wheeling diode stage, respectively, and ac-infeed stage). However, this comes with the drawback of tremendous simulation time and, as described above, the fault current is predominantly affected by the capacitor discharge in the first milliseconds after the fault. Moreover, especially in multi-terminal systems, the converter blocking should be avoided to continuously provide grid services to the ac and to limit the restoration effort after clearing and removing the fault. From this perspective, it is non-essential that the analytical methods, traveling wave and linear differential equation based, provide valid results just until a discrete event occurs, e.g. the converter turns into blocking state.

Applying traveling waves theory gives highly accurate descriptions of the transient fault current development with multiple surges as the frequency-dependent characteristic of the

lines or cables is considered. Moreover, through the usage of partial differential equations details on the spatial distribution of the current can be included, which is especially relevant for the placement of circuit breakers. On the contrary, the approach using coupled linear differential equations profits from its simplicity, which provides accurate estimation for the most important CB design parameters, i.e. fault current slope and maximum fault current, while facilitating parameter variation analysis in large multi-terminal networks as well and, in case suitable reduction techniques are applied to the differential equations, allows for analytical impact sensitivity analysis. In the following, a literature overview of recent fault current estimation techniques is given.

EMT-simulation based fault current estimation In [41], the development of fault currents in a multi-terminal VSC-HVdc cable system is investigated. A general dc fault current slope inside the dc CB including all three fault stages is established. A parameter variation analysis has been performed to analyze the influence of network components, such as size of dc capacitors, fault resistance and line length of adjacent feeders, which is relevant for the ac in-feed of remote converters. Since the dc CB are restricted in terms of their interruption time and the 12-pulse VSC has limited current capacity, potentially being forced to switch off in fault situation, fault current limiting dc inductors are included in the parameter analysis as well. This study is limited by the fact that only P2G faults in bipolar HVdc systems are studied. Moreover, for future HVdc systems, the MMC will most likely be the dominating converter technology and this study was based on 12-pulse two-level VSC.

The article [160] compares the fault currents in two-level VSC and half-bridge MMC HVdc systems. The analysis focuses on both P2P and P2G faults with respect to fault resistance and fault position. However, as a simplification of an HVdc link, it just includes a single converter with a dc cable connected. This allows for study of only the natural fault response of the converter itself, but cannot give insights into the fault behavior of the HVdc system, which involves the influence of adjacent lines and other converters. Also, this study is limited to cable systems and for the P2P faults only ideal short circuit with zero fault resistance has been considered.

In the article [161] based on PSCAD EMTDC simulations, a comparative analysis of the MMC control parameters' impact on dc faults in a two-terminal HVdc link has been performed. It has been revealed that a variation of control parameters of the output current control, SM balancing control, or type of modulation has no direct impact on the fault current behavior. Instead, the arm-balancing control impacts the modulation reference signal and consequently influences the dc fault current. The outer control loops, due to their relatively slow dynamics, have been neglected in this analysis. The aim of this study is a control parameter variation analysis of a single converter and not the study of fault currents in an MTdc system, which is also revealed by the very early converter trip at around 0.5 ms at

relatively low dc current threshold of around 3 kA. In an MTdc system, the CB would need longer interruption time and it is intended to keep the MMC in operation as long as possible to maintain the power flow in the grid and avoid complete de-energizing. Moreover, it has to be remarked that the negligible effect of control parameter variation must not be mistaken with the representation of power flow in the converter during the fault, which has to be considered for proper MMC representation and fault current estimation in multi-terminal HVdc systems. The power flow can be included by considering parts of the control in the converter model as demonstrated in Subsection 4.3.2.

Traveling-wave based fault current estimation The article [42] derives analytical expressions for the fault currents in a multi-terminal two-level VSC-HVdc system with the aim to specify HVdc circuit breaker requirements. The first milliseconds after the fault occurrence are the most relevant for the circuit breaker design. Since this period is dominated by the capacitor and adjacent feeder discharge, which also yield the highest rate of rise of the fault current, this study focuses on the influence of these two parameters' variation.

Analytical expressions of dc fault currents can be derived using the traveling-wave theory [42], [31] and partial differential equations for voltage v_x and current i_x at the point x of a long line:

$$-\frac{\delta v}{\delta x} = L_{\text{line}}\frac{\delta i}{\delta t} + R_{\text{line}} i \tag{4.5}$$

$$-\frac{\delta i}{\delta x} = C_{\text{line}}\frac{\delta v}{\delta t} + G_{\text{line}} v \tag{4.6}$$

with the line resistance R_{line}, inductance L_{line}, capacitance C_{line}, and shunt conductance G_{line}. Laplace-transformation leads to

$$\frac{\mathrm{d}V(s)}{\mathrm{d}x} = -Z_{\text{line}}(s)\, I(s) \tag{4.7}$$

$$\frac{\mathrm{d}I(s)}{\mathrm{d}x} = -Y_{\text{line}}(s)\, V(s) \tag{4.8}$$

$$Z(s) = R + sL \tag{4.9}$$

$$Y(s) = G + sC \ , \tag{4.10}$$

where $Z_{\text{line}}(s)$ is the cable impedance and $Y_{\text{line}}(s)$ is the cable admittance. Mathematical manipulation results in independent second-order differential equations for the voltage and current:

$$\frac{d^2V(s)}{dx^2} - \gamma^2(s)V(s) = 0 \tag{4.11}$$

$$\frac{d^2I(s)}{dx^2} - \gamma^2(s)I(s) = 0 \tag{4.12}$$

with the propagation constant $\gamma(s) = \sqrt{Z_{\text{line}}(s) \cdot Y_{\text{line}}(s)}$. The solutions of (4.11) and (4.12) can be found with the superposition of the forward and backward traveling waves and the characteristic line impedance $Z_{\text{c}}(s) = \sqrt{Z_{\text{line}}(s)/Y_{\text{line}}(s)}$:

$$V(x,s) = V^{+}(s)e^{-\gamma(s)x} + V^{-}(s)e^{\gamma(s)x} \tag{4.13}$$

$$I(x,s) = \frac{1}{Z_{\text{c}}(s)}\left[V^{+}(s)e^{-\gamma(s)x} - V^{-}(s)e^{\gamma(s)x}\right] \ . \tag{4.14}$$

Finally, the closed-form analytical short circuit current expression is calculated with back-transformation in time domain. In this study the converters are not represented in detail, but only as generic blocked topology, i.e. as diode rectifier. During a P2G fault, which is the focus point of this study, the blocked converter representation is not realistic, since in practice only those converters close to the fault are affected. Moreover, in a bipolar system, only the converter at the faulted pole would be blocked. This fact, together with the negligence of the converter control, does not allow for study of the transition from normal to fault condition [31].

In [31] the MMC dc fault response has been analyzed with the traveling waves approach. A simplified average MMC model without dc voltage and active power control influence and an ideal inductive line (no conductor resistance) has been assumed. The attenuation of traveling waves along the cable due to the line resistance is not considered, and the incident voltage wave is assumed as a negative step function. However, this is not a massive restriction, since this assumption will provide the limit for the largest possible drop in voltage and hence maximum current [39]. Mathematical expressions in time domain have been found for the propagating voltage waves, in order to determine the SM capacitor discharge current. The current output of the MMC under dc fault close to the converter is obtained as:

$$\frac{\mathrm{d}i(t)}{\mathrm{d}t} = \left[B\left(\omega^2+\alpha^2\right)\sin(\omega t) - A\left(\omega^2-\alpha^2\right)\cos(\omega t)\right]\exp(-\alpha t) \ , \tag{4.15}$$

where $\alpha = \frac{R_{\text{eq}}}{2L_{\text{eq}}}$, $\omega = \sqrt{\frac{1}{L_{\text{eq}}C_{\text{eq}}} - \left(\frac{R_{\text{eq}}}{2L_{\text{eq}}}\right)^2}$, $A = C_{\text{eq}}V_{\text{dc}}$, $B = \frac{I_0 + A\alpha}{\omega}$, $R_{\text{eq}} = R_{\text{dc}} + R_{\text{fault}} + \frac{2}{3}R_{\text{arm}}$, $L_{\text{eq}} = L_{\text{dc}} + \frac{2}{3}L_{\text{arm}}$, $C_{\text{eq}} = \frac{6C_{\text{SM}}}{n_{\text{SM}}}$ and I_0 is the initial steady state dc current. Neglecting the resistance in the circuit it can be simplified to

$$\frac{\mathrm{d}i(t)}{\mathrm{d}t} = \frac{V_{\text{dc}}}{L_{\text{eq}}}\cos(\omega t) \ . \tag{4.16}$$

In general, the analysis of the influence of specific components or parameters with the traveling wave approach leads to lengthy equations, if the exact time-domain solution is used, or complex approximations, which are only valid in both the time and spatial proximity of the fault, respectively [42]. The analytical expression in [31] is valid for faults close to the converter terminal until the converter blocking, which can result from either under-voltage

or over-current tripping, respectively. Moreover, detailed parameter analysis has been performed only by EMTDC simulations with focus on dc limiting inductance and fault location.

Another application of traveling waves to estimate dc fault currents can be found in [39]. The aim of this study is to define fault current envelopes, i.e. the collection of all possible fault currents a circuit breaker should be designed to deal with, for 2-level-VSC and MMC. These analytical expressions can be used to specify circuit breaker test circuits, which recreate the conditions of the power system. The study focuses on the fault current in-feed of a single converter and does not provide results for MTdc systems. In this paper, the traveling wave analysis is only applied to non-terminal faults, whereas for two-level VSC a simple sine-wave representation is used if the fault is located at the terminals (i.e. at the converter output):

$$i_{\mathrm{dc}}(t) = V_0 \sqrt{\frac{C_{\mathrm{dc}}}{L_{\mathrm{dc}}}} \sin(\omega t) + I_0 \ . \tag{4.17}$$

Also for MMC a similar equation is used, if the fault is located at the terminals (i.e. at the converter output):

$$i_{\mathrm{dc}}(t) = I_{\max} \sin(\omega t + \phi) \ , \tag{4.18}$$

valid only for a small time interval after the occurrence of the fault $t \leq \frac{\phi - (\pi/2)}{\omega}$, with $\phi = \arcsin\left(\frac{I_0}{I_{\max}}\right)$ and $\omega = \frac{1}{\sqrt{(L_{\mathrm{eq}}+L_{\mathrm{dc}})C_{\mathrm{eq}}}}$ and $I_{\max} = V_0\sqrt{\frac{C_{\mathrm{eq}}}{L_{\mathrm{eq}}+L_{\mathrm{dc}}}} + I_0$. This expression is not intended to exactly estimate the fault behavior of the MMC, but just to get the fault current envelope. Hence, converter control structure is kept constant and the converter does not block in the event of the dc fault. To study fault currents in MTdc systems, this MMC representation is oversimplified as it neglects the resistances (both arm and IGBT resistances) and does not represent the influence of the control and power flow during the fault in the equivalent model.

Differential equation based fault current estimation The article [43] provides a theoretical analysis of cable faults in VSC-HVdc systems based on circuit analysis. The cables are modeled with a series connection of resistance and inductance, whereas these parameters are the pi-model equivalent resistance and inductance of the positive and negative pole cables, respectively. The cable grounding capacitor is omitted, since it is dominated by the large dc capacitor. This cable modeling is not accurate for MMC-HVdc systems, where the capacitors along the cables have significant impact on the dc fault current evolution. From the equivalent circuit of a P2P fault in 2L-VSC-HVdc system it results in a second-order circuit, damped only by the line resistance, naturally leading to an oscillatory current i_{cable}:

$$v_{\mathrm{dc}}(t) = \frac{V_0\omega_0}{\omega} e^{-\delta t} \sin(\omega t + \beta) - \frac{I_0}{\omega C_{\mathrm{dc}}} e^{-\delta t} \sin \omega t \tag{4.19}$$

$$i_{\text{cable}}(t) = C_{\text{dc}} \frac{\mathrm{d}v_{\text{dc}}}{\mathrm{d}t} = -\frac{I_0 \omega_0}{\omega} e^{-\delta t} \sin(\omega t - \beta) + \frac{V_0}{\omega L_{\text{line}}} e^{-\delta t} \sin \omega t \ , \tag{4.20}$$

where $\delta = R_{\text{line}}/2L_{\text{line}}$, $\omega^2 = 1/L_{\text{line}}C_{\text{dc}} - (R_{\text{line}}/2L_{\text{line}})^2$, $\omega_0 = \sqrt{\delta^2 + \omega^2}$ and $\beta = \arctan(\frac{\omega}{\delta})$.

The equivalent circuit is valid only for a short time interval after the fault occurrence until the capacitor voltage drops to zero, which initiates the diode freewheeling stage and afterward the ac (or grid-side current) in-feed stage. However, this is not critical, since the capacitor discharge stage, which is accurately represented with the linear differential equations in 4.20, is most relevant for the circuit breaker design.

Also analyzed is the circuit for a P2G (here cable to ground) fault. The capacitor discharging stage is also represented as a second-order circuit, whose natural response gives a non-oscillation discharge process, though. The dc link voltage will not fully drop to zero, so no freewheeling diode stage will occur. During the ac in-feed period the converter topology will change due to commutation between the diodes, which makes it impossible to find continuous analytical expressions. The transient process is described with a stepwise solution of third-order state-space equations.

The study in [43] is limited to VSC-HVdc systems, whereby the modeling has only been validated for the 2-level converter. It reveals that the MMC behaves differently due to the distributed capacitors in the SM and other control structures. Although short circuits are more common in overhead lines due to direct exposure to atmospheric conditions, the authors of [43], as most of the reviewed studies, focus only on cable systems. Another limitation is the assumption of ideal short circuits, i.e. not considering a variable fault resistance.

Li et al were the first to apply circuit analysis by linear differential equations in MTdc systems based on the MMC technology [44]. The fault current estimation is applicable to MTdc systems with multiple dc/dc-converter connected areas, splitting the network in affected/non-affected areas. The article [44] uses a fully passive RLC model for the MMC, i.e. series connection of equivalent resistance, inductance, and capacitance, and mesh analysis to investigate the fault currents in the faulty overhead line. The overhead lines are modeled with series connection of equivalent resistance and inductance. The main target was to study the impact of resistive and inductive fault current limiters, which are included in the equivalent parameters of the line. The analytical results have been partially validated by PSCAD EMTDC simulations.

The method in [44] presents a critical drawback, which makes it unsuitable for CB or in general protection design in MTdc systems. Due to the oversimplified MMC model, which, being fully passive, neglects the influence of the power flow in the converter (from ac to dc) during the fault, the current estimations are only valid in the very proximity of the fault point in the faulty line. Neglecting the power flow results in incorrect results for dc terminal voltages and hence for the currents in adjacent lines of the grid, which are mostly influenced

by the terminal voltage difference and not by the fault parameters itself. Moreover, this work considers only one study case, P2P faults in symmetrical monopole grids.

Research Question The reviewed fault currents estimation techniques provide valid steps toward an analytically funded design of dc CB. However, they still show significant research gaps. EMT-simulation based methodologies are very time consuming, if multiple parameters should be varied to cover the big number of fault scenarios in the dc CB design process. Furthermore, they rely on detailed models of the converter and lines or cables, which require data not always available due to property restrictions. The traveling wave analysis instead requires the solution of lengthy equations, if the exact time-domain solution should be found to analyze the influence of specific components or parameters. To overcome this issue, complex approximations have to be performed, which are only valid in time and spatial proximity of the fault. The use of mesh analysis based on linear differential equations is a simple yet accurate approach to estimate the fault current slope and maximum peak current, which are the most relevant design parameters. Moreover, it allows to investigate multiple parameter variations in a very short time. However, the reviewed approaches in the literature either consider only VSC or are based on oversimplified passive modeling of the MMC, which makes them unsuitable for the analysis of multi-terminal systems. Another common drawback is that the fault current estimation is applied only to a restricted number of study cases, focusing for example on only one fault scenario (P2G or P2P) or assuming only ideal short circuit conditions neglecting the influence of the fault resistance or the presence of fault current limiting devices.

As an interesting research question has been found, to develop a fault current estimation method, which allows complex parameter variation analysis with limited computational effort for various fault scenarios in an MMC-based MTdc system. In the following section, it is presented a fault current estimation based on mesh analysis and modified average value model of the MMC, which includes the power flow by considering the MMC outer loop control. The presented fault current estimation also extends the mesh analysis to bipolar systems and considers pole-to-neutral faults, which are more common in MTdc systems, by the inclusion of virtual path resistance.

4.3.2. Pole-to-pole fault current calculation in symmetrical monopole MTdc grids considering control dynamics

The proposed P2P fault current calculation method is based on mesh analysis with coupled differential equations. A symmetrical monopole HVdc network can be separated into positive and negative poles, where, due to the symmetry, only the positive branch currents need to be calculated. The MMCs are represented with their modified average value model, i.e.

by series RLC circuits and controlled current source to represent the power flow as depicted in Fig. 4.8(b). The branches of the dc network are represented by a series RL circuit, where traveling wave phenomena are neglected. The RL-model can be regarded as an average approximation of the frequency dependent characteristic of the line, which is suitable for the fault current estimation as demonstrated in Subsection 4.2.1. It has to be remarked that the RL-approximation is only valid for overhead lines. However, overhead transmission lines are considered as the primary scheme for long distance transmission, because of relatively low cost and high technology readiness [83]. Moreover, they are directly exposed to atmospheric conditions, which makes them more vulnerable against short circuit events. Hence, the focus of the fault current estimation below lies on OHL HVdc systems. If a cable has to be represented, the pi-section model including shunt capacitors to ground is more suitable. In that case each parasitic capacitor will be added as supplementary state in the fault current estimation. Hence, for each cable pi-section two additional voltage differential equations have to be considered in the set of differential equations:

$$\frac{\mathrm{d}v_{\mathrm{par}}}{\mathrm{d}t} = \mathrm{diag}\left[\frac{1}{C_{\mathrm{par,12}}} \quad \ldots \quad \frac{1}{C_{\mathrm{par,ij}}}\right] \cdot i_{\mathrm{par}} \ . \tag{4.21}$$

The currents through parasitic capacitors can be expressed with KCL by branch and converter currents and thus do not require additional differential equations.

It must be noted that the RLC MMC model is an oscillatory circuit, that causes inaccurate results after the first ten milliseconds. However, to design a dc circuit breaker, exactly this time period is of the highest importance, since the maximum current and initial current rise are dominantly affected during this capacitor discharge phase [41], [31].

As basis of the mesh analysis, the nodes in the network must be classified based on their physical connection and hence their mathematical independence. Nodes connected to an MMC are defined as real (i.e. independent) nodes and dc connection points of more branches are defined as virtual (i.e. dependent) nodes. Both are labeled with n_{i}. The branch from node n_{i} towards node n_{j} representing an overhead transmission line is entitled with b_{ij}. The current in this branch i_{ij} is flowing from node n_{i} towards node n_{j}. The current injected by MMC i is i_{ci} and the voltage across the equivalent capacitor is v_{ci}, respectively. It represents the steady-state dc voltage of the respective MMC i. A P2P fault is modeled as a real node with variable fault resistance instead of the MMC equivalent circuit.
The dynamic behavior of the branch currents can be expressed with the following equation:

$$\mathbf{A}_{\mathrm{t}} \cdot \mathbf{v} = \mathbf{R}_{\mathrm{t}} \cdot \mathbf{i} + \mathbf{L}_{\mathrm{t}} \cdot \frac{\mathrm{d}\mathbf{i}}{\mathrm{d}t} \ , \tag{4.22}$$

where $\mathbf{i} = [i_{12} \ldots i_{\mathrm{ij}} \ldots]^{\mathrm{T}}$ is the branch current vector, $\mathbf{v} = [v_{\mathrm{c1}} \ldots v_{\mathrm{ci}} \ldots]^{\mathrm{T}}$ is the node voltage vector, $\mathbf{A}_{\mathrm{t}}$ is the network incidence matrix, and $\mathbf{R}_{\mathrm{t}}$ and $\mathbf{L}_{\mathrm{t}}$ are the network resistance and inductance matrix, respectively.

Table 4.4: Off-diagonal elements of resistance matrix for branch ij.

Branch current	i_{ik}	i_{ki}	i_{jk}	i_{kj}	i_{kp}	i_{pk}
Element	R_{ci}	$-R_{ci}$	$-R_{cj}$	R_{cj}	0	0

The elements of the incidence matrix are calculated based on equation (4.23):

$$a_{ki} = \begin{cases} 1, & \text{node } i \text{ is starting point of branch } k \\ -1, & \text{node } i \text{ is ending point of branch } k \\ 0, & \text{node } i \text{ is not a point of branch } k \ . \end{cases} \tag{4.23}$$

For subsequent simplification the incidence matrix is split into two parts. $\mathbf{A}_{t1}$ contains all real node columns and $\mathbf{A}_{t2}$ contains all virtual node columns.
The diagonal elements of the resistance and inductance matrix contain the sum of all resistances and inductances in the path of the respective branch current. For branch ij, its diagonal elements are $2R_{ij} + R_{ci} + R_{cj}$ and $2L_{ij} + L_{ci} + L_{cj}$, respectively. The off-diagonal elements represent the elements in the path in which the other branch currents flow. The off-diagonal element's sign represents the reference direction of the other branch current. Hence, the possible off-diagonal elements for branch ij are shown in Table 4.4.

Since the virtual node voltages are not mathematically independent, they result in an overdefined differential equation problem, which can be avoided by replacing the virtual node voltage by the voltage drop between virtual node and fault node. It is summarized in matrices $\mathbf{R}_1$ and $\mathbf{L}_1$, which contain the respective resistances and inductances in the virtual node row. Left multiplying $\mathbf{R}_1$ and $\mathbf{L}_1$ by $\mathbf{A}_t$ and subtracting them from $\mathbf{R}_t$ and $\mathbf{L}_t$, respectively, results in:

$$\mathbf{R}_2 = \mathbf{R}_t - \mathbf{A}_t \cdot \mathbf{R}_1 \tag{4.24}$$

$$\mathbf{L}_2 = \mathbf{L}_t - \mathbf{A}_t \cdot \mathbf{L}_1 \ . \tag{4.25}$$

The resulting matrices $\mathbf{R}_2$ and $\mathbf{L}_2$ are not full rank. Thus, the virtual node rows in $\mathbf{R}_2$ and $\mathbf{L}_2$, respectively, need to be replaced by $\mathbf{A}_{t2}$ and the corresponding rows in $\mathbf{A}_{t1}$ need to be set to zero. Essentially, this leads to the KCL equation at the virtual node. The updated matrices $\mathbf{A}_{t1}$, $\mathbf{R}_2$, and $\mathbf{L}_2$ are renamed as $\mathbf{A}$, $\mathbf{R}$, and $\mathbf{L}$ and (4.22) migrates to (4.26):

$$\mathbf{A} \cdot \mathbf{v} = \mathbf{R} \cdot \mathbf{i} + \mathbf{L} \cdot \frac{\mathrm{d}\mathbf{i}}{\mathrm{d}t} \ . \tag{4.26}$$

The dependence between MMC currents $\mathbf{i}_c = [i_{c1} \ldots i_{ci} \ldots]^T$ and branch currents can be found with:

$$\mathbf{i}_c = -\mathbf{A}_{t1}^T \cdot \mathbf{i} \ . \tag{4.27}$$

In the following, it is demonstrated without loss of generality for voltage controlling nodes,

how the source current representing the power flow in the MMC during the fault is considered in the fault current estimation. Regarding the MAVM of the MMC, the source current is calculated based on

$$i_{\mathrm{sMMC}} = \frac{P^*}{v_{\mathrm{c}}} \tag{4.28}$$

for power controlling terminals and

$$i_{\mathrm{sMMC}} = k_{\mathrm{p,vdc}} \cdot (V_{\mathrm{dc}}^* - v_{\mathrm{c}}) + k_{\mathrm{i,vdc}} \int (V_{\mathrm{dc}}^* - v_{\mathrm{c}})\,\mathrm{d}t \tag{4.29}$$

for dc voltage controlling terminals, respectively. In the case of voltage controlling terminals the dc voltage controller output based on p.u. values is used as input for the controlled current source. The current i_{d} is generally used to control the active power and consequently the dc voltage. If the converter is loss-less and is operated at its voltage rating (ac and dc voltage are 1 p.u.), it can be assumed from

$$P^* = i_{\mathrm{d}} \cdot v_{\mathrm{d}} = i_{\mathrm{sMMC}} \cdot v_{\mathrm{c}} \tag{4.30}$$

that the p.u. values of line and dc current are equivalent. By mathematical manipulation the source current derivative in the respective measurement units can be found in time domain with

$$\frac{\mathrm{d}i_{\mathrm{sMMC}}}{\mathrm{d}t} = \frac{P_{\mathrm{nom}}}{V_{\mathrm{dc,nom}}^2} \left(k_{\mathrm{i,vdc}} \left(V_{\mathrm{dc}}^* - v_{\mathrm{c}}\right) - k_{\mathrm{p,vdc}} \frac{\mathrm{d}v_{\mathrm{c}}}{\mathrm{d}t} \right) \ , \tag{4.31}$$

where $V_{\mathrm{dc,nom}}$ and P_{nom} are the converter nominal dc voltage and power, respectively. Consequently, (4.31) has to be included in the problem's set of coupled differential equations for each voltage controlled node and time-dependent variables for the source current $\mathbf{i}_{\mathrm{sMMC}} = [i_{\mathrm{sMMC1}} \ldots i_{\mathrm{sMMCi}} \ldots]^{\mathrm{T}}$ have to be respected in the dc voltage differential equations.

The dynamic relationship between the converter voltages across the equivalent MMC capacitor and the converter currents $\mathbf{i}_{\mathrm{c}}$ and $\mathbf{i}_{\mathrm{s}} = [i_{\mathrm{s1}} \ldots i_{\mathrm{si}} \ldots]^{\mathrm{T}}$ can be found with

$$\frac{\mathrm{d}\mathbf{v}}{\mathrm{d}t} = \mathbf{K} \cdot (\mathbf{i}_{\mathrm{c}} + \mathbf{i}_{\mathrm{sMMC}}) \ , \tag{4.32}$$

with

$$\mathbf{K} = \mathrm{diag} \begin{bmatrix} \frac{1}{C_{\mathrm{c1}}} & \ldots & \frac{1}{C_{\mathrm{ci}}} \end{bmatrix} \ . \tag{4.33}$$

Considering (4.27) and (4.32) and defining

$$\mathbf{P} = -\mathbf{K} \cdot \mathbf{A}_{\mathrm{t1}} \ , \tag{4.34}$$

the relationship between the node voltages, branch currents, and source currents can be found with (4.35):

$$\frac{\mathrm{d}\mathbf{v}}{\mathrm{d}t} = \mathbf{P} \cdot \mathbf{i} + \mathbf{K} \cdot \mathbf{i}_{\mathrm{sMMC}} \ . \tag{4.35}$$

The dynamics of the dc voltage PI- and power P-controller determine the time-dependency of the source current vector $\mathbf{i}_{\mathrm{sMMC}} = [i_{\mathrm{sMMC1}} \dots i_{\mathrm{sMMCi}} \dots]^{\mathrm{T}}$. In consequence, these control dynamics are included in the coupled differential equations. Solving the coupled differential equations given by (4.26), (4.31), and (4.35) allows to calculate all dc line currents in the multi-terminal network accurately in case of an P2P fault. To obtain the necessary initial values of the state variables $\mathbf{i}$ and $\mathbf{v}$, a load-flow analysis, e.g. based on the well known Newton-Raphson method, must be accomplished previously.

4.3.3. Fault current calculation in bipolar MTdc grids considering control dynamics

In its presented form, the fault current estimation in Subsection 4.3.2 is only applicable to pole-to-pole-faults in symmetrical monopole grids. The following subsection aims for generalizing the fault current estimation to both monopole and bipolar grids. At first, an extension from monopole P2P faults to those in bipolar MTdc grids is presented. Although the P2P faults are generally considered to be more severe, in future MTdc grids a distinction between P2P and other fault types such as pole-to-neutral (P2N) faults may be important. This is motivated by possible combined protection solutions, containing both converter and breaker actions, whose requirements vary with the type of fault. Therefore, in the second part of the subsection the generalized use of the fault current estimation to both fault types, P2P and P2N, will be enabled by introducing the concept of virtual path with infinite resistance between healthy pole and neutral conductor.

Generally, a bipolar MTdc system consists of two MMC with the midpoint grounded at each converter terminal and optionally a neutral conductor. In consequence, to include the additional (without loss of generality it is referred to as the negative) pole, the respective MMC variables $\mathbf{i}_{\mathrm{c}}$, $\mathbf{v}$ and $\mathbf{i}_{\mathrm{s}}$ need to be duplicated in the differential equations. Positive pole MMC variables are denoted with subscript p and negative pole MMC variables are denoted with subscript n, respectively. Since the branch currents in positive and negative pole are identical in the case of bipolar P2P faults, the branch definition of the monopole case can be applied and the definition of resistance and inductance matrix remain the same. The dynamic behavior of the branch currents can be found with (4.36):

$$\mathbf{A} \cdot \left(\mathbf{v}_{\mathrm{p}} + \mathbf{v}_{\mathrm{n}}\right) = \mathbf{R} \cdot \mathbf{i} + \mathbf{L} \cdot \frac{\mathrm{d}\mathbf{i}}{\mathrm{d}t} \ . \tag{4.36}$$

The dependence between positive pole MMC currents $\mathbf{i}_{\mathrm{cp}} = \left[i_{\mathrm{c1p}} \dots i_{\mathrm{cip}} \dots\right]^{\mathrm{T}}$ and negative pole MMC currents $\mathbf{i}_{\mathrm{cn}} = [i_{\mathrm{c1n}} \dots i_{\mathrm{cin}} \dots]^{\mathrm{T}}$, respectively, and branch currents can be obtained with (4.37):

$$\mathbf{i}_{\mathrm{cp,n}} = -\mathbf{A}_{\mathrm{t1}}^{\mathrm{T}} \cdot \mathbf{i} \ . \tag{4.37}$$

Consequently, the relationship between the node voltages, branch currents and source currents can be found with (4.38):

$$\frac{\mathrm{d}\mathbf{v}_{\mathrm{p,n}}}{\mathrm{d}t} = \mathbf{P}_{\mathrm{p,n}} \cdot \mathbf{i} + \mathbf{K}_{\mathrm{p,n}} \cdot \mathbf{i}_{\mathrm{sp,n}} \ , \tag{4.38}$$

with

$$\mathbf{K}_{\mathrm{p,n}} = \mathrm{diag}\left[\frac{1}{C_{\mathrm{c1p,n}}} \quad \ldots \quad \frac{1}{C_{\mathrm{cip,n}}}\right] \tag{4.39}$$

and

$$\mathbf{P}_{\mathrm{p,n}} = -\mathbf{K}_{\mathrm{p,n}} \cdot \mathbf{A}_{\mathrm{t1}} \ . \tag{4.40}$$

The P2N faults lead to an asymmetry in the equivalent network. To enable the generalized coupled differential equation based approach established in Subsection 4.3.2, it is necessary to include a virtual path from healthy pole to neutral conductor with infinite resistance. The concept is illustrated in Fig. 4.12. Also, the current flow in the positive and negative poles is different, which makes it necessary to express both currents with independent state variables i_{ij} and i_{bij}, which are included in the system's current vector $\mathbf{i} = [i_{12} \ldots i_{\mathrm{ij}} \ldots i_{\mathrm{b12}} \ldots i_{\mathrm{bij}} \ldots]^{\mathrm{T}}$.

The dynamic behavior of the branch currents can be expressed with the following equation:

$$\mathbf{A}_{\mathrm{z1}} \cdot \mathbf{v} = \mathbf{R}_{\mathrm{t}} \cdot \mathbf{i} + \mathbf{L}_{\mathrm{t}} \cdot \frac{\mathrm{d}\mathbf{i}}{\mathrm{d}t} \ , \tag{4.41}$$

where $\mathbf{v} = [v_{\mathrm{c1p}} \ldots v_{\mathrm{cip}} \ldots v_{\mathrm{c1n}} \ldots v_{\mathrm{cin}} \ldots]^{\mathrm{T}}$ is the adapted node voltage vector. The real node part of the adapted bipolar incidence matrix is defined as

$$\mathbf{A}_{\mathrm{z1}} = \begin{bmatrix} \mathbf{A}_{\mathrm{t1}} & \mathscr{O}_{\mathrm{At1}} \\ \mathscr{O}_{\mathrm{At1}} & -\mathbf{A}_{\mathrm{t1}} \end{bmatrix} \ , \tag{4.42}$$

where $\mathscr{O}_{\mathrm{At1}}$ is the zero matrix with the size of $\mathbf{A}_{\mathrm{t1}}$. For branch ij, the main diagonal elements of the resistance and inductance matrix are $R_{\mathrm{ij}} + R_{\mathrm{cip}} + R_{\mathrm{cjp}} + R_{\mathrm{nij}}$ and $L_{\mathrm{ij}} + L_{\mathrm{cip}} + L_{\mathrm{cjp}} + L_{\mathrm{nij}}$, respectively. R_{nij} and L_{nij} are the line parameters of the metallic ground return path. For branch bij, the main diagonal elements of the resistance and inductance matrix are $R_{\mathrm{ij}} + R_{\mathrm{cin}} + R_{\mathrm{cjn}} + R_{\mathrm{nij}}$ and $L_{\mathrm{ij}} + L_{\mathrm{cin}} + L_{\mathrm{cjn}} + L_{\mathrm{nij}}$, respectively. Assuming equal line parameters for the positive and the negative pole, the off-diagonal elements for branches ij and bij are given in Table 4.5. Similar to the monopole case, the virtual node voltages are replaced by the voltage drop between the virtual node and the fault node. However, in the P2N case, the equations are obtained for both poles separately. The matrices $\mathbf{R}_1$ and $\mathbf{L}_1$ contain the respective resistances and inductances in the virtual node rows. Left multiplying $\mathbf{R}_1$ and $\mathbf{L}_1$ by the adapted bipolar incidence matrix $\mathbf{A}_{\mathrm{z}}$ and subtracting them from $\mathbf{R}_{\mathrm{t}}$ and $\mathbf{L}_{\mathrm{t}}$, respectively, results in

$$\mathbf{R}_2 = \mathbf{R}_{\mathrm{t}} - \mathbf{A}_{\mathrm{z}} \cdot \mathbf{R}_1 \tag{4.43}$$

Table 4.5: Off-diagonal elements of resistance matrix for branch ij and bij for bipolar MTdc.

$\mathbf{i}_{ij}$							
Branch current	i_{ik}	i_{ki}	i_{jk}	i_{kj}	i_{kp}	i_{pk}	
Element	R_{ci}	$-R_{ci}$	$-R_{cj}$	R_{cj}	0	0	
Branch current	i_{bij}	i_{bik}	i_{bki}	i_{bjk}	i_{bkj}	i_{bpk}	i_{bkp}
Element	R_{nij}	0	0	0	0	0	0
$\mathbf{i}_{bij}$							
Branch current	i_{ik}	i_{ki}	i_{jk}	i_{kj}	i_{kp}	i_{pk}	i_{ij}
Element	0	0	0	0	0	0	R_{nij}
Branch current	i_{bik}	i_{bki}	i_{bjk}	i_{bkj}	i_{bpk}	i_{bkp}	
Element	R_{ci}	$-R_{ci}$	$-R_{cj}$	R_{cj}	0	0	

$$\mathbf{L}_2 = \mathbf{L}_t - \mathbf{A}_z \cdot \mathbf{L}_1 \ , \tag{4.44}$$

with the adapted bipolar incidence matrix

$$\mathbf{A}_z = \begin{bmatrix} \mathbf{A}_t & \mathscr{O}_{At} \\ \mathscr{O}_{At} & -\mathbf{A}_t \end{bmatrix} \ . \tag{4.45}$$

$\mathscr{O}_{At}$ is the zero matrix with the size of $\mathbf{A}_t$. The resulting matrices $\mathbf{R}_2$ and $\mathbf{L}_2$ are not full rank. Thus, to solve the DGL system, the positive pole virtual node rows in $\mathbf{R}_2$ and $\mathbf{L}_2$, respectively, need to be replaced by $\begin{bmatrix} \mathbf{A}_{t2} & \mathscr{O}_{At2} \end{bmatrix}$ and the negative pole virtual node rows by $\begin{bmatrix} \mathscr{O}_{At2} & \mathbf{A}_{t2} \end{bmatrix}$. $\mathscr{O}_{At2}$ is the zero matrix with the size of $\mathbf{A}_{t2}$. The corresponding rows in $\mathbf{A}_{z1}$ need to be set to zero. The updated matrices $\mathbf{A}_{z1}$, $\mathbf{R}_2$ and $\mathbf{L}_2$ are renamed as $\mathbf{A}$, $\mathbf{R}$ and $\mathbf{L}$ and (4.41) migrates to (4.46):

$$\mathbf{A} \cdot \mathbf{v} = \mathbf{R} \cdot \mathbf{i} + \mathbf{L} \cdot \frac{\mathrm{d}\mathbf{i}}{\mathrm{d}t} \ . \tag{4.46}$$

Also, in the case of P2N faults, the positive and negative pole MMC currents can be summarized in a single vector $\mathbf{i}_c = \begin{bmatrix} i_{c1p} \dots i_{cip} \dots i_{c1n} \dots i_{cin} \dots \end{bmatrix}^T$. Thus, the relationship between the MMC currents $\mathbf{i}_c$ and the positive and negative branch currents $\mathbf{i}$ is expressed by

$$\mathbf{i}_c = \mathbf{A}_i \cdot \mathbf{i} \ , \tag{4.47}$$

with

$$\mathbf{A}_i = \begin{bmatrix} -\mathbf{A}_{t1}^T & \mathscr{O}_{At1} \\ \mathscr{O}_{At1} & \mathbf{A}_{t1}^T \end{bmatrix} \ . \tag{4.48}$$

The source current vector of the MAVM of the MMC in the bipolar MTdc is defined as $\mathbf{i}_{sMMC} = \begin{bmatrix} i_{sMMC1p} \dots i_{sMMCip} \dots i_{sMMC1n} \dots i_{sMMCin} \dots \end{bmatrix}^T$. Thus, the relationship between node voltages, branch currents and source currents can be found with (4.49):

$$\frac{\mathrm{d}\mathbf{v}}{\mathrm{d}t} = \mathbf{P} \cdot \mathbf{i} + \mathbf{K} \cdot \mathbf{i}_{sMMC} \ , \tag{4.49}$$

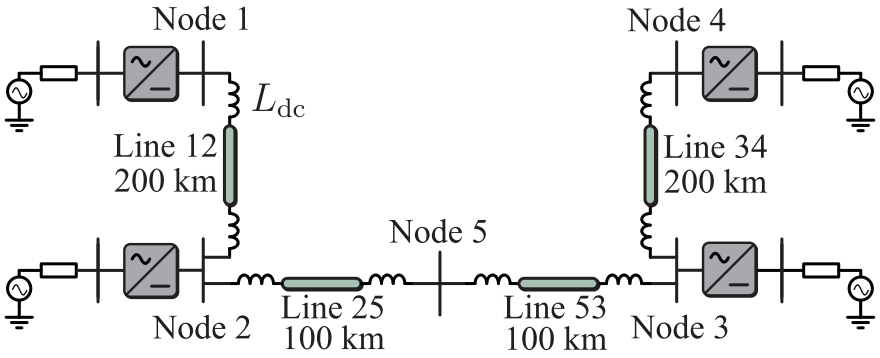


Fig. 4.9: Representation of CIGRE 4-bus MTdc benchmark grid [162].

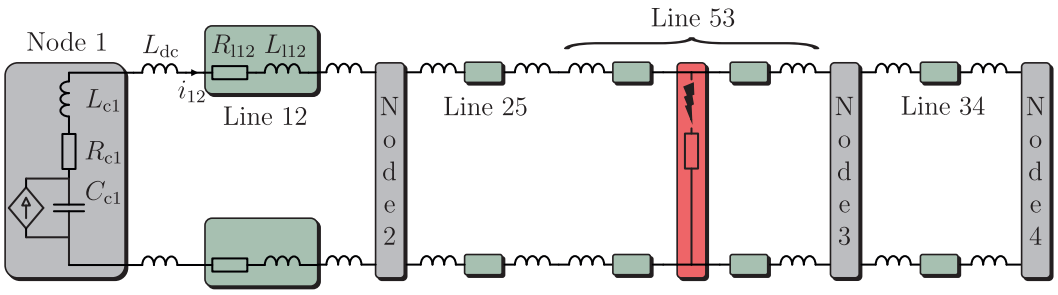


Fig. 4.10: Equivalent circuit model of CIGRE 4-bus MTdc benchmark grid [162] with pole-to-pole fault in line 53.

with

$$\mathbf{K} = \text{diag}\left[\frac{1}{C_{c1p}} \quad \cdots \quad \frac{1}{C_{cip}} \quad \cdots \quad \frac{1}{C_{c1n}} \quad \cdots \quad \frac{1}{C_{cin}}\right]^{T} \tag{4.50}$$

and

$$\mathbf{P} = \mathbf{K} \cdot \mathbf{A}_{i} \ . \tag{4.51}$$

4.3.4. Simulation results

PSCAD EMT-simulations of the 4-bus MTdc CIGRE benchmark grid [162] (see Fig. 4.9) are carried out to verify the accuracy of the proposed fault current estimation. First, it is assumed a symmetrical monopole MTdc grid configuration and a P2P fault is applied at the line 53. The relevant system parameters are listed in Table 4.6 to Table 4.8 and the exemplary resistance and inductance matrix calculations for the equivalent circuit model in Fig. 4.10 are given in (4.52) and (4.53), respectively, and the exemplary incidence matrix and voltage dynamic matrix are given in (4.54) and (4.55), respectively.

Table 4.6: Network Parameters.

Symbols	$V_{\mathrm{dc,nom}}$ [kV]	$I_{\mathrm{dc,nom}}$ [kA]	P_{nom} [MW]	$V_{\mathrm{ll,rms}}$ [kV]
Value	400	2	800	220
Symbols	L_{dc} [mH]	R_{oh} [Ω/km]	L_{oh} [mH/km]	
Value	200	0.006	0.945	

Table 4.7: MMC Parameters and dc Node Control Modes.

Node	L_0[mH]	$R_{\mathrm{on}}[\frac{\mathrm{m\Omega}}{\mathrm{SM}}]$	$R_{\mathrm{arm}}[\Omega]$	N_{SM}	$C_{\mathrm{SM}}[\mu\mathrm{F}]$	Mode	dc ref.
1	29	1.361	0	200	10000	PQ	$P^* = 400\mathrm{MW}$
2	19	0.908	0	200	15000	PQ	$P^* = -800\mathrm{MW}$
3	29	1.361	0	200	10000	$V_{\mathrm{dc}}Q$	$V_{\mathrm{dc}}^* = 400\mathrm{kV}$ $k_{\mathrm{p,U}} = 14$ $k_{\mathrm{i,U}} = 5$
4	116	5.445	0	200	2500	PQ	$P^* = 400\mathrm{MW}$

Table 4.8: Initial values of branch currents and node voltages.

Symbols	i_{12} (t=0)	i_{25} (t=0)	i_{30} (t=0)	i_{34} (t=0)	i_{50} (t=0)
Value [kA]	0.999	-1.044	1.044	-0.974	-1.044
Symbols	v_{c1} (t=0)	v_{c2} (t=0)	v_{c3} (t=0)	v_{c4} (t=0)	
Value [kV]	400.32	398.64	400.46	405.02	

$$\mathbf{R} = \begin{bmatrix} 2R_{12}+R_{\mathrm{c1}}+R_{\mathrm{c2}} & -R_{\mathrm{c2}} & 0 & 0 & 0 \\ -R_{\mathrm{c2}} & 2R_{25}+R_{\mathrm{c2}} & R_0 & 0 & R_0+2R_{50} \\ 0 & 0 & R_0+2R_{30}+R_{\mathrm{c3}} & R_{\mathrm{c3}} & R_0 \\ 0 & 0 & R_{\mathrm{c3}} & 2R_{34}+R_{\mathrm{c3}}+R_{\mathrm{c4}} & 0 \\ 0 & -1 & 0 & 0 & 1 \end{bmatrix} \tag{4.52}$$

$$\mathbf{L} = \begin{bmatrix} 2L_{12}+L_{\mathrm{c1}}+L_{\mathrm{c2}} & -L_{\mathrm{c2}} & 0 & 0 & 0 \\ -L_{\mathrm{c2}} & 2L_{25}+L_{\mathrm{c2}} & 0 & 0 & 2L_{50} \\ 0 & 0 & 2L_{30}+L_{\mathrm{c3}} & L_{\mathrm{c3}} & 0 \\ 0 & 0 & L_{\mathrm{c3}} & 2L_{34}+L_{\mathrm{c3}}+L_{\mathrm{c4}} & 0 \\ 0 & -1 & 0 & 0 & 1 \end{bmatrix} \tag{4.53}$$

$$\mathbf{A} = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{4.54}$$

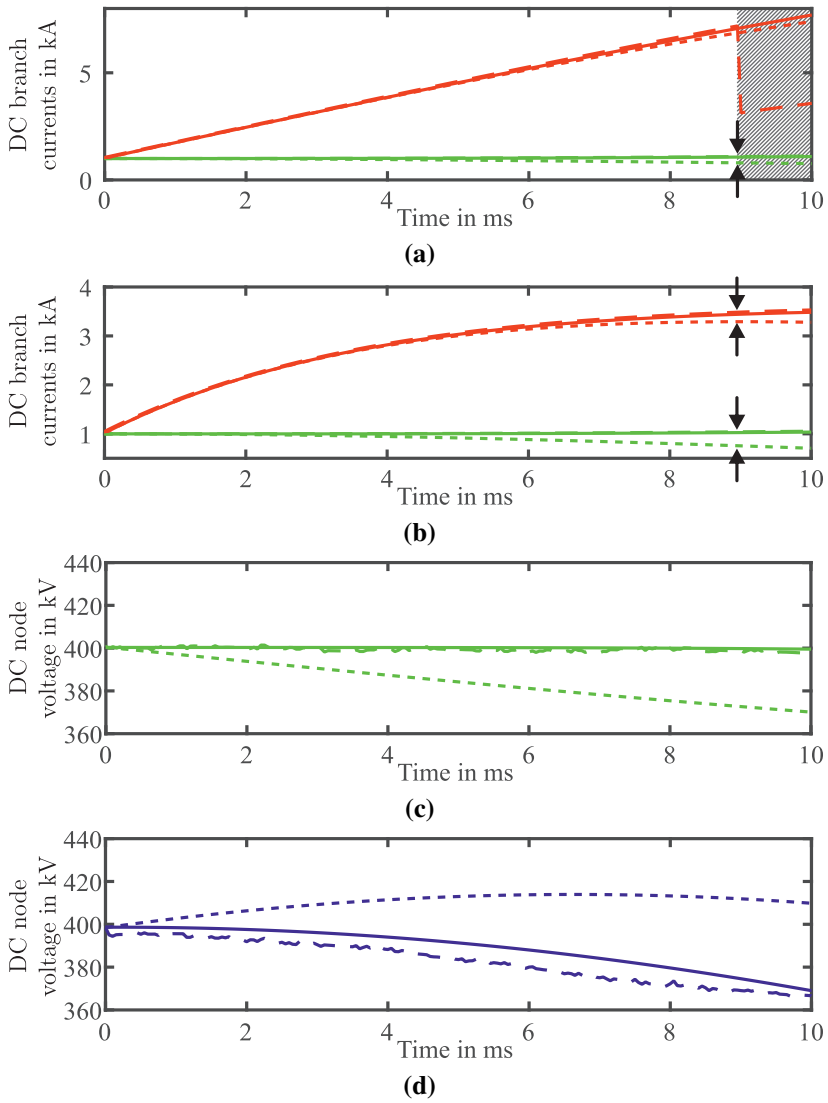


Fig. 4.11: Comparison of dc branch current results (i_{12} (green), i_{30} (red)) with varying fault impedance in symmetric monopole grid: (a) $R_0 = 0.1\ \Omega$, (b) $R_0 = 100\ \Omega$, and dc node voltage results (c) v_{c1}, (d) v_{c2} from presented improved estimation (solid), basic estimation from [44] (dotted) and EMT-simulation (dashed).

$$\mathbf{K} = \begin{bmatrix} \frac{1}{C_{c1}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{c2}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{c3}} & 0 \\ 0 & 0 & 0 & \frac{1}{C_{c4}} \end{bmatrix} \tag{4.55}$$

In Fig. 4.11 the branch currents and node voltages of EMT-simulations, basic differential equations based fault current estimation with simplified MMC representation from the literature [44], and the presented improved fault current estimation are compared. In contrast to the presented method, the basic approach in the literature makes use of an MMC averaged value model without controlled dc current source, which, consequently, does not include the power flow from ac to dc during the fault period leading to inaccurate estimations of the dc branch currents and node voltages. The simplified MMC average value model is an uncon-

trolled resonant circuit, in which the time-dependent parameters, here voltage and current, fully depend on their initial state. In consequence, the resulting modeling error is more than neglecting the ac power in-feed. Indeed, if the initial current flow has a positive sign, the equivalent dc capacitor in the uncontrolled RLC circuit will be charged. By definition, the dc terminal voltage is equal to the voltage across the equivalent capacitor and will increase as well, although the terminal might be connected to the faulty line (and a voltage drop would be expected). The modeling error is demonstrated in an exemplary way in Fig. 4.11(d). Since the remote dc line currents are mostly influenced by the voltage difference between the ends of the respective line, as a result, those current waveforms are inaccurately estimated (see Fig. 4.11(a) and Fig. 4.11(b)). This is a critical drawback, since adjacent feeder currents are known as a prominent contributor to the maximum dc fault current in the faulty path and hence influence the design of the dc CB [41]. Two study cases are carried out to verify the performance of the proposed fault current estimation: ideal short circuit (with low resistance 0.1 Ω) and high-impedance fault (with resistance 100 Ω). As a consequence of the low resistance in Fig. 4.11(a), the branch currents in the faulted line i_{30} show a rapid increase. The high over-current leads to a trip of converter 3 at around 9 ms. As explained above, the analytical methods to estimate fault currents are only valid until a discrete event occurs (i.e. the converter blocking). Hence, the converter blocking phase cannot be modeled with the proposed approach and this time range is grayed. Under the specified fault scenarios, it is assumed that the dc voltage never goes below the ac peak voltage. Hence, the converter never enters the diode rectifier mode. Including the controlled dc current source in the proposed fault current estimation method, gives not only accurate results for branch currents in the faulted line, but also for those located in remote areas of the network as demonstrated by Fig. 4.11(a) and Fig. 4.11(b). The maximum average deviation for the proposed fault current calculation including MMC control compared to EMT-simulation is -0.0315 p.u. Whereas for the basic approximation with simplified MMC modeling, the maximum average deviation is 0.0594 p.u. In Fig. 4.11(c) the voltage at remote MMC 1 is displayed. Including the power and dc voltage control by means of source current vector, the calculated voltage resembles the simulation results with an average deviation of 0.0015 p.u. Similar conclusions can be made for the voltage at MMC 2 in Fig. 4.11(d), which is connected to the faulted line. The analysis presents an average deviation of 0.0082 p.u. In Table 4.9 the average deviation of the proposed improved and basic estimation of the node voltages and branch currents with respect to EMT-simulations is summarized for different fault resistance. It can be concluded that the average accuracy of the proposed analysis is superior for any current or voltage in the grid compared to the basic fault current estimation approach.

Table 4.10 shows the initial branch current and node voltage values for the bipolar dc grid as depicted in Fig. 4.12. Fig. 4.13 demonstrates the accuracy of the proposed method for fault current calculations in bipolar dc grids with P2P faults (Fig. 4.13(a) and Fig. 4.13(b)) and P2N faults (Fig. 4.13(c) and Fig. 4.13(d)). Table 4.11 summarizes the average deviation of

Table 4.9: Average deviation in p.u. of basic and improved (Impr.) estimation with respect to EMT-simulations.

Variable	i_{12}	i_{25}	i_{30}	i_{34}	i_{50}
Basic (0.1 Ω)	−0.0495	−0.0175	−0.0443	0.0594	−0.0175
Impr. (0.1 Ω)	−0.0038	−0.0027	−0.0315	−0.0076	−0.0027
Basic (100 Ω)	−0.0588	0.0264	−0.0418	0.0702	0.0264
Impr. (100 Ω)	−0.0033	−0.0022	−0.0155	−0.0065	−0.0022
Variable	v_{c1}	v_{c2}	v_{c3}	v_{c4}	
Basic (0.1 Ω)	−0.0336	0.0635	−0.0137	0.1290	
Impr. (0.1 Ω)	0.0017	0.0157	0.0190	0.0073	
Basic (100 Ω)	−0.0370	0.0608	−0.0241	−0.1437	
Impr. (100 Ω)	0.0015	0.0082	0.0028	0.0046	

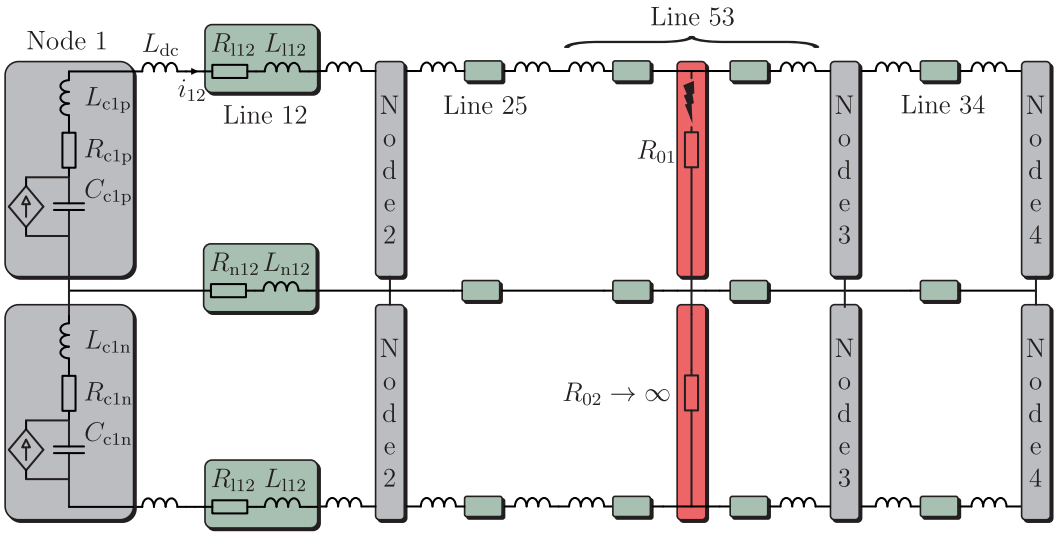


Fig. 4.12: Equivalent circuit model of bipolar CIGRE 4-bus MTdc benchmark grid [162] with pole-to-neutral fault in line 53.

Table 4.10: Initial values of branch currents and node voltages for bipolar dc grid.

Symbols	i_{12} (t=0)	i_{25} (t=0)	i_{30} (t=0)	i_{34} (t=0)	i_{50} (t=0)
Value [kA]	0.498	-0.506	0.506	-0.498	-0.506
Symbols	$v_{c1p,n}$ (t=0)	$v_{c2p,n}$ (t=0)	$v_{c3p,n}$ (t=0)	$v_{c4p,n}$ (t=0)	
Value [kV]	398.53	398.88	399.69	400.44	

bipolar branch current calculation with respect to EMT-simulation results.

The proposed fault current calculation method allows detailed parameter variation analysis in order to provide information for optimal dc CB and protection system design. It is of special interest for the dc CB design to know the fault current dynamic profiles for different grid conditions before grid operation. Critical testing parameters, which are influencing the fault current, are the fault resistance, dc side inductance, converter blocking instant, and fault location [163]. Other parameters, which are not within the scope of this thesis, are

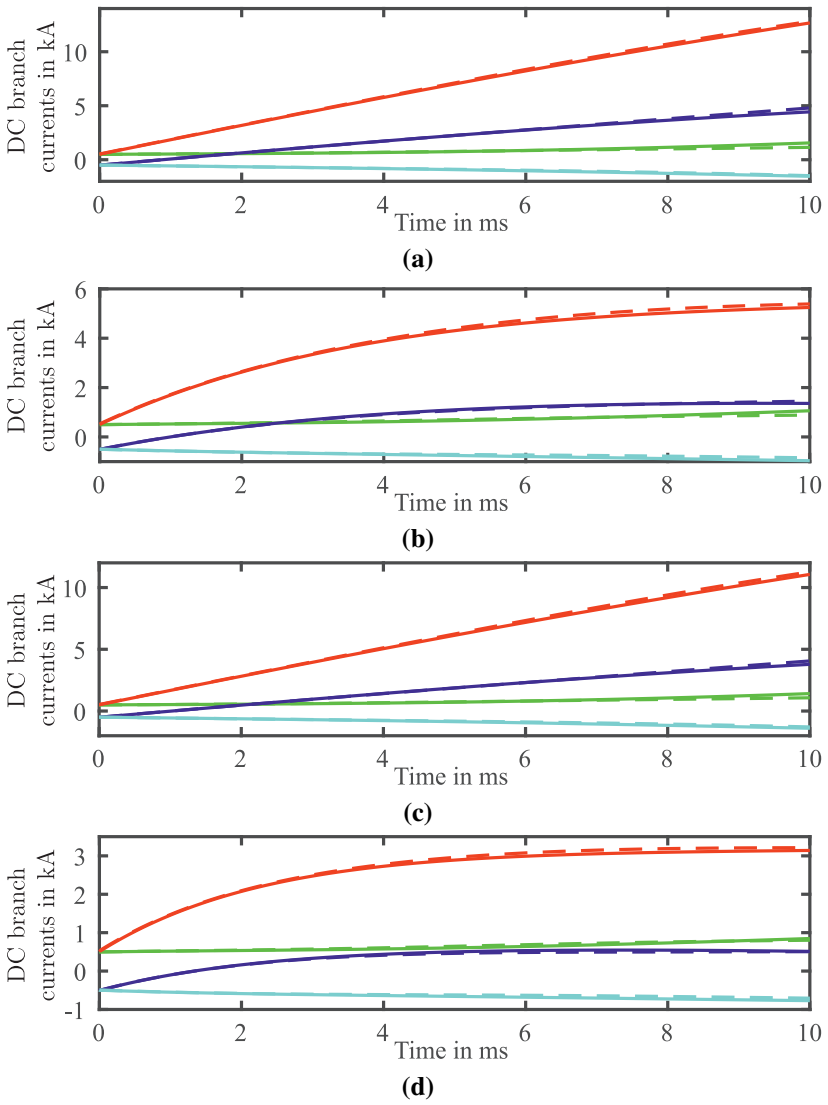


Fig. 4.13: Comparison of dc branch current results (i_{12} (green), i_{30} (red), i_{34} (cyan), i_{50} (blue)) under bipolar P2P and P2N fault with varying fault impedance: (a) P2P $R_0 = 0.1\ \Omega$, (b) P2P $R_0 = 100\ \Omega$, (c) P2N $R_0 = 0.1\ \Omega$, (d) P2N $R_0 = 100\ \Omega$ from presented estimation (solid) and EMT-simulation (dashed).

Table 4.11: Average deviation in p.u. of improved analysis with respect to EMT-simulations for bipolar fault currents.

Variable	i_{12}	i_{25}	i_{30}	i_{34}	i_{50}
P2P (0.1 Ω)	0.0299	−0.0387	−0.0670	0.0159	−0.0387
P2P (100 Ω)	0.0037	−0.0014	−0.0514	−0.0234	−0.0014
P2N (0.1 Ω)	0.0266	−0.0232	−0.0641	−0.0245	−0.0232
P2N (100 Ω)	0.0096	0.0125	−0.0309	−0.0177	−0.0125

the transmission line type (OHL or cable), the dc side capacitance (mostly relevant for 2L-VSC systems), the system earthing (analyzed in [164]), and ac system strength (covered in [165]).

In Fig. 4.14 the fault resistance R_{sc} (which is equal to the node resistance R_0 as explained

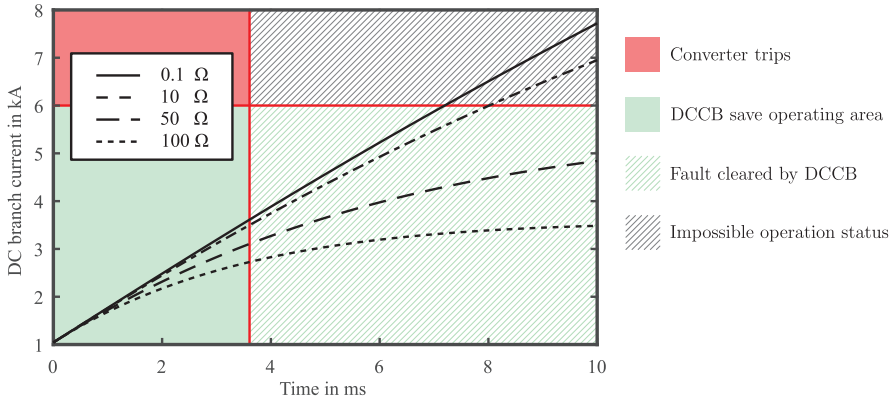


Fig. 4.14: Analytical dc branch current i_{30} with varying fault resistance (Fault at Node 5).

previously) is varied from 0.1 Ω (ideal short circuit) to 100 Ω (high impedance fault) with constant current limiting inductance. Typical high impedance faults can reach values up to 400 Ω [163].

It is visible that the fault current presents an inverted exponential increase, whose damping is proportional to the fault resistance, i.e. an increased resistance in the fault path leads to high damping and hence low maximum fault current.

The current limiting inductance plays an important role in limiting the fault current rise and slowing down the voltage decline in the healthy parts of the grid [34]. In Fig. 4.15 the limiting inductance L_{dc} is varied from 50 mH to 250 mH. It can be noted from Fig. 4.15 that the limiting inductance affects the current derivative. A small inductance lets the current increase fast, which leads to an early converter trip (trip current 6 kA indicated by horizontal red line) after less than 3.2 ms. The dc current limiting inductance does not only limit the fault current rise but also limits the magnitude of the transient voltage wave and hence the discharge of capacitors (of special importance in two or three-level VSC-HVdc systems) and adjacent feeders. This delays a potential converter blocking and makes it possible to keep the power flow longer in operation [41]. The size of the minimum dc current limiting inductor depends on several factors. For example, the IGBT-based hybrid dc CB (as mentioned in Subsection 4.1.2) presents minimum operation times (defined by the sum of detection time and breaking time) of up to 3.5 ms [166] (indicated by vertical red line) and hence, is not able to clear the fault under the assumed condition. It requires an additional current limiting inductor of at least 61.5 mH to operate safely.

In Table 4.12 it is summarized the calculated minimum dc inductance for variations of trip current of the converter (typical values according to [40]), operation time of the dc CB (solid-state (2 ms), IGBT-based hybrid (3.5 ms) and thyristor-based hybrid (5 ms) dc CB, with reference to [166] for typical identification and operation times), and the fault position (end (near the terminal) or beginning (away from terminal) of the line) for ideal short circuit condition. It has to be noted that the minimum dc inductance is only evaluated from the

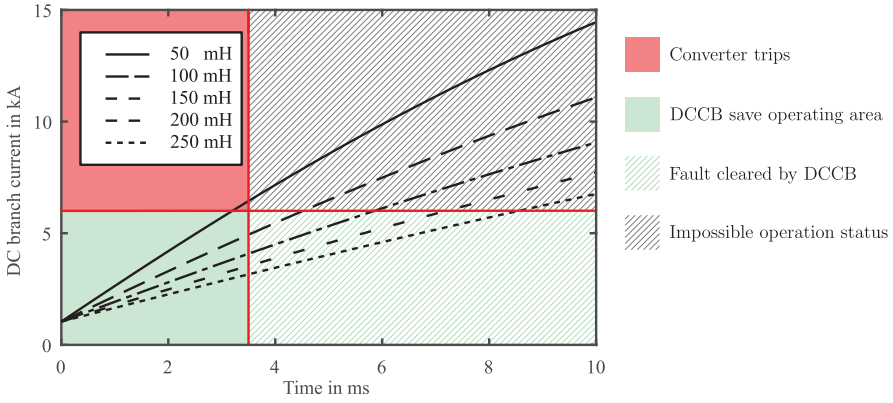


Fig. 4.15: Analytical dc branch current i_{30} with varying fault current limiting inductance L_{dc} (Fault at Node 5).

Table 4.12: Minimum dc inductance calculation with respect to converter trip current, dc CB operation time and fault position.

R_{sc}	i_{trip}	t_{op}	l_{fault}	Minimum L_{dc}
0.1 Ω	4.5 kA	2 ms	beginning	≈ 40 mH
			end	≈ 105 mH
		3.5 ms	beginning	≈ 120 mH
			end	≈ 190 mH
		5 ms	beginning	≈ 205 mH
			end	≈ 275 mH
	6 kA	2 ms	beginning	≈ 5 mH
			end	≈ 70 mH
		3.5 ms	beginning	≈ 62 mH
			end	≈ 129 mH
		5 ms	beginning	≈ 118 mH
			end	≈ 185 mH
	9 kA	2 ms	beginning	-
			end	≈ 40 mH
		3.5 ms	beginning	≈ 10 mH
			end	≈ 75 mH
		5 ms	beginning	≈ 42 mH
			end	≈ 110 mH

protection point of view and not to analyze potential effects on the dc grid stability for large inductance values.

The fault position is varied from a position next to the current limiting reactor at virtual Node 5 until the end of the line at Node 3 with fixed additional dc inductance of 61.5 mH (minimum value obtained from the previous case). Being interposed lower inductance between the fault point and the voltage source, the current i_{30} tends to rise faster at the end of the line than at its beginning. The converter's trip is shifted from 3.5 ms (original position) to 1.78 ms (assuming trip current 6 kA), if the fault is located at the end of the line. It can be seen from Fig. 4.16 that the dc inductance of 61.5 mH is chosen too small in case the fault is located at the end of the line. In this case a minimum dc current limiting inductance of 128.9 mH is necessary for the hybrid dc CB with 3.5 ms operation time (see Table 4.12). The variation of

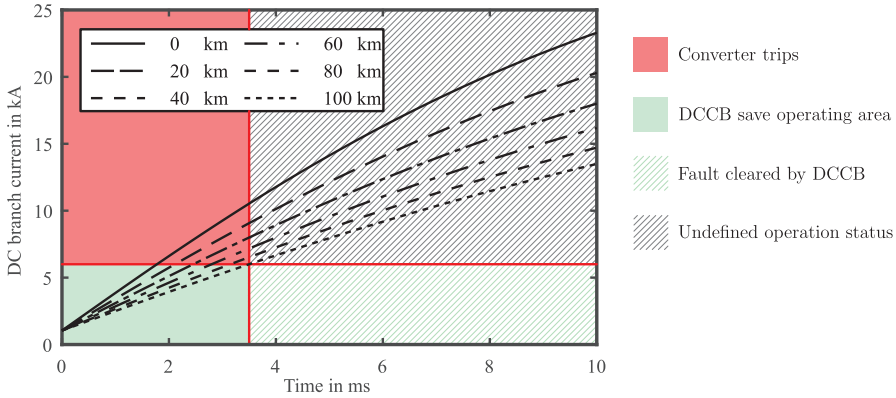


Fig. 4.16: Analytical dc branch current results with varying fault position (with respect to Node 3 (i_{30}).

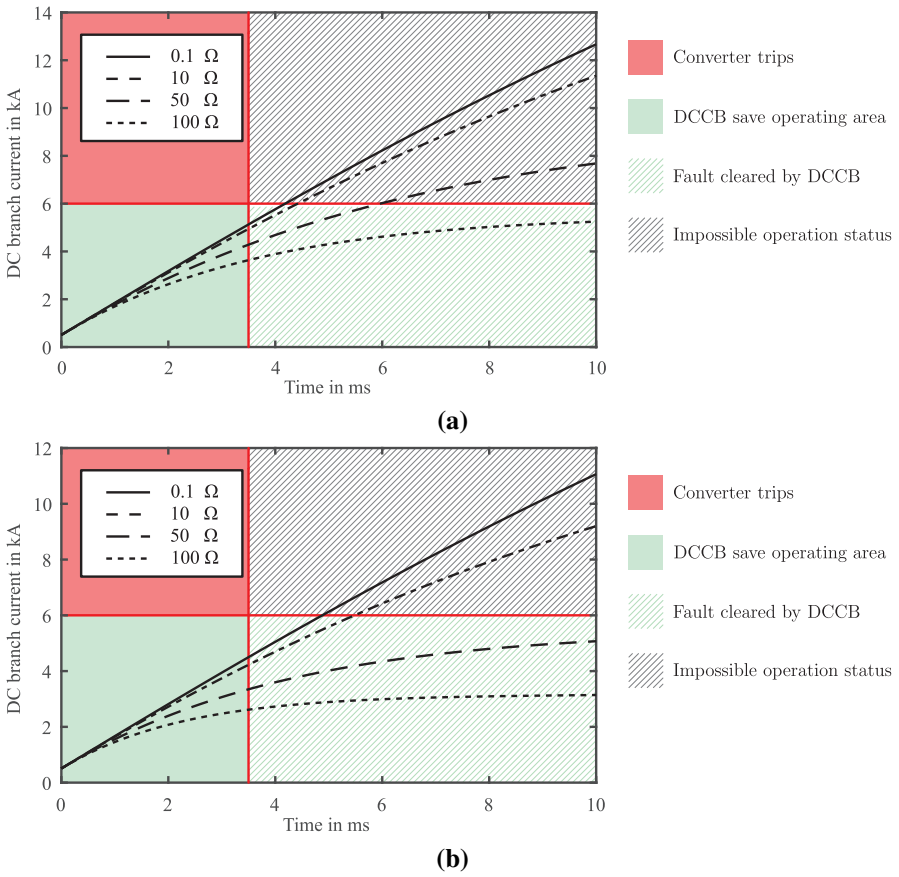


Fig. 4.17: Analytical dc branch current i_{30} with varying fault resistance (Fault at Node 5) in bipolar dc grid: (a) P2P, (b) P2N.

the fault position essentially reflects in changes of the equivalent resistance and inductance in the fault path. Hence, these conclusions could be generalized to variations in the line parameters.

In Fig. 4.17 the influence of fault resistance variation for P2P and P2N faults in the bipolar dc grid is shown. Similar to monopole dc grid, a larger fault resistance increases the fault current damping. As depicted in Fig. 4.17(a), the P2P fault is considered to be more severe and the maximum switch-off current margin of the dc CB is reduced.

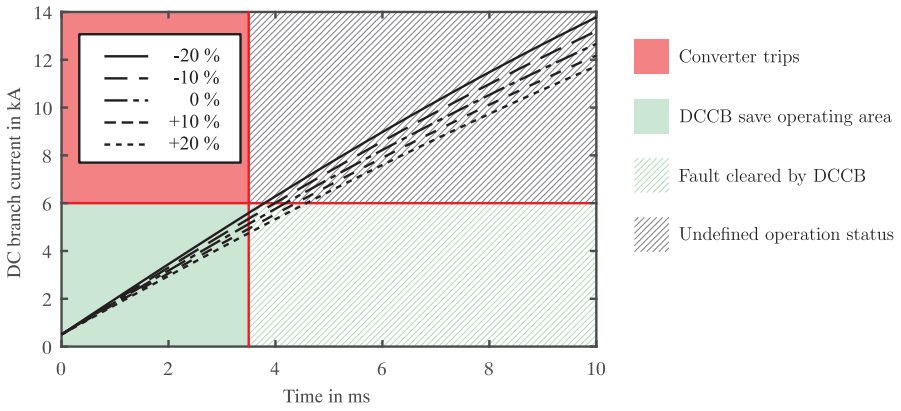


Fig. 4.18: Analytical dc branch current i_{30} with line parameter mismatch of negative pole with respect to positive pole (P2P Fault at Node 5) in bipolar dc grid.

Fig. 4.18 indicates the effects of parameter mismatch between the line parameters of positive and negative pole to study the influence of the healthy pole parameters on the currents in the faulty pole in case of P2P faults. If the healthy pole (here the negative) has reduced line resistance and inductance, the overall mesh resistance and inductance are reduced. Consequently, the current in the faulty pole (here the positive) is exposed to faster current rise and higher fault currents. Hence, the maximum switch-off current margin of the dc CB is reduced. It can be concluded that line parameter variation and mismatch should be considered in the dc CB design.

Similar to the monopole dc grid, minimum required current limiting inductance values can be obtained for the bipolar dc grid with respect to the fault distance to terminal. Faults with large distance to terminal require minimum inductance of 103.6 mH for P2N and 152.5 mH for P2P faults, respectively. The worst case scenario with ideal short circuit at the voltage controlling terminal requires a minimum inductance of 218.9 mH for both fault types. These example values are obtained for ideal short circuit and the use case of modular IGBT-based hybrid dc CB (i.e. operation time of 3.5 ms) and converter trip current level of 6 kA.

4.4. Fault identification and adaptive auto-reclosing with modular dc circuit breaker

In HVdc systems, despite the fault clearing process, the reclose or restart function after a temporary fault happened is important. A fast restoration improves the ac power system stability and transmission continuity. Since overhead transmission line systems are directly exposed to atmospheric conditions, those systems are more prone to temporary faults. In conventional operation, the reclosing process involves a fixed dead time and the same strategy is applied to permanent and temporary faults. However, a reclosing attempt on a permanent fault results in a restrike of the arc with additional energy brought in the insulation path, which delays the power flow recovery requesting a second auto-reclosing sequence [45].

Recently, adaptive auto-reclosing strategies have gained interest, which are based on a previous identification of the fault type - permanent or temporary - and hence the reclosing operation is only initiated, if the arc is sufficiently deionized. This topic has been recently investigated in MMC-HVdc systems.

In [45], an adaptive auto-reclosing concept has been introduced for single P2G faults. The system is based on full-bridge MMCs, which are controlled to force the current to zero to interrupt the fault. After the fault interruption, a small sinusoidal test current is injected by the grounded converter into the HVdc grid and the system's voltage response is recorded to identify the fault type. However, this concept requires knowledge of the arc hysteresis, since the arc extinction is captured by the voltage waveform, which depends on the nonlinear arc shape.

In [46], an adaptive auto-reclosing scheme has been proposed for HVdc systems with hybrid MMCs. After detection of a P2G fault, the converter is controlled to inject dc voltage perturbations in the healthy pole, which in turn induces characteristic signals in the faulty pole, from which the fault type can be identified. This concept requires an MMC with bipolar submodules, which can change the polarity of the dc output voltage. Suddenly changing the voltage polarity in some modules will change the dc voltage in the healthy pole and in consequence, will create a current pulse injection in the faulty pole. The pulse wave travels along the faulty line and from its refraction and reflection pattern both the fault type and fault location can be found with wavelet transformation. However, this concept is not applicable to HB-MMC-based HVdc systems and is limited to bipolar systems.

Instead, the authors of [47] propose to use the HB-MMC in combination with the hybrid dc CB with full-bridge SM (Hybrid 2). After the fault current interruption, the breaker remains connected to the MMC, which - after a fixed delay time - synthesizes the nominal dc voltage. Bypassing a certain number of full-bridge SM in the dc CB, voltage pulses are actively generated. The drawback of this topology is the high number of IGBTs and the requirement of safe discharging of the SM capacitors during active pulse generation and auto-reclosing mode.

In [167], the modular structure of a hybrid dc CB is employed to perform sequential auto-reclosing in a point-to-point HVdc system. However, the auto-reclosing process is non-adaptive as a fixed delay time of $200 - 500$ ms is applied before the breaker is sequentially closed. During the reclosing sequence, the line voltage is continuously monitored to identify whether the fault is permanent or temporary. If the dc voltage rebuilds to close to nominal value within a predefined time, the fault is assumed to be cleared. This approach impacts on the ac grid, if the fault is permanent and due to the fixed delay time, the fast reclosing and power recovery is impeded.

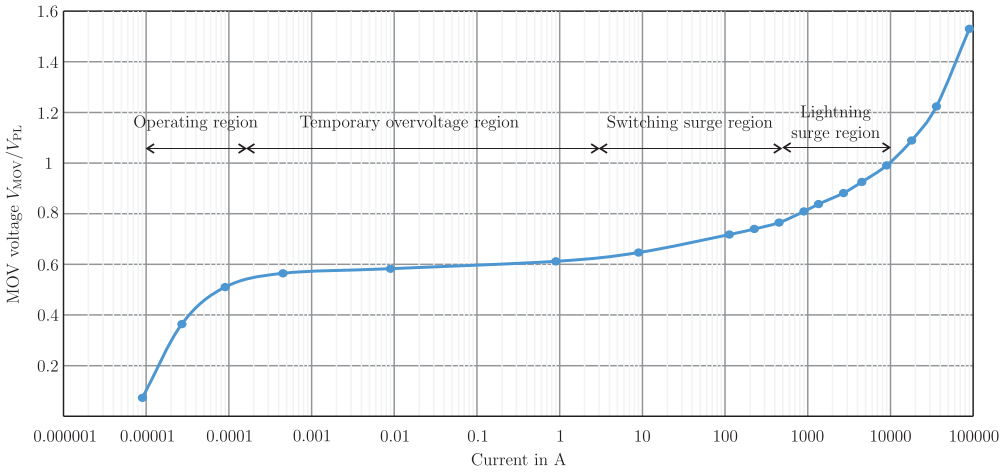


Fig. 4.19: Characteristic metal oxide varistor voltage-current curve obtained from [169].

A combination of MMC with bipolar submodules and hybrid dc CB is applied for adaptive auto-reclosing in [168]. During the short pulse generation period, the MMC is operated at a voltage lower than the nominal dc voltage and the main breaker path of the hybrid dc CB is turned on for a short time to provide a conduction path for the generated active pulses. The fault type is identified by analyzing the reflection and refraction coefficients of the traveling waves. However, to reduce the dc voltage temporarily, full-bridge topology of the MMC would be required, making the system expensive and complex. Moreover, this concept requires fast control of MMC and dc CB and communication between the two.

In contrast to the methods described above, in this work the unidirectional modular hybrid dc CB as introduced by ABB is employed at each end of the HVdc transmission line to provide fully selective fault interruption and to inject the active dc voltage pulses after fault current interruption and arc extinction. The proposed method can be applied to HVdc systems with half-bridge MMC as neither fault clearing capability nor bidirectional dc voltage controllability in the MMC are required. The method will be tested for P2P faults in a symmetrical monopole HVdc grid configuration.

To understand how the active pulses are generated with the modular hybrid dc CB, at first, one has to understand the structure of the breaker and the conduction behavior of the MOV.

The commutation path in the modular hybrid dc circuit breaker consists of n series connected modules. Each module is a combination of IGBTs and anti-parallel diodes as main breaker and MOV in parallel for energy absorption and voltage clamping purposes.

The MOV is a non-linear voltage dependent resistor, whose impedance curve (Fig. 4.19) can be divided in four different operating zones depending on the actual MOV voltage level [169]. In the normal operating region, the MOV has very high impedance and hence very low conduction. Above a critical voltage (so called temporary over-voltage region) the MOV is conducting. At the new operating point the behavior of MOVs is equivalent to a dc voltage

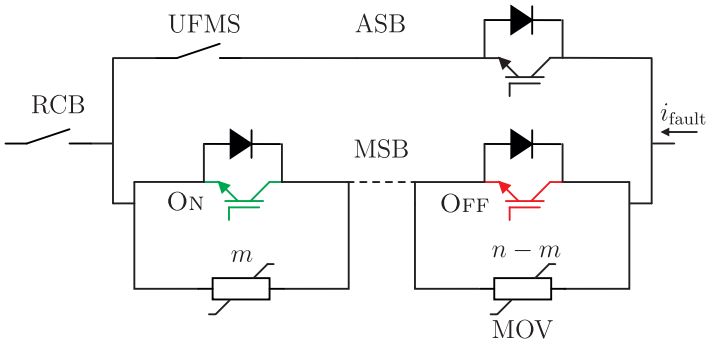


Fig. 4.20: Unidirectional hybrid dc CB: MSB switching states during the pulse injection period.

source in series with a low resistance. The following regions are switching surge region, in which the MOV can only remain few milliseconds, and lightning surge region with very high conduction in the µ*s*-range.

As starting point, it is assumed that after switching off the breaker to interrupt the fault current, the dc voltage V_{dc} is equally distributed among the n_{MOV} series connected MOVs in the breaker. In the proposed adaptive auto-reclosing method, after fault current interruption and extinction of the primary arc, a specified number of modules m_{MOV} are bypassed in the hybrid dc CB (e.g. 30%) by turning the respective IGBTs on (see Fig. 4.20). In consequence, the voltage in the remaining MOVs will increase and the operating point is shifted towards the temporary over-voltage region. Neglecting the MOVs dynamic effects, the MOV behaves in this region similar to a dc source with low series resistance. The parameters of the equivalent MOV model are obtained from the piecewise linear approximation of the MOV impedance curve. The resulting voltage difference between the MMC dc-link and the equivalent voltage of the remaining MOVs is applied as dc voltage pulse in the line ended after a short delay (equivalent to the desired pulse width, e.g. 100 µs) by the switch-off of all breaker modules. For redundancy purposes the pulse generation is repeated three times with a time delay of 15 ms between the attempts.

It should be noted that prior to the active pulse injection, a fixed waiting time, generally several tens of ms (here 50 ms), is considered to ensure that the temperature of the dielectric gas has reduced and hence to lower the risk for insulation failure and re-strike of the arc. However, that delay time is much shorter than in the conventional auto-reclosing process without fault identification.

To demonstrate the pulse injection principle with modular hybrid dc CB, a simplified model (as shown in Fig. 4.21) can be used, in which the short circuit is modeled with small resistance R_{sc}, the MMC with a constant dc voltage source, and the transmission line with frequency-dependent model with corresponding lumped parameters R_{line}, L_{line}, and C_{line}. After bypassing m_{MOV} modules of the modular hybrid dc CB, the voltage difference between the MMC and the breaker' MOVs will generate a voltage pulse with the amplitude

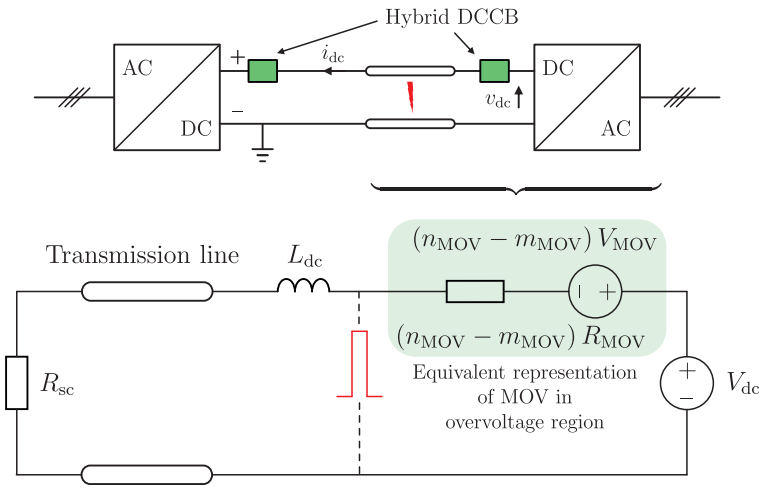


Fig. 4.21: Equivalent circuit of HB-MMC-HVdc system with hybrid dc CB during the pulse injection period after a pole-to-pole fault.

depending on the number of bypassed modules

$$v_{pulse} = v_{dc} - (n_{MOV} - m_{MOV})\, v_{MOV} \quad , \tag{4.56}$$

and the pulse duration controlled by the bypass period. The voltage of the MOV v_{MOV} can be extracted from the piecewise linear approximation of the arrester curve.

As a consequence of the voltage pulse, a current pulse is developed, which travels along the line as well. To identify the fault type - permanent or temporary - either the current wave (and its reflected wave) or the voltage wave (and its reflected wave) at the sending end can be analyzed by means of traveling wave analysis [168].

The injected voltage pulse is propagating along the faulted line. It is assumed a fault at any arbitrary point x at the transmission line between the sending and the receiving end, which forms a physical boundary to the injected voltage pulse. Following traveling wave theory, at the fault point the injected voltage wave will be partially reflected (back to the sending end) and refracted (forward to the receiving end). The reflected and refracted waves can be expressed with reflection coefficient

$$\xi = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{4.57}$$

and refraction coefficient

$$\zeta = \frac{2Z_2}{Z_2 + Z_1} \quad , \tag{4.58}$$

with Z_1 being the equivalent wave impedance of the transmission line, where the traveling wave first propagates, and Z_2 being the equivalent wave impedance of the transmission line, where the traveling wave reflects and refracts. Considering Z_l as the wave impedance of the transmission line and a permanent fault with fault impedance R_{sc}, the reflection coefficient

at the fault point can be found with

$$\xi_{\mathrm{x}} = \frac{R_{\mathrm{sc}} \parallel Z_{\mathrm{l}} - Z_{\mathrm{l}}}{R_{\mathrm{sc}} \parallel Z_{\mathrm{l}} + Z_{\mathrm{l}}} \tag{4.59}$$

and the refraction coefficient with

$$\zeta_{\mathrm{x}} = \frac{2\,(R_{\mathrm{sc}} \parallel Z_{\mathrm{l}})}{R_{\mathrm{sc}} \parallel Z_{\mathrm{l}} + Z_{\mathrm{l}}} \quad . \tag{4.60}$$

In general, the fault resistance can be assumed much smaller than the equivalent line impedance, resulting in $R_{\mathrm{sc}} \parallel Z_{\mathrm{l}} < Z_{\mathrm{l}}$. Thus, in the permanent fault case, the reflection coefficient is negative. The first reflected voltage pulse at the sending end is proportional to $2\xi_{\mathrm{x}}$. Consequently, the sign of the first reflected voltage pulse is also negative for permanent faults. The following pulses have alternating signs, i.e. positive, negative, positive. For temporary faults, on the other hand, the injected voltage pulse is not reflected at the fault position and is traveling to the receiving end, where the opened hybrid dc CB forms a high impedance, leading to $Z_2 \rightarrow \infty$ and hence $\xi_{\mathrm{receiv}} = 1$. The first reflected voltage pulse is proportional to $2\xi_{\mathrm{receiv}}$ and hence positive. Since the breaker at the sending end is also opened, the reflection at the sending end is positive and consequently, all following detected pulses are also positive in sign.

For redundancy purposes the pulse injection will be performed three times with a certain delay between the attempts. If the fault is identified as a permanent one, the residual breaker will be opened and the auto-reclosing will not be initiated. On the other hand, for a temporary fault, the auto-reclosing sequence will be completed by increasing the dc voltage gradually and finally closing the UFMS and the ASB to re-establish the active power transmission. The modular design of the hybrid dc CB allows to sequentially bypass the breaker modules with a fixed time interval, e.g. 5 ms and hence to gradually build-up the dc voltage.

The proposed method is verified with two PSCAD/EMTDC simulations of temporary and permanent dc fault cases. The system under study is a 150 kV, 150 MW symmetrical monopole point-to-point HVdc system (parameters in Table 4.13), where only a single end converter is fully represented (i.e. switch level) and the other end converter is modeled with a resistance. As it is common for MMC studies, the number of SM represented in the converter switching model is limited to 10 SM per arm in order to increase the simulation speed. The hybrid dc CB breaker is assumed to be made of $n_{\mathrm{MOV}} = 25$ series main breaker modules with parallel connected MOV. The transmission line is modeled with a frequency-dependent line model, of which the corresponding lumped parameters are given in Table 4.13.

In the first case, a temporary fault at $t = 0.1$ s is assumed, which is removed at $t = 0.104$ s. Three voltage pulses are injected for the fault type identification at time instants $t = 0.15$ s, $t = 0.165$ s, and $t = 0.18$ s (Fig. 4.22). As can be seen from the zoomed view of the dc line

Table 4.13: Parameters of the MMC-HVdc system under study (Base voltage $V_b = 150$ kV, base power $P_b = 150$ MW).

Quantity	Symbol	Value	Converter *per unit* Value
Nominal power	P_{nom}	150 MW	1 p.u.
Peak phase voltage	$\hat{v}_{ac}$	66 kV	0.44 p.u.
Nominal dc voltage	V_{dc}	150 kV	1 p.u.
Nominal dc line current	I_{dc}	1 kA	1 p.u.
Number of SM per arm	n_{SM}	10	
Nominal MMC SM voltage	V_{SM}	15 kV	
SM capacitance	C_{SM}	1 mF	0.021 p.u.
Arm inductance	L_{arm}	10 mH	0.021 p.u.
Arm resistance	R_{arm}	10 mΩ	0.000067 p.u.
DC current limiting inductance	L_{dc}	50 mH	0.105 p.u.
Fault resistance	R_{sc}	20 Ω	
Number of total dc CB modules	n_{MOV}	25	
Number of bypassed dc CB modules	m_{MOV}	9	
Arrester protection voltage level	V_{PL}	9.5 kV	
Line inductance	l_{line}	0.945 mH/km	
Line resistance	r_{line}	0.0066 Ω/km	
Line capacitance	c_{line}	0.0122 μF/km	

voltage in Fig. 4.23, the sign of the first reflected voltage pulse (and also all following ones) is positive, which indicates the temporary fault. The same conclusion can be drawn from the line current plot, since due to the high terminal resistance of the open dc CB at the receiving end no reflected current pulse is expected (and can be captured) at the sending end. After the successful fault type identification, at $t = 0.21$ s, the voltage is gradually build-up by sequentially closing the breaker modules and at $t = 0.35$ s the active power transmission is restored.

Fig. 4.24 demonstrates the system behavior under permanent fault case. Again, three active voltage pulses are generated to distinguish between temporary and permanent faults. The first reflected pulse of the line voltage wave is negative (and the following are alternating in sign) as can be seen in Fig. 4.25. Hence, the fault is identified as a permanent one and the residual breaker will be closed to isolate the faulty line.

The injected voltage pulses in Fig. 4.25(b) can be used to locate the fault position in the line. The first voltage reflection is captured at the sending end after approximately $t_1 = 0.33$ ms. Assuming that the traveling waves propagate with the speed of light (i.e. at 300000 km/s), the fault is located at

$$x_{fault} = \frac{t_1 \cdot 300000\,\text{km/s}}{2} = 50\,\text{km} \tag{4.61}$$

away from the sending end converter.

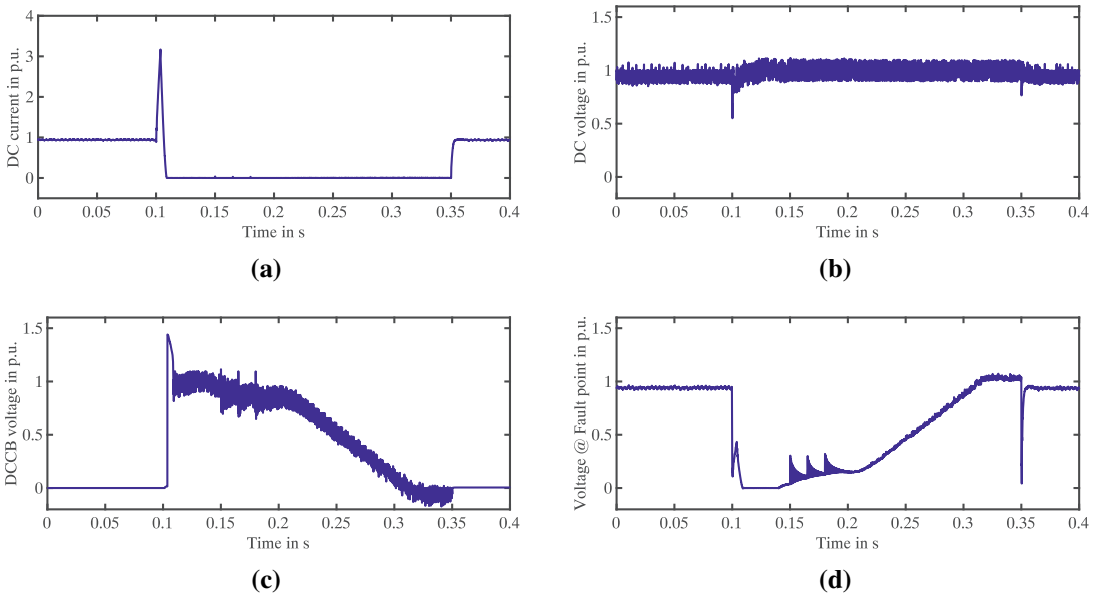


Fig. 4.22: Fault identification with active pulse injection by modular hybrid dc CB in temporary fault case: (a) DC current, (b) DC voltage, (c) DCCB voltage, (d) DC voltage @ fault point.

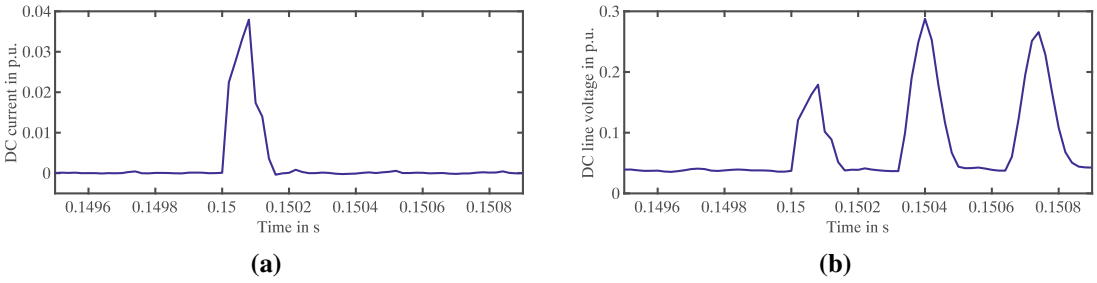


Fig. 4.23: Temporary faults: Zoom on first active pulse injection: (a) DC current, (b) DC line voltage.

4.5. Summary and conclusions of the section

In this section, design criteria for HVdc circuit breaker and analytical fault current estimation to evaluate such criteria in multi-terminal HVdc systems have been presented. The presented fault current estimation method is based on coupled linear differential equations and the modified average value model of the MMC, which allows to include the power flow through during the fault time and hence provides more accurate results for both terminal voltages and branch currents in the estimation, which has been validated with EMTDC simulations in PSCAD environment. This is of special importance, since in MTdc systems remote branch currents must be also known to properly design the overall protection system. Due to their technological readiness and simultaneous vulnerability against short circuit faults, the presented method concentrates on overhead transmission line HVdc systems, while the necessary adaptions to cable systems are presented in short and should be elaborated on in the future.

The analytical estimation offers the possibility to analyze a large set of grid parameters with

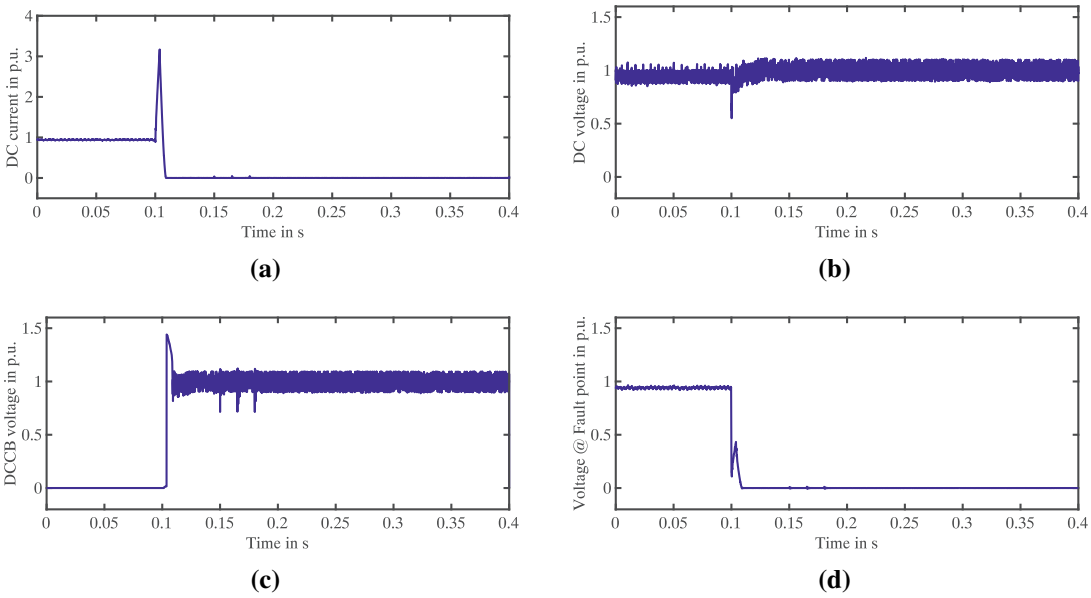


Fig. 4.24: Fault identification with active pulse injection by modular hybrid dc CB in permanent fault case: (a) DC current, (b) DC voltage, (c) DCCB voltage, (d) DC voltage @ fault point.

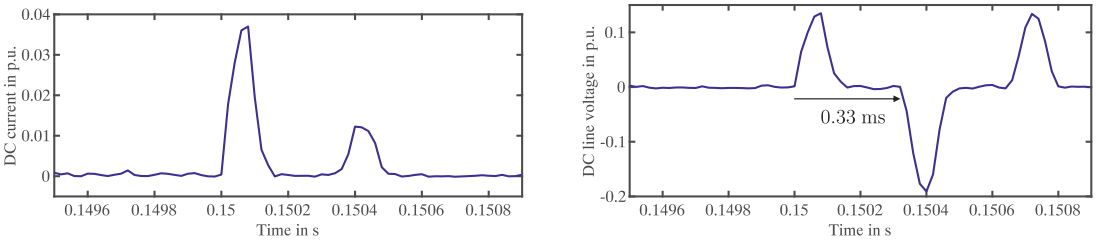


Fig. 4.25: Permanent faults: Zoom on first active pulse injection: (a) DC current, (b) DC line voltage.

limited computational effort. Main factors, which influence the dc CB design and determine its suitability to clear a fault under the given assumptions, such as fault resistance, fault location, breaker interruption time, and converter trip current level have been evaluated with the proposed method to determine the minimum required additional dc current limiting inductance. Other potential influencing factors are the MMC design and the maximum allowed current derivative, which can be included in future use cases.

As a possible extension of the presented work, the set of analytical differential equations could be reduced to a certain order by applying Taylor expansion to provide analytical expressions for the influence of certain system parameters. In this work P2P faults in symmetrical monopole and P2P and P2N in bipolar MTdc grids have been analyzed. In the future, the possible extension of the presented method to other fault scenarios should be evaluated, such as P2G faults in bipolar HVdc. Moreover, the method could form a basis for a holistic protection system design, i.e. providing individual designs for each breaker based on the system configuration.

Another focus is given to the modular hybrid dc CB, which is seen as a key technology for future MTdc grids, because of its good cost-fault-clearing-performance trade-off. In this work, the modular hybrid dc CB is further used to identify the fault type - permanent or temporary - after the fault interruption. The concept is based on active pulse injection by switching on and off a certain number of breaker modules and afterward analyzing the traveling wave reflection (either voltage or current). This enables adaptive auto-reclosing to limit the system's downtime after the fault and also the location of a permanent fault. To demonstrate the concept, EMTDC simulations in PSCAD environment of MMC and the hybrid dc CB are carried out.

5. Modular multilevel converter-based HVdc protection

A possible protection methodology in HVdc systems is to embed the dc fault blocking in the converter station. To achieve the fault blocking function, the MMC must provide reverse-biased voltage in the blocked state in order to prevent currents flowing uncontrolled from the ac to the dc side. In the following, starting from the drawbacks of conventional half-bridge SM, first an overview on different SM types for MMC with fault blocking capability is given. The SM have to account for the trade-off in the production of sufficient counter-emf in the MMC arms during the fault to reduce the fault current and the on-state losses in normal operating state. Then, different MMC architectures, which ensure fault blocking with increased efficiency by employing a mixture of bipolar or asymmetric SM together with the conventional half-bridge SM (HBSM) are analyzed, namely the hybrid MMC (HMMC), the hybrid arm MMC (HA-MMC), and the alternate arm converter (AAC).

This section contributes to the state of the art research by putting a new perspective on the HAMMC design with reduced number of bipolar SM, which is optimized in terms of on-state losses. The minimum number of SM to produce sufficient counter-emf will be derived analytically from the fault operational sequence of the HAMMC as well as the SM capacitor over-voltage during the fault clearing process. The HAMMC with reduced number of bipolar SM will be compared to other MMC architectures with fault blocking capability in terms of interruption time, over-voltage, and power losses. The results are verified with time-domain PSCAD/EMTDC simulations of the MMC represented with a full switching model.

5.1. Submodule types for MMC

5.1.1. Submodule types for MMC without fault blocking capability

Conventionally, HBSM (as shown in Fig. 5.1) are adopted in MMC, which are able to produce two output voltage levels for the normal operation of the MMC with minimum number of power semiconductor devices. In fact, only two complementary active switches are used in each HBSM together with one dc capacitor and hence, the power losses and costs of HBSM-MMC are comparatively low. The HBSM is a unipolar SM, which has three different switching states, namely the active, bypassed, and blocked state (Table 5.1). In the active state, the switch S_1 is ON and the switch S_2 is OFF. Depending on the arm current direction, the SM capacitor is charged (positive current) or discharged (negative current), while the SM output voltage in both cases is the positive SM capacitor voltage V_{SM}. To bypass the SM, i.e. to generate zero SM output voltage, the switch S_1 is OFF and the switch S_2 is ON. In the blocked state, both active switches are turned OFF [49].

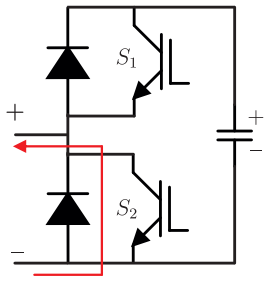


Fig. 5.1: Topology and fault current path of HBSM.

Table 5.1: Switching states of HBSM.

State	S_1	S_2	v_o	Capacitor	
				$i_{SM} > 0$	$i_{SM} < 0$
Active	ON	OFF	V_{SM}	Charging	Discharging
Bypassed	OFF	ON	0	-	-
Blocked	OFF	OFF	-	-	-

However, an MMC based on HBSM is vulnerable to dc side faults (e.g. P2G or P2P) in HVdc systems. In fact, the HBSM is not capable of producing a negative voltage in blocked state (see switching states in Table 5.1). Thus, in case of dc voltage collapse, the HBSM-MMC behaves as an uncontrolled diode rectifier feeding the dc fault point from the ac side, which leads to excessive currents flowing through the anti-parallel diodes and the converter arms (see Fig. 5.1), potentially causing failure of the devices [66, 49]. Hence, additional dc CB (see Section 4) are required to selectively interrupt the dc fault current and prevent - in the multi-terminal case - the whole system from blackout. If the HVdc system, as it is feasible for point-to-point HVdc links, is protected with conventional ac CB, the HBSM-MMC must be equipped with bypass thyristors in the SM to protect the freewheeling diodes from over-current in blocked state of the MMC, until the ac CB is fully open [49].

In order to further increase the ac waveform quality (smaller voltage ripple) as compared to HBSM, unipolar three-level SM, such as the flying-capacitor submodule (FCSM, Fig. 5.2(a)) or the neutral-point clamped submodule (NPCSM, Fig. 5.2(b)) can be used. This kind of SM has three output voltage levels: 0 V in the bypassed state and V_{SM}, and $2V_{SM}$ in the active states (Table 5.2 and Table 5.3). To generate the three-level output voltage, the inner capacitor voltage $V_{c2} = V_{SM}$ in the FCSM should be balanced to half of the voltage of the outer capacitor $V_{c1} = 2V_{SM}$, while in the NPCSM both capacitor voltages should be equal $V_{c1} = V_{c2} = V_{SM}$ [48]. While the FCSM has the advantage of offering lower circulating current than the HBSM, similar to the HBSM, both three-level structures do not provide any dc fault blocking capability, but are more expensive, need more complex control, and employ a higher number of components per SM and hence, are not very attractive from the manufacturing point of view [48, 170]. The NPCSM also suffers from the neutral point voltage balancing problem [48].

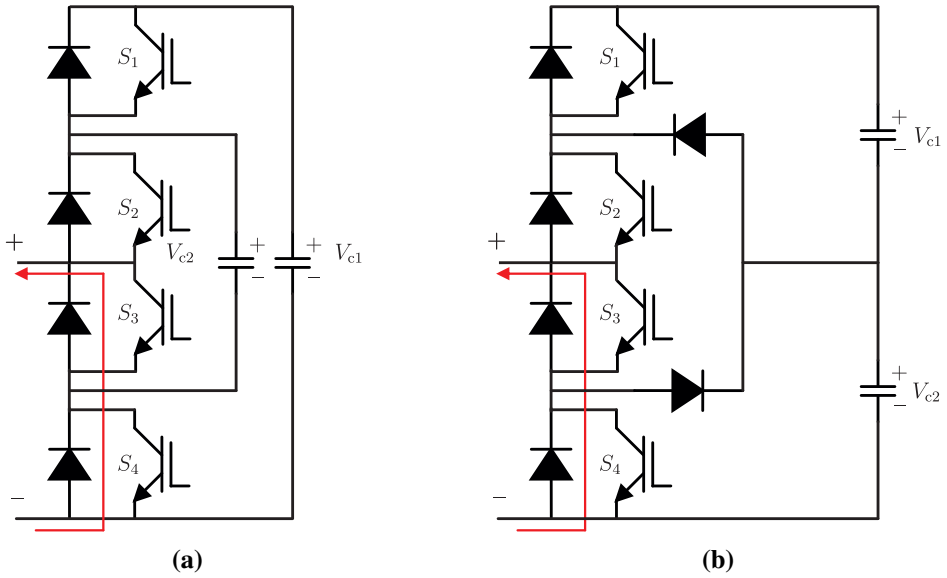


Fig. 5.2: Topology and fault current path of three-level SM without fault blocking capability: (a) FCSM, (b) NPCSM.

Table 5.2: Switching states of FCSM.

State	S_1	S_2	S_3	S_4	v_o	Capacitor	
						$i_{SM} > 0$	$i_{SM} < 0$
Active	ON	ON	OFF	OFF	$2V_{SM}$	C_1 Charging	C_1 Discharging
Active	OFF	ON	OFF	ON	V_{SM}	C_2 Charging	C_2 Discharging
Active	ON	OFF	ON	OFF	V_{SM}	C_1 Charging C_2 Discharging	C_1 Discharging C_2 Charging
Bypassed	OFF	OFF	ON	ON	0	-	-

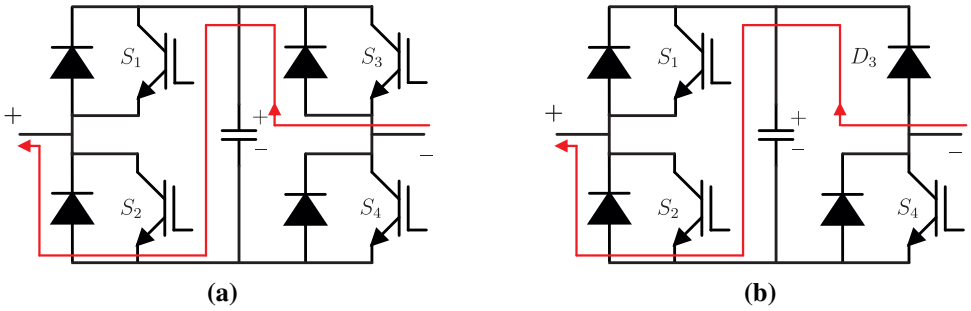
Table 5.3: Switching states of NPCSM.

State	S_1	S_2	S_3	S_4	v_o	Capacitor	
						$i_{SM} > 0$	$i_{SM} < 0$
Active	ON	ON	OFF	OFF	$2V_{SM}$	C_1 Charging C_2 Charging	C_1 Discharging C_2 Discharging
Active	OFF	ON	ON	OFF	V_{SM}	C_2 Charging	C_2 Discharging
-	ON	OFF	OFF	ON	-	-	-
Bypassed	OFF	OFF	ON	ON	0	-	-

5.1.2. Submodule types for MMC with fault blocking capability

This subsection aims to introduce the MMC submodule types and operational behavior suitable for dc fault current blocking.

Full-bridge submodule The most common SM type with fault blocking capability is the full-bridge submodule (FBSM) [50]. Essentially, it is a connection of two HBSM on the dc side with only one SM capacitor (Fig. 5.3(a)). The SM output terminals are the two half-bridge midpoints.



(a) (b)

Fig. 5.3: Topology and fault current path of full-bridge SM: (a) (Bipolar voltage) FBSM, (b) Unipolar voltage FBSM.

Table 5.4: Switching states of FBSM.

State	S_1	S_2	S_3	S_4	v_o	Capacitor	
						$i_{SM} > 0$	$i_{SM} < 0$
Active	ON	OFF	OFF	ON	V_{SM}	Charging	Discharging
Active	OFF	ON	ON	OFF	$-V_{SM}$	Discharging	Charging
Bypassed	ON	OFF	ON	OFF	0	-	-
Bypassed	OFF	ON	OFF	ON	0	-	-
Blocked ($i_{SM} < 0$)	OFF	OFF	OFF	OFF	$-V_{SM}$		Charging

The FBSM is able to produce three output voltage levels, namely $-V_{SM}$ and V_{SM} in the active state and 0 in the two bypassed states (Table 5.4). The redundant states can be used to equally distribute the power losses between the switches S_3 and S_4 [48]. The bipolar output voltage of the FBSM in normal operation, allows to operate the MMC in over-modulation range, i.e. at higher ac voltage for a given nominal dc voltage (also referred to as boost-type inverter mode), and in buck-type rectifier mode, i.e. at dc voltage lower than the total arm voltage [171]. Additionally, the FBSM offers smaller capacitor voltage ripple as compared to HBSM based MMC. The main drawback of the FBSM is the doubled number of semiconductors as compared to the HBSM and hence almost doubled losses and costs [49].

The FBSM topology in Fig. 5.3(a) demonstrates that by deactivating the IGBTs (blocked state) the FBSM can provide full reverse-biased voltage (i.e. $-V_{SM}$) in the fault current path to decay the fault currents and finally block them, if the total reverse-biased voltage is sufficiently high to block the conduction of freewheeling diodes [7]. In fact, inserting the capacitors with negative polarity in the fault path will let them be charged by the fault currents, so that the stored energy in the dc and arm inductances will be shifted to the capacitors and the currents in the arms decay to zero without the need for additional arresters [7].

Unipolar voltage full-bridge submodule Fig. 5.3(b) shows the topology of the unipolar voltage full-bridge submodule (U-FBSM), which is derived from the FBSM by replacing the active switch (IGBT) S_3 and its anti-parallel diode by the diode D_3 [49].

Table 5.5: Switching states of U-FBSM.

State	S_1	S_2	S_4	i_{SM}	v_o	Capacitor
Active	ON	OFF	ON	>0	V_{SM}	Charging
Active	ON	OFF	ON	<0	V_{SM}	Discharging
Bypassed	OFF	ON	ON	both	0	-
Blocked	OFF	OFF	OFF	>0	V_{SM}	Charging
Blocked	OFF	OFF	OFF	<0	$-V_{SM}$	Charging
Active	ON	OFF	OFF	>0	V_{SM}	Charging
Bypassed	ON	OFF	OFF	<0	0	-
Bypassed	OFF	ON	OFF	>0	0	-
Active	OFF	ON	OFF	<0	V_{SM}	Charging

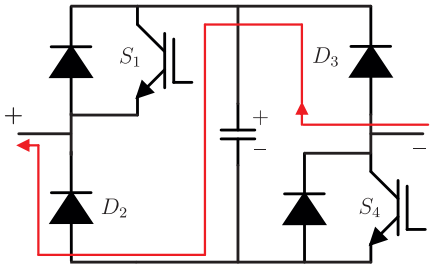


Fig. 5.4: Topology and fault current path of DBSM.

Table 5.6: Switching states of DBSM.

State	S_1	S_2	i_{SM}	v_o	Capacitor
Active	OFF	OFF	$i_{SM}>0$	V_{SM}	Charging
Active	ON	ON	$i_{SM}>0$	$-V_{SM}$	Discharging
Bypassed	ON	OFF	$i_{SM}>0$	0	-
Bypassed	OFF	ON	$i_{SM}>0$	0	-
Blocked	OFF	OFF	$i_{SM}<0$	$-V_{SM}$	Charging

In normal operation, i.e. the first three switching states in Table 5.5, the switch S_4 is always on and the SM capacitor is inserted in the current path or bypassed by controlling the switches S_1 and S_2. Likewise, two different output voltage levels can be achieved, 0 and positive voltage V_{SM}. In comparison with the FBSM, the U-FBSM requires less active switches, however, it is compromised by the higher conduction losses of the switch 4 being always ON.

Under fault condition, i.e. when all active switches are blocked, the U-FBSM behaves in a similar way to the conventional FBSM and, thus, can insert negative voltage in the fault current path and successfully block the dc fault current (see fault current path in Fig. 5.3(b)).

Diagonal bridge SM HVdc systems, which interconnect large power generation facilities, such as offshore wind farms or hydro-power stations, and the load centers, usually transfer bulk power in one main direction and hence can be designed with unidirectional power and current handling capability. In [172], the diagonal bridge submodule (DBSM) has been

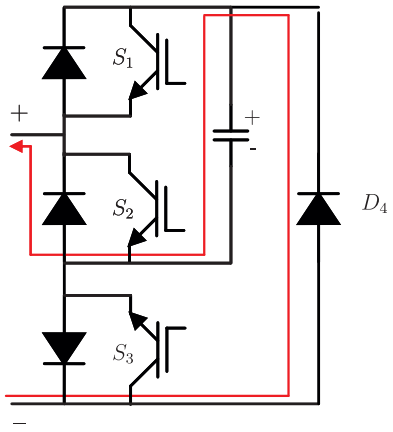


Fig. 5.5: Topology and fault current path of CSSM.

Table 5.7: Switching states of CSSM.

State	S_1	S_2	S_3	i_{SM}	v_o	Capacitor
Active	ON	OFF	ON	> 0	V_{SM}	Charging
Active	ON	OFF	ON	< 0	V_{SM}	Discharging
Bypassed	OFF	ON	ON	both	0	-
Blocked	OFF	OFF	OFF	> 0	V_{SM}	Charging
Blocked	OFF	OFF	OFF	< 0	$-V_{SM}$	Charging

presented for hybrid LCC-MMC HVdc systems for unidirectional power transmission. The DBSM consists of two active switches with anti-parallel diodes and two diagonally placed diodes as shown in Fig. 5.4.

As can be noticed from the switching states in Table 5.6, the DBSM can provide bipolar voltages (inserting the SM capacitor with positive or negative polarity) with unipolar currents (positive in the presented topology at inverter side). A third voltage level is achieved by bypassing the SM capacitor with inverse switch position of the two active switches. In the blocked state, the DBSM behaves similar to the FBSM and offers negative voltage and consequently fault current blocking capability [172].

This SM requires topology modifications depending on its usage in the inverter or rectifier side of the HVdc link. In fact, the positions of active switches and diodes in the diagonal connection must be switched to conduct the reverse current.

Clamp single SM A possibility to include the dc fault current blocking capability in HBSM with comparably low amount of additional costs is the clamp single submodule (CSSM). To provide the current path in blocked state, an additional combination of an active switch and an anti-parallel diode plus one additional diode are included in the CSSM (see Fig. 5.5, [48]).

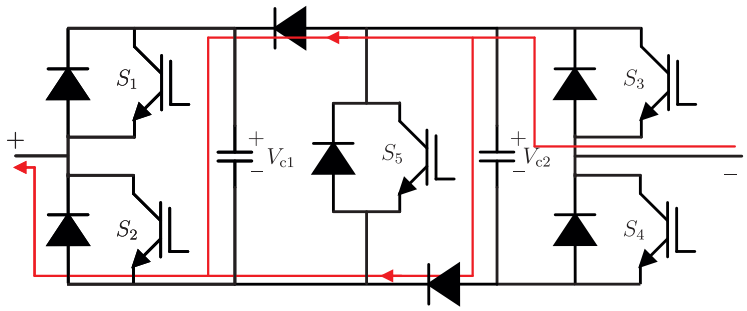


Fig. 5.6: Topology and fault current path of CDSM.

Table 5.8: Switching states of CDSM.

State	S_1	S_2	S_3	S_4	S_5	v_o	Capacitor	
							$i_{SM} > 0$	$i_{SM} < 0$
Bypassed	OFF	ON	ON	OFF	ON	0	-	-
Active	ON	OFF	ON	OFF	ON	V_{SM}	C_1 Charging	C_1 Discharging
Active	OFF	ON	OFF	ON	ON	V_{SM}	C_2 Charging	C_2 Discharging
Active	ON	OFF	OFF	ON	ON	$2V_{SM}$	C_1 Charging C_2 Charging	C_1 Discharging C_2 Discharging
Blocked ($i_{SM} > 0$)	OFF	OFF	OFF	OFF	OFF	$2V_{SM}$	C_1 Charging C_2 Charging	
Blocked ($i_{SM} < 0$)	OFF	OFF	OFF	OFF	OFF	$-V_{SM}$		C_1 Charging C_2 Charging

In normal operation, the CSSM can generate unipolar output voltage with voltage levels 0 (in bypassed state) and V_{SM} in active state, with the switch S_3 being always ON (see Table 5.7).

In blocked state, if all active switches are turned OFF, regardless of the current direction only two diodes are actively conducting the current and hence the SM voltage is always inserted in reverse direction to the current path (e.g. negative output voltage polarity to block the ac in-feed to dc side faults). Thus, this SM topology is a good candidate for hybrid MMC architectures, in which it is combined with other types of SM [173].

Its reduced overall power losses can be seen as a key advantage of the CSSM. In comparison with the FBSM, always having the switch S_3 ON, offers lower switching losses. The number of devices (active switch or diode) in the current path is the same as in the FBSM at any switching state, even with the switch S_3 always ON. Consequently, if similar conduction losses for active switches and diodes are assumed, the total conduction losses of the CSSM are equivalent to those in the FBSM and the overall losses of the CSSM are lower [48].

Clamp double SM The clamp double submodule (CDSM) as proposed in [50] connects two consecutive HBSM in series by use of one additional active switch S_5 with anti-parallel diode, which is always ON in normal operation. To clamp the SM capacitor voltage under blocked (i.e. fault) condition and provide reverse-biased voltage (negative polarity for current flowing from ac to dc side of the MMC), two additional diodes are included (Fig. 5.6).

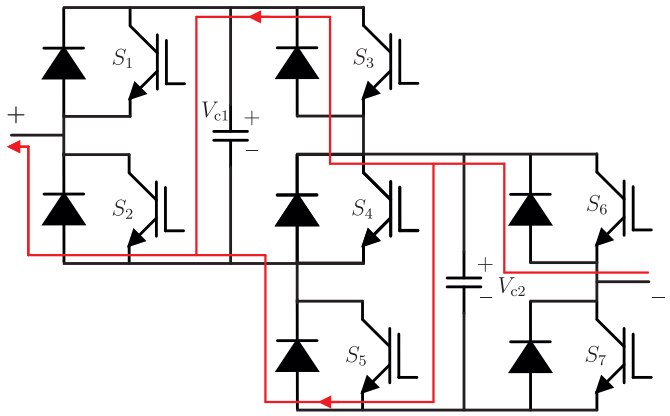


Fig. 5.7: Topology and fault current path of Semi-FBSM.

Table 5.9: Relevant switching states of Semi-FBSM.

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	v_o	Capacitor	
									$i_{SM} > 0$	$i_{SM} < 0$
Active	ON	OFF	OFF	ON	OFF	OFF	ON	$2V_{SM}$	C_1 Ch. C_2 Ch.	C_1 Dis. C_2 Dis.
Active	ON	OFF	ON	OFF	ON	OFF	ON	V_{SM}	C_1 Ch. C_2 Ch.	C_1 Dis. C_2 Dis.
Active	OFF	ON	ON	OFF	ON	ON	OFF	$-V_{SM}$	C_1 Dis. C_2 Dis.	C_1 Ch. C_2 Ch.
Bypassed	OFF	ON	OFF	ON	OFF	ON	OFF	0	-	-
Blocked ($i_{SM} < 0$)	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$-V_{SM}$		C_1 Ch. C_2 Ch.

In active state, the CDSM can provide two positive voltage levels, V_{SM} and $2V_{SM}$. The output voltage V_{SM} can be provided by either C_1 or C_2, as can be seen from Table 5.8, which offers redundant operation states and hence is beneficial for internal fault tolerant control and reliability [174]. In bypassed state, the output voltage is 0.

In the blocked state, the CDSM can produce reverse-biased voltage to block the dc fault current. Depending on the current direction, the two capacitors are either connected in series (positive SM current) or in parallel (negative SM current) [7].

In comparison with FBSM or HBSM-based MMC with the same number of output voltage levels, the CDSM has lower losses than the FBSM but higher losses than the HBSM [49]. However, the reverse voltage per arm offered by the CDSM is only half of the reverse voltage produced by the FBSM per arm (for the same number of voltage levels), which reduces the fault blocking capability and requires longer time to drive the fault current to zero [49].

Semi-full bridge SM In normal operation, the negative SM output voltage can be used to increase the modulation index above 1 and hence increase the ac voltage for a given dc voltage level. As stated in [175], this negative voltage level can be generally smaller than the maximum positive output voltage. A suitable topology to insert two positive voltage levels

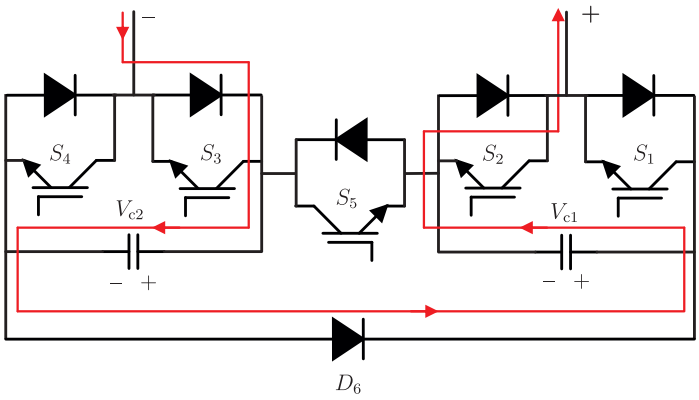


Fig. 5.8: Topology and fault current path of SCDSM.

Table 5.10: Switching states of SCDSM.

State	S_1	S_2	S_3	S_4	S_5	v_o	Capacitor	
							$i_{SM} > 0$	$i_{SM} < 0$
Bypassed	OFF	ON	ON	OFF	ON	0	-	-
Active	ON	OFF	ON	OFF	ON	V_{SM}	C_1 Charging	C_1 Discharging
Active	OFF	ON	OFF	ON	ON	V_{SM}	C_2 Charging	C_2 Discharging
Active	ON	OFF	OFF	ON	ON	$2V_{SM}$	C_1 Charging C_2 Charging	C_1 Discharging C_2 Discharging
Blocked ($i_{SM} > 0$)	OFF	OFF	OFF	OFF	OFF	$2V_{SM}$	C_1 Charging C_2 Charging	
Blocked ($i_{SM} < 0$)	OFF	OFF	OFF	OFF	OFF	$-V_{SM}$		C_1 Charging C_2 Charging

V_{SM} and $2V_{SM}$ and only one negative voltage level $-V_{SM}$ in active state (Table 5.9), is the semi-full bridge submodule (Semi-FBSM, [175]).

As can be seen from Fig. 5.7, the Semi-FBSM is an extension of the CDSM, in which the two clamping diodes are replaced by pairs of active switches and anti-parallel diodes. Similar to the CDSM, the Semi-FBSM contains two SM capacitors, which can be bypassed, connected in parallel or in series and thus, one Semi-FBSM replaces two HBSM in each arm of the MMC.

In the blocked state, the Semi-FBSM produces, depending on the current direction, reverse-biased voltage to block the dc fault current either by the series (positive SM current) or parallel connection (negative SM current) of the two capacitors. Hence, similar to the CDSM, it has half of the blocking capability of the FBSM.

In order to produce the two voltage levels in the active state, in any case only three devices are conducting at the same time. Thus, the Semi-FBSM has 50% higher losses compared to HBSM, but 25% lower losses compared to FBSM (assuming equal conduction losses for IGBTs and diodes) [175].

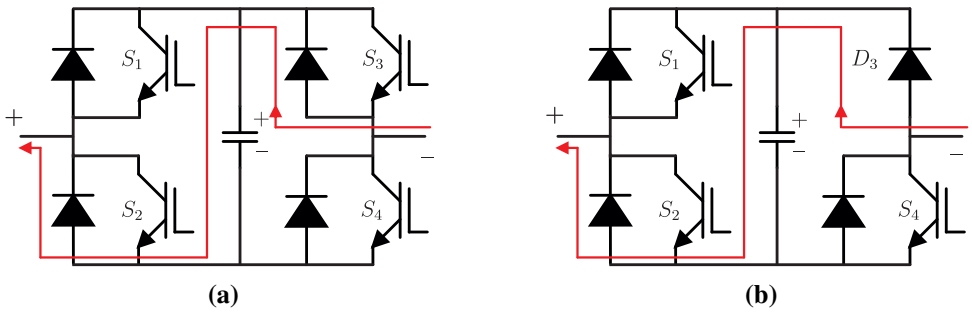


Fig. 5.9: Topology and fault current path of cross-connected SM: (a) 5L-CCSM, (b) 3L-CCSM.

Series-connected double SM In contrast to the CDSM, the series-connected double submodule (SCDSM) makes use of only one additional clamping diode to produce the reverse-biased output voltage during the blocked state (Fig. 5.8). The common point with the CDSM is the additional active switch with anti-parallel diode to interconnect two HBSM in series.

In normal operation, the interconnecting switch is always On and the SCDSM behaves as two HBSM and can produce three output voltage levels, namely 0 in bypassed state and V_{SM} and $2V_{\mathrm{SM}}$ in active state. Similar to the CDSM, the SCDSM also has redundant operation states and hence high fault tolerance towards internal short-circuit faults [174].

As can be seen from Table 5.10, the SCDSM in fault operation, i.e. when all active switches are blocked, is superior compared to the CDSM, since it can produce the same reverse-biased voltage as the series connection of two FBSM, namely $-2V_{\mathrm{SM}}$, while the CDSM can only produce $-V_{\mathrm{SM}}$.

Cross-connected SM Cross-connected submodules (CCSM) are presented in two configurations, namely the five level CCSM (5L-CCSM) with full bipolar operation in active state [48] and the unipolar voltage three level CCSM (3L-CCSM) [49]. Similar to other double SM structures, if the two capacitors are equally charged and balanced, the cross-connected SM can also replace two series connected HBSM to achieve the same arm voltage rating [49].

The 5L-CCSM is built by connecting two HBSM back-to-back by means of two crosswise active switches (Fig. 5.9(a). This SM has four-quadrant operation (i.e. full bipolar) with symmetrical output voltage levels of $-2V_{\mathrm{SM}}$, $-V_{\mathrm{SM}}$, V_{SM}, and $2V_{\mathrm{SM}}$ in active state and 0 in bypassed state for any current direction (Table 5.11).

The 3L-CCSM is derived from the CDSM and 5L-CCSM. Indeed, as shown in Fig. 5.9(b), in the 3L-CCSM, one of the cross-connected active switches is replaced by a diode and hence, in normal operation, the 3L-CCSM can produce three unipolar output voltage levels V_{SM} and $2V_{\mathrm{SM}}$ in active state and 0 in bypassed state like the CDSM (Table 5.12).

Table 5.11: Switching states of 5L-CCSM.

State	S_1	S_2	S_3	S_4	S_5	S_6	v_o	Capacitor $i_{SM} > 0$	Capacitor $i_{SM} < 0$
Bypassed	ON	OFF	OFF	ON	OFF	ON	0	-	-
Bypassed	OFF	ON	ON	OFF	ON	OFF	0	-	-
Active	ON	OFF	ON	OFF	OFF	ON	$-V_{SM}$	C_2 Dis.	C_2 Ch.
Active	OFF	ON	OFF	ON	OFF	ON	$-V_{SM}$	C_1 Dis.	C_1 Ch.
Active	OFF	ON	ON	OFF	OFF	ON	$-2V_{SM}$	C_1 Dis. C_2 Dis.	C_1 Ch. C_2 Ch.
Active	ON	OFF	ON	OFF	ON	OFF	V_{SM}	C_1 Ch.	C_1 Dis.
Active	OFF	ON	OFF	ON	ON	OFF	V_{SM}	C_2 Ch.	C_2 Dis.
Active	ON	OFF	OFF	ON	ON	OFF	$2V_{SM}$	C_1 Ch. C_2 Ch.	C_1 Dis. C_2 Dis.
Blocked ($i_{SM} > 0$)	OFF	OFF	OFF	OFF	OFF	OFF	$2V_{SM}$	C_1 Ch. C_2 Ch.	
Blocked ($i_{SM} < 0$)	OFF	OFF	OFF	OFF	OFF	OFF	$-2V_{SM}$		C_1 Ch. C_2 Ch.

Table 5.12: Switching states of 3L-CCSM.

State	S_1	S_2	S_3	S_4	S_5	v_o	Capacitor $i_{SM} > 0$	Capacitor $i_{SM} < 0$
Bypassed	OFF	ON	ON	OFF	ON	0	-	-
Active	ON	OFF	ON	OFF	ON	V_{SM}	C_1 Charging	C_1 Discharging
Active	OFF	ON	OFF	ON	ON	V_{SM}	C_2 Charging	C_2 Discharging
Active	ON	OFF	OFF	ON	ON	$2V_{SM}$	C_1 Charging C_2 Charging	C_1 Discharging C_2 Discharging
Blocked ($i_{SM} > 0$)	OFF	OFF	OFF	OFF	OFF	$2V_{SM}$	C_1 Charging C_2 Charging	
Blocked ($i_{SM} < 0$)	OFF	OFF	OFF	OFF	OFF	$-V_{SM}$		C_1 Charging C_2 Charging

However, in contrast to the CDSM, in the blocked state, both the 5L-CCSM and the 3L-CCSM provide fault blocking capability with reverse-biased voltage equivalent to FBSM-based MMC (doubled in comparison to CDSM) [49] and hence allow for compact converter structure in hybrid MMC structures. In [48] it is derived that dc fault blocking ability is already achieved with 25% 5L-CCSM together with 75% HBSM. This configuration would result in lower overall converter losses compared with hybrid MMC with only FBSM, and similar to CDSM-based MMC.

Asymmetrical double SM The article [52] presents the asymmetrical double submodule (ADSM), in which two HBSM with originally different voltage rating (one with $2V_{SM}$ and one with V_{SM} nominal SM voltage) are connected at their dc side (Fig. 5.10), though the resulting capacitor voltages in the ADSM are equal in the final configuration.

This type also allows for generating four-level output voltage in normal operation, i.e. $-V_{SM}$, V_{SM}, and $2V_{SM}$ in the active state and 0 in the bypassed state (Table 5.13). However, in

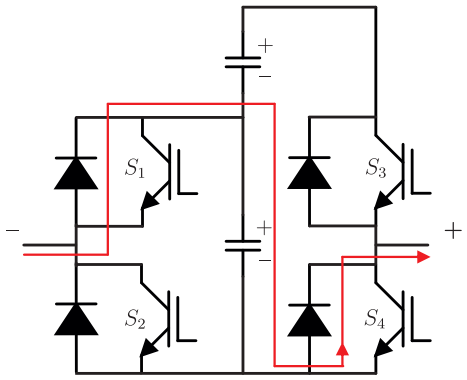


Fig. 5.10: Topology and fault current path of Asymmetrical-DSM.

Table 5.13: Switching states of ADSM.

State	S_1	S_2	S_3	S_4	v_o	Capacitor	
						$i_{SM} > 0$	$i_{SM} < 0$
Active	ON	OFF	ON	OFF	V_{SM}	C_1 Charging	C_1 Discharging
Active	ON	OFF	OFF	ON	$-V_{SM}$	C_2 Discharging	C_2 Charging
Active	OFF	ON	ON	OFF	$2V_{SM}$	C_1 Charging C_2 Charging	C_1 Discharging C_2 Discharging
Bypassed	OFF	ON	OFF	ON	0	-	-
Blocked ($i_{SM} < 0$)	OFF	OFF	OFF	OFF	$-V_{SM}$		C_2 Charging

contrast to the cross-connected SM, only half of the blocking voltage of a FBSM (i.e. $-V_{SM}$) can be provided for the current from ac to dc (negative current polarity).

5.2. MMC architectures with fault blocking capability

MMC architectures with fault blocking capability have the feature that by deactivating the active switches (in most cases IGBTs are used), a reverse-biased voltage is created in the fault current path, which lets the fault currents decrease and finally blocks them, if this counter voltage is sufficient to block the conduction of the freewheeling diodes. In other words, the inserted counter-voltage must be larger than the dc voltage generated by the MMC in the rectification mode and consequently, the current in inductive elements starts to decrease in a very short time.

The full-bridge MMC (FB-MMC), which employs FBSM in both arms instead of the HBSM (Fig. 5.11), is one of the most common structures to integrate the fault blocking capability in the MMC [50]. Offering per SM the full reverse biased voltage, namely in the arm in total twice the dc link voltage, the FBSM provides the shortest fault current decay time. Also, in normal operation it offers four-quadrant operation with full bipolar voltage and current and hence allows to operate the system at higher ac voltage for a given dc voltage level (boost-type inverter mode) or at lower dc voltage for a given ac voltage (buck-type rectifier mode),

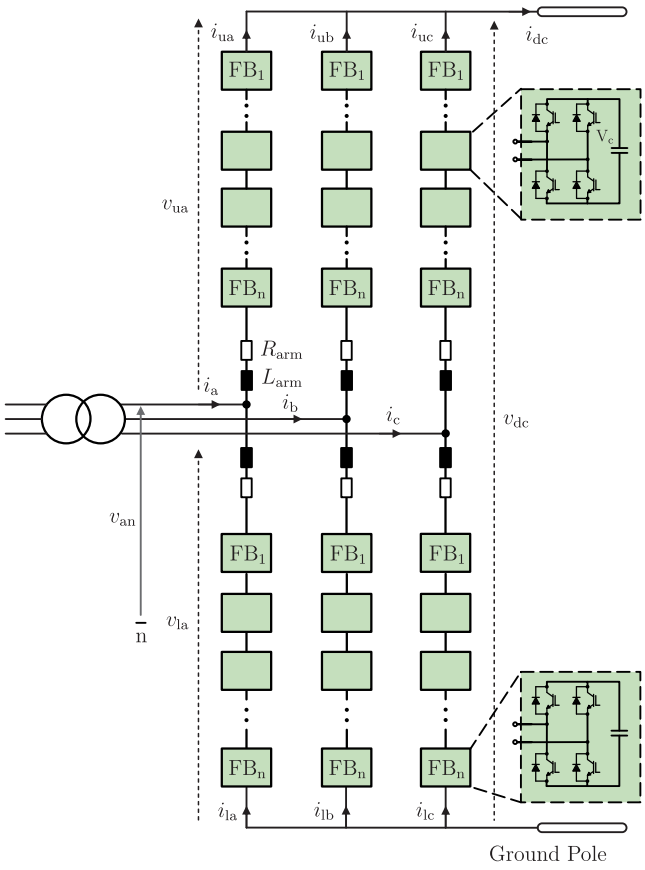


Fig. 5.11: Three-phase topology of FB-MMC.

respectively. However, the FB-MMC needs twice the amount of semiconductors compared to the HB-MMC and hence has high losses and costs.

While in the previous section the focus was laid on the different SM designs in MMC architectures with fault blocking capability in order to reduce the losses and costs, in the following section, the MMC architectures with fault blocking capability themselves are reviewed, which comprises of a mixture of bipolar or asymmetric SM with the conventional HBSM. Special emphasis is given to the minimum number of bipolar or asymmetric SM in the MMC to achieve the fault blocking capability.

5.2.1. Hybrid modular multilevel converter

Employing conjunctions of two types of SM, i.e. bipolar or asymmetric SM and conventional HBSM, in one arm of the MMC as shown in Fig. 5.12 enables fault blocking capability with low conduction losses. These methods are known as hybrid MMC and are designed to reduce the number of bipolar or asymmetric SM in order to minimize the losses and costs [49]. While in practical application different SM types with fault blocking capability can be used, in Fig. 5.12 for simplicity only the FBSM is shown.

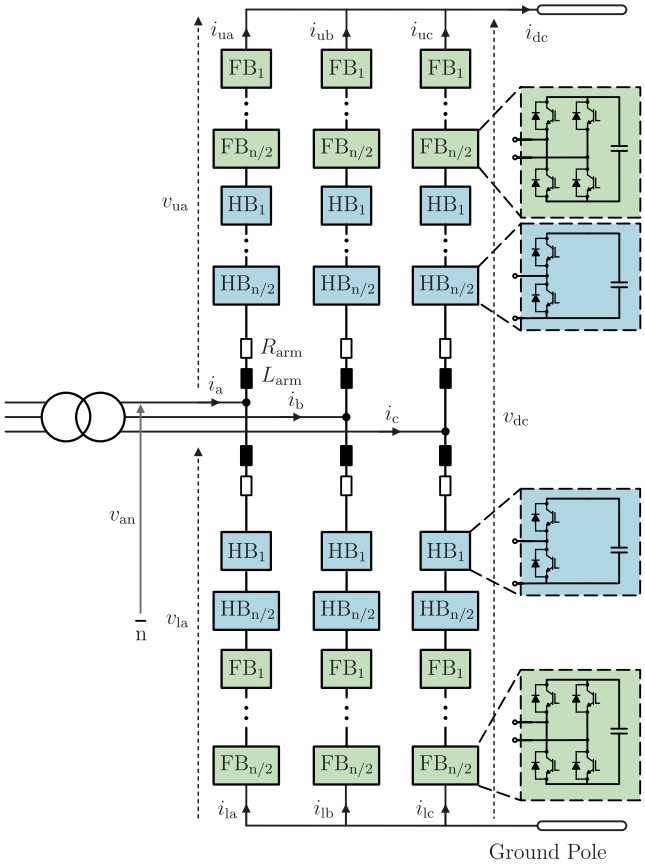


Fig. 5.12: Three-phase topology of Hybrid MMC.

The basic topology of the hybrid MMC (HMMC) in an asymmetrical monopole HVdc configuration comprises of n_{SM} SM in each arm, of which n_f are FBSM and n_h are HBSM. In practical application, the number of FBSM, which are allowed to operate in negative state ($-V_{SM}$) in normal operation may be constrained and is labeled in accordance with [51] with parameter $n_{f,n}$. The design objective is to optimize the ratio between FBSM and HBSM in order to increase the power transmission capability in normal operating condition by extending the output voltage range with the negative state SM (see Table 5.4) and ensure the fault blocking and capacitor voltage balancing in fault condition [51].

Assuming the conventional design of HMMC with n_f FBSM and $n_h = n_{SM} - n_f$ HBSM and no negative state SM, the total arm voltage range is 0 to $n_{SM}V_{SM}$, with V_{SM} being the nominal dc voltage across each SM capacitor. Assuming a maximum modulation index $m = 1$, the dc voltage is equal to

$$V_{dc} = n_{SM}V_{SM} \tag{5.1}$$

and the peak of ac phase voltage, the converter can generate at its output terminals is

$$\hat{v}_{ac} = \frac{1}{2}n_{SM}V_{SM} = \frac{1}{2}V_{dc}\ , \tag{5.2}$$

if the synthesized arm voltages can only have positive values.

Instead, if $n_{\mathrm{f,n}}$ FBSM are allowed to operate in negative state, the range of the total arm voltage will be extended from $-n_{\mathrm{f,n}}V_{\mathrm{SM}}$ to $n_{\mathrm{SM}}V_{\mathrm{SM}}$. Thus, the dc and peak of ac voltage are

$$V_{\mathrm{dc}} = \left(n_{\mathrm{SM}} - n_{\mathrm{f,n}}\right) V_{\mathrm{SM}} \tag{5.3}$$

and

$$\hat{v}_{\mathrm{ac}} = \frac{1}{2}\left(n_{\mathrm{SM}} + n_{\mathrm{f,n}}\right) V_{\mathrm{SM}} = \frac{1}{2}V_{\mathrm{dc}} + m \cdot \frac{n_{\mathrm{f,n}}V_{\mathrm{dc}}}{n_{\mathrm{SM}} - n_{\mathrm{f,n}}}\ , \tag{5.4}$$

respectively. (5.4) demonstrates the enlarged ac voltage operation range using FBSM in negative state.

One challenge related to the hybrid design are the differences in the charging and discharging process of FBSM and HBSM and the resulting effects on the capacitor voltage ripple and balancing [51]. While the FBSM can charge and discharge at any current direction, the HBSM can only charge for positive arm current flow and discharge during the negative current period. In [51] it is analyzed how the increased modulation index affects the arm currents and it is revealed that a maximum modulation index of $m = 2$ can be achieved with the negatively inserted FBSM to guarantee sufficient time to balance the HBSM capacitor voltages within one fundamental period of the arm current. Hence, the maximum achievable ac voltage (5.4) with $m = 2$ is always less than or equal to V_{dc} and from the balancing point of view, the maximum number of FBSM to generate negative output voltages is limited to

$$n_{\mathrm{f,n}} \leq \frac{1}{3}n_{\mathrm{SM}}\ . \tag{5.5}$$

The second design requirement for HMMC is the dc fault blocking ability, which is defined by the series reverse-biased voltage formed by the SM capacitors of the FBSM in the fault current path. This voltage must be higher than the ac line-to-line voltage to prevent the freewheeling diodes conduction and hence successfully block the dc fault current once all active switches are turned OFF.

The maximum peak line-to-line voltage for the HMMC during the dc fault at maximum modulation index $m = 2$ from previous consideration is obtained in [51] with

$$\hat{v}_{\mathrm{ac,ll,max}} = \sqrt{3}\frac{n_{\mathrm{SM}} + n_{\mathrm{f,n}}}{2\left(n_{\mathrm{SM}} - n_{\mathrm{f,n}}\right)}V_{\mathrm{dc}}\ . \tag{5.6}$$

By assumption, in the HMMC in each arm there are n_{f} FBSM, which can generate an arm voltage of

$$v_{\mathrm{arm}} = n_{\mathrm{f}}V_{\mathrm{SM}} = \frac{n_{\mathrm{f}}}{n_{\mathrm{SM}} - n_{\mathrm{f,n}}}V_{\mathrm{dc}} \tag{5.7}$$

In the fault current path, there is always one upper and one lower arm (in different legs) in series connection, which form the blocking voltage. The blocking voltage must be higher than the peak of the line-to-line voltage and thus the following criteria for minimum number

of FBSM has been developed in [51] for optimal HMMC design:

$$\hat{v}_{\mathrm{ac,ll,max}} = \sqrt{3}\frac{n_{\mathrm{SM}} + n_{\mathrm{f,n}}}{2\left(n_{\mathrm{SM}} - n_{\mathrm{f,n}}\right)}V_{\mathrm{dc}} \leq 2\frac{n_{\mathrm{f}}}{n_{\mathrm{SM}} - n_{\mathrm{f,n}}}V_{\mathrm{dc}} = 2v_{\mathrm{arm}} \Rightarrow n_{\mathrm{f}} \geq \frac{\sqrt{3}}{4}\left(n_{\mathrm{SM}} + n_{\mathrm{f,n}}\right) \ . \quad (5.8)$$

Two specific design scenarios are presented:

1. $n_{\mathrm{f,n}} = 0$, $n_{\mathrm{f}} = \frac{1}{2}n_{\mathrm{SM}}$
2. $n_{\mathrm{f,n}} = \frac{1}{3}n_{\mathrm{SM}}$, $n_{\mathrm{f}} = \frac{2}{3}n_{\mathrm{SM}}$

The first design is built out of 50% HBSM and 50% FBSM, which do not operate in negative state ($n_{\mathrm{f,n}} = 0$) and hence the conventional control strategy of HBSM-based MMC can be applied. The second design makes use of the maximum number of FBSM in negative output voltage state in order to double the power transmission in normal operation compared to the first design.

The article [176] develops a strategy for HMMC with a combination of HBSM and FBSM to ride-through pole-to-pole and pole-to-ground faults in symmetrical monopole HVdc systems. In symmetrical monopole configuration during a P2G fault, the pole-to-ground voltage of the healthy pole increases to twice the rated value. In addition, as described in ([176]), the secondary side voltage of the transformer is affected by an offset of half the rated dc voltage between the transformer neutral point and the ground. This offset voltage would lead to the tripping of the ac CB (which is considered for point-to-point HVdc connection) and hence transmission outage. Thus, it is stated that HMMC cannot continuously operate under P2G fault due to a possible breakdown of the transformer and healthy pole insulation.

Instead, the authors of [176] propose to control the FBSM in the HMMC to reduce the healthy pole dc voltage to half of the rated dc voltage, which would avoid the pole overvoltage and transformer offset voltage and still allows to transmit 50 % of the rated power during P2G faults in symmetrical monopole HVdc systems. Keeping the power transmission active during pole-to-ground faults is beneficial for the angle stability of the connected ac grid. In contrast to the previously presented HMMC, in [176] the FBSM are not blocked, but actively controlled to produce bipolar output voltage and to synthesize the dc voltage to zero at the faulty pole during P2G faults and at both the negative and positive pole during P2P faults, respectively. The HBSM are bypassed under this condition. In order to decrease the current decay time, an active damping control is proposed, which adjusts the dc voltage set-point with respect to the dc fault current under P2P faults. In the P2G fault case, the grounding resistor of the star point grounding circuit will help to reduce the fault current and hence no additional active damping is required.

The FBSM in the HMMC also allow - despite the fault blocking property - to operate the HVdc system at higher ac voltage for a given dc voltage level (over-modulation mode) as

well as at low dc voltage [171]. To calculate the minimum number of FBSM in the HMMC for such operation modes, two parameters must be introduced: the over-modulation constant $m_o \geq 1$ and the dc modulation index m_{dc}.

In over-modulation mode the ac phase voltage can be controlled in the range

$$-m_o m \frac{v_{arm,dc}}{2} \leq v_{ac} \leq m_o m \frac{v_{arm,dc}}{2} \tag{5.9}$$

with $v_{arm,dc}$ being the arm dc voltage. The arm dc voltage in steady-state is equal to the nominal dc voltage $V_{dc,nom}$. In dynamic state, however, the dc modulation index decouples the dc voltage and arm dc voltage:

$$v_{dc} = m_{dc} v_{arm,dc} \ . \tag{5.10}$$

This control mode can be only achieved with FBSM, hence, lowering the dc modulation index requires a higher number of FBSM in the HMMC design.

Neglecting the voltage drop across arm inductances and resistances, the dc voltage and ac phase voltage can be expressed by the upper v_u and lower arm voltages v_l as in (5.11) and (5.12):

$$v_{dc} = v_u + v_l \tag{5.11}$$

$$v_{ac} = \frac{v_l - v_u}{2} \ . \tag{5.12}$$

Considering the definition of the dc modulation index in (5.10) and rearranging (5.11) and (5.12) for $m = 1$ results in

$$v_u = m_{dc} \frac{v_{arm,dc}}{2} - v_{ac} \tag{5.13}$$

$$v_l = m_{dc} \frac{v_{arm,dc}}{2} + v_{ac} \ . \tag{5.14}$$

The normal (or in this case over-modulation) range of the ac output voltage must be guaranteed under minimum dc voltage, so that the converter can always exchange rated power. Thus, from (5.13) and (5.14) it follows for the maximum and minimum value for the upper arm voltage:

$$v_{u,max} = \frac{m_{dc,min} + m_o}{2} V_{dc,nom} \tag{5.15}$$

$$v_{u,min} = \frac{m_{dc,min} - m_o}{2} V_{dc,nom} \ . \tag{5.16}$$

Similar expression can be found for the lower arm. However, since the number of FBSM and HBSM is the same in both arms, in the calculation of the minimum number of FBSM required for this operation, only the positive arm voltage is considered. The positive output

voltage is generated by both FBSM and HBSM (i.e. $v_{\mathrm{u,max}} \approx n_{\mathrm{SM}} V_{\mathrm{SM}}$). The overall maximum positive output voltage is achieved for the nominal dc voltage (i.e. $m_{\mathrm{dc}} = 1$) thus, from (5.15) it follows for the total number of SM in the HMMC for a given over-modulation constant:

$$n_{\mathrm{SM}} = \frac{(1+m_{\mathrm{o}})\,\frac{V_{\mathrm{dc,nom}}}{2}}{V_{\mathrm{SM}}} \quad . \tag{5.17}$$

The minimum arm voltage in (5.16) can be negative, if $V_{\mathrm{dc,min}} = m_{\mathrm{dc,min}} V_{\mathrm{dc,nom}} < m_{\mathrm{o}} V_{\mathrm{dc,nom}}$. The FBSM are required to generate this negative arm voltage. Hence, it follows the minimum number of FBSM

$$n_{\mathrm{f}} = \frac{m_{\mathrm{o}} - m_{\mathrm{dc,min}}}{2} \frac{V_{\mathrm{dc,nom}}}{V_{\mathrm{SM}}} \quad . \tag{5.18}$$

Consequently, the number of HBSM is

$$n_{\mathrm{h}} = \frac{1+m_{\mathrm{dc,min}}}{2} \frac{V_{\mathrm{dc,nom}}}{V_{\mathrm{SM}}} \quad . \tag{5.19}$$

In the common case, the minimum dc voltage is assumed to be zero. Thus, (5.18) and (5.19) can be simplified to

$$n_{\mathrm{f}} = \frac{m_{\mathrm{o}}}{2} \frac{V_{\mathrm{dc,nom}}}{V_{\mathrm{SM}}} \tag{5.20}$$

$$n_{\mathrm{h}} = \frac{1}{2} \frac{V_{\mathrm{dc,nom}}}{V_{\mathrm{SM}}} \quad . \tag{5.21}$$

The article [173] investigates the trade-off between higher capability of handling dc faults and lower capital investments and power losses in the HMMC considering two designs:

1. HBSM + CSSM
2. HBSM + CDSM .

It is assumed a pole-to-pole fault in symmetrical monopole HVdc configuration, for which the minimum number of SM with fault blocking capability for the two designs is calculated. Assuming n_{h} and n_{cs} as the number of HBSM and CSSM in one arm of the HMMC, respectively. Then, the following relationship for dc and peak of ac phase and line-to-line voltage at modulation index $m = 1$ can be achieved (similar to the analysis presented above):

$$\begin{aligned} V_{\mathrm{dc}} &= (n_{\mathrm{h}} + n_{\mathrm{cs}})\, V_{\mathrm{SM}} \\ \hat{v}_{\mathrm{ac,ph}} &= \frac{1}{2} V_{\mathrm{dc}} = \frac{1}{2} (n_{\mathrm{h}} + n_{\mathrm{cs}})\, V_{\mathrm{SM}} \\ \hat{v}_{\mathrm{ac,ll}} &= \sqrt{3}\hat{v}_{\mathrm{ac,ph}} = \frac{\sqrt{3}}{2} (n_{\mathrm{h}} + n_{\mathrm{cs}})\, V_{\mathrm{SM}} \quad . \end{aligned} \tag{5.22}$$

The fault current flows through one upper and one lower arm in different legs of the MMC and hence, the number of CSSM to block the fault current is $2n_{\mathrm{cs}}$, which leads to the require-

ment for sufficient counter voltage:

$$2n_{\mathrm{cs}}V_{\mathrm{SM}} \geq \hat{v}_{\mathrm{ac,ll}} \ . \tag{5.23}$$

Substituting (5.22) in (5.23) leads to

$$\frac{\sqrt{3}}{4} \leq \frac{n_{\mathrm{cs}}}{n_{\mathrm{h}}+n_{\mathrm{cs}}} \leq 1 \ , \tag{5.24}$$

from which the minimum proportion of CSSM in one arm of the HMMC can be found with approximately 43 %, which is the same number of bipolar SM as in the HMMC with FBSM and HBSM.

The CDSM in normal operating state is equivalent to two HBSM. The dc link voltage and ac phase and line-to-line voltage for HMMC employing the CDSM as SM with fault blocking capability can be found with

$$\begin{aligned} V_{\mathrm{dc}} &= (n_{\mathrm{h}}+2n_{\mathrm{cd}})\,V_{\mathrm{SM}} \\ \hat{v}_{\mathrm{ac,ph}} &= \frac{1}{2}V_{\mathrm{dc}} = \frac{1}{2}(n_{\mathrm{h}}+2n_{\mathrm{cd}})\,V_{\mathrm{SM}} \\ \hat{v}_{\mathrm{ac,ll}} &= \sqrt{3}\hat{v}_{\mathrm{ac,ph}} = \frac{\sqrt{3}}{2}(n_{\mathrm{h}}+2n_{\mathrm{cd}})\,V_{\mathrm{SM}} \ . \end{aligned} \tag{5.25}$$

However, in blocked state the two capacitors are connected in parallel and hence only the same blocking voltage $-V_{\mathrm{SM}}$ can be achieved per SM. Similarly, to the CSSM-based HMMC the total reverse-biased voltage by the series connection of CDSM must fulfill the requirement

$$2n_{\mathrm{cd}}V_{\mathrm{SM}} \geq \hat{v}_{\mathrm{ac,ll}} \ . \tag{5.26}$$

From (5.25) and (5.26) the minimum number of CDSM can be found with

$$\frac{\sqrt{3}}{4-\sqrt{3}} \leq \frac{n_{\mathrm{cd}}}{n_{\mathrm{h}}+n_{\mathrm{cd}}} \leq 1 \Rightarrow n_{\mathrm{cd}} \geq 0.76n \ , \tag{5.27}$$

with $n = n_{\mathrm{cd}} + n_{\mathrm{h}}$ being the total number of SM in one arm.

In the article [177], instead of using different SM in the same MMC as in the previous designs, it is proposed to build the hybrid MMC by series connection of high-voltage rated HB-MMC and low-voltage rated FB-MMC on the dc side (see Fig. 5.13). On the ac side, the two converters are connected in parallel with different secondary side voltage rating of the transformer. The FB-MMC is parallel connected with a dc fault breaking circuit. The fault breaking circuit consists of an ultra-fast mechanical switch (which has opening times of around 2 ms) in parallel with a large dc capacitor connected between the positive pole and the two MMCs' midpoint in [177]. In principle, the FB-MMC commutates only the fault current to the fault breaking circuit. The counter-voltage to block the fault current is built by

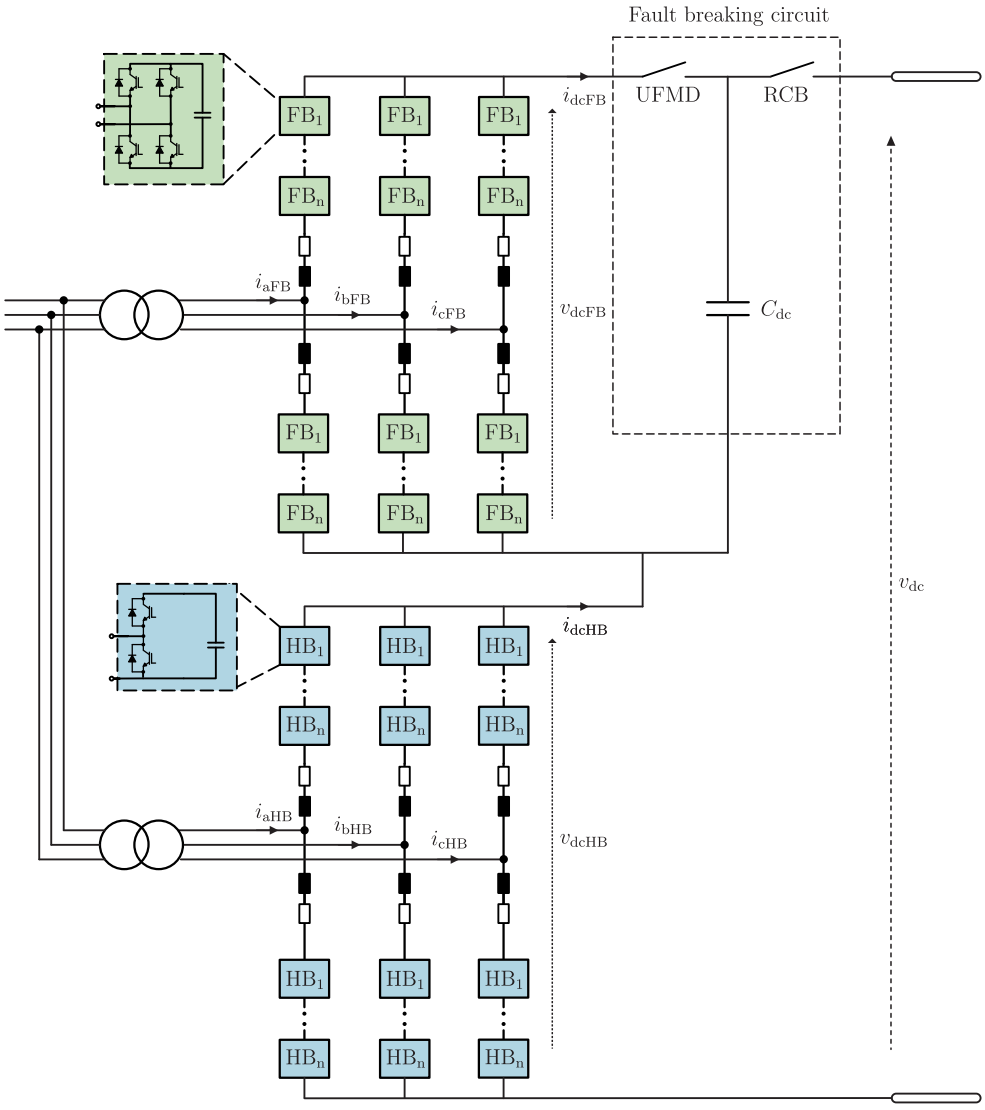


Fig. 5.13: Three-phase topology of hybrid MMC with reduced power rating FB-MMC and full power rating HB-MMC.

charging the large dc capacitor of the fault breaking circuit by the fault current flow. Thus, the FB-MMC can be designed with smaller voltage rating. In [177], a design with only 10-20% FBSM compared to the number of HBSM in the high-voltage HB-MMC is proposed, which can reduce the capital costs and losses. It has to be noted that the number of FBSM is not evaluated analytically (to find the minimum), but just assumed and demonstrated as practically feasible.

In normal operation, the mechanical breakers (both the UFMS and the RCD) of the fault breaking circuit are closed and the dc capacitor is charged to the dc link voltage of the FB-MMC. Both the FB-MMC and HB-MMC transmit power in normal operation. It is assumed a P2P fault in symmetrical monopole configuration, which leads to discharge of the dc capacitor and the HBSM capacitors, respectively [177]. Once the fault is detected by exceeding a pre-defined dc over-current, the HB-MMC and the FB-MMC are blocked. In blocked state, the FB-MMC inserts reverse-biased voltage in the current path, so that the

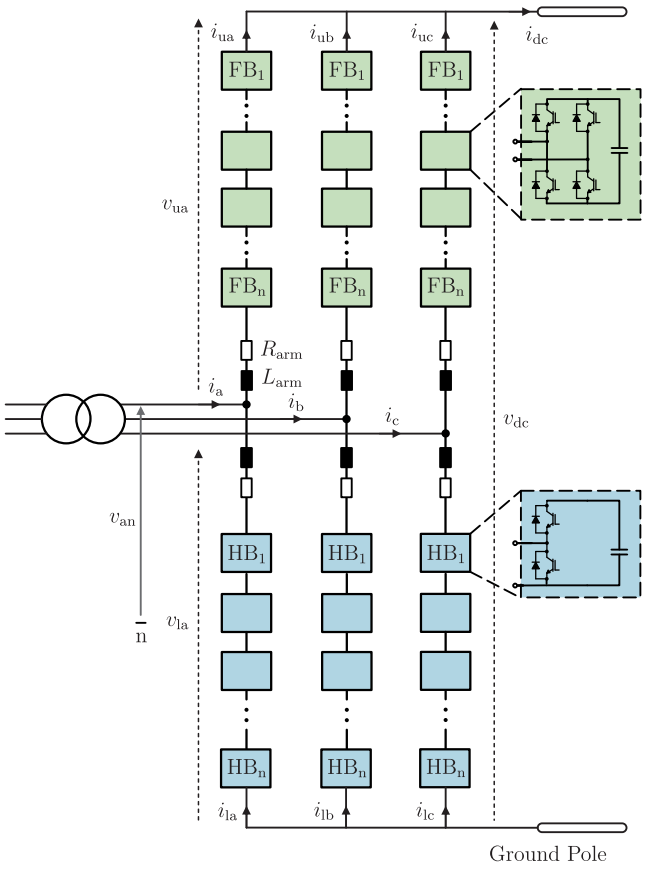


Fig. 5.14: Three-phase topology of the Hybrid Arm MMC.

arm currents (and in consequence the dc current) in the FB-MMC are suppressed to zero. The fault current still flows through the freewheeling diodes of the HB-MMC, but is now commutated to the dc capacitor of the fault blocking circuit. The dc capacitor is charged in reverse direction, until its negative voltage amplitude exceeds the peak ac line-to-line voltage (criterion for fault blocking), which in turn blocks the fault and suppresses the HB-MMC fault current to zero. Finally, the RCD opens to isolate the faulty line.

While this MMC architecture achieves lower costs and losses in normal operation (in between the HB-MMC and the HMMC), its fault blocking performance is severely reduced compared to the hybrid MMC designs presented before. Due to the involvement of UFMS and the charging of the dc link capacitor (instead of providing the blocking voltage instantly by the MMC FBSM), a comparably high delay time is introduced, which increases the dc fault blocking time to > 10 ms as demonstrated in [177].

5.2.2. Hybrid arm modular multilevel converter

An alternative MMC design with mixed SM types is the hybrid arm MMC. First proposed in [52], as shown in Fig. 5.14, this topology makes use of FBSM in one arm and HBSM in the other arm, instead of using both SM types in either arm as in the HMMC. The HA-MMC

is capable of blocking dc fault currents in asymmetric monopole and bipolar HVdc system configuration [52]. The initially presented design requires that 50 % of the arm voltage must be reversible to successfully block the dc fault current.

Bipolar SM have the feature that they can be charged in both current directions and that the SM capacitor can be inserted with positive and negative voltage polarity (four-quadrant operation). This enables a reverse-biased voltage in the converter arms (with respect to the ac voltage) by the natural commutation of the freewheeling diodes in blocked state and hence allows for fault current blocking. Moreover, due to the negative output voltage state, the bipolar SM can control the maximum ac voltage in over-modulation range independent of the available dc voltage. If just the fault blocking feature is required, asymmetric SM, such as the unipolar FBSM with three-quadrant operation, can be used [52]. Two designs using bipolar SM are presented in [52]. In the first design, 100 % HBSM in the arm connected to the ground pole and 100 % FBSM in the arm away from the ground pole are used. The alternative design employs 100 % semi FBSM and is not further investigated.

While the HA-MMC employs the same number of bipolar or asymmetric SM as the conventional design of the HMMC, it has the advantage of avoiding the over-voltage problem, which can occur in the case of station ac phase-to-ground faults. As demonstrated in [52], using bipolar SM in the arm close to the grounding pole leads to up to 100 % over-voltage in the bipolar SM converter arm, which would require significant overrating of the semiconductor devices.

The HA-MMC in [53] is built with the HBSM-based arm connected to the ground pole and a U-FBSM-based arm connected to the positive or negative pole in a bipolar HVdc configuration. This MMC architecture further reduces the number of semiconductor devices, however, it is not suitable for over-modulation operation (i.e. boost-type inverter). It is presented the fault and post-fault operation scheme of the HA-MMC based on finite state machine. In the normal state, i.e. before the dc fault occurs, the U-FBSM is controlled as a HBSM by keeping the active switch S_3 permanently switched On. Hence, conventional control and modulation strategies as in HBSM-based MMCs can be applied. A practical difficulty in the HA-MMC are the different power losses occurring in the different SM types in the upper and lower arm and the potential differences in the net power flow, which demand for additional arm energy balancing controller [53].

If the fault current exceeds a predefined threshold (e.g. two or three times the nominal current), all active switches in the MMC will be blocked (fault state) and the dc fault current will be blocked. The article [53] demonstrates that regardless of the arm current direction, the derivative of the UFBSM arm currents is always negative and the currents are decaying to zero. In turn, if all arm currents are zero, the dc current will also be zero. Moreover, it is shown that after all arm currents dropped to zero, the diodes in the UFBSM are reverse-biased and prevent the arm and fault current's re-ignition. Nevertheless, in practical applica-

tions mechanical residual current breakers (RCB) are installed at the dc side to finally clear the fault and isolate the HVdc link, if the fault is identified as permanent [53].

In contrast to the HMMC based on U-FBSM, in which all arms should stay in blocked state under dc fault condition, in the HA-MMC the HBSM-based arm can be de-blocked and actively controlled to exchange reactive power with the ac grid (STATCOM-state) as soon as the fault current drops below a critical residual value. The STATCOM action can stabilize the ac side voltage in order to counteract the influence of the missing active power transmission.

After a certain delay time (e.g. $120-500$ ms) to finish the de-ionization of the fault arc and wait for the restoration of the HVdc line insulation to full voltage, the MMC will start an auto-reclosing sequence, i.e. several attempts are made to recover the power transmission (e.g. 3-4 times with a delay of $20-100$ ms between each of them). This is to identify whether the fault is permanent or not, however, it contains the drawback of relatively large delay and hence power outage time and the possible damages a re-strike of the fault can cause as explained in Subsection 4.4. In case of a permanent fault, the U-FBSM will stay in blocked mode, while the HBSM will keep working as STATCOM. If the fault is temporary, the MMC will transit to recovery state and rebuild the dc voltage and afterward recover the power transmission.

Another application of the HA-MMC has been presented in [172]. It considers a scenario of unidirectional hybrid bipolar HVdc with LCC-HVdc at the rectifier and HA-MMC at the inverter terminal to connect large power facilities with weak ac grid. The unidirectional power transmission allows to use asymmetric SM with 3-quadrant operation, i.e. bipolar voltage to block the fault current and provide low-dc-voltage-mode together with a unipolar current, and it is proposed to use the diagonal bridge SM in the arm away from the grounding pole. The low-dc-voltage-mode implies that the HA-MMC keeps the power transmission active for slight deviations of the dc voltage, which are caused by the sending end LCC. In this case, the dc current is kept constant and the active power transmission is adjusted proportionally with the drop in the dc voltage. The HBSM keep the dc voltage across the HB-arm constant, while the diagonal bridge arm can decrease or even inverse the voltage and hence compensate the drop in the dc voltage.

5.2.3. Alternate arm converter

The alternate arm converter is a hybrid of FB-MMC and 2L-VSC. In each arm a stack of FBSM is connected in series with a series of IGBTs with anti-parallel diodes, the so-called director switch (Fig. 5.15). The key feature of this topology is to essentially use only one arm per half cycle to produce the ac voltage: the upper arm for the positive half cycle and the lower arm for the negative half cycle, which resembles the operation of a conventional

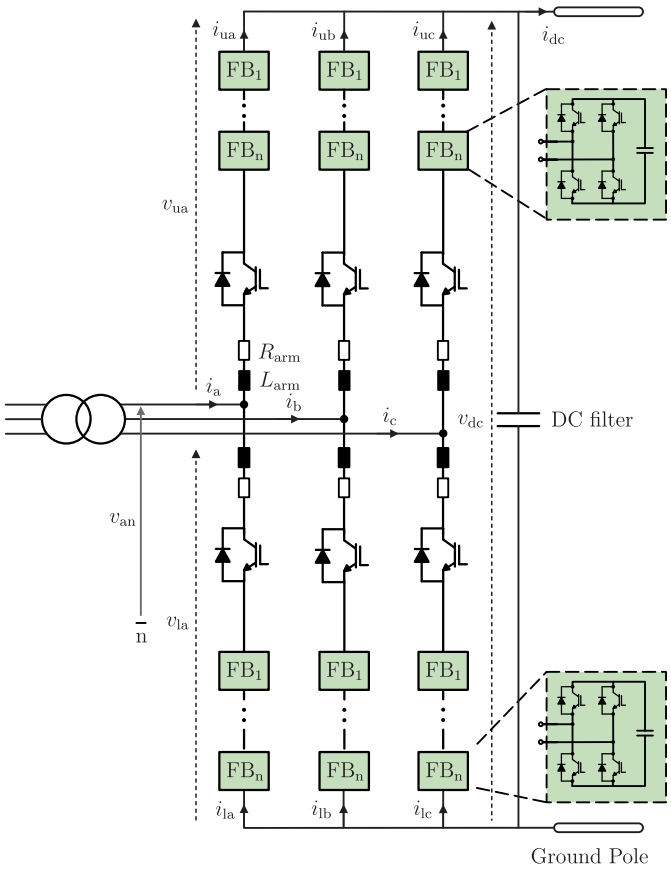


Fig. 5.15: Three-phase topology of the Alternate Arm Converter.

2L-VSC. Indeed, the role of the director switches is to determine which arm is used and to alternate the phase current conduction period of the upper and the lower arm, i.e. rectifying the ac currents into a dc current, while the FBSM stacks are employed to maintain the ac voltage waveform quality. The main advantage of the AAC is that each stack of FBSM only has to produce half of the dc voltage (in normal operation) and hence, the number of FBSM compared to FB-MMC at similar power and dc voltage rating can be significantly reduced. Consequently, the efficiency is also increased and cost and volume are decreased [66].

The relatively fine ac output voltage steps generated by the AAC are achieved in a similar way as in the MMC by inserting and bypassing the charged SM capacitors. As explained in the previous section, the capacitors are charged or discharged by the arm current depending on the arm current direction and the switching state. However, unlike the MMC, the alternate operation of the AAC hinders a continuous energy exchange between the upper and lower arms of the AAC [178]. An unbalance in the stored energy in the SM capacitors leads to a deviation of the SM voltages away from their reference.

The AAC's natural energy balance can only be achieved in a single operating point, the so-called sweet-spot, in which the converter operation ensures a strictly zero net energy exchange over each half cycle [66]. Assuming ac voltage and current with $v_{ac}(t) = \hat{v}_{ac} \sin(\omega t)$

and $i_{\mathrm{ac}}(t) = \hat{i}_{\mathrm{ac}} \sin(\omega t + \varphi_{\mathrm{ac}})$ and equating the energy coming from the ac side

$$\begin{aligned} W_{\mathrm{ac}} &= \int_0^{T/2} v_{\mathrm{ac}}(t) i_{\mathrm{ac}}(t) \mathrm{d}t \\ &= \frac{\hat{v}_{\mathrm{ac}} \hat{i}_{\mathrm{ac}} \cos(\varphi_{\mathrm{ac}}) T}{4} \end{aligned} \tag{5.28}$$

with the energy going to the dc side of the converter

$$\begin{aligned} W_{\mathrm{dc}} &= \int_0^{T/2} \frac{V_{\mathrm{dc}}}{2} i_{\mathrm{ac}}(t) \mathrm{d}t \\ &= \frac{V_{\mathrm{dc}} \hat{i}_{\mathrm{ac}} \cos(\varphi_{\mathrm{ac}}) T}{2\pi} \end{aligned} \tag{5.29}$$

results in the ideal operating point, defined by the ratio of ac to dc voltage magnitude:

$$\hat{v}_{\mathrm{ac}} = \frac{2}{\pi} V_{\mathrm{dc}} \Leftrightarrow \hat{v}_{\mathrm{ac,ll}} = \frac{2}{\pi} \sqrt{3} V_{\mathrm{dc}} \ . \tag{5.30}$$

This resembles an over-modulation operation of the converter, which is ensured by the ability of the FBSM to produce negative arm voltage [66].

The FBSM in the AAC also enable fault blocking capability, if sufficient SM are included in the stacks to oppose the ac line-to-line voltage and hence block the current flow from ac to dc. In addition, the AAC can be operated to keep control of its phase currents, which allows to continuously exchange reactive power with the ac grid also during the dc fault (STATCOM-operation) [66]. Since the AAC has to be operated in or at least very close to the sweet-spot, the number of FB must be chosen, so that the sum of its SM capacitor voltages is minimum 27 % bigger than half of the dc voltage, if dc fault blocking is requested [66].

A second requirement influencing the choice of the number of FBSM, is the active balancing control, which can be performed by extending the period to hand over the conduction of the phase current to the opposite arm by switching ON the director switches in both arms around the zero crossing of the phase voltage [178]. During this overlap period, a small dc circulating current can be injected in the phase leg of the AAC (through both arms towards the dc) to exchange energy between the SM capacitors and the dc filter capacitors and compensate small imbalances, which result in practice due to model inaccuracies in the energy expressions [66]. A full cycle overlap can be obtained by increasing the voltage rating of the FBSM stack to full dc voltage, however, with the drawback of doubling the cost and losses of the AAC [66]. Thus, this commutation overlap period is usually restricted to about 10° in conventional AAC, which considerably limits the energy balancing potential and hence restricts the AAC operation in proximity of the sweet-spot [178].

Given a specific voltage of the FBSM stack V_{stack}, the voltage of the director switch can be

written from KVL as

$$V_{\mathrm{ds}} = \hat{v}_{\mathrm{ac}} + \frac{V_{\mathrm{dc}}}{2} - V_{\mathrm{stack}} \ . \tag{5.31}$$

Inserting the sweet-spot definition (5.30) in (5.31) leads to

$$V_{\mathrm{ds}} = \frac{4+\pi}{2\pi} V_{\mathrm{dc}} - V_{\mathrm{stack}} \ . \tag{5.32}$$

Assuming equally distributed SM voltage in the stack, the number of FBSM in one arm of the AAC can be found with

$$n_{\mathrm{SM}} = \frac{V_{\mathrm{stack}}}{V_{\mathrm{SM}}} \ . \tag{5.33}$$

Thus the total number of active switches, including the series-connected IGBTs of the director switch (for which the same voltage rating as in the FBSM is assumed) can be obtained with

$$n_{\mathrm{IGBT}} = 6 \cdot (4 \cdot n_{\mathrm{SM}} + n_{\mathrm{ds}}) \ . \tag{5.34}$$

Assuming dc fault blocking capability of the AAC and short overlap period, it holds $V_{\mathrm{stack}} = \hat{v}_{\mathrm{ac}}$ and $V_{\mathrm{ds}} = \frac{V_{\mathrm{dc}}}{2}$ and hence (5.33) becomes

$$n_{\mathrm{IGBT}} = 6 \cdot \frac{4 \cdot \hat{v}_{\mathrm{ac}} + \frac{V_{\mathrm{dc}}}{2}}{V_{\mathrm{SM}}} \ . \tag{5.35}$$

Despite the already mentioned drawbacks of a limited operating area around the sweet-spot and the requirement of sharp transition in the arm current during the short overlap period, another challenge of the AAC is the substantial six-pulse ripple in the dc current (coming from the rectifier operation by the director switches) which requires for large dc-side filter capacitors, which are not only bulky and costly but potentially also endanger the system, when they discharge during a dc side short circuit fault [179].

To solve the above-mentioned problems, in [179] a novel operation mode for the AAC is presented, the extended overlap, i.e. the AAC works with 60° overlap period. With 60° overlap period in any conduction state, there are always exactly four arms conducting, two upper and two lower, of which one and only one upper and lower arm are in the same phase. This is important, since it guarantees a path for the dc current circulating through the AAC, which allows to balance the SM voltage with higher degree of freedom and in fact decouples the dc current from the rectification of the ac currents and hence obviates the need for bulky dc capacitors. Indeed, the ac currents sum to zero at the midpoint of the phase in conduction and are not transferred to the dc (which is referred to as active dc current filtering in [179]).

Thus, the sweet-spot does not longer exist in the extended overlap operation and the AAC can be operated away from its nominal operating point without balancing restrictions. A new optimal operating point has been found in [179] at $V_{\mathrm{ac}} = \frac{2}{3} V_{\mathrm{dc}}$, which results in smooth transition in the commutation and hence, no discontinuities occur in the arm current. This

has two advantages, first, a smooth current waveform releases the complexity of the current controller and second, the current returns to zero at the end of the arm's conduction period ensuring soft-switching operation of the director switch as demonstrated in [179].

As stated earlier, the extension of the overlap period influences the stack voltage and hence the number of FBSM to be installed in the AAC. The stack is controlled to maintain the ac voltage waveform quality and with the extension of the overlap period, it has to follow a voltage difference of more than half of the peak-to-peak phase voltage [179]. A possible control based solution in order to avoid the additional hardware is the injection of a third harmonic voltage $v_{3\mathrm{ac}}$. The arm voltage in this case is

$$v_{\mathrm{arm}} = \frac{V_{\mathrm{dc}}}{2} - (v_{\mathrm{ac}} + v_{3\mathrm{ac}}) \quad . \tag{5.36}$$

Thus, the third harmonic voltage injection decreases the positive peak of the arm voltage, while it increases the negative one. This makes better use of the bipolar voltage capability of the FBSM and reduces the required number of FBSM. However, this is only a compromise, as it increases the peak of the total converter voltage and hence increases the voltage rating of the director switches. With the proposed design and operation mode, [179] claims that the AAC's efficiency and number of semiconductors is comparable with the HMMC, while a smaller converter footprint can be achieved due to reduced passive components, namely the number of SM capacitors and arm inductor volume.

5.2.4. Hybrid cascaded multilevel converter

In [180] a novel hybrid cascaded multilevel converter (HCMC) topology is presented, which uses the 2L-VSC as the main power stage and a low-power FBSM chain link in each phase to the ac side. Initially, the FBSM chain link was intended as an active filter to attenuate the harmonic voltages generated by the 2L-VSC main power stage. To increase the ac voltage waveform quality, the HCMC can be also build with HB-MMC as the main power stage, which controls the active and reactive power exchange with the ac grid [181]. The HB-MMC must be rated at the full dc voltage, while the series connection of FBSM can be rated at half of the dc voltage (i.e. using the FBSM bipolar output voltage, their number is 25 % of the number of HBSM in the main power stage) to ensure the fault blocking capability. Fault blocking in the articles [180] and [181] is defined as preventing ac in-feed during dc short circuit faults. The blocked FB chain link acts as virtual dc link with reverse voltage to the ac side, but does not actively reduce the dc current, since the SM capacitors are not in the dc fault current path. As the focus of this thesis is the dc-side protection of the HVdc, the HCMC is not further analyzed.

5.2.5. Research question

Various hybrid architectures of the MMC have been presented in the literature, which aim to reduce the number of bipolar SM in order to reduce the on-state losses, while maintaining the dc fault blocking capability of the converter. In the following, a new perspective should be given to the efficiency-optimized design of the HA-MMC. The aim is to analyze the minimum number of bipolar SM (e.g. FBSM) in the hybrid arm MMC to achieve acceptable fault clearing time and SM over-voltages during the energy dissipation. Similar studies have been already presented for the hybrid MMC and should now be extended to the hybrid arm MMC. What differs with respect to the previous work is that the minimum number of bipolar SM will be found by analyzing the fault operation sequence of the HA-MMC, which has been originally presented by Iman-Eini et al in [182]. In consequence, the on-state losses in this hybrid arm MMC with reduced number of bipolar SM (RHA-MMC) can be decreased without losing the dc fault blocking capability. Additionally, analytical derivation of the worst-case over-voltage condition on the FBSM in the dc fault blocking state of the RHA-MMC is presented and the impact of SM capacitance and dc line inductance is studied.

5.3. Hybrid arm MMC with a reduced number of bipolar submodules and fault blocking capability

The following section, first briefly introduces the topology of the RHA-MMC. Then, the fault operation sequence of the HA-MMC is analyzed and extended to the case of the proposed architecture to analytically gather the minimum number of bipolar SM and the worst-case over-voltage, which occurs on the bipolar SM (here FBSM) in the upper arm of the RHA-MMC. Switch-level simulations in PSCAD/EMTDC environment are presented to verify the behavior of the proposed RHA-MMC. Finally, a comparison with other dc current interruption schemes is performed and its advantages and disadvantages under varying fault conditions are highlighted.

5.3.1. Topology of RHA-MMC

Fig. 5.16 depicts the three-phase topology of the RHA-MMC in asymmetric monopole configuration. In order to avoid the large SM over-voltage under ac pole-to-ground faults, the pure HBSM-based lower arm is located close to the ground pole, while the upper arm connected to the positive pole consists of a mixture of FBSM and HBSM. In the lower arm, n_{SM} HBSM are employed and in the upper arm n_{f} FBSM combined with $n_{\mathrm{h}} = n_{\mathrm{SM}} - n_{\mathrm{f}}$ HBSM. It has to be noted that this asymmetric structure limits the HA-MMC as well as the

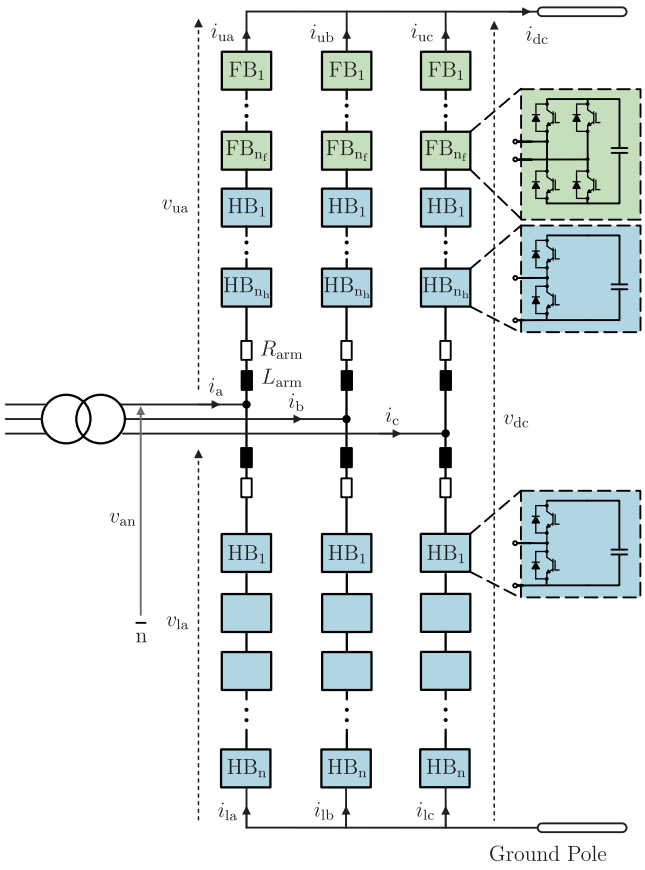


Fig. 5.16: Three-phase topology of the Hybrid Arm MMC with reduced number of bipolar submodules in asymmetric monopole HVdc configuration.

RHA-MMC application to asymmetric monopole and bipolar HVdc configuration. The implemented control scheme as explained in Subsection 2.3 can be split into dc voltage control (or active power for the slave terminal, respectively) and reactive power control acting on the phase currents on the one side and circulating current control on the other side to balance the arm voltages. The second order harmonic ripple in the circulating current is controlled to zero in order to relieve the semiconductors [70]. A phase shifted carrier modulation is used, which requires individual SM voltage balancing [65]. Thus, the SM voltage in both HBSM and FBSM is selected equally and a distributed SM voltage balancing control is implemented (more details can be found in Subsection 2.3).

5.3.2. DC fault current blocking capability of RHA-MMC

Hereafter, the initial fault operation sequence of the HA-MMC is investigated based on the analytical model originally developed in [182]. Initially, it is assumed to have only FBSM in the upper arm. It forms the basis to define the minimum number of FBSM required to successfully block a dc fault.

Following a P2G fault, the dc line current rapidly increases and reaches a pre-defined threshold (usually two or three times the nominal current). In consequence, all IGBTs in the SM

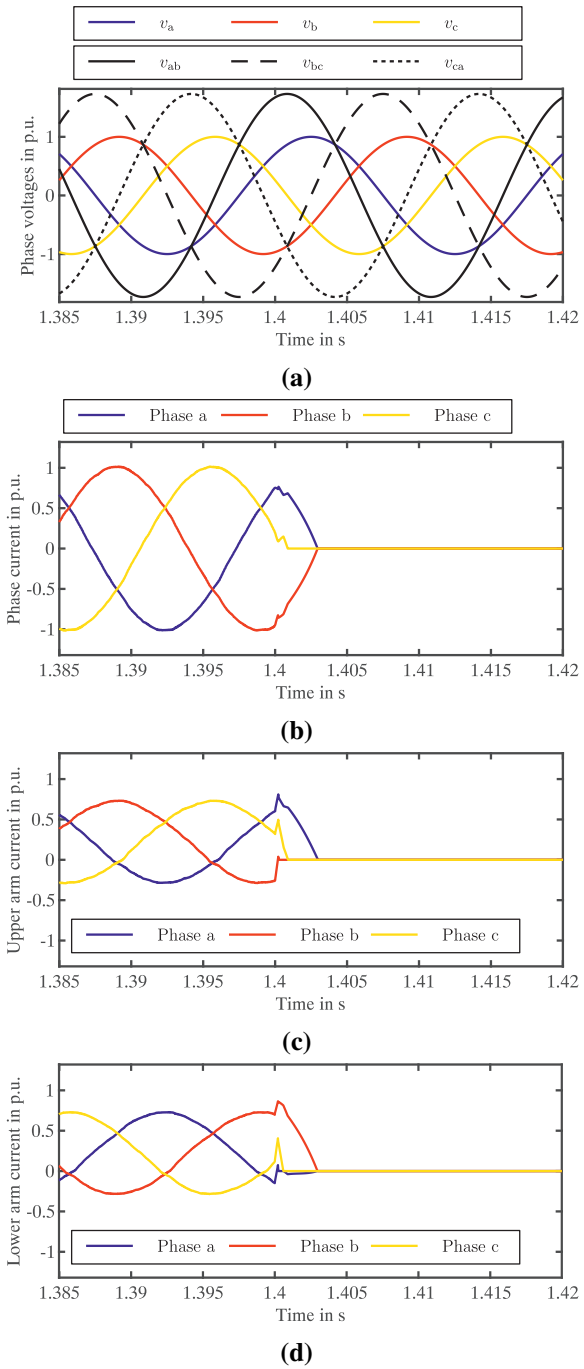


Fig. 5.17: Initial post-fault operation of HA-MMC: (a) Phase voltages, (b) Phase currents, (c) Upper arm currents, (d) Lower arm currents.

of the HA-MMC are switched OFF and the converter is in blocked state, which is shown in Fig. 5.18. Initially, the HA-MMC in blocked state is a six-diode rectifier and the FBSM in the upper arms insert a counter voltage equal to $n_f V_{SM} = V_{dc}$ and inversely biased to the fault current. The forward voltage drop across the free-wheeling diodes in the blocked SM is neglected. The following differential equation can be obtained, from which, neglecting the resistive voltage drop across the short circuit and arm resistances, it becomes obvious how

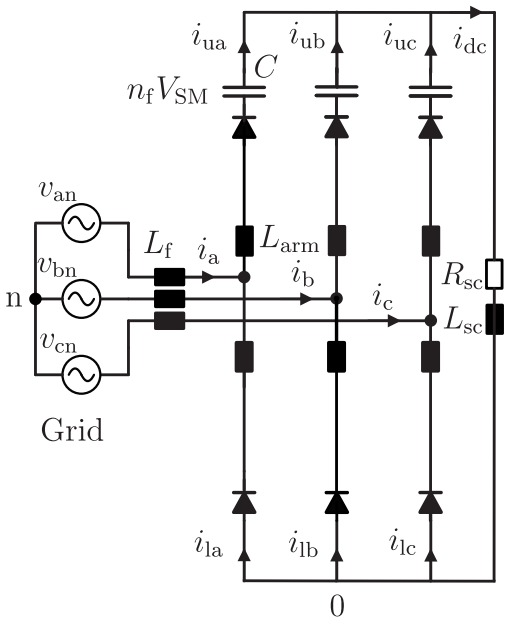


Fig. 5.18: Equivalent circuit model of RHA-MMC in blocking mode: Six-Diode Rectifier.

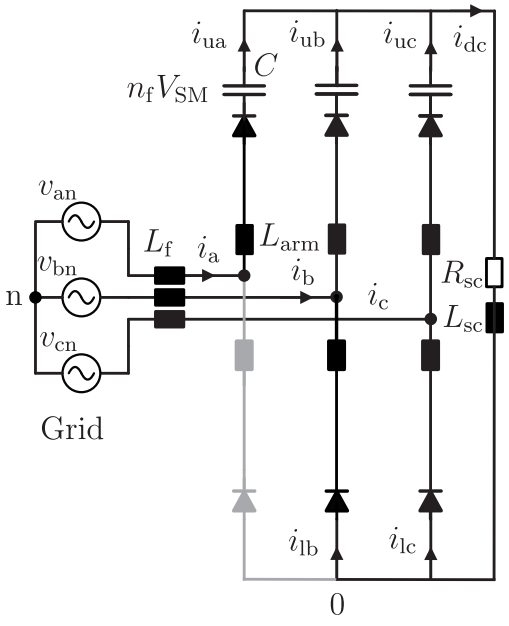


Fig. 5.19: Equivalent circuit model of RHA-MMC in blocking mode: Five-Diode Rectifier.

the inversely inserted sum of SM voltages decreases the fault current:

$$\left(L_{sc}+\frac{2}{3}L_{arm}\right)\frac{\mathrm{d}i_{dc}}{\mathrm{d}t}+\left(R_{sc}+\frac{2}{3}R_{arm}\right)i_{dc}=-V_{dc}\ . \tag{5.37}$$

Analyzing the mesh at the lower arms results in

$$L_{arm}\frac{\mathrm{d}i_{lx}}{\mathrm{d}t}+v_{xn}+v_{n0}=0\quad x=\mathrm{a},\mathrm{b},\mathrm{c}\ . \tag{5.38}$$

Now, assuming that the voltage between the neutral point and the dc side ground v_{n0} is

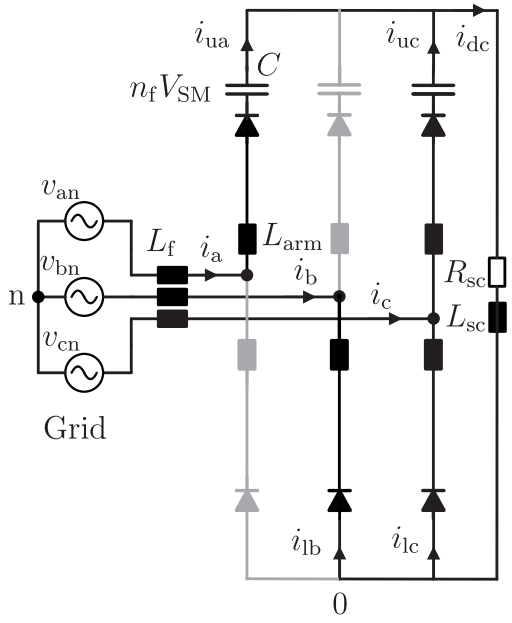


Fig. 5.20: Equivalent circuit model of RHA-MMC in blocking mode: Four-Diode Rectifier.

negligible compared to the phase voltage v_{xn}, the dynamics of lower arm currents can be expressed by

$$L_{arm}\frac{di_{lx}}{dt} \approx -v_{xn} \quad x = a,b,c \ . \tag{5.39}$$

Likewise, the dynamics of upper arm currents can be expressed with

$$L_{arm}\frac{di_{ux}}{dt} \approx v_{xn} \quad x = a,b,c \ . \tag{5.40}$$

From (5.39) and (5.40) three observations can be made: (1) For positive value of the phase voltage, the current in the corresponding lower arm is falling. (2) For negative value of the phase voltage, the current in the corresponding upper arm is falling. (3) For phase voltage values close to zero, neither the upper arm nor the lower arm current vary significantly. Thus, the lower arm current related to the phase with highest value, and the upper arm current related to the phase with lowest value, become zero first. Without loss of generality in the following it is assumed for the instantaneous phase voltages at the blocking instant $t = t_0$:

$$v_{bn}(t_0) < v_{cn}(t_0) < v_{an}(t_0) \ . \tag{5.41}$$

Considering (5.41), the current in the lower arm of phase a becomes zero (see Fig. 5.17), and the diode in the respective arm turns off. Hence, the HA-MMC switches into a five-diode rectifier mode (shown in Fig. 5.19). Similar to the six-diode rectifier operation before, the lowest instantaneous voltage leads to fastest reduction of the upper arm current of phase b (Fig. 5.17), which then becomes zero and the HA-MMC operation changes to four-diode rectifier mode (Fig. 5.20). In this stage, the current in one arm of the fully remaining phase (here the lower arm in phase c) becomes zero and the converter starts to behave as three-

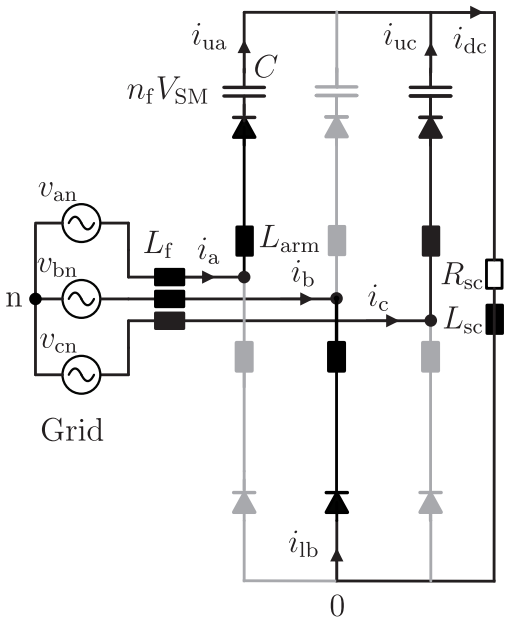


Fig. 5.21: Equivalent circuit model of RHA-MMC in blocking mode: Three-Diode Rectifier.

diode rectifier (Fig. 5.21). Essentially, the three-diode rectifier is similar to the commutation phase in the six-diode rectifier. It follows

$$\frac{\mathrm{d}i_{\mathrm{ua}}}{\mathrm{d}t} \approx -\frac{\mathrm{d}i_{\mathrm{uc}}}{\mathrm{d}t} \approx \frac{1}{2L_{\mathrm{arm}}} v_{\mathrm{ll,ac}} \ . \tag{5.42}$$

Thus, the line-to-line voltage between phase a and c $v_{\mathrm{ll,ac}}$ determines the current slope of upper arm currents. From Fig. 5.17, it can be observed that it is positive in the considered period and hence, the current commutates from phase c to phase a (i_{uc} becomes zero). In the final stage, the HA-MMC resembles a two-diode rectifier. From Fig. 5.22, the fault current dynamics in the final stage can be written as

$$(L_{\mathrm{sc}} + 2L_{\mathrm{arm}}) \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} + R_{\mathrm{sc}} i_{\mathrm{dc}} = v_{\mathrm{rect}} \ , \tag{5.43}$$

in which $v_{\mathrm{rect}} = -V_{\mathrm{dc}} + (\max(v_{\mathrm{an}},\, v_{\mathrm{bn}},\, v_{\mathrm{cn}}) - \min(v_{\mathrm{an}},\, v_{\mathrm{bn}},\, v_{\mathrm{cn}}))$ is the rectified output voltage of the HA-MMC. In fact, the two-diode rectifier operation is similar to that of a six-diode rectifier, in which only one diode in the upper and one diode in the lower arm can conduct simultaneously. Thus, its rectified output voltage is also of similar shape plus a dc offset determined by the counter voltage inserted by the FBSM in the remaining upper arm. Considering $(L_{\mathrm{sc}} + 2L_{\mathrm{arm}})$ is a large inductance, the rectified voltage can be replaced by its dc equivalent and it follows for the HA-MMC with only FBSM in the upper arm:

$$(L_{\mathrm{sc}} + 2L_{\mathrm{arm}}) \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} + R_{\mathrm{sc}} i_{\mathrm{dc}} = -V_{\mathrm{dc}} + \frac{3\sqrt{3}}{\pi} \hat{v}_{\mathrm{ac,ph}} \ . \tag{5.44}$$

In fact, the equation (5.43) can be generalized for an arbitrary number of FBSM in the upper

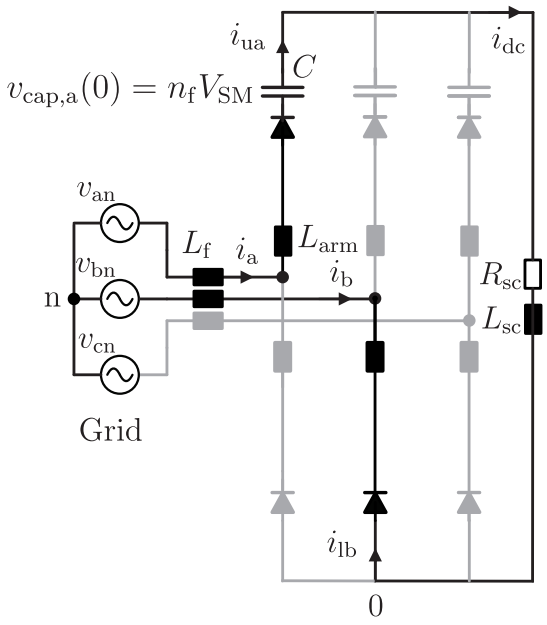


Fig. 5.22: Equivalent circuit model of RHA-MMC in blocking mode: Two-Diode Rectifier, when $v_{\mathrm{bn}} < v_{\mathrm{cn}} < v_{\mathrm{an}}$.

arm n_{f} of the HA-MMC, which are each charged to V_{SM} by:

$$(L_{\mathrm{sc}} + 2L_{\mathrm{arm}}) \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} + R_{\mathrm{sc}} i_{\mathrm{dc}} = -n_{\mathrm{f}} V_{\mathrm{SM}} + \frac{3\sqrt{3}}{\pi} \hat{v}_{\mathrm{ac,ph}} \ . \tag{5.45}$$

Thus, from (5.45) it is evident that to finally drive the fault current to zero and hence successfully block the fault, the reverse blocking voltage by the series connection of FBSM must fulfill

$$n_{\mathrm{f}} V_{\mathrm{SM}} > \frac{3\sqrt{3}}{\pi} \hat{v}_{\mathrm{ac,ph}} \ . \tag{5.46}$$

It is assumed that the SM voltages are ideally balanced, hence it holds $V_{\mathrm{SM}} = \frac{V_{\mathrm{dc}}}{n}$ and from (5.46) it follows:

$$\frac{3\sqrt{3}}{\pi} \hat{v}_{\mathrm{ac,ph}} < \frac{n_{\mathrm{f}}}{n_{\mathrm{SM}}} V_{\mathrm{dc}} \ . \tag{5.47}$$

Assuming there are no negatively inserted FBSM in normal operation, the internal emf of the MMC is less or equal to $\frac{V_{\mathrm{dc}}}{2}$. From (2.1) and (2.4) it follows that to generate reactive power, the internal emf must be greater than (or in worst case equal to) the peak of the ac phase voltage $\hat{v}_{\mathrm{ac,ph}}$. Consequently, for operation in linear modulation range $\hat{v}_{\mathrm{ac,ph}}$ should be lower than or in worst case equal to $\frac{V_{\mathrm{dc}}}{2}$. Replacing $\hat{v}_{\mathrm{ac,ph}} = \frac{V_{\mathrm{dc}}}{2}$ in (5.47), the minimum number of FBSM $n_{\mathrm{f,min}}$ in the HA-MMC can be derived:

$$\frac{3\sqrt{3}}{\pi} \frac{\hat{v}_{\mathrm{ph}}}{V_{\mathrm{dc}}} < \frac{n_{\mathrm{f}}}{n_{\mathrm{SM}}} \rightarrow \frac{3\sqrt{3}}{\pi} \cdot \frac{1}{2} = \frac{n_{\mathrm{f,min}}}{n_{\mathrm{SM}}} \rightarrow n_{\mathrm{f,min}} = 0.827 n_{\mathrm{SM}} \ . \tag{5.48}$$

5.3.3. Submodule over-voltage determination of RHA-MMC in fault blocking state

In the presented analysis to determine the minimum number of FBSM, it was initially assumed that the capacitor voltage in all SM stays constant during the blocked state of the MMC. However, being negatively inserted in the current path, the capacitors of the FBSM will be charged by the arm current flow through the anti-parallel diodes, until the current decays to zero. Hence, in order to estimate the amount of voltage increase in the blocked FBSM, the arm current dynamics during the blocked state of the RHA-MMC must be determined first.

From the post-fault operation sequence explained in Subsection 5.3.2, the worst case condition for the voltage increase occurs in the FBSM in the remaining upper arm (the one with the highest phase voltage) in the final two-diode rectifier state of the RHA-MMC. In the analysis, for the sake of simplicity it is assumed that the time of other arm currents (shown in gray in Fig. 5.22) to become zero after the blocking instant is negligible. Hence, the initial time $t = 0$ corresponds to the blocking instant as well as the time, when other arm currents became zero.

The corresponding equivalent circuit under the condition $v_{\mathrm{bn}} < v_{\mathrm{cn}} < v_{\mathrm{an}}$ is shown in Fig. 5.22.

Taking the KVL of the fault current loop from Fig. 5.22 results in

$$\frac{1}{C_{\mathrm{arm}}}\int_0^t i_{\mathrm{ua}}\mathrm{d}\tau + \left(L_{\mathrm{sc}} + 2\left(L_{\mathrm{arm}} + L_{\mathrm{f}}\right)\right)\frac{\mathrm{d}i_{\mathrm{ua}}}{\mathrm{d}t} + R_{\mathrm{sc}}i_{\mathrm{ua}} = v_{\mathrm{an}} - v_{\mathrm{bn}} - v_{\mathrm{cap,a}}(0) \ , \tag{5.49}$$

with $C_{\mathrm{arm}} = \frac{C_{\mathrm{SM}}}{n_{\mathrm{f}}}$ being the equivalent capacitance of the series connected FBSM in one arm of the RHA-MMC, v_{an} and v_{bn} the line-to-neutral phase voltages of remaining phases a and b, and $v_{\mathrm{cap,a}}(0) = V_{\mathrm{dc}}\frac{n_{\mathrm{f}}}{n_{\mathrm{SM}}}$ the initial arm voltage across the equivalent capacitor of FBSM in phase a. It needs to be noted that the current and voltage variables are all time dependent, however, for readability purposes the time dependency is not explicitly expressed. The above ordinary integro-differential equation can be solved by determining the initial conditions $i_{\mathrm{ua}}(0)$ and $\frac{\mathrm{d}i_{\mathrm{ua}}}{\mathrm{d}t}(0)$. Obviously, the difference between the phase-to-neutral voltages in (5.49) is the line-to-line voltage $v_{\mathrm{ll,ab}}$, which can be expressed by

$$v_{\mathrm{ll,ab}} = \sqrt{3}\hat{v}_{\mathrm{ac,ph}}\sin\left(\omega t + \theta_0\right) \ , \tag{5.50}$$

in which $\hat{v}_{\mathrm{ac,ph}}$ is the amplitude of the phase-to-neutral voltage and θ_0 is the initial phase angle of $v_{\mathrm{ll,ab}}$ at $t = 0$. Assuming the fault resistance R_{sc} is approximately zero, i.e. ideal short circuit condition, the initial condition for the arm current derivative can be obtained as

$$\frac{\mathrm{d}i_{\mathrm{ua}}}{\mathrm{d}t}(0) = \frac{\sqrt{3}\hat{v}_{\mathrm{ac,ph}}\sin\left(\theta_0\right) - v_{\mathrm{cap,a}}(0)}{L_{\mathrm{sc}} + 2\left(L_{\mathrm{arm}} + L_{\mathrm{f}}\right)} \tag{5.51}$$

The current in the upper arm can be generally expressed with

$$i_{\mathrm{ua}} = \frac{i_{\mathrm{dc}}}{3} + \frac{i_{\mathrm{sa}}}{2} \ . \tag{5.52}$$

If a dc fault occurs, the dc current i_{dc} quickly rises until it reaches a predefined threshold I_{trip} and the MMC is blocked. Thus, the initial dc current in (5.52) equals the trip threshold current. Moreover, to predict the maximum SM capacitor over-voltage the maximum arm current has been assumed. Thus, the ac phase current in (5.52) can be replaced by its peak value $\hat{i}_{\mathrm{ac,ph}}$ and it follows:

$$i_{\mathrm{ua}}(0) = \frac{I_{\mathrm{trip}}}{3} + \frac{\hat{i}_{\mathrm{ac,ph}}}{2} \ . \tag{5.53}$$

Now, the ordinary integro-differential equation in (5.49) can be solved with

$$i_{\mathrm{ua}}(t) = K \sin\left(\omega_0 t + \kappa\right) + \frac{A}{\omega_0^2 - \omega^2} \cos\left(\omega t + \theta_0\right) \tag{5.54}$$

with

$$A = \frac{\sqrt{3}\hat{v}_{\mathrm{ac,ph}}\omega}{L_{\mathrm{sc}} + 2\left(L_{\mathrm{arm}} + L_{\mathrm{f}}\right)} \tag{5.55}$$

and

$$\omega_0 = \frac{1}{\sqrt{\left(L_{\mathrm{sc}} + 2\left(L_{\mathrm{arm}} + L_{\mathrm{f}}\right)\right) C_{\mathrm{arm}}}} \ . \tag{5.56}$$

The first term in (5.54) represents the homogeneous solution and the second term the particular solution of (5.49). Considering the initial conditions, the constants K and κ can be determined with

$$K = \frac{i_{\mathrm{ua}}(0) - \frac{A}{\omega_0^2 - \omega^2} \cos\left(\theta_0\right)}{\sin\left(\kappa\right)} \tag{5.57}$$

and

$$\kappa = \arctan\left(\frac{i_{\mathrm{ua}}(0) - \frac{A}{\omega_0^2 - \omega^2} \cos\left(\theta_0\right)}{\frac{\frac{\mathrm{d}i_{\mathrm{ua}}}{\mathrm{d}t}(0)}{\omega_0} + \frac{A\omega}{\omega_0\left(\omega_0^2 - \omega^2\right)} \sin\left(\theta_0\right)} \right) \ , \tag{5.58}$$

respectively. Now, the voltage increase at each SM capacitor in the FBSM in the upper arm of phase a $\Delta v_{\mathrm{fbsm,a}}$ can be calculated by

$$\begin{aligned} \Delta v_{\mathrm{fbsm,a}} &= \frac{1}{C_{\mathrm{SM}}} \int_0^t i_{\mathrm{ua}}(\tau) \mathrm{d}\tau \\ &= \frac{K}{\omega_0 C_{\mathrm{SM}}} \left(\cos\kappa - \cos\left(\omega_0 t + \kappa\right)\right) + \frac{A}{\omega C_{\mathrm{SM}}\left(\omega_0^2 - \omega^2\right)} \left(\sin\left(\omega t + \theta_0\right) - \sin\theta_0\right) \ . \end{aligned} \tag{5.59}$$

Equation (5.59) describes the worst case scenario for the maximum voltage increase at the SM capacitors depending on the SM capacitance, the arm, filter and short circuit inductance and the line-to-line voltage amplitude and initial phase angle.

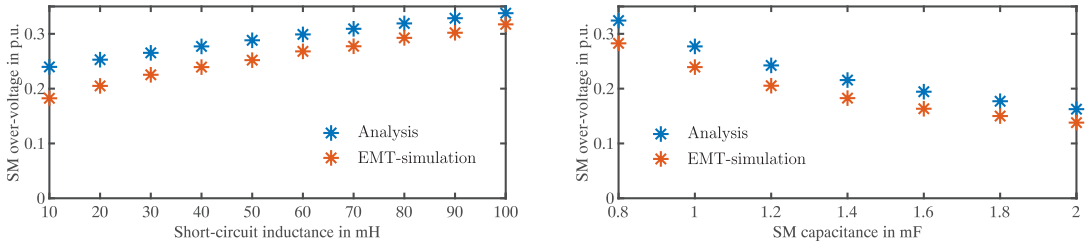


Fig. 5.23: Submodule over-voltage in RHA-MMC: (a) Varying short circuit inductance L_{sc}, (b) Varying SM capacitance C_{SM}.

Two study cases are presented for the maximum voltage increase. First, in Fig. 5.23(a), it is assumed $C_{SM} = 1$ mF, which corresponds to an energy storage requirement of 45 $\frac{kJ}{MW}$, and the fault distance is varied by varying the short circuit inductance L_{sc}. In the second case, shown in Fig. 5.23(b), the fault distance is kept constant at approximately 50 km away from the MMC, which corresponds to $L_{sc} = 40$ mH, while the SM capacitance is varied. The analytical estimation of the voltage increase is validated with PSCAD/EMTDC simulations and it results an approximately constant modeling deviation of less than 5 % of the observed over-voltage. The analysis is based on the simplification that the FBSM capacitors of only a single upper arm absorb the fault energy. However, in the simulation the second (and with very minor impact also the third) upper arm contribute in the fault clearing by absorbing part of the fault energy as well. Thus, the analytical results always exceed the simulation ones. Nevertheless, in order to follow a conservative design approach, the over-estimated analytical results are valid and applicable.

5.3.4. Simulation results of RHA-MMC

In the following, simulation results in PSCAD/EMTDC environment are presented in order to evaluate the dc fault current blocking capability of the hybrid arm MMC with reduced number of bipolar SM. In this case, the well-adopted FBSM is used.

The system under study is a point-to-point HVdc link in asymmetric monopole configuration with metallic return, in which the lower pole is the ground pole. Following the findings of [52], the worst case scenario for the SM over-voltage during the blocked state occurs in the rectifier terminal of the HVdc system, while the general fault current blocking capability does not depend on the terminal type or control design, but just on the hardware design, i.e. the number of FBSM and SM capacitance to generate sufficient blocking voltage. Hence, only the rectifier MMC, which is operated as master controlling the dc bus voltage, is modeled at switch level and connected to a resistance on the dc side. The short circuit path is modeled with series resistance $R_{sc} = 0.1\ \Omega$ resembling ideal short circuit conditions and inductance $L_{sc} = 40$ mH representing a fault in an overhead transmission line 50 km away from the

Table 5.14: Parameters of the RHA-MMC and HVdc system under study (Base voltage $V_b = 150$ kV, base power $P_b = 150$ MW).

Quantity	Symbol	Value	*per unit* Value
Nominal power	P_{nom}	150 MW	1 p.u.
Peak phase voltage	$\hat{v}_{ac,ph}$	66 kV	0.44 p.u.
Nominal dc voltage	V_{dc}	150 kV	1 p.u.
Nominal dc line current	I_{dc}	1 kA	1 p.u.
Number of SM per arm	n_{SM}	10	
Number of FBSM in upper arm	n_f	8	
Number of HBSM in upper arm	n_h	2	
Nominal MMC SM voltage	V_{SM}	15 kV	
SM capacitance	C_{SM}	1 mF	0.021 p.u.
Arm inductance	L_{arm}	30 mH	0.063 p.u.
Arm resistance	R_{arm}	10 mΩ	0.000067 p.u.
AC filter inductance	L_f	10 mH	0.021 p.u.
AC filter resistance	R_f	10 mΩ	0.000067 p.u.
Trip threshold current	I_{trip}	2 kA	2 p.u.

MMC. No additional dc fault current limiting inductance is considered. It should be noted that in order to speed up the simulation, the number of SM is chosen small, which is common practice in MMC related studies [183]. The parameters of the studied system are shown in Table 5.14.

RHA-MMC dc fault current blocking capability First, the HVdc system is working in normal condition, i.e. the RHA-MMC is controlling the dc voltage to its nominal value, while the power flow is determined by the chosen dc resistance value. At $t = 1.4$ s a short circuit to ground is introduced between the two poles of the HVdc systems. The dc voltage collapses and the dc line current increases rapidly as shown in Fig. 5.24. The fault is detected, if the dc fault current exceeds a pre-defined over-current threshold (here two times the nominal dc line current) and consequently all SM in the RHA-MMC are blocked. Communication delays in the detection are neglected. The corresponding waveforms of dc line current i_{dc}, dc voltage v_{dc}, phase current $i_s = [i_{sa}, i_{sb}, i_{sc}]$, upper and lower arm currents $i_u = [i_{ua}, i_{ub}, i_{uc}]$ and $i_l = [i_{la}, i_{lb}, i_{lc}]$, and SM voltage in the upper arm are shown for a zoomed view around the fault instant in Fig. 5.24.

As Fig. 5.24 shows, the RHA-MMC can block the fault current effectively and reduce it to zero in less than 4.8 ms. During the whole clearing time, the dc fault current is monotonically decreasing, which proves the sufficient counter voltage provision by the reduced number of FBSM in the RHA-MMC. In practical applications, the SM IGBTs are rated for higher voltages than the actually applied SM voltage (which is usually around $45-55\%$ of the IGBT rating) and thus the temporary over-voltage can be tolerated. In the presented study case, the maximum over-voltage across the FBSM capacitor in the upper arm of phase a

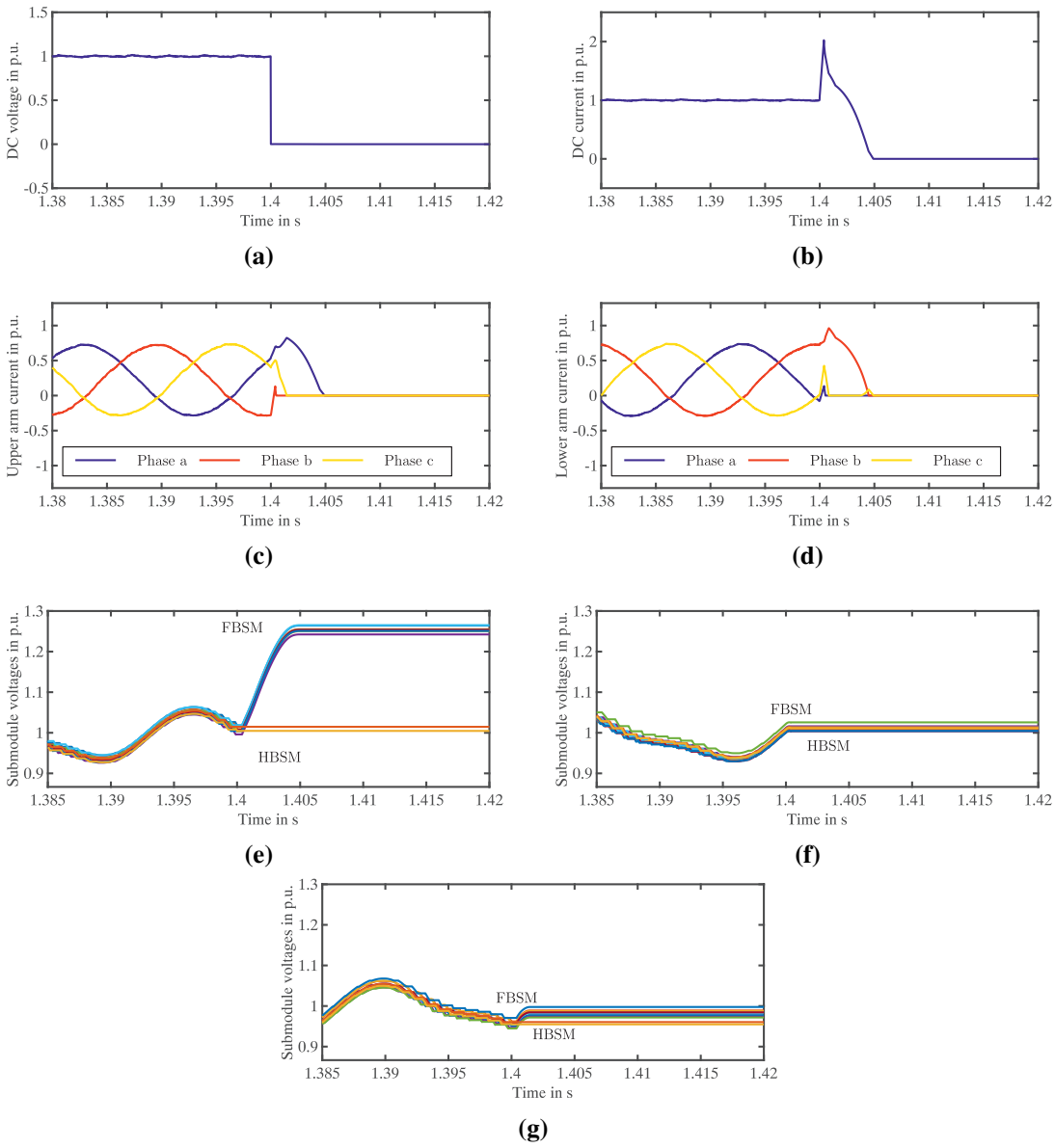


Fig. 5.24: Fault blocking performance of proposed RHA-MMC: (a) DC voltage, (b) DC current, (c) Upper arm current, (d) Lower arm current, (e) SM over-voltage in upper arm of phase a, (f) SM over-voltage in upper arm of phase b, (g) SM over-voltage in upper arm of phase c.

(which is the worst case) is 24.5 %.

Comparison of dc fault current blocking performance In the following, a comparison between conventional HA-MMC, FB-MMC, HB-MMC with hybrid dc circuit breaker, and the proposed RHA-MMC is made considering two operating conditions, i.e. short (12.5 km $\rightarrow L_{sc} = 10$ mH) and long (125 km $\rightarrow L_{sc} = 100$ mH) fault distance to the converter, respectively. The aim is to analyze the RHA-MMC behavior and compare it to other methods in terms of fault blocking time and resulting SM over-voltage.

In Fig. 5.25, a short fault distance to the converter is assumed. Under this condition, the

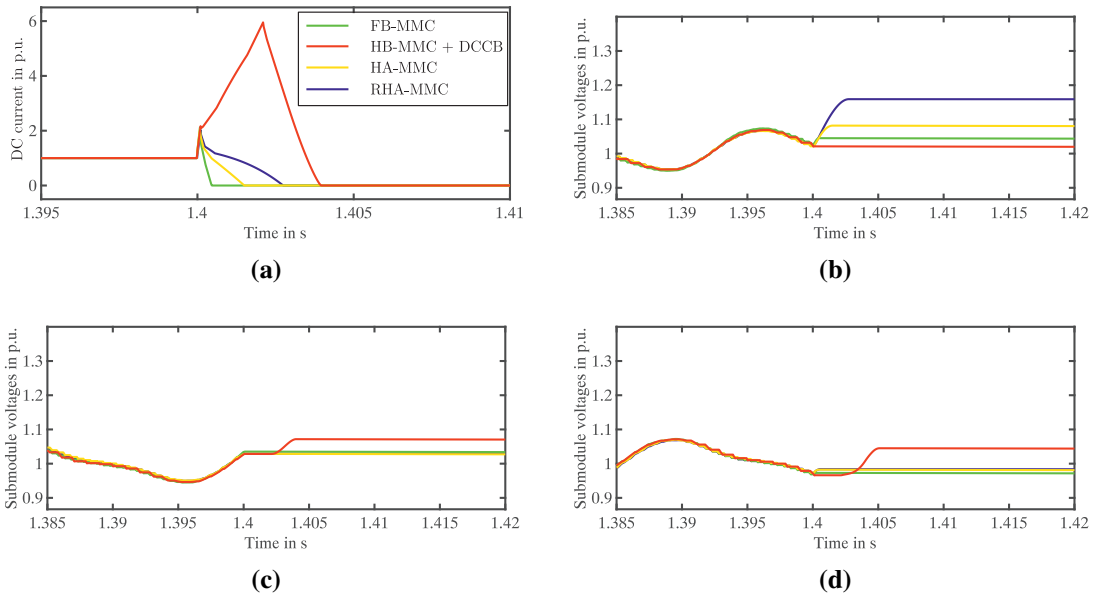


Fig. 5.25: Comparison of fault blocking performance of different MMC architectures with low dc side inductance ($L = 10$ mH): (a) DC current, (b) SM over-voltage in phase a, (c) SM over-voltage in phase b, (d) SM over-voltage in phase c.

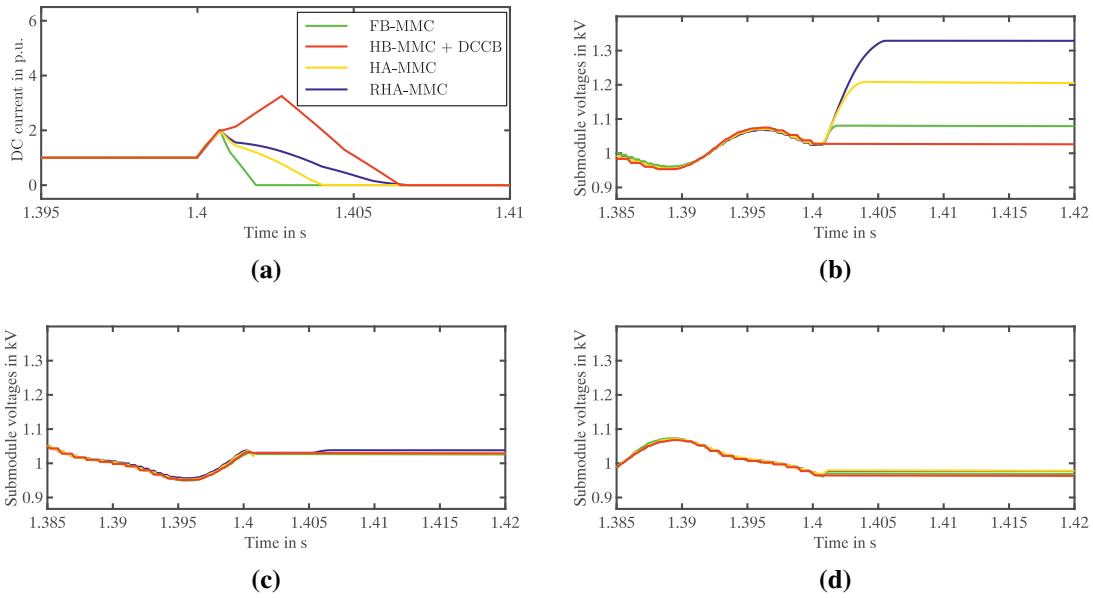


Fig. 5.26: Comparison of fault blocking performance of different MMC architectures with high dc side inductance ($L = 100$ mH): (a) DC current, (b) SM over-voltage in phase a, (c) SM over-voltage in phase b, (d) SM over-voltage in phase c.

RHA-MMC can interrupt the fault current in less than 2.7 ms with SM capacitor over-voltage less than 16%. With high fault distance, which reflects in high dc side inductance, the amount of stored inductive fault energy that the converter must dissipate is also high. Thus, as depicted in Fig. 5.26, the fault interruption time increases to 6.7 ms and the over-voltage reaches 33 %, which is still tolerable (from the IGBTs point-of-view) considering the usual operating voltage.

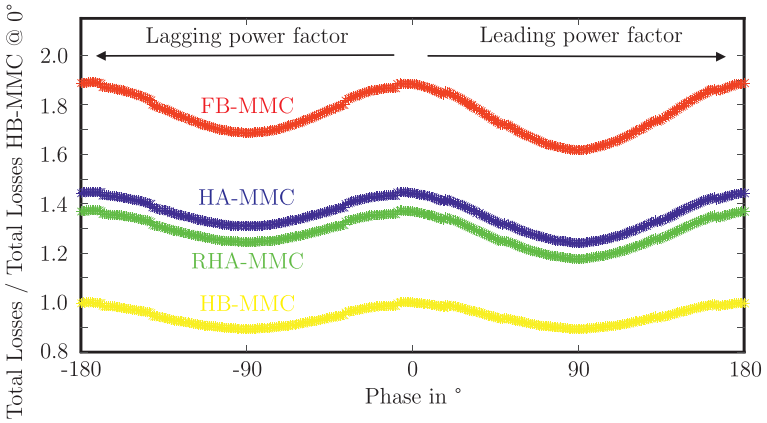


Fig. 5.27: Comparison of total losses as a function of phase difference and constant apparent power (the employed device for losses calculation is a 4.5 kV 1.2 kA IGBT (5SNA 1200G450300) from ABB). Total losses of HB-MMC are selected as the base power unit (1 p.u.) at different phase angles. Results obtained from [184].

The main challenge of the HB-MMC with hybrid dc CB is its long breaking time, i.e. the time the protection system needs to identify the fault and start the energy dissipation process. The mechanical switch introduces a significant delay of ≈ 2 ms involving high peak fault current, which potentially endangers the system's components. To mitigate such effects, additional dc current limiting inductors have to be installed at each end of the line (further details can be found in Section 4). Additionally, the dc CB suffers from the high amount of fault energy that the arrester has to dissipate in a short time, thus, accounting for high transient interruption voltage across the dc CB, e.g. 1.5 times the nominal dc voltage has been assumed in accordance with [40].

In comparison to the proposed RHA-MMC and the hybrid dc CB, the FB-MMC and HA-MMC show better interruption performance (FB: <0.5 ms for low dc inductance, 1.9 ms for high dc inductance, HA-MMC: <1.5 ms and 4 ms). However, a weak point of these methods is the large number of semiconductors, which involves low efficiency in normal operation as demonstrated in Fig. 5.27. Similar to the RHA-MMC, a large fault distance (or large dc inductance) creates over-voltages in the SM capacitors in the FB-MMC and HA-MMC as well.

The over-voltage across the SM capacitors is the result of the transfer of inductive energy stored in the dc and arm inductances and the energy flow from the ac side during the diode rectifier operation of the MMC until the phase currents are zero. Large fault distance or in general a large dc side inductance leads to a high amount of stored energy and hence long clearing time. In consequence, the ac energy flow is further incremented and so is the SM over-voltage. On one hand, this causes temporary over-voltage stress in the SM capacitors, which is, however, limited for very short time and is well below the breakdown threshold. Thus, it won't cause internal temperature or leakage current increase and is irrelevant for the capacitor lifetime. On the other hand, the SM over-voltage increases the blocking voltage of

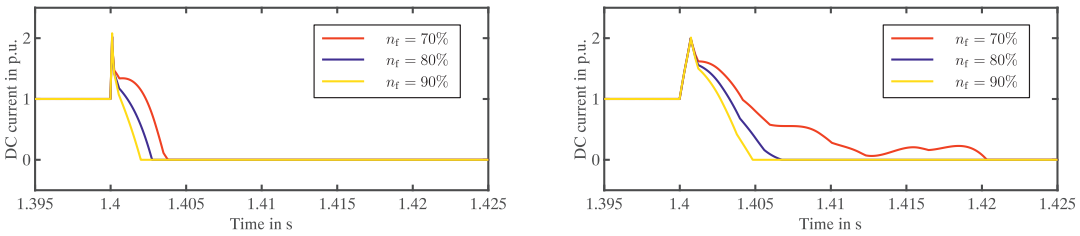


Fig. 5.28: DC current of proposed RHA-MMC with varying number of FBSM: (a) Low dc inductance ($L = 10$ mH), (b) High dc inductance ($L = 100$ mH).

each individual bipolar SM and hence enables fault blocking capability in the RHA-MMC also with less than the originally calculated 83% FBSM in operation. This feature can be used to continuously provide the fault protection to the dc grid, even if a small number of SM fail (e.g. due to internal short circuit).

Fig. 5.28 depicts three design cases of the RHA-MMC with 70%, 80% and 90% FBSM in the upper arm, respectively. Even though reducing the number of FBSM from 90% to 80% raises the clearing time, the SM over-voltage ensures sufficient counter voltage to successfully block the dc current. In contrast, the reduction to 70% results in uncontrolled commutation in case of high dc side inductance in later fault stages. This leads to periods with increasing current (between $t = 1.41$ s and $t = 1.42$ s) and a safe current blocking cannot be ascertained anymore.

5.4. Summary and conclusions of the section

In this section, MMC architectures with fault current blocking capability and suitable bipolar or asymmetric SM topologies for those are reviewed. The FBSM-based MMC, while it has the best fault blocking performance, suffers from its high on-state losses and costs. Therefore, hybrid or hybrid arm architectures have been developed in the past years, which comprise of a mixture of bipolar or asymmetric SM (with fault blocking capability) and the cost-efficient HBSM. In this thesis, a new perspective on the hybrid arm MMC with reduced number of bipolar SM is given, whereas both the minimum number of bipolar SM and the resulting over-voltage across them during the fault are developed analytically based on the fault operational sequence of the converter. PSCAD-EMTDC simulations of a full-switching model of the proposed RHA-MMC are presented to prove the analytical findings. In general, the HA-MMC is an asymmetric converter, which can be only applied in bipolar or asymmetrical monopolar HVdc configuration, because of its inability to clear a dc pole-to-ground fault at its HBSM-based arm.

The RHA-MMC shows acceptable fault blocking performance, e.g. relatively short clearing

time and low SM over-voltage, when the dc side inductance is small. However, if the dc side inductance is large (as it would be the case for remote faults in long HVdc links), the RHA-MMC experience large SM over-voltage due to the increased fault energy, which must be dissipated by the FBSM. This over-voltage must be considered in the design of the SM (IGBT and capacitor rating), however, assuming the conventionally applied operating voltage around 45 % to 55 % of the nominal voltage, the maximum over-voltage observed is still tolerable.

A common point of converter-based protection concepts is that they are non- or at most partially selective. Thus, their application in MTdc systems is restricted, since in case of fault the whole grid or larger parts of the grid have to be shut down. On the other hand, a fully selective strategy requires dc CB at both ends of each line. The increase in costs and complexity of protection coordination limits their expandability to larger meshed grids with a large number of lines. A compromise between selectivity and expandability is a critical task to be solved for future protection concepts.

A possible extension of the presented work is the application of RHA-MMC together with low-scale dc CB. It has to be evaluated, if using the combined approach, a further decrease in the total number of power electronics switches installed in the circuit (MMC + dc CB) can be achieved.

As a consequence of the converter blocking, the active power transmission (and for short time also the reactive power exchange) is interrupted. However, since HVdc systems usually participate in the ac grid voltage regulation by compensating reactive currents, it is desirable to limit the outage time and to regain the STATCOM functionality as soon as possible. This is especially important since due to the missing active power, the ac grid stability is already weakened.

It is assumed that a temporary fault happened. Nevertheless, the FBSM stay in blocked state for about $0.2 - 0.5$ s after current zero to account for typical de-energization time needed to let the arc at the fault location extinguish and the ionized air to disappear. Thus, for the STATCOM operation only the lower arm HBSM may be usable in the proposed converter topology, which may then be operated as star-connected cascaded HB STATCOM. Future work has to address the development of the STATCOM controller and evaluate the influence of the reactive power provision on the converter design. As a reference, in [185], a STATCOM control structure has been presented for the conventional HA-MMC in bipolar HVdc configuration, which includes an outer loop reactive power controller acting on the q-axis current reference and an average capacitor voltage controller acting on the d-axis current reference. The inner current loop is the same as in normal operation.

6. Summary, conclusions and future research

6.1. Summary and conclusions

This thesis aimed to investigate and propose new modeling, control and protection methods for HVdc systems based on modular multilevel converter, targeting an increased controllability of the transmission system.

In Section 2 the theoretical basis of this thesis has been presented by introducing the state-of-the-art knowledge on VSC-HVdc systems, their converter and grid control methods, and protection concepts. Moreover, the MMC fundamental operation and controller design has been explained. Furthermore, a guideline for power electronics modeling depending on the investigated power system problem has been presented.

The services, VSC-HVdc systems can provide to the ac grid, have been summarized in Section 3. Studying the recent implementations of frequency service support, i.e. primary frequency regulation and inertia emulation, has revealed a common drawback. In fact, if no additional source of energy as batteries or connected wind farms is available, significant frequency disturbances are caused in the supporting areas, which limit the control margin of the support action. Moreover, it has been shown that the conventional frequency support methodologies using power transfer between two areas cannot be applied to embedded HVdc systems, due to the strong synchronous coupling between the frequencies at the two terminals of the HVdc system in this application. As a solution, it has been proposed to shape the power consumption of voltage dependent loads in the proximity of the HVdc system by controlled grid voltage variation. Thus, additional energy independent of the synchronous generators is made available and the same frequency service as before can be provided, however, without affecting the frequency in supporting areas. Two study cases have been analyzed, which are the asynchronous HVdc interconnector and embedded HVdc system forming a parallel, hybrid connection with the surrounding ac grid. The effects of the so-called primary frequency regulation through HVdc-based control of voltage dependent loads have been analytically studied for both cases using a state-space model of an HVdc-interconnected modification of a two-area, two-machine benchmark system. The results have been verified in PSCAD/EMTDC simulations. First, using the two-area, four-machine Kundur benchmark grid and second using the large interconnected IEEE 39-bus system to justify the effectiveness of the approach in the truly embedded scenario. It has been demonstrated that using the proposed approach limits the frequency drop in supporting areas from 300 mHz to 50 mHz in the case of an asynchronous HVdc link and the frequency deviation at both terminals in the embedded case by 30 % independently of the system inertia. Possible restrictions of the proposed frequency support scheme in terms of the load power to voltage sensitivity, the restrictions in maximum change of the grid voltage as well as the loads electrical distance

to the HVdc terminals have been thoroughly studied. It can be concluded that even in the presence of mainly low-sensitive loads, only the control margin of the proposed approach is reduced, but still a generally positive effect on the damping in supporting areas is achieved. In order to tackle the restrictions in the allowed maximum change in the grid voltage, the proposed frequency support scheme has been extended to multi-terminal HVdc systems, in which the flexible power routing options, allow to optimally share the frequency support burden among the different terminals by adapting the droop constants proportionally to the estimated load power to voltage sensitivity in each area. The grid voltage variation using the optimal droop gains has been reduced by 1.2 % compared to the equal load power extraction, which led to reactive power savings of 25 %.

The design of dc circuit breakers is a crucial aspect in the development of MTdc systems. Therefore, in Section 4 a generalized list of criteria has been introduced to evaluate and compare the suitability of a given CB design, which is obtained from an in-depth literature survey on the requirements of HVdc CB and on commercially available HVdc CB designs. The central part of Section 4, however, is the development of an analytical fault current estimation method based on mesh analysis with linear differential equations and modified average value model of the MMC. It has been demonstrated that the proposed method provides accurate estimation of the fault current slope and maximum fault current for the initial fault stage until the moment of converter blocking and allows to analyze a large number of parameter variations for several grid conditions with very low computational time in comparison to detailed EMT-simulations (seconds instead of minutes). Moreover, it can be concluded that the proposed methodology overcomes critical drawbacks of existing methodologies using the linear differential equation approach. First, instead of relying on oversimplified, passive RLC-modeling of the MMC, it respects the power flow through the converter during the initial fault stage by including parts of the MMC control, which leads to more accurate results for remote fault currents in MTdc systems. Second, it is applicable not only to a single fault type, but to pole-to-pole faults in symmetrical monopole and bipolar grid configuration as well as to pole-to-neutral faults in bipolar grid configuration, which is possible by the introduction of a virtual fault path in the set of differential equations. The analytical derivations have been proven with PSCAD/EMTDC simulations of the four-terminal CIGRE B4 multi-terminal HVdc benchmark grid, resulting in a maximum estimation error of 3 % instead of ≈ 6 % with the simplified MMC model. In the remainder of the Section 4, a fault identification and adaptive auto-reclosing strategy using a modular, hybrid HVdc circuit breaker has been presented. In fact, it has been proposed to create active pulses in the line through controlled bypassing of a specified number of main breaker modules and to analyze the resulting traveling waves to identify the fault type. Thus, in permanent fault case, the breaker does not attempt to reclose, which avoids a re-strike of the fault arc and possible damage to the equipment, while in the temporary fault case, the breaker is switched back to normal operating status in steps, to enable a smooth dc voltage restoration. It has been shown that

the same strategy can also be applied to locate the fault position in permanent fault case.

Modular multilevel converter can block the dc fault current, if sufficient counter-emf is built-up in the fault path by using bipolar SM instead of the conventional half-bridge SM. However, this feature comes with additional costs and on-state losses. Thus, in Section 5 a hybrid-arm MMC with reduced number of bipolar SM has been presented. Observing the converter's fault operational sequence, the minimum number of bipolar SM - assuming the most common type, i.e. full-bridge SM - has been analytically derived: 83 % in the upper arm and 0 % in the lower arm. The proposed converter design has been compared to full-bridge MMC, conventional hybrid-arm MMC with equal number of bipolar and half-bridge SM and half-bridge MMC combined with hybrid dc CB under varying grid conditions. It can be concluded that reducing the number of bipolar submodules in the converter increases the efficiency in normal operation (i.e. 17% lower losses compared to the conventional hybrid arm MMC), while the fault blocking ability under low inductance is preserved with sufficient counter-emf provision and reasonable clearing time of 2.7 ms, which is in between the clearing times achieved with full-bridge MMC (< 0.5 ms) and hybrid dc CB (4 ms), respectively. It has been shown that during the clearing time, the fault current is charging the SM capacitors, which are negatively inserted in the current path in the converter's blocked state. Thus, a significant amount of over-voltage (up to 33% for 100 mH dc side inductance) can appear across the SM capacitors, which depends on the stored energy in the dc and arm inductances as well as on the energy transfer from the ac grid, until the arm currents decay to zero. The over-voltage must be considered in the design of the SM capacitors and semiconductors, even though, assuming conventionally applied operating voltages around $0.45 - 0.55$ p.u. of the nominal voltage, the observed over-voltage is still tolerable.

6.2. Future research

MMC-HVdc systems offer advanced control possibilities in the transmission grid, however, their vulnerability towards dc faults requires a careful protection system design to ensure a stable and reliable grid operation. This thesis has illustrated new strategies and concepts to control and protect MMC-HVdc systems.

The following research topics have been identified for potential future work:

- The proposed primary frequency regulation and inertia emulation strategy exploits the loads' active power to voltage sensitivity. In the future power system scenario, the share of power electronics-based resources will steadily grow. The power-electronics devices are usually controlled to not react on the imposed voltage variation (constant power behavior), which limits the load controllability by grid voltage control. Thus, it

must be comprehensively studied, if such a constant-power-based grid is a realistic scenario and to which extent it is feasible to provide the targeted services with the HVdc system. Additionally, it should be carefully assessed, which voltage constraints are set worldwide and how the controlled voltage variation during the frequency support might affect the customers.

- The load control has been proposed in this thesis for frequency support purposes as alternative energy source to energy storage systems and wind farm power curtailment, which can be alternatively used for the provision of the frequency support, especially for virtual inertia emulation. In the future, it must be carefully evaluated, which might be the optimal combination of the different sources and how they can be made available by the HVdc system with limited effect on the grid. As possible extension, also the HVdc dynamic capacity should be studied, which could make available either higher reactive or active power during the contingency. The preferred solution has to be assessed technically and economically taking into account also the remuneration of the grid services offered by the HVdc.

- The parameter variation analysis to evaluate dc circuit breaker designs has been only derived for few selected cases with focus on the dc current limiting inductance. Future research should exploit the full potential of the analytical approach, which includes the reduction of the set of differential equations to a suitable order and provide analytical expressions for each parameter's influence. A sensitivity evaluation of these parameters could guide engineers in the future design of dc circuit breakers.

- The analytical fault current estimation should be extended to all presented fault cases. Particularly, the pole-to-ground faults are of interest, in which the grounding configuration can be included as additional parameter in the problem's set of differential equations.

- The presented adaption of the hybrid-arm MMC increases the on-state converter efficiency, however, shows relatively weak fault blocking performance in combination with large dc side inductances and is not applicable, when full selectivity is required in the system's protection. As a possible extension of the presented work, the application of the proposed converter in combination with a low-scale dc circuit breaker should be evaluated. And it should be analyzed, if the total number of power electronic switches installed in the circuit (MMC + dc CB) can be reduced, while providing a partially selective protection approach.

- One key requirement on HVdc systems is a small outage time after fault and that they regain the grid support functionalities as soon as possible in order to minimally influence the ac grid. Thus, the proposed converter's post-fault control has to be investigated, which should include the reactive power provision to the ac grid during

the fault stage (STATCOM mode) and smooth dc voltage and power ramp-up after the fault is cleared.

References

[1] European Network of Transmission System Operators for Electricity, "Hvdc links in system operations," techreport, Dec. 2019.

[2] A. Nishioka, F. Alvarez, and T. Omori, "Global rise of hvdc and its background," Hitachi ABB HVDC Technologies, Ltd., Tech. Rep., 2020.

[3] GE Grid Solutions, "High voltage direct current systems," Tech. Rep., 2018.

[4] D. Van Hertem, O. Gomis-Bellmunt, and J. Liang, *HVDC Grids for Offshore and Supergrid of the Future*, T. Samad, Ed. Hoboken, NJ: John Wiley and Sons, 2016.

[5] K. Schonleber, A. Oudalov, A. Krontiris, and P. Lundberg, "Opportunities for embedded high-voltage direct current: Evaluating the benefits for the legacy ac grid," *IEEE Power and Energy Magazine*, vol. 18, no. 5, pp. 58–63, 2020.

[6] T. Meridji, F. Ceja-Gomez, J. Restrepo, and R. Azar, "High-voltage dc conversion: Boosting transmission capacity in the grid," *IEEE Power and Energy Magazine*, vol. 17, no. 3, pp. 22–31, 2019.

[7] T. H. Nguyen, K. A. Hosani, M. S. E. Moursi, and F. Blaabjerg, "An overview of modular multilevel converters in hvdc transmission systems with statcom operation during pole-to-pole dc short circuits," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4137–4160, May 2019.

[8] G. Falahi and A. Huang, "Low voltage ride through control of modular multilevel converter based hvdc systems," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 4663–4668.

[9] S. Chaudhary, R. Teodorescu, D. Rizadis, and L. Mathe, "Low voltage fault ride through control in mmc-hvdc," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, 2017, pp. 750–755.

[10] M. A. Elizondo, R. Fan, H. Kirkham *et al.*, "Interarea oscillation damping control using high-voltage dc transmission: A survey," *IEEE Transactions on Power Systems*, vol. 33, no. 6, pp. 6915–6923, 2018.

[11] A. Rodriguez-Cabero, J. Roldan-Perez, M. Prodanovic, J. A. Suul, and S. D'Arco, "Coupling of ac grids via vsc-hvdc interconnections for oscillation damping based on differential and common power control," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6548–6558, 2020.

[12] L. Harnefors, N. Johansson, L. Zhang, and B. Berggren, "Interarea oscillation damping using active-power modulation of multiterminal hvdc transmissions," *IEEE Transactions on Power Systems*, vol. 29, no. 5, pp. 2529–2538, 2014.

[13] S. Akkari, J. Dai, M. Petit, and X. Guillaud, "Interaction between the voltage-droop and the frequency-droop control for multi-terminal hvdc systems," *IET Generation, Transmission Distribution*, vol. 10, no. 6, pp. 1345–1352, 2016.

[14] T. M. Haileselassie and K. Uhlen, "Primary frequency control of remote grids connected by multi-terminal hvdc," in *IEEE PES General Meeting*, July 2010, pp. 1–6.

[15] N. R. Chaudhuri, R. Majumder, and B. Chaudhuri, "System frequency support through multi-terminal dc (mtdc) grids," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 347–356, Feb 2013.

[16] J. Zhu, C. D. Booth, G. P. Adam, A. J. Roscoe, and C. G. Bright, "Inertia emulation control strategy for vsc-hvdc transmission systems," *IEEE Transactions on Power Systems*, vol. 28, no. 2, pp. 1277–1287, May 2013.

[17] A. Clerici, S. Negri, and E. Tironi, "Inertia emulation in multiterminal hvdc networks," in *2019 IEEE PES Innovative Smart Grid Technologies Europe (ISGT-Europe)*, 2019, pp. 1–5.

[18] E. Rakhshani and P. Rodriguez, "Inertia emulation in ac/dc interconnected power systems using derivative technique considering frequency measurement effects," *IEEE Transactions on Power Systems*, vol. 32, no. 5, pp. 3338–3351, 2017.

[19] A. Ulbig, T. S. Borsche, and G. Andersson, "Impact of low rotational inertia on power system stability and operation," *IFAC Proceedings Volumes*, vol. 47, no. 3, pp. 7290 – 7297, 2014, 19th IFAC World Congress.

[20] Ying Jiang-Hafner, H. Duchen, M. Karlsson, L. Ronstrom, and B. Abrahamsson, "Hvdc with voltage source converters - a powerful standby black start facility," in *2008 IEEE/PES Transmission and Distribution Conference and Exposition*, 2008, pp. 1–9.

[21] H. Becker, A. Naranovich, T. Hennig *et al.*, "System restoration using vsc-hvdc connected offshore wind power plant as black-start unit," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1–P.8.

[22] CIGRE JWG C4/B4/C1.604, "Influence of embedded hvdc transmission on system security and ac network performance," *CIGRE Technical Brochure 536*, Apr. 2013.

[23] D. Chakravorty, B. Chaudhuri, and S. Y. R. Hui, "Estimation of aggregate reserve with point-of-load voltage control," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 4649–4658, Sep. 2018.

[24] Y. Wan, M. A. A. Murad, M. Liu, and F. Milano, "Voltage frequency control using svc devices coupled with voltage dependent loads," *IEEE Transactions on Power Systems*, vol. 34, no. 2, pp. 1589–1597, March 2019.

[25] A. Moeini and I. Kamwa, "Analytical concepts for reactive power based primary frequency control in power systems," *IEEE Transactions on Power Systems*, vol. 31, no. 6, pp. 4217–4230, Nov 2016.

[26] G. De Carne, G. Buticchi, M. Liserre, and C. Vournas, "Real-time primary frequency regulation using load power control by smart transformers," *IEEE Transactions on Smart Grid*, pp. 1–1, 2018.

[27] ENTSO-E, "Network code on operation security," February 2013.

[28] VDE, "Vde-ar-n 4131 technical requirements for grid connection of high voltage direct current systems and direct current-connected power park modules (tar hvdc)," Mar. 2019, german Language Version.

[29] S. G. Vennelaganti and N. R. Chaudhuri, "Selective power routing in mtdc grids for inertial and primary frequency support," *IEEE Transactions on Power Systems*, vol. 33, no. 6, pp. 7020–7030, Nov 2018.

[30] W. Wang, Y. Li, Y. Cao, U. Haeger, and C. Rehtanz, "Adaptive droop control of vscmtdc system for frequency support and power sharing," *IEEE Transactions on Power Systems*, vol. 33, no. 2, pp. 1264–1274, March 2018.

[31] N. A. Belda, C. A. Plet, and R. P. P. Smeets, "Analysis of faults in multiterminal hvdc grid for definition of test requirements of hvdc circuit breakers," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 403–411, Feb 2018.

[32] CIGRE WG B4/B5-59, "Protection and local control of dc grids," *CIGRE Technical Brochure 739*, Aug. 2018.

[33] K. Tahata, S. E. Oukaili, K. Kamei *et al.*, "Hvdc circuit breakers for hvdc grid applications," in *11th IET International Conference on AC and DC Power Transmission*, 2015, pp. 1–9.

[34] M. Abedrabbo, W. Leterme, and D. Van Hertem, "Systematic approach to hvdc circuit breaker sizing," *IEEE Transactions on Power Delivery*, vol. 35, no. 1, pp. 288–300, 2020.

[35] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid hvdc breaker an innovation breakthrough enabling reliable hvdc grids," 2012.

[36] J. Hafner and B. Jacobsen, "Proactive hybrid hvdc breakers - a key innovation for reliable hvdc grids," in *CIGRE Symposium Bologna*, 2011.

[37] W. Grieshaber, J.-P-Dupraz, D.-L-Penache, and L. Violleau, "Development and test of a 120 kv direct current circuit breaker," in *CIGRE Session B4-301*, 2014.

[38] W. Zhou, X. Wei, S. Zhang *et al.*, "Development and test of a 200kv full-bridge based hybrid hvdc breaker," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sept 2015, pp. 1–7.

[39] O. Cwikowski, B. Chang, M. Barnes, R. Shuttleworth, and A. Beddard, "Fault current testing envelopes for vsc hvdc circuit breakers," *IET Generation, Transmission & Distribution*, vol. 10, no. 6, pp. 1393–1400, 2016.

[40] D. Doering, D. Ergin, K. Würflinger *et al.*, "System integration aspects of dc circuit breakers," *IET Power Electronics*, vol. 9, 02 2016.

[41] M. K. Bucher and C. M. Franck, "Contribution of fault current sources in multiterminal hvdc cable networks," *IEEE Transactions on Power Delivery*, vol. 28, no. 3, pp. 1796–1803, 2013.

[42] ——, "Analytic approximation of fault current contributions from capacitive components in hvdc cable networks," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 74–81, 2015.

[43] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-circuit and ground fault analyses and location in vsc-based dc network cables," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3827–3837, 2012.

[44] C. Li, C. Zhao, J. Xu *et al.*, "A pole-to-pole short-circuit fault current calculation method for dc grids," *IEEE Transactions on Power Systems*, vol. 32, no. 6, pp. 4943–4953, 2017.

[45] M. Stumpe, P. Ruffing, P. Wagner, and A. Schnettler, "Adaptive single-pole autoreclosing concept with advanced dc fault current control for full-bridge mmc vsc systems," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 321–329, 2018.

[46] T. Wang, G. Song, and K. S. T. Hussain, "Adaptive single-pole auto-reclosing scheme for hybrid mmc-hvdc systems," *IEEE Transactions on Power Delivery*, vol. 34, no. 6, pp. 2194–2203, 2019.

[47] G. Song, T. Wang, and K. S. T. Hussain, "Dc line fault identification based on pulse injection from hybrid hvdc breaker," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 271–280, 2019.

[48] S. Ali, Z. Ling, K. Tian, and Z. Huang, "Recent advancements in submodule topologies and applications of mmc," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2020.

[49] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for hvdc systems based on various submodule circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385–394, 2015.

[50] R. Marquardt, "Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications," in *The 2010 International Power Electronics Conference - ECCE ASIA* -, 2010, pp. 502–507.

[51] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1137–1146, 2015.

[52] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2015.

[53] X. Yu, Y. Wei, Q. Jiang *et al.*, "A novel hybrid-arm bipolar mmc topology with dc fault ride-through capability," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1404–1413, 2017.

[54] T. Keim and A. Bindra, "Recent advances in hvdc and uhvdc transmission [happenings]," *IEEE Power Electronics Magazine*, vol. 4, no. 4, pp. 12–18, 2017.

[55] A. Moglestue et al. (ABB Technology Ltd.), "Abb review, special report 60 years of hvdc," July 2014.

[56] R. Teixeira Pinto, "Multi-terminal dc networks: System integration, dynamics and control," Ph.D. dissertation, TU Delft, 2014.

[57] D. Jovcic and K. Ahmad, *High Voltage Direct Current Transmission: Converters, Systems and DC Grids*. Hoboken, NJ: John Wiley and Sons, 2015.

[58] ENTSO-E, "Tyndp 2016 scenario development report," Tech. Rep., 2015.

[59] S. K. Chaudhary, R. Teodorescu, and P. Rodriguez, "Wind farm grid integration using vsc based hvdc transmission - an overview," in *2008 IEEE Energy 2030 Conference*, 2008, pp. 1–7.

[60] P. Bresesti, W. L. Kling, R. L. Hendriks, and R. Vailati, "Hvdc connection of offshore wind farms to the transmission system," *IEEE Transactions on Energy Conversion*, vol. 22, no. 1, pp. 37–43, 2007.

[61] P. RODRIGUEZ and K. ROUZBEHI, "Multi-terminal dc grids: challenges and prospects," *Journal of Modern Power Systems and Clean Energy*, vol. 5, no. 4, pp. 515–523, 2017.

[62] D. Van Hertem, M. Ghandari, and M. Delimar, "Technical limitations towards a supergrid - a european prospective," in *2010 IEEE International Energy Conference*, 2010, pp. 302–309.

[63] "North sea wind power hub," accessed 20.04.2021. [Online]. Available: https://northseawindpowerhub.eu/project/

[64] X. Han, W. Sima, M. Yang *et al.*, "Transient characteristics under ground and short-circuit faults in a ±500kv mmc-based hvdc system with hybrid dc circuit breakers," *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1378–1387, 2018.

[65] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. John Wiley & Sons, 2016.

[66] M. M. C. Merlin, T. C. Green, P. D. Mitcheson *et al.*, "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, 2014.

[67] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (mmcc)," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3119–3130, 2011.

[68] D. Schröder, *Elektrische Antriebe - Regelung von Antriebssystemen*. Heidelberg, Berlin: Springer-Verlag, 2009.

[69] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 358–371, 2015.

[70] F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, "Thermal analysis and balancing for modular multilevel converters in hvdc applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1985–1996, 2018.

[71] CIGRE WG B4-58, "Control methodologies for direct voltage and power flow in a meshed hvdc grid," *CIGRE Technical Brochure 699*, Sep. 2017.

[72] W. Wang and M. Barnes, "Power flow algorithms for multi-terminal vsc-hvdc with droop control," *IEEE Transactions on Power Systems*, vol. 29, no. 4, pp. 1721–1730, 2014.

[73] R. Li, L. Xu, D. Holliday *et al.*, "Continuous operation of radial multiterminal hvdc systems under dc fault," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 351–361, 2016.

[74] G. De Carne *et al.*, "Which deepness class is suited for modeling power electronics?: A guide for choosing the right model for grid-integration studies," *IEEE Industrial Electronics Magazine*, vol. 13, no. 2, pp. 41–55, June 2019.

[75] S. Brüske, G. De Carne, and M. Liserre, "Multi-frequency power transfer in a smart transformer based distribution grid," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 4325–4331.

[76] X. Wang, F. Blaabjerg, and W. Wu, "Modeling and analysis of harmonic stability in an ac power-electronics-based power system," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6421–6432, 2014.

[77] Y. Wang, X. Wang, F. Blaabjerg, and Z. Chen, "Harmonic instability assessment using state-space modeling and participation analysis in inverter-fed power systems," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 806–816, 2017.

[78] M. Bahrman, E. V. Larsen, R. J. Piwko, and H. S. Patel, "Experience with hvdc - turbine-generator torsional interaction at square butte," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-99, no. 3, pp. 966–975, 1980.

[79] N. Prabhu and K. R. Padiyar, "Investigation of subsynchronous resonance with vsc-based hvdc transmission systems," *IEEE Transactions on Power Delivery*, vol. 24, no. 1, pp. 433–440, 2009.

[80] X. Wang, L. Harnefors, and F. Blaabjerg, "Unified impedance model of grid-connected voltage-source converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1775–1787, 2018.

[81] C. Buchhagen, C. Rauscher, A. Menze, and J. Jung, "Borwin1 - first experiences with harmonic interactions in converter dominated grids," in *International ETG Congress 2015; Die Energiewende - Blueprints for the new energy age*, 2015, pp. 1–7.

[82] A. Jamshidifar and D. Jovcic, "Small-signal dynamic dq model of modular multilevel converter for system studies," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 191–199, 2016.

[83] W. Xiang, W. Lin, L. Xu, and J. Wen, "Enhanced independent pole control of hybrid mmc-hvdc system," *IEEE Transactions on Power Delivery*, vol. 33, no. 2, pp. 861–872, 2018.

[84] D. Sun, X. Xie, Y. Liu, K. Wang, and M. Ye, "Investigation of ssti between practical mmc-based vsc-hvdc and adjacent turbogenerators through modal signal injection test," *IEEE Transactions on Power Delivery*, vol. 32, no. 6, pp. 2432–2441, 2017.

[85] G. Pinares and M. Bongiorno, "Modeling and analysis of vsc-based hvdc systems for dc network stability studies," *IEEE Transactions on Power Delivery*, vol. 31, no. 2, pp. 848–856, 2016.

[86] M. K. Zadeh, M. Amin, J. A. Suul, M. Molinas, and O. B. Fosso, "Small-signal stability study of the cigré dc grid test system with analysis of participation factors and parameter sensitivity of oscillatory modes," in *2014 Power Systems Computation Conference*, 2014, pp. 1–8.

[87] M. Amin, M. Molinas, J. Lyu, and X. Cai, "Impact of power flow direction on the stability of vsc-hvdc seen from the impedance nyquist plot," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 8204–8217, 2017.

[88] G. P. Adam, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Generalized modeling of dc grid for stability studies," in *4th International Conference on Power Engineering, Energy and Electrical Drives*, 2013, pp. 1168–1174.

[89] A. A. van der Meer, M. Ndreko, M. Gibescu, and M. A. M. M. van der Meijden, "The effect of frt behavior of vsc-hvdc-connected offshore wind power plants on ac/dc system dynamics," *IEEE Transactions on Power Delivery*, vol. 31, no. 2, pp. 878–887, 2016.

[90] W. B4.57, "Guide for the development of models for hvdc converters in a hvdc grid," in *CIGRE, WG B4.57*. Paris, France: CIGRE, Dec. 2014.

[91] A. A. van der Meer, M. Gibescu, M. A. M. M. van der Meijden, W. L. Kling, and J. A. Ferreira, "Advanced hybrid transient stability and emt simulation for vsc-hvdc systems," *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1057–1066, 2015.

[92] . Göksu, R. Teodorescu, C. L. Bak, F. Iov, and P. C. Kjaer, "Instability of wind turbine converters during current injection to low voltage grid faults and pll frequency based stability solution," *IEEE Transactions on Power Systems*, vol. 29, no. 4, pp. 1683–1691, 2014.

[93] H. Villegas Pico, J. D. McCalley, A. Angel, R. Leon, and N. J. Castrillon, "Analysis of very low frequency oscillations in hydro-dominant power systems using multi-unit modeling," *IEEE Transactions on Power Systems*, vol. 27, no. 4, pp. 1906–1915, 2012.

[94] G. De Carne, G. Buticchi, Z. Zou, and M. Liserre, "Reverse power flow control in a st-fed distribution grid," *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 3811–3819, 2018.

[95] G. De Carne, G. Buticchi, M. Liserre, and C. Vournas, "Load control using sensitivity identification by means of smart transformer," *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1–1, 2016.

[96] L. Tang and B. Ooi, "Locating and isolating dc faults in multi-terminal dc systems," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1877–1884, 2007.

[97] D. Van Hertem, M. Ghandhari, J. B. Curis, O. Despouys, and M. Andree, "Protection requirements for a multi-terminal meshed dc grid." Cigre, 2011.

[98] M. Langwasser, G. De Carne, M. Liserre, and M. Biskoping, "Primary frequency regulation using hvdc terminals controlling voltage dependent loads," *IEEE Transactions on Power Delivery*, vol. 36, no. 2, pp. 710–720, 2021.

[99] M. Langwasser, G. De Carne, M. Liserre, and M. Biskoping, "Enhanced grid frequency support by means of hvdc-based load control," *Electric Power Systems Research*, vol. 189, p. 106552, 2020. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378779620303564

[100] M. Langwasser, K. Schoenleber, A. Wasserrab, M. Thiele, and M. Liserre, "Online estimation of dynamic capacity of vsc-hvdc systems: Power system use cases," in *Internationaler ETG-Kongress 2021*, 2021.

[101] Xiao-Ping Zhang and Liangzhong Yao, "A vision of electricity network congestion management with facts and hvdc," in *2008 Third International Conference on Electric Utility Deregulation and Restructuring and Power Technologies*, 2008, pp. 116–121.

[102] S. Corsi and C. Sabelli, "General blackout in italy sunday september 28, 2003, h. 03:28:00," in *IEEE Power Engineering Society General Meeting, 2004.*, 2004, pp. 1691–1702.

[103] Y. Liu, X. Zhou, Y. Wu *et al.*, "A study on vsc- hvdc based black start method," in *2019 4th IEEE Workshop on the Electronic Grid (eGRID)*, 2019, pp. 1–6.

[104] P. Kundur, *Power System Stability and Control*. Electric Power Research Institute, 1994.

[105] A. Johnson. Grid code frequency response working group - system inertia. [Online]. National Grid. [Accessed 10.04.2021]. [Online]. Available: https://www.nationalgrid.com/sites/default/files/documents/16890-Meeting%208%20-%20Inertia%20presentation.pdf

[106] ENTSO-E, "Continental europe significant frequency deviations january 2019," January 2019.

[107] National Grid ESO, "Interim report into the low frequency demand disconnection (lfdd) following generator trips and frequency excursion on 9 aug 2019," August 2019.

[108] Y. Jiang-Haefner and P. Lundberg, "Vsc hvdc transmission support variable electricity generation," in *2016 CIGRE SESSION*, 2016.

[109] F. Thams, J. A. Suul, S. D'Arco, M. Molinas, and F. W. Fuchs, "Stability of dc voltage droop controllers in vsc hvdc systems," in *2015 IEEE Eindhoven PowerTech*, 2015, pp. 1–7.

[110] L. Papangelis, M. Debry, T. V. Cutsem, and P. Panciatici, "Local control of ac/dc converters for frequency support between asynchronous ac areas," in *2017 IEEE Manchester PowerTech*, June 2017, pp. 1–6.

[111] O. D. Adeuyi, M. Cheah-Mane, J. Liang, and N. Jenkins, "Fast frequency response from offshore multiterminal vsc hvdc schemes," *IEEE Transactions on Power Delivery*, vol. 32, no. 6, pp. 2442–2452, Dec 2017.

[112] B. Silva, C. L. Moreira, L. Seca, Y. Phulpin, and J. A. P. Lopes, "Provision of inertial and primary frequency control services using offshore multiterminal hvdc networks," *IEEE Transactions on Sustainable Energy*, vol. 3, no. 4, pp. 800–808, Oct 2012.

[113] M. Guan, J. Cheng, C. Wang *et al.*, "The frequency regulation scheme of interconnected grids with vsc-hvdc links," *IEEE Transactions on Power Systems*, vol. 32, no. 2, pp. 864–872, March 2017.

[114] A. E. Leon, "Short-term frequency regulation and inertia emulation using an mmc-based mtdc system," *IEEE Transactions on Power Systems*, vol. 33, no. 3, pp. 2854–2863, May 2018.

[115] F. Giacomo Puricelli, S. D'Arco, J. Are Suul, and L. Piegari, "Evaluation of inertia emulation strategies for dc- voltage-controlled and power-controlled converter stations in hvdc interconnections," in *2020 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2020, pp. 832–838.

[116] S. D'Arco, T. T. Nguyen, and J. A. Suul, "Evaluation of virtual inertia control strategies for mmc-based hvdc terminals by p-hil experiments," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 4811–4818.

[117] S. I. Nanou and S. A. Papathanassiou, "Frequency control of island vsc-hvdc links operating in parallel with ac interconnectors and onsite generation," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 447–454, Feb 2018.

[118] 50Hertz Transmission GmbH, Amprion GmbH, TenneT TSO GmbH, TransnetBW GmbH, "Netzentwicklungsplan Strom 2030, Version 2017. Zweiter Entwurf der Uebertragungsnetzbetreiber." 2017.

[119] "Load representation for dynamic performance analysis (of power systems)," *IEEE Transactions on Power Systems*, vol. 8, no. 2, pp. 472–482, May 1993.

[120] Z. Wang and J. Wang, "Review on implementation and assessment of conservation voltage reduction," *IEEE Transactions on Power Systems*, vol. 29, no. 3, pp. 1306–1315, May 2014.

[121] J. V. Milanovic, K. Yamashita, S. Martinez Villanueva, S. Z. Djokic, and L. M. Korunovic, "International industry practice on power system load modeling," *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3038–3046, Aug 2013.

[122] W. Price, K. Wirgau, A. Murdoch *et al.*, "Load modeling for power flow and transient stability computer studies," *IEEE Transactions on Power Systems*, vol. 3, no. 1, pp. 180–187, 1988.

[123] "Standard load models for power flow and dynamic performance simulation," *IEEE Transactions on Power Systems*, vol. 10, no. 3, pp. 1302–1313, 1995.

[124] D. P. Stojanovic, L. M. Korunovic, and J. Milanovic, "Dynamic load modelling based on measurements in medium voltage distribution network," *Electric Power Systems Research*, vol. 78, no. 2, pp. 228 – 238, 2008.

[125] G. Delille, L. Capely, D. Souque, and C. Ferrouillat, "Experimental validation of a novel approach to stabilize power system frequency by taking advantage of load voltage sensitivity," in *2015 IEEE Eindhoven PowerTech*, June 2015, pp. 1–6.

[126] P. Regulski, P. Wall, Z. Rusidovic, and V. Terzija, "Estimation of load model parameters from pmu measurements," in *IEEE PES Innovative Smart Grid Technologies, Europe*, 2014, pp. 1–6.

[127] D. Han, J. Ma, R. He, and Z. Dong, "A real application of measurement-based load modeling in large-scale power grids and its validation," *IEEE Transactions on Power Systems*, vol. 24, no. 4, pp. 1756–1764, 2009.

[128] S. A. Arefifar and W. Xu, "Online tracking of voltage-dependent load parameters using ultc created disturbances," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 130–139, 2013.

[129] A. Ortega and F. Milano, "Estimation of voltage dependent load models through power and frequency measurements," *IEEE Transactions on Power Systems*, vol. 35, no. 4, pp. 3308–3311, 2020.

[130] P. Regulski, D. S. Vilchis-Rodriguez, S. Djurovic, and V. Terzija, "Estimation of composite load model parameters using an improved particle swarm optimization method," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 553–560, 2015.

[131] D. S. Callaway and I. A. Hiskens, "Achieving controllability of electric loads," *Proceedings of the IEEE*, vol. 99, no. 1, pp. 184–199, Jan 2011.

[132] G. De Carne, M. Liserre, and C. Vournas, "On-line load sensitivity identification in lv distribution grids," *IEEE Transactions on Power Systems*, vol. 32, no. 2, pp. 1570–1571, March 2017.

[133] A. Ballanti, L. N. Ochoa, K. Bailey, and S. Cox, "Unlocking new sources of flexibility: Class: The world's largest voltage-led load-management project," *IEEE Power and Energy Magazine*, vol. 15, no. 3, pp. 52–63, May 2017.

[134] D. Van Hertem, W. Leterme, G. Chaffey *et al.*, "Substations for future hvdc grids: Equipment and configurations for connection of hvdc network elements," *IEEE Power and Energy Magazine*, vol. 17, no. 4, pp. 56–66, 2019.

[135] K. Strunz *et al.*, "Benchmark systems for network integration of renewable and distributed energy resources," *WG C6.04, Task Force C6.04.02 Technical Brochure 575*, 2014.

[136] A. B. Jusoh, "The instability effect of constant power loads," in *PECon 2004. Proceedings. National Power and Energy Conference, 2004.*, Nov 2004, pp. 175–179.

[137] M. Cespedes, L. Xing, and J. Sun, "Constant-power load system stabilization by passive damping," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1832–1836, July 2011.

[138] K. R. Padiyar, "Energy function analysis for power system stability," *Electric Machines & Power Systems*, vol. 18, no. 2, pp. 209–210, 1990.

[139] S. Henry, O. Despouys, R. Adapa *et al.*, "Influence of embedded hvdc transmission on system security and ac network performance," *CIGRE*, vol. JWG C4/B4/C1, no. 536, April 2013.

[140] "Ensure," accessed 24.04.2021. [Online]. Available: https://www.kopernikus-projekte.de/projekte/ensure

[141] M. Langwasser, G. D. Carne, M. Liserre, and M. Biskoping, "Requirement analysis of hybrid direct current breaker in multi-terminal high-voltage direct current grids," *Journal of Engineering*, vol. 2018, no. 15, pp. 1066–1071, 10 2018.

[142] M. Langwasser, G. De Carne, M. Liserre, and M. Biskoping, "Fault current estimation in multi-terminal hvdc grids considering mmc control," *IEEE Transactions on Power Systems*, vol. 34, no. 3, pp. 2179–2189, 2019.

[143] H. Iman-Eini, M. Langwasser, L. Camurca, and M. Liserre, "Modular hybrid dc breaker-based adaptive auto-reclosing method for mmc-hvdc systems," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1–P.9.

[144] J. He, B. Li, and Y. Li, "Analysis of the fault current limiting requirement and design of the bridge-type fcl in the multi-terminal dc grid," *IET Power Electronics*, vol. 11, 11 2017.

[145] B. Geebelen, W. Leterme, and D. V. Hertem, "Analysis of dc breaker requirements for different hvdc grid protection schemes," in *11th IET International Conference on AC and DC Power Transmission*, 2015, pp. 1–7.

[146] R. Li, Z. X. Wang, D. Holliday, L. Z. Yao, and B. W. Williams, "Dc circuit breaker requirements in multi-terminal hvdc systems," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, 2016, pp. 1–6.

[147] C. M. Franck, "Hvdc circuit breakers: A review identifying future research needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, 2011.

[148] E. Kontos, R. T. Pinto, S. Rodrigues, and P. Bauer, "Impact of hvdc transmission system topology on multiterminal dc network faults," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 844–852, 2015.

[149] "Pscad," accessed 15.04.2021. [Online]. Available: https://www.pscad.com/webhelp/ol-help.htm#EMTDC/Transmission_Lines/Overview.htm:

[150] A. Morched, B. Gustavsen, and M. Tartibi, "A universal model for accurate calculation of electromagnetic transients on overhead lines and underground cables," *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp. 1032–1038, 1999.

[151] H. W. Dommel, "Digital computer solution of electromagnetic transients in single- and multiphase networks," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-88, no. 4, pp. 388–399, 1969.

[152] J. Grainger and W. Stevenson, *Power System Analysis*. McGraw Hill Inc., 1994.

[153] H. Saad, J. Peralta, S. Dennetière *et al.*, "Dynamic averaged and simplified models for mmc-based hvdc transmission systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 3, pp. 1723–1730, 2013.

[154] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level mmc-hvdc system," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1501–1508, 2012.

[155] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel hvdc converters (mmc) on electromagnetic transient simulation programs," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 316–324, 2011.

[156] N. Ahmed, L. Ängquist, S. Norrga, and H. Nee, "Validation of the continuous model of the modular multilevel converter with blocking/deblocking capability," in *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, 2012, pp. 1–6.

[157] H. Saad, S. Dennetière, J. Mahseredjian *et al.*, "Modular multilevel converter models for electromagnetic transients," *IEEE Transactions on Power Delivery*, vol. 29, no. 3, pp. 1481–1489, 2014.

[158] A. Beddard, C. E. Sheridan, M. Barnes, and T. C. Green, "Improved accuracy average value models of modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2260–2269, 2016.

[159] A. Wasserrab, B. Just, and G. Balzer, "Contribution of hvdc converters to the dc short circuit current," in *2013 48th International Universities' Power Engineering Conference (UPEC)*, 2013, pp. 1–6.

[160] D. Tzelepis, S. Ademi, D. Vozikis *et al.*, "Impact of vsc converter topology on fault characteristics in hvdc transmission systems," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, 2016, pp. 1–6.

[161] V. A. Lacerda, D. V. Coury, N. Y. Suzuki, and R. M. Monaro, "The impact of modular multilevel converter control on dc short-circuit currents of hvdc systems," in *2018 Power Systems Computation Conference (PSCC)*, 2018, pp. 1–7.

[162] T. K. Vrana, S. Dennetiere, Y. Yang *et al.*, "The cigre b4 dc grid test system," *Electra*, no. 270, pp. 10–19, 2013.

[163] Z. Liu, S. S. Mirhosseini, M. Popov *et al.*, "Protection testing for multiterminal high-voltage dc grid: Procedures and procedures and assessment," *IEEE Industrial Electronics Magazine*, vol. 14, no. 3, pp. 46–64, 2020.

[164] M. K. Bucher and C. M. Franck, "Comparison of fault currents in multiterminal hvdc grids with different grounding schemes," in *2014 IEEE PES General Meeting | Conference Exposition*, 2014, pp. 1–5.

[165] ——, "Analytic approximation of fault current contribution from ac networks to mtdc networks during pole-to-ground faults," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 20–27, 2016.

[166] M. J. Pérez Molina, D. M. Larruskain, P. Eguía López, and A. Etxegarai, "Analysis of local measurement-based algorithms for fault detection in a multi-terminal hvdc grid," *Energies*, vol. 12, no. 24, 2019. [Online]. Available: https://www.mdpi.com/1996-1073/12/24/4808

[167] K. Vinothkumar, I. Segerqvist, N. Johannesson, and A. Hassanpoor, "Sequential auto-reclosing method for hybrid hvdc breaker in vsc hvdc links," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, 2016, pp. 1–6.

[168] S. Yang, W. Xiang, X. Lu, W. Zuo, and J. Wen, "An adaptive reclosing strategy for mmc-hvdc systems with hybrid dc circuit breakers," *IEEE Transactions on Power Delivery*, vol. 35, no. 3, pp. 1111–1123, 2020.

[169] J. Woodworth. (2011) Arrester reference voltage. ArresterFacts-027. [Online]. Available: http://www.arresterworks.com.

[170] E. Solas, G. Abad, J. A. Barrena *et al.*, "Modular multilevel converter with different submodule concepts - part i: Capacitor voltage balancing method," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4525–4535, 2013.

[171] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Full-bridge mmc converter optimal design to hvdc operational requirements," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1342–1350, 2016.

[172] L. Hou, S. Zhang, Y. Wei, X. Li, and Q. Jiang, "A hybrid-arm modular multilevel converters topology with dc low voltage operation and fault ride-through capability for unidirectional hvdc bulk power transmission," *IEEE Transactions on Power Delivery*, vol. 35, no. 6, pp. 2812–2820, 2020.

[173] J. Xu, P. Zhao, and C. Zhao, "Reliability analysis and redundancy configuration of mmc with hybrid submodule topologies," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2720–2729, 2016.

[174] F. Deng, Y. Lü, C. Liu *et al.*, "Overview on submodule topologies, modeling, modulation, control schemes, fault diagnosis, and tolerant control strategies of modular multilevel converters," *Chinese Journal of Electrical Engineering*, vol. 6, no. 1, pp. 1–21, 2020.

[175] K. Ilves, L. Bessegato, L. Harnefors, S. Norrga, and H. . Nee, "Semi-full-bridge submodule for modular multilevel converters," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 1067–1074.

[176] S. Cui and S. Sul, "A comprehensive dc short-circuit fault ride through strategy of hybrid modular multilevel converters (mmcs) for overhead line transmission," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7780–7796, 2016.

[177] R. Li, L. Xu, L. Yu, and L. Yao, "A hybrid modular multilevel converter with reduced full-bridge submodules," *IEEE Transactions on Power Delivery*, vol. 35, no. 4, pp. 1876–1885, 2020.

[178] H. R. Wickramasinghe, G. Konstantinou, S. Ceballos, and J. Pou, "Alternate arm converter energy balancing under parameter variation," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 2996–3000, 2019.

[179] M. M. C. Merlin, D. Soto-Sanchez, P. D. Judge *et al.*, "The extended overlap alternate arm converter: A voltage-source converter with dc fault ride-through capability and a compact design," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3898–3910, 2018.

[180] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New breed of network fault-tolerant voltage-source-converter hvdc transmission system," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 335–346, 2013.

[181] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher, and B. W. Williams, "Hybrid cascaded modular multilevel converter with dc fault ride-through capability for the hvdc transmission system," *IEEE Transactions on Power Delivery*, vol. 30, no. 4, pp. 1853–1862, 2015.

[182] H. Iman-Eini and M. Liserre, "Analysis of the hybrid arm modular multilevel converter in dc-fault blocking state and post-fault condition," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018, pp. P.1–P.10.

[183] A. Nami, A. Hassanpoor, and Y.-j. Häfner, "Theory to practical implementation of full-bridge modular multilevel converter for hvdc applications," in *2016 IEEE International Conference on Industrial Technology (ICIT)*, 2016, pp. 378–383.

[184] H. Iman-Eini, M. Langwasser, L. Camurca, G. De Carne, and M. Liserre, "Hybrid arm mmc with reduced number of bipolar submodules and dc-current blocking capability," 2021, under review in Transactions on Power Electronics (2021).

[185] X. Yu, Y. Wei, Q. Jiang *et al.*, "A novel hybrid-arm bipolar mmc topology with dc fault ride-through capability," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1404–1413, 2017.

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Appendix A.

Journal publications

J1 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Primary Frequency Regulation Using HVDC Terminals Controlling Voltage Dependent Loads," in *IEEE Transactions on Power Delivery*, vol. 36, no. 2, pp. 710-720, April 2021, doi: 10.1109/TPWRD.2020.2990565.

J2 **M. Langwasser**, G. De Carne, M. Liserre, and M. Biskoping, "Enhanced grid frequency support by means of hvdc-based load control," in *Electric Power Systems Research*, vol. 189, p. 106552, December 2020, doi: 10.1016/j.epsr.2020.106552.

J3 G. De Carne, **M. Langwasser**, M. Ndreko, R. Bachmann, R.W. De Doncker, R. Dimitrovski, B.J. Mortimer, A. Neufeld, F. Rojas and M. Liserre, "Which Deepness Class Is Suited for Modeling Power Electronics?: A Guide for Choosing the Right Model for Grid-Integration Studies," in *IEEE Industrial Electronics Magazine*, vol. 13, no. 2, pp. 41-55, June 2019, doi: 10.1109/MIE.2019.2909799.

J4 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Fault Current Estimation in Multi-Terminal HVdc Grids Considering MMC Control," in *IEEE Transactions on Power Systems*, vol. 34, no. 3, pp. 2179-2189, May 2019, doi: 10.1109/TPWRS.2018.2887166.

J5 **M. Langwasser**, G. D. Carne, M. Liserre, and M. Biskoping, "Requirement analysis of hybrid direct current breaker in multi-terminal high-voltage direct current grids," *Journal of Engineering*, vol. 2018, no. 15, pp. 1066-1071, October 2018, 10.1049/-joe.2018.0267.

J6 R. Zhu, M. Liserre, **M. Langwasser** and C. Kumar, "Operation and Control of the Smart Transformer in Meshed and Hybrid Grids: Choosing the Appropriate Smart Transformer Control and Operation Scheme," in IEEE Industrial Electronics Magazine, vol. 15, no. 1, pp. 43-57, March 2021, doi: 10.1109/MIE.2020.3005357

J7 R. Zhu, M. Andresen, **M. Langwasser**, M. Liserre, J.P. Lopes, C. Moreira, J. Rodrigues, M. Couto, "Smart transformer/large flexible transformer," in CES Transactions on Electrical Machines and Systems, vol. 4, no. 4, pp. 264-274, Dec. 2020, doi: 10.30941/CESTEMS.2020.00033

J8 S. Giacomuzzi, **M. Langwasser**, G. De Carne, G. Buja and M. Liserre, "Smart transformer-based medium voltage grid support by means of active power control," in CES Transactions on Electrical Machines and Systems, vol. 4, no. 4, pp. 285-294, Dec. 2020, doi: 10.30941/CESTEMS.2020.00035

J9 G. De Carne, **M. Langwasser**, R. Zhu and M. Liserre, "Smart Transformer-Based Single Phase-To-Neutral Fault Management," in IEEE Transactions on Power Delivery, vol. 34, no. 3, pp. 1049-1059, June 2019, doi: 10.1109/TPWRD.2019.2899518

Conference publications

C1 **M. Langwasser**, K. Schoenleber, A. Wasserrab, M. Thiele, and M. Liserre, "Online estimation of dynamic capacity of vsc-hvdc systems: Power system use cases," *Internationaler ETG-Kongress 2021*, 2021.

C2 H. Iman-Eini, **M. Langwasser**, L. Camurca and M. Liserre, "Modular Hybrid DC Breaker-based Adaptive Auto-Reclosing Method for MMC-HVDC Systems," *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1-P.9, doi: 10.23919/EPE20ECCEEurope43536.2020.9215743.

C3 **M. Langwasser**, H. Imaneini, G. De Carne and M. Liserre, "Estimation and Interruption of Short Circuit Currents in HVDC Systems," *2019 IEEE Power & Energy Society General Meeting (PESGM)*, 2019, pp. 1-5, doi: 10.1109/PESGM40551.2019.8973517.

C4 **M. Langwasser**, M. Biskoping, G. D. Carne and M. Liserre, "Frequency support provision by parallel, hybrid HVDC-HVAC system with Voltage-based Load Control," *2019 IEEE Milan PowerTech*, 2019, pp. 1-6, doi: 10.1109/PTC.2019.8810519.

C5 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Voltage-Based Load Control for Frequency Support Provision by HVDC Systems," *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 311-316, doi: 10.1109/IECON.2018.8592709.

C6 **M. Langwasser**, G. De Carne, M. Liserre and M. Biskoping, "Improved Fault Current Calculation Method for Pole-to-Pole Faults in MMC Multi-Terminal HVDC Grids Considering Control Dynamics," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 5529-5535, doi: 10.1109/ECCE.2018.8557979.

C7 L. Camurca, **M. Langwasser** and M. Liserre, "Design Approach of Inductive Components in Medium Voltage Modular Multilevel Converter Considering DC Side Fault Protection Conditions," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 2617-2624, doi: 10.1109/APEC39645.2020.9124349

C8 L. Camurca, **M. Langwasser**, R. Zhu and M. Liserre, "Future MVDC Applications Using Modular Multilevel Converter," 2020 6th IEEE International Energy Conference (ENERGYCon), 2020, pp. 1024-1029, doi: 10.1109/ENERGYCon48941.2020.9236465

C9 S. Brueske, **M. Langwasser**, J. Goetze, X. Gao and M. Liserre, "Potential of EV Charging Stations for MV Grid Voltage Support," NEIS 2020; Conference on Sustainable Energy Supply and Energy Storage Systems, 2020, pp. 1-6.

C10 F. Cecati, R. Zhu, **M. Langwasser**, M. Liserre and X. Wang, "Scalable State-Space Model of Voltage Source Converter for Low-Frequency Stability Analysis," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 6144-6149, doi: 10.1109/ECCE44975.2020.9236020

C11 **M. Langwasser**, G. De Carne and M. Liserre, "Smart Transformer-based Frequency Support in Variable Inertia Conditions," 2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), 2019, pp. 1-6, doi: 10.1109/CPE.2019.8862365

C12 X. Gao, G. De Carne, **M. Langwasser** and M. Liserre, "Online Load Control in Medium Voltage Grid by Means of Reactive Power Modification of Fast Charging Station," 2019 IEEE Milan PowerTech, 2019, pp. 1-6, doi: 10.1109/PTC.2019.8810407

C13 A. Kazerooni, G. De Carne, M. Eves, J. Yu and **M. Langwasser**, "Technical requirements and challenges for grid applications of Smart Transformers," PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2019, pp. 1-5.

C14 **M. Langwasser** et al., "Requirement Analysis of Circuit Breakers in Future Hybrid AC/DC Grids," PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2019, pp. 1-6.

C15 **M. Langwasser**, G. De Carne, M. Fischer, M. Liserre and M. Biskoping, "Multi-terminal DC Fault Current Estimation Including the Influence of Superconducting Fault Current Limiters," PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2019, pp. 1-6.

C16 G. De Carne, **M. Langwasser**, X. Gao, G. Buticchi and M. Liserre, "Power-Hardware-In-Loop Setup for Power Electronics Tests," PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2017, pp. 1-7.

C17 H. Jedtberg, **M. Langwasser**, R. Zhu, G. Buticchi and M. Liserre, "Impacts of rotor current control targets on DC-link capacitor lifetime in DFIG-based wind turbine during grid voltage unbalance," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), 2017, pp. 3489-3495, doi: 10.1109/ECCE.2017.8096623

C18 H. Jedtberg, **M. Langwasser**, R. Zhu, G. Buticchi, T. Ebel and M. Liserre, "Impacts of unbalanced grid voltages on lifetime of DC-link capacitors of back-to-back converters in wind turbines with doubly-fed induction generators," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), 2017, pp. 816-823, doi: 10.1109/-APEC.2017.7930790