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Analysis of Overmodulation in Power Synchronization-based Voltage Source Converters

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***Abstract*—Low power system inertia in power electronics-dominated grids is a widely discussed problem. Power synchronization allows to emulate inertia by means of the active power low-pass filter, slowing down the grid frequency excursions. Nevertheless, inertia emulation during grid disturbances results in high energy exchange with the dc-link, which brings large dc voltage excursions. When the dc voltage dips below the ac line voltage peak, the modulation index can become too high and make the converter unable to produce the requested ac voltage. The consequent saturation of the voltage can cause current control wind-up, harmonic distortion and loss of controllability. Moreover, when the reference voltage is saturated, the converter does not behave anymore according to the power synchronization control law, making the conventional stability analyses not valid. Despite the relevance of these issues, a systematic analysis about the voltage saturation induced by grid disturbances in power converters is still missing. For that, this paper proposes a mathematical tool based on Bode plots. The target of this tool is to properly chose the converter parameters in order to tolerate grid disturbances without reaching the voltage saturation. Simulations and experiments are provided.**

***Index Terms*—Power Synchronization, Virtual Inertia, Overmodulation, State-Space Modeling**

I. Introduction

The evolution of the power generation from centralized towards distributed is pushing a change in the converter control strategy [1], [2]. Power synchronization control of Voltage Source Converters (VSCs) is gaining a prominent position in this change, for its ability to ensure converter stable operation also in absence of a main stiff grid [3], [4]. Power synchronization generally uses a low-pass filter in the measured active power both for harmonics filtering and for control loops stabilization [5], [6]. This filtering operation is responsible for the converter inertia emulation, proportionally to the filter time constant [5], [7]; inertia emulation results in energy exchange with the dc bus [8], which can bring a high dc voltage excursion.

When the dc voltage dips, the converter is not able to produce the desired reference voltage at the output terminals, if it becomes lower than the reference ac phase-to-phase inverter voltage. This phenomena is known as overmodulation and it causes the loss of converter controllability and high current distortion [9]. In order to avoid it, voltage limitation strategies and anti-windup current controllers have been proposed [9]–[11]. Nevertheless, when the voltage limitation is operational, the converter output ac voltage is different from the reference voltage produced by the control system. In that situation, the converter is not anymore operating as originally designed and there is no warranty that the stability is maintained for the entire duration of the grid disturbance. Thus, for a safe and stable power converter operation, it is desirable to avoid the dc voltage to dip below the ac phase-to-phase voltage, by properly designing the converter controller.

The occurrence of the voltage saturation depends on several factors, including dc nominal voltage, entity of the grid disturbance, dc voltage control bandwidth and frequency droop tuning among them. To have a deeper insight and understand how to address this problem, a mathematical tool for its study is necessary. Despite the relevance of this phenomena, such a tool has not been proposed in literature yet.

In this paper, a state-space model of a power synchronization-based converter including all the control loops and the dc-link dynamics is firstly derived and linearized around its operating point. From the mentioned model, the transfer functions from the grid

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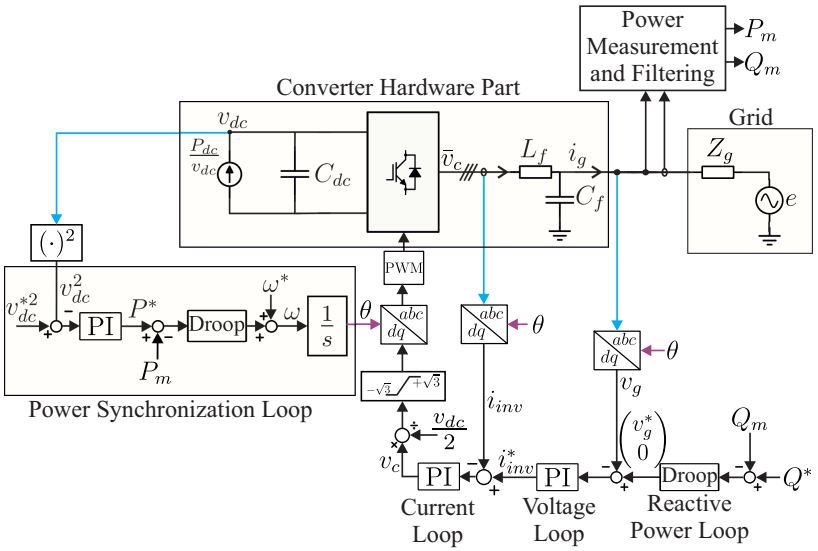


Figure 1: The considered three-phase power converter implementing power synchronization loop and reactive power loop.

disturbances to the modulation index are computed: the Bode plots of the latter transfer functions give a measure of the sensitivity of the modulation index with respect to the grid voltage and frequency disturbances at various frequencies. The higher the magnitude of the Bode plot, the higher the sensitivity and the higher the risk of reaching the voltage saturation after a grid disturbance. Simulations shows that the modulation index sensitivity evaluated through the transfer function is a good measure for the converter voltage saturation risk. The parameter variations, e.g. dc-link nominal voltage and frequency droop coefficients, allow to evaluate the influence of these parameters on the risk of voltage saturation, and to properly tune the controller in order to avoid it. Simulations and experimental results are carried out to validate the feasibility of the proposed analytic tool.

II. System Description and Overmodulation Discussion

The control scheme of the PWM power converter under analysis is depicted in Fig. 1. The synchronization is achieved through a power synchronization loop, composed of an outer dc-link voltage PI controller and an inner frequency droop controller [4]. The dc-link voltage control uses the square of the dc voltage v_{dc} to make the control dynamics independent on the dc nominal voltage [12]. A droop control is used for the reactive power regulation, cascaded with a double voltage-current loop, similar to [6]. The measured active power P_m and reactive power Q_m used in the droop controls are the result of a low-pass filtering [6]. The filtering serves not only to eliminate the measurement noise, but its cut-off frequency has a correlation with the virtual inertia provided by the power converter [5].

The digital delay and the semiconductor switching dynamics are neglected in this study, since they have a much faster dynamics in respect to the dynamics of interest (the dc capacitor discharge). Under this assumption, according to Fig. 1, it yields

$$v_c = \bar{v}_c \tag{1}$$

during normal operating conditions, i.e. when the modulation index defined as the ratio between the peak-to-peak line ac voltage and the dc voltage

$$m_i = 2\sqrt{3}\frac{\sqrt{v_c^T v_c}}{v_{dc}} \tag{2}$$

is lower than 1. The expression $\sqrt{v_c^T v_c}$ is the amplitude of the dq reference voltage v_c. If the modulation index m_i becomes higher than 1, the converter operates in the overmodulation region [10]. By using the third harmonic injection or different modulation techniques, the converter can keep the controllability and a good power quality even with $m_i > 1$ for a certain range [13]. However, there exists in each case a modulation index critical value $\bar{m}_i$ above which the converter is not able to properly produce the reference voltage v_c in the output terminals [10], [14]. In that case, the voltage v_c is saturated, and the condition (1) does not yield anymore [10]. With saturated voltage, the converter does not behave anymore according to the designed control law, and its stability is difficult to predict. Furthermore, the voltage saturation introduces harmonic distortion, loss of converter controllability and even the problem of the integrators wind-up, which needs anti-windup current control strategies to be mitigated [9], [11].

For these reasons, the voltage saturation represents a

risk for the converter stability and has to be avoided. The target of this paper is to investigate in which conditions and under which grid disturbances v_c reaches the voltage saturation level and how to design and tune the converter in order to avoid it. The modulation index critical value is considered $\bar{m}_i = 1$ in the following analysis, without loss of generality for the proposed method.

III. Converter State-Space Modeling

The converter and its control loops are modeled in the state-space through a set of nonlinear differential and algebraic equations [15]–[17] in the form:

$$\begin{cases} \dot{x} = f(x) + g(x) \begin{pmatrix} E_g \\ f_g \end{pmatrix} \\ m_i = h(x) \end{cases} \tag{3}$$

where the grid voltage amplitude E_g and frequency f_g are set as disturbance input variables, expressed in per unit. The state vector in (3) is defined as $x = \begin{pmatrix} i_i & v_g & \Phi_1 & \Phi_g & v_{dc} & \Phi_{dc} & P_m & Q_m & \delta_g & i_g \end{pmatrix}$. The variables Φ_{inv}, Φ_g and Φ_{dc} are the integral states of ac current, ac voltage and dc voltage PI controllers, respectively. The complete converter state-space model is composed of a set of differential equations

$$\begin{cases} \dot{i}_1 = -\Omega i_1 + \frac{1}{L_f} v_c - \frac{1}{L_f} v_g \\ \dot{v}_g = -\Omega v_g + C_f i_1 - C_f i_g \\ \dot{\Phi}_1 = i_1^* - i_1 \\ \dot{\Phi}_g = v_g^* - v_g \\ \dot{v}_{dc}^2 = -\frac{3}{2}\frac{1}{C_{dc}} v_g^T i_g + \frac{1}{C_{dc}} P_{dc} \\ \dot{\Phi}_{dc} = v_{dc}^2 - v_{dc}^{*2} \\ \dot{P}_m = -\omega_f P_m + \omega_f v_g^T i_g \\ \dot{Q}_m = -\omega_f Q_m + \omega_f v_g^T \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} i_g \\ \dot{\delta} = -m_p (P_m - P^*) \\ \dot{i_g} = -\frac{R_g}{L_g} i_g - \Omega i_g + \frac{1}{L_g} \left(v_g - T(\delta) T(\delta_g) E_n \begin{pmatrix} E_g \\ 0 \end{pmatrix} \right) \\ \dot{\delta_g} = 2\pi f_n (f_g - 1) \end{cases} \tag{4}$$

Table I: Simulation parameters for the power synchronization-based converter

Parameters	Values
Line-to-line grid voltage e (V)	690
Short Circuit Ratio of Z_g	1.5
R/X ratio of Z_g	0.3
Nominal active power P_{dc} (MW)	1
Nominal dc-link voltage v_{dc}^* (V)	1200
Switching frequency (kHz)	2
DC-link capacitor C_{dc} (mF)	22
Filter inductor L_f (mH)	0.1

and a set of algebraic equations

$$\begin{cases} v_c = K_p(i_1^* - i_1) + K_i \Phi_1 \\ i_g^* = K_{p_v}(v_g^* - v_g) + K_{i_v} \Phi_g \\ v_g^* = \begin{pmatrix} E_n - n_q (Q_m - Q^*) \\ 0 \end{pmatrix} \\ P^* = K_{p_{dc}} \left(v_{dc}^2 - v_{dc}^{*2} \right) + K_{i_{dc}} \Phi_{dc} \\ T(\delta) = \begin{pmatrix} \cos\delta & \sin\delta \\ -\sin\delta & \cos\delta \end{pmatrix} \\ \Omega = \begin{pmatrix} 0 & -\omega \\ \omega & 0 \end{pmatrix} \end{cases} \tag{5}$$

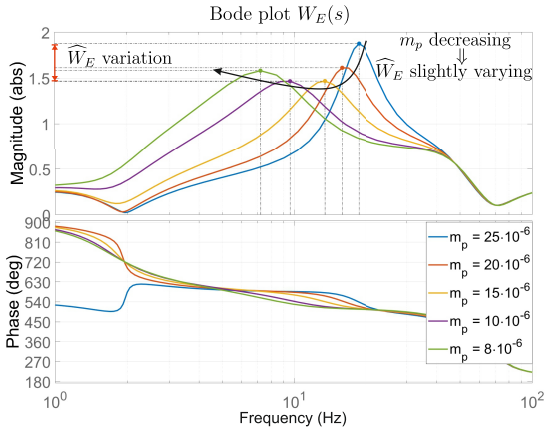
ω_f is the power filter time constant, E_n and f_n are the grid voltage nominal amplitude and frequency respectively, m_p is the P-ω droop gain, n_q is the Q-V droop gain and v_g is the voltage across the capacitor C_f. The parameters K_p and K_i are the current controller proportional and integral gains, K_{p_v} and K_{i_v} the ac voltage controller proportional and integral gains, $K_{p_{dc}}$ and $K_{i_{dc}}$ are the dc voltage controller proportional and integral gains. Φ_1, Φ_v and Φ_{dc} are the integral states of inner current loop, ac voltage controller and dc voltage controller, respectively. The modulation index m_i is chosen as the output of the model (3), and it can be expressed through (2).

IV. A Mathematical Tool for the Study of the Voltage Saturation

The first step to investigate the voltage saturation phenomena is to quantitatively study how the modulation index varies in response to grid disturbances. The saturation is more likely to occur when the modulation index is highly *sensitive* to grid disturbances, e.g. the converter reacts to a relatively small grid disturbance with a relatively large oscillation in the modulation index. The information about this sensitivity is enclosed in the input-output characteristic of the model (3), which indeed has been defined with the grid voltage and frequency as input and the modulation index as output. The modulation index expression (2) as well as

Table II: Analytic results of the Bode analysis done in Fig. 2

Frequency droop gain m_p	$25 \cdot 10^{-6}$	$20 \cdot 10^{-6}$	$15 \cdot 10^{-6}$	$10 \cdot 10^{-6}$	$8 \cdot 10^{-6}$
$\widehat{W}_E$	1.87	1.62	1.46	1.46	1.58
$\widehat{W}_f$	24.54	31.14	42.62	67.71	88.80
$\Delta m_i = \widehat{W}_f \Delta f_g$	0.15	0.19	0.25	0.4	0.53
$m_{i,eq} + \Delta m_i$	0.73	0.77	0.83	0.98	**1.11**



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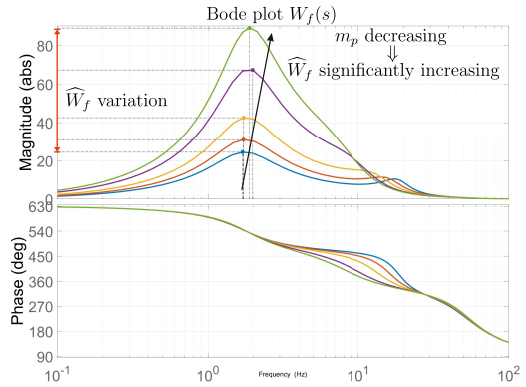

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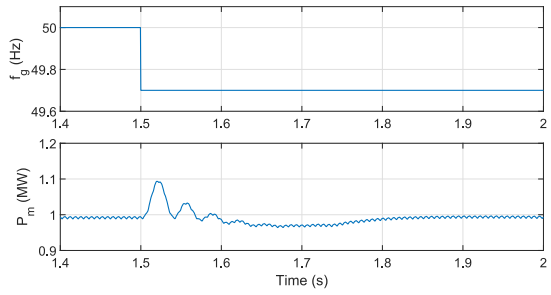
Figure 2: The proposed Bode analysis under different values of the frequency droop gain. (a) The frequency response from a voltage disturbance to the modulation index. (b) The frequency response from a frequency disturbance to the modulation index.



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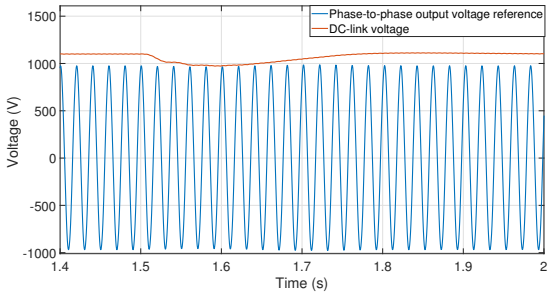


(b)

Figure 3: Simulation of a frequency dip for the power converter in the case of $m_p = 10 \cdot 10^{-6}$. (a) The frequency dip and the converter active power (b) The converter dc and ac terminal voltages.

the saturation phenomena itself are nonlinear. However, the modulation index *sensitivity* in respect to small-signal grid disturbances can be investigated also with linear analysis tools. It will be shown through simulation results that the modulation index sensitivity obtained through the proposed linear analysis is a good measure of the risk of voltage saturation in response to grid disturbances.

For the proposed study, the steady-state values of the state x and modulation index m_i are needed. The equilibrium state x_{eq} is computed by numerical integration of the nonlinear model in (3) in the grid nominal point defined by $E_g = 1$ p.u., $f_g = 1$ p.u. for a time T large enough:

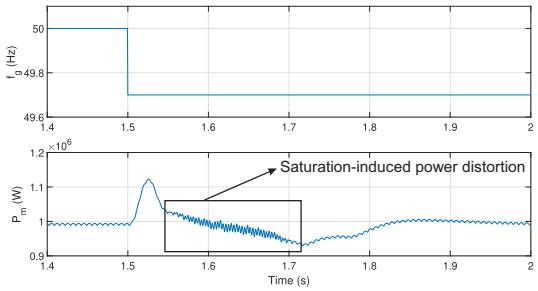
$$x_{eq} = \int_0^T f(x) + g(x) \begin{pmatrix} 1 \\ 1 \end{pmatrix} dt \tag{6}$$

The output function $h(x)$ is then evaluated in the equilibrium state x_e computed through (6), obtaining the steady-state value of the modulation index

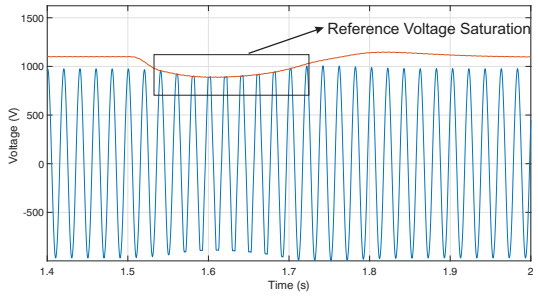
$$m_{i,eq} = h(x_{eq}) \tag{7}$$

The nonlinear model in (3) is linearised through Jacobian matrices computation, obtaining:

$$\begin{cases} \dot{x} = Ax + B \begin{pmatrix} E_g \\ f_g \end{pmatrix} \\ m_i = Cx \end{cases} \tag{8}$$



(a)



(b)

Figure 4: Simulation of a frequency dip for the power converter in the case of $m_p = 8 \cdot 10^{-6}$. (a) The frequency dip and the converter active power (b) The converter dc and ac terminal voltages.

From the linearised model (8), the transfer function $W(s)$ can be computed as $W(s) = C\,(sI - A)^{-1}\,B$.

$$m_i = W(s)\begin{pmatrix} E_g \\ f_g \end{pmatrix} = \begin{pmatrix} W_E(s) & W_f(s) \end{pmatrix}\begin{pmatrix} E_g \\ f_g \end{pmatrix} \quad (9)$$

The transfer function $W(s)$ is a 1×2 matrix: the element $W_E(s)$ describes how a disturbance in the voltage amplitude E_g reflects on the modulation index m_i, while $W_f(s)$ describes the influence of a grid frequency f_g disturbance on m_i. The peak magnitudes of $W_E(s)$ and $W_f(s)$, highlighted with the colored dot in Fig. 2, are denominated $\widehat{W}_E$ and $\widehat{W}_f$ respectively, and given in Table II. They represent the maximum gain from a generic grid disturbance to the modulation index, and give therefore a measure for the modulation index *sensitivity*: the higher the peak magnitudes, the more *sensitive* the modulation index to grid disturbances, the higher the risk of voltage saturation. Being this analysis based on the linearised system, the obtained results are accurate for small grid disturbances (± 0.15 p.u. for E_g, ± 0.5 Hz for f_g) and loose progressively the accuracy for larger disturbances.

A 1 MW power converter as in Fig. 1 is modeled according to (3), linearised, and the its transfer function $W(s)$ as defined in (9) is computed. The converter and grid parameters are summarized in Table I.

In Fig. 2, $W(s)$ is plotted for different values of m_p, to see its influence on the modulation index sensitivity. Table II reports the magnitude peak values of $W_E(s)$ and $W_f(s)$ in Fig. 2. By decreasing m_p, the equivalent inertia provided by the converter increases [5] and higher active power is injected during the frequency dips. Therefore, the dc capacitor discharges more, increasing the risk of voltage saturation. This intuition is confirmed by the Bode plot of $W_f(s)$ in Fig. 2 where the peak magnitude increases when m_p decreases. Conversely, $W_E(s)$ does not vary significantly with m_p.

Table III: Back-to-back converter and power amplifier parameters

Parameters	**Values**
Line-to-line power amplifier voltage e (V)	430
Power amplifier inductance Z_g (mH)	7.5
R/X ratio of Z_g	0.3
Power rating P_{dc} (kW)	4
DC-link voltage v^*_{dc} (V)	700
Switching frequency (kHz)	10
DC-link capacitor C_{dc} (mF)	1.2
Filter inductor L_f (mH)	5.5

V. Simulation Results

The Bode analyses in Fig. 2 and Table II reveal if the converter is able to support a given grid disturbance without reaching voltage saturation with different values of m_p. Considering a frequency dip $\Delta f_g = 0.006$ p.u., corresponding to 0.3 Hz, the consequent modulation index deviation Δm_i is computed as $\widehat{W}_f \Delta f_g$ and reported in Table II for different values of m_p. The steady state value of the modulation index, computed through (6), is $m_{i,eq} = 0.58$. From $m_{i,eq}$, if the modulation index deviation Δm_i is high enough to bring m_i above 1, the converter will reach the voltage saturation during the disturbance. Table II report the value of $m_{i,eq} + \Delta m_i$ which becomes higher than 1 only in the case $m_p = 8 \cdot 10^{-6}$, marked in bold font. The simulations in Figs. 3 and 4 are realized to validate the analytic results of Table II. A frequency dip $\Delta f_g = 0.006$ is simulated at the instant $t = 1.5s$ and the converter response is evaluated in the cases $m_p = 10 \cdot 10^{-6}$ and $m_p = 8 \cdot 10^{-6}$, according to the mathematical analysis reported in Table II. In Fig. 3, the dc capacitor C_{dc} discharges during the frequency dip, but not enough to go below the ac terminal voltage and trigger the voltage saturation. Different is the case of Fig. 4, where the dip results in a modulation index deviation Δm_i large enough to trigger the saturation. Indeed, ac voltage reference saturation due to overmodulation can be observed in Fig. 4(b). The consequence of the voltage saturation is the output power distortion, evident in Fig. 4(a). The phenomena of windup is avoided thanks to a anti-windup strategy implemented in the current control [9]. The simulation results in Figs. 3 and 4 are in

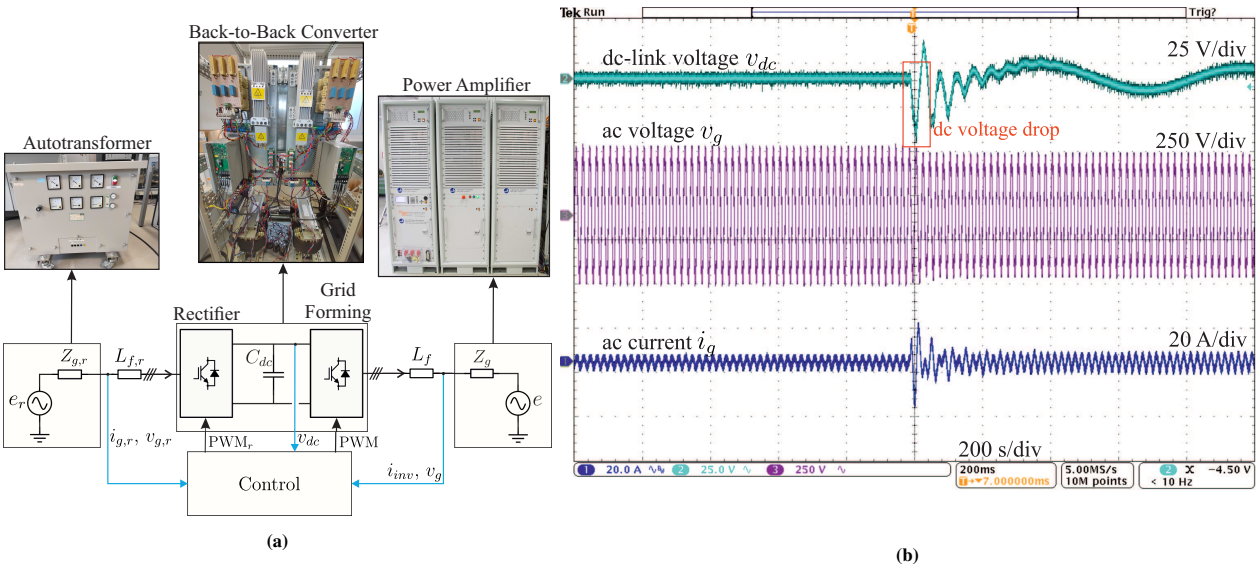


Figure 5: Experimental results. (a) The experimental setup. (b) Grid voltage sag in the considered experimental setup.

accordance with the analytic results in Fig. 2 and Table II.

It is important to notice that with the tuning $m_p = 8 \cdot 10^{-6}$, whereby the converter reaches the voltage saturation level, the converter is small-signal stable. That reveals that voltage saturation and small-signal stability are two distinct aspects: a controller tuning, which implies good and robust small-signal stability has no implication on the risk of voltage saturation, and vice versa. Therefore, it is important to consider the voltage saturation risk as a target in the converter tuning and design, in particular when implementing virtual inertia and active power support strategies, which cause wide fluctuations of the dc voltage and it is potentially dangerous for the voltage saturation [18], [19].

VI. Experimental Results

The converter in Fig. 1 is reproduced in the lab with a 4 kW scaled-down setup, as shown in Fig. 5(a). The dc power P_{dc}, modeled in Fig. 1 as a current source, is generated by a rectifier connected in back-to-back configuration with the considered VSC. A DSpace® MicroLabBox is used to control the back-to-back converter. A voltage sag of 0.2 p.u. is applied in the power amplifier, and dc voltage, ac voltage and ac current are shown in Fig. 5(b). In the instant of the sag, the dc voltage rapidly decrease, before being restored from the control to its nominal value. In case the dc voltage drop is large enough, voltage saturation can occur and jeopardize the converter integrity and stability.

VII. Conclusion

In this paper, the voltage saturation phenomena triggered by grid disturbances are studied starting from the complete state-space model of a power synchronization-based power converter. The transfer functions from the grid voltage magnitude to the modulation index, $W_E(s)$, and from the grid frequency to the modulation index, $W_f(s)$, are derived. The higher the peak magnitudes of these two transfer functions, the more *sensitive* the modulation index to the grid voltage and frequency variations, and the higher the risk of voltage saturation. Different values of the frequency droop coefficient result in different modulation index sensitivity, providing a guideline to tune this parameter with the consideration of voltage saturation. Simulation results show furthermore that voltage saturation and small-signal instability are two different concepts: a converter can suffer from the voltage saturation problem due to not proper controller tuning even when the used parameters ensures a good and robust small-signal stability.

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