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### **Performance Evaluation of the Multiwinding Redundancy Approach in MTB DC-DC Converters**

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# Performance Evaluation of the Multiwinding Redundancy Approach in MTB DC-DC Converters

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**Abstract**—The Multiwinding transformer-based (MTB) DC-DC converter topologies have been investigated to be applied as the key component in different application fields, in particular those which are safety-critical ones, such as aerospace, energy distribution, and data-centers (data-processing). Thus, this paper presents a fault-tolerance concept associated with the possibility of operating the MTB topologies even under fault conditions, by only disconnecting the faulty cell and keeping the healthy ones operating continuously. In this approach, named multiwinding redundancy (MWRed), the MTB converter is equipped with additional isolation switches which enhance its fault-tolerant capability. In contrast to competing approaches, MWRed utilizes the magnetic coupling of the MWT to reduce the use of several redundancies, which makes the strategy more appealing in critical applications. Further, in order to evaluate the impact of the isolation switches on MTB converters, the MWRed is assessed in terms of efficiency and reliability, so that the superior advantages to conventional approaches are presented and demonstrated. Finally, the investigated MWRed is evaluated experimentally to validate its effectiveness in different scenarios.

**Index Terms**—Active Bridge, DC-DC Converter, Fault-Tolerant Capability, Fault-Tolerance, Isolation Switches, Multiwinding Transformer (MWT), Modular Converters, Reliability.

## I. INTRODUCTION

THE isolated DC-DC converter has been widely used in a large range of voltage and power applications. Since most of the power electronic converters do not present an inherent redundancy, any failure in these components might result in an interruption of the operation. However, in some application, such as aerospace (more electric aircraft [1], [2]), distribution energy (e.g., a smart transformer [3], [4]), telecommunication, or even in renewable energy system [2], [5], the continuity of operation is of paramount importance. In fact, a failure of the power converter affects not only the operational cost but also the maintenance cost once the service is interrupted. For that reason, a highly available and reliable system is required.

Since the lifetime of power semiconductors is generally much shorter than the passive components, the reliability of DC-DC converters, which might contain several power semiconductor devices, is one of the most critical concerns for the safe operation of the system [5]–[7]. The solutions to improve the reliability and lifetime of the DC-DC converter are still an open topic which deserves attention. In this scenario, several non-isolated and isolated DC-DC converter topologies have been widely investigated in the literature for integrating distributed DC power sources, storage units, and DC loads,

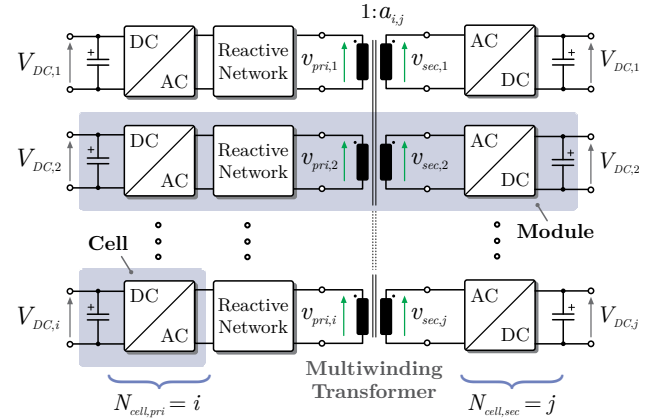


Figure 1. Generic scheme of the MTB DC-DC converter topology, consisting of cells coupled magnetically by using the MWT to compose entire system. Whereas  $i = 1, 2, \dots, N_{cells,pri}$ ,  $j = 1, 2, \dots, N_{cells,sec}$  and  $a_{i,j} = n_{sec,j}/n_{pri,i}$  is the turn-ratio between the  $i$ th and  $j$ th winding.

increasing the conversion efficiency and enhancing the fault-tolerant capability. However, the isolated multiport DC-DC converters, in particular, those based on the MWT have been drawn more attention, due to their advantages related to the inherent magnetic coupling provided by the MWT [8].

The MTB DC-DC converter consists of several cells connected to the same MWT, as illustrated in Figure 1 [8]. In this modular architecture, the MWT performs an important role by establishing the high-frequency magnetic coupling between the cells and consequently composing the modules and the overall MTB converter. As a result, the MWT can ensure redundant power paths, which provide an alternative fault-tolerant capability by means of this magnetic coupling.

In this context, this paper evaluates a fault-tolerance concept based on the MWT, considering the reconfiguration and continuous operation of MTB DC-DC converters [9]. The proposed fault-tolerant approach is quite promising for safety-critical applications, since the inherent and redundant power path created by the MWT permits that the power could be smoothly and efficiently routed among the cells. Therefore, when one cell fails, the power flow is reestablished among the healthy ones, so that the MTB DC-DC converter might continue its operation without interruption in the power processing. The performance of the MWRed is ensured by means of fault management which defines how and when the system should be reconfigured to maintain the power flow. Further, the

MWRed approach is also evaluated with respect to efficiency, reliability, and availability, demonstrating lower impact of the isolation switches on the MTB DC-DC converter.

The paper is organized as follows: Section II shows the failure analysis and prevalent fault-tolerant approaches. Section III assesses the MWRed approach and its features to keep the continuous operation. Section IV presents the implemented prototype and some experimental results. In Section V, the outcomes are discussed.

## II. FAILURE ANALYSIS AND PREVALENT FAULT-TOLERANT APPROACHES

### A. Failure Analysis and Reliability Requirements

The large number of fragile components in power electronics systems includes semiconductors, capacitors, sensors and integrated circuit, which have a high influence on the reliability, as expressed in (1). The reliability function  $R_{syst}(t)$ , cf. (1), indicates the probability that the converter will operate without failures during a time interval.

$$R_{syst}(t) = R_{syst}(0) \cdot e^{-\int_0^t \lambda_{syst}(\tau) d\tau} \quad (1)$$

Where  $R_{syst}(0)$  is the initial reliability of the system, i.e. when  $R_{syst}(0) = 1$ , the system is fully functional at initial state;  $\lambda_{syst}(t)$  is the failure rate, which indicates the number of failures per unit time (i.e. one *failure in the time*: 1 FIT =  $10^{-9}$  failure/hour).

The failure of aforementioned components can be generally classified as catastrophic failure and wear-out failure. The wear-out failure is mainly induced by accumulated degradation during the time, while catastrophic failure is caused by an unexpected overstress, such as overvoltage, overheat (originated by overload, short-circuit, or start-up transient [5]–[7]).

In this scenario, regardless of the reason, the damaged component can assume one of the states: open-circuit (OC) or short-circuit (SC). Consequently, depending on its role and position within the system, the damaged component can affect partial the normal operation of the system or even interrupt the power flow. Thus, minimizing the impact of these failures by means of a fault-tolerant strategy, the system's availability ( $A_{syst}$ ) can be significantly extended, cf. (2), by increasing the overall mean time to failure (whereas  $\sigma = \text{MTTR}_{syst}/\text{MTTF}_{syst}$ ). In other words, this means that the system is able to operate even under faulty conditions so that the power flow can be reduced but hardly interrupted.

$$A_{syst} = \frac{\text{MTTF}_{syst}}{\text{MTTF}_{syst} + \text{MTTR}_{syst}} = \frac{1}{1 + \sigma} \quad (2)$$

The  $\text{MTTF}_{syst}$  is the expected time before a failure occurs and  $\text{MTTR}_{syst}$  is the mean repair time that it takes to eliminate a failure and to restore the system operation. The repair time depends on maintainability, such as effective diagnosis of faults, operational time to replace the faulty cell, and so on. In contrast to the reliability,  $\text{MTTF}_{syst}$  provides only the average time that the system operates without failing [10]–[12]. Hence,

the relation between MTTF and reliability function is defined by (3), when the useful-life region of the "bathtub curve" is considered, so that  $\lambda_{syst}(t)$  is constant and it can be assumed that  $\lambda_{syst}(t) = \lambda_{syst}$ .

$$\text{MTTF}_{syst} = \int_0^{+\infty} R_{syst}(\tau) d\tau = 1/\lambda_{syst} \quad (3)$$

Thus, for the DC-DC converters,  $\lambda_{syst}$  is defined by  $\lambda_{syst} = (\sum_{k=i+j} \lambda_{cell,k})$ , where  $\lambda_{cell}$  is the resulting failure rate of all individual components' failure rates (e.g. capacitor, power semiconductors switches), so that  $\lambda_{cell} = \lambda_{cap} + \lambda_{sw} + \dots$ .

### B. Overview of the Prevalent Fault-Tolerant Approaches

The fault-tolerant feature contributes to increase the availability of the system and several fault-tolerance solutions have been proposed in the literature [2], [5], [7], [13]–[21]. Among the most often solutions in industry and academia, the fault-tolerant approaches based on overdesign, hardware redundancy are the most popular ones [5], [15], [22]. However, due to the inherent advantages of the MTB topologies, the MWRed approach based on the MWT is introduced, as will be discussed in the next section.

1) *Overdesign*: The simplest solution is to overdesign the most critical components of the system. The overdesign of a component is defined as the design margin which provides the safe operation of the circuit even under the worst-case operating conditions [7], [23]. Although this approach might increase the cost and reduce the power density ( $\text{W}/\text{m}^3$ ), the overdesign is usually adopted when the failure cause is unknown and when the system should work in a wide range of operation points. For the DC-DC converter, this approach might be suitable for passive components (e.g. capacitors, inductors, and transformer) and even mechanical ones such as the cooling system (i.e. heatsink).

2) *Hardware Redundancy*: In this scenario, the most frequently adopted solution for enhancing the availability of the power converter is to use hardware redundancy. In this approach, the converter is implemented by connecting multiple redundant elements (i.e. extra switch, phase-leg, or the entire module) in series or parallel (cf. Figure 2).

Based on the application of hardware redundancy, this strategy is divided into three categories: switch-level [cf. Figure 2 (a)–(c)]; phase-level [cf. Figure 2 (d)] and converter-level [Figure 2 (e) and (f)] [5]–[7]. Further, the hardware redundancy can still be implemented in two different modes: standby or power-sharing [5], [7]. In the standby mode, if some main element fails, the standby one is inserted into the system to replace the faulty element, as illustrated in Figure 2. On the other hand, in power-sharing mode, since the additional elements are involved in the power flow, they can work at the same time along with the main ones.

For isolated DC-DC converters based on 2WT, such as DAB, LLC, or SR converter, depending on the application and how the modules are interconnected, the redundancy approach might require an extra-module as a replaceable part of the whole system, as depicted in Figure 2 (f). Besides

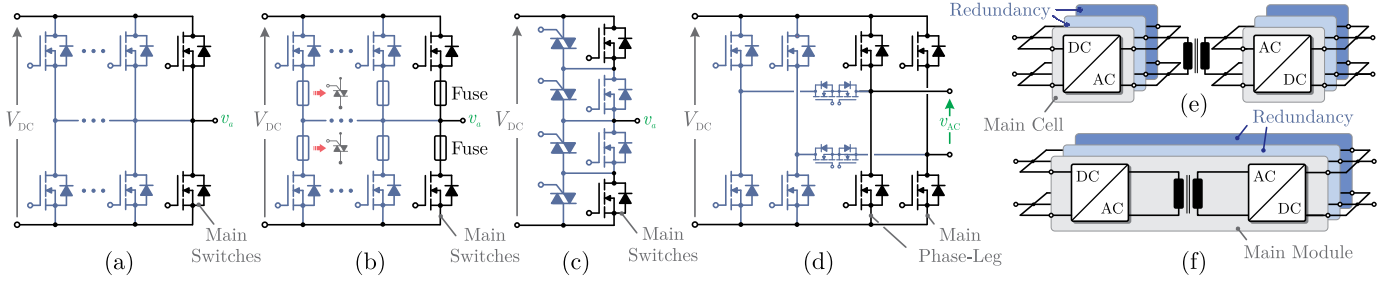


Figure 2. Prevalent hardware redundancy approach for: (a) switch-level considering the parallel connection of extra switches in a phase-leg for the power-sharing mode; (b) extra switches in a phase-leg for the standby mode through a relay (mechanical or solid-state switch), TRIAC, and/or fuse; (c) switch-level considering the series connection of extra switches in a phase-leg for the standby mode by using TRIAC; (d) phase-leg considering the parallel connection of extra phase-legs in full bridge topology for both modes (standby or power-sharing mode) through bidirectional switches (anti-series configuration of transistors, relay or TRIAC); (e) converter-level considering the parallel connection of extra cells or (f) modules in both modes, depending on the application, the most convenient mode can be adopted, including the strategy to connect and disconnect the extra components to the system.

the cost, even with redundant parts available, the transition time to restore the operation of a complete module can be relatively slow and risky due to the hazardous transients (e.g. overvoltage and overcurrent). Therefore, DC-DC converter topologies based on magnetic coupling provide an interesting solution for this issue, since the redundant power path is an inherent feature of these power converters. In this context, the MWRed approach is investigated for both non-resonant and resonant MTB converters, as discussed next.

### C. Multiwinding Redundancy Approach

As discussed before, most of fault-tolerance solutions include a significant amount of extra hardware (such as semiconductors, phase-leg redundancy, or series connection of fuses/switches to isolate the fault), increasing in some of the cases the cost and complexity, as well as compromising the efficiency of the system. Moreover, the inclusion of extra elements connected to the main devices increases the total stray inductance, representing an issue for fast-switching devices (e.g. of wide-bandgap devices). Thus, special attention must be given during the transient, since the stored energy in the passive components can be enough to propagate the faults through the power converter [5].

In this context, this section presents a fault-tolerance solution with a minimum of additional hardware (by means of isolation switches based on MOSFETs/IGBTs, for example) and minor impact on the efficiency of the converter, using the advantage of the inherent fault-tolerant capability of the MTB topology and its redundant power paths, as shown in Figure 3.

The proposed fault-tolerant approach aims at the realization of DC-DC converters with particular attention to the continuous operation of the system, even under faulty conditions. For that reason, the fault-tolerant scheme is composed of isolation switches (i.e. bidirectional arrangement of power semiconductor devices or simple mechanical switches), which acts directly on the cells, either disconnecting the faulty cell in case of any failure or connecting the healthy ones, i.e. redundant cells (standby mode).

In Figure 3, the cells of the power converter can operate either in power-sharing mode, where the main and redundant

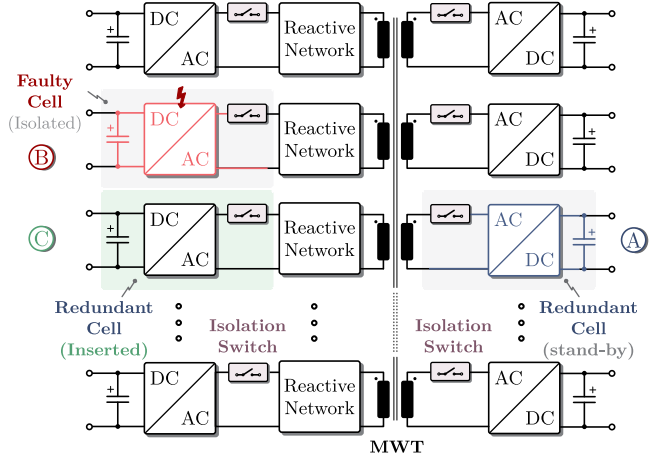


Figure 3. Generic scheme of the proposed fault-tolerance solution based on multiwinding redundancy approach: (A) normal operation with redundant cells in standby mode and others in power-sharing mode (as part of the MTB DC-DC converter), (B) reconfiguration example after a fault by means of the isolation switches to disconnect the faulty cell and (C) connect the redundant cell previously in standby (or just routing the power by the healthy ones).

parts perform the same role, or the converter can be designed considering extra windings so that some standby cells might be integrated into the converter. Both approaches are equally feasible, the implementation will depend only on the design requirements and the cost constraints from each application. In normal conditions, all cells of the converter might operate simultaneously, sharing the power among the cells. In case of a fault, only the faulty cell is isolated from the entire system, as shown in Figure 3, whereas the healthy cells maintain the power flow and the system operating.

In contrast to the conventional converter-level redundancy aforementioned, cf. Figure 2 (e)-(f), the MWRed approach can further reduce the number of redundant cells. For instance, considering the particular application, where multiple isolated-DC sources/loads (or a single one shared in parallel by the cells) should be interconnected by means of the main DC bus, cf. Figure 4. As can be noted, in the 2WT-based DC-DC converters whether only one single cell fails, the module (i.e. two cells) will be thoroughly affected, so that the power flow is

interrupted, cf. Figure 4 (a). On the other hand, comparatively to multiples 2WT-based converters, MTB DC-DC converters are able to keep the power flow, cf. Figure 4 (b). This happens because the 2WTs are not coupled, and thus the power cannot be routed among the other healthy cells in this kind of system.

As a result, the inherent redundancy provided by the magnetic coupling between the cells along with the isolation switches can reduce up to 50 % the number of redundant cells  $N_{red}$ , as illustrated in Figure 4 and listed in Table I.

Table I  
REQUIRED NUMBER OF STANDBY REDUNDANT CELLS  $N_{red}$ .

Architecture	Primary Side	Secondary Side	Total
2WT-based Converter	$N_{cell,pri}$	$N_{cell,sec}$	$2N_{cell,i,j}$
MWT Converter	$N_{cell,pri}$	0	$N_{cell,i,j}$

### III. ANALYSIS AND ASSESSMENT OF THE MULTIWINDING REDUNDANCY APPROACH

#### A. Current on the Resonant Network

The *rms* current on the resonant network and hence on the isolation switches can be defined by (4) and (5), for the non-resonant and resonant MTB topologies, cf. Figure 5 (a), respectively. In Figure 5 (b) is illustrated these currents in terms of the power processed by each port, considering the same voltage on the ports. As can be seen, in this particular case, the *rms* current values are roughly the same.

$$I_{L,pri,res(rms)} = \frac{\pi P_o}{2a\sqrt{2}V_{DC,i,j}} = \frac{I_{L,sec,res(rms)}}{a} \quad (4)$$

$$I_{L,pri,nres(rms)} = \frac{\sqrt{\pi^3 k_1^2 + k_2}}{4\pi f_{sw} L_{eq} \sqrt{3\pi}} = a I_{L,sec,nres(rms)} \quad (5)$$

Whereas,  $k_1$  and  $k_2$  are defined by (6) and (7), respectively.

$$k_1 = (V_{DC,i} - V_{DC,j}) \quad (6)$$

$$k_2 = 4\varphi^2 V_{DC,i} V_{DC,j} (3\pi - 2\varphi) \quad (7)$$

Further,  $V_{DC,i,j}$  is the voltage on each port,  $L_{eq}$  is the equivalent inductance of the reactive network seen by the primary-side (i.e. leakage and external inductances),  $a_{i,j} = a$  is the turn-ratio,  $f_{sw}$  is the switching frequency,  $\varphi$  is the phase-shift angle considering the single phase-shift (SPS) modulation employed in the non-resonant converters, and  $P_o$  is the power processed by each port of the MTB converter.

#### B. Losses Analysis on the Isolation Switches

Once the isolation switches, cf. Figure 6 (a), operate permanently under two states: either conducting (normal condition) or blocking (faulty condition), the switching losses might be assumed zero in this application (i.e.  $P_{loss,sw} = 0$ ). Thus, the total instantaneous power losses are fully defined by the conduction losses, which can be estimated by (8), where the instantaneous voltage  $v(i_L(t), V_{gate}, T_j)$  on the power semiconductor device is function of the instantaneous current  $i_L(t)$  through the device, junction temperature ( $T_j$ ), and gate voltage ( $V_{gate}$ ).

$$p_{loss}(t) = v(i_L(t), V_{gate}, T_j) \cdot i_L(t) \quad (8)$$

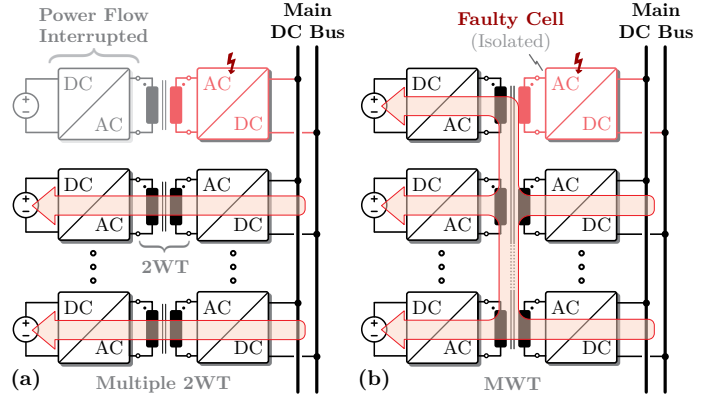


Figure 4. Interconnection among multiple DC sources (e.g. PV system, storage system, super-capacitor, and so on) considering systems based on: (a) multiple 2WTs (requiring in total  $2N_{cell,i,j}$  redundant cells) and (b) one MWT (requiring in total  $N_{cell,i,j}$  redundant cells). For a fault in one of those cells connected to the main bus, MTB topologies are able to ensure at least the partial power from all isolated DC sources/loads, by using the MWRd.

Thus, the integration of the instantaneous power losses over one switching period provides the average value of the conduction losses  $P_{loss}$ , as defined by (9).

$$P_{loss} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v(i_L(\tau), V_{gate}, T_j) \cdot i_L(\tau) d\tau \quad (9)$$

Considering the conduction characteristics of the respective power semiconductor device, cf. Figure 6 (b)-(c), and assuming that  $T_j$  and  $V_{gate}$  are constants, (9) can be rewritten in terms of loss parameters (cf. Table II). These loss parameters are obtained by means of a first-order approximation at the quiescent point ( $v(i_L), i_L$ ) of the non-linear  $i$ - $v$  characteristic curve of the power semiconductor device, cf. Figure 6 (d), so that (9) is simplified to (10).

$$P_{loss}^{IGBT} = \frac{1}{\pi} \left( \int_{\alpha}^{\pi+\alpha} (V_{CE} + V_F) \cdot i_L(\tau) d\tau + \int_{\alpha}^{\pi+\alpha} (R_{CE} + R_D) \cdot i_L^2(\tau) d\tau \right) \quad (10)$$

Whereas, the angle  $\alpha$  is calculated according to (11).

$$\alpha = \begin{cases} 0 & \text{for resonant topologies} \\ \frac{2i_L(0)\pi f_{sw} L_{eq}}{V_{DC,i} + V_{DC,j}} & \text{for non-resonant topologies} \end{cases} \quad (11)$$

Thus, solving (10) yields the total power losses on the isolation switch based on IGBTs, for both non-resonant and resonant topologies, as defined by (12) and (13), respectively.

$$P_{loss,nres}^{IGBT} = k_3 \left\{ (R_D + R_{CE}) (\pi^3 k_1^2 + k_2) + 12\omega_{sw} L_{eq} (V_F + V_{CE}) [\alpha(\pi k_1 - \alpha k_4) + k_5] \right\} \quad (12)$$

$$P_{loss,res}^{IGBT} = \frac{2I_{L(pk)}(V_{CE} + V_F)}{\pi} + \frac{I_{L(pk)}^2(R_D + R_{CE})}{2} \quad (13)$$

Table II  
LOSS PARAMETERS OF IGBT AND MOSFET CONSIDERING THE FIRST-ORDER APPROXIMATION AT QUIESCENT POINT  $(v(i_L, V_{gate}, T_j), i_L)$ .

Power Semiconductor Device	Transistor Characteristics		Anti-parallel or Body Diode Characteristics	
	On-State Resistance (m $\Omega$ )	Forward Voltage (V)	On-State Resistance (m $\Omega$ )	Forward Voltage (V)
IGBT	$R_{CE}$	$V_{CE}$	$R_D$	$V_F$
MOSFET	$R_{DS}$	—	$R_{BD}$	$V_F$

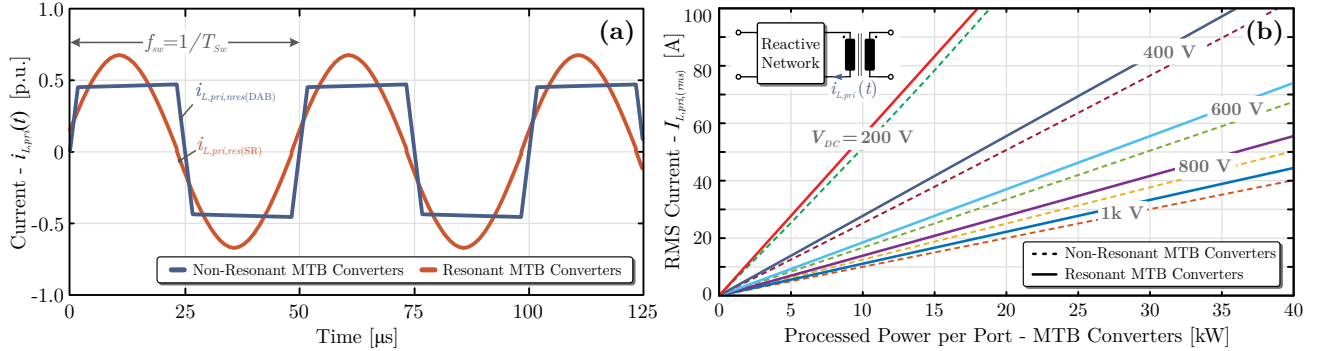


Figure 5. (a) Current waveform on the reactive network of the non-resonant and resonant MTB converter (whereas  $f_{sw}$  = resonance frequency = 20 kHz). (b) *rms* Current  $I_{L,pr,i,(rms)}$  on the reactive network and isolation switches considering both operation modes of the MTB Converters: resonant and non-resonant in terms of processed power and voltage on the ports.

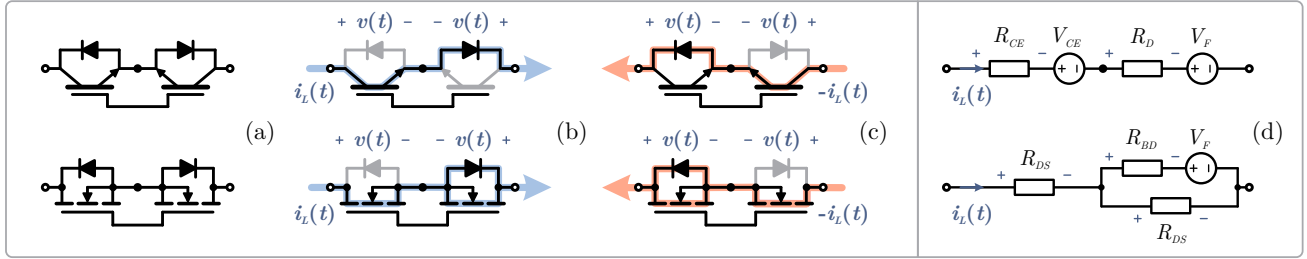


Figure 6. (a) Isolation switch arrangement based on IGBT and MOSFET; Conduction of a (b) positive current and (c) negative current through the isolation switches for a direct and reverse power flow; and (d) the equivalent first-order model, i.e.  $v(i_L) = v_0 + i_L \cdot r_{on}$ , considering the resulting loss parameters.

Whereas,  $k_3$ ,  $k_4$  and  $k_5$  are given by (14), (15) and (16).

$$k_3 = \frac{1}{12\pi\omega_{sw}^2 L_{eq}^2} \quad (14)$$

$$k_4 = (V_{DC,i} + V_{DC,j}) \quad (15)$$

$$k_5 = \varphi(2\alpha + \pi - \varphi)V_{DC,j} \quad (16)$$

Differently of IGBTs, the MOSFETs are able to conduct simultaneously current through its main channel and body diode, as shown in Figure 6 (c), depending on the reverse conduction characteristics (third-quadrant operation) of the employed MOSFET. Thus, in order to estimate properly the power losses of isolation switches, the reverse conduction characteristic should be considered in the losses analysis.

For this purpose, the first-order approximation of  $v(T_j, V_{gate}, i_L)$  is used to derive the analytical expressions in terms of the loss parameters. As a result, at a specific quiescent point, (9) can be simplified to (17) or (18), where the indices (1) and (2) represent respectively the expression without and with reverse conduction.

$$P_{loss(1)}^{MOS} = \frac{2}{\pi} \int_{\alpha}^{\pi+\alpha} R_{DS} \cdot i_L^2(\tau) d\tau \approx 2(R_{DS} I_{L,rms}^2) \quad (17)$$

$$P_{loss(2)}^{MOS} = \frac{1}{\pi} \left( \int_{\alpha}^{\pi+\alpha} R_{DS} \cdot i_L^2(\tau) d\tau + \int_{\pi+\alpha}^{2\pi+\alpha} R_{DS} \left( \frac{i_L R_{BD} - V_F}{R_{DS} + R_{BD}} \right)^2 d\tau + \int_{\pi+\alpha}^{2\pi+\alpha} R_{BD} \left( \frac{i_L R_{DS} + V_F}{R_{DS} + R_{BD}} \right)^2 d\tau - \int_{\pi+\alpha}^{2\pi+\alpha} V_F \left( \frac{i_L R_{DS} + V_F}{R_{DS} + R_{BD}} \right) d\tau \right) \quad (18)$$

The reverse conduction is achieved when (19) is true [24].

$$P_{loss}^{MOS} = \begin{cases} P_{loss(1)}^{MOS} & \text{if } V_F > (i_L(t) \cdot R_{DS}) \\ P_{loss(2)}^{MOS} & \text{if } V_F \leq (i_L(t) \cdot R_{DS}) \end{cases} \quad (19)$$

Similarly, solving (18) yields the total power losses on the isolation switch based on MOSFETs, as defined by (20) and (21), respectively, where  $k_6 = R_{DS}/(R_{DS} + R_{BD})$ .

$$P_{loss,nres(2)}^{MOS} = k_3 k_6 \left\{ (R_{DS} + 2R_{BD})(\pi^3 k_1^2 + k_2) + 12\omega_{sw} L_{eq} V_F [\alpha(\pi k_1 - \alpha k_4) + k_5] \right\} \quad (20)$$



$$P_{loss,res(2)}^{MOS} = \frac{k_6 I_{L(pk)} V_F}{\pi} + \frac{k_6 I_{L(pk)}^2 (R_{DS} + 2R_{BD})}{2} \quad (21)$$

As a matter of comparison, the losses of the isolation switches based on IGBTs and SiC MOSFETs are illustrated in Figure 7, considering different junction temperature  $T_j$ . As can be seen, at the low-power level range, the isolation switch based on SiC MOSFETs presents better performance. However, for the high-power level range, the IGBTs overcome the MOSFETs, since the body diode losses on the SiC MOSFET enlarge even further the losses during the reverse conduction. Besides, the main advantages of SiC MOSFETs are barely used in this application for power level above 20 kW.

Finally, in order to verify quantitatively the performance of the MTB converters in terms of efficiency after the insertion of the isolation switches, they were evaluated considering the following electrical specifications and parameters: 400 V, 10 kW, 20 kHz,  $a_{i,j} = 1$  and  $L_{eq} = 0.1$  mH). Thus, the resulting efficiencies taking into account different semiconductor technologies are summarized in Table III. Where  $\eta_0$  is the efficiency without the isolation switches.

Table III  
QUANTITATIVE ANALYSES OF A 4-PORTS MTB DC-DC CONVERTER WITH ISOLATION SWITCHES (400 V, 10 kW, AND 20 kHz).

Efficiency reduction with the Isolation Switches			
Non-Resonant Converter		Resonant Converter	
Si IGBT	SiC MOSFET	Si IGBT	SiC MOSFET
$\eta_0 - 1.08 \%$	$\eta_0 - 0.46 \%$	$\eta_0 - 1.15 \%$	$\eta_0 - 0.56 \%$

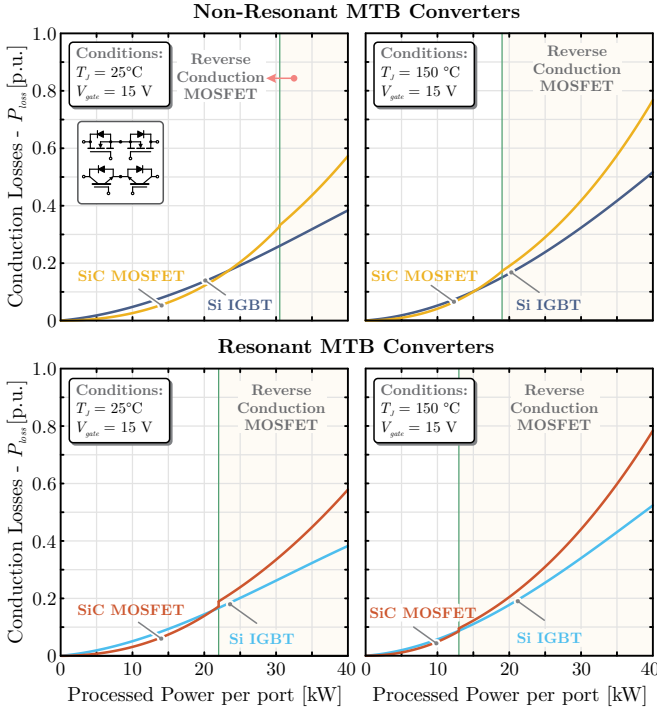


Figure 7. Normalized conduction losses of the isolation switches based on IGBTs (IKW40N120T2) and MOSFETs (C2M0025120D) for the non-resonant and resonant MTB converters. In order to evaluate fairly the devices, it is considered the same gate driver circuit and hence the same gate voltage.

### C. Reliability and Availability Assessment

As the MTB topologies are composed of several cells, with the addition of isolation switches inherent to the MWRed, the total number of employed components is increased compared to an equivalent converter based on 2WTs. In effect, this increases the probability of failures [5]–[7]). However, in contrast to the multiple 2WT-based converters, the failure of a single component does not necessarily conduct to a failure of the whole converter, since the healthy cells can still be functional in partial power flow, as previously described. Thus, minimizing the failure of those elements and mainly their impact, the overall reliability and availability can be enhanced.

Since the failure rates of the reactive network along with MWT are much lower than those of semiconductors and DC-Link capacitors, their failures are neglected [7], and any fault of capacitors and semiconductors might lead the cell to fail. As a matter of fact, it is assumed that the system is non-repairable and that the fault management is able to detect the fault, isolate it and reconfigure the system, i.e., the system has a perfect fault-management [3].

Furthermore, the cells which compose the DC-DC converters are considered identical and with a failure rate equal to  $\lambda_{cell}$  (i.e.  $\lambda_{cell,MWT} = \lambda_{cell,2WT}$ ), so that  $MTTR_{syst}$  is the same for all cells. Thus, in order to evaluate the availability, the  $MTTF_{syst}$  for the entire system with  $N_{cells}$  based on MWT and 2WT can be estimated by (22) and (23), respectively.

$$MTTF_{syst,MWT} = \frac{1}{2N_{cells}(\lambda_{cell} + \lambda_{iso})} \quad (22)$$

$$MTTF_{syst,2WT} = \frac{1}{4N_{cells}\lambda_{cell}} \quad (23)$$

Where,  $\lambda_{iso}$  is the failure rate of the additional isolation switches used in the MWT redundancy approach. Since the failures rates  $\lambda_{cell}$  and  $\lambda_{iso}$  are proportional to thermal cycle and hence the processed power by the MTB converter, it is possible to assume that  $\lambda_{cell} \propto k_{iso}\lambda_{iso}$ , so that  $k_{iso}$  can be defined according to  $k_{iso} = \lambda_{cell}/\lambda_{iso}$ , as shown in Figure 8.

For instance, considering the application illustrated in Figure 4 for sake of comparison, a fault in the 2WT-based converter can affect two cells at once. This happens because the 2WTs are not coupled, and thus the power cannot be routed among the other healthy cells in this kind of system. As a result,  $MTTF_{syst,MWT}$  is higher than  $MTTF_{syst,2WT}$ , affording an increase of the time before a failure in 50 % and an improvement of the availability, since the converter can maintain the operation, even without some of the cells.

In order to take advantage of the standby redundancy, (22) and (23) can be rewritten in terms of number of standby redundant cells  $N_{red,stab}$ ; as defined by (24).

$$MTTF_{syst,red} = \begin{cases} (1 + N_{red,stab}^{MWT})MTTF_{syst,MWT} \\ (1 + N_{red,stab}^{2WT})MTTF_{syst,2WT} \end{cases} \quad (24)$$

Hence, rearranging (24), the required number of redundant cell for MTB converters  $N_{red,stab}^{MWT}$  can be expressed in term of the required redundant cells for the 2WT-based converters

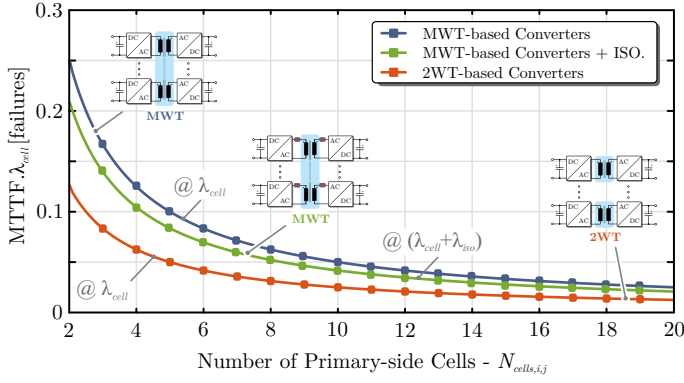


Figure 8. Failure behavior of the DC-DC converters, considering the isolation switches (whereas  $k_{iso} = 0.2$ ), according to MIL-HDBK-217F.

$N_{red, stb}^{2WT}$ , cf. (25). As can be noted, for  $k_{iso} < 1$ , the MTB converters require less standby redundant cells when compared to 2WT-based converters.

$$N_{red, stb}^{MWT} = \frac{N_{red, stb}^{2WT}(1 + k_{iso}) - (1 - k_{iso})}{2} \quad (25)$$

Therefore, the MWRed approach can extend the availability of system at same time that the redundant cells are reduced, instead of a standby cell for each port as demanded by the 2WT-based converters.

#### IV. IMPLEMENTATION AND EXPERIMENTAL VALIDATION OF THE MULTIWINDING REDUNDANCY APPROACH

In order to verify the performance of the proposed fault-tolerant approach based on the MWT, a prototype of a symmetrical QAB (SQAB) converter was built and experimental results were obtained, cf. Figure 9 (a). To evaluate dynamically the performance of the converter under fault, cf. Figure 9 (b), a short-circuit on the cell 2 was emulated by software, cf. [3].

Figure 10 presents the main waveforms of the SQAB converter operating dynamically before and after a fault at the cell 2, cf. Figure 10. The dynamic behavior during the fault at the cell 2 is depicted in Figure 10 (a), demonstrating that the converter maintains operational after the failure and the immediate disconnection of the faulty cell (through the isolation switches), cf. Figure 10 (b). As can be noted, while the cell 2 is not reconnected to the system, cell 1 processes more power to compensate the absence of cell 2, keeping the partial power flow (nearly the rated power), cf. Figure 10 (c). After the fault, the system verifies if the fault was cleared and then if the isolated-cell remains healthy to be reconnected to the converter, cf. Figure 10 (d). Otherwise, it is reconfigured to partial load mode: the faulty cell remains disconnected and the power flow is adjusted for the resulting topology, as illustrated in Figure 11. In that case, it is emulated that the cell is injured after the fault and therefore the system have to reconfigure itself to keep the operation.

As can be noted in Figure 11, the DC-DC converter behaves as an SQAB before the faults, as an TAB after the fault at cell 1 and like an DAB after the fault at cell 3. The experimental waveforms emphasize the dynamic behavior of the converter

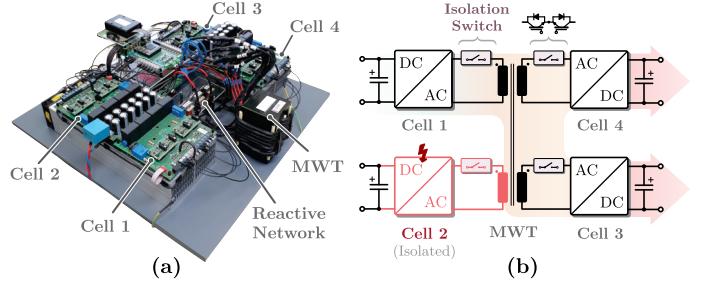


Figure 9. (a) Hardware prototype of the SQAB converter. (b) Power flow on the SQAB considering a fault at the cell 2 [8].

considering one fault in two cells (one in primary side and another in the secondary side). After the reconnection of the isolated cell fails, the system adjust the power flow on the resulting converter. The operation intervals are divided in five states: I; II; III; IV and V. For each interval is presented the equivalent resulting DC-DC converter and its power flow.

#### V. CONCLUSIONS

The paper has presented and assessed the MWRed in MTB converters for safety-critical applications. The described fault-tolerant approach aims at the continuous operation of the MTB DC-DC converter by leveraging the magnetic coupling among the cells. Thus, in case of a fault, the power might be effectively routed among the healthy cells without affecting the operation of the converter. For this purpose, isolation switches are used to reconfigure it, disconnecting the faulty cell.

The main advantages of the fault-tolerance concept are post-fault operation (at either partial or rated power), simple implementation and integration to an existing system, reduced number of additional components (one bidirectional switch per port), no significant efficiency deterioration considering the enhanced fault-tolerant feature (around 1.0 % for IGBTs and 0.5 % for MOSFETs), and reduced number of standby redundant cells (up to 50 %). As a weak point, the cells have to be oversized for ensuring the continuous operation at rated power during a faulty condition, since the number of healthy cells is reduced if standby redundancies are not considered.

Finally, a fault-tolerant SQAB converter embedded with the isolation switches has been evaluated and experimental results were also presented to validate the effectiveness of the MWRed approach in different scenarios.

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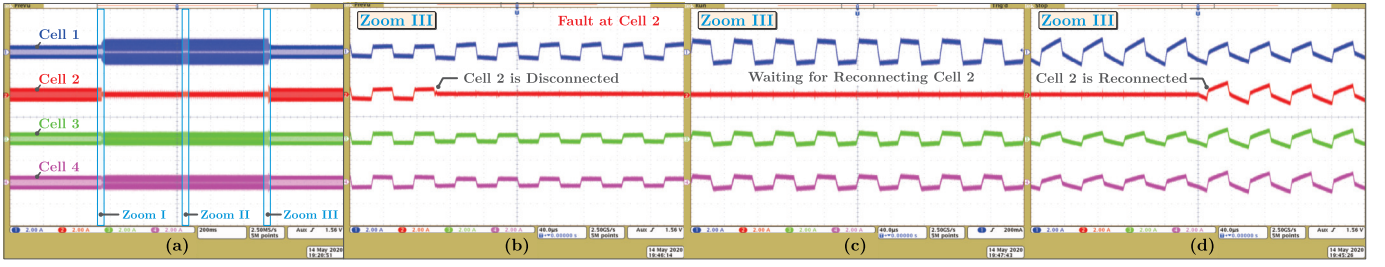


Figure 10. Experimental results of the SQAB under a fault at the Cell 2: (a) dynamic behavior of the SQAB converter before, during and after the fault; (b) highlighting the disconnection of the cell 2 when the fault is detected; (c) partial operation after the disconnection of the cell 2; and (d) when the cell 2 is reinserted to the system and the total power flow is reestablished [8].

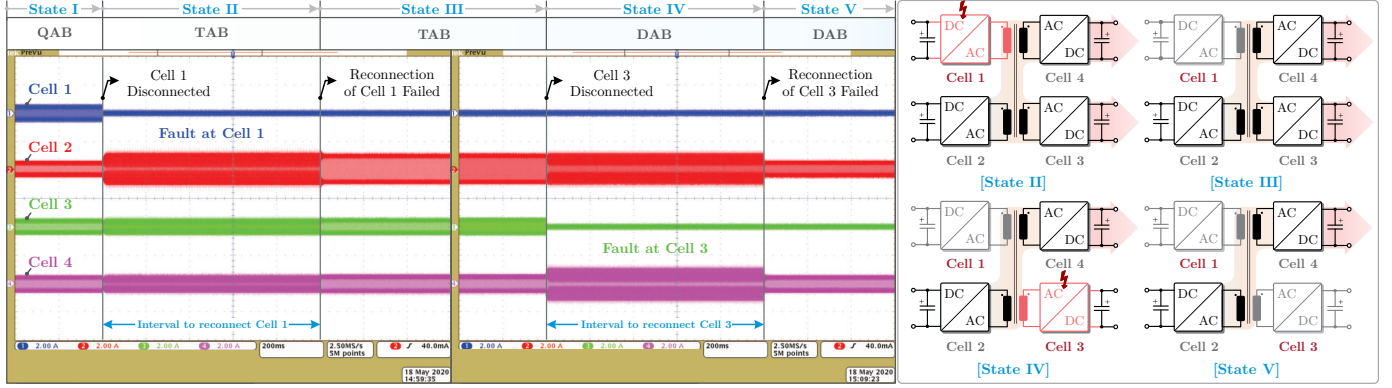


Figure 11. Experimental results of the SQAB under a fault at the cell 1 and cell 3 and the posterior reconfiguration to the resulting DC-DC converter: after the cell 1 be disconnected, the SQAB is reconfigured to a TAB and then when the cell 3 is disconnected the converter is reconfigured to a DAB.

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