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Space Vector Modulation Technique for Reducing Harmonics in Current with Zero Common-Mode Voltage for Two-Parallel Three-Level Converters

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Abstract— A zero common-mode voltage (ZCMV) modulation has the advantage of reducing electromagnetic interference (EMI) and a feature that hardly generates a zero-sequence circulating current (ZSCC) in converters operating in parallel. However, this modulation has a critical issue related to the increase in harmonics in the phase current due to the limitation of using voltage vectors generating ZCMV. Thus, this paper proposes an optimal space vector modulation (SVM) technique for two-parallel three-level converters to reduce the harmonics increased by using the ZCMV PWM. The creation of virtual voltage vectors (VVs) using vector synthesis based on the ZCMV PWM is addressed. Accordingly, new small regions in each sector of the SVM are defined in consideration with the nearest three voltage vectors, including the virtual vectors. In addition, PWM sequences for each region and dwell time for each voltage vector are also determined. Optimal vector utilization of the proposed ZCMV SVM can further reduce the current harmonics. The performance comparison between the proposed ZCMV SVM and existing methods are presented in simulation and experimental results.

Keywords—Parallel converters, zero-sequence circulating current (ZSCC), common-mode voltage (CMV), space vector modulation (SVM).

I. INTRODUCTION

Parallel operation of power converters is preferred in high-power systems due to power capacity scalability and easy maintenance [1]. In addition to these advantages, parallel converters can achieve better harmonics in the phase current by using interleaved modulations that are phase shifts of PWM in each parallel-connected converter [2]. On the other hand, the parallel operation concerns a zero-sequence circulating current (ZSCC) flowing through parallel-connected converters [3]–[7]. Since the ZSCC makes additional losses and reduces the reliability of the converters, this current should be suppressed even though the ZSCC does not affect the phase current output by the entire converter system.

As described in several papers, ZSCC is caused by the difference in common-mode voltages (CMVs), known as the main cause of conducted EMI generated by PWM converters [8]. The ZSCC consists of low- and high-frequency components, LF-ZSCC and HF-ZSCC. In general, LF-ZSCC can be suppressed by using an appropriate controller [4], [5], and HF-ZSCC can be reduced by applying modified modulations [6], [7]. However, the ZSCC generation is inevitable as long as the CMV occurs in the converters. For this reason, the application of the zero CMV (ZCMV) PWM

methods, [9] and [10], to each parallel-connected converter is effective in eliminating the ZSCC. In the case of the ZCMV modulation, however, the harmonics in the phase current deteriorate due to the limitation of using voltage vectors far from a reference voltage vector.

Among recent studies on the modulation for parallel converters, space vector modulation (SVM) techniques utilizing virtual voltage vectors (VVs) are proposed in [11] and [12] for two- and three-level converters, respectively. In [11], additional VVs between two vectors used in each two-level converter are defined. These additional vectors are the same as the small- and medium vectors used in the three-level converter so that this modulation shows similar results to the three-level converter. Similarly, the two-parallel three-level converter with the SVM using the VVs can be performed like five-level converters [12]. These SVMs for two-parallel converters can further decrease harmonics in the phase current than the interleaved modulations. Because these SVMs utilize only three nearest voltage vectors, including VVs. On the other hand, interleaved modulations tend to utilize three or more voltage vectors to make the reference voltage vector. Despite these advantages of SVMs using VVs, concerns about ZSCC remain because each converter generates CMV.

Similar to these SVMs for parallel converters, this paper proposes a novel SVM technique based on the ZCMV PWM to reduce the harmonics included in the phase current for a two-parallel three-level converter. Since each parallel-connected converter uses the ZCMV PWM, it is possible to eliminate ZSCC at both high- and low-frequency and reduce the conducted EMI. Additional twelve VVs, which are placed between zero- and medium-voltage vectors used in the ZCMV PWM, are defined in the proposed modulation. Based on the SVM using the nearest three voltage vectors, each sector on a space vector diagram of the ZCMV PWM can be divided into new four regions, and dwell times for the voltage vectors in each region are described. Furthermore, one of the new regions can be divided into two sub-regions, considering the symmetry of the PWM sequence and the switching loss. Consequently, the proposed SVM has a total of five PWM sequences in each sector. In simulation and experimental results, CMV and ZSCC reduction of the proposed ZCMV SVM is validated, and the THD comparison of modulations is performed.

This paper is organized as follows. In section II, ZSCC caused in the two parallel-connected PWM converters and existing ZCMV modulations are described. In Section III, existing SVM based on virtual voltage vectors is introduced

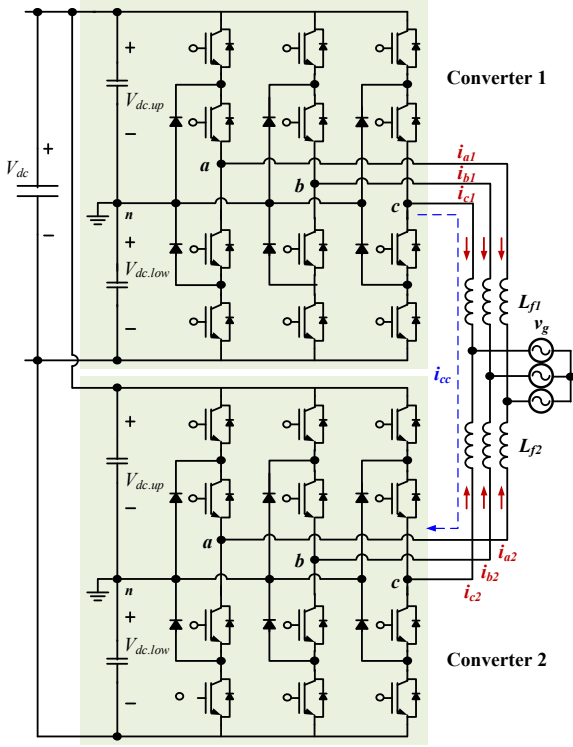


Fig. 1. Grid-connected two-parallel three-phase three-level PWM DC-AC converter.

first. And then, VVVs used in the proposed ZCMV SVM and new regions in each sector are defined considering VVVs. The dwell time for three voltage vectors is derived for each region, and five PWM sequences are proposed. Section IV presents simulation and experimental results to compare existing modulations in terms of CMV, ZSCC and current harmonics.

II. ZERO-SEQUENCE CIRCULATING CURRENT IN PARALLEL CONVERTERS

Fig. 1 shows a two-parallel three-phase three-level neutral-point-clamped (NPC) converter. Two converters share the same dc voltage source (v_{dc}), and each phase of the converters is connected to the corresponding ac grid (v_g) through harmonic filters (L_{fx} , $x=1, 2$). In general, the parallel connection of converters is known as a structure that easily increases the power capacity of the entire converter system. Moreover, it is possible to reduce the harmonics in the output phase current using the interleaved modulation, and modularization of each converter has advantages in terms of management and maintenance.

A. Zero-Sequence Circulating Current

However, parallel converters have a problem that a zero-sequence circulating current (ZSCC) flows between the converters. This ZSCC must be suppressed because it causes problems such as additional loss and weakened system reliability. The ZSCC (i_{cc}) flowing through each converter is represented with the sum of the three-phase current (i_{abx}) as expressed in (1). This current can be classified into low- and high-frequency ZSCC (LF-ZSCC and HF-ZSCC).

$$i_{cc} = \frac{i_{a1} + i_{b1} + i_{c1}}{3} = -\frac{i_{a2} + i_{b2} + i_{c2}}{3} \quad (1)$$

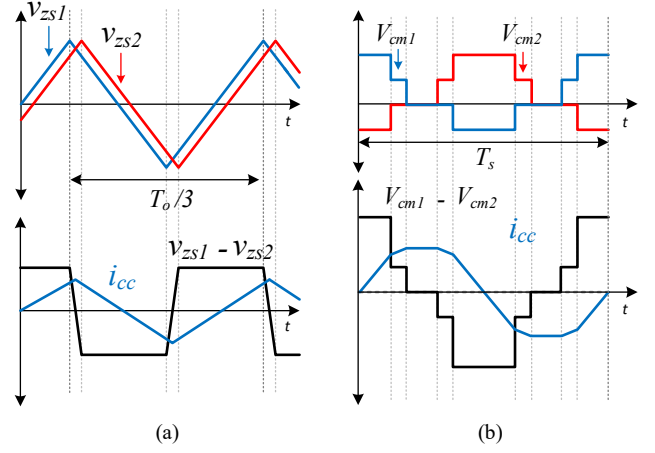


Fig. 2. Two types of ZSCC in parallel converters. (a) LF-ZSCC, (b) HF-ZSCC (Interleaved modulation).

It is known that the ZSCC is caused by the common-mode voltage (CMV, $v_{cm,x}$) difference output by each parallel-connected converter, as given in (2).

$$i_{cc} = \frac{1}{L_{f1} + L_{f2}} \int (v_{cm,1} - v_{cm,2}) dt \quad (2)$$

The CMV can be presented as the sum of three-phase voltage outputs from each converter, like ZSCC and defined as (3).

$$v_{cm,x} = \frac{v_{an,x} + v_{bn,x} + v_{cn,x}}{3} \quad (3)$$

The LF-ZSCC is generated by the difference in the zero-sequence voltage, $v_{zs,x}$, the CMV at a fundamental operating frequency ($f_o = 1/T_o$) or three times, as shown in Fig. 2(a). In general, this type of ZSCC can be suppressed with a controller based on a P or PR controller [4]. In the case of the HF-ZSCC, the difference in the discrete CMV ($V_{cm,x}$), which changes for one period of PWM, generates the ZSCC, as shown in Fig. 2(b). The HF-ZSCC cannot be suppressed by using a controller. Because the HF-ZSCC is related to the switching frequency, the bandwidth is relatively too low to use the controller for suppressing LF-ZSCC. Therefore, it is possible to reduce the HF-ZSCC only by increasing the size of the filter or by modifying the modulation [6], [7].

B. Zero Common-Mode Voltage Modulation

From the description in a previous section, if each converter does not generate any CMV, it is expected that neither type of ZSCCs flows inside the parallel converter system. A way to satisfy this condition is to use zero CMV (ZCMV) modulations for each parallel-connected converter.

The ZCMV PWM methods can be applied to multilevel converters, utilizing more voltage vectors than conventional two-level converters. These modulations have been proposed to reduce conducted EMI emitted by PWM converters. For example, as shown in Table I, six medium voltage vectors (e.g. [PON] and [PNO]) and zero voltage vector [OOO] do not generate CMV. Thus, ZCMV modulations do not generate the CMV due to the synthesis of a reference voltage vector (V_{ref}^*) using voltage vectors ([OOO], [PNO] and [PON]). According to the symmetry of the PWM sequence,

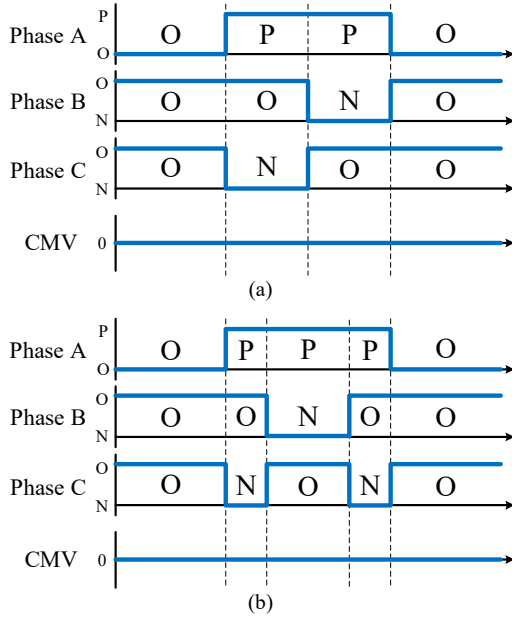


Fig. 3. PWM sequence and output CMV of ZCMV modulations. (a) Asymmetric [9] (b) Symmetric [10].

TABLE I. VOLTAGE VECTORS AND CMV OF THREE-PHASE THREE-LEVEL CONVERTERS

	Switching states	CMV	Magnitude
Zero Vector (V_0)	[PPP]	$V_{dc}/2$	$0V$
	[OOO]	$0V$	
	[NNN]	$-V_{dc}/2$	
Small Vector ($V_1 \sim V_6$)	[POO],[OPO],[OOP]	$V_{dc}/6$	$V_{dc}/3$
	[PPO],[POP],[OPP]	$V_{dc}/3$	
	[ONN],[NON],[NNO]	$-V_{dc}/3$	
	[NOO],[ONO],[OON]	$-V_{dc}/6$	
Medium Vector ($V_7 \sim V_{12}$)	[PON],[OPN],[NPO] [NOP],[ONP],[PNO]	$0V$	$\sqrt{3} V_{dc}/3$
Large Vector ($V_{13} \sim V_{18}$)	[PPN],[PNP],[NPP]	$V_{dc}/6$	$2V_{dc}/3$
	[PNN],[NPN],[NNP]	$-V_{dc}/6$	

there are two representative ZCMV modulations, as shown in Fig. 4. An asymmetric ZCMV modulation [9] in Fig. 3(a) is easy to compensate dead-time effects, but it has slightly more harmonics included in the current than symmetric ZCMV PWM [10] in Fig. 3(b).

Although these ZCMV modulations can be applied to the parallel converter to solve the problems of ZSCC and EMI emission, there is a limit in that the harmonics of the output phase current increase considerably, even if the interleaved modulation is implemented. Because the ZCMV modulations utilize voltage vectors that are relatively farther from the reference voltage vector than the general SVM [13] shown in Fig. 4.

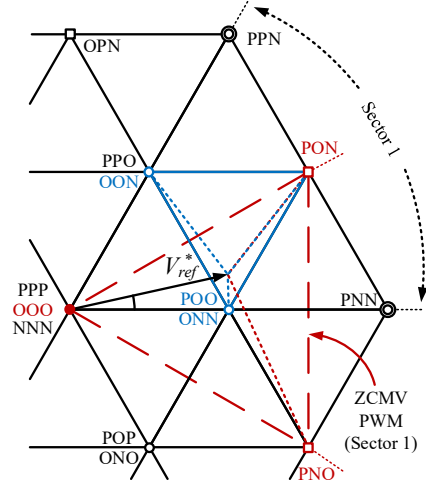


Fig. 4. Generation of reference voltage vector using nearest three voltage vectors in three-level converters with normal SVM and ZCMV PWM.

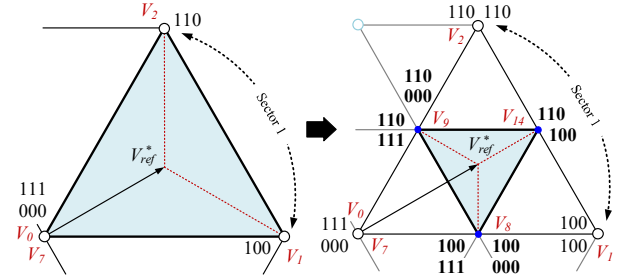


Fig. 5. Virtual voltage vector-based space vector modulation for two-parallel two-level PWM converters.

III. PROPOSED SVM BASED ON ZCMV PWM

A. Existing SVMs for two-parallel converter

One of the advantages of the parallel operation of converters is the reduction of phase current harmonics using the interleaved modulation, which can be implemented simply by making a phase difference to PWM signals input to each parallel-connected converter.

Recently, a new space vector modulation (SVM) using virtual voltage vectors (VVVs) has been proposed for two-parallel PWM converters [11], [12]. The VVVs are placed between two voltage vectors output by each parallel-connected converter, and new regions on a space vector diagram can be defined with these additional vectors. For example, as shown in Fig. 5, when voltage vectors of [000] and [100] in sector 1 are output by a two-parallel two-level converter, these vectors can create a new VVV, V_8 , at the midpoint between the two vectors. In the same way, two more VVVs can be defined, and Sector 1 can be divided into four regions considering three additional vectors. Since the reference voltage vector can be generated with SVM using the nearest three voltage vectors, V_8 , V_9 and V_0 , a better phase current is expected than the interleaved modulation, which utilizes not only the three nearest voltage vectors but also other vectors. However, there are still concerns about the ZSCC, which is an inherent feature of the parallel converters.

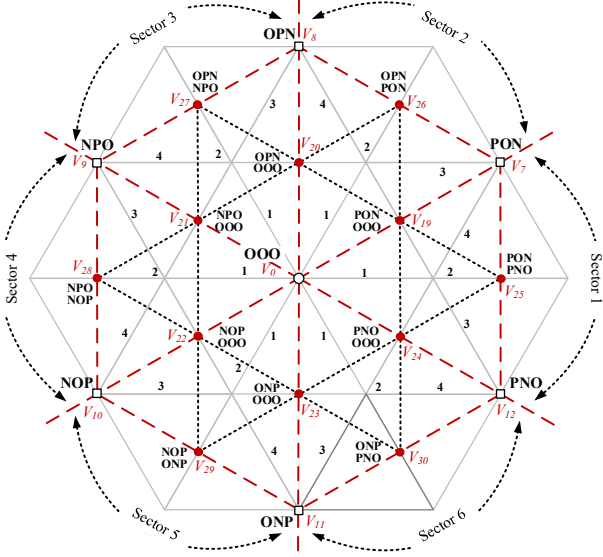


Fig. 6. Space vector diagram of the proposed SVM based on ZCMV PWM for two-parallel three-level converters.

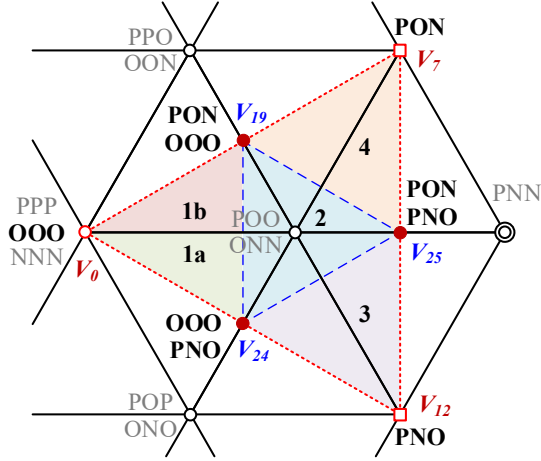


Fig. 7. Regions in Sector 1 of the proposed ZCMV SVM.

B. Proposed SVM based on ZCMV PWM

The proposed SVM for two-parallel three-level converters is based on the ZCMV PWM and utilizes twelve virtual voltage vectors in addition to seven voltage vectors used for the ZCMV PWM. As shown in Fig. 6, six voltage vectors ($V_{19} \sim V_{24}$) of $\sqrt{3}V_{dc}/6$ can be defined at the midpoint between zero and medium vectors. In addition, the other six voltage vectors of $V_{dc}/2$ can be defined between two medium vectors. Fig. 7 shows the space vector diagram of the proposed modulation in Sector 1 as an example. Since only medium voltage vectors and zero vector [OOO] can be used to make the reference voltage vector (V_{ref}^*) for the ZCMV, three additional virtual voltage vectors, V_{19} , V_{24} and V_{25} , can be defined. For example, if one converter generates V_0 , [OOO], and another converter produces V_7 , [PON], a new voltage vector, V_{19} , corresponding to the midpoint between two vectors, can be applied to the load. Other new vectors, V_{24} and V_{25} , can be obtained in the same way. Six voltage vectors in Sector 1, including new vectors, are presented in Table II. These virtual voltage vectors are redundant because

TABLE II. VOLTAGE VECTORS OF PROPOSED SVM IN SECTOR 1

Symbol	Switching states	Magnitude and phase
	Converter 1- Converter 2	
V_0	[OOO] - [OOO]	0V
V_7	[PON] - [PON]	$\frac{\sqrt{3}}{3} V_{dc} e^{j\pi/6}$
V_{12}	[PNO] - [PNO]	$\frac{\sqrt{3}}{3} V_{dc} e^{-j\pi/6}$
V_{19}	[PON] - [OOO] [OOO] - [PON]	$\frac{\sqrt{3}}{6} V_{dc} e^{j\pi/6}$
V_{24}	[PNO] - [OOO] [OOO] - [PNO]	$\frac{\sqrt{3}}{6} V_{dc} e^{-j\pi/6}$
V_{25}	[PNO] - [PON] [PON] - [PNO]	$\frac{1}{2} V_{dc} e^{-j0}$

there are two ways of generating the vector depending on the vectors output by the two converters (e.g. V_{25} , [PON]-[PNO] or [PNO]-[PON]).

Considering the SVM using the nearest three vectors, each sector can be divided into four regions using six voltage vectors. For example, in Region 1 of Sector 1 ($-\pi/6 < \theta \leq \pi/6$), three voltage vectors used for SMV are V_0 , V_{19} and V_{24} , and they can be used to make the reference voltage vector as given in (4).

$$V_{ref}^* T_s = V_{24} T_a + V_{19} T_b + V_0 T_c \quad (4)$$

$$T_s = T_a + T_b + T_c \quad (5)$$

Where T_a , T_b and T_c are dwell times for corresponding voltage vectors, and their sum is equal to T_s , which is one period of PWM.

By substituting voltage vectors in Table II into (4), an equation for the reference voltage vector in Region 1 of Sector 1 can be obtained as (6).

$$V_m e^{j\theta} T_s = \frac{\sqrt{3}}{6} e^{-j\frac{\pi}{6}} T_a + \frac{\sqrt{3}}{6} e^{j\frac{\pi}{6}} T_b \quad (6)$$

Where V_m is the magnitude of the reference voltage vector.

This voltage vector can be derived into (7) using Euler's formula.

$$\begin{aligned} & V_m T_s (\cos \theta + j \sin \theta) \\ &= \frac{\sqrt{3}}{6} V_{dc} T_a \left\{ \cos\left(-\frac{\pi}{6}\right) + j \sin\left(-\frac{\pi}{6}\right) \right\} \\ &+ \frac{\sqrt{3}}{6} V_{dc} T_b \left\{ \cos\left(\frac{\pi}{6}\right) + j \sin\left(\frac{\pi}{6}\right) \right\} \end{aligned} \quad (7)$$

Real and imaginary axis terms of (7) are given as follows:

$$\begin{cases} \text{Re:} & T_a + T_b = \frac{4V_m T_s}{V_{dc}} \cos \theta \\ \text{Im:} & -T_a + T_b = \frac{4\sqrt{3}V_m T_s}{V_{dc}} \sin \theta \end{cases} \quad (8)$$

TABLE III. DWELL TIMES FOR VOLTAGE VECTORS IN SECTOR 1

Region	Vectors	Dwell time
1	$V_{24} (T_a)$	$T_a = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} - \theta)$
	$V_{19} (T_b)$	$T_b = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} + \theta)$
	$V_0 (T_c)$	$T_c = T_s - \frac{4V_m T_s}{V_{dc}} \cos \theta$
2	$V_{24} (T_a)$	$T_a = T_s - \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} + \theta)$
	$V_{19} (T_b)$	$T_b = T_s - \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} - \theta)$
	$V_{25} (T_c)$	$T_c = \frac{4V_m T_s}{V_{dc}} \cos \theta - T_s$
3	$V_{24} (T_a)$	$T_a = 2T_s - \frac{4V_m T_s}{V_{dc}} \cos \theta$
	$V_{12} (T_b)$	$T_b = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} - \theta) - T_s$
	$V_{25} (T_c)$	$T_c = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} + \theta)$
4	$V_{19} (T_a)$	$T_a = 2T_s - \frac{4V_m T_s}{V_{dc}} \cos \theta$
	$V_7 (T_b)$	$T_b = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} + \theta) - T_s$
	$V_{25} (T_c)$	$T_c = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} - \theta)$

By solving simultaneous equations in (8), three dwell times for three voltage vectors can be obtained in (9)-(11).

$$T_a = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} - \theta) \quad (9)$$

$$T_b = \frac{4V_m T_s}{V_{dc}} \sin(\frac{\pi}{6} + \theta) \quad (10)$$

$$T_c = T_s - \frac{4V_m T_s}{V_{dc}} \cos \theta \quad (11)$$

In this way, the dwell times for the voltage vectors of four regions in Sector 1 are presented in Table III.

ZCMV SVM proposed in this paper is constructed considering the symmetry of the PWM sequence, the minimization of switching losses and the convenience of implementation.

Measuring the average current during one PWM cycle is essential for desired performance of a current controller. The average current can be sampled more simply with the symmetric PWM sequence than with the asymmetric sequence. Therefore, the proposed ZCMV SVM is based on the symmetric ZCMV PWM of Fig. 4(a) proposed in [10].

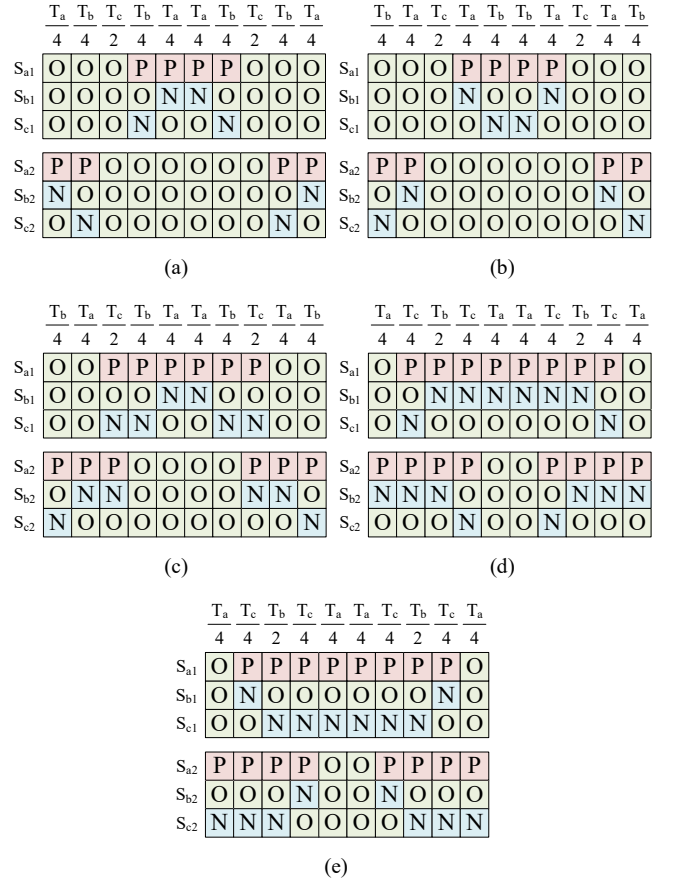


Fig. 8. PWM sequences in Sector 1 of the proposed SVM. (a) Region 1a. (b) Region 1b. (c) Region 2. (d) Region 3. (e) Region 4.

As shown in Fig. 3(b), the PWM pattern of phase C is divided around the center of the sequence. That is why there are two times of turn-on and turn-off switching, and it makes additional losses compared to other phases. Therefore, the PWM sequences in Region 1 are configured in Fig. 8(a) and (b) to minimize the switching loss and balance the loss between the phases. For instance, the C-phase PWM pattern is divided in Region 1a, as shown in Fig. 8(a), since the magnitude of the phase C current is the smallest among three-phase currents. In Region 1b, on the other hand, the B-phase PWM pattern is split, as shown in Fig. 8(b), because the magnitude of the phase B current is the smallest. This principle is also considered when PWM sequences in regions 3 and 4 are constructed. It results that the C-phase pattern in Region 3 and B-phase pattern in Region 4 are divided, respectively, as shown in Fig. 8(d) and (e). The PWM sequences in Region 2 is different from other regions. The sequences of two converters in other regions are symmetrical in consideration with a 180° phase shift. Nevertheless, the two sequences in Region 2 are not the same because the proposed ZCMV SVM uses three nearest voltage vectors.

For this reason, the phase in which the pattern division occurs in the PWM sequence of the two converters is different. When the phase angle (θ) is between $-\pi/6$ and 0, the switching loss occurs in phase B of the converter '2' is larger than the phase C of the converter '1'. On the other hand, the loss in phase B is smaller than the phase C in another area in Region 2 ($0 < \theta \leq \pi/6$). As a result, the loss that occurs in phases B and C can be balanced.

TABLE IV. SIMULATION CONDITIONS

Parameters	Value
Grid line-to-line voltage	400 [Vrms]
Inductance of filter	0.5 [mH]
Fundamental operating frequency	50 [Hz]
Switching frequency	10 [kHz]
Dead time	2 [μ s]

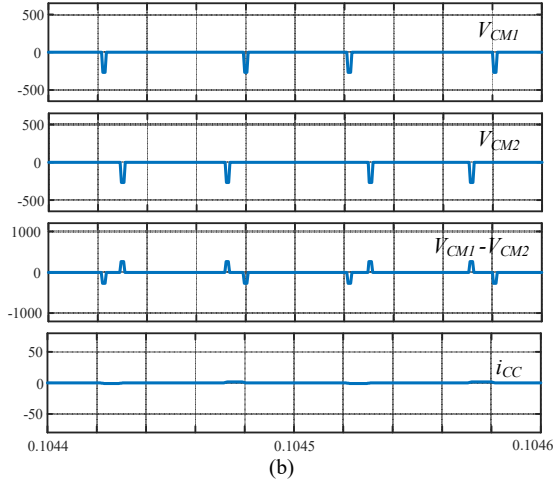
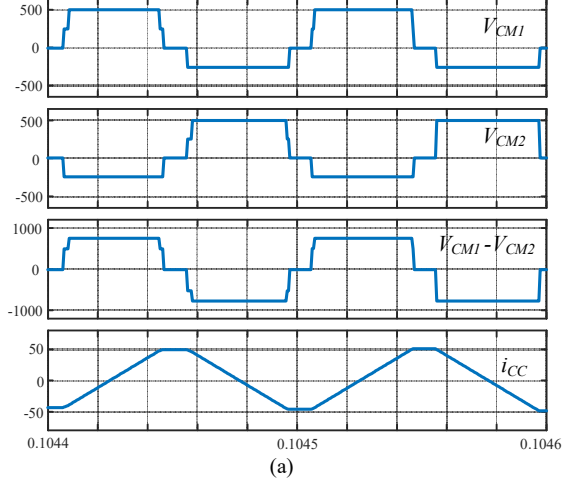


Fig. 9. CMV of two converters, CMV difference and ZSCC (a) Interleaved normal SVM. (b) Proposed ZCMV SVM.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation results

Simulation is conducted to validate the performance of the proposed SVM. A grid-connected two-parallel three-level NPC DC/AC converter in Fig. 1 is used with conditions as shown in Table IV.

Fig. 9(a) shows simulation results about CMV output by each converter, CMV difference between two converters and ZSCC when the 180° interleaved general SVM is used for two converters. Under the dc voltage of 1500V, CMV occurs up to 500V ($V_{dc}/3$), and the amplitude of the CMV difference is about 750V. This voltage difference causes the ZSCC

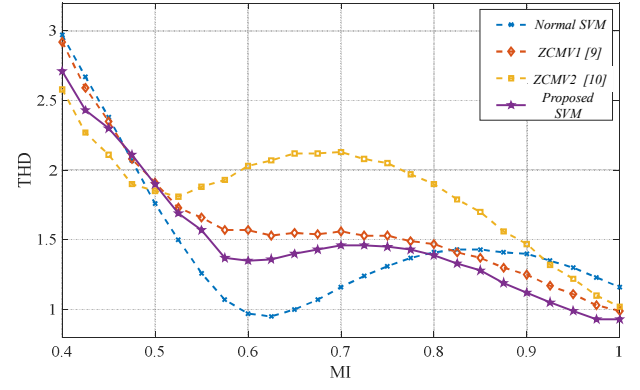


Fig. 10. THD comparison results according to MI.

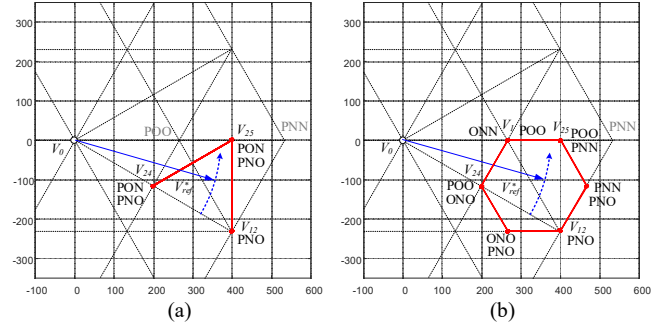


Fig. 11. Voltage vectors used in Region 3 of Sector 1. (a) Proposed ZCMV SVM. (b) Interleaved normal SVM.

ripple corresponding to the switching frequency, and its amplitude is about 50A. This ZSCC ripple deteriorates the reliability of the converter, especially dc capacitors. On the other hand, as shown in Fig. 9(b), the parallel converter to which the proposed SVM is applied generates little CMV compared to the results in Fig. 9(a). Even though CMV is caused twice during one period (100 μ s) due to the dead time, this CMV hardly affects the ZSCC. If the compensation for the dead time is applied, almost zero CMV can be achieved.

Fig. 10 presents THD comparison results of three existing modulations based on 180° Interleaving and the proposed SVM according to the modulation index (MI) from 0.4 to 1. Comparing results of ZCMV modulations, the proposed ZCMV SVM shows better results over 0.5 MI. In particular, when MI is 0.6, the measured THD of the proposed SVM is about 0.22% and 0.68% smaller than those of the existing two methods, respectively. Furthermore, the proposed modulation shows the best results when MI is more than 0.8.

In order to find the reason that the proposed SVM is better than the result of the interleaved general SVM, additional simulation is conducted to check the voltage vectors used by both modulations, as shown in Fig. 11. When the reference voltage vector passes Region 3 of Sector 1, the proposed ZCMV SVM uses three voltage vectors, V_{12} , V_{24} and V_{25} . Under the same condition, however, the general SVM uses four voltage vectors (e.g. V_1 , V_{24} , V_{12} and a vector [ONO]-[PNO]), and these vectors are not close to V_{ref}^* enough to reduce the harmonics in the current. From this result, it can be deduced that SVMs based on the optimal voltage vector utilization, including the

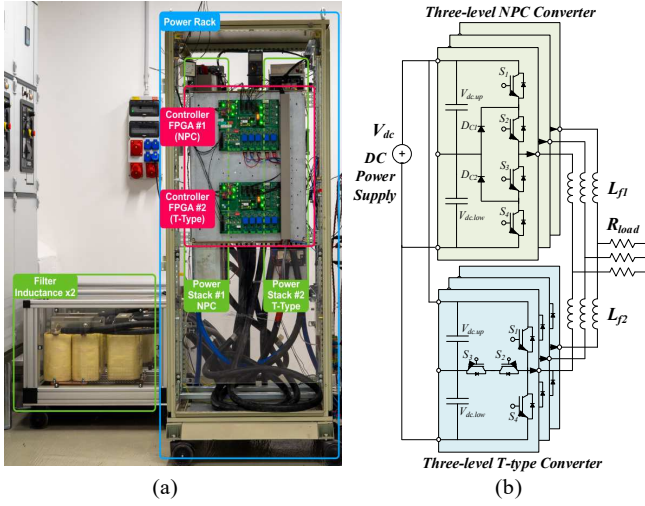


Fig. 12. Experimental setup. (a) Two-parallel three-level converter setup. (b) Circuit configuration for experiment.

TABLE V. EXPERIMENTAL CONDITIONS

Parameters	Value
Resistance load	10 [Ω]
Inductance of filter	2.1 [mH]
DC voltage	200 [V]
Fundamental operating frequency	50 [Hz]
Switching frequency	10 [kHz]
Dead time	2 [μ s]

virtual vectors, are effective in reducing the harmonics more than the interleaved modulations, which are simple to implement, but not optimal.

B. Experimental results

As shown in Fig. 12, three-level NPC and T-type converter setup with inductive filters are used for the experiment. And resistive loads are connected instead of the grid voltage source as depicted in Fig. 12(b). Detailed experimental conditions are presented in Table V.

Fig. 13 shows PWM sequences in Sector 1 and Regions 1a, 2 and 3, when the proposed ZCMV SVM is applied to the two parallel-connected converters. As described in Fig. 8, PWM sequences are symmetrical, and the voltage vectors which do not generate CMV are used in the PWM sequence.

In Fig 14 the 180° interleaved general SVM and the proposed ZCMV SVM are compared in terms of CMV, CMV difference and ZSCC at the switching frequency. As shown in Fig. 14(a), each converter generates CMV in a range between about $-33V$ ($-V_{dc}/6$) and $66V$ ($+V_{dc}/3$), and there is a 180° phase difference between two CMV waveforms. In addition, the magnitude of the peak to peak CMV difference is about $200V$ (V_{dc}). Due to this CMV difference, sinusoidal ZSCC is caused as expressed in (2), and its amplitude and frequency are about $1A$ and $10kHz$, equal to the switching frequency. On the other hand, in the case of the proposed SVM, it can be seen in Fig. 14(b) that the CMV is completely removed, excluding the voltage

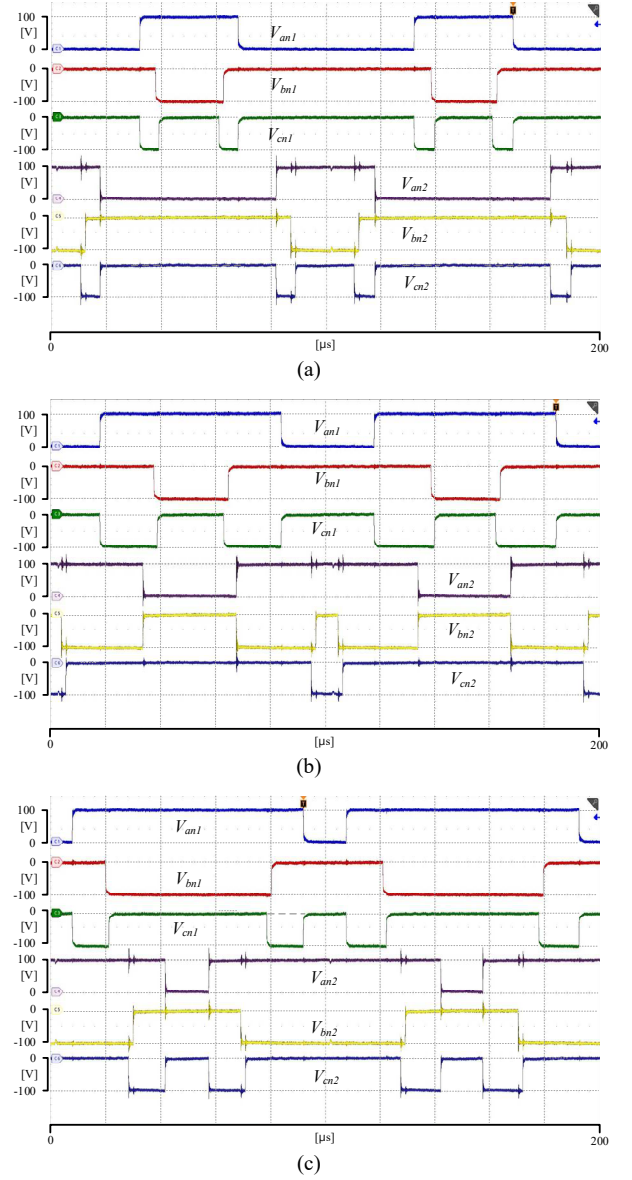


Fig. 13. Output terminal voltage of each phase in a two-parallel three-level converter with the proposed ZCMV SVM (a) Region 1a (MI = 0.35) (b) Region 2 (MI = 0.65) (c) Region 3 (MI = 0.8).

caused by the dead time. And although CMV is generated due to the dead time, this voltage is not large enough to generate ZSCC like Fig. 14(a) and ZSCC is almost 0A, excluding noise caused by the switching operation.

V. CONCLUSION

This paper proposes an optimal ZCMV SVM technique for two-parallel three-level converters to reduce the current harmonics increased by ZCMV PWM. The need for ZCMV PWM to eliminate ZSCC and the increase in current harmonics due to the ZCMV PWM are described first. For the proposed SVM, additional VVV's are created by synthesizing two voltage vectors output by two converters, and four new regions on the space vector diagram are defined. In addition, the dwell time for voltage vectors of each region are presented, and five PWM sequences in each sector are proposed considering the symmetry of the sequence and minimization of switching losses. Simulation

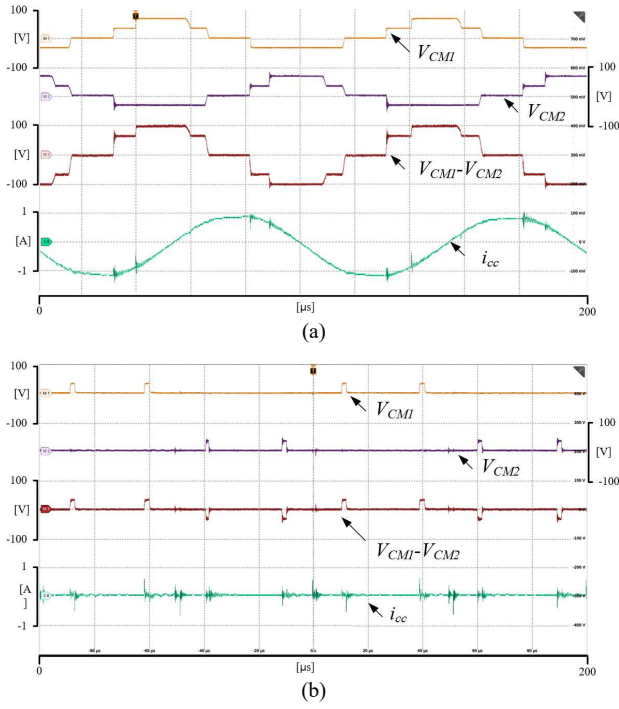


Fig. 14. Comparison results about CMV, CMV difference and ZSCC according to the modulation (a) Interleaved general SVM (b) Proposed ZCMV SVM.

and experimental results show that the proposed ZCMV SVM can eliminate CMV and ZSCC. From THD comparison results, furthermore, it is verified that the proposed SVM is at least 9.2% more effective in reducing harmonics in the phase current than methods interleaving ZCMV modulations.

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