Control Strategies for Improving Reliability and Efficiency in Modular Power Converters

Dissertation

zur Erlangung des akademischen Grades
Doktor der Ingenieurwissenschaften
(Dr.-Ing.)
Technische Fakultät
der Christian-Albrechts-Universität zu Kiel
vorgelegt von

Vivek Raveendran, M.Sc.

Kiel
2022

1. Gutachter:	Prof. Dr.-Ing. Marco Liserre
2. Gutachter:	Prof. Dr.-Ing. Timm Faulwasser
3. Gutachter:	Prof. Dr. Zoubir Khatir
Datum der mündlichen Prüfung:	30.03.2022

Erklärung

Ich erkläre an Eides statt, dass ich die Dissertation zum Thema:

Control Strategies for Improving Reliability and Efficiency in Modular Power Converters

abgesehen von der Betreuung durch Herrn Prof. Marco Liserre selbstständig und ohne Hilfe angefertigt habe und bisher weder ganz noch zum Teil an einer anderen Stelle im Rahmen eines Prüfungsverfahrens vorgelegt, veröffentlicht oder zur Veröffentlichung eingereicht habe. Weiterhin versichere ich hiermit, dass ich die vorliegende Arbeit unter Einhaltung der Regeln guter wissenschaftlicher Praxis der Deutschen Forschungsgemeinschaft angefertigt habe und alle von anderen Autoren wörtlich übernommenen Stellen wie auch die sich an die Gedankengänge anderer Autoren eng anlehnenden Ausführungen meiner Arbeit besonders gekennzeichnet und die entsprechenden Quellen angegeben sind.

Kiel, den 10. Juni 2021

Vivek Raveendran

To my father & mother

Acknowledgement

This doctoral thesis was carried out as a part of 'The Highly Efficient And Reliable smart Transformer (HEART)' project under the European Union's Seventh Framework Program (FP/2007-2013)/ERC Grant Agreement [616344]. First of all, I would like to sincerely thank my supervisor Prof. Dr.-Ing. Marco Liserre for the opportunities and guidance received during my doctoral journey. His vision and thoughts have always inspired me, and I will cherish the learning for my future ventures. I am grateful to Prof. Dr.-Ing. Timm Faulwasser and Prof. Dr. Zoubir Khatir for being part of the PhD examination committee and for their valuable contributions.

I would like to specially mention Prof. Dr.-Ing. Giampaolo Buttichi and Dr.-Ing. Markus Andresen for giving fruitful insights and guidance that helped me to stay motivated and focused amidst the challenges. My sincere gratitude to all my co-authors for their support and collaboration which helped me to strengthen the research work.

I am thankful to my colleagues and staff at the Chair of Power Electronics for their support, guidance, discussions, and friendship during my time in Kiel. I would like to thank Pramod Kumar Prasobhu, who was always there as a colleague and friend. Special thanks to Xiang Gao and Luis Juarez for our technical and non-technical conversations, and above all, friendship.

I sincerely appreciate the trust and love of my parents and brother who supported me wholeheartedly during my time abroad, without which, I could not have pursued my passion. Last but not least, I would like to thank the special person in my life who backed and trusted me at every stage of this endeavour, my wife Anagha.

Kiel, October 2022

Vivek Raveendran

Contents

Deutsche Kurzfassung der Arbeit

Die Signifikanz von modularen Stromrichtern hat in verschiedenen Anwendungen wie der elektrischen Energieverteilung, industriellen Antrieben und More Electric Aircraft (MEA) aufgrund der Vorteile wie Skalierbarkeit, Designflexibilität, höherer Fehlertoleranz und besserer Wartung drastisch zugenommen. Darüber hinaus hat der Paradigmenwechsel des Geschäftsmodells in der Leistungselektronik vom Produktlieferanten zum umfassenden Serviceanbieter die Forschung im Bereich der Zuverlässigkeitstechnik in der Leistungselektronik verstärkt. In diesem Zusammenhang haben die Herausforderungen für den zuverlässigen Betrieb modularer Stromrichter und die Lösungen zur Verbesserung ihrer Zuverlässigkeit in den letzten Jahren die notwendige Aufmerksamkeit erhalten. Wartungszyklen in modularen Systemen führen zu einem System von Stromrichterzellen mit unterschiedlicher Alterung. Ein System mit unterschiedlich gealterten Zellen birgt die Gefahr von Mehrfachwartungen, geringerer Zuverlässigkeit und Verfügbarkeit sowie hohen Wartungskosten. Um die auf thermischer Belastung basierende Alterung modularer Stromrichter zu kontrollieren, wurde eine Power-Routing Strategie vorgeschlagen. Die vorliegende Arbeit befasst sich mit den verschiedenen Implementierungsstrategien des Power Routings für modulare Stromrichter. Leistungshalbleiter sind eine der zuverlässigkeitskritischsten Komponenten in Stromrichtern, und thermische Beanspruchung - Temperatur und Temperaturwechsel - wurde als Hauptursache für deren Ausfall identifiziert. Diese Arbeit konzentriert sich auf die Algorithmen zur Verbesserung der Zuverlässigkeit von Leistungshalbleitern. Im Vergleich zu einzelnen Stromrichtern haben modulare Stromrichter eine große Anzahl von Komponenten, die aufgrund von Fertigungstoleranzen und unterschiedlichen Betriebsbedingungen mit unterschiedlichen thermischen Spannungen arbeiten. Die Auswirkung solcher Parametervariationen von Leistungshalbleitern auf die thermische Belastung und folglich auf die Lebensdauer des modularen Systems wird im Detail untersucht. Um die Lebensdauer des Systems zu verbessern, wurden auf virtuellen Widerständen basierende Power-Routing-Algorithmen für einstufige und mehrstufige modulare Architekturen durch Simulationen untersucht und mit Experimenten validiert. Basierend auf der Graphentheorie wird ein einheitlicher Rahmen für das Routing der Leistung in komplexen modularen Wandlerarchitekturen definiert. Beliebte Umrichterarchitekturen für Smart Transformer (ST) und MEA Anwendungen werden als Graphen modelliert, um als Grundlage für die Entwicklung der Leistungsflussoptimierung zu dienen. Die Wirksamkeit der Graphentheorie für die Optimierung des Leistungsflusses in modularen Systemen wird mit Hilfe von drei Algorithmen demonstriert. Der erste Algorithmus konzentriert sich auf die Verbesserung der Zuverlässigkeit des ST ohne Einschränkung der Effizienz. Der zweite Algorithmus hat das Ziel, die Wartungsplanung des ST durch Regelung des internen Leistungsflusses zu verwalten. Die Optimierung des Leistungsflusses zum Erreichen einer hohen Zuverlässigkeit für eine MEA-Anwendung wird im dritten Algorithmus untersucht. Modulationsstrategien für Stromrichter sind weit verbreitet, um ein Power-Routing auf Stromrichterebene zu erreichen. Ein fortschrittliches diskontinuierliches Modulationsschema, das für mehrstufige modulare Umrichter geeignet ist, wird diskutiert. Die Auswirkungen des Modulationsschemas auf die Lebensdauer von Stromrichterzellen in einer CHB-DAB Architektur werden durch Simulationen und Experimente validiert.

English Summary

The significance of modular power converters has escalated drastically in various applications such as electrical energy distribution, industrial motor drives and More Electric Aircraft (MEA) owing to the benefits such as scalability, design flexibility, higher degree of fault tolerance and better maintenance. Moreover, the paradigm shift of power electronics business model from product supplier to comprehensive service provider has boosted the reliability engineering research in power electronics. In this context, challenges for the reliable operation of modular power converters and the solutions for improving their reliability are getting the required attention over the past years.

One of the main advantages of modular systems is the ability to replace the faulty converter cells during maintenance instead of the entire system. However, such maintenance cycles will result in a system of converter cells with different aging. A system with cells having different aging arises the threats of multiple maintenance, lower reliability and availability, and high maintenance costs. For controlling the thermal-stress based aging of modular power converters, power routing strategy was proposed. The thesis focuses on the different implementation strategies of power routing for modular converters.

Power semiconductors are one of the most reliability critical components in power converters, and thermal-stress; temperature and thermal cycling, has been identified as the main cause of their failure. This thesis work concentrates on the power semiconductor reliability improvement algorithms. Compared to single converters, modular power converters have large number of components which operates with different thermal-stress due to manufacturing tolerances and variations in operating conditions. The impact of such parameter variations of power semiconductors on the thermal-stress and consequently the modular system lifetime is studied in detail. For improving system lifetime, virtual resistor based power routing algorithms for single stage and multi-stage modular architectures have been investigated through simulations and validated with experiment.

A unified framework for routing the power in complex modular converter architectures is defined based on graph theory. Popular converter architectures for Smart Transformer (ST) and More Electric Aircraft (MEA) applications are modeled as graphs to serve as the basis for developing power flow optimization. The effectiveness of graph theory for optimizing the power flow in modular systems is demonstrated with the help of three algorithms. First algorithm focuses on improving the reliability of ST without sacrificing the efficiency. Second algorithm has the objective of managing the maintenance scheduling of the ST by controlling the internal power flow. Power flow optimization for achieving high reliability for an MEA application is investigated in the third algorithm.

Power converter modulation strategies are widely employed for achieving power routing on converter level. An advanced discontinuous modulation scheme suitable for multi-stage modular converters is discussed. The impact of the modulation scheme on the lifetime of converter cells in a CHB-DAB architecture is validated through simulations and experiment.

General symbols

General symbols

$u(t)$	Instantaneous value

Superscripts

$*$	Reference value
th	Order

Subscripts

dc	DC-link related
d	related to diode
i	index for converter cells
sys	system level parameter
x	percentage of samples failed
exp	related to experimental result
$period$	related to the control period
η	efficiency related parameter

Special symbols

$*$	Convolution
t_r	Rise time
β	Weibull parameter
$\hat{V}_g$	Peak grid voltage
$K_{Bayerer}$	Fitted parameter in Bayerer lifetime model
α	Weibull parameter
α_v	Coefficient of virtual resistor
β_v	Exponential coefficient of virtual resistor
β_1	Fitted parameter in Bayerer lifetime model
β_2	Fitted parameter in Bayerer lifetime model
β_3	Fitted parameter in Bayerer lifetime model
β_4	Fitted parameter in Bayerer lifetime model
β_5	Fitted parameter in Bayerer lifetime model
β_6	Fitted parameter in Bayerer lifetime model
ΔT_j	Junction temperature swing

η	Efficiency factor
λ	failure rate
λ_m	Maintenance interval factor
ω	Grid frequency in radians
Ψ_G	Incidence function of graph G
ρ	Reliability factor
θ	Angular displacement between voltage and current
$A(G)$	Adjacency matrix of graph G
a_1	Fitted parameter in lifetime model
a_2	Fitted parameter in lifetime model
a_3	Constant parameter in lifetime model
B_x	B_x lifetime
C	Thermal Capacitance
C_{dc}	Cell DC-link capacitance
D	Accumulated damage
D_{bond}	Diameter of bond wire of the power semiconductor device
d_{diode}	Duty cycle of anti-parallel diode
d_{IGBT}	Duty cycle of IGBT
$D_{ini,i}$	Initial accumulated damage
D_{old}	Total accumulated damage till last sample
D_{period}	Damage accumulated during current period
di	Change in current
dt	Change in time
dv	Change in voltage
$E(G)$	Edges of graph G
E_{off}	Turn-off energy of IGBT
E_{on}	Turn-on energy of IGBT
E_{rec}	Diode recovery energy
$E_{sw,igbt}$	Switching energy loss of IGBT for one switching instance
$F(t)$	Unreliability at time t
$f_{sw,DAB}$	Switching frequency of DAB
f_{sw}	Switching frequency of power converter
g_m	Transconductance
$I(G)$	Incidence matrix of graph G
i_{device}	Current flowing through device under consideration
$I_{rated,sys}$	Rated current of the modular converter system
i_c	Collector current of IGBT
i_f	Diode forward current
$K_{p,bal}$	Proportional constant of PI controller
K_r	Resonant controller gain
kA	kiloampere
kV	kilovolt
$L_{i,j}$	Edge connecting nodes i and j

L_g	Line inductance
LT_{exp}	Expected remaining useful lifetime
m	Modulation index
N	Number of cells in modular converter
n	Order of thermal network
$N(G)$	Nodes of graph G
N_{un}	Number of unloaded converter cells
N_f	Number of cycles to failure
N_{fi}	Durability of the i-th stress range
N_i	Number of cycles of the i-th stress range
$P_{\text{rec,diode,avg}}$	average reverse recovery diode losses
$P_{\text{sw,igbt,avg}}$	Average switching loss in IGBT
$P_{cond,device}$	Conduction loss of device under consideration
$P_{cond,diode,avg}$	Average conduction loss of diode
$P_{cond,IGBT,avg}$	Average conduction loss of IGBT
$P_{cond,IGBT}$	Conduction losses of IGBT
P_{max}	Maximum power unbalance limit
P_{min}	Minimum power unbalance limit
P_{rated}	Rated power of a converter
P_{tot}	Total loss of device under consideration
R	Thermal resistance
r	Number of Monte-Carlo simulations
$R(t)$	Reliability at time t
R_{th}	Thermal resistance
R_v	Virtual resistor
R_g	Line resistance
T	Time period
T_{bal}	Integral time constant of PI controller
T_{device}	Junction temperature of device under consideration
T_{hs}	Heatsink temperature
$T_{j,av}$	Average junction temperature
T_j	Junction temperature
t_{on}	On-duration of power cycling test
T_{on}	On-time of a device in a switching period
T_{sw}	Switching period
T_d	Junction temperature of diode
V_c	Output DC voltage of H-bridge cell
$V_{ce,sat}$	Collector emitter saturation voltage
$V_{DC,i}$	DC-link voltage of cell i
V_{device}	Voltage range of the device in power cycling test
V_g	RMS grid voltage
$V_{GE,th}$	Gate threshold voltage
V_f	Diode forward voltage drop

$W_{i,j}$	Weight of edge connecting nodes i and j
$Z_{th,jhs}$	Thermal impedance from junction to heatsink

Abbreviations

ADPWM	Advanced Discontinuous Pulse Width Modulation
ATC	Active Thermal Control
CBM	Condition Based Maintenance
CCSN	Center-Clamped Side-Non clamped
CDF	Cumulative Distribution Function
CHB	Cascaded H-bridge
CL	Constant Loads
CM	Condition Monitoring
CNSC	Center-Non clamped Side-Clamped
CTE	Coefficient of Thermal Expansion
DAB	Dual Active Bridge
DBC	Direct Bonded Copper
DER	Distributed Energy Resource
EMI	Electro-Magnetic Interface
FEM	Finite Element Method
FTA	Fault-Tree Analysis
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistors
IPOP	Input Parallel Output Parallel
ISOP	Input Series Output Parallel
ISOS	Input Series Output Series
LED	Light Emitting Diode
LESIT	Leistungs Elektronik Systemtechnik und Informations Technologie
LFT	Low Frequency Transformer
LVAC	Low Voltage Alternating Current
LVDC	Low Voltage Direct Current
MAB	Multiple Active Bridge
MEA	More Electric Aircraft
MMC	Modular Multilevel Converters
MPC	Model Predictive Control
MTTF	Mean Time To Failure
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PDF	Probability Density Function

PDS	Power Distribution System
PI	Proportional Integral
PMSM	Permanent Magnet Synchronous Machine
PoF	Physics-of-Failure
PR	Proportional Resonant
PRC	Power Routing Control
PV	Photo-Voltaic
PWM	Pulse Width Modulation
QAB	Quadruple Active Bridge
RUL	Remaining Useful Lifetime
SM	Sub-Module
ST	Smart Transformer
SST	Solid-State Transformer
THD	Total Harmonic Distortion
TSEP	Temperature Sensitive Electrical Parameter
UPS	Uninterrupted Power Supply
VL	Variable Loads
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

1 Introduction

Past decades have witnessed a radical change in the key performance indicators of power electronics systems. Apart from efficiency and power density, reliability has become the third pillar for the design in power electronic applications [1, 2]. The main focus of power electronics research over the years has been the improvement of efficiency and power density driven by power device technologies, magnetic solutions, topologies and control schemes. Motivated by carbon emission reduction policies worldwide, power electronics has emerged as the backbone of numerous industrial sectors such as renewable energy generation and distribution, electric vehicles, more electric aircraft, smart grids etc [3]. The business model of power electronics applications from mere product suppliers to comprehensive service providers has motivated the designers and researchers to give necessary importance to reliability engineering to guarantee reliable operation during the product life-cycle [2]. The evolution of reliability engineering in power electronics over the years illustrated in Fig. 1.1 depicts the gained momentum of reliability research in recent years.

In this context, this thesis work aims to investigate the impact of control strategies to optimize the reliability of the modular converter systems without compromising the efficiency. The importance of power electronics reliability and the application of modular power converters are motivated in this chapter. The necessity of an optimization control strategy through the management of power flow among the modular converter cells is explained to formulate the research proposal of the thesis. The final section of the chapter presents the structure of the thesis including the list of publications resulting from this work.

1.1 Importance of Power Electronics Reliability

Reliability is defined as the ability of an item to perform its designated function for the specified period under the given conditions [4, 5]. The reliability is usually measured using reliability metrics such as the probability of failure, frequency of failure, or availability of the item. The automotive and aerospace sectors demand very high reliability constraints since the failures could potentially result in fatal accidents. In the energy sector, power electronics based Smart Transformer (ST) is a promising solution for the various challenges posed by the high renewable energy penetration. However, ST needs to meet the high reliability standards set by its counterpart, the Low Frequency Transformer (LFT) [6].

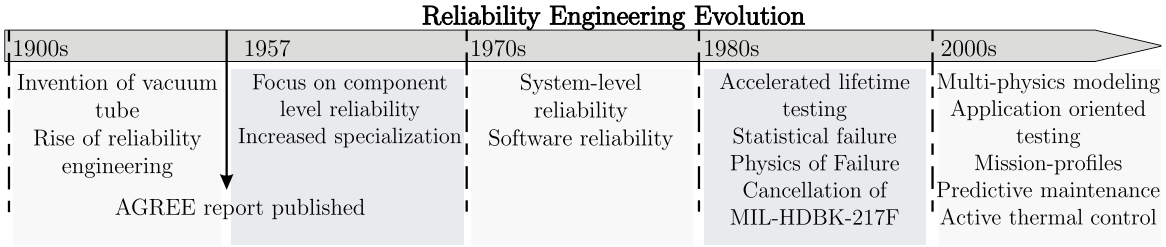


Figure 1.1: Evolution of reliability engineering over the years [2].

In general, the methodology of reliability engineering in power electronics can be broadly divided into three steps: 1) understanding the reasons of the failure with the help of analytical and empirical models, 2) reliability-oriented design of the system to account for the application specific stressors, and 3) active methods involving condition monitoring and control to enhance the reliability during the life-cycle of the product [6, 7]. As shown in Fig. 1.1, the reliability analysis heavily depended on the failure statistics in the past. Today, it is well-established that the pure statistics-based constant failure rate reliability methods are not relevant to power electronics systems as they do not address the cause of failure. Therefore, the Physics-of-Failure (PoF) approach has been introduced in power electronics to understand the physical causes of the failure and to evaluate the power electronics reliability systematically [1]. Based on the PoF approach, many industrial and academic studies have identified that the main challenges for the reliability in power electronic systems are the power semiconductors and capacitors [8, 9]. The failure mechanisms of the power devices and capacitors have been thoroughly studied in the literature leading to the development of many lifetime models. The major cause for the failure of the power semiconductor devices has been identified as the thermal stress caused by the thermal cycling [9, 10, 11].

The methods for reliability improvement in power electronics can be broadly classified into two categories, 1) passive methods, and 2) active methods [12, 7]. The passive methods mainly focus on designing the hardware of the power converters for enhanced reliability. Such approaches evaluate the reliability of critical components according to the application specific mission profile and lifetime requirements. Reliability-oriented design mainly focuses on optimizing the hardware design for fulfilling the lifetime criteria, and could potentially increase the cost of total hardware [2, 13, 14]. The active methods are mainly software based methods to actively control the failure causes of critical components. In contrast to the reliability-oriented design, the active methods such as the software based Active Thermal Control (ACT) uses the existing hardware and uses control algorithms to reduce the thermal stress of the power devices [15, 16, 12]. Software based thermal stress control methods can be deployed with marginal requirement of additional hardware and even could potentially be incorporated into the existing converter systems resulting in a cost effective solution.

In this thesis, active methods for improving the reliability of the power electronics system are investigated in detail due to their cost-effectiveness and the ability to respond to changes in the working condition of the converter.

1.2 Motivation for Modular Power Converters

The concept of modularity is not new and it has been widely employed in different fields such as automotive, computer technologies, electric power distributions, solar panels etc. primarily due to the offered benefits such as scalability, re-usability, cost-effectiveness, design flexibility, and augmentation [17, 18, 19, 20]. The motivation for the use of modular solutions in the field of power electronics arises from a multitude of reasons. The main benefits of modular architecture can be summarized as follows.

- Better availability due to a higher degree of fault tolerance and potential derated operation
- Potential increase in efficiency
- Voltage and power scalability
- Superior power quality
- Reduced voltage and current stress (dv/dt and di/dt)
- Decrease in filter size and reduced Electro-Magnetic Interface (EMI) emission

The Smart Transformer employs a multi-stage modular architecture to compete with the high reliability and efficiency benchmarks set by the LFT [6]. The studies show that the use of a lower blocking voltage power device can result in better efficiency compared to the higher blocking voltage devices [21, 22]. Moreover, the voltage and current scalability offered by the modular solutions combined with the unavailability of a single semiconductor power module for the medium voltage applications drives the industry to adopt modular architectures for high power applications [23]. For example, Modular Multilevel Converters (MMC) is one of the main topologies for high voltage applications such as High Voltage Direct Current (HVDC) transmission [17, 18].

Modular topologies/architectures increase the degree of failure tolerance and facilitate post fault operation without system shutdown [24, 25]. The faulty building block/cell of the modular converter can be replaced with another cell during maintenance [6, 26]. The cost of an additional building block to increase redundancy is much lower than that of adding redundancy to a non-modular system. Moreover, reduced voltage/power stress in the modular converter architectures also decreases the probability of failures [25]. With respect to efficiency, the reduced output filter size in modular architectures increases the system efficiency. The superior electrical parameters of the lower blocking voltage devices result in a better efficiency compared to the non-modular systems [22]. In the case of Input Parallel Output Parallel (IPOP) modular topologies, the light load efficiency is improved by deactivating the modular cells and this technique is popularly known as phase shedding [27].

In short, modular topologies are a necessity when the voltage levels are higher than the available power semiconductor blocking voltage limits. However, for high reliability and high efficiency applications, modular power converters offer cost-effective solutions with superior power quality and better maintenance opportunities.

1.3 Motivation for Optimal Power Flow Solutions

Even though modular converters offer higher flexibility of redundancy, the potential for efficiency improvement, and better maintenance opportunities, some challenges need to be addressed for high reliability applications. For any power electronics system, failures can be classified into random and wear-out based failures according to the bathtub curve [28]. To

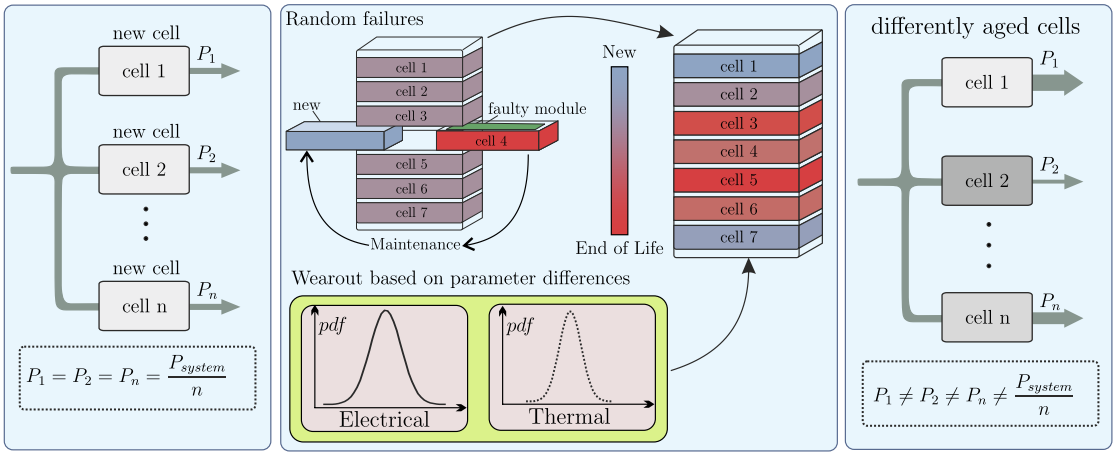


Figure 1.2: Failure and replacement cycle of modular power converters without and with power routing control [6].

ensure the reliable operation of the modular converter, the failure cases and replacement cycle are analyzed and are shown in Fig. 1.2. In the case of any failure, the replacement cycle follows the illustration in Fig. 1.2. It is logical that when one cell fails, it is sent to maintenance and replaced irrespective of the failed component. Consequently, a modular converter system comprises cells with different aging [6]. Fig. 1.2 also shows the failures due to the wear-out-based aging of converter cells. For a modular power converter system with N cells, the power device dependent parameters such as the average on-state voltage drop and on-state resistance vary between these cells due to the tolerances in the manufacturing process. The heatsink temperatures also differ between the cells, even when they process the same power, depending on the spatial configuration of the heatsinks and the direction of flow of the coolant. These electrical and thermal parameter variations result in different junction temperatures among the cells, and thereby different accumulated damages even if they process equal power [29]. Therefore, some cells fail earlier than the other ones, even when the power is equally distributed among them [30, 29].

Therefore, both the failure replacement cycles and asymmetric wear-out due to the differences in electrical and thermal parameters lead to cells with different aging in a modular converter. This has an impact on the maintenance scheduling and can result in intermittent failures leading to higher maintenance costs and possible service interruptions. The solution proposed to overcome this challenge is through power routing: "uneven loading of the cells of a modular converter to control the thermal stress among cells" [6]. With the help of power routing, the thermal stress based failures can be delayed, maintenance can be scheduled optimally and abnormal operation of the converter due to changes in ambient conditions or auxiliary system failures can be controlled.

The thesis work explores different power routing strategies in modular converters to increase system reliability. Since thermal stress is not the only challenge in modular systems, factors such as efficiency and maintenance scheduling shall be considered while developing power routing techniques. To tackle this multi-objective optimization problem, graph theoretic models are used in this work to develop optimal power flow solutions.

1.4 Research Proposal

The thesis aims to develop a generalized method to optimize the reliability and efficiency of modular power converters. The reliability analysis is mainly focused on the thermal stress of the power semiconductor devices for different modular converter architectures with different operating conditions. Based on the reliability studies, new algorithms for system level control of the reliability of the modular converters without compromising the efficiency are presented. The main targets of the thesis can be classified into two as follows:

Target I: Analysis, design and implementation of power routing based active thermal control in modular converters

The first research objective is to motivate the necessity of power routing in modular power converters and subsequently develop system level power routing algorithms to control the thermal stress in modular converter cells. The developed algorithms shall be validated by simulation and experimental methods. Challenges to the implementation of power routing algorithms shall be investigated and necessary improvement strategies shall be explored.

Target II: Modeling and development of graph theory based optimal power flow solutions for modular power converters

Another target of this work is to develop a unified modeling technique for the power routing of modular converters using graph theory. Graph theory is well-known for its application in several fields such as computer science and communication, and is typically used for solving network flow problems. The goal is to model the modular power converter as a graph considering the power flow analogous to the information flow in data networks. Afterward, the graph model of modular converters can be used for developing optimal power flow solutions to improve system reliability and efficiency.

1.5 Structure of the Thesis

The topics investigated in this thesis are organized into 7 chapters as depicted in Fig. 1.3 along with their associated publications.

- Chapter 2 provides the necessary theoretical background for this work focusing on the fundamentals of power electronics reliability, condition monitoring techniques, and prognostic maintenance. The active thermal control methods are reviewed and the methodology of thermal stress and reliability analysis of the power converters adopted in this work is presented [J8, C3].
- Chapter 3 introduces the selected modular power converter topologies for Smart Transformer and more electric aircraft applications. A novel approach for the representation of the modular power converters is proposed using graph theory for developing optimal power flow algorithms [J5, C6].

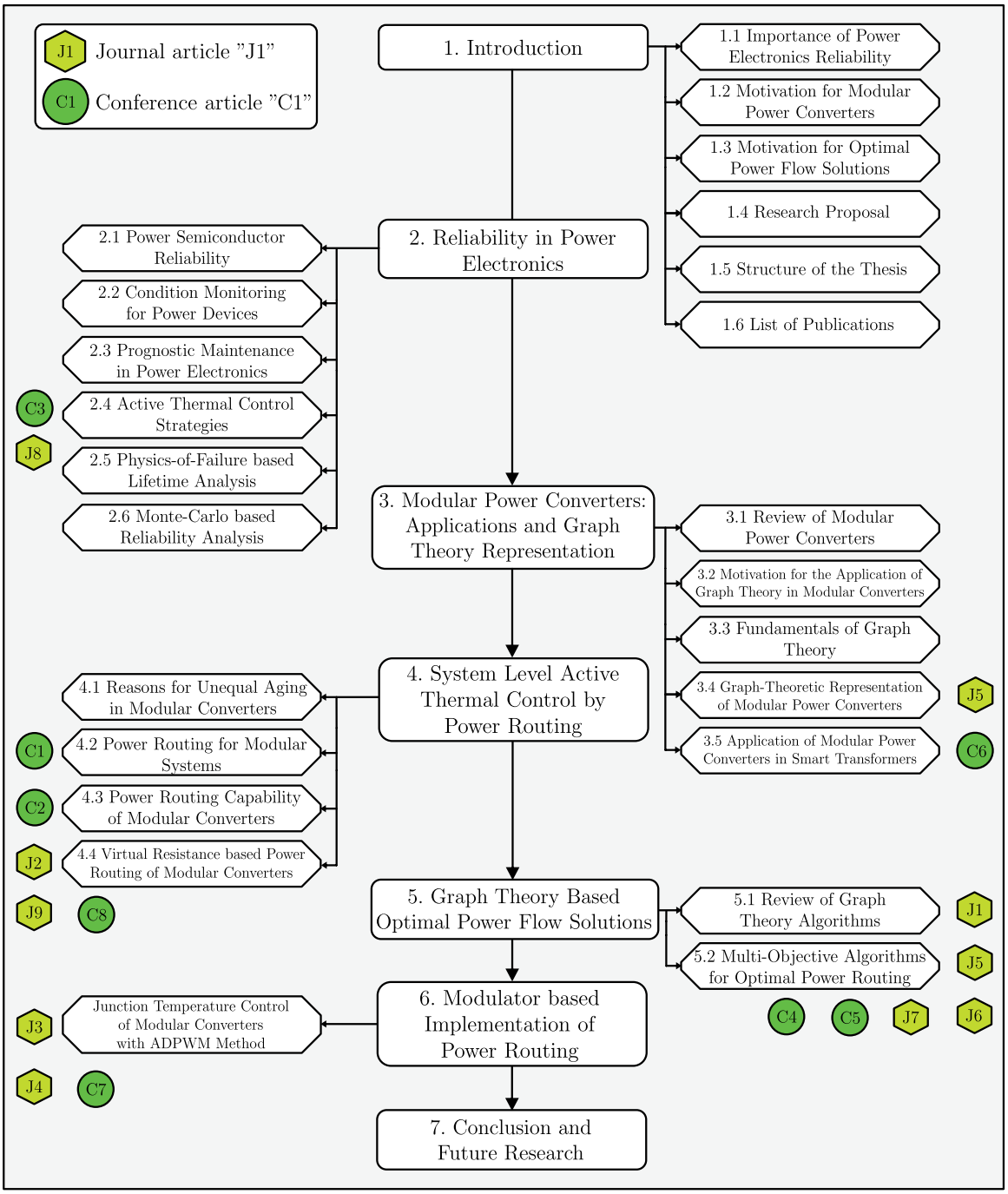


Figure 1.3: Structure of the thesis.

- Chapter 4 explores the power routing strategy for the system level active thermal control in modular power converters. The necessity for power routing is motivated and a virtual resistance based power routing strategy is proposed of modular converter systems [J2, J9, C1, C2, C8].

- Chapter 5 describes the development of graph theory based optimal power flow algorithms in modular converters. Starting from the fundamentals of graph theoretical optimization, three power flow optimization algorithms are developed for improving the reliability, efficiency, and maintenance scheduling of modular systems [J1, J5, J6, J7, C4, C5, C6].

- Chapter 6 depicts the reliability analysis of a novel modulation strategy to implement power routing in multi-stage modular converter systems without compromising system efficiency [J3, J4, C7].
- Chapter 7 summarizes the main findings of this thesis work followed by conclusion and future research.

1.6 List of Publications

The list of scientific papers associated with this thesis which have been published are given as follows:

Journal publications

J1 M. Liserre, G. Buticchi, J. I. Leon, A. Marquez Alcaide, **V. Raveendran**, Y. Ko, M. Andresen, V. G. Monopoli, L. Franquelo, "Power Routing: A New Paradigm for Maintenance Scheduling," in IEEE Industrial Electronics Magazine, vol. 14, no. 3, pp. 33-45, Sept. 2020

J2 **V. Raveendran**, M. Andresen, G. Buticchi and M. Liserre, "Thermal Stress Based Power Routing of Smart Transformer With CHB and DAB Converters," in IEEE Transactions on Power Electronics, vol. 35, no. 4, pp. 4205-4215, April 2020.

J3 Y. Ko, **V. Raveendran**, M. Andresen and M. Liserre, "Advanced Discontinuous Modulation for Thermally Compensated Modular Smart Transformers," in IEEE Transactions on Power Electronics, vol. 35, no. 3, pp. 2445-2457, March 2020.

J4 Y. Ko, **V. Raveendran**, M. Andresen and M. Liserre, "Thermally Compensated Discontinuous Modulation for MVAC/LVDC Building Blocks of Modular Smart Transformers," in IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 220-231, Jan. 2020.

J5 M. Liserre, **V. Raveendran** and M. Andresen, "Graph Theory Based Modeling and Control for System-level Optimization of Smart Transformers," in IEEE Transactions on Industrial Electronics.

J6 **V. Raveendran**, M. Andresen and M. Liserre, "Improving Onboard Converter Reliability for More Electric Aircraft With Lifetime-Based Control," in IEEE Transactions on Industrial Electronics, vol. 66, no. 7, pp. 5787-5796, July 2019.

J7 M. Andresen, J. Kuprat, **V. Raveendran**, J. Falck and M. Liserre, "Active thermal control for delaying maintenance of power electronics converters," in Chinese Journal of Electrical Engineering, vol. 4, no. 3, pp. 13-20, September 2018.

J8 P. Kumar Prasobhu, **V. Raveendran**, G. Buticchi and M. Liserre, "Active Thermal Control of GaN-Based DC/DC Converter," in IEEE Transactions on Industry Applications, vol. 54, no. 4, pp. 3529-3540, July-Aug. 2018.

J9 M. Andresen, **V. Raveendran**, G. Buticchi and M. Liserre, "Lifetime-Based Power Routing in Parallel Converters for Smart Transformer Application," in IEEE Transactions on Industrial Electronics, vol. 65, no. 2, pp. 1675-1684, Feb. 2018.

Conference publications

C1 **V. Raveendran**, M. Andresen, G. Buticchi and M. Liserre, "Reliability Enhancement of Modular Smart Transformers by Uneven Loading of Cells," PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2017, pp. 1-8.

C2 **V. Raveendran**, G. Buticchi, A. Mercante and M. Liserre, "Comparison of voltage control methods of CHB converters for power routing in smart transformer," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 1652-1658.

C3 P. K. Prasobhu, **V. Raveendran**, G. Buticchi and M. Liserre, "Active thermal control of a DC/DC GaN-based converter," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 1146-1152.

C4 **V. Raveendran**, M. Andresen and M. Liserre, "Lifetime Control of Modular Smart Transformers Considering the Maintenance Schedule," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 60-66.

C5 **V. Raveendran**, M. Andresen and M. Liserre, "Reliability Oriented Control of DC/DC Converters for More Electric Aircraft," 2018 IEEE 27th International Symposium on Industrial Electronics (ISIE), Cairns, QLD, 2018, pp. 1352-1358.

C6 **V. Raveendran**, M. Andresen and M. Liserre, "Graph Theory-Based Power Routing in Modular Power Converters Considering Efficiency and Reliability," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, 2018, pp. 1237-1242.

C7 Y. Ko, **V. Raveendran**, M. Andresen and M. Liserre, "Discontinuous Modulation based Power Routing for Modular Smart Transformers," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 1084-1090.

C8 **V. Raveendran**, M. Andresen, M. Liserre and G. Buticchi, "Lifetime-based power routing of smart transformer with CHB and DAB converters," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 3523-3529.

2 Reliability in Power Electronics

Power electronics is becoming the backbone of a multitude of fields such as the automotive industry, energy sector, aerospace, industrial drives, railway, and shipping sector to achieve higher efficiency, performance, power density, and reduced carbon footprint [3, 31]. With the increased number of power electronic components, reliable operation of power electronics for the designated lifetime becomes more crucial for safety critical applications. There are many stressors identified for the failure of power electronics systems such as temperature cycling, high temperatures, humidity, vibration, pollution, and radiation. According to the latest industrial survey covering various areas such as wind power, Photo-Voltaic (PV), electric vehicles, Uninterrupted Power Supplies (UPS), aviation, and energy transmission, power semiconductor devices are identified as the most vulnerable component to failure [32]. These findings corroborate the earlier studies which have identified power semiconductor devices being one of the most fragile components in a power converter along with the capacitors [9, 1, 33]. The industry believes that the future reliability research of the power converters should mainly focus on the power semiconductors and capacitors as indicated in Fig. 2.1, since about 40 % of the failures arise from the power semiconductors [32]. Since it is well-established that the power semiconductors are one of the most vulnerable components in a power converter system, the main focus is on the power semiconductor reliability to evaluate the power converter reliability.

The chapter presents the theoretical background for the reliability analysis and methodology of reliability evaluation followed in this work. First, a brief discussion about power module reliability, condition monitoring methods, and maintenance strategies are given. Then, Physics of Failure based reliability analysis using lifetime models, mission profiles, and electro-thermal models is explained in detail. The chapter ends with the fundamentals of Monte-Carlo based reliability analysis relevant for this thesis. The publications [J8] and [C3] contribute to the content of this chapter.

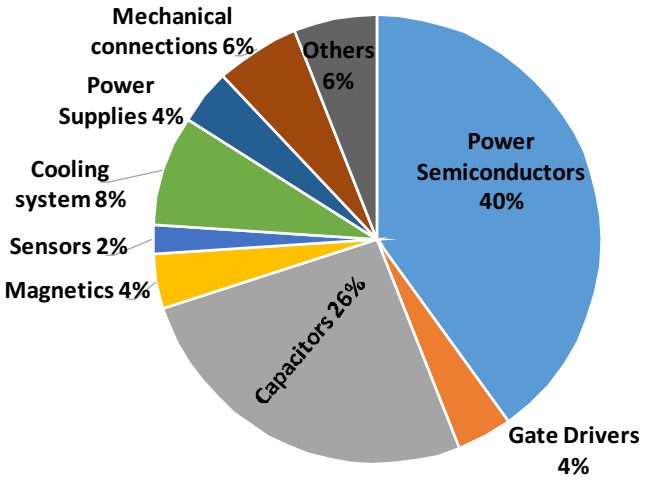


Figure 2.1: Industry perspective: Normalized failures in power electronics components [32].

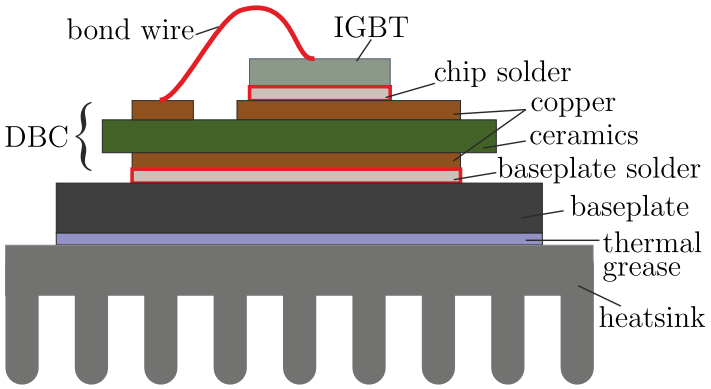


Figure 2.2: Standard structure of an IGBT module.

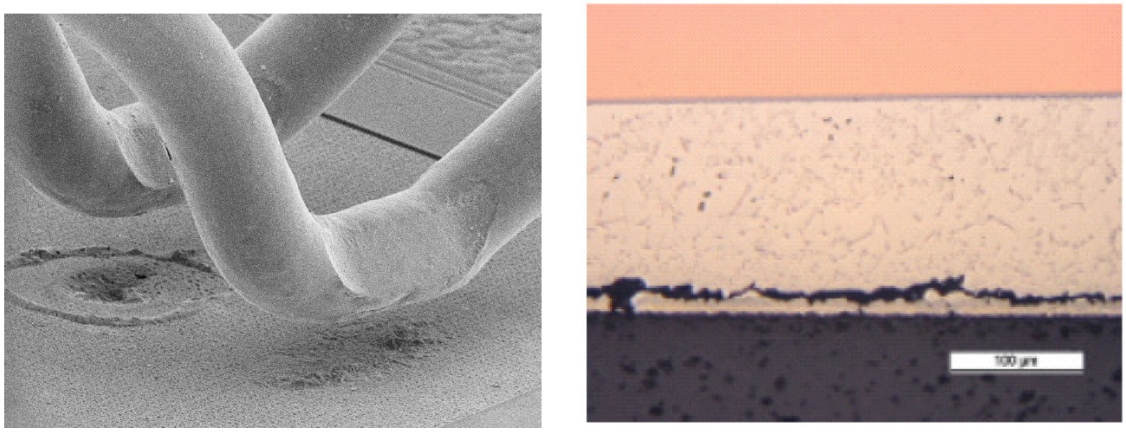
2.1 Power Semiconductor Reliability

Among the power semiconductor devices, Insulated Gate Bipolar Transistors (IGBT) are the most commonly used ones owing to their high performance, low cost, better reliability and wide power range. Since its invention in 1982, IGBTs have penetrated the power converter market with devices available up to voltage and current ratings in the range of kilovolt (kV) and kiloampere (kA) respectively [4]. For the modular power converter topologies analysed in this thesis, IGBT modules have been considered due to their power rating compatibility.

In several applications, the power devices are used as power modules with special packaging. The module packaging provides the necessary electrical connection between the semiconductor chips, guarantees the necessary insulation, facilitates the dissipation of generated heat, protects the semiconductor chip from ambient conditions, and reduces the costs [34]. One of the widely popular packaging technologies for power devices is the use of Direct Bonded Copper (DBC). Fig. 2.2 shows the Direct Bonded Copper structure of an IGBT module. The DBC structure is adopted to provide good electrical and thermal properties for the IGBT module. The ceramic provides the electrical insulation between the power and cooling components and is usually made of aluminium oxide or aluminium nitride. Copper conducts the current and also provides a good thermal connection to the heatsink. The base plate is an optional component in the low power range. The IGBT chips are soldered to the DBC and the DBC is soldered to the base plate. The chips are connected to the upper copper substrate with the help of solder and the top of the chips are connected electrically using bond wires. The power modules are usually encased with a molding material, and for low voltage applications, open module construction is also followed. [35].

The most fragile connections in the IGBT structure are the bond-wire, chip solder and baseplate solder, and are marked in red in Fig. 2.2 [36]. The main failure mechanisms identified in the IGBT modules are:

- Bond-wire liftoff
- Chip solder fatigue
- Base plate solder fatigue



(a) (b)

Figure 2.3: IGBT failure mechanisms (a) Bond-wire lift-off (b) Solder joint cracking [34].

- Metallization reconstruction

Bond-wire liftoff is perhaps the most prominent failure mechanism of IGBT power modules. It is clear that the IGBT module consists of different materials with different Coefficient of Thermal Expansion (CTE) as shown in Fig. 2.2. The IGBT and diode chips produce losses during the operation, which results in the heating of the materials in the module. The CTE mismatch of the Aluminium bond wires and the silicon IGBT chip is the largest in the module and this leads to the bond wire crack failure or liftoff. Thermal cycling has been identified as the main cause of bond wire liftoff [34]. When one bond wire fails due to crack or liftoff, the remaining bond wires need to carry the full device current, thereby accelerating the degradation due to higher thermo-mechanical stress. An electron microscope image of the bond wire liftoff is illustrated in Fig. 2.3 (a).

Many solutions have been investigated to prevent bond-wire related failures. Since the CTE mismatch between Aluminium and Silicon is the main reason for higher thermo-mechanical stress, copper has been used to replace Aluminium to provide better performance [37]. Other approaches involve avoiding bond-wires through direct bonding, and increasing the contact area offering a lower resistance path [38]. Solutions with an intermediate layer to act as strain buffer and optimal design of bond-wire geometries are also considered [39]. However, the alternatives have not been successful in replacing the Aluminium bond wires in high power IGBT modules due to the simple packaging procedure, flexibility and low cost.

Solder fatigue has been identified as another major failure mechanism in IGBT which occurs at the chip solder joint and baseplate solder joint as indicated by the red color in Fig. 2.2. The main reason for the solder fatigue is the thermo-mechanical stress introduced by the thermal cycling and the CTE mismatch between the solder, substrate, silicon chip, and baseplate. The solder fatigue results in cracks and voids in the solder joints as shown in Fig. 2.3 (b). Once the degradation starts, the additional stress on the non-affected part accelerates the damage similar to that of the bond-wire fatigue. The solutions for preventing solder fatigue include replacing the solder interface with sintering technology. The solder interface

between the chip and the substrate is replaced using silver diffusion sinter technology to form a homogeneous layer without voids [40].

Metallization reconstruction is the result of thermo-mechanical stress at the interface of silicon chips and electrical connections. In order to facilitate electrical connection with the Silicon, the standard technique is to add a film of Aluminum through vapour deposition and thermal annealing. Similar to other fatigue mechanisms, the CTE mismatch between Aluminium and Silicon creates high thermo-mechanical stress at this interface when subjected to thermal cycling. Prolonged thermal cycling results in the creation of voids or extrusion of aluminium grain at the metallization interface and is called metallization reconstruction. [41].

Since the main failure mechanisms of power devices have been recognized, the next step is to detect and prevent these failures in the field. The following section details the methods for detecting the failures in advance by suitable condition monitoring techniques.

2.2 Condition Monitoring for Power Devices

Condition Monitoring (CM) is defined as a technique used to monitor the relevant parameter of an operating system for scheduling maintenance before failure or performance degradation [42, 43]. CM is a multidisciplinary strategy that includes the knowledge of the physics of failure of the components and the system, sensor technology, data acquisition and analysis, and the capability to determine the health of the system. As illustrated in Fig. 2.1, power semiconductor devices constitute the majority share of failures in a power electronics system. Hence, only the CM techniques relevant to the power devices are discussed in this section.

Power semiconductor devices and power converters are striving to improve the power density by reducing the size and increasing the rated power which makes the design of CM techniques more challenging. For any CM technique, the nature of the physical degradation of the device and its impact on the converter operation shall be investigated. The principle behind condition monitoring can be categorized into three types [44];

- Monitoring of device parameters indicative of degradation: Instead of directly measuring the degradation of the component itself, usually it is easier and less invasive to monitor the electrical or mechanical parameters that are sensitive to the device degradation. For example, thermal resistance R_{th} and on-state collector-emitter voltage drop $V_{ce,sat}$ of the IGBT modules are used to monitor solder cracks and bond wire liftoff respectively.
- Direct monitoring of device degradation: This can be done using sensors embedded in the device to monitor any physical degradation; for instance, mechanical stress monitoring of the power modules using sensors.
- Model-based Condition Monitoring: Model-based CM plays a major role in system level lifetime estimation and fault-detection strategies. For example, the degree of

Table 2.1: Condition Monitoring Techniques for Power Devices.

CM Parameter	Detected Failure	Challenges	Pros
$V_{ce,sat}$	Bond wire liftoff/crack	Difficult to guarantee accuracy and immunity to switching transients	Less invasive with medium implementation effort
R_{th}	Solder fatigue/crack	Internal temperature and power loss data required	Less invasive
T_j	Indirect Bond wire liftoff solder fatigue detection	Direct sensing is invasive and indirect methods pose inaccuracy	Multiple techniques available
Bond wire resistance	Bond wire liftoff	Highly invasive	Higher accuracy

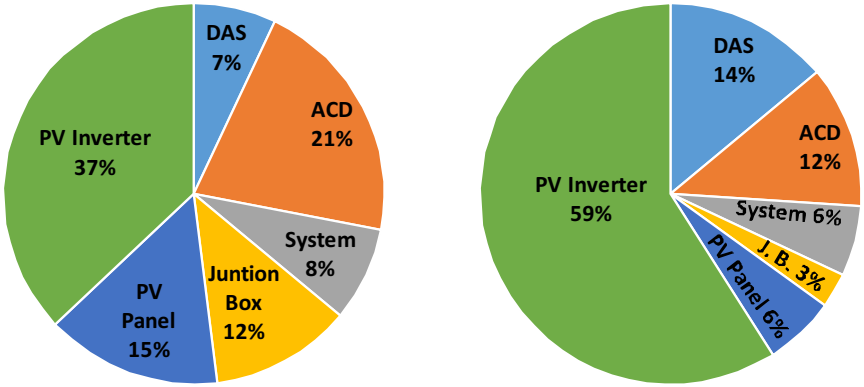
degradation can be estimated by the comparison of the response of measurement data with that of prediction by the model.

One of the most promising CM techniques for the IGBT power module is the on-state collector-emitter voltage drop measurement. The power cycling tests show that the $V_{ce,sat}$ changes significantly with bond wire liftoff degradation. When the $V_{ce,sat}$ increases by 15 %, IGBT is considered to be seriously damaged [44]. The on-state voltage drop is also used to calculate the junction temperature of the IGBT since it is a Temperature Sensitive Electrical Parameter (TSEP). The $V_{ce,sat}$ varies with the junction temperature and by using calibrated $V_{ce,sat}$ vs. junction temperature curves, device junction temperature can be estimated during the operation of the power converter [45, 46, 47, 48]. In this work, the $V_{ce,sat}$ sensing circuit illustrated in Fig. C.4 is used to estimate the device junction temperature and health status.

The thermal resistance of the power modules also varies with the degradation of the solder joints. Therefore, thermal resistance based condition monitoring is preferred to detect solder cracks or fatigue within the module. A 20 % increase in the R_{th} from the initial value is considered as the end-of-life of the power device [49, 50]. However, the main challenge for the calculation of the R_{th} is the knowledge of the internal temperature of the module and the power dissipation. One method to overcome the challenges is to embed thermal sensors within the module and measure the load current for power loss estimation.

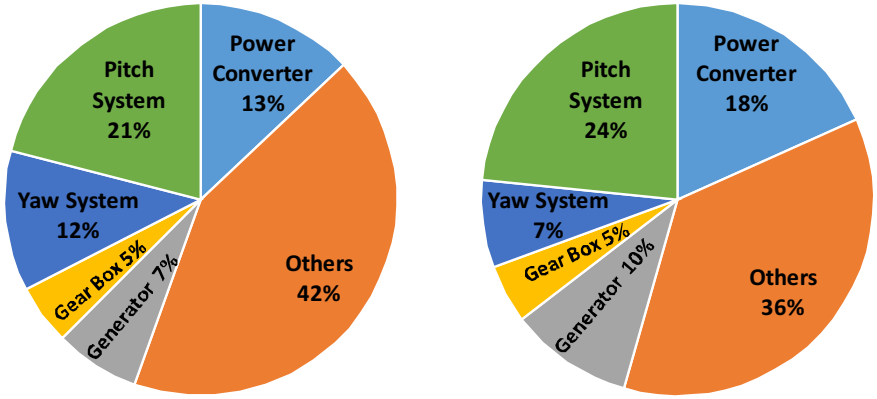
Another popular monitoring parameter for the power device is the junction temperature, but it is difficult to measure directly [51, 46]. Therefore, many research works focus on the indirect measurement of junction temperature with the help of TSEPs such as the $V_{ce,sat}$, gate threshold voltage $V_{GE,th}$ and transconductance g_m [44]. The $V_{ce,sat}$ varies almost linearly with the temperature and $V_{GE,th}$ decreases as the temperature rises [45, 52]. The measured/estimated junction temperature can be used to calculate the R_{th} or as an input for the lifetime models for predicting the health status of the power device [53]. The importance of CM has encouraged power module manufacturers like Semikron to produce intelligent power modules with sensors to detect bond wire liftoff [54]. In these intelligent modules, the DBC layout is modified to incorporate additional sensing elements to detect bond wire liftoff by monitoring the change in resistance. Selected CM techniques for the power devices have been summarized in Table 2.1.

To utilize the advantages offered by CM techniques, and to prevent unwanted disruption of



(a) (b)

Figure 2.4: PV plant maintenance experience (a) Unscheduled maintenance event share of subsystems (b) Unscheduled maintenance cost share of subsystems [33].



(a) (b)

Figure 2.5: Wind power plant failure share among subsystems (a) Failure rate (b) Downtime [55].

services due to power converter failures, maintenance based on condition monitoring needs to be in place. The next section discusses common maintenance practices and presents the advancements in the field of condition monitoring based maintenance.

2.3 Prognostic Maintenance in Power Electronics

In industry, the conventional maintenance strategies can be broadly classified into two categories; corrective and preventive maintenance [26]. Corrective maintenance is performed when a failure occurs whereas preventive maintenance focuses on the maintenance scheduled at predefined intervals to prohibit failures. Even though corrective maintenance does not have the cost burden for condition monitoring and scheduled maintenance routines, the cost of unexpected downtime and repairs may not be acceptable for most of the industries. The preventive maintenance is usually performed after a particular period of time, hours of operation, or kilometers driven. Although preventive maintenance improves the system re-

Table 2.2: Overview of Maintenance Strategies [56].

	Maintenance Strategies			
	Corrective	**Preventive**	**Condition Based Maintenance**	
			Diagnostic	**Prognostic**
Principle	Maintenance based on demand	Based on field experience	Identify impending failures based on CM data	RUL prediction based on CM data
Advantages	No CM costs	Control over maintenance schedules, labor and cost	Reduced unexpected failures	Higher availability
	No special maintenance requirement	Reduced chances of failures	No prognostic know-how required	Higher reliability and fewer secondary failures
Disadvantages	Lower reliability and availability	Scheduled repairs replace healthy components	High initial cost	High initial cost
	High repair costs	Cannot prevent unscheduled faults	Overall system health is unknown	Requires system model or data-driven methods

liability through inspections, tests, replacements etc., risk of failures remain high since the health of the system is unknown. For instance, maintaining power electronics in systems such as large fleets of aircraft and remotely located STs can be very challenging.

The maintenance activities require trained personnel with expertise, and according to level of fault, the system downtime can vary. Unscheduled maintenance can result in revenue loss and unavailability of the systems and these facts become crucial with increasing operational demands and lack of fiscal resources. For instance, [33] presents maintenance data from a large PV power generation plant. As illustrated in Fig. 2.4 (a), the power converter is the reason for the major share (37 %) of unscheduled maintenance events. The impact of unscheduled maintenance events on the maintenance cost is summarized in Fig. 2.4 (b), which clearly shows that the maintenance of the power converter is the most expensive (59 %) among all the subsystems. In wind turbine systems, the power converter is responsible for 13 % of total failures and 18 % of total system downtime as shown in Fig. 2.5 [55]. In short, the power converters play a crucial role in the reliable operation of renewable energy systems such as wind and solar power plants.

Due to increasing reliability requirements and costs associated with unexpected failures, newer maintenance policies based on Condition Based Maintenance (CBM) have gained importance in the last decades. CBM can be again classified into two sub-categories, namely, diagnostic and prognostic maintenance [56]. Diagnostic maintenance is defined as maintenance based on the current condition of the system under consideration. The definition of prognostics is the ability to provide early detection of the incipient faults of a component and to predict the progression of such a fault resulting in the component failure [26]. With prognostics, the remaining useful life of the system can be predicted with an acceptable degree of confidence and when such a piece of information is used to schedule maintenance, it is termed prognostic maintenance [57]. Prognostic maintenance becomes an essential requirement of systems, which require high reliability and availability.

The major maintenance strategies followed in the industry are summarized in Table. 2.2 clearly indicating the principle, advantages and disadvantages of each maintenance policy. The CBM based on prognostic is preferred in applications requiring high availability and

reliability since the health of the system is evaluated based on physical models, data-driven methods or hybrid approaches. In contrast to the diagnostic approach which monitors impending failures based on CM data, prognostics provides a more concrete picture of the failure probability of the system based on RUL. Prognostics can help to optimally schedule maintenance, procure spare parts and labour optimally, and use the system components to their end of life while keeping the failure probability within limits.

Several papers have discussed optimizing the maintenance schedules and predicting failures based on the monitored data considering operational constraints [58, 57]. In [58], maintenance schedule optimization of an aircraft fleet focusing on a trade-off analysis considering cost, capacity expansion and other key performance indexes in aircraft fleet management is discussed. Engine fault prediction of aircraft using CBM and machine learning has been proposed in [57]. Compared to the traditional data-driven prognostic algorithms, a computationally efficient and real-time RUL estimation of the IGBTs using the degradation profile from the power cycling tests is presented in [59]. Remarkably, $V_{ce,sat}$ is considered as the CM parameter indicative of power device degradation in this approach [59]. In summary, condition based maintenance has opened up new research frontiers for power electronics reliability.

Although prognostic maintenance relies on the physics-of-failure to detect and prevent failures based on condition monitoring, the root-cause of failures is not addressed. In this context, active thermal control methods have been proposed in the literature to act directly on the failure root-cause, thereby aiming to prolong the power device lifetime. A short overview of active thermal control strategies is detailed in the following section.

2.4 Active Thermal Control Strategies

As discussed in the previous sections, thermal cycling has been identified as one of the major causes of failures of power devices. Therefore, it is necessary to develop methods to improve the thermal performance of the power devices by reducing the potentially damaging stresses. These methods shall also safeguard other operating performance indices at the same time. The methods developed to improve the thermal performance of the power electronic devices by controlling the junction temperature cycling are termed active thermal control strategies. The active thermal control methods can be classified into three levels depending on the hierarchy of implementation, namely, device level, modulator level and system level [15, 60, 61].

2.4.1 Device Level

The device level active thermal control methods directly act on the device characteristics to reduce the thermal cycling. This requires modifications in the hardware to directly influence the operation of the device and hence, most of the literature focus on active gate driver methods [62, 63, 64, 65]. A temperature dependent gate driving of power MOSFETs is developed

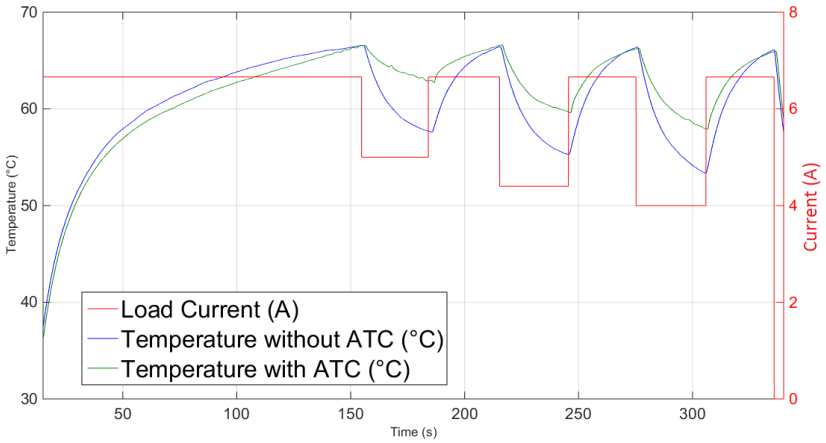


Figure 2.6: Case temperature measurement of GaN device without and with active thermal control for a given load profile [J8].

in [63] to decrease the thermal stress and losses. In [65], an active gate driver is proposed to balance the current among parallel IGBTs since the losses are different due to the tolerances of the semiconductor. The turn-on and turn-off of the devices are controlled to achieve transient current balancing among the paralleled IGBTs. Another method to achieve thermal balance among parallel devices by controlling the gate voltage and resistance is demonstrated in [62]. The main advantage of the gate driver based ATC is that the thermal stress reduction effort is independent of the converter control or modulation strategies. Therefore, these ATC strategies can be used for any converter topology without modification in the control system. The main challenge with device level ATC methods is the hardware efforts while designing the system.

Another popular technique to thermally balance the power devices is active cooling. A dynamic cooling system has been developed in [66] to reduce the thermal cycling of power modules by actively varying the cooling fan speed. This method uses a state observer for estimating the junction temperature and is demonstrated to reduce the thermal cycling under varying load conditions. The development of the required hardware for an active cooling system is described in detail in [67]. Compared to the active gate driver methods, the main disadvantage of the active cooling methods is the inability to reduce the high frequency thermal cycles due to relatively slower cooling time constants.

To limit the thermal cycling induced failures in solder joints, an active thermal control scheme using a two-step gate driver designed for GaN is presented [68]. In contrast to the active thermal control techniques employing variable switching frequency control, this method does not alter the converter operation frequency, instead, it merely controls the GaN device slew rates. The two-step gate driver designed and developed is for GS66508T (top side cooled GaN device from GaNSystems) [69, 70]. The two-gate driver provides a stepped voltage during turn-on to actively control the rise time t_r of the GaN device. Thus, by varying the rise time t_r, the switching loss variation is ensured.

The impact of the active thermal control on a bidirectional single-phase DC/DC converter is validated experimentally using the prototype of the two-step gate driver based buck converter

shown in Fig. C.5. In order to show the effectiveness of the thermal cycle minimizing the effect of active gate driver, a mission profile with varying load current is chosen as shown by the red trace in Fig. 2.6. The blue trace in Fig. 2.6 shows the case temperature thermal cycling without active thermal control for the given load profile. When the aforementioned active thermal control scheme is active, the gate driver increases the switching losses to minimize the thermal cycling. The impact of active thermal control is evident by the reduction of temperature swings indicated by the green trace in Fig. 2.6. The result demonstrates a reduction of thermal swing from 13°C to 7°C with the proposed active gate driver.

2.4.2 Modulator Level

One of the well-known modulation based method to control the losses in the power devices is by actively changing the switching frequency. Switching frequency based active thermal control methods are investigated in [71, 72, 73], where the switching frequency is varied to reduce the thermal cycling due to load fluctuations. A novel switching frequency variation based ATC without a priori knowledge of the mission profile for a single phase converter is demonstrated in [71]. An electro-thermal model based junction temperature estimation is developed for realizing ATC for an electric vehicle application is studied in [72]. Another approach combines switching frequency based ATC with active cooling to reduce the thermal stress in wind power converter [73]. The main drawback of the switching frequency variation methods are the varied current spectrum, higher mean temperature, and lower efficiencies at higher switching frequencies. Rather than directly reducing the switching losses by reducing switching frequency, switching losses of power devices in a power converter is reduced through different modulation techniques. For the converter in an electric vehicle application, discontinuous PWM is employed to reduce the switching losses of the power devices during the start-up procedure to safeguard the converter thermal limits [74].

2.4.3 System Level

System level ATC methods focus on adjusting the control parameters to reduce thermal stress. One opportunity to control the device losses of the power devices in a converter is by changing the applied voltage. In the case of a Permanent Magnet Synchronous Machine drive, the DC-link voltage is dynamically adapted to achieve thermal cycling reduction and higher efficiencies in [75]. The losses of the power devices can be reduced by lowering the DC-link voltage, particularly at lower motor speeds. The control system design to provide an optimal torque while reducing the thermal cycling of the devices with a variable DC-link is challenging in this approach. In parallel Neutral Point Clamped (NPC) converters for wind power application, the thermal swing of the most stressed devices is reduced by increasing the generated losses using the reactive power circulation method [76]. The main drawback of the reactive power circulation method is the resulting higher mean junction temperatures of the stressed devices and the increase in thermal stress of the other devices.

2.5 Physics-of-Failure based Lifetime Analysis

Previous sections discussed the major power device failure mechanisms, condition monitoring of the relevant physical parameters to schedule maintenance, as well as active thermal control methods to influence the failure root cause. However, it is essential to quantitatively determine the expected lifetime of a device during the design stage, and to establish scientific methodologies for evaluating the reliability impact of aforementioned ATC approaches. In this context, this section elaborates on the lifetime and reliability evaluation methods adopted in this thesis.

First, a short theoretical background about the reliability metrics is presented. Subsequently, motivation to adopt the Physics-of-Failure (PoF) approach is given. The is followed by the lifetime modeling of power devices based on the physics of failure. The reliability analysis of converters with the help of mission profile and PoF based lifetime models is covered in the final part of the section.

2.5.1 Reliability Metrics

Before venturing into the reliability analysis, the fundamentals of reliability engineering are presented first. For reliability analysis, it is imperative to understand the Weibull distribution and its properties. The distinguishing feature of the Weibull compared to the normal distribution is that the cumulative distribution function (CDF) of Weibull is bounded, which hence makes it attractive for predicting the failure probability. Depending on the number of parameters, Weibull distribution can be classified into a three-parameter distribution and a two-parameter distribution. The CDF of a three-parameter Weibull is expressed as

$$F(x) = 1 - \exp\left[-\left(\frac{x-\gamma_w}{\alpha_w}\right)^{\beta}\right], \tag{2.1}$$

where $x > \gamma_w$, and γ_w is called the threshold or location parameter which indicates that the failure occurs only when the x is greater than the threshold value γ_w. Assuming that the failure can occur from the beginning of operation of a component, γ_w becomes 0 and the aforementioned Weibull distribution reduces to a two-parameter version. The parameters α_w and β are respectively known as the scale parameter and shape parameter. When β is 1, the Weibull distribution transforms into an exponential distribution. The Weibull distribution offers the flexibility to model different lifetime behaviours by adjusting the parameters [77].

In order to quantify the reliability of power electronics systems, different metrics such as reliability, failure rates, unreliability, Mean Time To Failure (MTTF) and B_x lifetime are employed. It is common practice to use Weibull distribution to define these reliability metrics. However, to derive these metrics, aspects such as failure criteria, environment factors, stress conditions, confidence interval, and time are critical. If any of these factors vary, the reliability description can vary.

Reliability $R(t)$ is defined as the percentage of samples under consideration that can function properly at an instant t. For each sample, $R(t)$ is the probability that the sample functions at time t. The unreliability $F(t)$ is defined as the probability of failure of a sample at an instant t. It is calculated as [5]

$$F(t) = 1 - R(t). \tag{2.2}$$

The variation of unreliability $F(t)$ in time is expressed as the cumulative distribution function curve and in the case of a two-parameter Weibull distribution, the $F(t)$ can be given as

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\alpha_w}\right)^{\beta}\right]. \tag{2.3}$$

In industrial applications, MTTF is the most commonly used reliability metric which denotes the average time at which a sample fails. However, it does not reflect the variation of the reliability over time and the root cause of failure is ignored. MTTF can be calculated as [5, 28]

$$MTTF = \int_0^{\infty} R(t)d(t). \tag{2.4}$$

Today, the use of B_x lifetime is gaining popularity over the MTTF metric. B_x lifetime of a group of samples is defined as the time at which x percentage of samples have failed. For instance, B_{10} lifetime is defined as the time at which 10 % of the samples under the test have failed. The B_x lifetime can be obtained from the CDF curve and therefore the time-varying nature of the reliability function is reflected in the B_x lifetime [78, 1].

Another important reliability metric is the failure rate $\lambda(t)$ which defines the frequency of failure of the sample under consideration. Mathematically, the failure rate is expressed as

$$\lambda(t) = \frac{1}{R(t)} \frac{d(1-R(t))}{dt}. \tag{2.5}$$

2.5.2 Motivation for the adoption of PoF based approach

In the case of power electronics components, the plot of failure rate $\lambda(t)$ against time results in a bathtub shaped curve as shown in Fig. 2.7 [28]. The bathtub curve is composed of three types of failures; namely early failures, random failures and wear-out failures. Depending on the dominant failure mechanism, the overall lifetime of the electronics component can be divided into three stages; infant mortality, useful life and end of life respectively as indicated in Fig. 2.7. In the early stages of the product life, the majority of failures occur due to the defects arising out of the manufacturing processes or improper installation or operation. Such failures are termed early failures. The second stage is dominated by the random failures and this period is termed the useful life of the product. As shown in Fig. 2.7, the wear-out failures increase as time progresses and towards the end of life of the component, wear-out failures become the dominant failure mechanism [28, 2].

As discussed in Section 2.1, thermo-mechanical stress in power modules leads to failures over time because of the CTE mismatch of different materials used in power module con-

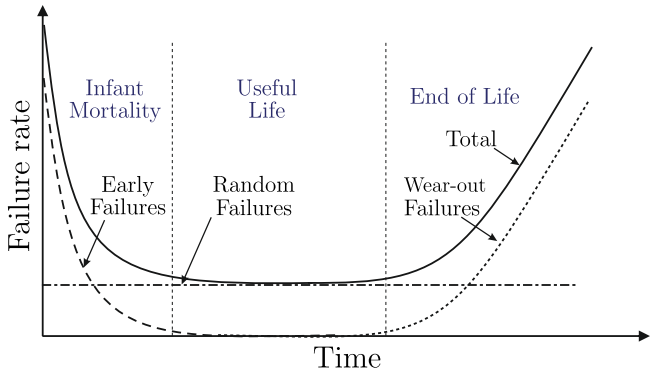


Figure 2.7: The bathtub curve or failure rate curve of typical power electronics component.

struction. However, conventional reliability prediction methods for electronics such as MIL-HDBK-217, FIDES and PRISM utilize collected failure data from the field and adopt constant failure rate with some factors to account for the environmental and operating conditions [79]. These traditional handbooks do not consider the root cause of failure or any uncertainty analysis, but rely purely on statistical methods. Due to heavy criticism, MIL-HDBK-217 was officially canceled in 1995 for reliability analysis by the Army. However, the usage of constant failure rate for reliability analysis is still popular. One of the reasons for its popularity could be due to the fact that the system level reliability prediction methods such as Fault-Tree Analysis (FTA) and state-space analysis are conventionally applicable only to constant failure rates [1]. Recent literature mentions that the latest revision of MIL-HDBK-217 shall also include the PoF based reliability analysis [80, 1].

An important assumption of the traditional reliability handbooks is the constant failure rate over the operational lifetime. Hence, the MTTFs are directly calculated irrespective of the knowledge of the exact application or mission profile of the system. Although this method is easier to use, it is considered incorrect for most practical applications [10, 81]. This is evident from the bathtub curve in Fig. 2.7 since the wear-out failures become dominant towards the end of useful life.

The PoF approach is based on the analysis of root-cause of failures and the effect of materials, stress, operating and environmental conditions on the product reliability [1, 10]. For a power electronic converter system, the failure mechanisms of each component are investigated and thereby the system failure is modeled as a combination of component level failure mechanisms. The failure mechanisms could also transcend component level to packaging level and Printed Circuit Board (PCB) level. Therefore, the PoF based failure mechanism model of a power electronics system can be complex and challenging. Hence, it is important to differentiate critical failure mechanisms and critical components for each application [1].

2.5.3 Lifetime Modeling of Power Semiconductor Devices

For industrial applications, it is necessary to know the relationship between the usage and failure of power electronic devices. Since the major failure mechanisms of power electronic

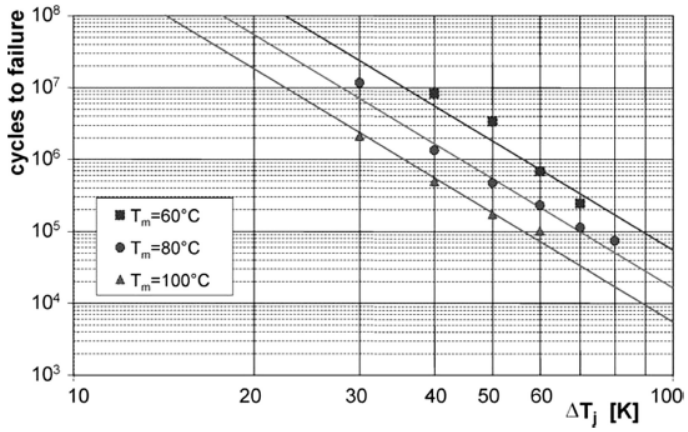


Figure 2.8: Power cycling results from LESIT [82].

modules are known from the power cycling studies, researchers have been deriving lifetime models from the power cycling tests, which mathematically establishes the relationship between thermal cycling and the number of cycles to failure. The project Leistungs Elektronik Systemtechnik und Informations Technologie (LESIT) was one of the first power cycling tests performed in the 1990s to identify the physics behind the failure of power modules [82]. In this test, modules were tested at different mean junction temperatures T_m and different thermal cycling amplitudes ΔT_j. The results of the LESIT tests are shown in Fig. 2.8 which illustrates the number of cycles to failure N_f for different ΔT_j and T_m. From the results, it is clear that the N_f has two dependencies; Coffin-Manson term which depends on the thermal swing and an Arrhenius term which is a function of the mean junction temperature. Based on the experimental data shown in Fig. 2.8, a lifetime model is derived as [83]

$$N_f = a_1 \cdot (\Delta T_j)^{a_2} \cdot e^{\frac{a_3}{T_{j,av}+273°C}}, \tag{2.6}$$

where a_1 and a_2 are the experimentally determined parameters which are related with the physical characteristics of the power module, whereas a_3 is a constant denoting the influence of the Arrhenius factor. The values of a_1 and a_2 used in this work are $3.025 \cdot 10^5$ and -5.039 respectively [35]. The constant a_3 is calculated by dividing activation energy ($\approx 0.8\,eV$) by the Boltzmann constant ($8.314 J/mol \cdot K$) [4]. Here, $T_{j,av}$ denotes the average junction temperature of the power semiconductor device.

Construction of power modules has undergone a lot of advances over the years which resulted in modifications to the lifetime model (2.6). The power cycling test conducted to derive the lifetime models can have different test conditions and module parameters which make the derivation of a single lifetime formula applicable for all the power modules a difficult task. To account for the various parameters during the power cycling tests, Bayerer *et.al*. has proposed a new lifetime model given by [11]

$$N_f = K_{Bayerer} \cdot (\Delta T)^{\beta_1} \cdot e^{\frac{\beta_2}{T_{low}+273°C}} \cdot {t_{on}}^{\beta_3} \cdot {I_{bond}}^{\beta_4} \cdot {V_{device}}^{\beta_5} \cdot {D_{bond}}^{\beta_6}. \tag{2.7}$$

Apart from the Coffin-Manson and Arrhenius terms, the on-duration of the power cycling

Table 2.3: Lifetime model benchmarking results for Wind-power application [85].

Lifetime model	Total consumed lifetime/year	Deviation [%]
Benchmark	9.22E-02	0
Coffin-Manson Arrhenius (2.6)	1.49E-01	62
Bayerer (2.7)	1.28E+01	13783

test t_{on}, the current per bond wire of the chip I_{bond}, the voltage range of the device V_{device} and the bond wire diameter D_{bond} are considered for the model derivation. The coefficients $K_{Bayerer}$, $\beta_1 - \beta_6$ are obtained experimentally [11]. However, the Bayerer model (2.7) is valid only for DBCs with Al_2O_3 substrates. It is worth noting that the model (2.7) is an outcome of pure statistical analysis, and therefore cannot be presumed as a physics-based failure model since the parameters are not physically independent [4].

Numerous lifetime models have been proposed in the literature by power module manufacturers and researchers, which essentially modify the Coffin-Manson-Arrhenius lifetime model (2.6) according to the test results. For the power modules with sintered chips and aluminum bond wires, a new lifetime model has been proposed in [84]. Even though there are many lifetime models available, it is important to know which lifetime model can be used for a particular application. Benchmarking of various lifetime models for MMC is investigated in [85]. The consumed lifetime of the IGBT modules for the MMC in wind-power application according to the manufacturer aging data has been compared with several models such as the Coffin-Manson-Arrhenius (2.6) and Bayerer model (2.7). The results are summarized for both the aforementioned lifetime models in Table. 2.3 [85]. The Bayerer model has resulted in a large deviation compared to the Coffin-Manson Arrhenius model for this particular application. This is due to the fact that the power-on time for the wind profile is in hours whereas the t_{on} time of the Bayerer model has a limited range. Therefore, the use of analytical lifetime models for the lifetime calculation need to be checked for relevancy in a particular application.

In this thesis, the Coffin-Manson-Arrhenius (2.6) lifetime model has been utilized to evaluate the lifetime of power semiconductor devices. Even though there are numerous lifetime models available, all other models are obtained through modifications of the Coffin-Manson-Arrhenius lifetime model. As described in [85], use of lifetime models with t_{on} may result in large errors if the thermal cycle on-time of the application and the employed model are not in agreement. Therefore, the lifetime model (2.6) has been chosen to prove the effectiveness of the reliability improvement algorithms.

2.5.4 Mission Profile Based Reliability Analysis

System level reliability prediction with conventional methods such as the FTA, Markov chain analysis etc. use constant failure rate of the system components [8, 1]. Over the past decades, PoF based failure mechanisms of power electronics components have been widely accepted as the de facto standard for reliability prediction. The PoF based component level failure

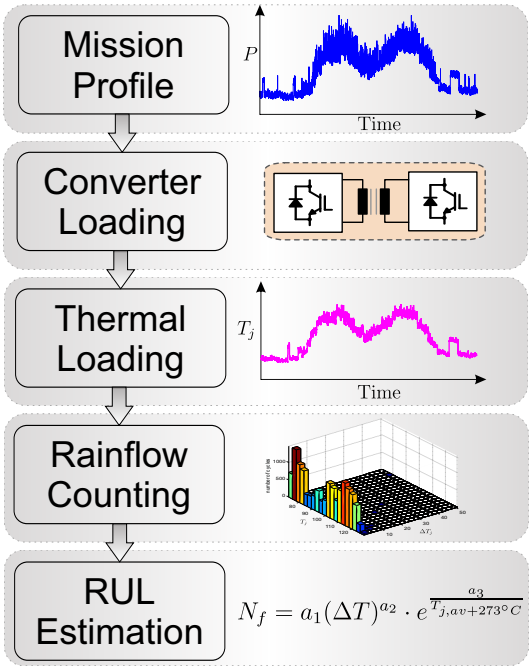


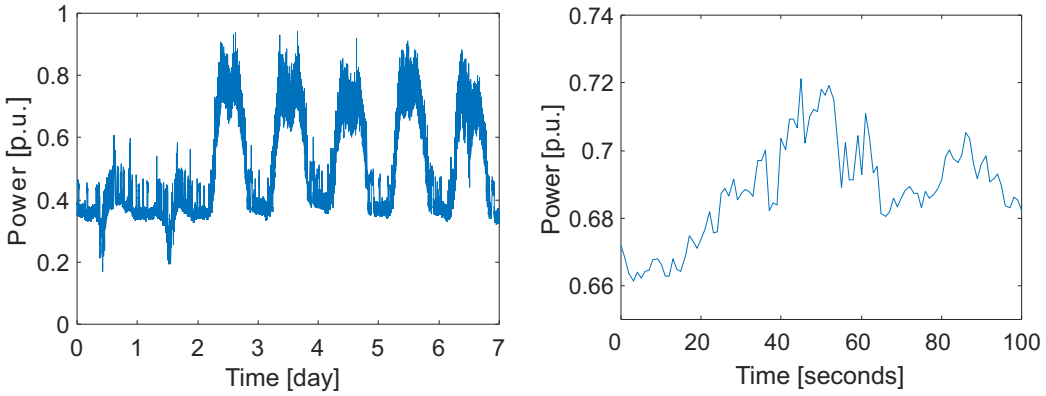
Figure 2.9: Method for estimating device wear-out from thermal cycling based on mission profile and PoF approach [C8].

mechanisms need to be translated into system level reliability prediction and this is accomplished through mission profile based reliability analysis [2]. In [86, 13], state-of-the-art for mission profile based reliability analysis of PV inverters and MMCs have been presented.

Steps involved in PoF and mission profile based reliability analysis is illustrated in Fig. 2.9. In order to analyze the lifetime consumption resulting from thermal stress based wear-out, a mission profile is considered to generate the working condition of the power converter. Depending on the mission profile, the thermal loading of the converter is obtained using an electro-thermal model of the system. Once the junction temperature fluctuations are known, the lifetime consumption is calculated using the cycle counting method and lifetime model of the power device. Steps necessary for the conversion of the mission profile into lifetime consumption are described in detail in the latter part of the section.

Mission Profile

Mission profile represents the operating/environmental conditions of the power electronics system and the relevant stress experienced during the expected life cycle which includes manufacturing, transportation, installation and operational phase [2]. However, it is often difficult to acquire the entire data for the expected life cycle, and therefore the reliability predictions are carried out by representative data. Mission profile parameters vary according to the application. In the case of renewable energy applications, wind profile or solar irradiance are the typical mission profile parameters. However, for an electric vehicle application, speed and torque profiles describe the operating condition of the system. Ambient factors such as temperature, humidity, vibration, etc. and the control algorithm to determine the voltage and currents in the power electronics components shall also be taken into account for



(a) (b)

Figure 2.10: (a) Grid mission profile for 7 days. (b) Grid mission profile for 100s. [89, 90].

accurate reliability evaluation [87]. In short, the mission profiles shall emulate the working condition of the electronics component in the field as close as possible.

In [88], a comparison of reliability analysis using military handbook MIL-HDBK-217 and IEC-TR-62380 standard for a PV application has been presented. Compared to the MIL-HDBK-217, the IEC-TR-62380 approach also considers the impact of mission profile into account. Nevertheless, the IEC-TR-62380 approach is not a pure PoF based method, but incorporates the impact of mission profile for the calculation of constant failure rate. Therefore, it is interesting to discuss the outcome of the study to highlight the importance of mission profiles for reliability prediction. Four converter prototypes with different power devices were investigated using the above-mentioned approaches. According to MH217, the power devices with the lowest on-resistance and better thermal impedance is the best reliable choice. The analysis using IEC-TR-62380 considering the PV mission profile shows that four power devices have similar failure rates even though they have different electrical and thermal parameters. The large difference in failure rates obtained from the two methodologies is due to the selection of influence factors for reliability prediction; MH217 has the component temperature as the largest contributing factor whereas IEC-TR-62380 considers thermal cycling as the prominent factor. In short, the investigation asserts the importance of mission profile to evaluate the reliability of power electronic components compared to the traditional pure statistics based reliability prediction methods [88].

For investigating thermal cycling based wear-out failures, it is the state-of-the-art practice to use mission profiles as the input to emulate the real working conditions of the power electronic system [79, 91, 86, 92]. The importance of mission profile based analysis lies on the fact that the electronics component stress is application dependent. Therefore, each design needs to be evaluated individually to ensure reliability and to avoid over-design. For example, if same inverter design criteria is used for two inverters operating predominantly at ambient temperatures $25°C$ and $100°C$ respectively, the latter will fail quickly and can adversely affect product reputation. On the other hand, designing all the power electronics inverters to withstand the worst-case operating conditions could be an over-design and costly solution for many applications. Therefore, understanding the mission profile of an

application is vital to ensure the desired reliability at a minimal cost.

For analysing the reliability of Smart Transformer converter topologies, mission profile of a smart grid system is considered [89, 90]. Since no real field data from ST is available yet, and ST is mainly designed to cater distribution grid, the data from a smart grid is found to be the closest match to the mission profile for ST. Fig. 2.10 (a) shows the normalized active power in one of the phases of a smart grid for 7 days. It can be seen that the weekend power consumption is different from the rest of the week as indicated by the first and second day profile. The smart grid data is recorded with a sampling rate of $1\,s$ and the power variation for a period of $100\,s$ is illustrated in Fig. 2.10 (b). For analysing grid-connected modular converter topologies, the mission profile in Fig. 2.10 is utilized. The resolution of the mission profile plays an important role while translating the mission profiles to junction temperature profiles, which is covered later in this section.

Power Electronics Circuit Modeling

As shown in Fig. 2.9, the mission profile is applied on a converter model following state-of-the-art practices [91, 86]. Since the mission profile can have timescales ranging up to years, the power electronics converters need to be modeled for simulating the converter loading. From the converter model, the power loss in each component is calculated and then converted into thermal loading with the help of electro-thermal models of power devices assembled on the heatsink. The modeling of the converters is state-of-the-art and hence it is not attempted to give a detailed description of power converter system modeling in this section. However, all the converter models used in this work namely inverter, CHB and DAB topology models are presented in A. The approach used in this work for modeling the power device loss from the mission profile is discussed in the following part.

Power Semiconductor Loss Modeling

The semiconductor device losses can be generally classified into conduction and device losses while neglecting the driver losses and losses due to leakage current. In this thesis, the loss calculation with the analytical averaged method and numerical circuit simulation method are presented and compared.

When the semiconductor device is used as a switch, the conduction losses incur when the device is in on-state. For IGBT, the conduction losses ($P_{cond,IGBT}$) at any time instant t is calculated by multiplying the on-state voltage drop across the collector and emitter terminals, $V_{ce}(t)$, with the current flowing through it, termed as the collector current, $i_c(t)$, given by

$$P_{cond,IGBT}(t) = V_{ce}(t) i_c(t). \tag{2.8}$$

Average conduction loss modeling When the device voltage and current waveform are periodic signals, as is the case with most of power electronic applications, the simplest method is to calculate the average conduction loss ($P_{cond,IGBT,avg}$) for the period T using

$$P_{cond,IGBT,avg} = \frac{1}{T}\int_0^T V_{ce}(t)i_c(t)dt. \tag{2.9}$$

For the anti-parallel diode across the IGBT, V_f is the forward voltage drop and i_f is the forward current flowing through it. Similar to the IGBT, the average conduction losses for the diode ($P_{cond,diode,avg}$) is computed by

$$P_{cond,diode,avg} = \frac{1}{T}\int_0^T V_f(t)i_f(t)dt. \tag{2.10}$$

Usually, in the device datasheets, the on-state voltage drop V_{ce} of the IGBT and the forward voltage drop V_f of the diode are given as the function of the current flowing through the device and the junction temperature. Therefore, in order to include these dependencies, the conduction loss is modeled using polynomial fits as described in [93]. The characteristic curve of the voltage drop is multiplied by the corresponding device current at the given temperature to obtain the instantaneous conduction losses as a function of the current. Using a linear relationship between the polynomial fits for conduction losses at different junction temperatures given in the datasheet, the junction temperature dependency is also taken into account for the loss calculation.

Considering the on-state voltage drop dependency on device current and junction temperature, the average IGBT and diode conduction losses are calculated as follows:

$$P_{cond,IGBT,avg} = \frac{1}{T}\int_0^T P_{cond,IGBT}(i_c(t),T_j)dt \tag{2.11}$$

$$P_{cond,diode,avg} = \frac{1}{T}\int_0^T P_{cond,diode}(i_f(t),T_j)dt \tag{2.12}$$

Conduction loss modeling with numerical simulation The averaged loss calculation of power devices is popular for analysing the power converter efficiency and cooling system design [35]. However, for accurate electro-thermal modeling and analysis, the averaging of the losses may cause a loss of information. Accurate loss calculation of the power devices can be performed using an electronic circuit simulation environment using the device physical models available from the manufacturer or from experimental measurements [94]. However, these simulations are computationally demanding and are not suitable for simulating the operation of a power electronic converter for hours, days, or even more.

In this thesis, loss modeling with a numerical simulation is performed to improve the accuracy of the electro-thermal modeling. The instantaneous current through the device (i_{device}), either IGBT or diode and the device junction temperature (T_{device}) are fed to the polynomial fit of the device conduction losses as illustrated in Fig. 2.11 to compute the device instantaneous conduction losses ($P_{cond,device}$) [93].

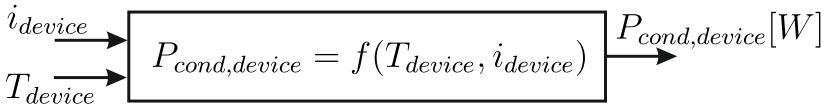


Figure 2.11: Scheme for numerical calculation of conduction losses.

When the semiconductor switch is turned on or off, losses occur in the device due to non-ideal characteristics of the device. In an ideal switch, when the device is turned on, the current instantaneously starts flowing and the voltage across the switch becomes zero. However, in real devices, during turn-on the current does not instantaneously achieve the required value, and the device voltage does not drop to zero as well. Depending on the nature of the load and commutation characteristics attributed to the topology, switching losses occur in the device. In case of hard switching, the voltage and current overlap during the switching process, leading to higher losses and device stress.

For the computation of the switching losses, the turn-on (E_{on}), turn-off (E_{off}) energies of the IGBT and the diode recovery energy (E_{rec}) are usually given in the device datasheets. The switching energy depends on various factors such as the voltage across the switch, the current flowing through it, junction temperature, parasitics in the circuit, and the gate bias parameters. Neglecting the effect of circuit parasitics and assuming that the gate bias parameters are constant, the switching energy can be described as a function of the IGBT collector-emitter voltage V_{ce}, junction temperature T_j and collector current I_c using polynomial fit [93]. The switching energy loss for one switching cycle is given by

$$E_{sw,igbt} = E_{\text{on}}\left(V_{\text{ce}},I_c,T_j\right) + E_{\text{off}}\left(V_{\text{ce}},I_c,T_j\right). \tag{2.13}$$

Average switching loss modeling The average switching losses ($P_{(\text{sw,igbt})}$) of the IGBT during hard switching is given as [93]

$$P_{\text{sw,igbt,avg}} = \frac{1}{T}\left(\begin{array}{l} \sum_{n=1}^{N_{\text{sw}}} E_{\text{on}}\left(V_{\text{ce}},I_c,T_j\right) \\ +\sum_{n=1}^{N_{\text{sw}}} E_{\text{off}}\left(V_{\text{ce}},I_c,T_j\right) \end{array} \right), \tag{2.14}$$

where N_{sw} is the number of switching instants of the IGBT for the time interval T, V_{ce} is the collector-emitter voltage, I_c is the current flowing through the IGBT and T_j is the IGBT junction temperature.

The average reverse recovery diode losses ($P_{\text{rec,diode,avg}}$) is expressed as

$$P_{\text{rec,diode,avg}} = \frac{1}{T}\left(\sum_{n=1}^{N_{\text{sw}}} E_{\text{rec}}\left(V_{\text{f}},I_f,T_d\right) \right). \tag{2.15}$$

In equations (2.14) and (2.15), the switching energies are averaged over the fundamental period T and multiplied by the number of switching events to obtain the average switching losses.

To reduce the switching losses, soft switching is employed by making one electrical param-

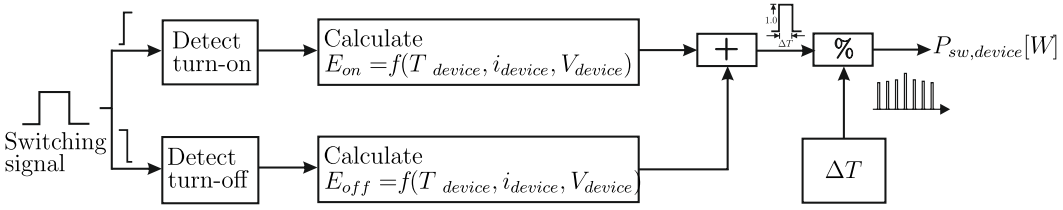


Figure 2.12: Scheme for calculating switching losses with numerical simulation.

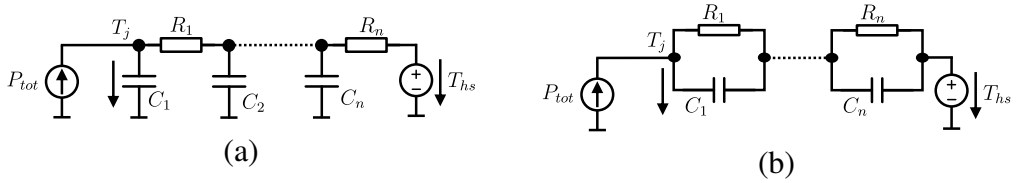


Figure 2.13: Equivalent thermal network (a) Cauer model (b) Foster model.

eter such as voltage or current to zero before the switching action. When the voltage across the switch is made zero before switching, usually using the conduction of the anti-parallel diode, it is termed Zero Voltage Switching (ZVS) [95]. Another type of soft switching known as Zero Current Switching (ZCS) can occur when the current flowing through the switch becomes zero before turn-off or when the rise of the current is delayed by a series inductor while turn-on [96]. Thus, the switching losses are considerably reduced and can be neglected for loss calculations. Hence, it is critical to differentiate between soft and hard switching while performing loss calculations.

Switching loss modeling with numerical simulation In contrast to the averaged switching loss calculation, in the case of numerical loss modeling, the switching losses are not averaged for the fundamental period. The method of numerical switching loss modeling is illustrated in Fig. 2.12. For each switching cycle, the turn-on and turn-off losses are calculated from the curve-fitted polynomial functions. The advantage of calculating the turn-on and turn-off separately compared to [93] is the straightforward inclusion of soft turn-on/off if applicable. After computing the switching energy for a switching instant, it is multiplied with a unit pulse having a width of ΔT and is divided with the pulse-width ΔT as shown in Fig. 2.12 to obtain the switching power loss. The power loss is independent of the selected pulse width ΔT [93]. The advantage of loss modeling with numerical simulation compared to that of averaged loss modeling is explained later in this section.

Thermal Network Modeling

The thermal network modeling of the power semiconductor switches is a challenging topic for lifetime evaluation. Mostly followed approaches for modeling of the thermal impedance fall into two categories, namely Finite Element Method (FEM) based modeling and heating/cooling curve based model extraction [91, 97]. Since the heat flow in a power device is three-dimensional, it is quite challenging to extract precise models in a system with multiple heat sources adjacent to each other. With knowledge of the material properties in power

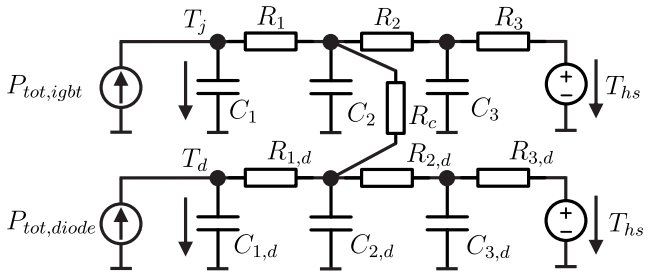


Figure 2.14: Typical equivalent thermal network of thermally coupled IGBT and diode in a power module [93] .

electronic modules, FEM based models can simulate the thermal dependencies of the various physical layers in a typical device assembly shown in Fig. 2.2 [98, 35]. However, power module manufacturers usually do not provide the exact material properties which makes the simulation studies challenging. To model the temperature hotspots at different layers in power modules such as the junction, solder joints, or DBC, a Cauer thermal network is used. Depending on the physical layers and temperature hotspots, n^{th} order Cauer network is modeled which consists of a combination of thermal resistances ($R_i, i \in [1,n]$) and capacitances ($C_i, i \in [1,n]$) as shown in Fig. 2.13 (a) [98].

Either from FEM simulation or experimental thermal step response, when a thermal impedance curve is available, an equivalent thermal network can be obtained by a Foster model consisting of thermal resistances and capacitances by curve fitting as shown in Fig. 2.13 (b). The Foster model does not have any direct physical relationship to the temperature flow in the power electronics assembly. The thermal impedance of the Foster network in Fig. 2.13 (b) can be mathematically represented as

$$Z_{th,jhs} = \sum_{i=1}^{n} R_i \left(1 - e^{\frac{-t}{R_i C_i}}\right), \tag{2.16}$$

where t denotes time.

To incorporate the influence of thermal coupling between the IGBT and the anti-parallel diode in a power module, a coupled thermal network can be used as described in [93]. Such a model can be obtained from FEM studies. In a power module, the IGBT die and the diode die are soldered to the DBC very close to each other. The thermal coupling through the DBC between IGBT and diode is represented by a thermal resistance R_c as shown in Fig. 2.14 [93].

The junction temperature T_j of the device at time t is calculated from the losses and the thermal model as

$$T_j(t) = Z_{th,jhs} * P_{tot}(t) + T_{hs}(t), \tag{2.17}$$

where $Z_{th,jhs}$ is the equivalent impedance of the Foster network, $*$ represents convolution, P_{tot} is the total losses in the device comprising switching losses and conduction losses, and T_{hs} is the heatsink temperature.

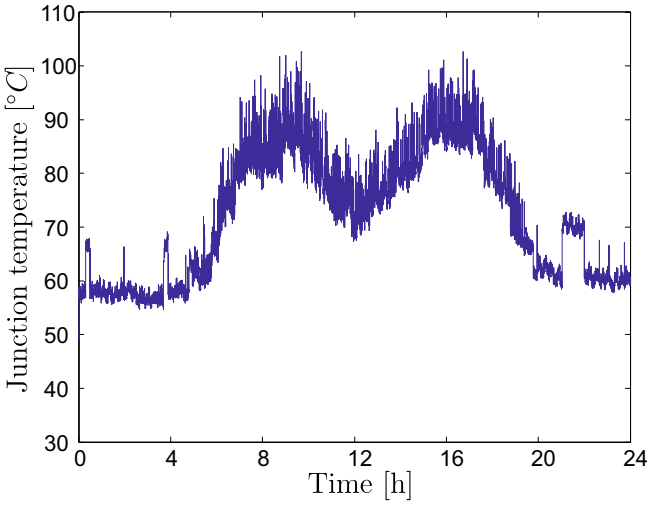


Figure 2.15: Junction temperature profile for a day.

Table 2.4: Simulation parameters of CHB converter.

Parameter	**Value**
Grid voltage (rms), V_g	$1.1kV$
Power rating, P_{rated}	$60kVA$
Line inductance, L_g	$6.8mH$
Number of cells, N	3
Cell DC-link voltage, $V_{DC,i}$	$800V$
Switching frequency, f_{sw}	$5kHz$

Table 2.5: Thermal network parameters [99].

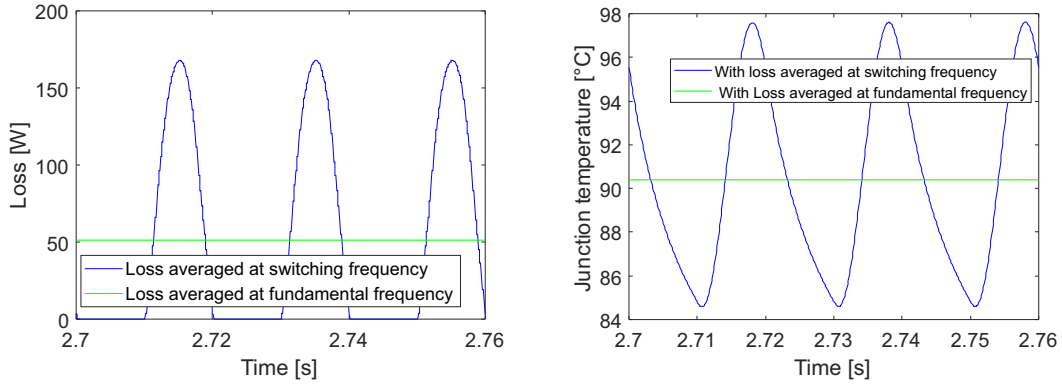
IGBT		Diode	
R_i $[K/W]$	C_i $[J/K]$	$R_{i,d}$ $[K/W]$	$C_{i,d}$ $[J/K]$
0.09025	0.026	0.1375	0.024
0.3612	0.0781	0.888	0.0385
0.2031	0.5554	0.2558	0.5062
0.1403	2.010	0.0810	9.4593

As discussed in [87], the power electronics system has multiple timescales of device loading which makes the translation of mission profile to device-stress difficult. The timescales in a thermal profile can be classified into short, medium, long and very long time scales.

- Very long time scale (range: months to years) includes the temperature fluctuations owing to seasons and environmental changes over the years. The exact replication of these variations in the mission profile is challenging.

- Long time scale (range: days to weeks) temperature variations are typically caused by the change in the consumption behavior over the days and weeks and environmental factors. This is evident in Fig. 2.10 (a) where the power consumption over weekdays and weekends are different. The power consumption changes over the week could be applicable for many sectors such as industrial drives or traction applications. Therefore, to make the lifetime analysis more accurate, these long time scale temperature variations shall be considered.

- Medium time scale (range: minutes to hours) variations in junction temperature consist of the power consumption or generation variations in the range of minutes to hours. Fig. 2.10 (a) shows the variation of a typical grid profile having the peak power consumption during morning and evening. The junction temperature variation of a grid-connected converter for a typical day is shown in Fig. 2.15 which gives an indication



a b

Figure 2.16: (a) IGBT losses with averaged and numerical simulation models (b) IGBT junction temperature with averaged and numerical simulation models.

of the low frequency temperature variations over the minutes and hours.

- Short time scale (range: milliseconds to seconds) fluctuations in the temperature are usually caused by the fundamental frequency of the converter and sudden changes in load/generation. To demonstrate the significance of the short time scale temperature variations due to fundamental frequency, a simulation study is performed with a grid-connected CHB converter having 3 cells with $1200V$ IGBT modules *FP25R12KT3* [99]. Simulation parameters of the CHB system and the equivalent thermal network parameters of the IGBT module are given in Table 2.4 and Table 2.5 respectively. IGBT loss calculation is performed with an averaged model at fundamental frequency and numerical simulation models (see Section 2.5.4 for details). The result is presented in Fig. 2.16 (a). To demonstrate the impact of the loss modeling method on short time scale temperature fluctuations, the junction temperature of the IGBT is calculated with averaged loss model and using a numerical simulation model. A comparison of the junction temperatures with loss averaged at the fundamental frequency ($50Hz$) and numerical simulation is illustrated in Fig. 2.16 (b). With averaging of losses at fundamental frequency, these high frequency temperature fluctuations are ignored. In this work, the short time scale temperature cycling is included with the help of numerical simulations of device losses.

Cycle Counting and Miner's Rule

The thermal profiles as illustrated in Fig. 2.15 consist of various stress cycles resulting from a range of thermal cycles with different thermal swings and mean temperatures. However, the lifetime models obtained through power cycling tests can consider only one thermal cycle with a mean temperature and cycle amplitude at a time as indicated by (2.6). Therefore, cycle counting algorithms are required to count thermal cycles in a thermal profile so that the lifetime model can process each thermal cycle separately [79].

There are several cycle counting methods available for lifetime estimation such as peak counting, level counting, simple range counting and rainflow counting [100, 101]. In [101], a

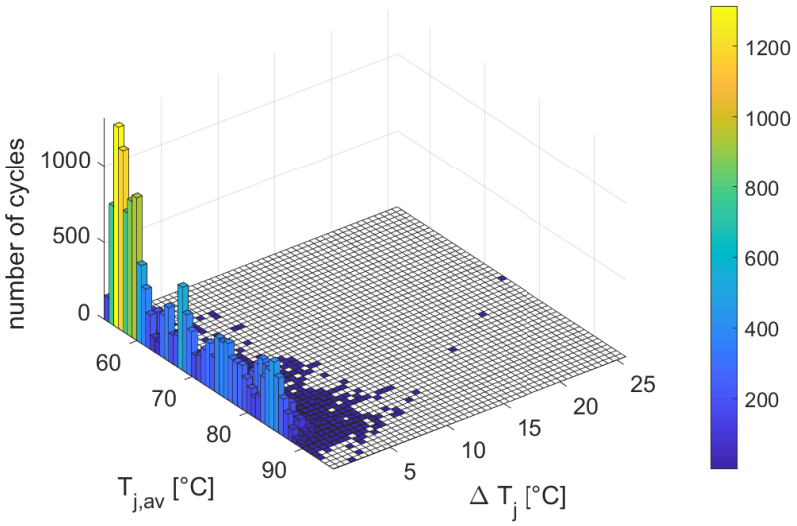


Figure 2.17: Result of rainflow counting algorithm of the thermal profile in Fig. 2.15.

comparative study of the temperature cycle counting methods such as rising edge, half-cycle, maximum edge and rainflow counting were performed with Finite Element Method (FEM) simulation. It is demonstrated that the rainflow counting algorithm provides higher accuracy than the other algorithms. Rainflow counting is one of the most commonly used cycle counting method to identify the stress levels of power electronic devices [102, 103]. It is a statistical method to model the stress strain behavior of the material. Each cycle is defined by a closed hysteresis loop which has an amplitude and a mean value. From the thermal profile, rainflow counting algorithm extracts the statistics of the thermal cycles including the type and number of thermal cycles. Fig. 2.17 illustrates the result of rainflow algorithm applied to the thermal profile shown in Fig. 2.15. The mean value and the amplitude of the thermal cycles are shown on the X and Y axis respectively, whereas the Z axis represents the number of cycles.

Once the necessary input (cycle amplitude and mean value) for the thermal model (2.6) is obtained using the rainflow algorithm, the total number of the cycles to failure of the power device is calculated. The total wear-out of the power device resulting from the thermal profile is calculated using the Miner's rule [104] as given by

$$D_{acc} = \sum_i \frac{N_i}{N_{fi}}, \tag{2.18}$$

where D_{acc} is the accumulated damage, N_i is the number of cycles to failure in the stress range i and N_{fi} is the durability of the i-th stress range. According to the Miner linear accumulation damage theory, when the accumulated damage becomes 1, the device is said to be failed. The Remaining Useful Lifetime (RUL) of a power device at any point in time is defined as

$$\text{RUL} = 1 - D_{acc}. \tag{2.19}$$

The use of linear accumulated damage is still a topic of interest in power electronics. In

[105], superimposed power cycling tests are performed on power modules with different stress levels to validate the linear accumulation of damage. The test results show that the expected lifetime from the model with linear damage accumulation and that from the superimposed power cycling tests are in agreement. The major failure mechanism for these power cycling tests was bond-wire cracks. Another combined power cycling tests with different stress conditions are performed in [106] on IGBT modules to verify the linear accumulation of damage. The study verifies the linear accumulation of damage and the failure mechanism was bond-wire cracking. However, it is worth noting that the accumulation of damage can be non-linear when different failure mechanisms such as solder fatigue and bond-wire cracks act together to accelerate the aging process [106, 83]. In this work, the state-of-the-art linear damage accumulation method is followed.

Limitations of Mission Profile based Reliability Prediction

Before concluding the section, it is worth discussing the limitations of mission-profile based reliability prediction followed in this thesis [2].

- The thesis mainly focuses on wear-out based failure mechanisms and other failures due to vibration, environmental contamination or cosmic rays are not covered. Hence, the reliability prediction is not comprehensive since only limited failures are investigated.
- The damage accumulation is assumed to be linear as given by (2.18). But it is still unclear whether this assumption is valid over the lifetime of the system [106, 83].
- The system level reliability analysis with PoF based mission profile analysis needs to be investigated more deeply. The interconnection of different failures on system level is usually neglected in most studies [13]. However, failures can be more complex and are interconnected on system level.

2.6 Monte-Carlo based Reliability Analysis

As mentioned in the previous sections, traditional system level reliability prediction is carried out using handbooks such as MIL-HDBK-217which relies on constant failure rate. However, this methodology of reliability prediction is discouraged through the cancellation of MIL-HDBK-217F in 1995. The PoF based lifetime models are used to predict the reliability of power electronics systems which are obtained through accelerated power cycling tests. These lifetime models are also obtained through statistical analysis of the power cycling data and hence contain some uncertainties due to the fitting factors and adopted test conditions [11, 107].

After estimating the number of cycles to failure of the power device resulting from a certain mission profile, further reliability assessment is necessary to efficiently utilize the obtained result. This is required due to the following reasons:

- There are uncertainties and parameter deviations in the converters operating on the field compared to the simulated converter models. The power devices, capacitors, passive and active electronic devices, etc. have manufacturing tolerances that are not easy to consider in the simulation models [108].

- Deviations in the lifetime models owing to the variations in the power cycling test conditions and curve fitting parameters [11].

- The complexity of the power electronic systems demands system level reliability evaluation considering possible uncertainties and variations on system level.

- Mission profiles considered for evaluating the reliability of a system is a representative of the stresses experienced by the converter. However, it is almost impossible to generate a mission profile representing the exact working condition for a particular application over the lifecycle. Hence, the impact of possible variations in the mission profile on the field needs to be considered for a comprehensive reliability prediction.

There is still a lack of investigation regarding the impact of electrical and thermal parameter variations in IGBT on the lifetime model [107]. One of the popular technique to include variances into consideration is the Monte-Carlo method. Monte-Carlo simulations are state-of-the-art in reliability prediction [7, 108, 107, 109, 110, 111]. In [109], the variations in the geometry of the IGBT module is considered with Monte-Carlo simulations. The variations in the mission profile is analyzed through Monte-Carlo simulations in [111]. The lifetime model fitting coefficients are considered as Gaussian distributions with $3\sigma = 0.05$, where σ denotes the standard deviation of the Gaussian distribution. This implies that the curve fitted parameters with $\pm 5\%$ tolerance band are modeled as normal distributions with 99.7 % confidence. Subsequently, the lifetime is derived as a probabilistic function with the Monte-Carlo method [108]. Monte-Carlo method can be considered as the state-of-the-art for system level reliability analysis with PoF based lifetime models [111].

A general scheme of Monte-Carlo simulation for a modular converter system followed in this thesis is graphically represented in Fig. 2.18 [107]. In Monte-Carlo analysis, the desired parameter variations are modeled as probability distributions and the results are simulated for a very large number of samples. When the simulations are performed with a large enough sample size, the results converge to an expected value. The input for the Monte-Carlo simulation is the mission profile and the required parameter variations. The parameter variations include all the factors with uncertainty in the evaluated system such as in lifetime model, power device manufacturing tolerances, or ambient conditions. For each input set, the simulation outputs the remaining useful lifetime following the methodology described in Fig. 2.9. In Monte-Carlo analysis, the simulation is repeated for a sufficiently large number of times, denoted as r cases, for r sets of inputs.

The process of system level reliability evaluation is graphically illustrated in Fig. 2.18. In a modular system, each converter cell has an RUL probability distribution and this is converted into an unreliability curve at the converter level. Finally, a system level unreliability/CDF is

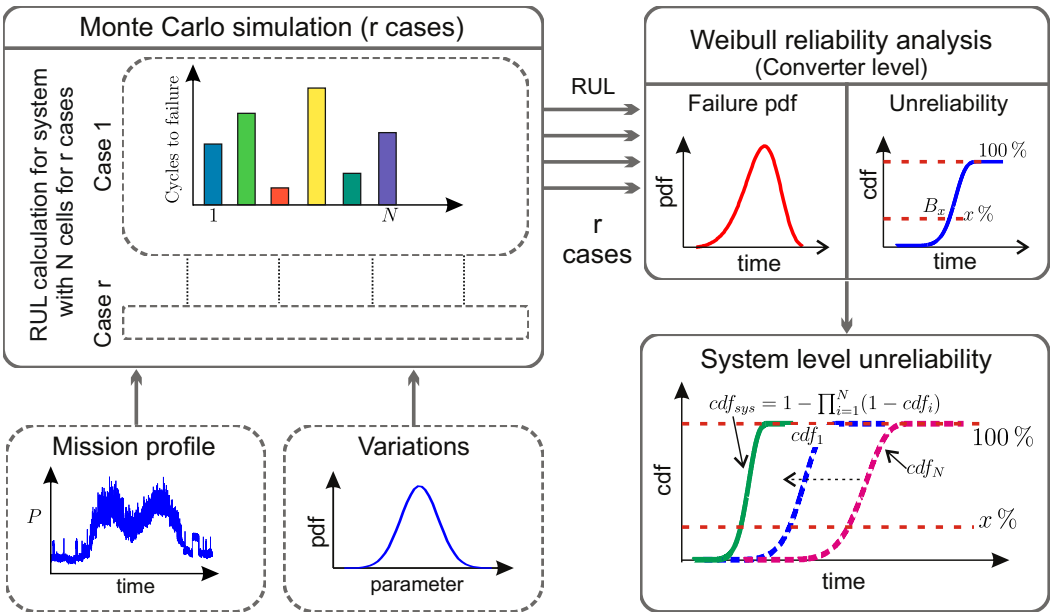
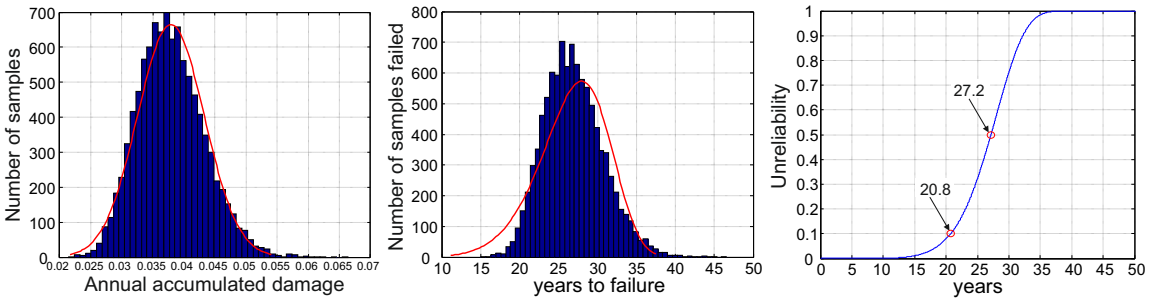


Figure 2.18: Monte-Carlo reliability analysis of a modular converter system.



(a) (b) (c)

Figure 2.19: Monte-Carlo analysis considering the parameter variations of lifetime model (a) Annual accumulated damage (b) Time to failure (c) Unreliability [C5].

expressed as

$$CDF_{sys} = 1 - \prod_{i=1}^{N}(1 - CDF_i), \tag{2.20}$$

where CDF_{sys} denotes the system level CDF and CDF_i indicates the CDF of a cell i.

Following the state-of-the-art methodology, the impact of lifetime model fitting parameter variations is analyzed with Monte-Carlo simulations. [107, 108]. The lifetime models in (2.6) are obtained from the accelerated lifetime tests with a certain number of sample devices and the obtained experimental data is curve fitted to derive the relationship between lifetime and thermal stress [82, 11]. This implies that there is a degree of uncertainty in the derived parameters and hence the calculated lifetime is not a single deterministic value. The device-dependent parameters a_1 and a_2 are curve fitted variables from the power cycling tests [82]. Assuming that these parameters have 5 % tolerance, they are modeled by Gaussian distribution considering that $3\sigma = 0.05$, following the state-of-the-art methodology [107, 108, 112].

The impact on the lifetime while considering these parameter variations is demonstrated using a Monte-Carlo simulation of 10000 samples in a modular converter system with 10 Dual Active Bridge converter cells is illustrated in Fig 2.19(a)-(c) [30]. The number of samples for the Monte-Carlo simulation is chosen to keep a minimum of 90 % confidence interval [107]. Annual accumulated damage from the Monte-Carlo simulations is shown in Fig 2.19 (a). Fig 2.19 (b) shows the estimated lifetime of the samples which can be approximated by a Weibull distribution. Subsequently, unreliability or cumulative percentage of failure can be calculated using the Weibull distribution parameters as in Fig 2.19 (c), and can be noted that 10 % of total cells are predicted to fail at 21 years and 50 % at 27 years. Rather than expressing the lifetime of the power converter by a single value, B_x lifetime can be obtained from the unreliability curve shown in Fig 2.19 (c) where x denotes the percentage of samples failed.

3 Modular Power Converters: Applications and Graph Theory Representation

This chapter focuses on the modular power converter topologies for the Smart Transformer and More Electric Aircraft (MEA) applications. As a prerequisite for the development of intelligent control algorithms in modular power converters, a novel approach for the representation of the modular power converters is proposed using graph theory. The graph theory representation forms the basis of power flow management solutions for improving the reliability and efficiency of modular converters. Starting with the review of modular power converter topologies for the Smart Transformer, traction and MEA applications, the fundamentals of graph theory and systematic modeling of power converters with graph theory are discussed. The proposed graph theory representation of modular converters in [J5] and [C6] forms the basis of this chapter.

3.1 Review of Modular Power Converters

The significance of modular power converters has escalated drastically in various applications such as electrical power distribution, industrial motor drives and more electric aircraft [113, 96]. Today, MMC is popular in high voltage systems owing mainly to the excellent power quality, the simple realization of redundancy, lower device losses and smaller filter size. In energy distribution applications, power electronics based modular Smart Transformer is gaining popularity due to their ability to offer a myriad of grid services [6]. Modular converter systems have already been proposed for traction, electric ships and MEA for achieving higher redundancy and availability [114, 96].

The rapid penetration of modular power converters can be attributed to a number of defining qualities such as reduced dv/dt, improved power quality, cost-effectiveness, easy maintenance and higher redundancy. For instance, in HVDC applications, modular converters made up of a large number of individual converter cells are considered to be cost-effective due to scalability [24]. In such systems, maintenance is easier, since only the individual faulty cells are replaced in case of failure. Furthermore, redundancy is achieved by simply adding additional cells. When modular multilevel topologies such as MMC and Cascaded H-bridge (CHB) converters are utilized, the voltage across the individual converter cell can be controlled, thereby ensuring voltage balancing across the power electronic devices. Instead, if series connected power electronic devices are used, complex gate drivers and additional components are necessary to ensure a safe operating voltage across the devices. Some of the most popular modular topologies in the Smart Transformer and DC-DC conversion applications relevant to MEA are described in detail as follows.

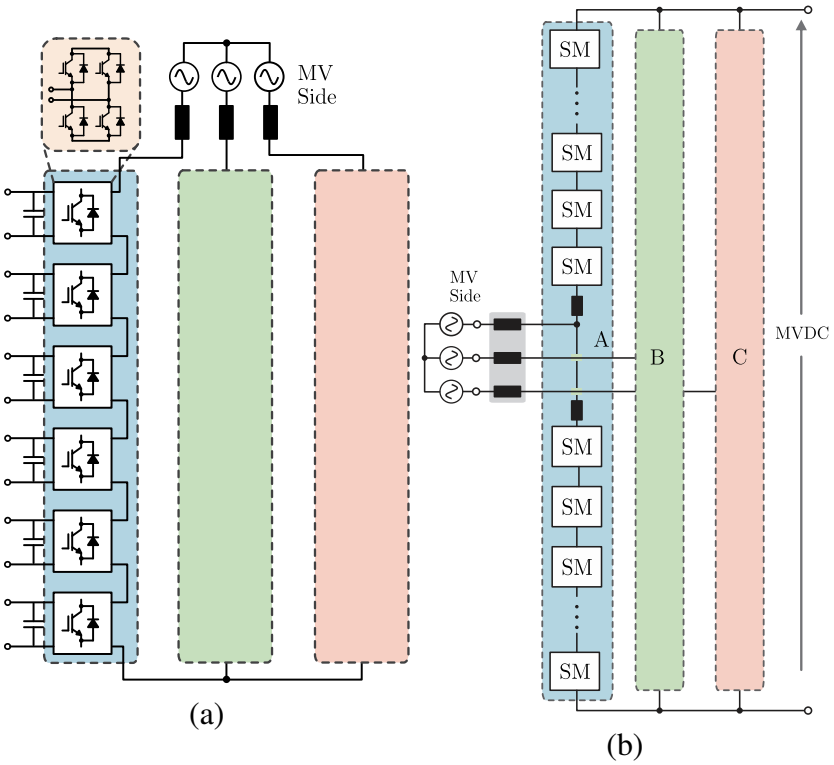


Figure 3.1: (a) CHB converter (b) Modular Multilevel Converter [C6].

3.1.1 CHB

The CHB multilevel modular converter topology was first introduced in [115] and almost a decade later, started receiving more popularity and attention [116, 117]. The CHB converter originates from the cascaded connection of the H-bridges as shown in Fig. 3.1 (a). Each phase consists of a series connection of H-bridges and the neutral point is obtained by the star connection of the converter cells 3 phases as illustrated in Fig. 3.1 (a). Each H-bridge cell can produce an output voltage of $+V_c$, 0 and $-V_c$, where V_c represents cell voltage. Therefore, for the phase to neutral connection, a connection of N cells results in $2N+1$ voltage levels and for the phase-to-phase connection, $4N+1$ voltage levels are obtained. Each H-bridge cell in a CHB provides an isolated DC source. Thus, when the CHB is connected to the MVAC grid, the DC-link voltage is distributed among the H-bridge DC-link capacitors, which act as an isolated DC source. The absence of a common DC-link is one of the main features of the CHB topology. The main characteristics of the CHB topology are summarized as follows.

- Simple construction based on the series connection of H-bridges
- The required blocking voltage of the power semiconductor device is limited by the DC-link voltage of a cell
- Easier addition of redundancy by increasing the number of cells
- No common DC-link available

- Shares common features of cascade-connected modular topologies such as better voltage/power quality, reduced filter requirements, lower Electromagnetic Interference (EMI) and potential device loss reduction.

3.1.2 MMC

MMC topology started gaining importance as a topology suitable for high voltage applications at the beginning of the 2000s [17, 18]. MMC can be seen as a modified CHB with the availability of a common DC-link. The DC-link connection is obtained by a double star configuration of CHB legs as shown in Fig. 3.1 (b). Each submodule (SM) of the MMC can be a half-bridge, full-bridge or any other custom topology. The most commonly used submodule topology is the half-bridge topology. When the load is connected, DC current flows through it. The DC current sums up to the AC currents in the arms, which form the circulating current, and does not reflect in the input AC current which is purely sinusoidal. The main characteristics of the MMC topology are summarized as follows.

- Voltages in the arm of the MMC are homopolar and generate a unipolar phase to neutral voltages. Therefore, the MMC requires twice the number of cells per arm compared to the CHB to operate under given DC and AC voltages. In total, four times the number of cells of a CHB topology is required for an MMC.
- For the basic cell or submodule, the voltage produced must be bipolar in the case of a CHB and hence a full bridge is necessary. Since MMC requires only a unipolar voltage at the cell level, half bridge topology can also be used. This decreases the number of components.
- Availability of an MV/HV DC-link.

3.1.3 Modular Dual Active Bridge Topologies

Dual Active Bridges (DAB) are featured as an ideal candidate for modular converter architectures in several applications [118]. DAB is a DC-DC converter with galvanic isolation and has a symmetrical structure with two H-bridges connected through a high frequency transformer. It offers many advantages such as high power density, soft switching, simple control structure and bidirectional power transfer capability. The bidirectional power flow capability enables the use of DAB when active loads are present, and the simplest and most popular control technique is the phase-shifted modulation. Each full bridge is switched with a constant 50 % duty cycle to generate high frequency square waves on the primary and secondary winding of the transformer. Utilizing the leakage inductance of the transformer, the square wave voltages are phase shifted to control the power transfer between the H-bridges. Simply by changing the sign of the phase shift, bidirectional power flow between the primary and secondary of the transformer is achieved [19]. Although there are several isolated

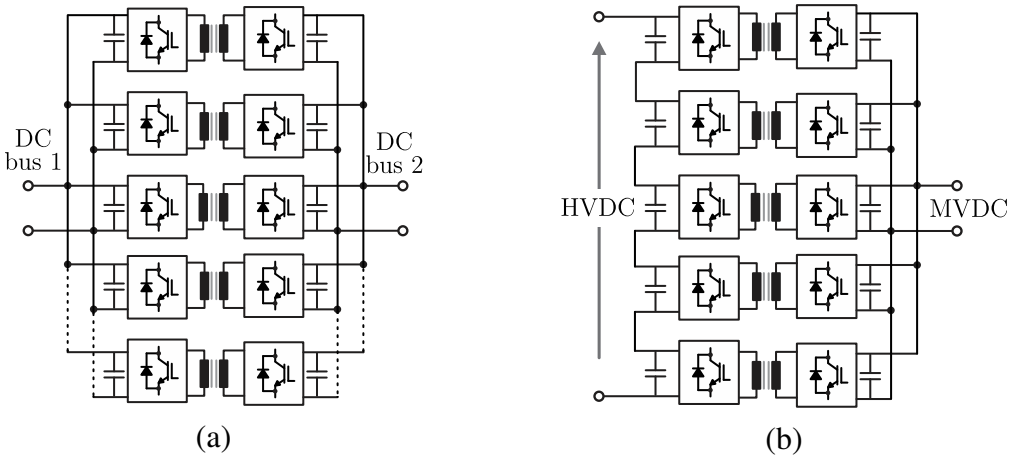


Figure 3.2: (a) Modular DAB in IPOP configuration (b) Modular DAB in ISOP configuration [C6].

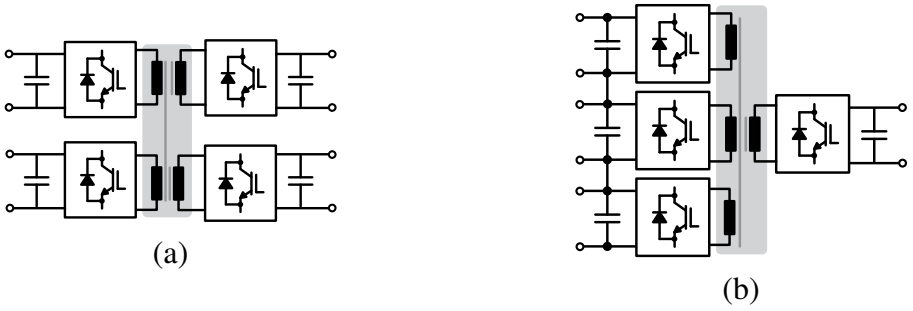


Figure 3.3: (a) Symmetrical QAB configuration (b) Unsymmetrical QAB configuration.

DC-DC converters, DAB is widely popular in modular converters mainly due to its symmetric structure and simple control requirements. Comparison of DAB with other topolgies are presented in [119, 120].

A modular DAB converter architecture for the interconnection of the HVDC and MVDC grid has been proposed in [121]. It is shown that the modular DAB converter is able to achieve very high efficiencies up to 99.2 % [120]. Input Parellel Output Parallel (IPOP) modular DAB converter architecture shown in Fig. 3.2 (a) is suitable to achieve very high current rating. An exemplary Input Series Output Parallel (ISOP) DAB architecture for connecting HVDC and MVDC grids is shown in Fig. 3.2 (b). For SST and ST applications connecting MVDC and LV grids, it is imperative to provide galvanic isolation between the grids, and therefore, isolated DC-DC converter topologies such as DAB and multiple active bridges are preferred. Moreover, the usage of high frequency transformer in DAB reduces the overall size of the power electronics based transformers.

3.1.4 Multiple Active Bridge Topologies

Multiple Active Bridge (MAB) topologies can be seen as an extension to the DAB topology with a coupled transformer. As the name suggests, MAB has multiple active bridges, and as an example, Quadruple Active Bridge (QAB) having four H-bridges coupled by a single

transformer is shown in Fig. 3.3. The motivation for the development of MAB topologies was primarily governed by the inability of DAB to cater to a wide input voltage range without sacrificing soft switching. Therefore, multi-port active bridges were proposed to cater to multiple loads while maintaining soft switching properties [95]. QAB is a special case of MAB and it has been very popular in the SST/ST applications [122, 123, 124]. In the SST applications, a clear advantage of using MAB topology is the integration of several sources with minimum conversion stages resulting in a higher power density. In the case of Smart Transformer, QAB topology enables the use of intelligent control algorithms to improve the reliability of the system [124].

In general, the salient features of the MAB converters can be summarized as:

- Facilitates connection of different sources or loads by adjusting transformer turn ratios
- Soft switching capability
- High power density

However, as the number of active bridges increases, the complexity of the transformer and the controller design also aggravate. Therefore, the choice of the number of active bridges mainly depends on the application. In this regard, QAB has been selected as the preferred MAB topology for the ST application. The QAB can be configured symmetrically as illustrated in Fig. 3.3 (a), where there are two active bridges on the input and output side respectively. In an unsymmetrical configuration, there are three active bridges on the input side and one bridge on the output side as shown in Fig. 3.3 (b). For the power flow control in QAB, phase shift modulation similar to the DAB topologies can be utilized. The modeling and control of MAB and QAB topologies are analyzed in detail in [122].

3.2 Motivation for the Application of Graph Theory in Modular Converters

In this section, the necessity of modeling modular power converters using graph theory is presented. The reliability challenges in a modular converter system are addressed and the different techniques for the proposed power routing technique are evaluated.

3.2.1 Reliability Challenge and Power Routing Technique

Even though modular converters offer better power quality, higher redundancy, fault-tolerant capabilities and better maintenance opportunities, there are many open questions concerning the reliability of the system. For applications with high reliability requirement such as ST and MEA, the system failure due to the failure in a modular converter cell is unacceptable. The typical replacement cycle of a modular converter together with the failure cases are shown in Fig. 1.2. In the case of a failure, taking the advantage of modularity, the failed component is replaced with a new component as illustrated in Fig. 1.2. Consequently, a

modular converter system consists of cells with different aging [6]. Moreover, the individual converter cells can have different wear-out due to several electrical and thermal parameters (see Section 4.1 for details). When the converter cells have different aging due to random failures or unsymmetrical aging, they can fail at different instants. This leads to multiple maintenances and may even lead to the unavailability of the power converter.

To address this challenge, a novel power routing strategy has been proposed in [6]. In the conventional control strategies, the power is shared equally among the converter cells as indicated in Fig. 1.2. With the power routing technique, the cells of the modular converter are loaded unequally to control the thermal stress of individual cell. By controlling the thermal stress, the wear-out based failures can be delayed, and thereby the frequency of maintenance is reduced. Moreover, any abnormal thermal behavior of an individual converter cell can be monitored and controlled. To summarize, the power routing strategy is optimizing the reliability, aging and maintenance of the modular converters.

3.2.2 Review of Reliability and Efficiency Optimization Algorithms in Power Electronics

For the implementation of the power routing algorithm in a modular converter system, it is necessary to search for a suitable generic methodology applicable to all modular topologies. Even though the focus is to improve the reliability of the system, the efficiency shall not be sacrificed in due process. Hence, in this section, state-of-the-art optimization techniques in power electronics are evaluated to identify the best method for implementing power routing in modular converters.

The optimization of power electronics for efficiency and reliability is a vast field with a myriad of available techniques as possible candidates for solving the problem. For instance, Model Predictive Control (MPC) is a technique that has gained popularity in recent years to solve optimization problems in power electronics. In [125], an MPC based droop controller has been proposed to improve the efficiency and faster response of current sharing control for multiple power sources connected to a single DC bus. MPC is applied in a microgrid framework to optimally manage the energy among the sources to improve system efficiency by considering cost, profiles and constraints in [126]. For improving the reliability of the system, MPC based inverter fault detection algorithm without extra hardware is discussed in [127]. For drive applications, [16, 128] introduces a finite control set model predictive control strategy for reducing the thermal cycling of the IGBTs in the converters to decrease the thermal stress, and thereby increasing the converter reliability.

Apart from the model predictive control techniques, there are several works focusing on efficiency and reliability optimizations using modulation strategies, topology design, etc. For example, [129, 130] proposes modulation techniques to achieve higher efficiency in the DC-DC converter topologies. In a system level approach, the efficiency of the parallel connected converters is optimized by a current sharing method [131]. Apart from this, other works focus on improving the efficiency of modular power converter systems by optimizing the

topologies [132, 120]. In order to optimize the reliability of the converters, control strategies are employed to reduce the thermal stress of the converters [133, 134]. Optimizing the reliability and efficiency in the design stage of the converter is presented in [135]. A reconfigurable DC-DC converter system has been presented in [136] to optimize the efficiency and reliability, but the reliability assessment is based on the military handbook, which is now considered to be obsolete.

Most of the above-mentioned techniques focus on optimizing the efficiency and reliability on the converter level and when the system becomes more complex with many components and different operating conditions, modeling of the system for optimization and control becomes a bottleneck. With the evolution from the conventional uni-directional grid to the present bidirectional multi-agent internet based grid, the research on energy routers has attracted attention from both academia and industry. The electric vehicles, battery storage systems, renewable energy sources, etc. with intermittent loads and transmission constraints have rendered the energy routing into a complex multi-objective optimization problem. For instance, a minimum cost flow algorithm is proposed in [137] to route the energy in the network with electric vehicles and a graph theory based energy routing algorithm with the convex cost is adopted in [138] for a local area energy network. Improving the drawbacks of congestion management and time-consuming computation in [138], a minimum loss routing algorithm has been introduced in [139]. The energy routing algorithms are based on graph-theoretic solutions since graph theory solutions take into account the network structure of the power grid while performing multi-objective optimization. Graph theory models are extensively used in various fields such as communication, transportation, power systems etc. [140, 141].

From the literature review, it is evident that the potential of graph theory in energy routing problems is well-established. Since power routing in modular converters can be considered to be similar to an energy routing problem in electrical-network, graph theoretic methods remain a strong candidate for implementing optimal power flow solutions in modular converters.

3.3 Fundamentals of Graph Theory

The development of graph theory dates back to 1736 with the graphical solution of the ‘Seven Bridges of Königsberg’ problem by Euler. The application of graphs in electrical engineering was pioneered by Gustav Robert Kirchhoff in 1847 when he associated electrical circuits with graphs for developing a new methodology to solve electrical network problems. Apart from devising voltage and current network laws, Kirchhoff made a significant contribution to the foundation of graph theory [142]. It is worth mentioning the significance of graph theory developments such as Tellegen’s theorem, Signal-Flow Graph, Bond Graph, Petri Nets, etc. in the field of electrical and control engineering. In short, Graph theory is an essential element in solving modern applied mathematics problems in computer science, combinatorial optimization, communication, etc. [143].

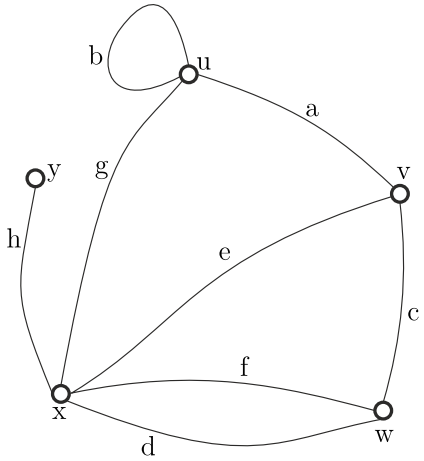


Figure 3.4: Diagram of the graph G.

A graph G is usually denoted as $G(N(G),E(G))$ and consists of a set $N(G)$ nodes and a set of $E(G)$ edges. Another way of graph representation is by an incidence function Ψ_G that associates the relationship of each edge in G with the nodes/vertices. For instance, if e is an edge connecting the nodes x and v, then $\Psi_G(e) = \{x,v\}$.

A graph G with nodes and edges is shown in Fig. 3.4. The graph G is represented as

$$G = (N(G),E(G)), \tag{3.1}$$

where $N(G) = \{u,v,w,x,y\}$ and $E(G) = \{a,b,c,d,e,f,g,h\}$. The incidence function Ψ_G for each edge will be the pair of nodes at the end of the edge. For storing the graph in computers and for calculations, a matrix representation is used and can be represented as an incidence matrix $I(G)$. The incidence matrix size depends on the number of edges and nodes and it is

$$\begin{array}{c} \\ u \\ v \\ w \\ x \\ y \end{array}\!\!\begin{array}{c} \begin{array}{cccccccc} a & b & c & d & e & f & g & h \end{array} \\ \begin{pmatrix} 1 & 2 & 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \end{array} \qquad \begin{array}{c} \\ u \\ v \\ w \\ x \\ y \end{array}\!\!\begin{array}{c} \begin{array}{ccccc} u & v & w & x & y \end{array} \\ \begin{pmatrix} 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 2 & 0 \\ 1 & 1 & 2 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 \end{pmatrix} \end{array}$$

$I(G)$: Incidence Matrix of G $\qquad$ $A(G)$: Adjacency matrix of G

clear that each entry in the matrix represents the number of times the edge and the node are incident. For example, the edge a is incident only once on the node u, which corresponds to value 1 in the $I(G)$. Whereas, edge b forms a self-loop on node u and thus results in an incidence value 2 in the matrix $I(G)$.

Another way of the matrix representation of the graph for computation is using an adjacency matrix. In the adjacency matrix representation, the relation between two nodes is given as

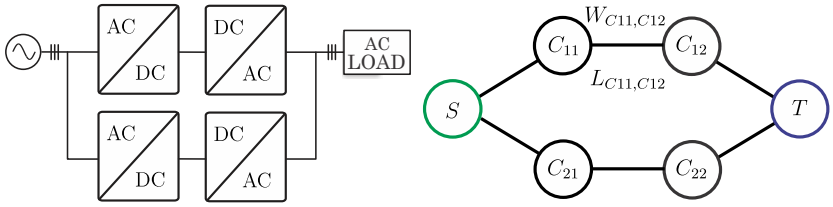


Figure 3.5: Exemplary modular converter architecture (a) Electrical schematic (b) Graph theory representation [J5].

shown in the matrix $A(G)$ of graph G. The adjacency matrix is a square matrix and the graph without any self-loop must have 0s in the diagonal.

For solving the problems such as traffic flow or power flow in the case of electric circuits, a graph-theoretic formulation without any specific direction is meaningless. Therefore, a directed graph consists of edges with a specific direction having a head and a tail. Formally, a directed graph is an ordered pair $D(N(D),E(D))$ consisting of a set of nodes $N(D)$ and a set of edges or arcs $E(D)$ disjoint from $N(D)$. The incidence function $\Psi_D(a) = \{p,q\}$ represents an edge a connecting p to q and the node p is said to be the tail and q forms the head. In this work, arc and edges are used interchangeably for digraphs.

Many applications require a cost to be associated with the edge of the graph and this cost is termed the weight of the edge. The weights may represent the length of the route, capacity of the line or the losses in the flow network, etc., and such a graph is called weighted graph. For representing the power flow in a modular converter, a directed graph with weights is required to depict the direction of power flow along with the cost associated with each power path.

3.4 Graph-Theoretic Representation of Modular Power Converters

3.4.1 Graph-Theoretic Definitions

The idea behind the graph-theoretic representation of modular power converters is to visualize the power flow in the converter as a graph-theoretic network flow problem and subsequently formulate the optimal power flow for improving the system reliability and efficiency. The modular power converters consisting of many cells with power flowing from the source to load can be visualized as a graph with nodes and edges.

In order to define the graph-theoretic equivalent of a modular power converter, a two stage modular AC-AC converter with 2 power flow paths is considered as shown in Fig. 3.5 (a). Here, the source is the AC grid and the load can be any AC load.

The graph theoretic model of the modular converter system is defined as follows:

- Definition of Node: The modular converter cells form the nodes of the graph. The basic building block of each modular topology has been considered as a node. For example, each H-bridge in a CHB cell and each submodule in an MMC is treated as a

node. In the case of DAB and QAB converters, each H-bridge cell is taken as a node since the reliability of each H-bridge can vary according to the power flow conditions. Since the objective of the graph theory representation of the modular converter is to develop a power routing algorithm considering reliability and efficiency, it is critical that each node definition is able to incorporate these factors while modeling the system. Apart from the converter cells, the source and load points are also defined as nodes as illustrated in Fig. 3.5 (b).

The nodes of the graph G consisting of the AC source, load and the converter cells shown in Fig. 3.5 (b) are given by

$$N(G) = \{S, C_{11}, C_{12}, C_{21}, C_{22}, T\}, \tag{3.2}$$

where S denotes the Source, T indicates the sink/load and C_{11},...,C_{22} represents the converter cells.

- Definition of Edge: The edge between two nodes represents the power flow path between them. It is to be noted that the edges between the nodes do not represent the exact electrical connections. The edge shall be visualized as the path followed by the power to flow from the source to the load. For instance, the edges of the modular converter graph representation given in Fig. 3.5 (b) are given by

$$E(C) = \{..., L_{i,j}, ...\}. \tag{3.3}$$

Here, $L_{i,j}$ is the edge connecting nodes i and j where $i, j \in N(G)$. Unless otherwise specified, the graphs illustrated in this work has the direction from source to sink and the direction arrows are not shown in the graphs explicitly.

- Definition of Weight: Weights are assigned to the edge in a graph to denote the cost associated with it. Weights can be associated with any parameter relevant to the optimization problem associated with the graph. In the case of a modular system consisting of many converter cells, each converter cell can have different aging and efficiency. In the power routing optimization algorithm, converter efficiency and reliability are chosen as the parameters for optimization. Therefore, it is necessary to assign weights to the edges considering the reliability and efficiency aspects. The weight $W_{i,j}$ of the edge connecting a node i to j is given as

$$W_{i,j} = f(\eta_j, \rho_j), \tag{3.4}$$

where $W_{i,j}$ is a function of the efficiency factor η_j and reliability factor ρ_j of the destination node.

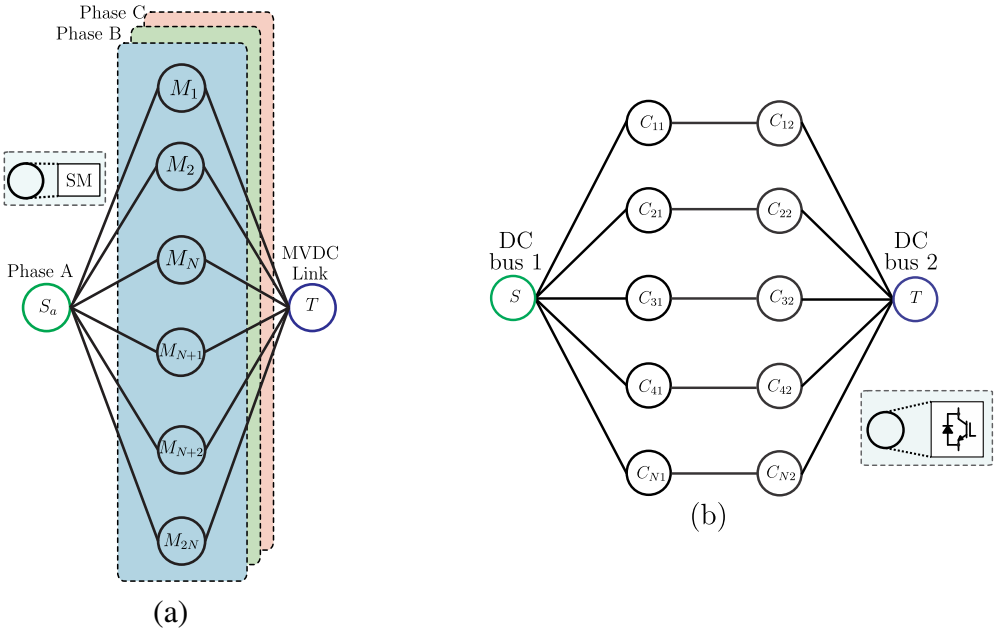


Figure 3.6: (a) Graph representation of MMC topology shown in Fig. 3.1(b), (b) Graph representation of Modular Dual active bridge topology shown in Fig. 3.2 [C6].

3.4.2 Graph Theory Representation of Selected Modular Topologies

In order to demonstrate the implementation of graph theoretic representation in power electronic systems, popular modular converter topologies and their graph theory representation are discussed here.

Fig. 3.6 (a) illustrates the graph representation of the MMC topology shown in Fig. 3.1 (b). Here, each submodule is represented by a node. The phases A, B and C are considered as the source nodes and the MVDC-link is the sink node. The connection between the nodes indicates the power flow path from the source to the sink. Even though the submodules are electrically connected in series, the power flow paths are shown as parallel in Fig. 3.6 (a). Owing to the series connection of the SMs, the current in each SM is equal. However, the power redistribution among the SM can be achieved through voltage variation, switching frequency control or modulation techniques [144]. Since the power processed by each individual submodule can be controlled independently of the other, the power flow paths between the source and sink are considered as parallel. The power handling constraints imposed by the topology/operating conditions of a node can be formulated mathematically and are considered for the optimization function. The path from source to sink is given as

$$path(S \rightarrow T) := S \equiv \left\{ \begin{array}{c} M_1 \\ \ldots \\ M_{2N} \end{array} \right\} \equiv T. \tag{3.5}$$

Fig. 3.2 (a) and (b) show Dual Active Bridges in IPOP and ISOP configuration respectively, and their graph representation is shown in Fig. 3.6 (b). It is worth noting that both IPOP and ISOP configurations share the same graph representation even though they have differ-

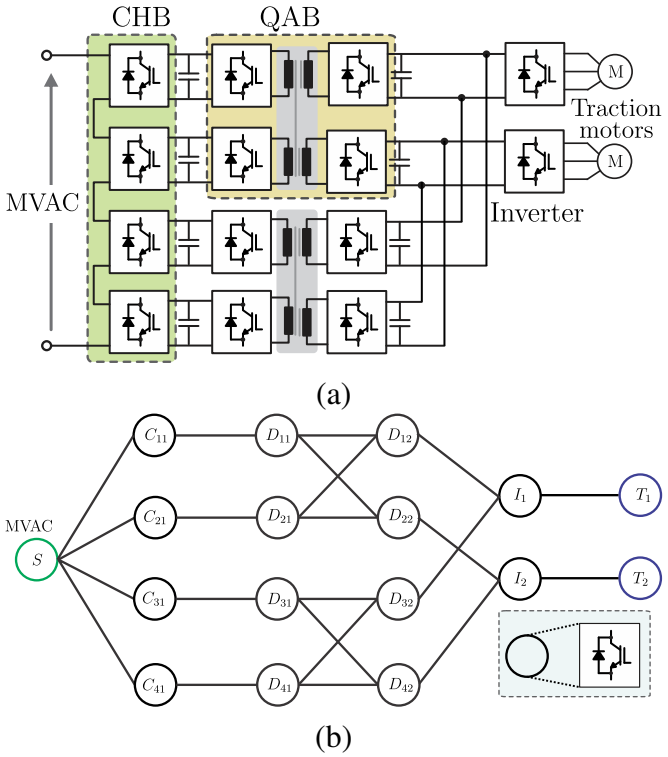


Figure 3.7: Power electronic transformer for traction (a) Electrical schematic (b) Graph theory representation [C6].

ent electrical connections. In case of IPOP configuration, power routing can be achieved by controlling the distribution of current among the cells, whereas in ISOP configuration, voltage or modulation methods are employed to route the power [19]. Therefore, in both IPOP and ISOP topologies, thepower flow of the individual converter cells can be controlled and this gives rise to the same graph representation as shown in Fig. 3.6 (b). The power flow path between source and sink is represented as

$$path(S \rightarrow T) := S \equiv \left\{ \begin{array}{c} C_{11},C_{12} \\ \ldots \\ C_{N1},C_{N2} \end{array} \right\} \equiv T. \tag{3.6}$$

The graph representations of CHB and QAB converters are described through an architecture of power electronics traction transformer proposed in [145]. Power electronics transformer with CHB and QAB converters for the traction drive is shown in Fig. 3.7 (a). The power is fed from the medium voltage AC grid to drive the traction motors. The power conversion stages include the Cascaded H Bridge for rectification, Quadruple Active Bridges for DC-DC conversion and inverters for DC-AC conversion. The equivalent graph is drawn in Fig. 3.7 (b), which provides a comprehensive understanding of system level power flow. CHB converter cells are indicated by the nodes C_{11} - C_{41}, QAB converter cells by D_{11} - D_{22} and inverter cells by I_1 and I_2. The MVAC grid forms the source node (S) and the two traction motors are the sink nodes (T_1, T_2). Power flows from each CHB cell to the connected QAB cell. The symmetrical QAB configuration has two input cells, and they are coupled to the

two output cells through a common transformer. Therefore, the power can flow from one input QAB cell to the two output QAB cells as indicated by the connections between D_{11}, D_{12} and D_{22}. The power flow paths between MVAC and two traction motors are represented as:

$$path(S \rightarrow T_1) := S \equiv \left\{ \begin{array}{c} C_{11},D_{11},D_{12},I_1 \\ C_{21},D_{21},D_{12},I_1 \\ \ldots \end{array} \right\} \equiv T_1 \tag{3.7}$$

$$path(S \rightarrow T_2) := S \equiv \left\{ \begin{array}{c} C_{11},D_{11},D_{22},I_2 \\ C_{21},D_{21},D_{22},I_2 \\ \ldots \end{array} \right\} \equiv T_2 \tag{3.8}$$

3.5 Application of Modular Power Converters in Smart Transformers

3.5.1 Concept of Smart Transformers

The power electronics based transformer, also known as Solid-State Transformer (SST), was originally proposed by McMurray in 1968 by using a high frequency transformer and solid-state switches. SST boasts reduced volume and weight while providing additional functions which are not provided by passive low frequency transformer. Utilizing the aforementioned advantages, companies such as ABB, Alstom, Siemens, Bombardier, etc. have developed SSTs for traction applications [146, 147, 20, 148]. However, even after 50 years, the SST has not been able to replace the traditional LFT in energy transmission and distribution systems, mainly due to efficiency, reliability and cost concerns.

Recent penetration of renewable energy and electric vehicle charging stations has changed the dynamics of a conventional electrical grid. Traditionally, electric power had a unidirectional flow; from the power plants to the end consumers. Distributed Energy Resources (DER) integrated by power electronic systems in the grid has altered the conventional unidirectional power flow into bidirectional one. Moreover, the transition from deterministic power generation by power plants to probabilistic power generation owing to renewable resources such as solar and wind has challenged the conventional concept of an electric-grid. Furthermore, the inclusion of DC-grids has been gaining momentum due to the integration of electric vehicles and power electronics enabled DER.

The transformation of the electric grid has motivated the research fraternity to investigate more into the potential of the SST for managing the grid. FREEDM center has been a strong advocate of the SST to manage the electric grid analogous to an energy internet [149]. The proposed energy router facilitates the plug-and-play connection of residential and industrial end users through AC and DC grids. SST utilizes the communication network to coordinate the activities of energy management. Further advancements in the SST designs have been reported in the literature such as UNIFLEX [150], EPRI [151] and GE [152]. The SSTs from FREEDM, UNIFLEX and EPRI are based on multilevel inverters with the capability

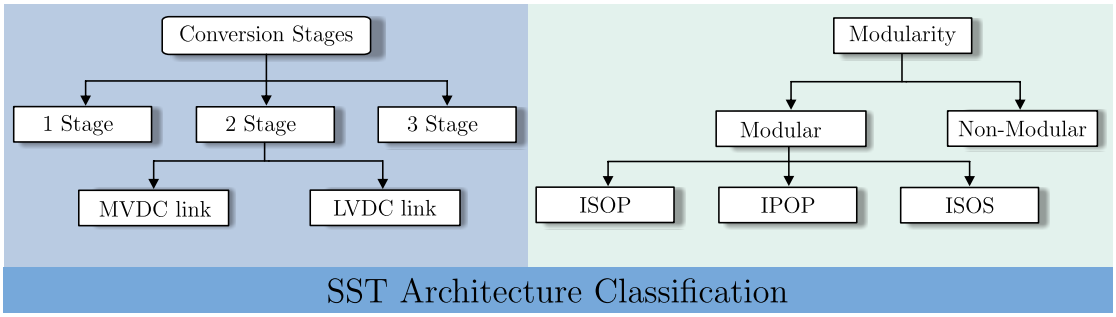


Figure 3.8: ST architecture classification based on conversion stages and modularity.

to provide network functionalities such as reactive power compensation, voltage regulation, harmonic isolation, fault isolation etc., but have an average efficiency compared to that of GE. However, the increased efficiency of the GE SST comes at the cost of some system functionalities due to the line frequency commutation in its high voltage rectification stage.

Nonetheless, the aforementioned designs don't provide a comprehensive solution to make the SST reliable, efficient, easy to maintain and capable of delivering ancillary grid services. To make SST a more economically viable solution, the smart transformer concept was introduced in the "Highly Efficient And Reliable Transformer" project [6]. The ST is a power electronics based transformer that offers DC-link connectivity and additional services to the grid and has advanced control and communication capabilities to improve reliability and efficiency. One of the distinguishing features of the ST is the increased reliability and easy maintenance through intelligent algorithms such as power routing. In energy distribution applications, Smart Transformer is gaining popularity due to its ability to offer a myriad of grid services and the potential to reduce infrastructure costs [6, 153].

From the system architecture perspective, the power electronics based transformers are typically classified according to the number of power conversion stages and modularity. The classification of the SST architectures based on the conversion stages and modular connection is illustrated in Fig. 3.8. The single stage SST can be realized by simple AC-AC full-bridge converters, AC-AC flyback converters or direct matrix converters. As all these single stage topologies lack the bulky DC-link capacitors, the power density is high and requires only fewer number of components. On the other hand, lack of DC-link results in direct coupling of the input disturbances to the output and the absence of power factor correction. Thus, this topology does not justify the deployment of a power electronic transformer in the distribution system. Two stage architecture comprises an AC-DC stage and DC-AC stage connected through a DC-link capacitor. The electrical isolation can be considered either in the AC-DC stage or DC-AC stage and depending on this, either MVDC or LVDC link is available. This architecture can provide reactive power support to the grid due to the availability of the DC-link. However, the DC-link voltage regulation is limited due to the lower bandwidth of the cascaded control structure. Power electronics transformers with three conversion stages comprising MVAC to MVDC, MVDC to LVDC, and LVDC to LVAC conversion stages are also popular to the ability to provide additional grid services.

One of the distinguishing features of the ST is that it adopts a three-stage architecture with

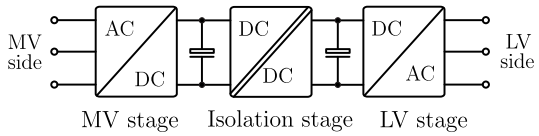


Figure 3.9: Three-stage ST architecture.

modular converters. The three-stage architecture enables the ST to decouple the MVAC grid and LVAC grid. It also provides the provision for direct connection of the MVDC and LVDC grids. Moreover, since both the MVDC and LVDC-links are available, independent control of the MVAC grid and LVDC grid reactive power is possible. Even though a three-stage architecture results in an increased number of components compared to the others, the controllability and functionalities offered are much required for a modern-day SST or ST.

Since the power electronics based transformer is meant to cater to high power applications in the electric grid, many proposed topologies have the modular connection of power converters [150, 151, 152]. As shown in Fig. 3.8, the aforementioned modular SST architectures can be classified into ISOP, IPOP, and Input Series Output Series (ISOS) configurations based on the connection of modular power converters. However, there are non-modular SST topologies that are primarily based on Silicon Carbide (SiC) devices [23]. Compared to the state-of-the-art SST topologies, modularity is a vital characteristic of the ST. The ST is designed to cater to the needs of the electrical distribution grid which ranges typically from $2.3\,kV$ to $35\,kV$. As of today, the semiconductor technology has not been able to offer single devices capable of blocking such high voltages. For the Silicon based IGBTs, the maximum blocking voltage of the commercially available device is $6.5\,kV$. The widebandgap based Silicon Carbide MOSFETs and IGBTs offer higher blocking voltages up to $15\,kV$. However, these devices are available only for research purposes and not for commercial use. Even with the available power device with the highest blocking voltage, a two-level converter cannot operate under a grid voltage of $35\,kV$. Moreover, high frequency transformer with distribution grid voltages are also not readily available. A modular approach can be used to solve this problem by using lower blocking voltage devices in series or parallel connections to attain voltage/power scalability.

Together with multi-stage architecture and modularity, the ST aims to tackle the main challenges of conventional solid state transformer configurations such as reliability, efficiency and cost. The ST architectures provide the flexibility to implement intelligent control algorithms to optimize maintenance, failures and efficiency.

3.5.2 Application of Graph Theory in ST Architectures

Since ST adopts a modular three-stage architecture, the opportunity to apply intelligent algorithms such as power routing becomes more evident and challenging at the same time. As discussed in Section 3.4, graph theory representation of modular converters enables the identification of power flow paths from one module to another. In this section, the application of

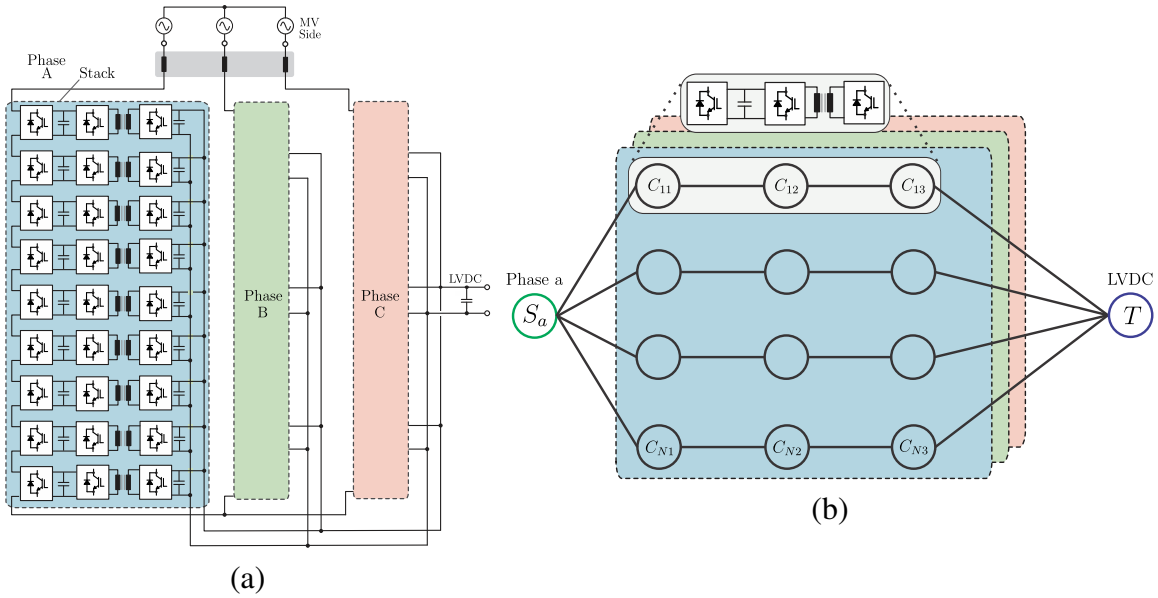


Figure 3.10: (a) CHB-DAB based ST architecture (b) Graph theory representation of CHB-DAB based ST.

graph theory to model the most commonly discussed ST architectures in [60, 154, 15, 25] is introduced. The selected ST architectures are listed below.

- CHB DAB based ST
- CHB QAB based ST
- CHB QAB based interphase ST
- MMC DAB based ST

CHB-DAB based ST

The medium voltage AC-DC stage of the ST controls the active and reactive power consumption from the MV grid and converts the AC voltage into an appropriate DC voltage level demanded by the isolation stage. Considering modularity as a vital characteristic of ST, CHB and MMC have been identified as the most suitable topologies for the ST application [25]. As discussed in Section 3.1, both converters are an outcome of the cascaded connection of the basic converter topologies but provide different functionalities owing to their configuration. In this CHB-DAB based ST, CHB topology is chosen as the MV side AC-DC converter.

The DC-DC stage of the ST shall provide galvanic isolation between the MV and LV grids since the AC-DC stage does not offer galvanic isolation. Additionally, high efficiency and bidirectional power flow capability shall be considered for the selection of DC-DC stage topologies. Considering all these aspects, the Dual Active Bridge is an ideal candidate as described in Section 3.1, and constitutes the DC-DC stage of CHB-DAB based ST.

In this architecture, each CHB cell is connected to the DAB cell as shown in Fig. 3.10 (a). Therefore, the power from one CHB cell flows directly to the primary side of the DAB cell. The secondary sides of the DAB converter cells are connected in parallel to form the LVDC-link. The equivalent graph of the CHB-DAB based ST is illustrated in Fig. 3.10 (b). Here, a CHB cell connected to a DAB converter constitutes one power flow path, and the power flow paths from MVAC to LVDC are given by

$$path(S \rightarrow T) := S \equiv \left\{ \begin{array}{c} C_{11},C_{12},C_{13} \\ \ldots \\ C_{N1},C_{N2},C_{N3} \end{array} \right\} \equiv T. \tag{3.9}$$

The graph shown in Fig. 3.10 (b) has the three-phase of the MVAC side as source nodes and LVDC-link as the sink node. The converter cells of the CHB and the primary and secondary sides of the DAB converter cells are represented as nodes. The modularity of the CHB-DAB based architecture is evident in the graph theory representation since no converter cells are shared among the power flow paths given in (3.9).

CHB-QAB based ST

By replacing the DC-DC stage of a CHB-DAB based ST with a Quadruple Active Bridge, a semi-modular ST architecture known as CHB-QAB based ST is obtained as illustrated in Fig. 3.11 (a). An asymmetrical configuration of the QAB is used in this architecture with three QAB cells connecting the MV CHB cells and one QAB cell catering the LV side. The LV sides of the QAB cells are connected in parallel to form the LVDC-link.

Following the methodology for modeling the modular converter as a graph, the equivalent graph of CHB-QAB based ST is illustrated in Fig. 3.11 (b). Here, a basic power flow unit consists of 3 CHB cells connected to the QAB as highlighted in Fig. 3.11 (a). The power flow paths from source to sink are given as:

$$path(S_a \rightarrow T) := S \equiv \left\{ \begin{array}{c} C_{11},C_{14},C_{17} \\ C_{12},C_{15},C_{17} \\ C_{13},C_{16},C_{17} \\ \ldots \\ C_{N1},C_{N4},C_{N7} \\ C_{N2},C_{N5},C_{N7} \\ C_{N3},C_{N6},C_{N7} \end{array} \right\} \equiv T \tag{3.10}$$

By analysing the power flow paths from source to sink given in (3.10, the following observations are obtained.

- For each unit consisting of 3 CHB cells connected to a QAB converter, the LV side QAB cell, for example C_{17}, repeats three times. The repetition of a node in the power

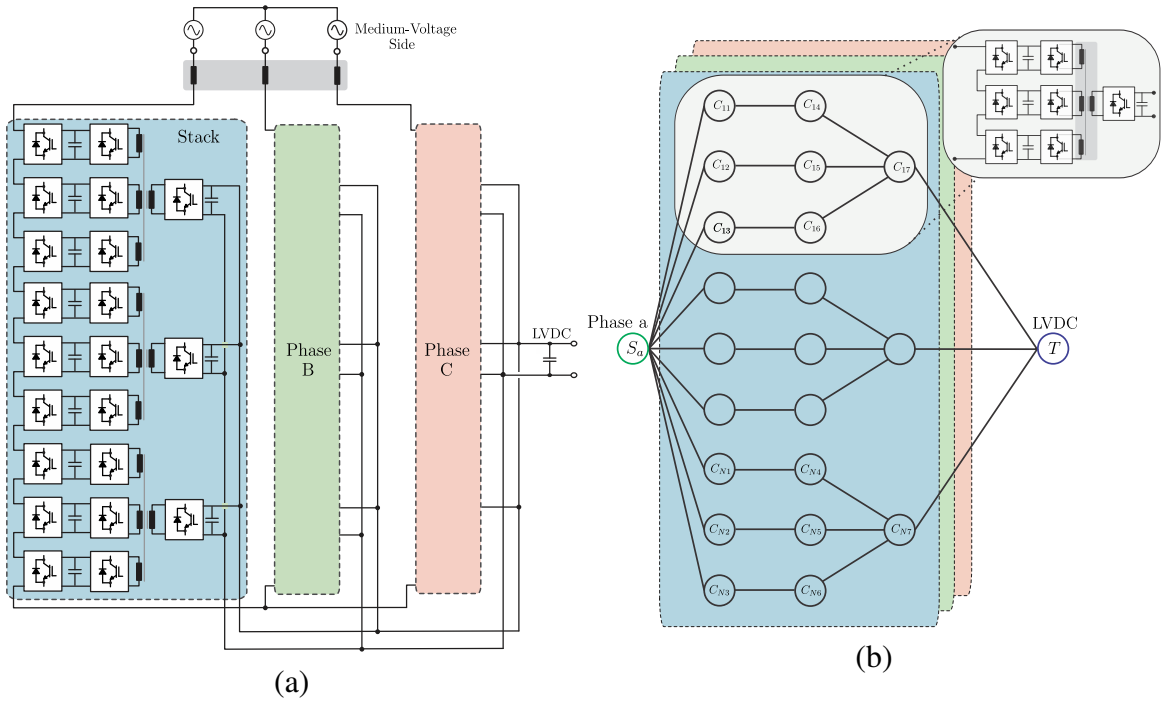


Figure 3.11: (a) CHB-QAB ST architecture (b) Graph theory representation of CHB-QAB ST [J5].

flow path will automatically multiply its weight in the optimization algorithm. Since the failure of the LV side QAB cell will lead to the failure of a power flow unit, it is vital to consider its importance in power routing algorithms.

- Unlike the DAB based ST architectures, QAB provides multiple opportunities for power routing. As shown in Fig. 3.11 (b), the power can be shared unequally by each power flow unit, and within one unit itself, again there is a possibility of power routing through the three available paths.

- The disadvantage of this architecture is evident from the power flow paths given in (3.10) since a single point failure of the LV QAB cell will lead to the unavailability of one unit or 3 power flow paths.

CHB-QAB based Interphase ST

In order to achieve easier power exchange between the MVAC phases and simpler control effort for a three-phase power balance loop, an interphase ST architecture with CHB and QAB is proposed in [155, 6]. The schematic of the CHB-QAB based Interphase ST shown in Fig. 3.12 (a). In this architecture, the MV QAB cells in a single power flow unit are connected to the three phases instead of a single phase as in CHB-QAB based ST. The equivalent graph theory representation of the CHB-QAB based interphase ST is shown in Fig. 3.12 (b). Here, the power flow paths between the power flow units can be visualized more clearly. It is evident that each QAB converter process the power flowing from all three phases. Therefore, in case of power imbalance among the three phases, the power flowing

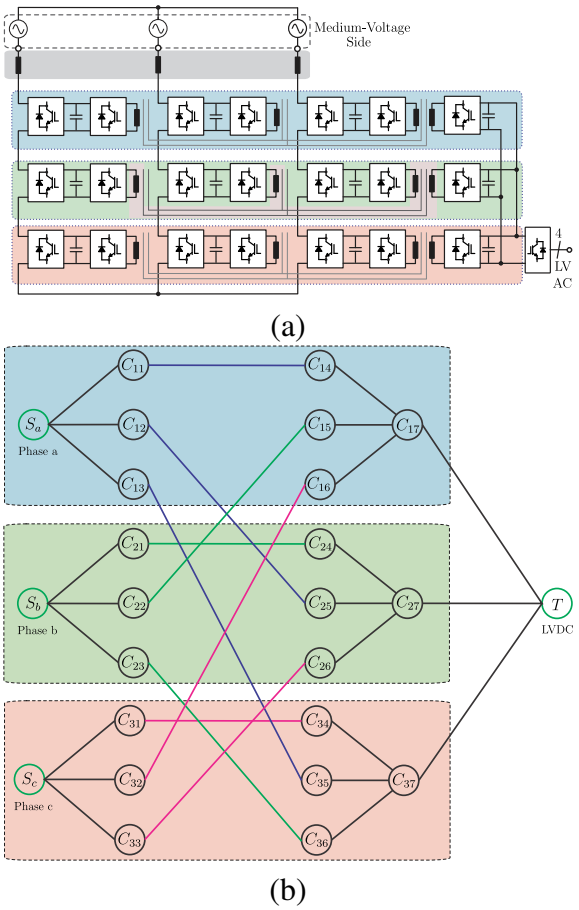


Figure 3.12: (a) Interphase ST architecture (b) Graph theory representation of interphase ST [J5].

through each unit can be adjusted to regain power balance. The power flow paths for phase S_a for this architecture is given as

$$path(S_a \rightarrow T) := S \equiv \left\{ \begin{array}{l} C_{11},C_{14},C_{17} \\ C_{12},C_{25},C_{27} \\ C_{13},C_{36},C_{37} \end{array} \right\} \equiv T. \tag{3.11}$$

Similarly, power flow paths for the other two phases are obtained.

The essential features of this architecture from power routing perspective are as follows:

- For the power flow paths from a phase to the LVDC-link as given in (3.11), no nodes are repeated. This implies that a single point failure cannot result in the shut down of power flow from the phases to the LVDC side. For instance, the failure of the LV port of the QAB C_{17} does not result in the complete shut down of all the phases. The failure of node C_{17} results in the absence of three power flow paths, but all the three MVAC phases are still connected to the LVDC through other 2 paths. Therefore, the ST can still potentially function in a de-rated mode.
- The graph representation enables potentially simple formulation of the power balance control algorithms among the three phases.

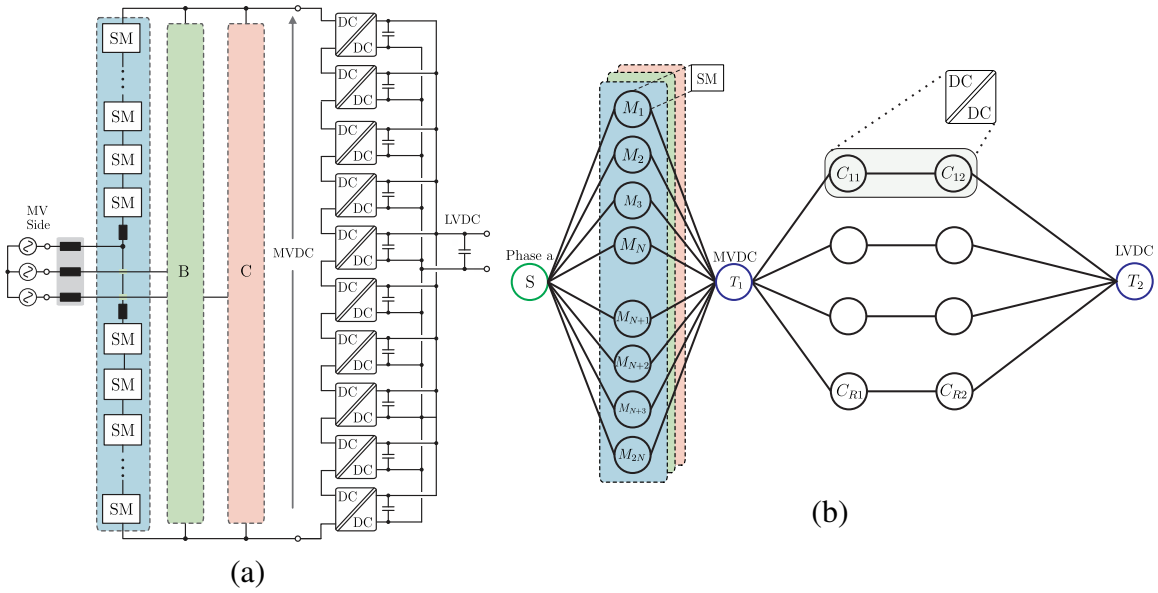


Figure 3.13: (a) MMC-DAB ST architecture (b) Graph theory representation of MMC-DAB ST.

MMC-DAB based ST

As the name indicates, MMC-DAB based ST utilizes MMC converter for the MVAC to MVAC stage and DAB converters for the MVDC to LVDC stage. Fig. 3.13 (a) shows the block diagram of an MMC-DAB based ST. Compared to the CHB based ST architectures, MMC provides an MVDC-link as shown in Fig. 3.13 (a). The DAB converters are connected in ISOP configuration to fulfill the input voltage requirement of the MV side and the current requirement of the LV side. The equivalent graph representation is a combination of MMC graph and ISOP DAB system and is shown in Fig. 3.13 (b). In this case, the power flow is split into two parts; from MVAC to MVDC and from MVDC to LVDC. The power flow paths are obtained as a combination of power flowing through MMC and DABs as given below.

$$
\begin{aligned}
path(S \rightarrow T_2) := S \equiv \left\{ \begin{array}{c} 1 \\ \ldots \\ 2N \end{array} \right\} \equiv T_1, \\
T_1 \equiv \left\{ \begin{array}{c} C_{11}, C_{12} \\ \ldots \\ C_{N1}, C_{N2} \end{array} \right\} \equiv T_2.
\end{aligned}
\tag{3.12}
$$

The distinguishing characteristics of the MMC-DAB based ST architecture graph are as follows:

- Power flow paths from S to T_1, and T_1 to T_2 can be considered as independent of each other. This implies that the power flow within the converter cells of the MMC can be controlled independently of the power flow control within DAB cells.
- Any single point failure of a converter cell within this architecture affects only that

converter cell. For instance, failure of a DAB cell does not affect the MMC converter cells directly as in the case of a CHB-DAB based ST architecture. When redundant cells are available for replacement, any single converter cell failure can be repaired by replacing that cell only.

3.6 Brief Summary of the Chapter

A new approach for the modeling of the internal power flow through the modular converter cells has been discussed in this chapter. Since the power flow between the individual converter cells can be considered analogous to the information or energy low, graph theory is identified as a suitable candidate for converter modeling. Starting with the fundamentals of graph theory, the representation of simple and complex modular converter topologies/architecture with graph theory is explained. Graph theory is used to represent and identify the distinguishing features of the selected ST architectures. This chapter forms the basis of graph theory based optimization algorithm development in Chapter 5.

4 System Level Active Thermal Control by Power Routing

This chapter introduces the concept of system level active thermal control for modular power converters. In contrast to the active thermal control methods reviewed in Chapter 2, the system level active thermal control focuses on equalizing the aging of the modular converter cells. First, the reasons for the difference in aging of the converter cells of a modular system are discussed in detail. Subsequently, the proposed solution to route the power internally in a modular converter system is explained and the limitations of the power routing capability of modular topologies are analyzed [C1, C2]. A virtual resistor based power routing control developed for the power conversion stages of the modular ST is discussed and the impact of the power routing on the system lifetime is analyzed [J2, J9, C8]. The publications [J2, J9, C1, C2, C8] have contributed to the content of this chapter.

4.1 Reasons for Unequal Aging in Modular Converters

Modular converters are composed of a number of converter cells and when each cell has different aging, it can lead to multiple maintenance instants. For high reliability applications such as ST and MEA, unscheduled maintenance and failures are unacceptable. Power devices have been identified as one of the major failing component in a power converter, and hence this study focuses mainly on the reliability of power devices. According to the bathtub curve for the reliability of the power semiconductor devices, there are mainly three failure mechanisms; namely, initial failures, random failures and wear-out based failures [28].

The initial failures happen in the early stage of the lifespan of a power device. These failures are mainly due to manufacturing defects or incorrect installation or operation of the devices. The initial failures can be substantially reduced by better manufacturing practices, correct design and operation of the converter system. Random failures occur due to several factors such as cosmic rays, faults etc. The advantage of having modularity is that the failed cells can be replaced with a new module as illustrated in Fig. 3.14(a). Thus, the whole converter system does not need to be replaced and only the failed cell needs to be exchanged. In the

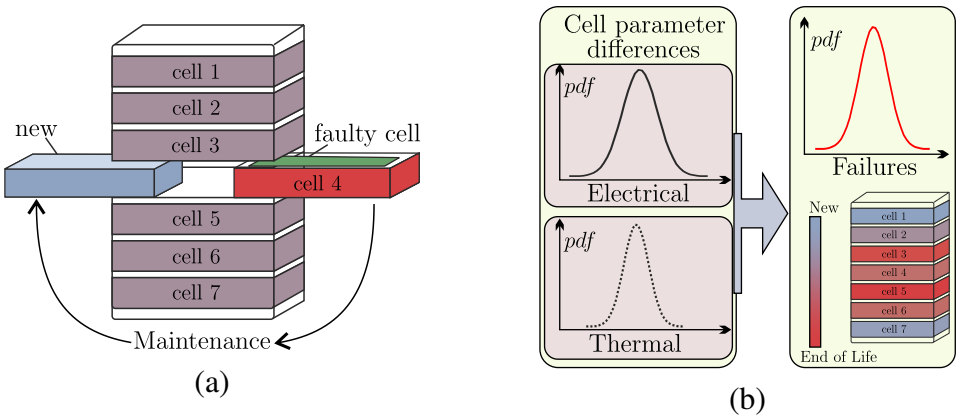
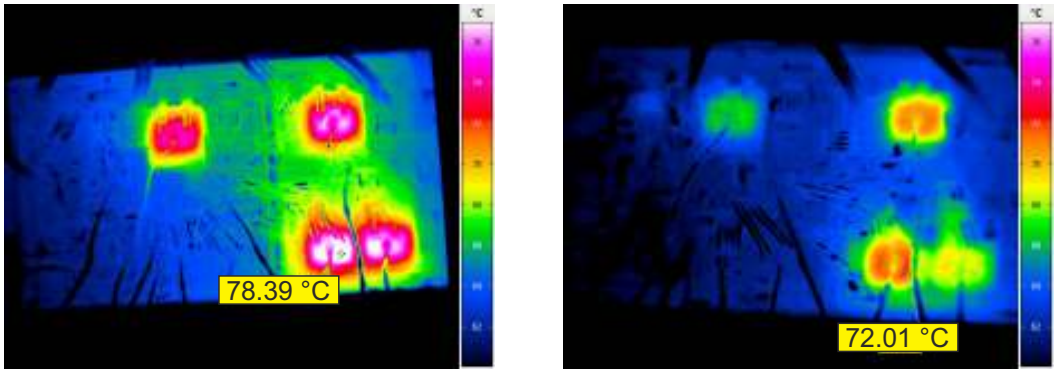


Figure 3.14: (a) Failures and replacement cycle (b) Wear-out based failure distribution due to parameter differences [J5].



a b

Figure 4.1: Temperature distribution of modular converter processing equal power (a) cell 1 (b) cell 2.

lifespan of the converter system, many such random failures can result in a modular system with cells having unequal aging.

The wear-out based failures are based on the Physics of Failure (PoF) approach which has been discussed in Chapter 2. Thermal cycling is identified as the major cause of wear-out based failures of power devices. In a modular system, the cells can have different thermal cycling due to the differences in the thermal and electrical parameters of the power converter. The impact of the variation of the thermal and electrical parameters on the aging of the converter cells is discussed as follows.

4.1.1 Impact of Parameter Variations on Converter Lifetime

The electrical parameters of the power devices such as the collector-emitter voltage (V_{ce}), turn-on and turn-off energies vary around a typical mean value. The datasheet of the power devices indicates a maximum variation of 20 % from the mean value for the collector-emitter voltage (V_{ce}) [99]. The turn-on and turn-off energies also vary from one device to the other. These variations in the device electrical parameters result in the difference of losses generated by the power devices even when they process equal power. The difference in loss generation in turn results in different thermal cycling for each device, and thereby unequal aging. This is illustrated in Fig. 4.1, where two H-bridge converter cells of a CHB converter process equal power with equal heatsink temperatures, but have a junction temperature difference of $6.38°C$. The temperature distribution of the open IGBT module $DP25H1200T101667$ is captured with an IR camera.

Another major concern in a modular system is the temperature distribution of the heatsink. The heatsink temperatures are maintained by the cooling system; either water or air cooling. In a modular system, the heatsink temperatures can vary since the temperature at the inlet and outlet of the coolant are different. In addition to this, typically the modular cells are arranged in a converter rack and the geometrical positioning of the cells can also affect the degree of cooling. Thus, it is logical to assume that the heatsink temperatures of each converter cell in

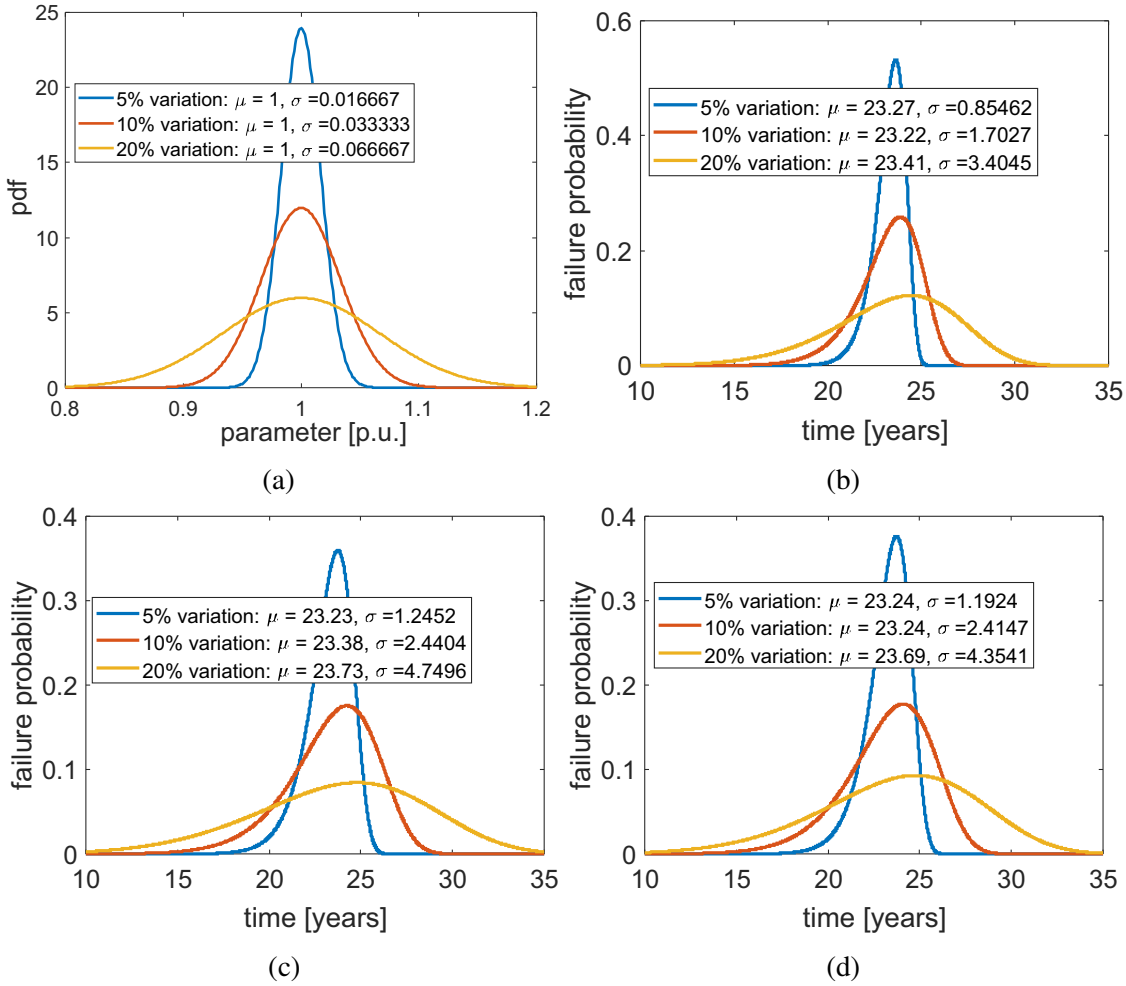


Figure 4.2: (a) Probability density function with different degree of variations (b) Probability of failure with V_{ce} variation (c) Probability of failure with switching energy variation (d) Probability of failure with heatsink temperature variation.

a modular system are not necessarily equal. This will result in a difference in the junction temperature of the cells, and thereby different thermal cycling and aging.

To analyze the impact of parameter variations on the lifetime of the power semiconductor device, a simulation study is performed on a CHB converter system with system parameters given in Table 2.4 and Table 2.5. The mission profile shown in Fig. 2.10 is used as the input for the electro-thermal simulation. The general scheme for the Monte-Carlo simulation given in Fig. 2.18 is followed to analyze the impact of parameter variations. The electrical and thermal parameter variations are modeled with a Gaussian probability density function (pdf) in Fig. 4.2 (a). Here, three cases are presented with 5 %, 10 % and 20 % variation of the parameter from its mean value. The nominal values of the parameters, namely V_{ce}, heatsink temperature, switching energies are considered as $1\,p.u.$ and hence the mean value of the probability distribution is taken as $1\,p.u.$ in Fig. 4.2 (a). Here, μ represents the mean value and σ represents the standard deviation.

Using the pdf of the parameters, a Monte-Carlo simulation is performed to evaluate the lifetime variation of the CHB converter for the three cases. The probability of failure with

Table 4.1: B_{10} lifetime with electrical and thermal parameter variation.

Parameter	B_{10} **lifetime (5 % variation)**	B_{10} **lifetime (10 % variation)**	B_{10} **lifetime (20 % variation)**
V_{ce}	22.14 years	20.96 years	18.86 years
Switching energy	21.58 years	20.11 years	17.36 years
Heatsink temperature	21.66 years	19.99 years	17.83 years

the variation in V_{ce} is shown in Fig. 4.2 (b). The mean and standard deviation of the Weibull fits of the Monte-Carlo simulation indicates the trend of failure probability with the increase in variation of the parameters from 5 % to 20 %. The mean lifetime remains almost equal with increasing variation whereas the standard deviation of the failures increased by almost 4 times from 5 % to 20 %. The failure probability of the power device with switching energy and heatsink temperature variations are given in Fig. 4.2 (c) and (d) respectively. Since the inverter is hard switched, the switching energy variation has a high impact on the lifetime. The heatsink temperature variations also result in a considerable increase in the standard deviation of failure probability.

The B_{10} lifetime of the converter is calculated from the unreliability curve obtained from the Weibull pdf (see Chapter 2 for details) and the results are summarized in Table 4.1. As the parameter variation increases, the B_{10} lifetime of the system decreases. The failure probabilities with parameter variations quantify the impact of different parameters leading to unequal aging of the modular system.

4.2 Power Routing for Modular Systems

The active thermal control methods for individual converter cells introduced in Chapter 6 focus on increasing the lifetime of a converter. In the case of modular power converters, which consist of many converter cells, the individual goal of increasing the lifetime of each converter is not sufficient. The active thermal control strategies aim to achieve reduced thermal cycling of a converter, but it is clear from Section 4.1 that each converter can have different thermal cycling even while processing equal power. Therefore, even when we use independent active thermal control for prolonging the lifetime of each converter, they can fail at different instants. This motivates the requirement of a system level active thermal control to prolong the lifetime of the converter cells to achieve goals such as lower maintenance schedules and delaying early failures caused by thermal stress.

When the converter is located in remote areas, frequent maintenance schedules can result in very high costs. There are many scientific publications regarding the prognostic maintenance scheduling in high reliability industrial applications, aviation sector, etc. [26, 156]. However, fewer references investigate the maintenance scheduling focusing on the system level control algorithms to delay the maintenance.

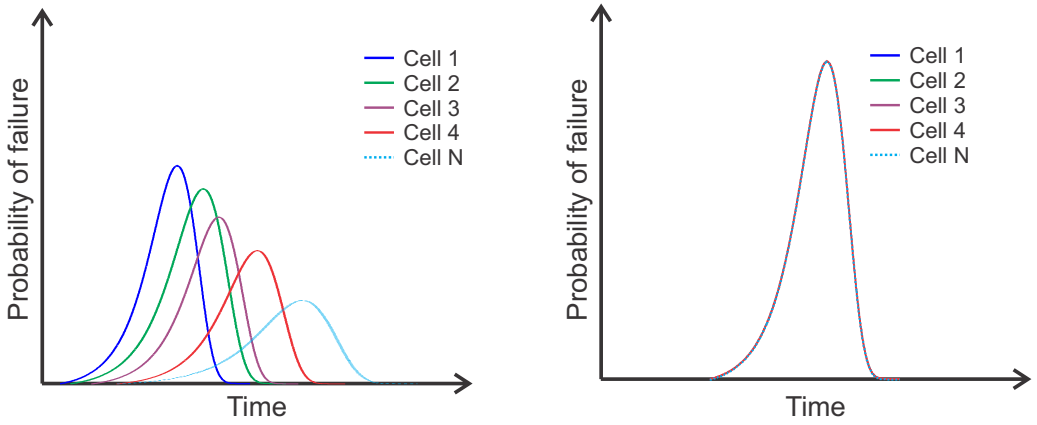
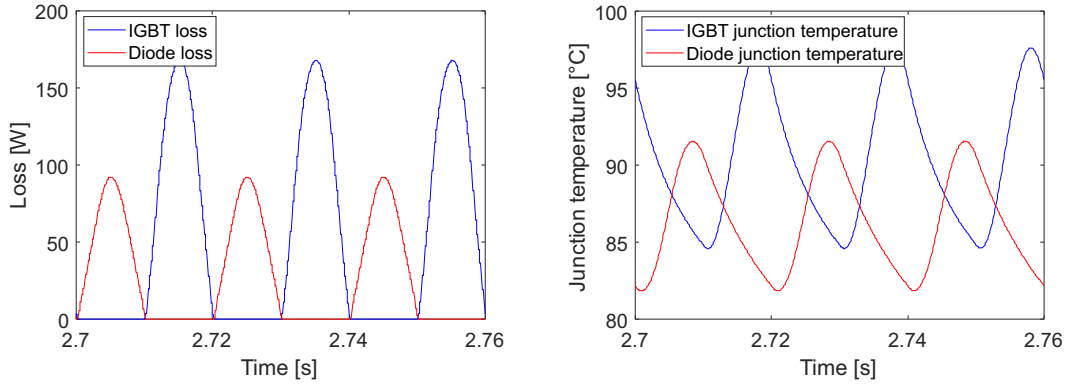


Figure 4.3: Exemplary probability of failure distribution of the converter cells in the modular converters (a) Under normal operation (b) With power routing control.

For improving the reliability of a modular converter system consisting of many cells, the aging of the cells can be actively controlled by unequal sharing of the power depending on the remaining useful life of each module, and is termed power routing [6, 157]. This concept is further explained by using an exemplary failure probability distribution of individual cells of the modular power converter without and with power routing control. Fig. 4.3 (a) shows the probability of failure of a modular system with N cells without any power routing control. As explained in Chapter 2, the lifetime model itself is obtained from the power cycling tests with curve fitting of the experimental data. Thus, the RUL calculation for a given converter cell and mission profile with fixed electrical and thermal parameters can be represented by a Weibull failure probability curve (see Chapter 2). Considering the parameter variations for the cells in a modular system, the failure probabilities of N cells are distributed in time as illustrated in Fig. 4.3 (a) even while processing equal power. It is evident that such a failure probability distribution results in frequent maintenance and the number of maintenance increases with the number of cells. The objective of power routing is to equalize the thermal stress so that the failure probabilities of the individual converter cells are concentrated around a common point in time as shown in Fig. 4.3 (b).

For the series and parallel connected modular topologies, methods such as the multi-frequency power routing, discontinuous modulation based power routing, advanced discontinuous modulation technique, virtual resistance based power-sharing etc. have been proposed to achieve unbalanced power share among the cells [158, 159]. Although these techniques are proposed to achieve power routing, an in-depth analysis of the need for the power routing strategy for different modular topologies/architectures are missing. Therefore, in the following section, the impact of parameter variations on the reliability of series and parallel connected modular topologies are analyzed. Subsequently, the effect and limitations of power routing on these topologies are also investigated.



a b

Figure 4.4: CHB converter connected to the AC grid (a) IGBT and diode losses (b) IGBT and diode junction temperatures.

4.2.1 Analysis of Power Routing on Series Connected Modular Topologies

The series connected modular structure is used to achieve the required voltage rating by the use of power devices with a lower rating in series. For the HVDC and MVDC applications, it is the de facto solution to achieve the required voltage level since devices with such high power ratings are not yet available in the market. In this section, the power semiconductor reliability of the converter cells of series connected modular converters feeding AC loads is studied considering electrical and thermal parameter variations. Subsequently, the scope of power routing is analyzed.

The series connected modular power converters such as CHB or MMC can be connected to an AC grid or an AC motor drive. For any converter feeding alternating current, the losses generated in the power device carrying the current follow the current shape. For example, consider a switch carrying sinusoidal current with power factor 1, when the current is zero, the device losses are minimum and when the current reaches the maximum amplitude, the losses are at maximum. This is illustrated with the help of simulation of the IGBT and diode losses of a CHB cell connected to the AC grid in Fig. 4.4 (a). The simulation parameters of the CHB system and the equivalent thermal network parameters of the IGBT module are given in Table 2.4 and Table 2.5 respectively. The IGBT conducts for the positive current and the diode conducts for the negative half of the grid current resulting in the loss distribution as shown in the figure. The resulting IGBT and diode junction temperatures are shown in Fig. 4.4 (b) using the thermal network parameters in Table 2.5 and considering an ambient temperature of $50\,°C$.

Fig. 4.5 (a) shows the junction temperature of an IGBT in a power module when subjected to variations in the thermal impedance. As explained in Section 4.1.1, the thermal and electrical parameter variations affect the lifetime of the converter. However, in the case of a converter feeding AC load, these variations have a stronger impact due to the low-frequency cycling caused by the alternating nature of the current. The equivalent Thevenin impedance $Z_{th,jhs}$ is varied up to 20 % in discrete steps of 10 % keeping the losses and heatsink temperature constant. The resulting junction temperature with thermal parameter variations is depicted

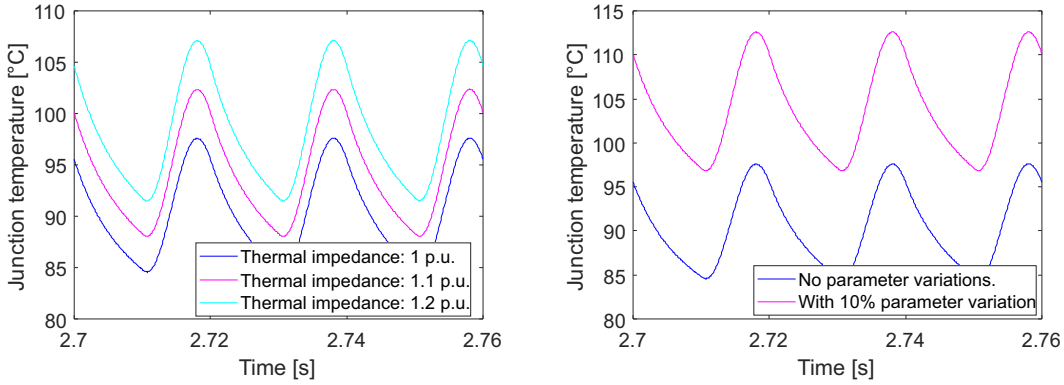


Figure 4.5: IGBT junction temperature of a CHB cell (a) with thermal impedance variation (b) with device losses, thermal impedance and heatsink temperature variation.

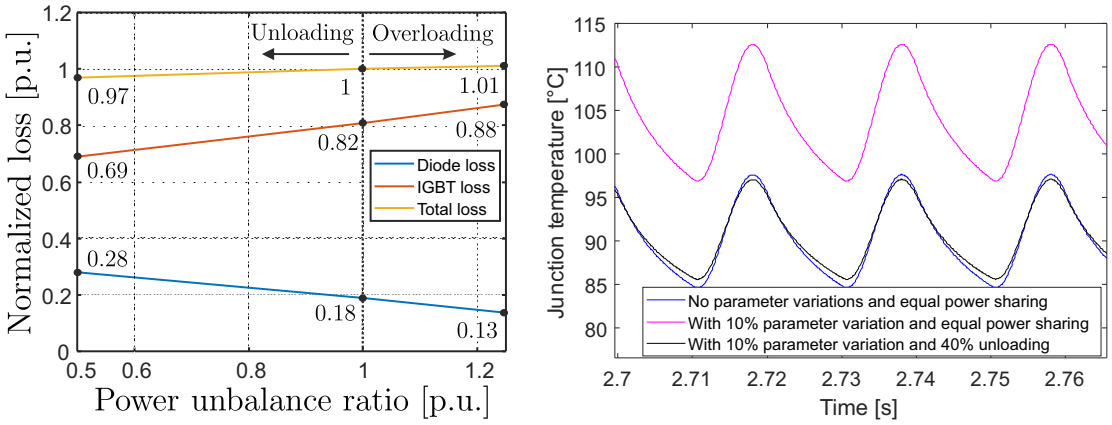
in Fig. 4.5 (a) and it is evident that even a 10 % increase in the thermal impedance leads to an increase of 5 $^{\circ}C$ in the maximum junction temperature, and thereby causing a significant increase in the thermal wear-out.

The worst case for lifetime degradation occurs when all the factors affecting the thermal cycling are at their maximum value. This implies that the power device has maximum switching losses and conduction losses values (compared to the nominal datasheet value) and is connected to a heatsink assembly having a higher thermal impedance and ambient temperature than the nominal value. To demonstrate the impact of such a worst-case scenario, the device losses, thermal parameters, and heatsink temperatures are considered as 10 % higher compared to the nominal value. The resulting thermal cycling behavior of these parameter variations is illustrated in Fig. 4.5 (b) with the magenta curve. The maximum junction temperature has increased by 15$^{\circ}C$ compared to that of the operation with nominal values. Using rainflow counting algorithm and lifetime model (2.6) together with the Miners rule (2.18), the accumulated damage of the device with 10 % parameter variations is found to be 4.9 times that of the device with nominal values in the datasheet.

It is worth noting that the decrease in the lifetime is due to the alternating nature of the load and not due to the variations in the mission profile. Therefore, the lifetime of any modular power converter feeding an AC load is affected due to the thermal cycling corresponding to the fundamental frequency of the load. Another important remark is that this junction temperature cycling is not reflected in the case temperature [16]. Hence, these junction temperature fluctuations might be overlooked while designing the system and can potentially lead to failures before the intended lifespan of the converter.

In order to mitigate such variations in the lifetime among the converter cells, power routing has been proposed. In the case of a CHB converter system, power routing can be achieved by various methods such as sinusoidal modulation, multi-frequency modulation and discontinuous modulation techniques. Sinusoidal modulation is a widely used modulation for CHB due to its superior power quality and ease of implementation.

Since the AC current flows through all the series connected CHB cells, the variation in device



a b

Figure 4.6: (a) IGBT and diode loss variation with power unbalance in a CHB cell [159] (b) IGBT thermal cycling with equal and unequal power sharing.

loss with sinusoidal modulation based power routing is minimal as shown in Fig. 4.6 (a). Here, loss variation with the power unbalance is analyzed for a 3-cell CHB with system parameters given in Table 2.4. It is clear from the device loss variation for unloading and overloading of the CHB cells that the overall losses of the device do not vary significantly. However, the loss share between the diode and IGBT changes by almost 16 % when the CHB cells is unloaded up to 50 % compared to the balanced operation [159].

To demonstrate the effect of unbalancing power, the worst case scenario with a 10 % increase in electrical and thermal parameters presented in Fig. 4.5 (b) is considered. In order to compensate for the increase in junction temperature due to the variation in losses, heatsink temperature and thermal impedance, the CHB cell is unloaded by 40 %. The junction temperature of the unloaded cell is presented in Fig. 4.6 (b) along with an equal power-sharing scenario with and without parameter deviations. It is clear from the waveform (blue and black) in Fig. 4.6 (b) that the unbalancing of power is able to compensate for the variations in junction temperatures of different converter cells.

In nutshell, the impact of parameter variations is not negligible for converters feeding alternating loads and power routing has the potential to address the unequal thermal stress among converter cells in a series connected modular system.

4.2.2 Analysis of Power Routing on Parallel Connected Modular Topologies

The uninterruptible power supply system was one of the first major applications of parallel power converters to increase the output power capacity and reliability of the system. Parallel connected DC/DC converters are also popular due to the increase in the current capacity, reliability, power quality, and filter size reduction. Therefore, an investigation about the impacts of parameter variations on the reliability of the parallel connected modular topologies is essential. In this study, IPOP configuration of the modular DC/DC DAB topologies is considered. However, without the loss of generality, the study is applicable to other IPOP topologies as well.

Table 4.2: Simulation parameters of parallel DAB converter.

Parameter	**Value**
Input voltage	$800V$
Output voltage	$800V$
Rated power per cell	$20kW$
Number of cells, N	3
Switching frequency, $f_{sw,DAB}$	$20kHz$

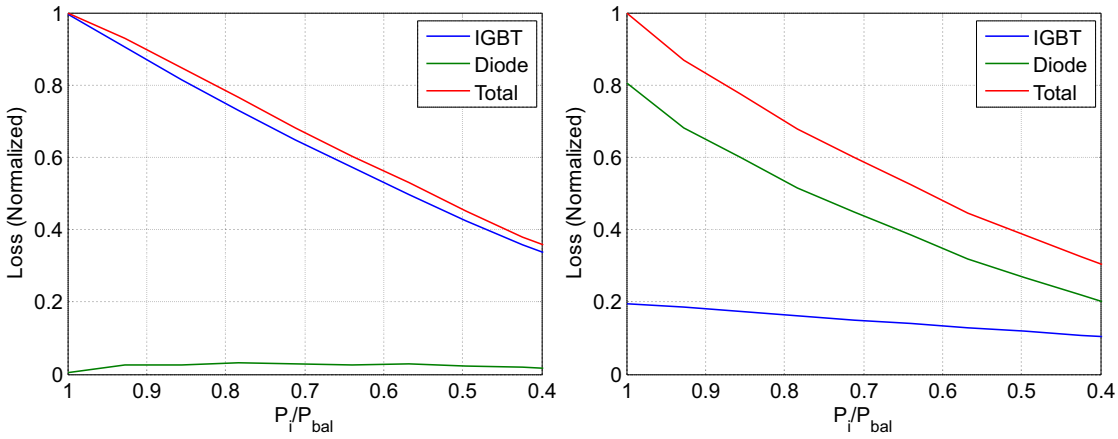


Figure 4.7: Loss distribution of the power semiconductors in DABs (a) Unloaded cell primary side H-bridge (b) Unloaded cell secondary side H-bridge.

The IPOP DAB topology is illustrated in Fig. 3.2 (a). Since the output and input side of each DAB is connected in parallel, each converter has equal input and output voltage. The main purpose of an IPOP system is to increase the current capacity and reliability of the system. To improve the light load efficiency, activation and deactivation of the cells or also known as phase shedding is proposed in the literature [160, 161, 162, 163]. In the case of modular interleaved DC-DC converters, the modular cells are activated and deactivated according to the operating points. Thus, the converter cells can be completely unloaded according to the load profile. The maximum current I_{un} at which a specific number of converter cells can be unloaded is given by

$$I_{un} = I_{rated,sys}\left(1 - \frac{N_{un}}{N}\right), \tag{4.1}$$

where $I_{rated,sys}$ is the rated current of the modular system, N_{un} is the number of cells to be unloaded and N is the total number of converter cells. For example, consider a modular system of 3 cells ($N = 3$) and 2 cells that need to be unloaded ($N_{un} = 2$), then using (4.1), the maximum current up to which 2 cells can be unloaded is $33\,\%I_{rated,sys}$. From (4.1), it is clear that as the total number of cells in the modular converter increases, the flexibility to unload more cells at higher load current increases. For instance, when $N = 15$ and $N_{un} = 2$, the system can be operated up to 86.6 % of the total current without activating the two converter cells.

To study the impact of loss variation of parallel connected DABs, a simulation study is performed using the system and power device parameters given in Table 4.2 and Table 2.5

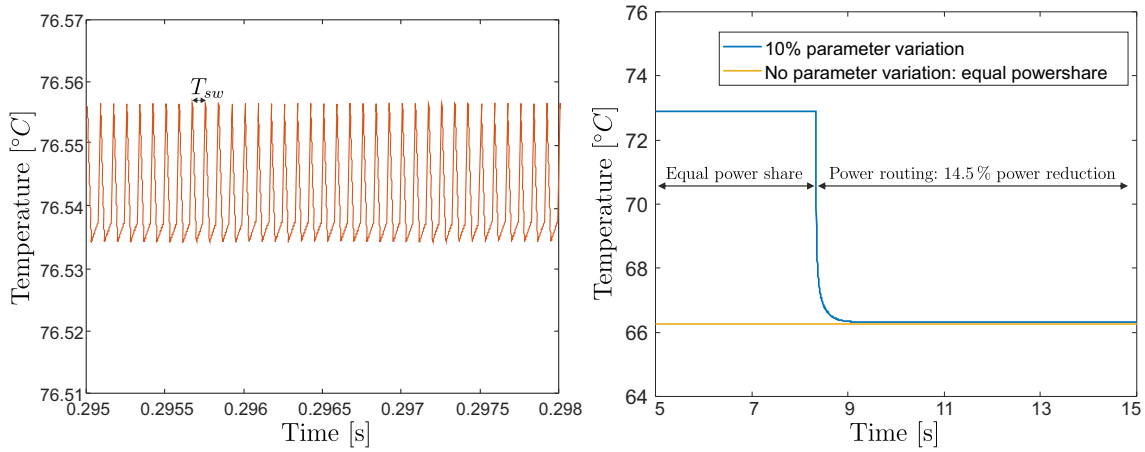


Figure 4.8: (a) Thermal cycling of IGBT in a DAB cell under constant load (b) IGBT thermal cycling with equal and unequal power sharing.

respectively. The loss variation of the power devices in the case of unloading for the primary and secondary side of a DAB is illustrated in Fig. 4.7 (a) and (b) respectively. When the power flows from the primary side to the secondary side, the IGBT of the primary side and the diode of the secondary side conducts the most, and hence the losses are more as seen in Fig. 4.7 (a) and (b). The most distinguishing feature compared to the loss distribution of the unloaded cell in series connected modular topology is the linear reduction of losses according to the power reduction. Therefore, differing from the series connected modular structure, parallel converters offer higher flexibility in terms of power routing control strategies.

Before analyzing the impact of parameter variations, it is necessary to discuss the thermal performance of parallel connected modular converters. Since the load connected to the converter system is a DC load, the impact on semiconductor reliability is different compared to a system with an alternating current load. In the case of DC loads, the RMS value of the current flowing through the power devices in a switching period remains constant. Unlike AC loads, there is no fundamental frequency variation in the load current, and thus the average losses over the switching period remain constant as long as the load is constant. The current through the switches changes at every switching period and the current shape depends on the topology, modulation technique, circuit parameters, load, etc.

An exemplary IGBT junction temperature for a modular DAB feeding a constant DC load is shown in Fig. 4.8 (a). In contrast to the modular converter feeding AC load, there is no fundamental frequency thermal cycling in the junction temperature of a DC/DC converter feeding constant current loads. Thermal cycling of a smaller magnitude in accordance with the switching frequency is visible, however, the magnitude of thermal cycling is very small as illustrated in Fig. 4.8 (a). Therefore, in the case of modular converters feeding DC loads, the major concern is the average junction temperature when the mission profile is assumed to be constant.

To demonstrate the impact of power routing, an example scenario is considered with parameter deviations. The equivalent Thevenin impedance $Z_{th,jhs}$ is increased by 10 % and the resulting junction temperature with thermal parameter variations is depicted in Fig. 4.8 (b).

It is evident that even a 10 % increase in the thermal parameters leads to a significant increase in the average junction temperature compared to that without any parameter variations and equal power share. In order to equalize the junction temperatures amid parameter variations, the power routing technique is applied by reducing the power by 14.5% of the cell with higher junction temperature. As shown in Fig. 4.8 (b), the reduction in the processed power results in the reduction of losses, and consequently reduces the junction temperature achieving thermal balance among the converter cells. It is worth noting that this is an example only to demonstrate the impact of power routing. The exact values for power reduction/increase for thermal balancing depend on the operating point of the converter, ambient conditions and thermal and electrical parameters of the converter system.

Since the parallel connected modular converters have a higher degree of flexibility to unbalance the cells according to (4.1), and loss reduction has a linear relationship with power reduction as indicated in Fig. 4.7, the junction temperature of the individual cells can be controlled easier than the series connected topologies. Therefore, the impact of power routing is more dominant in parallel connected modular topologies.

4.3 Power Routing Capability of Modular Converters

The amount of achievable power unbalance in the modular converters depends primarily on the converter architecture. The power routing can be achieved either by changing the voltage or current or both processed by the modular converter cells. In the case of parallel connected cells, the degree of power routing is mainly determined by the operating point. It is to be noted that the partial load operation is a primary requirement of power routing and the degree of unbalance depends on the number of cells and operating point.

For series connected cells, the current flowing through them is equal, and thus the power routing capability is limited to changing the voltage level of the cell. However, the minimum and maximum input and output voltage deviations of the system are dictated by the application and the selected topology. The power routing capability of different series and parallel connected modular power converters have been already discussed in [164] under the project HEART [165]. Therefore, the focus is given to the analysis of power routing capability due to commonly used modulation methods.

As explained in [164], the series connection of the cells imposes major limitations for uneven loading of the power. Usually, each cell has a voltage margin and this can be used to unbalance the power among them. Modulation methods utilize this voltage margin in different ways leading to different unloading/overloading capabilities. Two modulation strategies for the CHB converter are analyzed to evaluate their power routing capability.

4.3.1 Power Routing Capability of CHB with Sinusoidal PWM

Sinusoidal modulation is the state-of-the-art modulation technique used for the CHB topology due to its simplicity, easier implementation and satisfactory performance. For the anal-

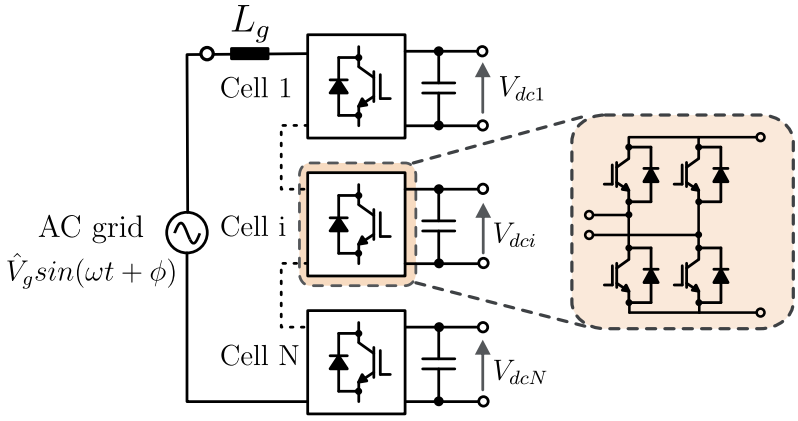


Figure 4.9: Single phase CHB converter.

ysis, a CHB modular topology for the rectification of AC grid voltage to DC voltage is considered. The CHB controls the input power factor, input AC current and regulates the DC-link voltage. The maximum power, P_{tot_max}, that can be processed by the converter is given by

$$P_{tot\_max} = \hat{V}_g \frac{\sqrt{(\sum_{i=1}^{N} V_{dci})^2 - \hat{V}_g^{\,2}}}{2\omega L_g}, \tag{4.2}$$

where $\hat{V}_g$ is the peak grid voltage, V_{dci} is the DC-link voltage of each CHB cell and ω is the grid frequency in radians. But the power distribution among H-bridges is determined by the modulation scheme.

For the sinusoidal PWM, assuming the converter is operated without over-modulation, the maximum power delivered by each cell is given as [166]

$$P_{max} = \sum_{i=1}^{N} P_i \frac{V_{dc}^*}{\hat{V}_g} \sqrt{1 - \left(\frac{\omega L_g I_g}{N V_{dc}^*}\right)^2}, \tag{4.3}$$

where V_{dc}^* is the reference DC-link voltage of each cell, I_g is the RMS grid current and N is the total number of CHB cells.

The minimum power delivered by a CHB cell is expressed as

$$P_{min} = P_{tot} - \sum_{i=1}^{N-1} P_{max,i}. \tag{4.4}$$

In order to validate the theoretical power limits, a 7-level CHB experimental setup with 3 CHB cells as shown in Fig. C.1 is used (see attachment C). For experimental validation, the control system for the voltage and current control for the grid-connected CHB needs to be implemented. Several control strategies have been discussed in literature [167, 168, 169, 170], and here, a cascaded control structure is considered as shown in Fig. 4.10. For the current control loop, Proportional-Resonant (PR) current controller is used. The Proportional Integral (PI) controllers cannot track sinusoidal reference without error, and since the single-phase CHB system has a sinusoidal current reference, a PR controller is preferred. The

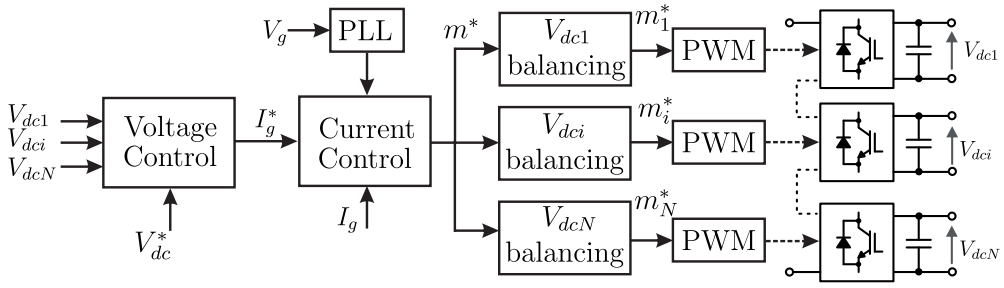


Figure 4.10: Single phase CHB controller structure with resonant current controller.

Table 4.3: CHB experimental system parameters.

Parameter	**Value**
Grid voltage (rms), V_g	$230V$
Power rating, P_{tot}	$2.1kVA$
Line inductance, L_g	$3.8mH$
Line resistance, R_g	$1m\Omega$
Cell DC-link voltage, V_{dc}	$130V$
Cell DC-link capacitance, C_{dc}	$0.5mF$
Switching frequency, f_{sw}	$10kHz$

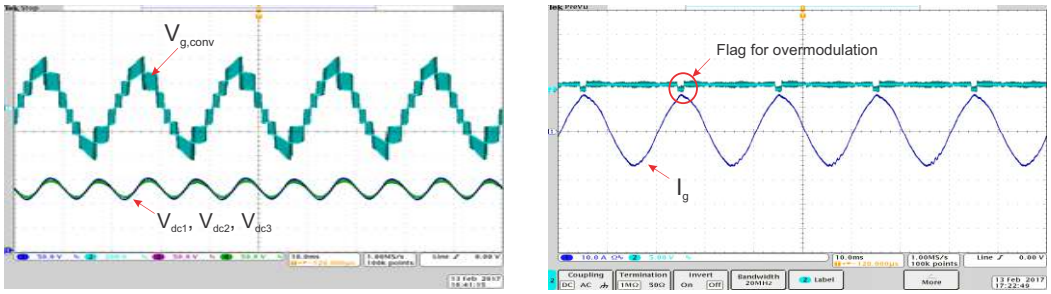
controller design process is given in detail in Appendix B.

Fig. 4.10 shows the configuration of capacitor voltage balancing with PI controllers for each H-bridge. The idea is to adjust the duty cycle of individual H-bridges to balance the DC-link capacitor voltage according to the power fed to the load. When the theoretical power unbalance limits are violated, the modulation index becomes larger than 1 and goes into over-modulation, and causes the deviation of DC-link voltages from the reference value. The modulation index of the individual H-bridge m_i^* is defined as

$$m_i^* = m^* - m^* sign(I_g^*) K_{p,bal} \left(1 + \frac{1}{T_{bal} s}\right) \left(\frac{1}{N} \sum_{i=1}^{N} V_{dci} - V_{dci}\right), \tag{4.5}$$

where m^* is the reference modulation index, $sign(I_g^*)$ says whether grid current is positive or negative, $K_{p,bal}$ and T_{bal} are the proportional and integral time constants of the voltage balancing controller. The voltage balancing controller must have a bandwidth much lower than that of the voltage control loop to avoid mutual coupling. Since the focus is not on the controller dynamics, and instead on the steady state operation for evaluating power unbalance limits, it has not been attempted to vividly show the dynamics of the developed controller.

For the laboratory validation, system parameters for the 7-level CHB prototype are given in Table 4.3. The cascaded controller with PI-based voltage balancing keeps the DC-link voltages of the H-bridges equal to the reference voltage, $130V$, as shown in Fig. 4.11 (a). The three DC-link voltages (V_{dc1-3}) are balanced and the 7-level converter output voltage ($V_{g,conv}$) follows the reference voltage. To find the maximum power processed by each cell without voltage unbalance and over-modulation, the power delivered by one cell is increased



(a) (b)

Figure 4.11: (a) CHB with sinusoidal PWM modulation V_{dci} - $(50V/\text{div})$, $V_{g,conv}$ - $(200V/\text{div})$, (b) I_g - $(10A/\text{div})$ [C2].

Table 4.4: Processed power of CHB for PI-based voltage balancing controller.

Parameter	**Power**	**Power (in terms of P_{tot})**
P_{max}	$839W$	$0.40P_{tot}$
$P_{max,exp}$	$820W$	$0.39P_{tot}$
P_{min}	$420W$	$0.20P_{tot}$
$P_{min,exp}$	$460W$	$0.22P_{tot}$

by varying the load resistance while keeping the total power constant. When the power through the cell is increased beyond the permissible power unbalance limits, the controller enters into over-modulation. This is verified by using a flag for checking over-modulation as shown in Fig. 4.11 and the grid current becomes non-sinusoidal. Thus, the maximum power unbalance limit of each bridge without entering over-modulation is experimentally calculated. The minimum power unbalance limit is the power processed by the third H-bridge cell when the other two cells are operating at their maximum power unbalance limit P_{max}.

Table 4.4 shows the experimentally obtained maximum power unbalance limit ($P_{max,exp}$) and minimum power unbalance limit ($P_{min,exp}$). Compared to the analytical power unbalance limits P_{max} and P_{min} obtained using (4.3) and (4.4) respectively (see Table 4.4), it is clear that the experimental results are in agreement. With sinusoidal PWM, for a 7-level CHB with the parameters in Table 4.3, the maximum power unbalance limit is $\approx 40\,\%$ of the total power processed and the minimum power unbalance limit is $\approx 20\,\%$ of the total power.

4.3.2 Power Routing Capability of CHB with Direct Modulation

Since the power unbalance limit depends on the modulation method employed, a popular direct modulation method for CHB converter is analyzed in this section. In this direct modulation scheme, the voltage balancing scheme is embedded in the modulator to balance the DC-link voltages under unequal power-sharing. The aim of modulator-embedded voltage balancing algorithm is to synthesize AC voltage V_g using the DC-link voltages V_{dci}. The switches of H-bridge are operated in 3 modes to generate $+V_{dci}$, $-V_{dci}$ and 0 voltage at the

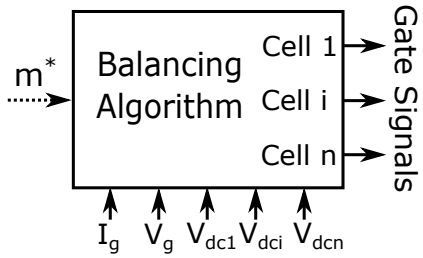


Figure 4.12: Direction modulation with modulator-embedded voltage balancing algorithm [171].

input. The capacitor voltages are sorted in ascending order and only one H-bridge operates in PWM mode at any instant. The rest of the cells are charged, discharged or operated in zero modes according to the current direction to follow the grid voltage. The cascaded controller maintains the total DC-link voltage. Since only one cell operated in PWM mode at any instant, device switching losses are reduced [171]. An illustration of the direct modulation with modulator embedded voltage balancing algorithm indicating the inputs and outputs is shown in Fig. 4.12. The maximum power ($P_{max}^{'}$) and minimum power ($P_{min}^{'}$) that can be delivered by each H-bridge for a 7-level H-bridge under consideration are as follows [171]:

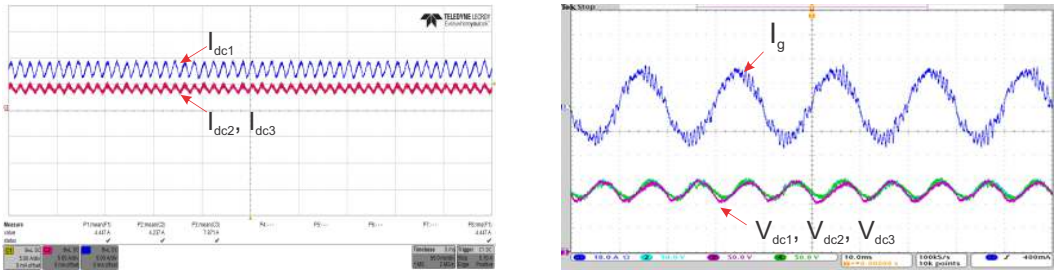
$$P_{max}^{'} = \frac{\hat{I}_g}{\pi}[\int_{\theta}^{\gamma} \hat{V}_g sin(\iota) sin(\iota-\theta) d\iota + \int_{\gamma}^{\pi-\gamma} V_1 sin(\iota-\theta) d\iota + \int_{\pi-\gamma}^{\pi} \hat{V}_g sin(\iota) sin(\iota-\theta) d\iota] \tag{4.6}$$

$$P_{min}^{'} = \frac{\hat{I}_g}{\pi}[\int_{0}^{\theta} \hat{V}_g sin(\iota) sin(\iota-\theta) d\iota + \int_{\kappa}^{\pi-\kappa} \hat{V}_g sin(\iota - V_1 - V_2) sin(\iota-\theta) d\iota]. \tag{4.7}$$

Here, $V_1 < V_2 < V_3$ represent the sorted DC-link voltages in ascending order, γ and κ are the angles at which the reference AC voltage crosses the voltage levels V_1 and $V_1 + V_2$ respectively. The angle θ is defined as the angular displacement between the synthesized CHB voltage and grid current. These parameters are represented as follows:

$$\gamma = sin^{-1}\left(\frac{V_1}{\hat{V}_g}\right),\ \kappa = sin^{-1}\left(\frac{V_1+V_2}{\hat{V}_g}\right),\ \theta = sin^{-1}\left(\frac{\omega L \hat{I}_g}{\hat{V}_g}\right). \tag{4.8}$$

The equations (4.6) - (4.8) can be extended to CHB with N number of cells by simply adding the additional voltage levels. For laboratory validation of the unbalance power limits, the 7-level CHB experimental setup shown in Fig. C.1 is used (see attachment C). To maintain consistency, the experimental system parameters remain the same as that of the sinusoidal PWM test given in Table 4.3. Since only the modulation method has changed, the cascade control structure with PR current controller and PI voltage controller as illustrated in Fig. 4.10 is used to generate the common modulation signal for all cells. The modulator-embedded voltage balancing algorithm produces the individual gate signals for each H-bridge converter cell by taking grid current (I_g), grid voltage (V_g), DC-link voltages (V_{dc1-3}) and the common



(a) (b)

Figure 4.13: (a) Current sharing in CHB cells with cell 1 operating at $P_{max,exp}^{'}$, , I_{dc1-3}-(5A/div) (b) CHB with direct modulation V_{dci}-(50V/div), I_g-(10A/div) [C2].

Table 4.5: Processed power with direct modulation.

Parameter	**Power**	**Power (in terms of P_{tot})**
$P_{max}^{'}$	1038W	0.49P_{tot}
$P_{max,exp}^{'}$	1020W	0.48P_{tot}
$P_{min}^{'}$	276W	0.13P_{tot}
$P_{min,exp}^{'}$	300W	0.14P_{tot}

Table 4.6: Comparison of power unbalance limits with two modulation methods for the CHB.

Method	**Maximum unbalance power**	**Minimum unbalance power**	**THD**
Sinusoidal modulation	0.39P_{tot}	0.22P_{tot}	3.1%
Direct modulation	0.48P_{tot}	0.14P_{tot}	6.1%

modulation signal (d) as input as shown in Fig. 4.12 [171]. In order to validate the maximum power unbalance limit, the output current of the cell 1 is increased while reducing the output currents of cells 1 and 2. Fig. 4.13 (a) shows the output currents (I_{dc1-3}) of the CHB cells and it is clear that the cell 1 is processing much higher power than that of the other two cells. Fig. 4.13 shows the grid current and the balanced three DC-link capacitor voltages using the modulator-embedded voltage balancing algorithm for the unbalanced operation. When the power through the cell is increased beyond the permissible power unbalance limits, the controller enters into over-modulation and the DC-link voltages start to deviate from the reference value. Similar to the sinusoidal PWM, a software flag is used to detect the over-modulation and the maximum power unbalance limit ($P_{max,exp}^{'}$) is calculated. Similarly, the minimum power unbalance limit ($P_{max,exp}^{'}$) is also experimentally verified and the results are given in Table 4.5. It is clear that the analytically calculated values, $P_{max}^{'}$ and $P_{min}^{'}$ are in agreement with the experimentally calculated values given in Table 4.5.

Table 4.6 summarizes the power unbalance limits and THD obtained by experiment for the two methods. The direct modulation with modulator-embedded balancing algorithm provides an extended range of power unbalance, but the THD is much higher than the conventional PI based on PWM modulation. Therefore, a larger filter inductance is required for the modulator-embedded balancing algorithm method to comply with the grid code.

In short, it is practically demonstrated that the modulation methods can influence the power

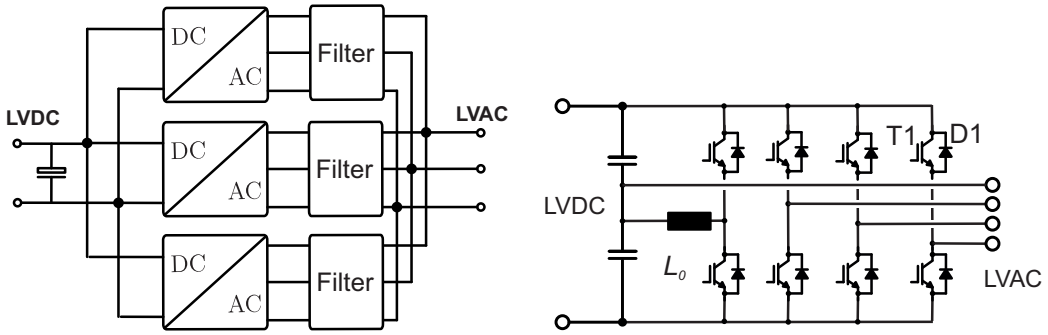


Figure 4.14: (a) System of three power converters for the LV stage. (b) Topology of one two level VSI [J9].

unbalance limits of the series connected modular converters. The identification of power unbalance limits lays the foundation for the development of the power routing algorithms.

4.4 Virtual Resistance based Power Routing of Modular Converters

In order to develop a system level controller to route the power among the building blocks, a virtual resistance based power-sharing strategy is proposed. In the proposed strategy, each converter cell in the modular converter is represented by a resistor indicating the aging of that particular cell. The more the age of a cell, the higher the virtual resistance value. The power or current reference for each converter is modified according to the virtual resistance value of that cell. When the aging of the converter cells are equal, the virtual resistances are equal and so is the power-sharing. When the virtual resistance is higher in one power path, the power flowing through that path is lower, and therefore the aging of the converter cells in the path is reduced. Since the resistors are implemented in software to generate the current/power references, they are termed as virtual resistors. In this section, the virtual resistance based power routing controller design for parallel connected inverters and a multi-stage input series output parallel modular architecture are presented. The impact of the proposed power routing controller on the lifetime of the system is evaluated.

4.4.1 Virtual Resistance based Power Routing for IPOP Modular Converters

For the analysis of IPOP connected modular converters, the LV stage of the three-stage ST architecture is considered here. The LV stage of the ST is forming the LV grid and consists of three parallel converter cells as schematically shown in Fig. 4.14 (a). The converters require access to the fourth wire, because of the numerous single-phase loads in the grid. Using the two-level voltage source converter, as it is commonly done for motor drives, enables to add a fourth half bridge to the converter as it is shown in Fig. 4.14 (b). This half bridge is connected to the star point of the DC link for preventing high common mode voltages. The loading of the power semiconductors is symmetrical over time, which requires only investigation of the effect on one IGBT T1 and one Diode D1 in a half bridge.

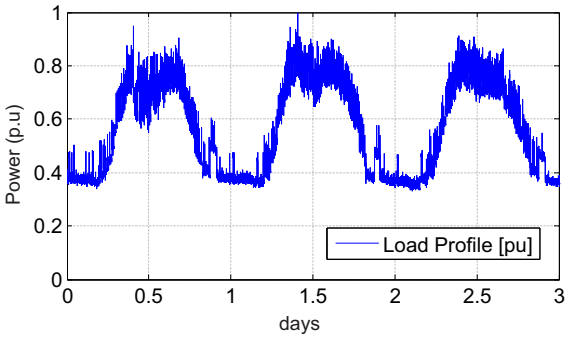


Figure 4.15: Example for a mission profile of an ST fed micro-grid [J9].

Since the ST operates at partial load for most of the time as shown in Fig. 4.15, the parallel converters allow redundancy at partial load operation. However, since there is no oversizing of converters, all the converters are required to cater to the full power operation. The possibility of interleaved operation of the converters enables a reduction of either the switching frequency or the filter size in comparison with a single power converter. Apart from the advantages of parallel converters, there are issues, such as circulating currents if a shared DC link is used for the three converters [172]. However, this is not within the scope here, and the known solution to use single phase inductors for each converter is applied to overcome this problem.

Power Routing Controller Design Using Virtual Resistance

The main control objective of the LV stage converter of the ST is to form the LVAC grid. Therefore, the shape of the grid voltage needs to be controlled and the active power depends on the connected loads. A cascaded control structure with voltage control using the outer control loop and the current performed by an inner control loop is adopted. However, the cascaded controller design is not the focus here, and attention is given to the power routing based on the current control loop. The implementation of the power routing in the current controller is shown in Fig. 4.16. The virtual resistors are used to route the power similar to current divider in the basics of electronics by distributing the current references for the three converters. A closed loop control for the power routing is necessary to prevent power circulation among different converters.

To define how the power is routed in the system, the virtual resistors need to be tuned based on the condition of the converters in the parallel power paths. High resistance of a path leads to low loading and a low resistance leads to high loading of the path. For similar conditions of the converter, the power needs to be distributed equally and all virtual resistors need to have the same size. As an example for the current transferred in converter 1, i^*_{c1}, is dependent on the overall reference current generated by the voltage controller i^*_{ref} and all virtual resistors in the parallel paths. This is expressed as

$$i^*_{c1} = i^*_{ref} \cdot \frac{R_{v2}R_{v3}}{R_{v2}R_{v3} + R_{v1}R_{v2} + R_{v1}R_{v3}}. \tag{4.9}$$

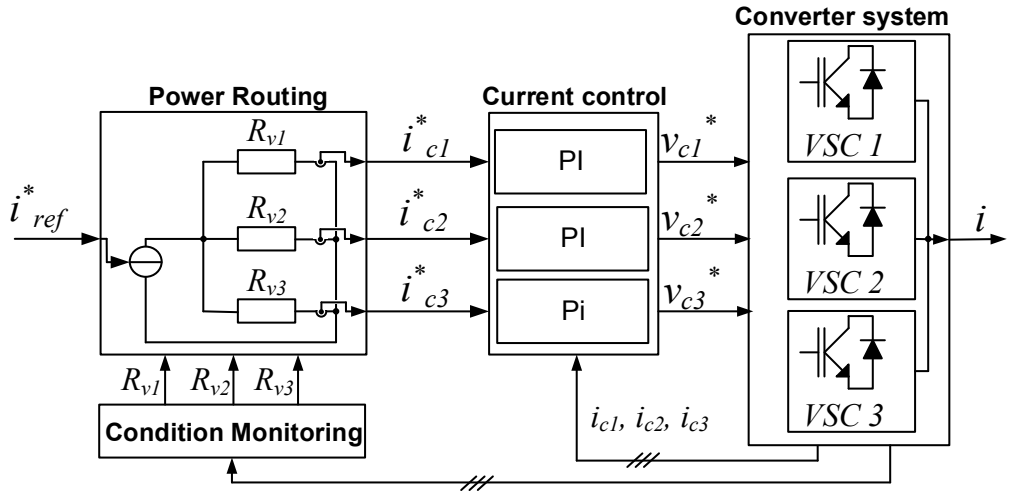


Figure 4.16: Control diagram of the power routing algorithm based on condition monitoring [J9].

Table 4.7: ST LV stage simulation parameters.

LVDC	LVAC	Grid frequency	Power device	No: of converters
800 V	400 V	$50\,Hz$	Danfoss $DP25H1200T101667$	3

The power routing for all three reference currents is shown in a matrix representation given by

$$\begin{bmatrix} i^*_{c1} \\ i^*_{c2} \\ i^*_{c3} \end{bmatrix} = \frac{i^*_{ref}}{R_{v2}R_{v3} + R_{v1}R_{v2} + R_{v1}R_{v3}} \begin{bmatrix} R_{v2}R_{v3} \\ R_{v1}R_{v3} \\ R_{v1}R_{v2} \end{bmatrix}. \tag{4.10}$$

It needs to be pointed out that the power routing does not require an oversizing of the converter system. In case that a converter receives a higher current reference than the maximum current, the power exceeding the limit is redistributed to the other converters. Consequently, under full load, every single converter is processing the rated power, independently of the tuning.

In order to establish the relation between the virtual resistance and the estimated lifetime of the converters, first, a simplified electro-thermal model of the parallel converters is developed in MATLAB. The simulation parameters of the parallel converter system are given in Table 4.7. The inverter modeling described in Section A is followed to determine the duty cycle of the power devices for the mission profile given in Fig. 2.10 (a). The power semiconductor losses are subsequently modeled using the numeral simulation technique described in Section 2.5.4. The thermal parameters of the IGBT given in Table 2.5 serve as the inputs for thermal modeling. Finally, the junction temperature is simulated with the help of the developed electro-thermal model.

The number of cycles to failure can be calculated from the junction temperature using (2.6). Since the mission profile of an ST is affecting different thermal cycles, which are not recurring, the Rainflow algorithm is used as the cycle counting method and Miner's rule (2.18) is

applied to calculate the accumulated damage.

The virtual resistor based power routing algorithm uses the sensed junction temperatures T_j of the power semiconductors to estimate the accumulated damage of each converter for a fixed time period. This accumulated damage D gets updated after a fixed time period given by

$$D = D_{old} + D_{period}. \tag{4.11}$$

The virtual resistors which facilitate the power routing are expressed as a function of the accumulated damage as

$$R_{vi} = f(D). \tag{4.12}$$

In order to define the function, $f(D)$, one approach is to define a linear relationship given by

$$R_{vi} = D. \tag{4.13}$$

The linear relationship is used for easy implementation. An exponential relationship for the function $f(D)$ is also evaluated as

$$R_{vi} = \alpha_v \cdot (D)^{\beta_v}, \tag{4.14}$$

where the parameters α_v and β_v depend on the coefficients a_1 and a_2 since (4.14) is derived from (2.6) considering $D = f(N_f)$, $\Delta T = f(I)$ and $I = f(R_{vi})$.

Impact on Reliability and Power Quality

Case studies to establish the relationship between the accumulated damage, virtual resistance, and its effect on the aging of converters are carried out in this subsection. For this analysis, a three-day mission profile of an ST-fed micro-grid, as shown in Fig. 4.15, is considered [89, 90].

First, the three converters are fed with balanced power distribution, irrespective of the initial accumulated damages, the accumulated damages and end-of-lifetimes are calculated. Then virtual resistors are introduced according to (4.13)-(4.14), and the accumulated damages and RULs are calculated.

Three cases with different initial damages for each converter are considered here. Fig. 4.17(a), (b) and (c) show the damage accumulation over the years for a modular converter system with different initial damages for cases $1-3$. It is evident that without power routing, the converters will fail at different time instants. With the virtual resistor method, the accumulated damages converge resulting in the control of the processed power dependent failure mechanisms of the system. The impact of power routing on the lifetime extension of the total system of the cases $1-3$ is summarized in Fig. 4.17 (d). The exponential function describes the relationship between damage and virtual resistors more accurately and hence the RULs are better compared to the linear one in all three cases. The percentage increase in the total RUL of the system is depicted in Fig. 4.17 (d). In all the cases with different initial RULs, there is an increase in the total RUL of the system up to 44%.

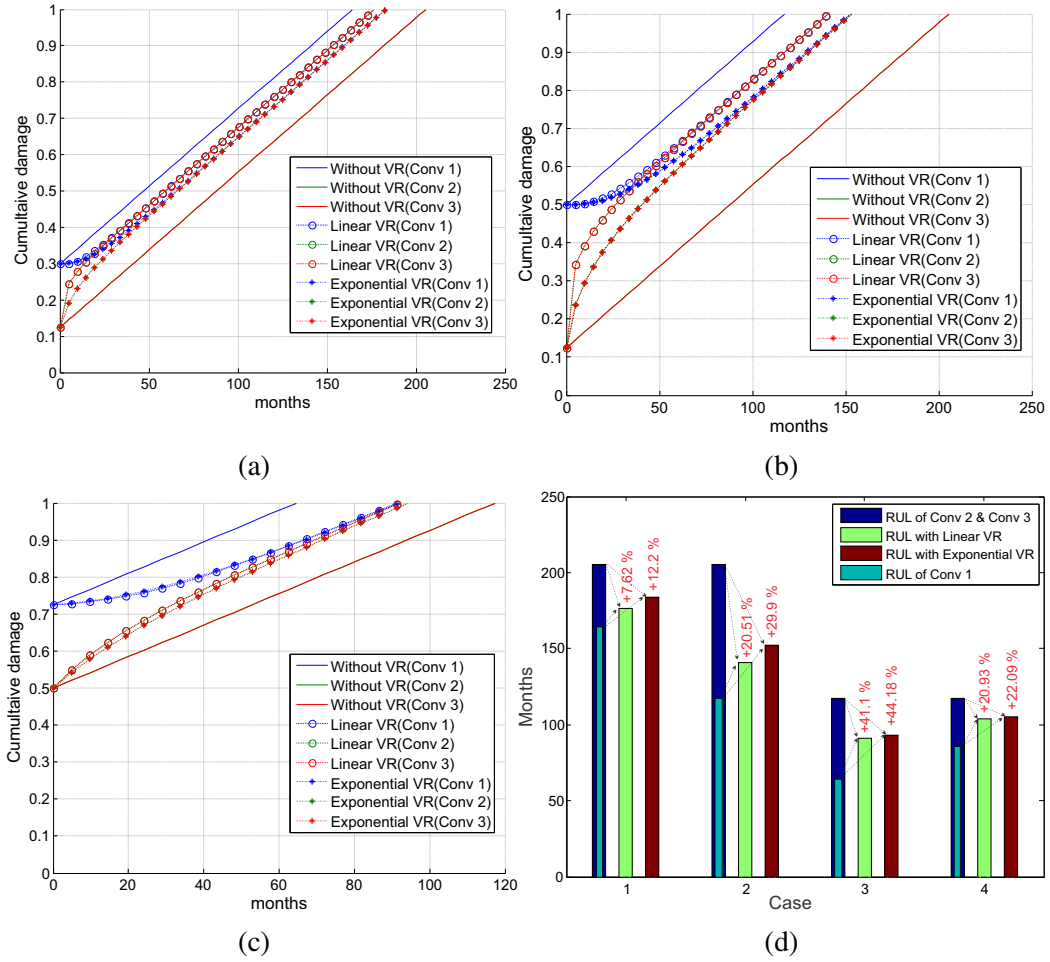


Figure 4.17: Variation of accumulated damage of parallel converters without and with Virtual Resistor (VR) power routing for (a) Case 1 (b) Case 2 (c) Case 3, and (d) RUL of parallel converters for cases 1-3 [J9].

It is assumed that the modular system reaches its end-of-life when the module with the lowest RUL fails. The results clearly show that the virtual resistors can increase the lifetime of the most aged cell and most importantly, decrease frequent maintenance schedules. However, it is evident that the increase in RUL of the system comes at the expense of lowering the RULs of the higher loaded cells.

To validate the performance of virtual resistors for a parallel converter system with different thermal characteristics, another case study is performed. Here, all converters are assumed to have identical initial accumulated damages. Due to the difference in thermal characteristics, the converters have different RULs, which is shown as case 4 in Fig. 4.17 (d). Here, the heatsink temperature of one of the parallel converters is assumed to be 5°C higher than that of the others. This is a reasonable assumption since the heatsinks are cooled with air/water entering from one end and leaving at the other, resulting in an uneven distribution of the heat. The RULs of the converters without power routing are 86 and 117 months for the converter with higher heatsink temperature and others respectively. A significant increase of the total lifetime of the system of 22% or 19 months is obtained with the virtual resistor based power routing. Thus, the power routing strategy does not only increase the reliability of systems

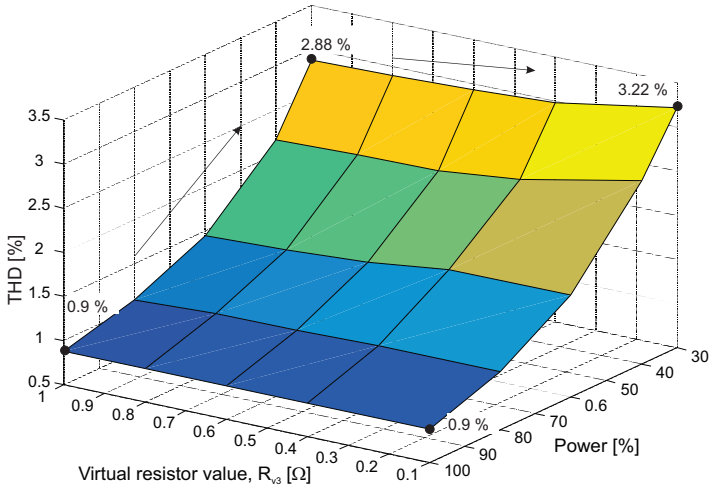


Figure 4.18: THD variation of line current with virtual resistance unbalance for entire power range. The virtual resistance of converter 1 and converter 2 is normalized to $R_{v1} = R_{v2} = 1\,p.u.$ [J9].

with different initial aging but also for systems with different thermal behavior.

It can be concluded from the case studies that the linear and exponential functions of virtual resistors provide comparable results. The linear function does not require any tuning based on the expected mission profile of the system, which makes the implementation simple and straightforward. The exponential function instead offers one more tuning parameter, which can be tuned based on the expected mission profile and the remaining useful lifetime of the other parts to control the convergence time of the different lifetimes.

Effect of power routing on line current ripple

To demonstrate the effect of a power unbalance on the line current ripple and consequently the THD, a simulation study with unbalanced virtual resistors is carried out. Two of the three virtual resistors are constant $R_{v1} = R_{v2} = 1\,p.u.$, while the third one is varied to show the effect on the current ripple. The result is illustrated in Fig. 4.18, where the x-axis shows the output power and the y-axis shows the virtual resistor of converter 3. For $R_{v3} = 1\,p.u.$, the system is operated under balanced condition and as the value decreases, the power distribution changes according to (4.10). The THD (in %) is shown on the z-axis. As expected, the THD of the line current increases for a reduction of the output power. For an increasing power imbalance, an increase in the THD of the output current can be seen. Under full load, this does not occur, because the power is equally distributed in the converters in order to prevent the oversizing of components.

Experimental Validation of Virtual Resistance Based Power Routing

The concept of power routing is validated experimentally on three parallel converters with open IGBT modules that share the same DC link and have single-phase inductors at the output of each phase. The IGBT modules are not filled with gel for direct measurement of the

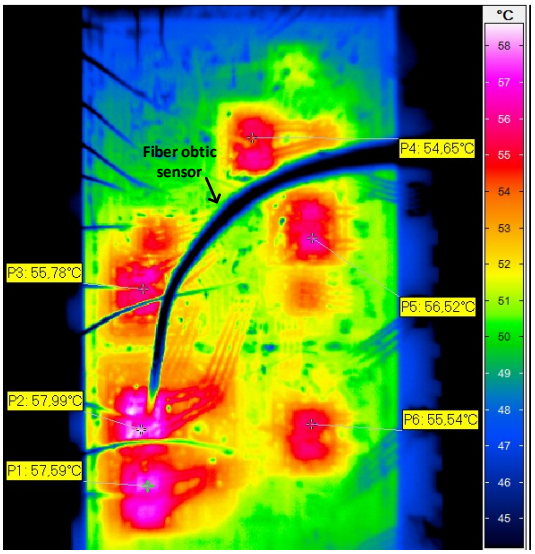


Figure 4.19: Infrared camera picture of the power electronic module showing the thermal distribution of a full power electronic module highlighting the temperature on the IGBTs [J9].

Table 4.8: Parameters of the laboratory setup.

Parameter	**Value**
Rated current per converter	25 A
DC link voltage	200 V
Filter size	1.8 mH
Load R	3.5 Ω
Fundamental frequency	50 Hz
Switching frequency	20 kHz
Power Semiconductor module	Danfoss $DP25H1200T101667$

junction temperature, which is reducing the voltage blocking capability of the power module. However, the removal of silicone gel does only marginally affect the thermal behavior, because the thermal conductivity of silicone gel or air is very low. A three-phase resistive load is fed by the converters and the parameters of the setup are shown in Table 4.8.

The infrared camera is used to detect the hottest spots in the power electronic module. An image of the power electronic module is shown in Fig. 4.19. The highest temperature is indicated with the measurement point ”P2” and measures the temperature of IGBT 1. For this reason, in each of the converters the junction temperature of the IGBT T1 is measured.

For the implementation of power routing, the reference current i^*_{ref} is varied for different virtual resistors and the resultant power distribution is expressed as

$$\begin{bmatrix} R_{v1} \\ R_{v2} \\ R_{v3} \end{bmatrix} = \begin{bmatrix} 0.5 \\ 0.5 \\ 1 \end{bmatrix} \rightarrow \begin{bmatrix} P_{c1} \\ P_{c2} \\ P_{c3} \end{bmatrix} = \begin{bmatrix} 40\ \% \\ 40\ \% \\ 20\ \% \end{bmatrix}. \tag{4.15}$$

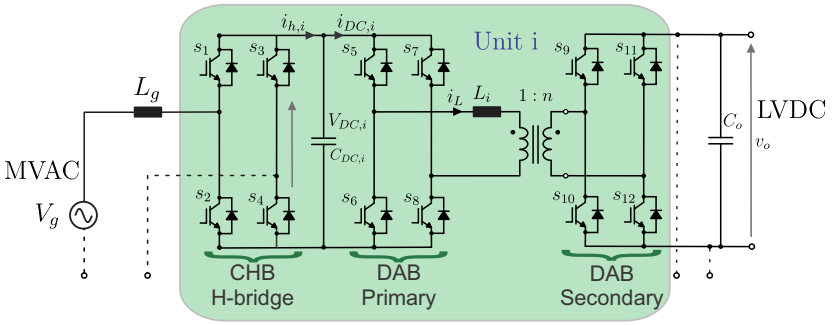


Figure 4.20: Detailed schematic of CHB and DAB converter unit in the ST [J2].

In this case, only the current is varied, while all other parameters are kept constant. The power cycle is causing a thermal cycle in the junction temperature measurements as expected. The thermal cycling shows a proportional behaviour to the power distribution, which results in a $\Delta T = 10\ K$ for converter 1 and converter 2, while the thermal cycling in converter 3 is only $\Delta T = 5\ K$. Also, the average temperature of converter 3 is reduced. As a consequence, the lifetime of the power semiconductors is consumed unequally. Following the simple lifetime model expressed in (2.6), the ΔT influences the lifetime consumption exponentially with a factor $a_2 \approx 5$, leading to 32 times higher damage for the power semiconductors in converters 1 and 2 in comparison to those in converter 3. This is even amplified by the difference in the average junction temperature, which is also higher for the two highly loaded converters. Consequently, a relatively high remaining lifetime requires only a very small imbalance of the power in the converters. A small remaining lifetime results in the potential to effectively unload the thermal stress from the device for extending its lifetime.

4.4.2 Virtual Resistance based Power Routing for Multi-Stage ISOP Modular Converters

For the analysis of multi-stage Input Series and Output Parallel modular converters, the MVAC-MVDC and MVDC-LVDC stages of the three-stage ST architecture is considered here. The investigated architecture is composed of modular CHB and DAB converters. AC-DC stage is realized by the CHB converter and the DC-DC stage by the DAB converter. CHB converter connected to the MVAC grid rectifies the AC voltage into DC. DAB DC-DC converters convert the rectified DC-link voltage of each CHB cell into low voltage DC while providing the isolation between MV and LV sides. Fig. 3.10 shows the system architecture. Fig. 4.20 shows the detailed schematic of a unit composed of one CHB cell and one DAB cell. The unit is taken as the building block for MVAC to LVDC conversion because if one of the cells in a unit fails, the power cannot flow through that unit since the cells are connected in series. For the simulation/analytical studies, the system parameters are given in Table. 4.9.

Power routing has been implemented on the CHB in [159]. It is evident that the total losses of the power semiconductors do not vary much with unequal power-sharing for the CHB. For the selected IGBT in [159], even 80% unloading of a cell leads to only $\approx 5\%$ decrease

Table 4.9: ST specification.

Rated Power	MVAC	LVAC	Grid frequency	LVDC
1 MVA	10 kV	$400V$	$50Hz$	$800V$

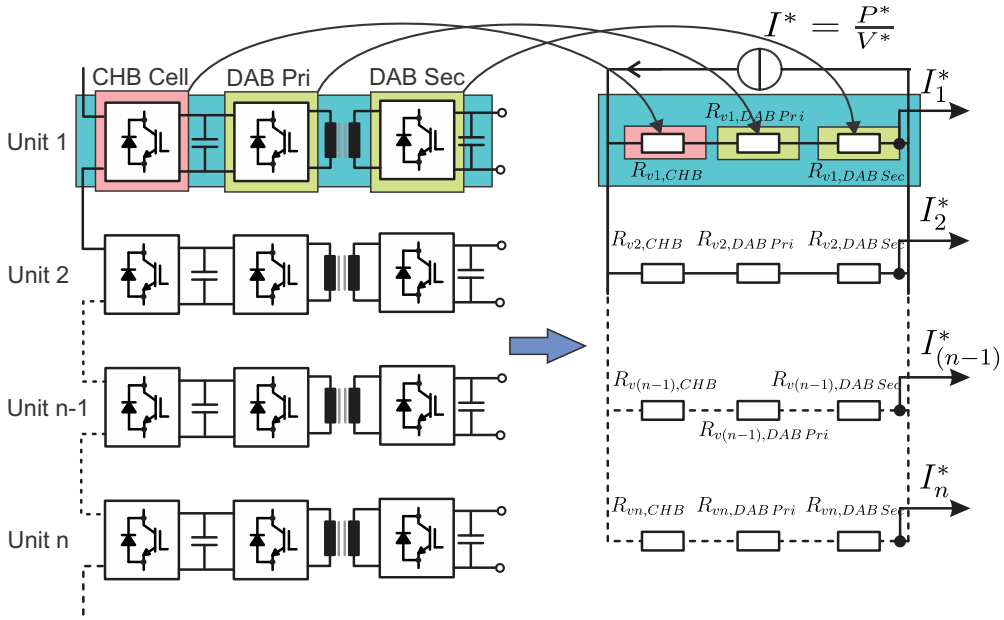


Figure 4.21: Equivalent circuit design of virtual resistor based power routing in the modular converter with CHB and DAB [J2].

in the total losses as illustrated in Fig. 4.6 (a). In general, since the H-bridges in a CHB are connected in series, the power routing has limited effect on the device losses.

Design of Virtual Resistance based Power Routing Controller

The methodology for estimating the device wear-out from thermal cycling is illustrated in Fig. 2.9 (see Chapter 2 for details). The mission profile of the converter system for a time period generates the junction temperature profile for each converter. Since the converters are equipped with V_{ce} junction temperature sensing system as shown in Fig. C.4, the junction temperature profiles are obtained directly. This junction temperature profile of the past time period can be used to calculate the consumed lifetime ΔD_i of each cell using rainflow counting and the lifetime model as described in Chapter 2 [104]. Subsequently, the total accumulated damage can be calculated for each converter using

$$D_i = \sum_i \Delta D_i, \tag{4.16}$$

where D_i is the accumulated damage of the i^{th} cell. Based on the accumulated damages of the semiconductor modules, the power distribution is changed to delay the power dependent failures.

As depicted in Fig. 4.21, $R_{vi,CHB,IGBT}$, $R_{vi,CHB,DIODE}$, $R_{vi,DAB\,Pri}$ and $R_{vi,DAB\,Sec}$ are calculated

from their respective accumulated damages using the relation

$$\text{Virtual resistor} \propto D_{acc,i}. \tag{4.17}$$

$R_{vi,CHB,IGBT}$ and $R_{vi,CHB,DIODE}$ are the virtual resistance values for the IGBTs and diode in the CHB respectively, whereas $R_{vi,DABPri}$ and $R_{vi,DABSec}$ represent the virtual resistance values of primary and secondary sides of DABs. For the next step, a weighted average of the virtual resistances of CHB and DAB modules in one power path is considered for the total virtual resistance calculation as

$$\begin{aligned} R_{vi} = w_{i,CHB,IGBT} \cdot R_{vi,CHB,IGBT} + w_{i,CHB,DIODE} \cdot R_{vi,CHB,DIODE} \\ + w_{i,DAB} \cdot max(R_{vi,DABPri}, R_{vi,DABSec}), i \in [1\ N]. \end{aligned} \tag{4.18}$$

The maximum virtual resistance value among the two bridges, $(max(R_{vi,DABPri}, R_{vi,DABSec}))$, is chosen for calculation (4.18) because both bridges process the same power, and the bridge with higher virtual resistance is expected to fail first. For the CHB, power routing has relatively little impact on the total losses [159]. However, the loss distribution among IGBTs and diodes can be affected by routing the power. The damage accumulation of the most damaged IGBT and diode in a cell is considered for modeling the CHB virtual resistance.

Finally, the power reference P_i^* is obtained by solving the virtual resistor network as illustrated in Fig. 4.21. For a system with $N = 3$ cells, the power references P_1^*, $P_2^* P_3^*$ are given by

$$\begin{bmatrix} P_1^* \\ P_2^* \\ P_3^* \end{bmatrix} = \frac{P^*}{R_{v2}R_{v3} + R_{v1}R_{v2} + R_{v1}R_{v3}} \begin{bmatrix} R_{v2}R_{v3} \\ R_{v1}R_{v3} \\ R_{v1}R_{v2} \end{bmatrix}. \tag{4.19}$$

Therefore, the higher the value of virtual resistance, the lower the processed power through each unit. The total power of the system is divided among the cells according to the value of the virtual resistance for the cell.

The equation (4.18) is used for the design of virtual resistance for routing the power in CHB and DAB virtual resistors based modular converter. The influence of weights for the CHB and DAB in (4.18) on the system lifetime is analyzed. Fig. 4.22 shows the results of the simulation study on the influence of weights of CHB and DAB virtual resistors on the system lifetime. When both the CHB and DAB cells in one unit have equal weights, the first DAB cell fails at 230^{th} month. As the weight of the CHB virtual resistance decreases, the RUL of the DAB cells increases considerably. Even with an increase in the weight of the CHB virtual resistor from 0.1 to 1, the increase in RUL of CHB is marginal, $\approx$ 4.5 months. The result is in agreement with the loss variation with power unbalance for CHB connected to the DAB architecture. Since the influence of CHB power unbalance has a lower impact on the loss CHB distribution, a higher weight of the CHB has less impact on the lifetime variation of the CHB. However, since the DAB cell is connected in series to the CHB cell, the power imbalance in CHB affects the DABs more than that of the CHB cell.

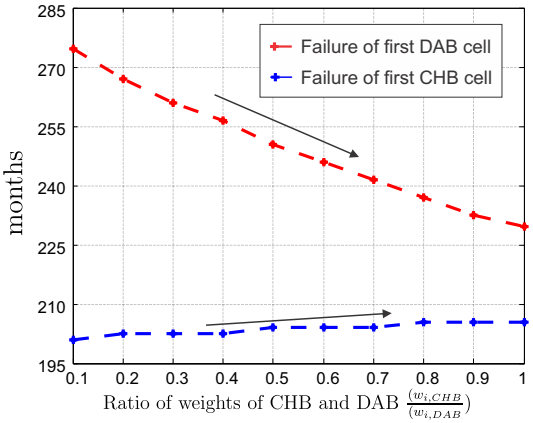


Figure 4.22: Influence of weight of virtual resistors on the failure of first cell of CHB and DABs in multi-stage modular converter [J2].

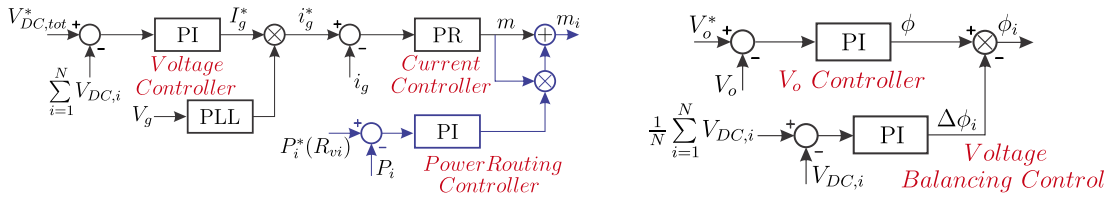
Table 4.10: System parameters.

Symbol	Description	Value
V_g (rms)	Grid voltage (rms)	$230V$, $50Hz$
L_g	Filter inductance (MV side)	$3.8mH$
$V_{DC,1} = V_{DC,2}$	DC-link voltage reference	$250V$
V_0	DC-link voltage (LV side)	$250V$
n_{DAB}	Transformer turns ratio	$1:1$
$f_{sw,CHB}$	Switching frequency of the CHB	$3kHz$
$f_{sw,DAB}$	Switching frequency of the DAB	$12kHz$

Experimental Validation of the Proposed Virtual Resistance based Power Routing

In order to realize the testing of the proposed power routing controller with virtual resistors, a control scheme for a scaled-down prototype of the modular converter with five level CHB and two DABs has been developed. The system parameters of the laboratory prototype are given in Table 4.10. The overall control strategy for CHB and DAB converters in the ST application is shown in Fig. 4.23 (a) and (b) respectively. The CHB rectifier stage controls and shapes the input AC current and controls the total MVDC-link voltage. Current and voltage control are achieved through cascaded controller structure with proportional-resonant controller and Proportional-Integral (PI) controller respectively (see Section 4.3.1 for details) [173]. Power references (P_i^*) generated by the virtual resistors are given to the power routing controller as depicted in Fig. 4.23 (a). The modulation index, m, produced by the PR controller is modified by the PI-based power routing controller to achieve different power flow through the DC-links of CHB.

A control scheme with output and input voltage control is adopted for the DAB as shown in Fig. 4.23 (b). The input MVDC-link voltages are balanced by the DAB, which is critical for stability while processing unequal power through each H-bridge of the CHB. For the output LVDC-link voltage control, a PI voltage controller is designed using pole-zero cancellation technique [174].



(a) (b)

Figure 4.23: (a) CHB control scheme with power routing controller (b) DAB control scheme [J2].

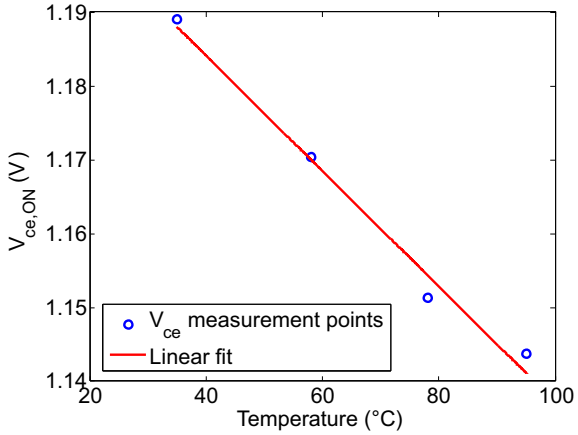
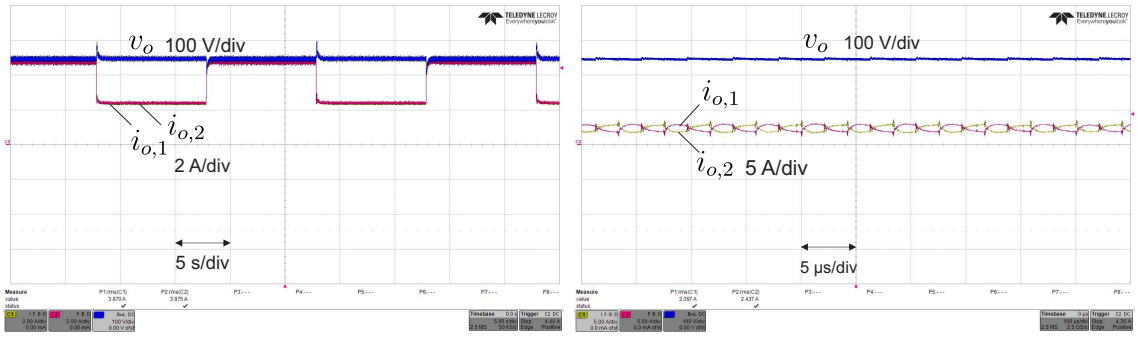


Figure 4.24: V_{ce} variation with junction temperature [J2].

The small-scale laboratory prototype of a five level CHB connected to two DABs is illustrated in Fig. C.3 (see attachment C). The H-bridges of CHB and DAB are made with open-module *DP25H1200T101616* from Danfoss to facilitate direct junction temperature measurements. A high speed infrared thermal camera is used to obtain the thermal response of the power semiconductors of the open module. The camera is controlled by an automatic positioning system for fast and accurate measurements. The setup is controlled by dSPACE SCALEXIO system. The V_{ce} measurement board integrated to each converter cell provides the junction temperature information and this is validated using the thermal camera. The variation of the V_{ce} vs. temperature is shown in Fig. 4.24 and subsequently, the junction temperature is estimated using a fitting model for the selected device.

The controller of the ST should be able to maintain the reference LVDC voltage even when the power flowing through each unit is different. Moreover, the CHB DC-link voltages should be balanced and must be equal to their reference value. The proper functioning of power routing controller is tested by changing the power distribution among the ST units.

When the power routing is not activated, the DABs share the power equally, as shown in Fig. 4.25. Here, a mission profile with a step change from $P_n = 1.2\,kW$ to $P_n = 2.4\,kW$ with each power cycle lasting for $10\,s$ is applied as the input for the modular architecture. Fig. 4.25(a) shows the output currents of DAB,1 ($i_{o,1}$) and DAB,2 ($i_{o,2}$) along with voltage across the load resistor (v_o) for the applied mission profile. Fig. 4.25(b) shows the zoomed image of the DAB currents when delivering balanced power. When the power references are changed, $i_{o,1}$ and $i_{o,2}$ change accordingly while v_o maintains the reference voltage of $250\,V$.



(a) (b)

Figure 4.25: (a) The output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) for equal power sharing for the given mission profile (b) The output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) with time scale $5\,\mu s/div$ [J2].

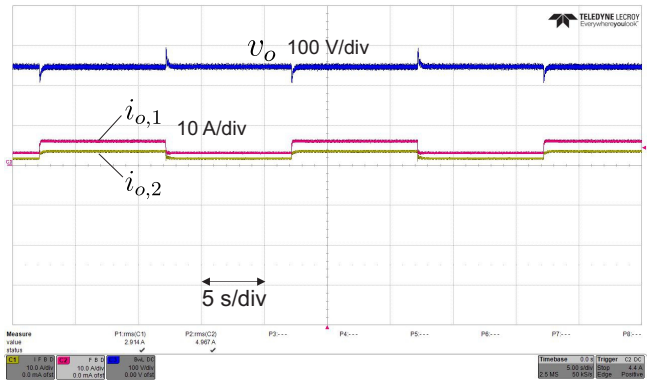
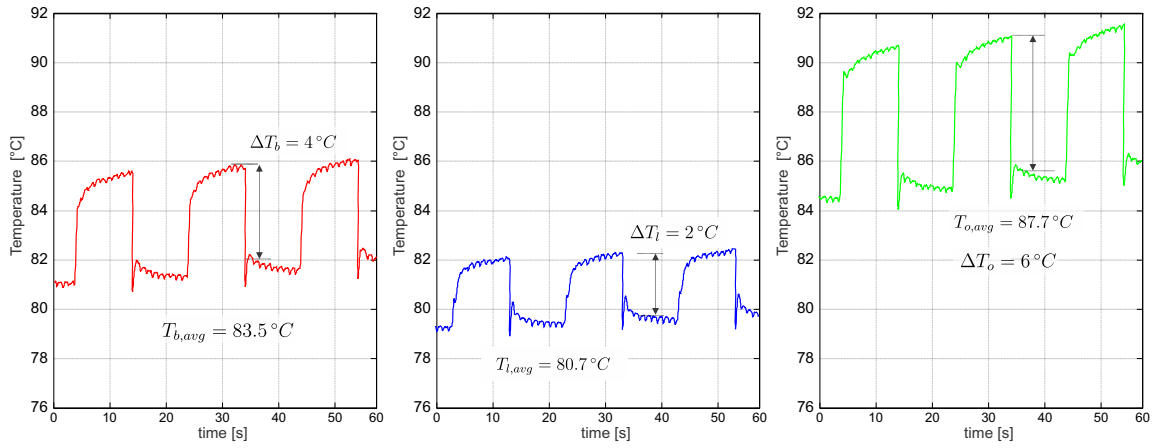


Figure 4.26: The output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) with activated power routing controller for the given mission profile [J2].



(a) (b) (c)

Figure 4.27: Variation of primary side IGBT junction temperatures over time of the DAB cells for (a) Balanced operation (b) Lightly loaded cell (c) Over loaded cell [J2].

Fig. 4.26 shows the output currents of DABs and the output voltage when the power routing strategy is activated. The DAB,1 process $\approx 70\%$ more power than the DAB,2 in this case. The DC-link voltages of the CHBs are controlled and kept equal to the reference value, even

Table 4.11: Normalized number of cycles to failure (N_f) for equal and unequal power sharing.

Case	N_f (norm.)
Balanced	1
Over-loaded cell	$\frac{1}{10}$
Lightly-loaded cell	38

with the unequal power-sharing. This validates the proper functioning of the control scheme developed in Section 4.4.2.

The temperature changes in the primary sides of the DABs in both cells are measured during the equal and unequal power-sharing. The results of the high speed infrared camera measurement for DAB cell 1 showing the temperature of the IGBTs are shown in Fig. 4.27 (a), (b) and (c). The results show a difference of $\Delta T_b = 4\,^{\circ}C$ in the junction temperature for the balanced power-sharing mode with average junction temperature $T_{b,avg} = 83.5\,^{\circ}C$ as in Fig. 4.27(a). When the power routing controller is activated, the average junction temperature of the DAB cell 2 has reduced to $T_{l,avg} = 80.7\,^{\circ}C$ and the temperature swing has also reduced to $\Delta T_l = 2\,^{\circ}C$ as illustrated in Fig. 4.27(b). Fig. 4.27(c) shows the temperature profile of the overloaded cell DAB,1, which has a higher average junction temperature of $T_{b,avg} = 87.7\,^{\circ}C$ and a temperature swing of $\Delta T_l = 6\,^{\circ}C$.

This results in the different remaining useful lifetimes of the cells and the Table 4.11 depicts the number of cycles to failure for the three cases using (2.6). The lifetime in Table 4.11 is normalized with respect to that of balanced power-sharing. By lowering thermal cycling in the lightly loaded cell, the RUL has increased by a factor of 38 times. In this case, the lifetime of the overloaded cell has been reduced by 10 times compared to that of balanced operation. The reduction in lifetime of the overloaded cell is less than that of the increase in lifetime for the lightly loaded cell. The IGBT is rated for $25A$ rms and is operated with a much lower current, and hence the lifetime reduction of the overloaded cell is lower. This shows that at lower power levels, a net increase in the system lifetime is achieved through power routing.

The objective of the experiment is to validate the design of power routing controller and its effect on the junction temperature, and consequently the aging. It is clear that the power routing controller can influence the junction temperature of the modules, and thereby the stress on the semiconductors in different cells of the modular converter.

Evaluation of the Impact on System Level Reliability

To evaluate the impact of power routing on wear-out based failures in the ST, a RUL estimation study without and with the power routing control has been carried out. The methodology shown in Fig. 2.9 is used for lifetime analysis. The multi-stage modular converter with 10 units consisting of 10 CHB cells connected to 10 DAB cells are fed with the mission profile given in Fig. 2.10 to evaluate the wear-out based failure. It is assumed that all the cells

Table 4.12: Estimated RUL in p.u. for multi-stage modular converter without and with power routing control (PRC).

Unit	CHB RUL (p.u.)		DAB RUL (p.u.)	
	Without PRC	With PRC	Without PRC	With PRC
1	1.00	1.19 (+0.19)	1.00	1.28 (+0.28)
2	1.06	1.22 (+0.16)	1.07	1.28 (+0.22)
3	1.14	1.23 (+0.10)	1.12	1.28 (+0.17)
4	1.21	1.28 (+0.07)	1.18	1.28 (+0.10)
5	1.28	1.30 (+0.01)	1.25	1.28 (+0.03)
6	1.36	1.35 (+0.01)	1.32	1.28 (-0.03)
7	1.44	1.38 (-0.06)	1.38	1.28 (-0.10)
8	1.54	1.44 (-0.10)	1.47	1.28 (-0.18)
9	1.64	1.51 (-0.14)	1.55	1.28 (-0.27)
10	1.74	1.57 (-0.17)	1.63	1.28 (-0.35)
	$Mean\,\Delta$RUL (p.u.) = +0.005		$Mean\,\Delta$RUL (p.u.) = -0.013	

have zero wear-out due to thermal cycling at the beginning of the operation. The electrical parameters affecting the losses of the converters and the heatsink temperatures are different for each cell according to the normal distribution. When the accumulated damage reaches unity according to (2.18), the cells are assumed to reach their end of life.

Without any thermal stress control, the individual CHB and DAB cells have different thermal cycling due to the differences in electrical and thermal parameters. Therefore, the wear-out of each cell is different and this leads to their failure at different times. The electro-thermal model of the modular converter generates the thermal cycling profile of the cells in accordance with the mission profile, and subsequently, the wear-out based remaining useful lifetimes are calculated. Table 4.12 summarizes the results of the thermal stress based lifetime evaluation. The RUL values are normalized for CHB and DABs by the failure of the first CHB and DAB cell respectively. The first CHB cell fails in 19^{th} year and the first DAB cell in 18^{th} year and these values are considered as the base value for per unit (p.u.) calculations.

Lifetime models such as (2.6) are obtained from the accelerated lifetime tests with a certain number of sample devices and the obtained experimental data is curve fitted to derive the relationship between lifetime and thermal stress [82, 11]. This implies that there is a degree of uncertainty in the derived parameters and hence the calculated lifetime is not a single deterministic value. The lifetime model fitting coefficients are considered as Gaussian distributions with $3\sigma = 0.05$, as discussed in Section 2.6. Then the estimated number of cycles to failure (2.6) follows the Weibull distribution and the failure probability of the cells can be represented as unreliability curve or cumulative distribution function given by (2.3) [108].

The unreliability curves for the DAB cells without and with thermal stress based power routing control are as shown in Fig. 4.28 (a) and (b) respectively. Here, the cells are replaced when they reach 10 % failure probability, also commonly known as the B_{10} lifetime [108].

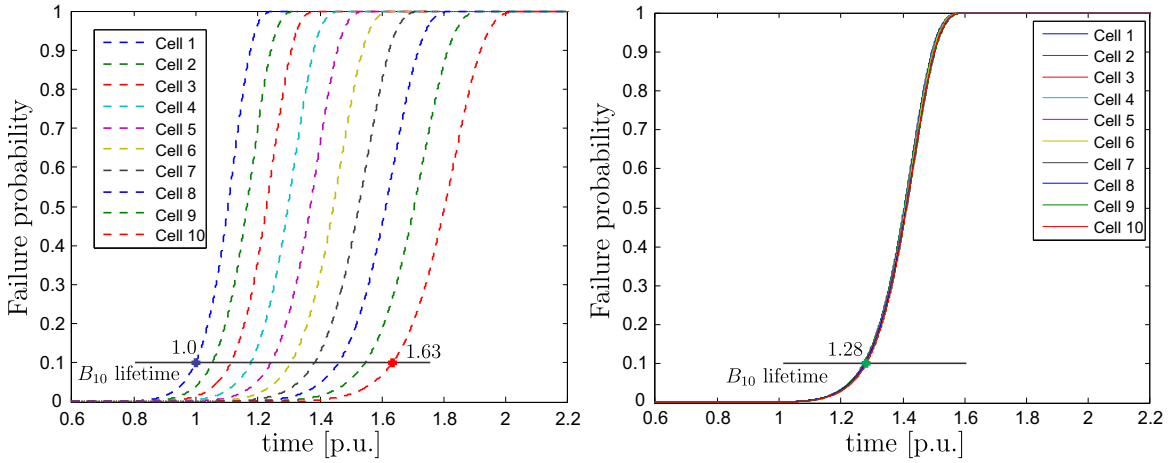


Figure 4.28: Unreliability of the DAB cells (a) without power routing (b) with power routing [J2].

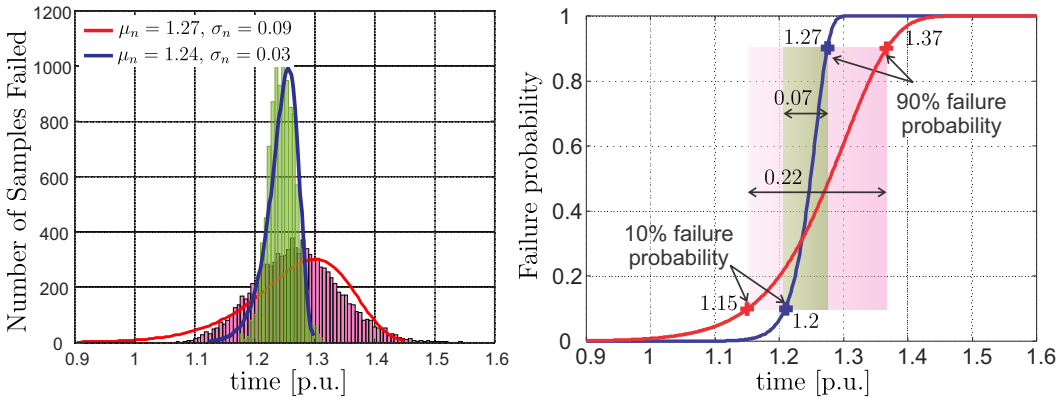


Figure 4.29: Monte-Carlo analysis without and with power routing control (a) Distribution of failures over time (b) Unreliability or cumulative probability distribution over time [J2].

Without power routing it is clear from Fig. 4.28 (a) that the DAB cells are replaced at different instants.

In order to control the thermal stress based aging, the power-sharing between the units of the multi-stage modular converter are dynamically changed according to the developed virtual resistor based power routing. The results of the case study are given in Table 4.12. Compared to the conventional equal power-sharing, the power routing method can effectively converge the RUL of the DAB cells, whereas it results in an improvement of the total RUL of the CHB cells. The power routing has a lower impact on changing the loss distribution among the CHB cells due to the series connection of the cells. Whereas, for the DAB cells, the unequal power-sharing can effectively vary the device losses, and hence the thermal cycling based wear-out is actively controlled. Failure of the first CHB cell is delayed by 19 % with power routing strategy and that of the DAB cell is delayed by 28 %.

When the thermal stress control is applied, the failure probability of the cells converges

and the B_{10} lifetime becomes 1.28 p.u. as shown in Fig. 4.28 (b). Thus, the number of maintenance can be reduced by manipulating the thermal stress among the cells. However, the mean RUL for DABs is decreased by 1.3 % with the power routing method. On the other hand, for the CHB cells, a slight increase in the mean RUL of 0.5 % is obtained by adopting the proposed control strategy.

For sensitivity analysis considering the thermal parameter variations, a Monte-Carlo simulation for 1000 cases with and without power routing is carried out using the system model. The schematic representation of the analysis is shown in Fig 2.18. Here, the thermal parameters such as heatsink temperature and device parameters with 5 % tolerance band are modeled as normal distributions with $3\sigma = 0.05$ to emulate a real operating environment. The mission profile input along with the parameters given as the inputs to the electro-thermal model generates the number of cycles to failure or RUL of the system for two cases; without thermal stress control and with power routing for thermal stress control. As illustrated in Fig 2.18, the Monte-Carlo simulation is performed for r cases and the RUL thus obtained follows a Weibull distribution. Subsequently, the pdf and cdf of the Weibull distribution of individual converter cells are calculated. Finally, a system level unreliability/cdf is obtained using the formula given in (2.20),

Fig. 4.29 (a) shows the failure distribution of the modular converter with 10 DAB cells over the years with Monte-Carlo analysis. During the normal operation without active thermal stress control, the earliest wear-out based failures start around 19 years (considered as 1 p.u.) and reach the maximum probability of failure around 1.27 p.u. years. The failure distribution approximated by a Weibull distribution has the mean and standard deviation as 1.27 p.u. and 0.09 p.u. respectively. From the Weibull distribution, the unreliability or the cumulative failure probability distribution can be obtained as shown in Fig 4.29 (b). The unreliability plot illustrates clearly the spread of failure distribution without any thermal stress control. Here, 80 % of failures are spread over 0.22 p.u. time, making the maintenance scheduling difficult.

To evaluate the impact of power routing, the Monte-Carlo analysis is repeated for the modular architecture model with the virtual resistance based power routing control. The thermal parameters of the system remain the same as that of the normal operation. The thermal stress control is able to achieve a 3 times reduction in the standard deviation of failures compared to that of normal operation. However, the mean lifetime of the system is slightly decreased by 2.4 % in comparison with normal operation. Fig. 4.29 (b) depicting the unreliability curve vividly demonstrates the advantage of the proposed strategy. In this case, 80 % of failures occur in a span of 0.07 p.u., resulting in better maintenance scheduling. Moreover, the B_{10} lifetime of the system is improved by 4.4 % or 11.4 months as shown in Fig. 4.29 (b).

4.5 Summary of the Chapter

This chapter has presented the algorithms for system level power routing control of modular power converters to equalize the aging of the converter cells. To analyse the reasons for

unequal aging of the converter cells in modular converter cells, the random failure and wear-out based failures of the power devices have been considered. The results show that the thermal and electrical parameter deviations of the power devices in the converters can result in a substantial difference in the aging of the modular converter cells. Moreover, the failure-replacement cycles due to random or wear-out failures result in converter cells with different ages in a modular system.

The power routing strategy proposed for equalizing the aging of the converter cells by unequal loading has been carefully studied. First, the limits of the power unbalance in a CHB modular converter topology with two commonly used modulation methods are experimentally evaluated. Thus power unbalance limits are established for CHB for developing power routing controller. As the next step, a system level control for power routing based on virtual resistance method has been proposed. The virtual resistance based power routing for the three stage ST architecture is evaluated with experimental and analytical studies.

In case of modular converter in IPOP configuration for the LV side of the ST, by routing the power, the time to the next maintenance can be maximized and the lifetime of the system can be increased by approximately $7.5-44\%$ under the investigated conditions. It is experimentally proven that the stress distribution between parallel cells can be controlled, and thereby the wear-out of the components. As a price to pay for this increased reliability, the efficiency is slightly reduced for unequally loaded converters. For the multi-stage ISOP modular converter with CHB and DAB converters for ST application, systematic development of a virtual resistance based system level control is presented, along with its validation in case of thermal and electrical parameter variations using Monte-Carlo analysis. Monte-Carlo analysis shows that the proposed strategy is able to reduce the standard deviation of the failure probability by 3 times compared to that of normal operation. Moreover, the proposed strategy improves the B_{10} lifetime of the system resulting from thermal stress based wear-out of the devices by $4.4\,\%$ or 11.4 months. Experimental results demonstrate the potential of the modular architecture control system to route the power internally to achieve thermal stress control.

5 Graph Theory Based Optimal Power Flow Solutions

The system level control of modular ST architectures becomes more challenging with the increasing number of converter cells and multiple conversion stages. The graph representation facilitates a simpler analysis of complex systems and lays down the foundation of the optimization strategies for power routing. Graph theory representation of the modular converters introduced in Chapter 3 lays the foundation. The graph theory based power routing algorithms proposed in this chapter are based on publications [J1, J5, J6, J7, C4, C5, C6].

The power routing control strategy with virtual resistors discussed in Chapter 4 has the demerit of decreasing the mean system lifetime even though the early wear-out failures are delayed. Virtual resistors offer a simple solution for power routing problem but does not provide an optimal solution considering the efficiency, reliability and maintenance scheduling. This serves as the motivation for adopting new approaches that can serve as a tool for system level control strategies. Considering the power flow analogous to the information flow in data networks, the modular converter architectures can be represented as a graph with nodes and edges exemplifying the flow of power as illustrated in Chapter 3. Then, graph theory algorithms are formulated to route the power in order to optimize the efficiency, reliability and maintenance schedule of the system.

First, an overview of the graph-theoretic optimization strategies is given. Subsequently, systematic development of a graph theory based system level optimization algorithms for modular power converters is discussed. Three main optimization algorithms are developed in this chapter. The first one presents an efficiency and reliability improvement method for the ST application [J5]. The second algorithm focuses on managing the maintenance schedules for the ST application [C4]. Finally, an optimization algorithm for improving reliability in a more electric aircraft application is discussed [J6]. The graph theory based power routing method has been compared with the state-of-the-art phase shedding or activation/deactivation method to highlight the benefits. Moreover, reliability analysis with Monte-Carlo simulation considering the thermal and electrical parameter deviations is presented to demonstrate the effectiveness of the proposed method in the case of converters operating under different conditions.

5.1 Review of Graph Theory Algorithms

Graph theoretical concepts are widely used in different fields to study and model various applications. The application of the graph theory algorithms span through various areas such as chemistry, physics, biology, computer science, communication, mathematics, operations research, electrical networks, etc. [143]. For instance, graph theory is used to study atoms, molecules, construction of bonds, and so on, in chemistry. The application of graph theory in biology includes the formulation of migration and movements of species in different regions. In case of mathematics and operations research, the traveling salesman problem, graph coloring, optimal scheduling of jobs, and locating the shortest path between two nodes

in a graph are a few examples of applications of graph theory. The use of graphs in game theory helps to solve problems in engineering, economics and other competitive platforms. A directed graph is used to represent a finite game with nodes representing the positions and edges denoting the moves of the players. The most commonly used graph theory algorithms are summarized as follows [175, 143]:

- The shortest path algorithm in a network
- Algorithms to find adjacency matrices
- Algorithms for scheduling
- Algorithms for graph coloring
- Algorithms for searching an element in a data structure
- Graph algorithms for computer network security
- Algorithms for finding maximum network flow

It is clear that the graph theory has diverse applications in different areas, and the above-mentioned graph theory algorithms are a research topic on their own. For example, to find the shortest path in a network, there are several algorithms available where Dijkstra's algorithm, Bellman Ford algorithm, Floyd Warshall algorithm and Johnson's algorithm are among the most popular ones. The shortest path algorithms have applications in navigation, transportation, highway planning, finance, electrical networks, etc.

Among the different areas of graph theory applications, the power flow problem can be considered as a network flow problem in graph theory. Flow network is a directed graph with nodes receiving or sending flows and edges having capacity constraints. The flow coming into a node must be equal to the flow going out of the node unless it is a source or sink node. A source node has only outflow and a sink node has only inflow. The graph theory representation of the modular converters in Chapter 3 depicts the system with source, sink and converter nodes and this is in agreement with the general structure of a flow network. The following section analyses the network flow problem algorithms to identify the suitable one for optimal power flow in modular converters.

5.1.1 Network Flow Problem in Graph Theory

Network flows are essential elements in computer science, operations research, electrical engineering, communication, etc. Most investigated network flow problems can be categorized as [140, 175]:

- Shortest path problem: Discuss the best way from one node to another node in the graph with the lowest cost.
- Maximum flow problem: Deals with achieving the maximum flow from one node to the other while respecting the flow capacities of the edges.

- Minimum cost flow problem: Category of network flow problems with a cost associated to the flow and the objective is to achieve the desired network flow with the lowest cost from source to destination.

Out of these three algorithms, the minimum cost flow algorithm seems to be the best candidate for the power flow problem in modular power converters [176, 177]. The fundamental concept behind the power routing is to unequally load the power flow in modular converter cells according to their age. In this case, the age of each converter cell will define the cost of the power flow through that cell and the output power requirement of the load/sink must be satisfied in such a way that the cost is minimum. It is to be noted that the cost function is not limited to the age of the converter cell, but can also be other factors such as the efficiency of the converter.

Let $G = (N(G), E(G))$ be a directed graph defined by a set N of n nodes and a set E of m directed edges. The supply or demand of each node $i \in N$ is represented using an integer s_i, where $s \in \mathbb{R}^n$. If s_i is positive, the node i is a supply node, and s_i is negative, node i is a demand node, and a zero value indicates a transshipment node. Let $c, b, l \in \mathbb{R}^{n \times n}$, where each edge $L_{i,j} \in E$ has a cost $c_{i,j}$ and a maximum flow capacity of $b_{i,j}$ and a minimum flow capacity of $l_{i,j}$ associated with it. The flow through the edge $L_{i,j}$ is represented by $x_{i,j}$, where $x \in R^{n \times n}$. A feasible minimum cost flow optimization problem is defined as

$$\min_{x} \quad \sum_{i,j \in E} c_{i,j} x_{i,j} \tag{5.1a}$$

$$\text{subject to} \quad \sum_{j:(i,j) \in E} x_{i,j} - \sum_{j:(j,i) \in E} x_{j,i} = s_i \quad \forall\ i \in N(G), \tag{5.1b}$$

$$l_{i,j} \leq x_{i,j} \leq b_{i,j} \tag{5.1c}$$

$$\sum_{i=1}^{n} s_i = 0. \tag{5.1d}$$

The constraint in (5.1b) represents the supply or demand of a node i, where the first term denotes the total outflow of the node and the second term represents the total inflow of a node. Constraint (5.1c) gives the lower and upper boundary conditions for the network flow through each node. Equation (5.1d) indicates that the total input flow should be equal to the output flow, which is a necessary condition for the feasibility of the problem.

In case of power flow problems, usually, a quadratic convex cost function is used instead of a linear function [138, 139]. The primary reason for using a quadratic cost in electrical network flow problems is that the power losses usually have a square relationship with the processed power, and the losses do not vary linearly with the processed power. Hence, quadratic program is chosen for implementing power routing algorithms.

5.2 Multi-Objective Algorithms for Optimal Power Routing

In this section, three different optimal power routing algorithms are formulated and evaluated based on convex flow optimization. The 3 application algorithms are as follows:

- An Efficiency and Reliability Improvement Algorithm for ST Application [J5]
- An Algorithm Focusing on Maintenance Scheduling of ST [C4]
- An Optimization Algorithm for Improving Reliability in More Electric Aircraft [J6]

The first two algorithms are focusing on ST application, where efficiency, reliability and maintenance are the main challenges of the power electronics transformer. The third algorithm is focusing on improving the reliability of a modular DC-DC converter in more electric aircraft where reliability is the main concern.

5.2.1 Efficiency and Reliability Improvement Algorithm for the ST Application

The main challenge of the power electronics based ST is to deliver high efficiency and reliability to compete against the conventional low frequency transformer. Modular ST with multiple energy conversion stages has several power flow paths providing the potential for higher efficiency and reliability. To increase the reliability of ST, the proposed power routing strategy is implemented with graph theory and the objective is to improve reliability without sacrificing efficiency. The topology under study is the CHB-DAB based ST shown in Fig. 3.10 (a). The CHB provides isolated MVDC-links which are connected to the DABs and the outputs of all the DABs are connected in parallel to form the low voltage DC.

The power routing is formulated as a network flow problem and the nominal power rating of the converter determines the capacity constraints of the power flow through a path. Weights are given to the power flow paths depending on the remaining useful lifetime and efficiency of each converter cell. The power flow optimization function routes the power according to the weights of each power path without deteriorating the efficiency in order to enhance the reliability. The formulation of the power flow optimization problem is discussed as follows.

Formulation of the Graph-theoretic Power Flow Problem

The graph theory representation of the modular power converters introduced in Chapter 3 define the nodes and edges to exemplify the internal power flow in the modular structure. The flowchart of the power routing algorithm with graph theory optimization is shown in Fig. 5.1. The algorithm performs the optimization function for each power routing control period. The power routing control period should not be confused with the control period of the individual converters and the power routing control period can be minutes, hours or days according to different applications.

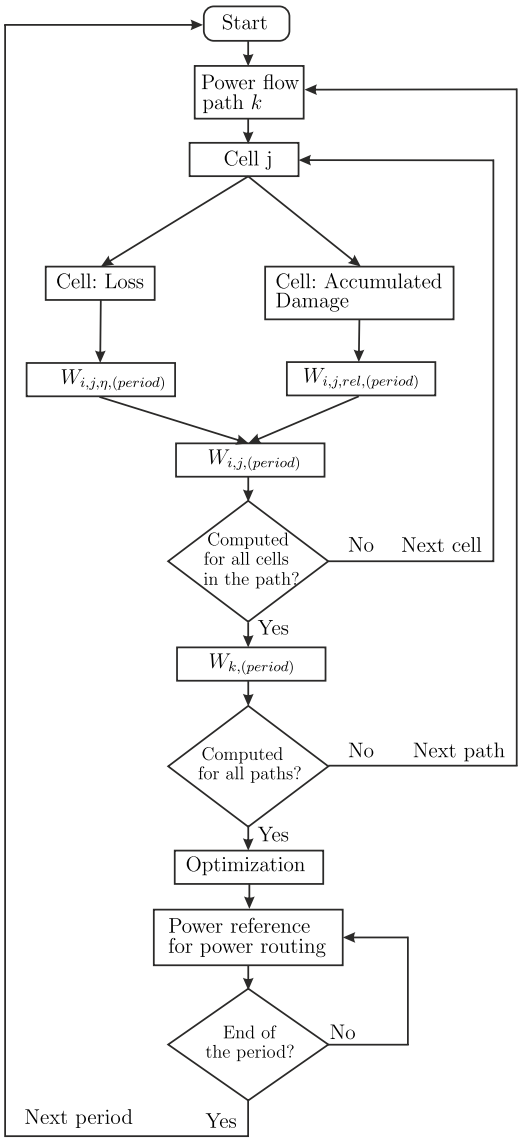


Figure 5.1: Flowchart of the power routing algorithm with graph theory optimization.

To develop an algorithm to optimally route the power among the power flow paths available, the weights of the edges and the capacity constraints have to be defined. The weights of the power flow paths define the cost of a path and in this case, the cost is defined by the efficiency and reliability of the path. Two important factors shall be considered for the power flow problem definition, and they are as follows.

- Definition of weights according to the optimization objectives
- Definition of constraints for optimization to respect the electrical network laws and converter limitations

The power flow in one phase of the CHB-DAB based ST is shown with a graph representation in Fig. 3.10 (b). Clearly, this can be visualized as a network flow problem with power flowing from the MVAC source to LVDC sink through the paths comprised of CHB and DAB cells. As indicated in Fig. 3.10 (b), each edge has a weight and the weight is defined as the cost of the power flow from the tail node to the head node. For instance, the weight $W_{S_a,C_{11}}$

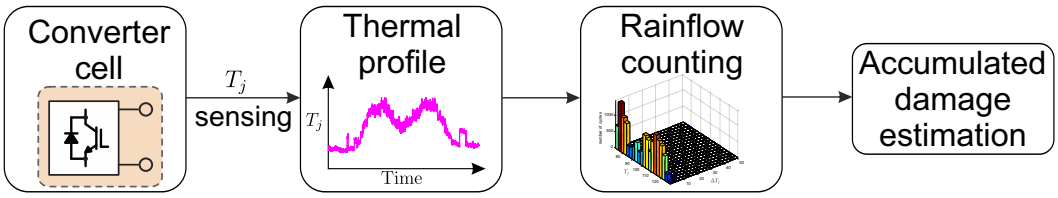


Figure 5.2: Accumulated damage estimation scheme for a converter cell.

represents the weight of the edge between nodes S_a and C_{11}.

Each weight is composed of two factors; efficiency and reliability weights. Depending on the converter losses, efficiency weights have been assigned. The objective is to minimize the use of paths with lower efficiencies when the power is routed internally within the converter. For a particular time interval *'period'*, the efficiency weight of the edges, $W_{i,j,\eta}$, is given by

$$W_{i,j,\eta,(period)} = k_{i,j}(1-\eta_j), \tag{5.2}$$

where η_j is the efficiency of the destination node and $k_{i,j}$is a tunable parameter. In this case, $k_{i,j}$ is considered as 1. The coefficient $k_{i,j}$ brings an additional degree of freedom to adjust the efficiency weight of a particular edge.

Under ideal conditions, individual cells of a modular converter have equal efficiency weights considering they have equal efficiencies. This implies that the power is distributed equally among the cells leading to maximum system efficiency. This can be ensured in the proposed method using a quadratic convex optimization, where equal weights result in equal power distribution among the power flow paths to minimize the cost.

For the formulation of reliability weights, accumulated damage D_i of each cell is used as a measure of reliability. For each power routing control period, the junction temperature data of the converter cell is fed into the rainflow algorithm and lifetime model to obtain the accumulated damage and is illustrated graphically in Fig. 5.2 (see Chapter 2 for details). The accumulated damage of a cell i for a period is defined as ΔD_i. The total accumulated damage D_i of the converter cell is given as

$$D_i = D_{ini,i} + \sum_{period=1}^{m} \Delta D_i, \tag{5.3}$$

where $D_{ini,i}$ is the initial damage. At the beginning of operation of the converter system, it is assumed that all the newly manufactured power devices have zero initial damage and hence $D_{ini,i}$ is taken as zero.

The expected remaining useful lifetime $LT_{exp,i}$ at every control interval can be calculated as

$$LT_{exp,i} = \frac{1-D_i}{\Delta D_i}. \tag{5.4}$$

The ΔD_i is the rate of change of damage for the past control interval. Since the ΔD_i is used for RUL calculation at every control interval, the variations in the mission profile are already taken into account.

The temperature swing variations in the converter cells will result in different expected RUL $LT_{exp,i}$ for each converter cell. In order to adjust the power flow through each cell to obtain an equal lifetime, a weight is assigned to each converter to determine the power flow. Depending on the expected lifetimes of each converter, the weights are assigned, which in turn determines the power flow through them from the source to the sink. The weight for each cell is formulated as

$$W_{i,j,rel,(period)} = W_{i,j,rel,(period-1)} + K_{D,i,j}\left(\frac{\sum_{i=1}^{N} LT_{exp,i}}{N} - LT_{exp,i}\right), \tag{5.5}$$

where $W_{i,j,rel,(period)}$ is defined as the weight assigned to the converter cell i for the current period and $W_{i,j,rel,(period-1)}$ denotes the weight of the cell in the previous period. $K_{D,i,j}$ is a proportional factor, which is defined as the function of individual accumulated damage of each cell D_i given by

$$K_{D,i,j} = f\left(\frac{D_i}{LT_{exp,sys}}\right). \tag{5.6}$$

Here, $LT_{exp,sys}$ is the expected lifetime of the system.

Finally, the efficiency and reliability weights are summed up for each edge by combining (5.2) and (5.5) as

$$W_{i,j,(period)} = W_{i,j,\eta,(period)} + W_{i,j,rel,(period)}. \tag{5.7}$$

Once the weight of an edge $W_{i,j}$ for a period is determined, the weights of the cells in a power flow path are summed up as indicated in the algorithm flowchart Fig. 5.1. For a path with r number of converter cells, the total weight is given by

$$W_{k,(period)} = \sum_{i=1}^{r} W_{i,j,(period)}, \tag{5.8}$$

where $W_{i,j,(period)}$ is the weight of the edges in path k for the current period.

The advantage of using graph modeling is the simplification of the complex architectures shown in Section 3.5.2. Since the power flow paths are already known from graph traversal, the cumulative weight of the converter cells in each path is calculated using (5.8). Thereby, the complex modular architectures with different power paths are simplified into parallel paths from source to sink.

For a CHB-DAB ST architecture depicted in Fig. 3.10 (a), the weights for the power flow paths are identified as:

$$\begin{Bmatrix} W_1 \\ W_2 \\ W_3 \\ \dots \end{Bmatrix} = \begin{Bmatrix} W_{S_a,C_{11}} + W_{C_{11},C_{12}} + W_{C_{12},C_{13}} \\ W_{S_a,C_{21}} + W_{C_{21},C_{22}} + W_{C_{22},C_{23}} \\ W_{S_a,C_{31}} + W_{C_{31},C_{32}} + W_{C_{32},C_{33}} \\ \dots \end{Bmatrix} \tag{5.9}$$

For each period, the weights for the power flow paths are calculated and is represented graph-

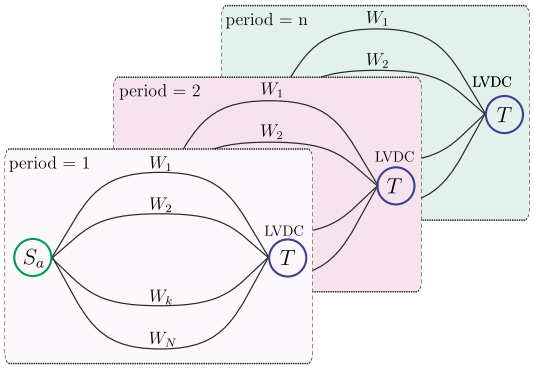


Figure 5.3: Flowchart showing definition of power flow optimization.

ically in Fig. 5.3. Thus, the weights change according to the accumulated damage progression of the converter and the efficiency variations.

Although this section focuses on the CHB-DAB based ST architecture, similar approach is applicable for the other ST architectures as well. For instance, the weights for the CHB-QAB based ST shown in Fig. 3.11 are formulated as:

$$\begin{Bmatrix} W_1 \\ W_2 \\ W_3 \\ \dots \end{Bmatrix} = \begin{Bmatrix} W_{S_a,C_{11}} + W_{C_{11},C_{14}} + W_{C_{14},C_{17}} \\ W_{S_a,C_{12}} + W_{C_{12},C_{15}} + W_{C_{15},C_{17}} \\ W_{S_a,C_{13}} + W_{C_{13},C_{16}} + W_{C_{16},C_{17}} \\ \dots \end{Bmatrix} \tag{5.10}$$

Here, the subscript of the weights is the same as that of the graph representation for preserving coherence. The power allocation depends on weights $W_1, W_2, \dots$ which in turn depends on the reliability and efficiency of CHB and QAB cells. Since the node C_{17} is considered for the three power flow paths, the reliability of QAB secondary has higher priority over the other cells. From Fig. 3.11 (b), it is evident that the failure of QAB secondary will result in the loss of 3 power flow paths leading to the unavailability of the whole unit. Similarly, all ST architectures including more complex interphase ST architecture shown in Fig. 3.12 can also be expressed as the sum of weights of the parallel power flow paths.

Even more complex interphase ST architecture shown in Fig. 3.12 can be expressed as the sum of weights of the parallel power flow paths from each phase to LVDC link given by

$$\begin{Bmatrix} W_1 \\ W_2 \\ W_3 \\ \dots \end{Bmatrix} = \begin{Bmatrix} W_{S_a,C_{11}} + W_{C_{11},C_{14}} + W_{C_{14},C_{17}} \\ W_{S_a,C_{12}} + W_{C_{12},C_{25}} + W_{C_{25},C_{27}} \\ W_{S_a,C_{13}} + W_{C_{13},C_{36}} + W_{C_{36},C_{37}} \\ \dots \end{Bmatrix}. \tag{5.11}$$

In short, all the ST architecture graphs can be simplified by following this approach and the formulated weights can be used for the optimized routing of power.

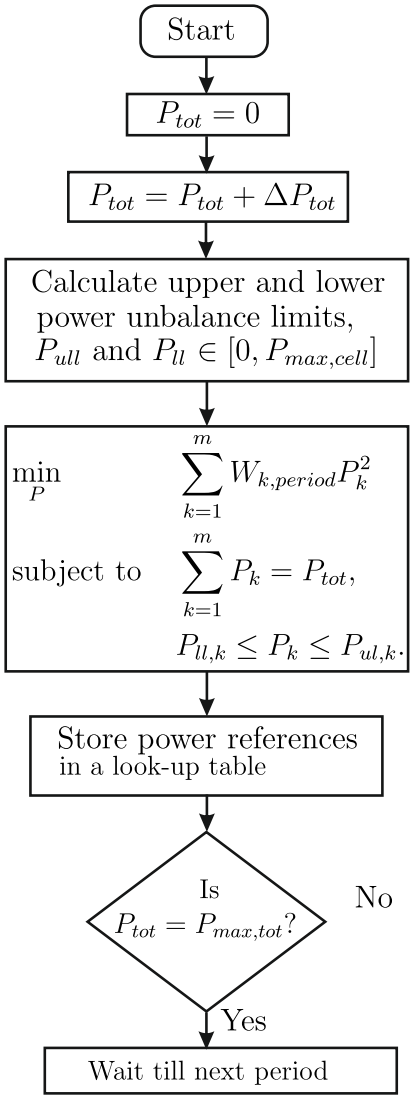


Figure 5.4: Flowchart showing power reference generation.

In order to respect the electrical power flow limitations, the constraints need to be considered while formulating the optimization. The maximum power that can be processed by each cell shall not be greater than the nominal power of the converter. Moreover, the sum of power processed by the modular cells has to be equal to the total input power. Additionally, the upper and lower power unbalance limits for the topology has to be respected. For example, the upper and lower power unbalance limits for the CHB due to sinusoidal modulation for a single cell is $0.39P_{tot}$ and $0.22P_{tot}$ respectively (see Section 4.3). This needs to be considered while performing the optimal power routing algorithm.

The optimization algorithm minimizes the total system cost by changing the power distribution through each path while respecting the constraints. Minimum cost convex flow problem in graph theory is considered here. When all the converters have equal thermal stress and efficiency, equal power-sharing among the cells provides the maximum system efficiency. The optimization is performed offline and the results of the optimization are stored in a 3D lookup table. Therefore, for each operating point of the modular system, power references for all the cells have to be determined. The optimization algorithm is shown as a flowchart

in Fig. 5.4. Here, the total power demand of the system is denoted as $P_{tot} \in [0\ P_{max,tot}]$, and P_{tot} cannot exceed the maximum power rating of the modular converter $P_{max,tot}$. Since the power references for each operating point need to be computed, the operating point is varied from 0 to $P_{max,tot}$ in steps of ΔP_{tot} as depicted in the flowchart. For each total power demand P_{tot} and let $P \in \mathbb{R}^m$, a convex quadratic optimization algorithm is performed as

$$\min_{P} \quad \sum_{k=1}^{m} W_{k,period} P_k^2 \tag{5.12a}$$

$$\text{subject to} \quad \sum_{k=1}^{m} P_k = P_{tot}, \tag{5.12b}$$

$$P_{ll,k} \leq P_k \leq P_{ul,k}, \tag{5.12c}$$

where P_k is the optimal power flowing through path k and m is the total number of paths from source to sink. It is to be noted that constraints play an important role in the power routing algorithm. The equality constraint (5.12b) ensures that the power routing affects only the internal power-sharing in the converter cells and the total power demand P_{tot} is satisfied. The inequality constraint (5.12c) defines the power routing constraints in the power flow paths. As discussed in Section 4.3, the maximum power unbalance limits are defined by topology, modulation technique, etc. and these upper and lower power unbalance limits (P_{ul} and P_{ll} respectively) should be respected while optimizing the power flow. The upper power unbalance limit should not exceed the rated power of the converter cells $P_{max,cell}$ in the path.

Once the power references of all the cells for every operating point are computed and stored in a 3D lookup table, the whole process is repeated in the next power routing control period. Even though the lookup table provides the power references in discrete steps, the interpolation technique is used to obtain the power references for all the operating points. The use of look-up tables can potentially reduce the computational burden compared to an online power routing optimization function.

Evaluation of Power Flow Optimization Method

In order to evaluate the effectiveness of the proposed algorithm, simulation studies are conducted with the electro-thermal model developed in Chapter 2. System architecture with 10 CHB cells connected to DAB cells shown in Fig. 3.10 (a) is considered here with each cell having different initial accumulated damage. The graph theory representation given in Fig. 3.10 (b) shows the possible power flow paths of this topology. It is to be noted that the proposed algorithm is applicable for any modular topology. In order to emulate the working of a modular converter to study the lifetime/reliability and efficiency, a mission profile is given as the input. Depending on the mission profile, the thermal loading of the converter is estimated from the electro-thermal model. From the junction temperature estimation, the remaining useful lifetime can be calculated using rainflow counting method and the lifetime

Table 5.1: Performance parameters (Loss and RUL) without and with power routing control (PRC).

DAB Cell	**Loss [p.u.] (without PRC)**	**±% Loss (with PRC)**	T_h	**RUL [p.u] (without PRC)**	**±% RUL (with PRC)**
1	1	+3%	$30\,^{\circ}C$	2.4	−20.5%
2	1.21	−2.5%	$26\,^{\circ}C$	1.5	+28.9%
3	1.05	0%	$32\,^{\circ}C$	1.8	+7.5%
4	1.11	+0.9%	$25\,^{\circ}C$	2.3	−14.3%
5	1.16	+0.9%	$22\,^{\circ}C$	2.3	−13.7%
6	1	+1%	$33\,^{\circ}C$	2.0	−5.0%
7	1	+4%	$28\,^{\circ}C$	2.7	−29.2%
8	1.05	0%	$31\,^{\circ}C$	1.9	+1.2%
9	1.32	−6.8%	$27\,^{\circ}C$	1	+94.4%
10	1.05	+1.9%	$29\,^{\circ}C$	2.2	−9.9%
$\sum \pm\%$ Loss with PRC		+2.4%	$\sum \pm\%$ RUL with PRC		39%

model of the power device. Chapter 2 describes the methodology of analysis in detail. Here, only the failures of DAB cells are shown since the effect of power routing algorithm on CHB is limited [178].

It is assumed that all the cells have initial accumulated damage as zero. The thermal parameters of the devices and the heat sink temperatures are also different for the 10 DAB cells according to normal distribution. For the case study, the heat sink temperatures are given in Table 5.1.

The junction temperature sensing from each converter cell is used to calculate the accumulated damage using (2.6), in which the device dependent parameters are curve fitted values. The lifetime model fitting coefficients a_1 and a_2 are considered as Gaussian distributions with $3\sigma = 0.05$. For sensitivity analysis considering these parameter variations, Monte-Carlo simulation for 10000 samples is done and the estimated lifetime of the samples are approximated by a Weibull distribution. Subsequently, the cumulative probability of the failure of the system is obtained.

Fig. 5.5 (a) shows the failure probability of the cells for the investigated system. Here, it is assumed that the cells are replaced when they reach 10 % probability of failure. RUL and losses given in the Table 5.1 are normalized with respect to the minimum RUL and minimum loss respectively. The time axis is shown in per unit with 1 p.u. being 30 years. The first cell fails at 0.35 p.u. years whereas the 10^{th} cell fails at 0.96 p.u. years. Thus, the failures within the system are spread over $0.61\,p.u.$ years depending on the thermal parameter variations.

For the implementation of power flow optimization, the reliability and efficiency weights of each converter cell need to be calculated. For the efficiency weight calculation, only the peak efficiency is considered for simplicity. The peak efficiency of the 10 DAB converter cells are calculated to obtain the efficiency weights using (5.2). Reliability weights in the beginning

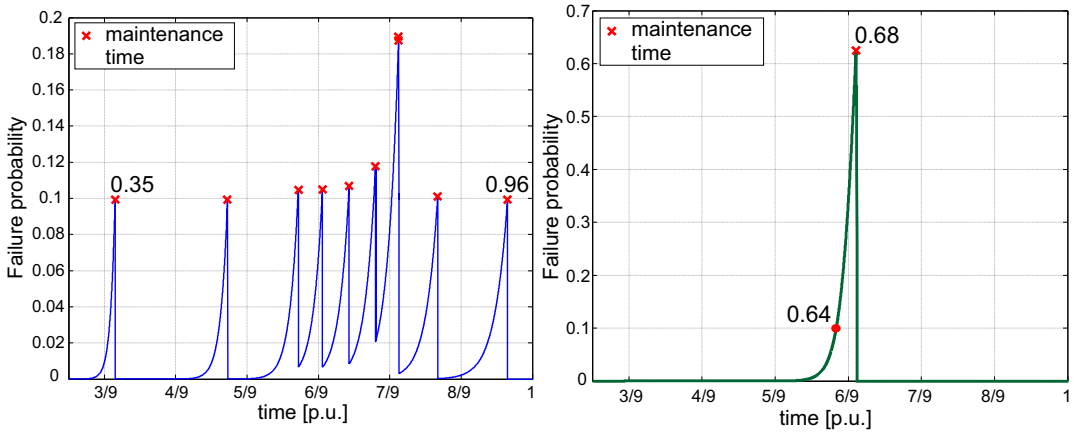


Figure 5.5: Failure probability of the DAB modular converter a) with equal power sharing (b) with proposed power routing [J5].

are assumed to be equal and are taken as 1 as expressed by

$$W_{i,j,rel,(period=0)} = 1. \tag{5.13}$$

The reason for initializing the weights as 1 instead of zero is to ensure that the weights are not negative at any point in time. For each period or the control interval for power routing optimization, the junction temperature profile of the individual converter cell is used to calculate the accumulated damage using (2.6) and (2.18). The junction temperature profiles of the cells are different due to the different losses and heatsink temperatures of the individual cells. Therefore, the different individual accumulated damages is used to calculate the reliability weight of the DAB cells using (5.5). The reliability weight generates an error proportional to the deviation from the average expected lifetime. Finally, the weights are combined using (5.8).

In the beginning, since the accumulated damage is very small, the efficiency weight dominates over the reliability weight. When the difference between the accumulated damage among the cells becomes significant, the reliability weight gains domination over the efficiency weight.

The power routing algorithm based on graph theory provides the power reference to each DAB converter to control the system wear-out and efficiency. The simulation result is shown in Fig. 5.5 (b) illustrating the probability of failure of the system. Here, the probability of failure of the individual cells also converges to a common point in time. The probability of failure of the overall system reaches 10 % in 232^{nd} month. Defining that each cell being replaced at 10 % probability of failure, the system should be replaced on 245^{th} month or 0.68 p.u. years. The failures of the cells are not intermittent unlike in the case without power routing algorithm, which makes the maintenance scheduling easier. The overall lifetime of the system ($\sum RUL$) is increased by 39 % with power routing algorithm.

Table 5.1 shows the distribution of average losses among the DAB cells without and with power routing algorithm. Without power routing, the losses are distributed among the cells

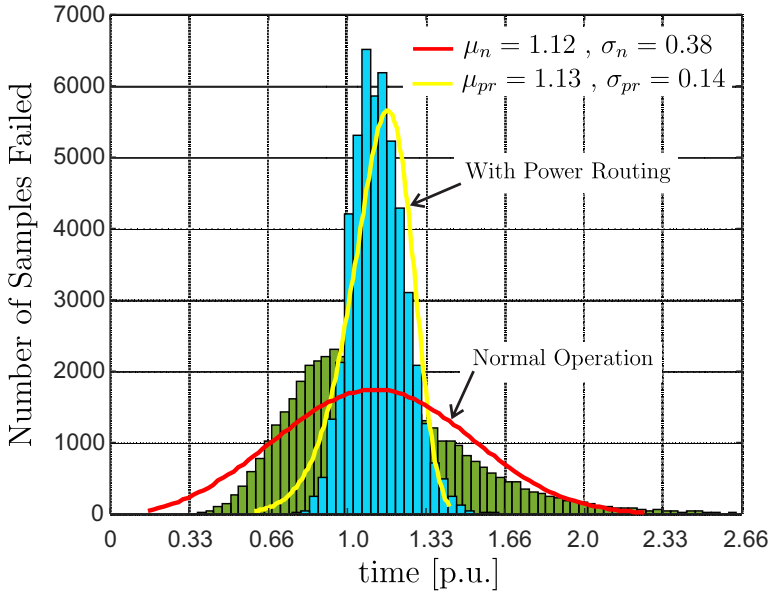


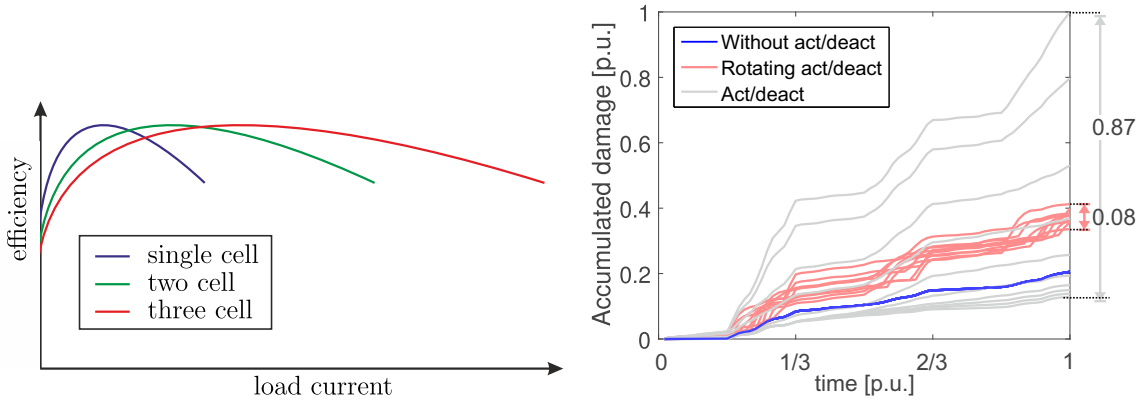
Figure 5.6: Monte-Carlo analysis without and with power routing control [J5].

according to their efficiency. With power routing, the total system losses are redistributed among the cells in such a way that the cells with lower efficiency process less power and thereby produce fewer losses. The efficiency of the system has decreased by 0.19 % because of the increase in losses. However, with this slight efficiency decrease, the overall lifetime of the system has increased considerably.

Analysis of Thermal Parameter Sensitivity on Power Routing Control

For sensitivity analysis considering the thermal parameter variations, a Monte-Carlo simulation for 10000 cases without and with power routing is carried out using the system model. The schematic representation of the analysis is shown in Fig 2.18. Here, the thermal parameters such as heatsink temperature and device parameters are considered as a normal distribution with a standard deviation of 10 % to emulate a real operating environment. Here, a 10 % standard deviation in the parameters is taken to consider the worst-case scenarios. The mission profile input along with the parameters given as the inputs to the electro-thermal model generates the number of cycles to failure or RUL of the system for two cases; without thermal stress control and with power routing for thermal stress control. As illustrated in Fig 2.18, the Monte-Carlo simulation is performed for n cases and the RUL thus obtained follows a Weibull distribution. Subsequently, the probability density function (PDF) and cumulative distribution function (CDF) of the Weibull distribution of individual converter cells are calculated. Finally, a system level unreliability/CDF is obtained using the formula given in (2.20).

Fig. 5.6 shows the failure distribution of the ST with 10 DAB cells over the years with Monte-Carlo analysis. The expected lifetime of the ST is 30 years and is considered as 1 p.u. During the normal operation without power routing control, the earliest wear-out based failures start around 10 years (0.33 p.u.) and reach the maximum probability of failure around 1.12 p.u. years. The failure distribution approximated by a Weibull distribution has the mean



(a) (b)

Figure 5.7: (a) Exemplary efficiency curves for activation/deactivation methods. (b) Accumulated damage progression for equal power sharing, activation/deactivation and rotating activation/deactivation control strategies [J5].

and standard deviation as 1.12 p.u. and 0.38 p.u. respectively. From the Weibull distribution, the unreliability or the cumulative failure probability distribution can be obtained using (2.3). From the unreliability curve, the B_{10} lifetime of the system is obtained as 0.62 p.u. years. The B_{10} lifetime is defined as the time at which 10 % of the samples under the test have failed.

To evaluate the impact of power routing, Monte-Carlo analysis is repeated for the ST model with the graph theory optimization based power routing control. The thermal parameters of the system remain the same as that of the normal operation. The result is shown in Fig. 5.6. Optimization control is able to achieve a 2.7 times reduction in the standard deviation of failures compared to that of normal operation. The mean lifetime of the system has slightly increased to 1.13 p.u. in comparison with the normal operation. From the unreliability curve in this case, the B_{10} lifetime of the system is calculated as 0.94 p.u. years. This indicates an increase of 66 % increase in the B_{10} lifetime of the system with the proposed method.

Comparison with State-of-the-Art Power flow Control Methods

The common practice in modular converter systems is to share the power equally among the cells. However, to improve the light load efficiency, activation and deactivation of the cells or also known as phase shedding is proposed in the literature [160, 161, 162, 163]. In the case of modular interleaved DC-DC converters, the modular cells are activated and deactivated according to the operating points. An exemplary efficiency vs. load current for operating with a single cell, two cells and three cells is shown in Fig. 5.7 (a). It is evident that the system efficiency at light load operating points is better when all the cells are not activated. In [163], a lookup table based phase shedding scheme is presented whereas [162] focuses on a current sensorless phase shedding control. Depending on the load profile, some cells are over-utilized in activation/deactivation method. To compensate for the over utilization of cells due to the activation/deactivation method and to equalize the thermal stress among the cells, a rotating activation/deactivation strategy is discussed in [179]. The stress on the semiconductor depends on the loading condition of the converter cell which in turn is

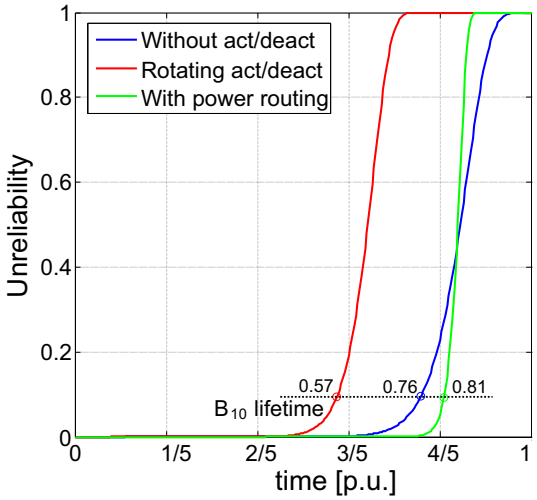


Figure 5.8: System unreliability for equal power sharing, rotating activation/deactivation and power routing [J5].

determined by the mission profile. Therefore, the rotation of the turned on/off cells does not guarantee equal stress on the semiconductors, and thereby equal aging.

To analyze the impact of equal power-sharing and activation/deactivation method on the thermal stress of modular system, 10 DAB converter cells connected in IPOP configuration as shown in Fig. 3.2 are considered. Here, all the electrical and thermal parameters of the converters are assumed to be equal. The normalized accumulated damage is calculated for a mission profile for a period of 30 days for the system with, a) equal power-sharing, b) activation/deactivation, and c) rotating activation/deactivation control strategies and is shown in Fig. 5.7. The results show that the activation and deactivation methods have an adverse effect on the reliability leading to a very high difference in accumulated damages among the cells. Conventional activation and deactivation lead to over utilization of some cells resulting in their relatively early failure. The rotating activation/deactivation method manages to utilize the converter cells equally but results in increased damage compared to the equal power sharing. The frequent turn-on and turn-off according to the load conditions result in large thermal cycles and thereby reducing the lifetime of the respective cells. The activation/deactivation method yields lower losses at low loads compared to equal power-sharing as expected. It is to be noted that the lower loss benefit due to the activation/deactivation method is significant only when the converter operates at light load for most of the time.

In case of an ideal system with no parameter deviations, the power routing strategy produces the same result as that of the equal power-sharing method. To emulate a real scenario, Monte-Carlo analysis is performed for a) rotating activation/deactivation, b) equal power-sharing and c) power routing method. Here, the heatsink temperature, collector-emitter voltage and turn on/off energies with 2.5 % tolerance are modeled as Gaussian distribution having 99.7 % confidence. The estimated Weibull cumulative probability density/ unreliability of the system of 10 DAB cells for the 3 methods are illustrated in Fig. 5.8. The 10 % failure probabilities of the system (B_{10} lifetime) for the 3 cases are indicated in the figure. Here the time axis is given in per unit with $1\,p.u.$ being 25 years. The rotating activation and deacti-

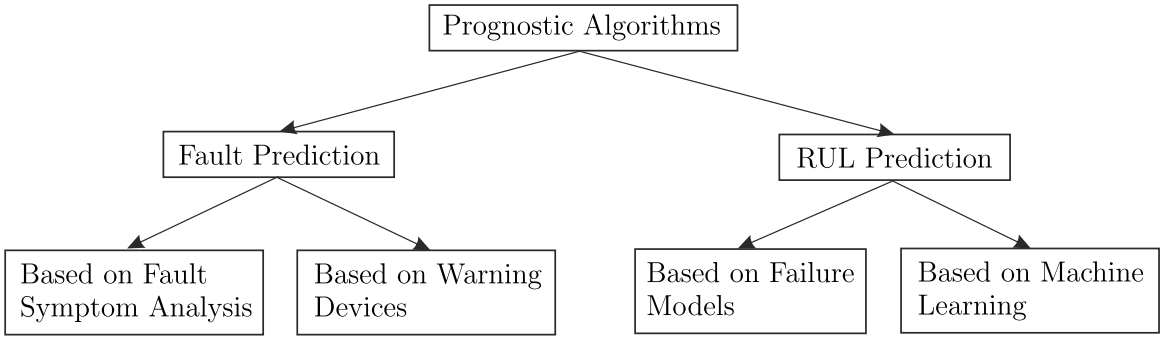


Figure 5.9: General classification of prognostic algorithms.

vation method has the lowest B_{10} lifetime of 0.57 p.u. followed by equal power-sharing with 0.76 p.u. The power routing strategy enables a 24 % increase in the B_{10} lifetime compared to that of the rotating activation/deactivation method. It is worth noting that the unreliability with power routing reaches unity before the equal power-sharing method indicating that the spread of the probability of failure is reduced with the power routing algorithm. This helps in scheduling the maintenance in longer time periods.

5.2.2 Graph Theory based Algorithm Focusing on Maintenance Scheduling of ST

In this section, a novel strategy for optimizing the maintenance scheduling with power routing has been proposed. First, a brief overview about the existing literature on maintenance scheduling is given. Subsequently, the proposed algorithm is introduced and the impact of the method has been validated using electro-thermal simulation.

Review of Prognostic Maintenance Scheduling

Maintaining power electronics systems in systems such as large fleets of aircraft and remotely located STs can be very challenging. The maintenance activities require trained personnel with expertise and according to the level of fault, the system downtime can vary. Unscheduled maintenance can result in revenue loss and unavailability of the systems and these facts become crucial with increasing operational demands and lack of fiscal resources. Therefore, prognostic maintenance becomes an essential requirement of systems that require high reliability and availability. The definition of prognostics is the ability to provide early detection of the incipient faults of a component and to predict the progression of such a fault resulting in the component failure. With prognostics, the useful life remaining in the system can be predicted with an acceptable degree of confidence and when such information is used to schedule maintenance, it is termed as prognostic maintenance. It is different from the static methods such as mean time to failure based on statistical data since the RUL prediction is based on the monitored conditions and is dynamic in both accuracy and uncertainty.

A general classification of the prognostic algorithms for maintenance is illustrated in Fig. 5.9 [57]. The prognostic algorithms can predict the remaining useful lifetime or the impending faults in the system using the data from the condition monitoring sensors. In case of fault

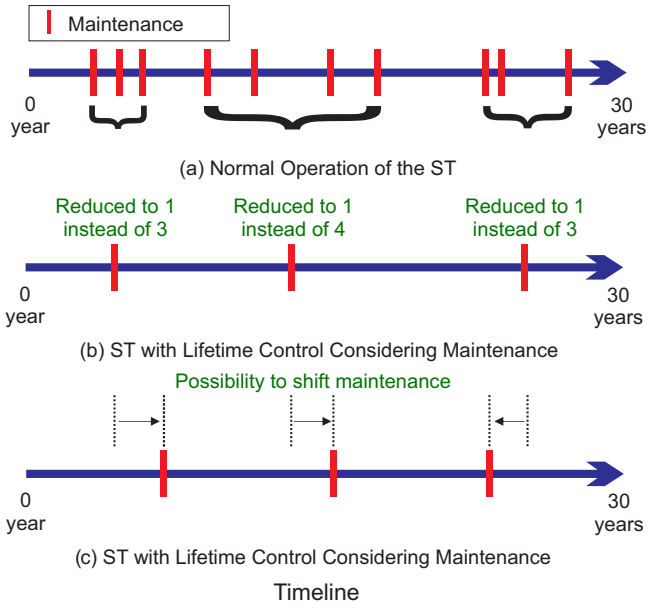


Figure 5.10: Impact of the proposed algorithm on the maintenance scheduling of modular ST (a) Without proposed algorithm (b) With proposed algorithm (c) Demonstrating the flexibility of shifting maintenance [C4].

prediction algorithms, the techniques are based on warning sensors incorporated in the design stage of the circuits. They provide failure prediction at the component level rather than the system level. Data-driven or component models can be used to predict the faults at the component level using the information from dedicated incipient fault sensing devices. For predicting the RUL, either model based approaches using the established failure models or data-driven methods using machine learning techniques are used. A physics of failure based health management strategy for a high power Light Emitting Diode (LED) is proposed in [180]. In case of power electronics systems, the device models for the most critical components such as capacitors and semiconductor switches can be used to estimate the RUL of the system.

The most popular data-driven methods used for prognostic algorithms are Neural Networks, Support Vector Regression, Genetic Algorithms, Multiple Linear Regression, Expert System etc. In [26], a genetic algorithm based system maintenance scheduling using the prognostic information has been proposed incorporating various constraints such as availability of parts, personnel and maintenance conflicts. Another data-driven method using the degradation data for an LED application has been proposed in [181] for predicting the RUL. In general, prognostic maintenance predicts the RUL of the system using techniques such as model-based, data-driven or hybrid approaches.

Algorithm for Adaptive Lifetime Control

Several papers discuss about optimizing the maintenance schedules based on the monitored data considering operational constraints [58]. However, literature discussing actively influencing the RUL and thereby optimizing the maintenance scheduling is scarce. In this section,

a novel maintenance optimization strategy using graph-theoretic optimization is proposed. The maintenance scheduling has been proposed for the ST, but is applicable to any modular power converter system. The concept of maintenance optimization with power routing is graphically illustrated in Fig. 5.10. Here, it is shown that without any lifetime control, the individual units fail at different points in time resulting in a higher number of maintenance schedules as depicted in Fig. 5.10(a). With active control of the RUL considering the maintenance schedules, the number of maintenance can be reduced as illustrated in Fig. 5.10(b). The proposed method also has the flexibility to shift the maintenance as shown in Fig. 5.10(c), which would be helpful to optimize the maintenance costs considering constraints such as availability of parts, personnel, etc.

The ST is composed of many converter cells which have embedded junction temperature sensing of the power devices through the measurement of collector-emitter voltage [182]. By knowing the junction temperature profile of the devices, the accumulated damage, D, can be calculated using the method described in Chapter 2.

The idea is to control the lifetime of the power semiconductor devices by actively controlling the power flow through them. The proposed algorithm uses optimization to define the power flow through each of the cells depending on the aging of the cell. The algorithm is similar to the efficiency and reliability improvement algorithm in Section 5.2.1. In this method, the mission profile for the past week is used to calculate the incremental accumulated damage, ΔD, for each cell. Subsequently, the total accumulated damage can be calculated for each converter for each week using (5.3)

The expected remaining useful lifetime for cell i ($LT_{exp,i}$) at every control interval can be calculated using (5.4). The required number of maintenance is defined by the maintenance interval factor λ_m. For example, considering an ST with a required lifetime of 30 years and 3 maintenance schedules, the maintenance intervals can be defined as

$$\lambda_{m1} = [0,10]\,\text{years},\ \lambda_{m2} = [10,20]\,\text{years},\ \lambda_{m3} = [20,30]\,\text{years}.$$

Cells with $LT_{exp,i}$ in the corresponding maintenance interval λ_{m1-3} are grouped together and the objective of the algorithm is to converge the failures of these cells in the specified maintenance intervals. Consequently, a weight is assigned to each converter in a group to determine the power flow and thereby control the lifetime. The weight for each edge connection of the converter cell nodes i and j in the group is formulated as

$$W_{i,j,maint,(period)} = W_{i,j,maint,(period-1)} + K_{D,i,j}\left(\frac{\sum_{i=1}^{t} LT_{exp,i}}{k} - LT_{exp,i}\right), \tag{5.14}$$

where $K_{D,i,j}$ is a proportional constant which is a function of individual accumulated damages of each cell, D_i, and t is the number of cells in a group belonging to the corresponding maintenance interval λ_m. The computation of the weight $W_{i,j,maint,(period)}$ is similar to (5.5), but since the importance is for optimizing the frequency of maintenance, the cells with RUL belonging to the maintenance intervals are grouped together to determine the weights.

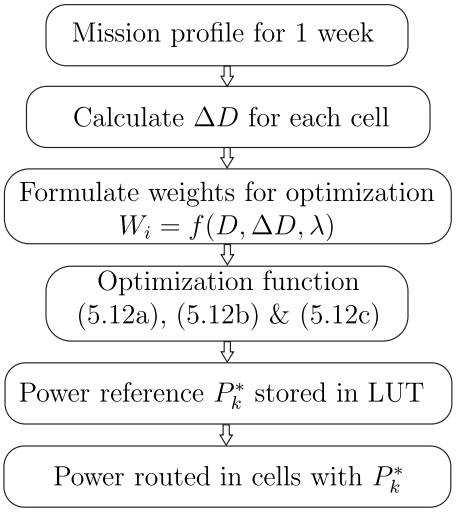
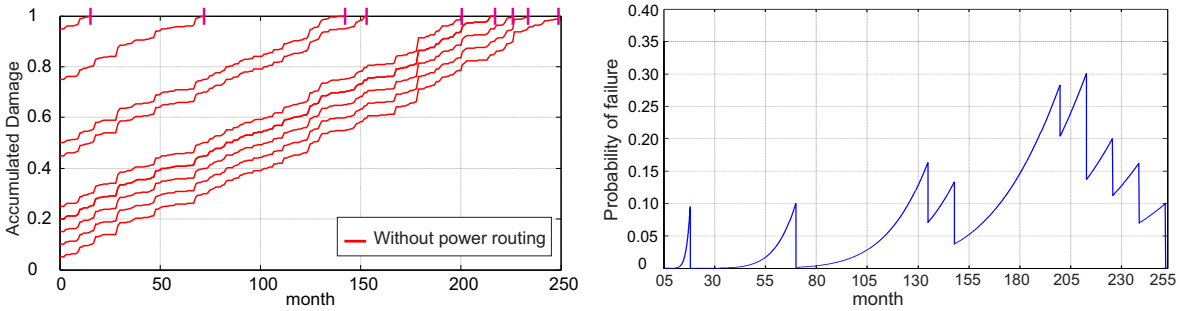


Figure 5.11: Graphical representation of lifetime control algorithm [C4].



(a) (b)

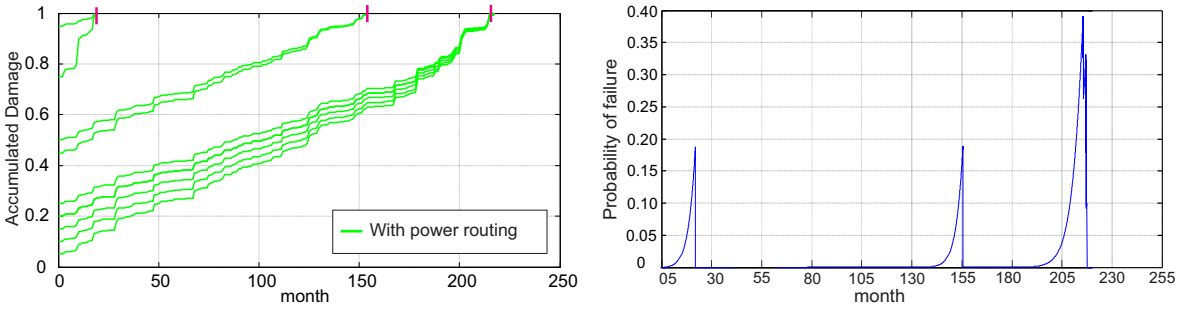
Figure 5.12: Normal operation of the ST (a) Progression of accumulated damage vs. time (b) Probability of failure of any cell [C4].

Subsequently, the weights are summed up for r converter cells in each path k as given by

$$W_{k,(period)} = \sum_{i=1}^{r} W_{i,j,maint,(period)}. \tag{5.15}$$

Finally, the weights are given to an optimization algorithm using a convex optimization function as given in (5.12a) subjected to the constraints (5.12b) and (5.12c). The flowchart of the algorithm for maintenance scheduling is summarized in Fig. 5.11.

The constraints are imposed on the converters in such a way that the power routing is active in partial load operation, whereas all processes equal power when the system is at full load. Most of the time, the system is not operating at full load, which enables to route the power unequally. This means the converters need not be oversized for this strategy. Here, the optimization is performed offline and the results of the optimization are stored in a 3D lookup table. Therefore, for each operating point of the modular system, power references for all the cells have to be determined. The optimization algorithm is summarized in flowchart in Fig. 5.4. The methodology of optimization is similar to Section 5.2.1 with the difference in weight formulation.



(a) (b)

Figure 5.13: Power routing control of the ST (a) Progression of accumulated damage vs. time (b) Probability of failure of any cell [C4].

Evaluation of Proposed Maintenance Scheduling Algorithm

In order to evaluate the effectiveness of the proposed algorithm, simulation studies are conducted with the electro-thermal model developed in Chapter 2. A system with 10 DAB cells connected to CHB cells is considered here as shown in Fig. 3.10 (a) with each cell having different initial accumulated damage. The electro-thermal model of the ST is fed with different mission profiles reflecting the grid conditions [89].

The progression of accumulated damage over time for the normal operation of the ST is shown in Fig. 5.12 (a). Here, only the failure of DAB cells are shown since the effect of power routing algorithm on CHB is limited [178]. Without any lifetime control, the cells fail at different instants in time, leading to many maintenance schedules. Fig. 5.12 (a) shows the progression of accumulated damage for the 10 DAB cells over time. Here, the cells have different initial damages and this results in their failure at different instants in time. Fig. 5.12 (b) shows the probability of failure of the system with the assumption that the cells are replaced at 10 % probability of failure. The probability of failure of the ST shows that there is a high chance of failure in the system spread over years, which can significantly affect the availability of the ST.

With the proposed algorithm, the accumulated damage, D_i, of each cell converges in such a way that the number of maintenance schedules is reduced while the decrease in the lifetime of the healthy cells is minimal. In this case, three maintenance events are selected with the maintenance intervals given by

$$\lambda_{m1} = [0,96],\ \lambda_{m2} = [96,192],\ \lambda_{m3} = [192,288] \text{ months}.$$

The cells in a particular maintenance interval are grouped together and the weights of the optimization (5.12a) are formulated to converge the failures of these cells. The effectiveness of the method is illustrated in Fig. 5.13 (a) and Fig. 5.13 (b). Fig. 5.13 (a) shows the progression of accumulated damages of the cells with lifetime control. The accumulated damages of the selected cells in the three maintenance intervals effectively converge to 3 maintenance schedules. The probability of failure of the system for the proposed algorithm is depicted in Fig. 5.13 (b). Compared to the failure probability without lifetime control, the proposed algorithm demonstrates a concentrated probability of failure around 3 maintenance

Table 5.2: Failure rate requirement for onboard hardware.

Design Assurance Level	Failure Rate	Remarks
Level A (Catastrophic)	< 1 FIT	Loss of aircraft
Level B (Hazardous)	< 100 FIT	Fatal injuries
Level C (Major)	< 10000 FIT	Discomfort/Injuries
Level D (Minor)	No criteria	May cause inconvenience
Level E (No effect)	No criteria	Safety not compromised

instants. Therefore, the risk of failure of the ST is reduced compared to the operation with balanced power.

5.2.3 Optimization Algorithm for Improved Reliability in More Electric Aircraft

In this section, an advanced power routing algorithm with an optimization function is proposed so that the cells are loaded in an optimal way to increase the overall system reliability of a more electric aircraft. The lifetime control is implemented for the DC/DC converters interfacing the HVDC and LVDC bus for the architecture shown in Fig. 5.14. First, an overview about the reliability requirement for MEA is given and the proposed modular topology is introduced. Subsequently, the algorithm for high reliability is proposed and the validation of the impact of the algorithm on system lifetime and reliability is presented.

Overview about MEA reliability

The concept of More Electric-Aircraft (MEA) is receiving more focus than ever with the advances in power electronics to decrease the weight and increase the overall efficiency [183, 184, 185]. MEA focuses on replacing the conventional non-propulsive functions onboard powered by mechanical, pneumatic and hydraulic systems with electrical system [186].

Regarding the electronic hardware reliability on the aircraft, DO-254 provides the necessary guidance [187]. Accordingly, there are 5 levels of compliance depending on the effect of failure of a hardware on the operation of the aircraft. The levels and failure rates are summarized in Table 5.2. The required failure rate of critical loads is 10^{-9} per hour (1 FIT) for a commercial aircraft.

The FITs are obtained from failure test statistics. 1 FIT corresponds to 114000 years of operation of a component without failure, which does not provide any comprehensive information about the required lifetime of the component. FIT reliability metric is obtained from reliability tests performed on a large number of components and hence, can't be directly interpreted as the lifetime of a single component. Moreover, the standards are based on constant failure rate (λ), which is only applicable in the 'useful life' region of the bathtub curve [28]. In order to better estimate the lifetime of a component, 'B_x lifetime' is used. It is defined as the time at which x percentage of components are failed and is calculated from the unreliability ($F(t)$) curve given by (2.3)

Apart from the hardware, software failures also contribute to equipment failures. DO-178C standard handles the safety of critical software used in aircraft systems [187]. Depending on the effect of the failure condition, there are also 5 levels of compliance ranging from the highest catastrophic level to no-effect level. The software for airborne systems should comply with this standard to obtain the certification from aviation authority. Other requirements for safe operation include the compliance of all onboard devices to DO-160 standard, which provides guidelines for environmental conditions and test procedures. The power converters should adhere to various norms regarding temperature variation, explosion proofness, voltage spikes, electro-static discharge, flammability, etc.

The Boeing 787 adopts a new design method called life-cycle cost design philosophy which comprises two additional design parameters namely maintenance cost and airplane availability. With this new design philosophy, Boeing claims a lowering of airframe maintenance cost by 30 %. Moreover, the elimination of mechanical based integrated drive generator unit by electrical system enables a 300 % increase in the reliability [188]. The evaluation of reliability for an electrical system for MEA using different reliability assessment techniques is provided in [189]. The standards also delineate the various methods for assessing the reliability such as Fault Tress Analysis and Markov Analysis. With more complex power electronics systems onboard, the reliability assessment becomes extremely complex. However, these standards still consider the constant failure rate for power electronic component reliability assessment. It is well-known that the constant failure rate is inadequate to evaluate the reliability of power electronic converters and the Physics of Failure approach has gained popularity over the past decades, which relies on the cause of failures instead of pure statistics [92]. With the increasing number of power electronic converters, the reliability assessment of MEA is expected to follow this trend.

Power Flow in the Onboard Electrical System

The penetration of electrical systems onboard opens up new challenges for the power distribution. The Power Distribution System (PDS) of the Airbus A380 uses an ac bus architecture with variable frequency, whereas the Boeing 787 introduces a $270\,V$ DC distribution system. One of the main goals of these PDS architectures is to reduce the weight and size, either by utilizing variable frequency or DC power. However, in order to comply with airworthiness standards, the PDS should allocate enough redundancy to operate even in case of multiple failures [190]. Nevertheless, having a duplicate for each system adds up to the weight and thereby reduces the efficiency of the airplane. In this scenario, modular power converters, which have the potential for high efficiency and power density while catering the redundancy requirements, are a promising solution [191]. With the trend of increasing distribution voltage levels, studies are focusing on the use of modular power converters [192].

The MEA concept introduces the possibility of different grid configurations comprising AC and DC systems. The ac distribution of no-bleed aircraft typically consists of $115\,V$, $400\,Hz$ three-phase, and $230\,V$ variable frequency system. Low voltage DC distribution (LVDC) is standardized at $28\,V$. A High voltage DC (HVDC) bus of $270\,V$ is used in Boeing 787 and

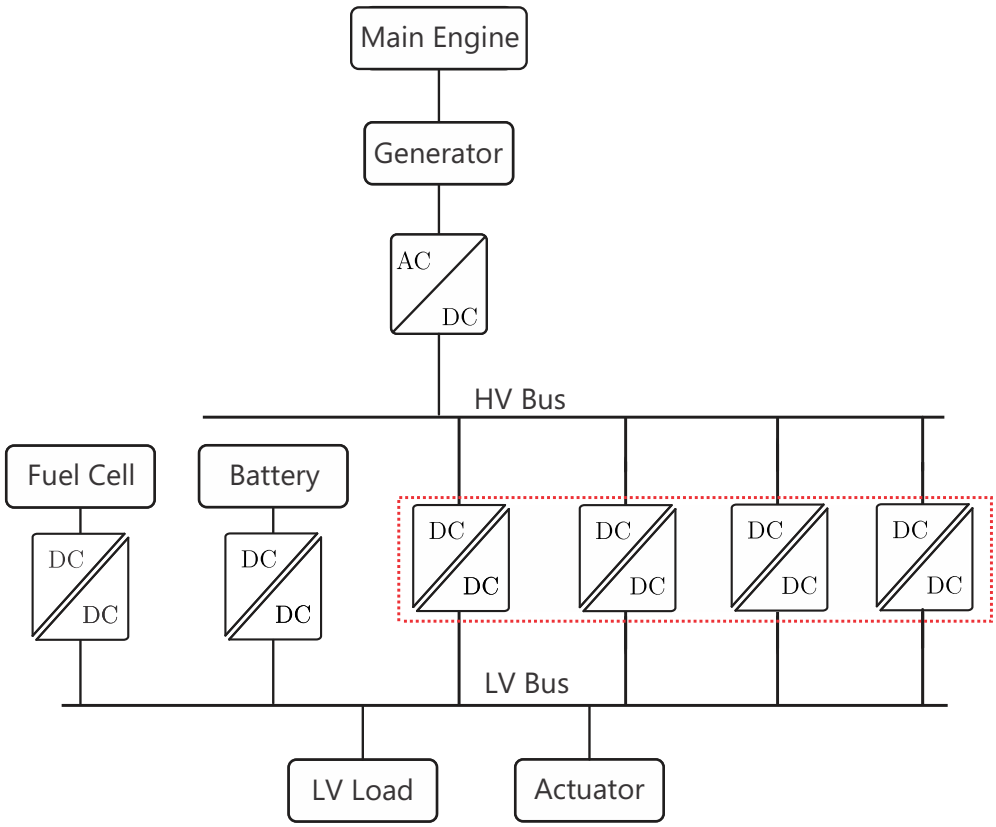


Figure 5.14: Proposed DC-grid architecture for MEA [J6].

Joint Strike Fighter. One of the promising solutions to improve efficiency is to make the distribution system DC since it offers less conversion stages to the load. Fig. 5.14 shows the proposed architecture of the DC distribution grid with modular DC-DC converters based on the literature [192, 193]. Here, the HVDC bus is powered by the converter connected to the generator and the LVDC bus supplies all the low voltage DC loads. A modular architecture with four DC-DC converters is considered here for enhanced reliability. Even if one of the converters fails, the system can still operate in derated mode till it is replaced. Any DC-DC converter with galvanic isolation can be used depending on the requirements. In this study, a Dual Active Bridge (DAB) topology is investigated owing to its compatibility with the MEA requirements.

For conducting the lifetime study of a power converter, it is essential to understand the behavior of the loads catered by this converter. The DC/DC converters feeding the LVDC bus feed all the LV loads supplied with 28V DC. Main loads include the actuators for the flaps, galley appliances, lighting loads, communication loads and In-Flight Entertainment/Seat Power Supply System (IFE/SPSS). Out of these loads, some loads, for example, lighting, can be classified as continuous loads. Loads such as (IFE/SPSS) have probabilistic nature and the actuators also operate only for a short time [194]. Therefore, it is realistic to assume the LVDC load as a combination of constant and variable loads. Fig. 5.15 (b) shows the modeling of mission profile with a normal distribution. Here, mean, μ = Constant Loads (CL) and standard deviation is given by σ = Variable Loads (VL). It is assumed that the constant loads can also vary up to a certain range depending on the number of passengers. This is

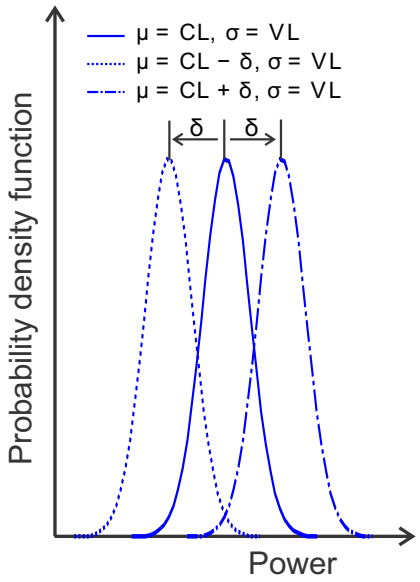


Figure 5.15: Mission profile representation by probability density [J6].

taken into account by the deviation δ around the mean value, for example, δ is assumed to have a variation of $10-20\,\%$ from the mean value.

Evaluation of the Proposed Optimization Algorithm

In this section, the detailed formulation of the lifetime control algorithm using an optimized power routing strategy is presented. The algorithm is shown graphically in Fig. 5.11. All the converters are equipped with junction temperature sensing systems based on V_{ce} measurement [182]. The converters used for high reliability applications are expected to be equipped with V_{ce} sensing for condition monitoring. The mission profile of the converter system for a time period generates the junction temperature profile for each converter. Here, a certain time period is considered (e.g. one hour) and it is termed as the lifetime-control-period. This junction temperature profile of the past control period can be used to calculate the consumed lifetime ΔD_i of each converter using rainflow counting and the lifetime model (see Chapter 2 for details). Subsequently, the total accumulated damage can be calculated for each converter over m hour using (5.3)

At the beginning of operation of the converter system, it is assumed that all the newly manufactured power devices have zero initial damage and hence $D_{ini,i}$ is taken as zero. The expected Remaining Useful Lifetime (RUL) ($LT_{exp,i}$) at every control interval can be calculated using (5.4). Since the ΔD_i is used for RUL calculation at every control interval, the variations in the mission profile are already taken into account.

The temperature swing variations in the converter cells will result in different expected RUL $LT_{exp,i}$ for each converter cell. In order to adjust the power flow through each cell to obtain an equal lifetime, a weight is assigned to each converter to determine the power flow. The weight for each cell is formulated using (5.5) and (5.6)

In the beginning, $W_{i,j,(period-1)}$ is initialized as 1 for every cell. This results in equal power-

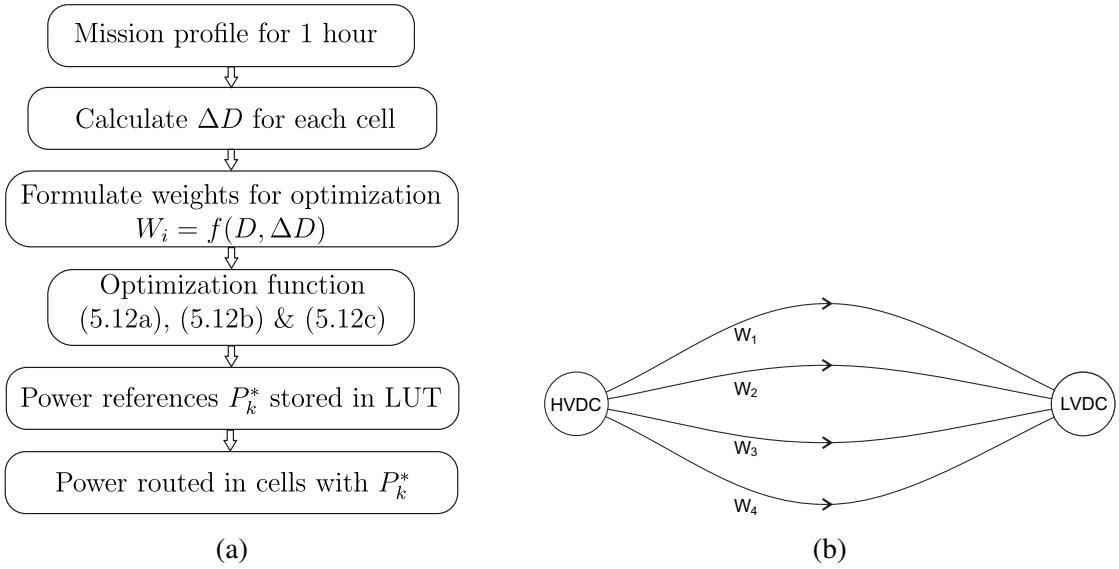


Figure 5.16: (a) Lifetime control with power routing using optimization (b) Graphical representation of the power flow in the investigated DC architecture [J6].

sharing among the cells. Since the deviation of the expected RUL of the individual cells from the average RUL of the system is less than that of $LT_{exp,sys}$ and the maximum value of D_i is 1, the weights $W_{i,period}$ remain positive. Finally, these weights are given to an optimization function, which minimizes the power flow through each cell depending on the respective weights. The optimization algorithm uses a convex quadratic optimization function as expressed in (5.12a) for a period, subjected to the constraints (5.12b) and (5.12c).

In an ideal case where all the converters have identical thermal parameters, the weights for each path become equal. For the topology in Fig. 5.14, weights become

$$W_1 = W_2 = W_3 = W_4 = W. \tag{5.16}$$

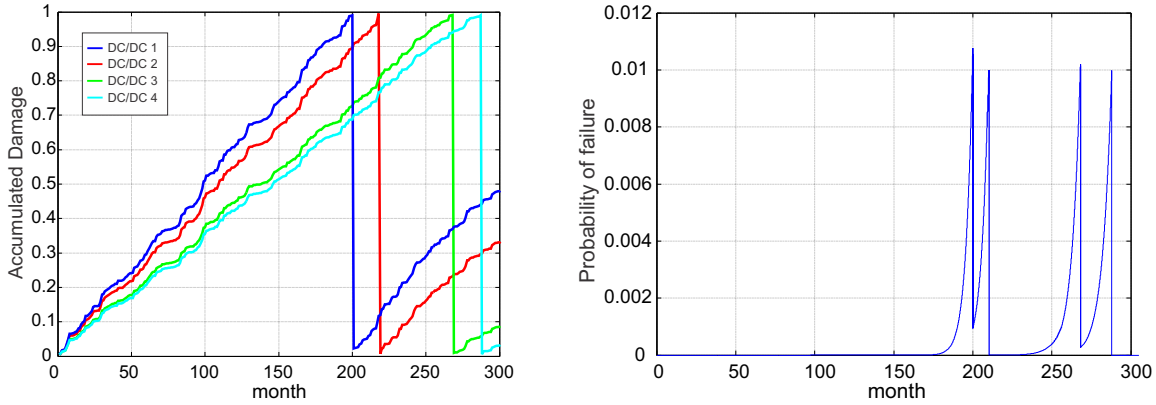
The resulting minimization according to (5.12a) yields equal power-sharing among the four converter cells. The deviation from the ideal equal power-sharing condition depends on the extent of aging of individual converter cells. The weight assigned to each converter determines the power flow through them from the HVDC to LVDC bus.

Since the accumulated damage of each cell does not change in the lifetime control period (1 hour), the weight computed for each cell is fixed. Therefore, the power references calculated for each converter cell can be stored in a look-up for the entire power range as illustrated in Fig. 5.16 (a). Since the references get updated only every hour, very fast computation of the optimization algorithm is not required.

To further analyze the impact of the algorithm on the lifetime of the modular system, a simulation study is carried out using the electro-thermal model of the 4 DAB converter cells connected in parallel. It is assumed that all the cells have initial accumulated damage as zero. The mission profile for the study changes every hour according to the use of the airplane. To model the varying power processed by the converters, a profile with a certain probability

Table 5.3: Simulation parameters.

Symbol	Description	Value
V_{HVDC}	DC-link voltage reference	$270\,V$
V_{LVDC}	DC-link voltage (LV side)	$28\,V$
f_{sw}	Switching frequency of the DAB	$12\,kHz$
P_n	Nominal power of the system	$10\,kW$



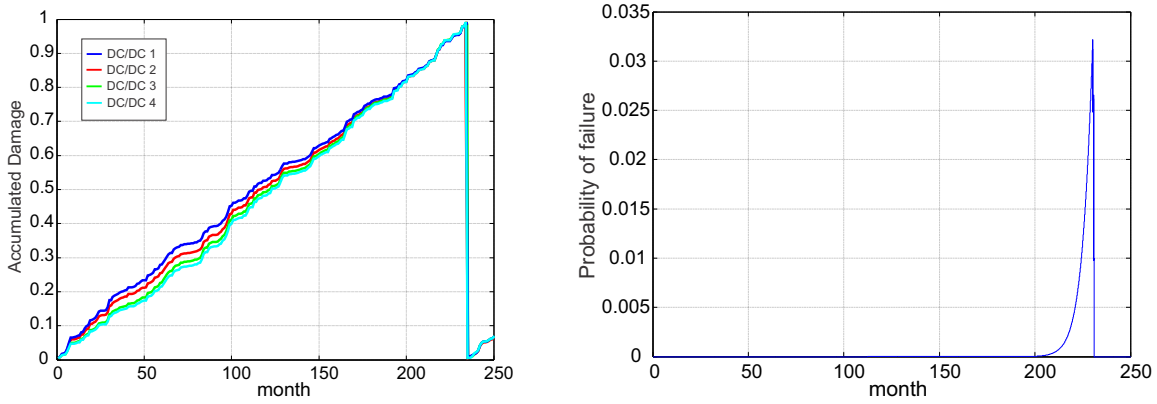
(a) (b)

Figure 5.17: (a) Accumulated damage progression over time for normal operation (b) Probability of system failure for normal operation [J6].

distribution function as described in Section 5.2.3 is considered. The system parameters for simulation are summarized in Table 5.3.

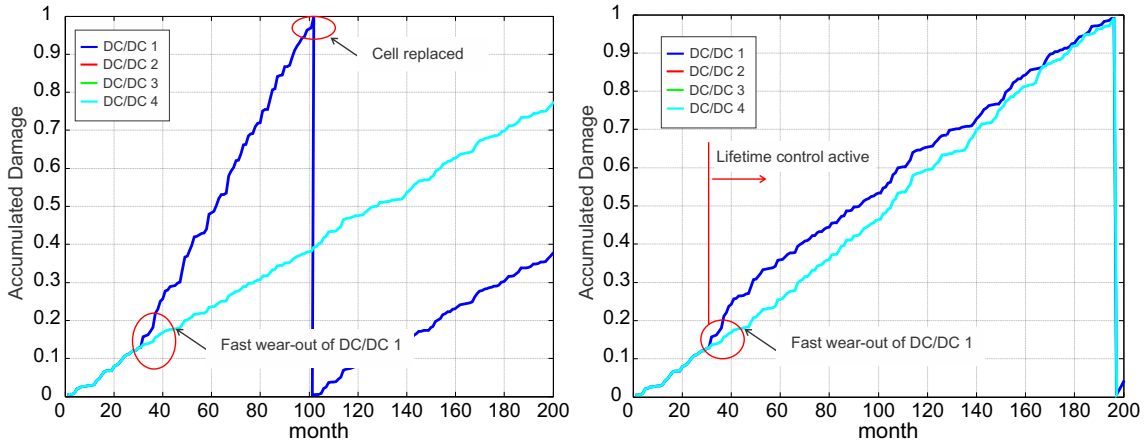
The progression of the accumulated damages of the 4 cells without any control algorithm is shown in Fig. 5.17(a). Here, even though the power shared by each converter is equal, the accumulated damages are different for each of them and subsequently, the lifetimes. The variation in the mission profile results in a variable rate of change of the accumulated damage. When the D_i of the converter cell reaches unity, the cell fails and it is replaced. In Fig. 5.17(a), the first cell fails at the 200^{th} month and after replacement, the D_1 starts at 0 for the new cell. Table 5.4 summarizes the RUL and the heatsink temperatures for the simulation case study. Fig. 5.17 (b) shows the probability distribution of failure of the cells for the investigated system. Here, it is assumed that the cells are replaced when they reach $1\,\%$ probability of failure.

In the following, the same system is used with the control algorithm developed in Section 5.2.3, which provides the individual power reference to each DAB converter to control the system lifetime. The simulated values of accumulated damage over the lifetime are shown in Fig. 5.18(a), illustrating the convergence of accumulated damages to a common point in time. This proves the effectiveness of the control algorithm, which actively controls the power flow to delay the system failure. The probability of a failure of the system is plotted in Fig. 5.18(b). Here, the probability of failure of the individual cells also converges to a common point in time. The prognostic maintenance can be scheduled based on a threshold failure probability depending on the criticality of the device [195, 196].



(a) (b)

Figure 5.18: (a) Accumulated damage progression over time for system with lifetime control (b) Probability of system failure with lifetime control [J6].



(a) (b)

Figure 5.19: Accumulated damage progression over time for system (a) Without lifetime control (b) With lifetime control [J6].

Table 5.4: RUL without and with lifetime control.

Cell	Heatsink Temperature	RUL (p.u.)	
		Normal operation	With lifetime control
DC/DC 1	25 °C	0.84	1.00
DC/DC 2	26 °C	0.92	1.00
DC/DC 3	30 °C	1.13	1.00
DC/DC 4	32 °C	1.21	1.00
Mean RUL		1.02	1.00

Table 5.4 summarizes the lifetime of DC/DC converter cells without and with the lifetime control. All cells fail approximately around 237^{th} month (1 % failure probability) with the lifetime control. The relative lifetime is the normalized lifetime of each converter cell with respect to the lifetime achieved with the lifetime control algorithm. For example, there is an increase in lifetime of the first DC/DC converter by $0.15\,p.u$ with the proposed control

algorithm compared to the normal operation. It is clear that the lifetime of converters 1 and 2 increases whereas the lifetimes of converters 3 and 4 have reduced. However, the average lifetime of the converter system is only reduced by 2 % and the time between failures of the cells is maximized.

In another case study to demonstrate the impact of accelerated aging without and with reliability optimization control, all the thermal parameters are considered to be similar at the beginning of the operation. Therefore, the devices age equally. However, during the operation over time, an increase in the device on-resistance or lack of cooling of the heatsink of a cell would result in rapid aging of the cell. Fig. 5.19 (a) shows the accumulated damage progression of the system when the converter cell DC/DC 1 wears out faster than the others. Here, it is assumed that the cell receives insufficient cooling resulting in a higher heatsink temperature compared to the others. Without any active lifetime control, the cell fails in 100^{th} month resulting in a lower overall system reliability.

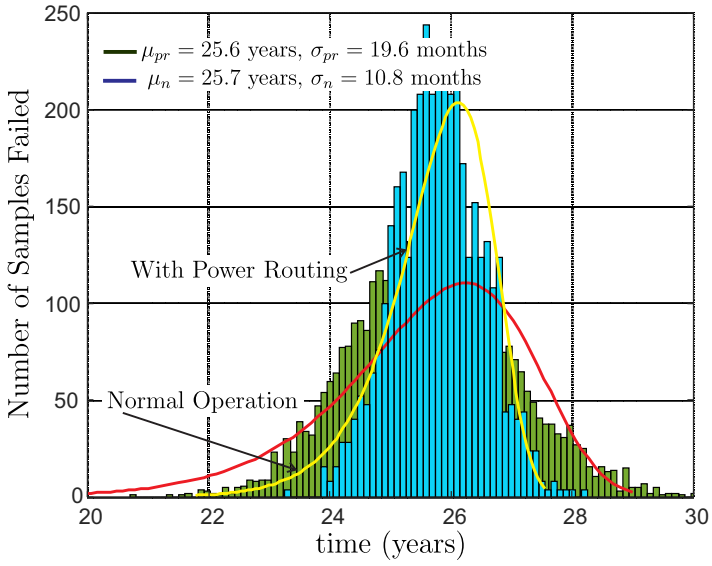
With the power routing control algorithm being active, the over-stressed cell DC/DC 1 process less power compared to the others. This results in an increased overall system lifetime with an increase of 100 % of cell 1's lifetime as shown in Fig. 5.19 (b). The most significant aspect of the active lifetime control algorithm is to delay the failures during the flight. For example, a failure in the cooling system during the flight can result in an abnormal rise in the junction temperature and thereby, speeding up the aging process. This is detected by the lifetime control algorithm and to ensure a safe operation of the system by delaying the failure, the power is routed from over-stressed cells to the fresh cells.

Validation of the Impact of Parameter Sensitivity On Lifetime Control

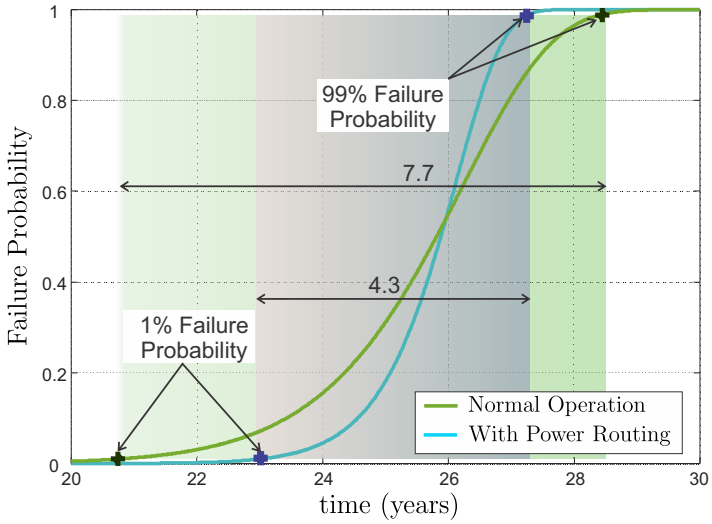
In order to validate the sensitivity of the controller to the thermal parameter variations, a Monte-Carlo simulation is carried out for 10000 test cases without and with lifetime control. The schematic explaining the Monte-Carlo analysis is shown in Fig. 2.18.

As explained in Fig. 2.18, the mission profile serves as the input to calculate the converter loading with the help of electro-thermal model of the system. To validate the effectiveness of the controller, the converter loading without and with the lifetime control is subjected to Monte-Carlo analysis. Without lifetime control, the four cells share the power equally, whereas the lifetime control routes the power according to the lifetime control algorithm and this is shown in Fig. 2.18. In the previous case studies, specific heatsink temperatures were selected to demonstrate the capability of the algorithm to control the lifetime. But in a real scenario, the heatsink temperatures for each of the cells can have many possible values. To validate the effectiveness of the lifetime control under different possible heatsink temperatures, a Monte-Carlo simulation with the heatsink temperature of 5 % tolerance band is modeled as a Gaussian distribution having 99.7 % confidence.

The lifetime estimated for n cases follows a Weibull distribution, and therefore the reliability metrics such as the PDF and CDF/Unreliability of the individual cells are extracted first. Finally, a system level unreliability/CDF is obtained using the formula given in (2.20). Here,



(a)



(b)

Figure 5.20: Monte-Carlo analysis without and with lifetime control (a) Distribution of failures over time (b) Unreliability or Cumulative probability distribution over time [J6].

Table 5.5: System lifetime without and with power routing control.

Operation Mode	$B_{0.1}$ **lifetime**	B_1 **lifetime**
Without lifetime control	18.43 years	20.75 years
With lifetime control	21.5 years	22.95 years
Lifetime improvement	+3.07 years	+2.2 years

both B_1 and $B_{0.1}$ lifetimes are shown. B_1 and $B_{0.1}$ lifetimes mean that 1 % and 0.1 % of the samples have failed in time respectively.

Fig. 5.20 (a) shows the failure distribution of the ST with 4 DAB cells over the years with Monte-Carlo analysis. During the normal operation without active lifetime control, the earliest failures start around 22 years, reaching the maximum failure probability around 25.6

years. The failure distribution can be approximated by a Weibull distribution [108]. The mean and standard deviation of the Weibull distribution are calculated as 25.6 years and 19.6 months respectively. From the Weibull distribution, the unreliability or the cumulative failure probability distribution can be obtained as shown in Fig 5.20 (b). The unreliability plot illustrates clearly the spread of the failure distribution without any lifetime control. With the normal operation, the system reaches $B_{0.1}$ and B_1 lifetime around 18.43 years and 20.75 years respectively. Here, 98 % of failures are spread over 7.7 years, making the maintenance scheduling difficult.

To evaluate the impact of power routing, Monte-Carlo analysis is repeated for the ST model with the power routing control. The thermal parameters of the system remain the same as that of the normal operation. The lifetime control is able to achieve a 44 % reduction in the standard deviation of failures compared to that of normal operation. Moreover, the mean lifetime of the system is slightly increased in comparison with normal operation. Fig. 5.20 (b), depicting the unreliability curve vividly demonstrates the advantage of the proposed strategy. The system attains $B_{0.1}$ and B_1 lifetime around 20.75 years and 22.95 years respectively. The results are summarized in Table 5.5.

5.3 Summary of the Chapter

This chapter has proposed graph theory based optimization algorithms in modular power converters for reliability, efficiency and maintenance scheduling optimization. Three approaches based on a minimum convex cost power flow optimization technique are considered.

In the first approach, a minimum convex cost flow algorithm is applied on the modeled graph to control the efficiency and reliability of the ST architectures with multiple stages and topologies. By actively controlling the power flow among the cells, the failures of the individual cells are controlled as demonstrated by the case study. The proposed algorithm is able to achieve a 39 % increase in the total system lifetime, decreasing the spread of the failures substantially by a factor of 18, and thereby potentially leading to better maintenance scheduling. Moreover, the losses are redistributed among the cells according to their efficiency and thereby increasing the overall system losses only by 2.4 % and decreasing the system efficiency by less than 0.2 %. Monte-Carlo analysis shows that the proposed strategy is able to increase the B_{10} lifetime of the system by 66 % compared to that of normal operation. The proposed methodology has the potential to be applied to any complex power electronic architecture for reliability and efficiency improvement.

The second approach focuses on the optimization algorithm for maintenance scheduling considering the ST application. Simulation results demonstrate the effectiveness of the proposed algorithm to synchronize the failures of the cells with maintenance of the ST and thereby decreasing the maintenance schedules from 10 to 3 times. Moreover, the proposed method reduces the probability of failure of the ST over time by concentrating the failures around the maintenance period.

The third approach is to use the optimization algorithm to achieve very high reliability for a modular DC-DC in MEA power distribution system. To delay the early wear-out failures, a lifetime control algorithm with an optimized power routing strategy relying on the power semiconductor's junction temperatures is proposed for a modular system. Monte-Carlo simulation shows a reduction in the standard deviation of failures of about 44 % with the proposed strategy compared to the normal operation. The proposed strategy results in an increase of 3 years in the $B_{0.1}$ lifetime of the system. Moreover, the mean lifetime of the system is slightly increased with the proposed method in comparison to the normal operation. In addition, the control strategy delays the failures during flying time by actively sensing the junction temperature and controlling the power flow. The prognostic maintenance can be scheduled more precisely using the probability distribution of failure in the system.

Through these approaches, the potential of the graph theory based power routing for multi-objective optimization in modular power converters has been demonstrated. It is evident from the results that the optimization method offers better system level performance compared to the virtual resistance based system level control.

6 Modulator based Implementation of Power Routing

System level power routing methods based on graph theory focus on achieving system level reliability, efficiency and maintenance scheduling targets. This chapter discusses the implementation method for power routing on the converter level. For the implementation of power routing algorithms based on graph theory, the following strategy proposed in [J3] lays the foundation of this chapter:

- Modulator based junction temperature control of modular power converters using an Advanced Discontinuous Pulse Width Modulation (ADPWM) method [J3].

The ADPWM modulation scheme is proposed for a CHB-DAB based Smart Transformer architecture illustrated in Fig. 3.10. One of the major challenges for power routing in a multi-stage modular converter is due to the fact that when power flows through the cells connected in series, independent control of reliability and efficiency of series connected cells becomes difficult. Therefore, to facilitate independent control of junction temperature and power flow among two modular converter cells connected in series, ADPWM method is proposed.

First, a review of the state-of-the-art modulation-based junction temperature control methods for the modular converter architectures is presented. Afterward, the principle and application of the proposed modulation scheme are described. An experimental validation together with the lifetime impact of the proposed method concludes this chapter.

6.1 State-of-the-art Modulation based Junction Temperature Control Methods for Modular Converters

For modular power converters, modulation strategy focusing on distributed commutations to reduce the device switching frequency in the Cascaded H-Bridge converter for lowering the losses and thereby achieving thermal balance among the converter cells is discussed in [197]. In modular converter based Smart Transformer applications, the active thermal control strategies can have multiple objectives compared to the unique objective of thermal cycling reduction in single converters. In case of converter level strategies, the objective is to attain the thermal balance among the devices. However, for the complex modular architectures used in the Smart Transformer application, the converter level ATC to attain thermal balance among the power devices seems insufficient to attain high reliability, and hence power routing is proposed.

To achieve the junction temperature control by distributing the processed power through power routing, two modulation methods were proposed for the Smart Transformer application; multi-frequency [159] and variable-clamping angle discontinuous modulation [199]. The concept of these modulations is shown in Fig. 6.1 (a) and (b), respectively. The multi-frequency method was proposed to extend the power imbalance capability by employing the third-order harmonic as shown in Fig. 6.1 (a). This results in 15.5 % improved capability. However, it is limited in manipulating the thermal stress of devices in different building

blocks. In particular, the devices in the DC/DC converter and the CHB converter cannot be manipulated simultaneously without affecting the other one [198]. In order to overcome the limitation of the multi-frequency method, the discontinuous modulation was proposed, which exploits the clamping angle as a control parameter to perform the thermal stress control as shown in Fig. 6.1 (b) [199]. In this method, the losses of a CHB cell in an additional loading path are significantly decreased by the clamping region. However, since the loading of the CHB cells depends on the clamping angle, the thermal stress manipulation of the CHB cells leads to the power imbalance in series connected DAB cells, and consequently undesired thermal stress in DAB converters. Therefore, such a modulation scheme has limited flexibility for the reliability improvement strategies at the system level [178].

6.2 Principle, Applicability and Validation of ADPWM

The principle of the proposed method is shown in Fig. 6.2, which exploits the clamping angle φ and the shifting angle α as control parameters. Here, one modulation signal is clamped signal $m_{dm,c}$ and the other is non-clamped signal $m_{dm,nc}$. Remarkably, the clamping and shifting angles should be identical for both modulation signals so that the discontinuous regions in both signals are completely compensated.

Employing the concept described above, the proposed modulation strategy is shown in Fig. 6.3. The modulation has two variant signals: (a) a Center-Clamped Side-Non clamped (CCSN) m_{ccsn} signal and (b) a Center-Non clamped Side-Clamped (CNSC) m_{cnsc}. The proposed modulation signals have three discontinuous regions during a half period (from $-\pi/2$ to $\pi/2$), where $R1$ is centered at 0 rad with the clamping angle φ_c. $R2$ and $R3$ are centered at shifting angle $\pm\alpha$ rad with the clamping angle φ_s. Another half period (from $\pi/2$ to $3\pi/2$) is symmetric with the previous period as shown in Fig. 6.3.

For the CCSN signal m_{ccsn}, the power is increased by R1 (clamped region), whereas it is reduced by R2 and R3 (non-clamped regions). In contrast, the power is decreased by R1 (non-clamped region) and increased by the R2 and R3 (clamped regions) for the CNSC m_{cnsc}. Consequently, the signal which processes more power or less power is determined by the three angles φ_c, φ_s and α. For example, if $\varphi_c > 2\varphi_s$, the CCSN signal m_{ccsn} allows additional loading, whereas if $\varphi_c < 2\varphi_s$, the CNSC signal m_{cnsc} allows additional loading.

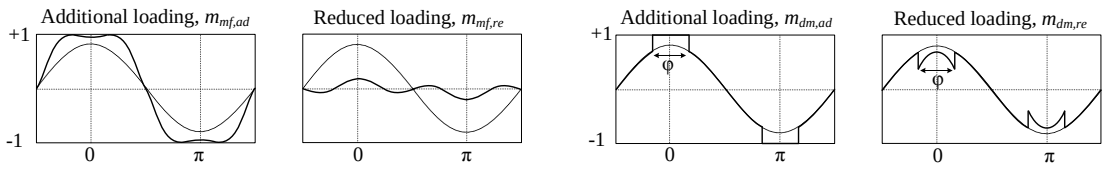


Figure 6.1: Conventional modulation based active thermal control methods for modular converters in ST application; (a) multi-frequency modulation [198] and (b) discontinuous modulation [199] [J3].

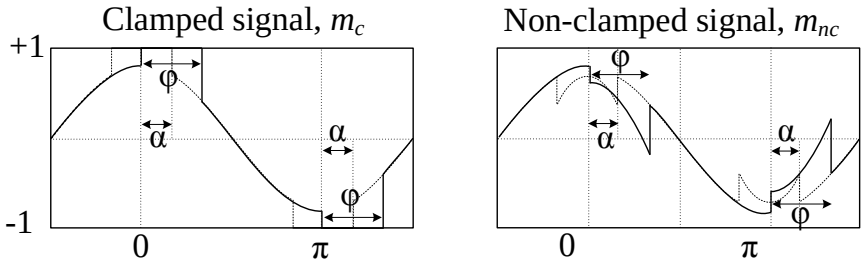


Figure 6.2: Discontinuous modulation with the clamping angle φ and the shifting angle α [J3].

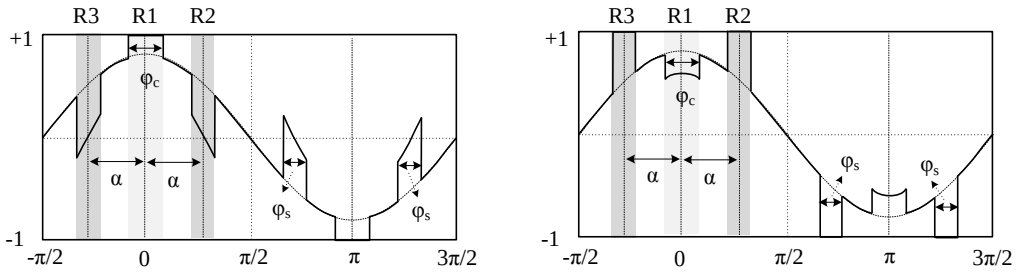


Figure 6.3: Proposed discontinuous modulation, which has two variant signals; (a) Center-Clamped Side-Non clamped (CCSN) m_{ccsn} and (b) Center-Non clamped Side-Clamped (CNSC) m_{cnsc} [J3].

Here, the shifting angle α should be carefully chosen in order to avoid overlapping between the discontinuous regions (R1, R2 and R3). This condition is expressed in

$$\alpha \geq \frac{1}{2}(\varphi_s + \varphi_c). \tag{6.1}$$

The loss distribution among CHB cells determines the junction temperature of the individual cells. The loss distribution is mainly decreased by the clamped region, while it is hardly modified by the non-clamped region. Namely, for the CCSN signal m_{ccsn}, the loss distribution is determined by the clamping angle φ_c (R1), whereas it is controlled by the clamping angle φ_s and the shifting angle α (R2 and R3) for the CNSC signal m_{cnsc}. Due to a large set of operating points (i.e. combination of clamping angle and shifting angle), it is assumed that the shifting angle is zero. It is reasonable since the loss distribution is mainly affected by the clamping angle as mentioned before. The loss distribution of the CHB cell and DC/DC cell is shown in Fig. 6.4 (a), depending on loading power. The loss of DC/DC cell features a positive coefficient for the loading power, whereas the loss of CHB cell is non-linear for the loading power as analyzed in [199]. The loss of the overall system is obtained by a summation of the loss of CHB and DC/DC cells as shown in Fig. 6.4 (b). As it can be seen, the loss of both additional loading and unloading building blocks is reduced with the proposed method. Consequently, the proposed method performs thermal stress manipulation, while achieving a higher efficiency.

However, it would be worth pointing out a shortcoming of the proposed method. One of the

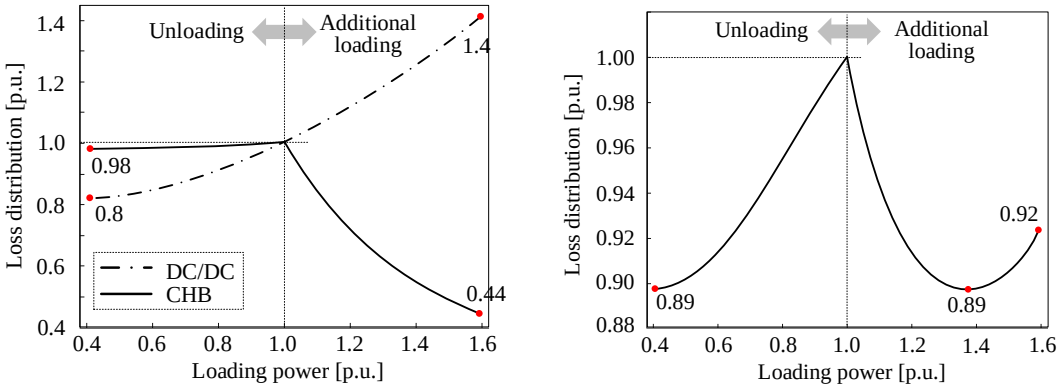


Figure 6.4: Loss distribution as a function of loading power: (a) DC/DC and CHB cells and (b) overall system [J3].

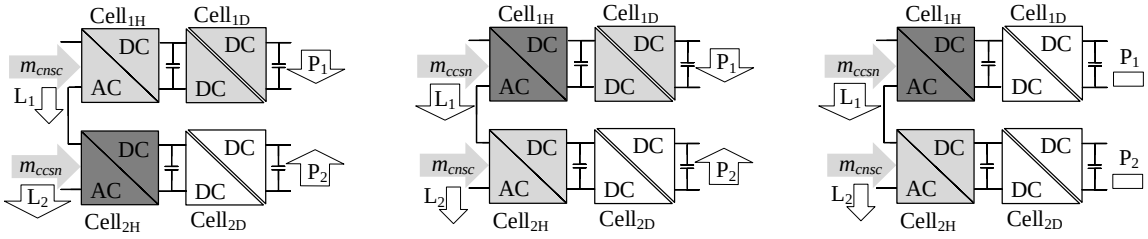
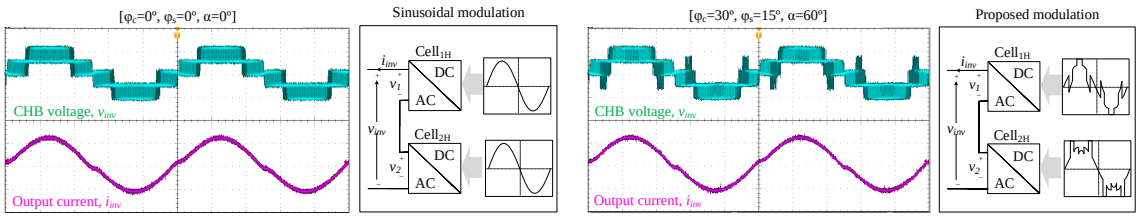


Figure 6.5: Representative scenarios for remaining useful lifetime of modular smart transformer; (a) one weak CHB cell and DC/DC cell in a same path and one very weak cell in a different path; (b) one very weak CHB cell and one weak DC/DC cell in a same path and one weak CHB cell; (c) one very weak CHB cell and one weak DC/DC cell in different path (white: healthy, light gray: weak, dark gray: very weak) [J3].

most attractive features of the CHB converters operating with the phase-shifted carriers is the higher equivalent switching frequency in AC-side. This feature achieves a higher power quality with a lower filter requirement. However, this is valid only when the CHB converter is operating under balanced conditions, namely, balanced cell voltage and modulation signal. The balanced condition is hardly achieved in many practical applications as mentioned in [200, 201]. The proposed ADPWM based power routing method would decrease the power quality as analyzed in [202], and furthermore, a method to improve the power quality with the discontinuous modulation has been proposed in [203].

To validate the significance of the proposed modulation strategy, various scenarios of the active thermal control for the modular smart transformer are considered. The possible combinations of health status of cells are shown in Fig. 6.5, considering two building blocks, where L_x is the required loss reduction of CHB cell and P_x represents the required loading power of DC/DC cell.

Figs. 6.5 (a) and (b) show challenging scenarios, where the lifetime of three cells needs to be



(a) (b)

Figure 6.6: CHB output voltage and current when (a) sinusoidal modulation ($\varphi_c = \varphi_s = \alpha = 0°$) and (b) proposed modulation ($\varphi_c = 30°$, $\varphi_s = 15°$, $\alpha = 60°$) [J3].

increased: One of DC/DC cells and two CHB cells have a lower remaining useful lifetime. The power of $Cell_{1D}$ is reduced, while the losses of both $Cell_{1H}$ and $Cell_{2H}$ are decreased. Here, one of two CHB cells (indicated in dark gray) has a much shorter remaining useful lifetime than the others. Hence, in Fig. 6.5 (a), the loss reduction of $Cell_{2H}$ should be more than that of $Cell_{1H}$ ($L_1 < L_2$) as the remaining useful lifetime of $Cell_{2H}$ is much shorter. On the other hand, for the case of Fig. 6.5 (b), the requirement of $L_1 > L_2$ should be satisfied by processing more power in path 1. As it is indicated, the cell with the shorter remaining useful lifetime is modulated by the CCSN signal, because the losses can be further reduced with the center-clamped region. For the scenario in Figs. 6.5 (c), only two CHB cells need to be thermally compensated, whereas the power through each path remains equal. One of the CHB cells has a shorter remaining useful lifetime and the cell with shorter remaining useful lifetime is operated by the CCSN signal to achieve the loss reduction ($L_1 > L_2$).

The proposed method is validated with a developed experimental setup, which consists of 5-level CHB converter and two Dual Active Bridge (DAB) DC/DC converters as shown in Fig. C.6. Remarkably, the power of each power path is measured by a power analyzer 'Yokogawa WT3000E' to confirm the power routing and the open power modules (part number: DP25H1200T101667) are employed, which enables direct access to power semiconductors. The junction temperature is measured through optic fiber sensors 'OTG-F' with signal conditioner 'ProSens'.

First, the feasibility of the proposed method is validated in Fig. 6.6, showing the output voltage and current of the CHB converter. Fig. 6.6 (a) presents the waveforms with sinusoidal modulation ($\varphi_c = \varphi_s = \alpha = 0°$), in which the output voltage definitely has the 5-level and the current is sinusoidal. As the power quality is one of the most important criteria in most applications, it is essentially required to validate if the discontinuous regions in the proposed method are completely internally compensated, resulting in a sinusoidal output current. This is shown in Fig. 6.6 (b), when $\varphi_c = 30°$, $\varphi_s = 15°$, $\alpha = 60°$ as an example. Here, one cell is modulated with m_{ccsn} and another by m_{cnsc}. As it is seen, the switching frequency of the voltage during the clamped regions is reduced, while keeping the current sinusoidal.

The influence of the proposed method on thermal stress control is validated by directly measuring the junction temperature. For this, three scenarios (a), (b) and (c) (refer Fig. 6.5) are considered and they are demonstrated under three operating points described in Table 6.1

Table 6.1: System operating condition to validate the thermal stress control ability.

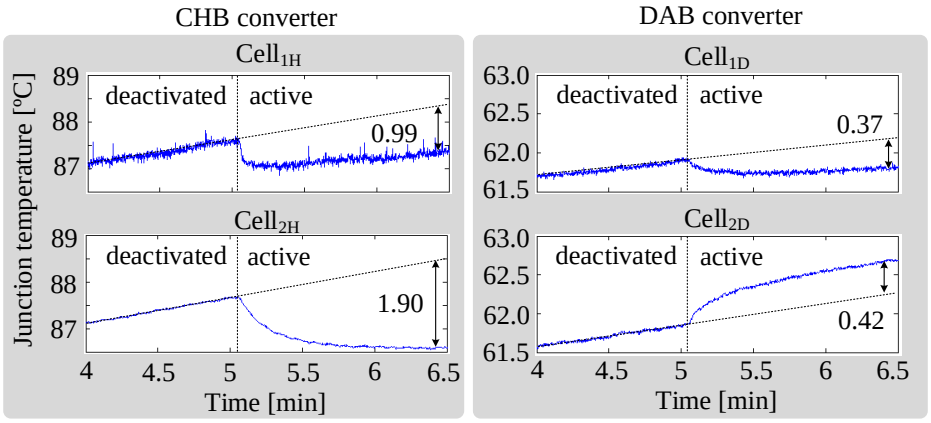
[Scenario]	φ_c	φ_s	α	P_1	P_2	L_1	L_2
	[°]			[p.u.]			
Fig. 6.5 (a)	60	15	75	0.897	1.103	0.916	0.721
Fig. 6.5 (b)	60	40	65	0.908	1.092	0.721	0.917
Fig. 6.5 (c)	30	11	30	1.005	0.995	0.855	0.958

along with respective powers (P_1 and P_2) and loss reductions (L_1 and L_2). The measured junction temperature is illustrated in Fig. 6.7, where the proposed method is activated at certain point to observe its influence (i.e. from sinusoidal method to proposed method). Under the first operating condition in Fig. 6.7 (a), the first CHB cell $Cell_{1H}$ has 0.99 K reduction, while the second cell $Cell_{2H}$ features the higher reduction of 1.9 K. Focusing on the DAB, it is expected that the junction temperature of the first cell $Cell_{1D}$ is reduced with the power of 0.897 [p.u.], whereas that of the second cell $Cell_{2D}$ increases with the power of 1.103 [p.u.]. The junction temperature clearly shows the influence of the modified loading. For the second case in Fig. 6.7 (b), the power routing strategy is the same (i.e. increased loading in path 1 and reduced loading in path 2). However, the reliability requirement for CHB cells is different. The first cell needs a further loss reduction (0.721 [p.u.]) than that of the second cell (0.917 [p.u.]). As it is seen, the temperature reduction of the first cell (2.01 K) is larger than that of the second cell (1.78 K). The final case in Fig. 6.7 (c) shows that the total power is equally loaded, while achieving the loss reduction of CHB cells. Only CHB cells have the temperature reduction of 1.35 K and 1.05 K respectively, whereas the temperature of the DAB cells is not varied as the power is not changed.

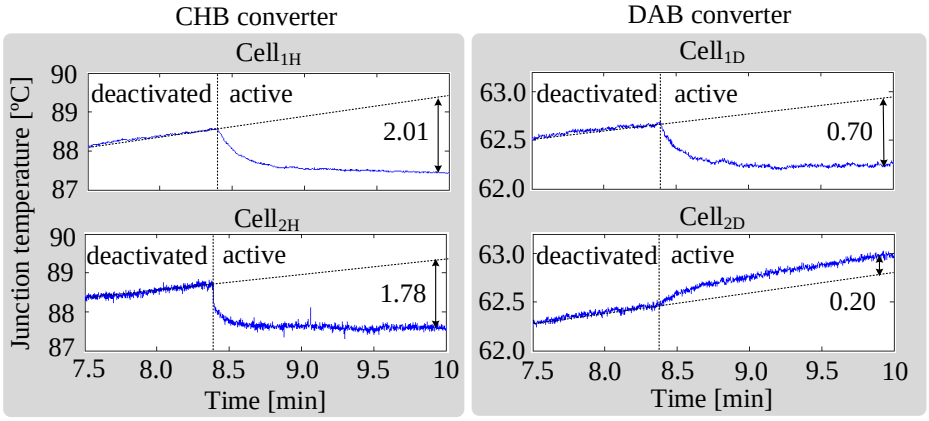
Through the above results, it has been confirmed that the proposed method has capability to individually control the thermal stress of cells. Further, it needs to be noted that the DC-link voltage for the above experiments is limited to $200V$ even though the device is rated for $1200V$, because of the lower insulation voltage of the open IGBT module. This means that the switching loss reduction by the proposed modulation is lower than the nominal value. Consequently, it can be expected that a higher temperature reduction can be achieved with the nominal DC-link voltage (i.e. typically between $600V$ and $800V$).

Impact of Proposed Method on Lifetime

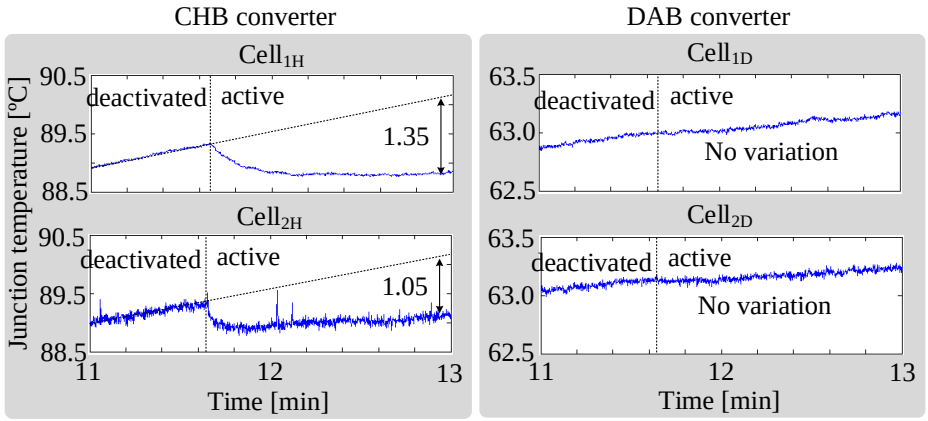
Based on the result in Fig. 6.7, the impact of the proposed method on the lifetime is analytically discussed. Therefore, the lifetime is compared to the equal power loading case. In other words, the relative lifetime change with the equal loading and the unequal loading is derived. Remarkably, it should be mentioned that since there is no power cycling (i.e. constant total power) in Fig. 6.7, the mean junction temperature $T_{j,av}$ is solely considered in the lifetime model as an effective factor. The results for both CHB and DAB cells are summarized in Table 6.2 using (2.6) and (2.18), where ΔN_f is the change in the number of cycles to failure. As it can be seen, the temperature reduction leads the lifetime increase, whereas the lifetime



(a)



(b)



(c)

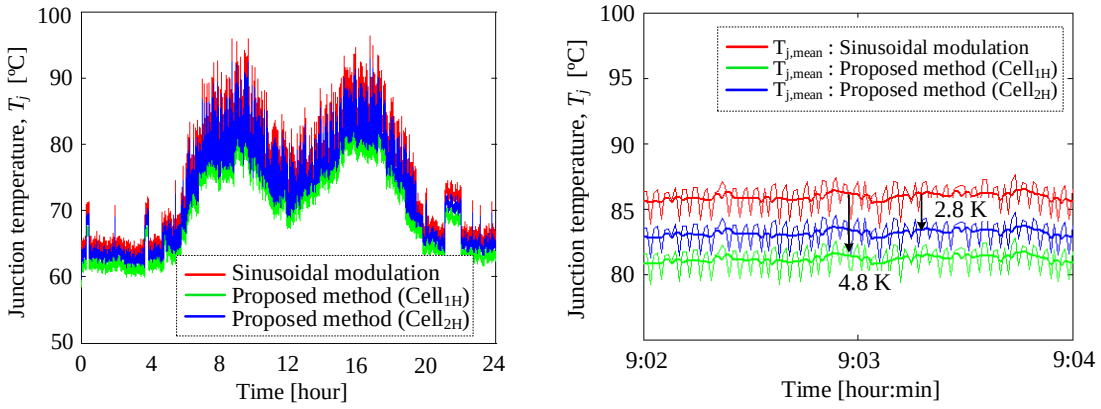
Figure 6.7: Verification of thermal behavior under system operating condition in Table 6.1, representing the scenario in: (a) Fig. 6.5 (a), (b) Fig. 6.5 (b) and (c) Fig. 6.5 (c) [J3].

decreases with the temperature increase. The results of the lifetime variation are according to the scenarios presented in Fig. 6.5.

To evaluate the remaining-useful-lifetime of power semiconductor devices based on the thermal stress, an analytical study with the electro-thermal model is conducted, as presented in Chapter 2 [178, 199]. The impact of the proposed method on the lifetime is evaluated with

Table 6.2: Impact of temperature reduction in Fig. 6.7 on number of cycle to failure.

Scenario Fig. 6.5	ΔN_f [%]			
	$Cell_{1H}$	$Cell_{2H}$	$Cell_{1D}$	$Cell_{2D}$
(a)	+5.59	+10.21	+2.39	-2.64
(b)	+11.74	+10.32	+2.39	-2.63
(c)	+7.63	+5.88	0	0



(a) (b)

Figure 6.8: The junction temperature profile for the CHB cells $Cell_{1H}$ and $Cell_{2H}$ without and with proposed power routing for the scenario in Fig. 6.5 (b): (a) for one day and (b) enlarged for 2 minutes [J3].

Table 6.3: Remaining useful lifetime change with the proposed method with electro-thermal ST model under one day mission profile.

Scenario Fig. 6.5	Percentage change in N_f (ΔN_f) [%]			
	$Cell_{1H}$	$Cell_{2H}$	$Cell_{1D}$	$Cell_{2D}$
(a)	+33.18	+45.30	+77.83	-315.76
(b)	+48.07	+39.25	+73.84	-259.29
(c)	+32.93	+23.25	-7.01	+6.65

one day mission profile presented in [199], considering the scenarios in Table 6.1. In Fig. 6.8 (a), the junction temperature profiles of the CHB cells for one day mission profile is shown for the scenario in Fig. 6.5 (b). To clearly distinguish the thermal stress differences without and with the proposed method, the enlarged junction temperature profiles for 2 minutes are shown in Fig. 6.8 (b), where the mean junction temperature of $Cell_{1H}$ is reduced by 4.8 K and that of $Cell_{2H}$ by 2.8 K. Here, it is evident that the thermal stress of both CHB cells have decreased compared to that of the equal power sharing operation with the sinusoidal modulation. The lifetime calculation from these temperature profiles indicates that the percentage lifetime increase of $Cell_{1H}$ (+48.07 %) is higher than that of $Cell_{2H}$ (+39.25 %) as given in Table 6.3.

The results for all three cases are summarized in Table 6.3. The case given in Fig. 6.5 (a)

shows that the CHB cell $Cell_{2H}$ is weaker than and the CHB cell $Cell_{1H}$. In addition, the DAB cell $Cell_{1D}$ needs to be thermally compensated. The lifetime evaluation results show that the lifetime of the weaker CHB cell $Cell_{2H}$ is improved by +45.30 %, while that of $Cell_{1H}$ is by +33.18 %. The lifetimes of the weak DAB cell have also improved significantly by +77.83 %, on the other hand, the lifetime of the healthy DAB cell $Cell_{2D}$ has decreased by approximately 3 times. Similarly, the proposed method is able to achieve a lifetime increase for the weak CHB cells, while maintaining a similar lifetime of DAB cells for the scenario indicated in Fig. 6.5 (c).

6.3 Summary of the Chapter

The ADPWM based power routing implementation strategy utilizes the modulator to control device losses and thereby thermal stress for a multi-stage modular converter architecture used in applications such as Smart Transformer. Experimental validation of different scenarios in the multi-stage modular converter demonstrates the capability for independent control of thermal stress in the medium voltage converter and the isolation stage. A case study of one day mission profile based lifetime analysis indicates the remaining useful lifetime of a very weak CHB-cell to increase by 48 % and the remaining useful lifetime of a weak DC/DC converter cell to increase by 77 %. It is to be noted that the increase in lifetime of weak cells is achieved by over-stressing the healthy converter cell. In addition, it has been revealed that the proposed method has the potential to achieve higher efficiency of the overall system.

7 Summary, conclusion and future research

7.1 Summary

The consolidation of power electronics as an actuator in various sectors such as renewable energy generation and distribution, more electric aircraft and electric vehicles has boosted reliability research in power electronics. Remarkably, the significance of modular power converters has escalated drastically in various applications such as electrical power distribution, industrial motor drives and more electric aircraft. For modular systems, one of the promising features is the ability to replace converter cells in case of failures. Manufacturing tolerances and operating condition variations of each cell in a modular system result in difference in wear-out of the cells. As a consequence, both the failure replacement cycles and asymmetric wear-out lead to cells with different aging in a modular converter.

The difference in aging among the cells can lead to multiple maintenance instances, lower availability and higher maintenance cost. The solution proposed to overcome this challenge is through power routing. With the help of power routing, the thermal stress based failures can be delayed, maintenance can be scheduled optimally, and abnormal operation of the converter due to the change in ambient conditions or auxiliary system failures can be controlled. In this context, this thesis focuses on the implementation strategies of the system level power routing in modular converters to improve reliability. The idea of using graph theory for achieving optimal power flow in modular power converters was proposed in the framework of HEART project. As a part of the research activity under HEART project, this work has contributed to the further development of the unified modeling technique of modular converters using graph theory for the implementation of multi-objective power flow solutions. The power flow optimization algorithms are proposed to address reliability, efficiency and maintenance scheduling challenges in modular converters.

Since it is well-known that the power semiconductors are one of the most vulnerable components in a power converter system contributing to about 40 % of total failures, the focus is on the power semiconductor reliability to evaluate the power converter reliability. The main failure mechanisms in power semiconductor modules have been identified as the bond-wire liftoff, solder fatigue and metallization reconstruction. Thermal cycling is established as the major stressor behind the aforementioned failure mechanisms. To counteract the challenges posed by power semiconductor reliability, techniques such as condition monitoring and prognostic maintenance are employed to monitor and schedule maintenance before the occurrence of failures. Apart from these passive methods, there are software and hardware based active thermal control methods to reduce the thermal cycling based wear-out, which are covered in Chapter 2. For the analysis of lifetime and thermal stress based wear-out, mission profile and Monte-Carlo based reliability analysis are performed using state-of-the-art approaches. A detailed explanation of the methodology of thermal stress and reliability analysis based on PoF concludes the chapter.

In Chapter 3, selected modular topologies in the Smart Transformer and MEA applications are described in the detail. As a prerequisite for the development of intelligent control algorithms in modular power converters, an approach for the representation of the modular power converters using graph theory has been developed. Graph theory is used to model the power flow between the individual converter cells analogous to the information flow in communication networks. Complex multi-stage modular converter architectures are represented as graphs to establish a common framework for the implementation of optimal power flow solutions.

Analysis in Chapter 4 shows that the thermal and electrical parameters variations of the power devices and cooling system results in the difference in aging of the converter cells. The power routing strategy proposed for equalizing the aging of the converter cells by unequal loading has been carefully studied. First, the power unbalance limits for the CHB converter is derived analytically and validated experimentally for two state-of-the-art modulation schemes. Subsequently, a system level power routing algorithm based on virtual resistors has been proposed for IPOP modular converters and multi-stage ISOP configurations. The virtual resistor based power routing in IPOP configuration for the LV side of the ST focuses on delaying failures of individual cells. The results show that the system lifetime increased by approximately $7.5-44\%$ under the given conditions. In the case of multi-stage ISOP modular converters, the definition of virtual resistance becomes more complex due to the series connected nature of the cells. For CHB-DAB modular converter architecture, virtual resistance based power routing is developed considering the individual impact of CHB and DAB virtual resistance values on the total system lifetime. To evaluate the performance of the proposed method in real-field applications, a Monte-Carlo analysis is performed to consider the electrical and parameter variations from their nominal values. The results indicate that the proposed virtual resistance method is promising since an improvement of $4.4\,\%$ in B_{10} lifetime is obtained compared to the conventional method without power routing. The potential of the modular architecture control system to route the power internally to achieve thermal stress control is demonstrated experimentally.

Since equalizing thermal stress is not the only target in many applications, it is necessary to develop generalized modeling and control of modular converters to enable power routing strategy to achieve multiple targets. With this perspective, graph theory has been identified as a suitable approach to model and develop multi-objective control algorithms. In Chapter 5, graph theory based optimization algorithms have been proposed for modular power converters to tackle the multi-objective problems of reliability, efficiency and maintenance scheduling improvement. Three power routing optimization algorithms for achieving different targets are studied. The first method focuses on improving both the reliability and efficiency of the ST application. The algorithm is proposed for CHB-DAB architecture and a case study has been performed to evaluate the effectiveness of the method. Under the given boundary conditions, the algorithm is able to increase the lifetime of the system by $39\,\%$ and is able to concentrate the failure probability around the maintenance instance. Since the efficiency of the cells is also considered for optimization, the losses are redistributed according to the individual efficiencies of the cells, and thereby the system efficiency has only

decreased by 0.2 % to achieve the increase in lifetime. In order to generalize the proposed algorithm for different operating conditions, Monte-Carlo simulation has been carried out. The results show that the B_{10} lifetime of the system increased by 66 % compared to that of normal operation. In the second method, the main goal is to improve the maintenance scheduling of modular converters for the ST application. This algorithm offers the flexibility to schedule maintenance according to the availability of maintenance personnel and resources by controlling the wear-out based failures of power devices. Moreover, the results demonstrate the effectiveness of the proposed algorithm to decrease the maintenance schedule frequency from 10 to 3 times. Since the algorithm maintains the probability of failure of the converter cells very low during the normal operating period, the overall reliability and availability of the system increases. The third algorithm is proposed for a very high reliability application in more electric aircraft. The optimization algorithm is developed for a modular DC-DC in MEA power distribution system to actively monitor and control the junction temperature. With the help of Monte-Carlo simulations, it is demonstrated that the proposed power routing control is able to reduce the standard deviation of failures by 44 % compared to the normal operation and increase $B_{0.1}$ lifetime by 3 years. Apart from this, the proposed strategy has the potential to delay failures during flying hours caused by abnormalities such as insufficient coolant, increased power device losses, etc. The development of these three optimization algorithms with different objectives based on graph theory for modular power converters demonstrate the potential of using graph theoretic models and optimization techniques as a generalized method for power routing. Moreover, the optimization algorithms offer better system level performance compared to the virtual resistance based power routing strategies.

Chapter 6 explores a novel modulator based implementation of power routing in multi-stage modular converter architectures. The ADPWM method demonstrates very high flexibility to independently control the thermal stress in the series connected multi-stage modular converter cells in CHB-DAB ST architecture. Experimental validation of different scenarios of cell aging in the CHB-DAB converter demonstrates the capability for independent control of thermal stress in the medium voltage converter and the isolation stage. The mission profile analysis shows that the remaining useful lifetime of a very weak CHB-cell has increased by 48 % and that of a weak DC/DC converter cell increased by 77 %. Moreover, the proposed method has the potential to achieve higher overall system efficiency.

7.2 Conclusion

The research work carried out in this thesis has been able to deliver the following contributions considering the research targets established in Section 1.4.

Target I: Analysis, design and implementation of power routing based active thermal control in modular converters

- Chapter 2 investigated physics-of-failure based reliability analysis of power converters and developed a methodology for evaluating the lifetime of power converters.

- Chapter 4 evaluated the limitations of power routing in modular converters and verified results experimentally.
- Chapter 4 introduced novel virtual resistor based system level power routing algorithms for the ST converter architectures and presented experimental proof-of-concept.
- Chapter 6 investigated the impact of a novel modulation scheme on the implementation of power routing in the given modular converter architecture.

Target II: Modeling and development of graph theory based optimal power flow solutions for modular power converters

- Chapter 3 presented a unique modeling technique of modular power converters as graphs for developing power routing algorithms.
- Chapter 5 explored graph theory based optimization algorithms for improving reliability with minimal efficiency reduction in modular power converters.
- Chapter 5 also discussed the formulation and evaluation of a novel methodology for actively controlling the maintenance scheduling.

7.3 Future research

The modular power converters offer the opportunity to investigate new control strategies to improve key performance indicators such as reliability, efficiency, maintenance and fault-tolerance. This thesis has proposed modeling and control of modular power converters for the implementation of power routing.

To bolster the research outcomes of this thesis, the following research topics have been identified for potential future work.

- **Optimal power flow solutions considering power semiconductor devices and capacitors**

  In this work, only power semiconductor reliability was considered for reliability evaluation and improvement. However, it is well-known that capacitor reliability is critical for power converters. In the generalized power routing approach using graph theory, it is possible to consider the capacitor as a reliability critical element and optimize the power routing control for both capacitors and power devices. Future studies can evaluate the impact of power routing on the capacitor lifetime/reliability and propose methods to consider it in optimal power flow solution algorithms.

- **Experimental verification of the proposed power routing strategies with lifetime tests**

  The impact of power routing on the junction temperature of the power devices are experimentally demonstrated in Chapter 4. However, the impact of the power routing control on the lifetime for a given mission profile on modular systems needs to be investigated by performing long-term reliability tests. The experimental validation of the maintenance schedule optimization and delaying failures is challenging due to the requirements such as online condition monitoring techniques, controlled operating environmental conditions (for example, temperature and humidity) and suitable mission profiles. Such an extensive experimental investigation could reinforce the contribution of power routing methods discussed by analytical/simulation and conceptual experimental studies.

- **Extension of the graph theory based modeling and control by the integration of data-driven models**

  The active thermal control of the power semiconductors is driven mainly by the thermal stress based wear-out. However, thermal stress is not the only factor governing the failures in power devices and this is a potential opportunity to develop data-driven models to define lifetime/reliability. The graph theory modeling of the modular power converters visualizes it as a power flow network formed by nodes and edges. This provides the opportunity to use data-driven methods to formulate weights for the graphs. In short, the generalized graph theory based modeling of power converters is a potential platform for the development of data-driven based power routing or advanced control strategies.

- **Inclusion of power quality and EMI emission in the multi-objective optimization criteria for power routing**

  Apart from reliability, efficiency and power density, power quality and EMI are two main aspects considered for the design of power converters. The variation of total harmonic distortion for a virtual resistor based power routing algorithm is presented in Chapter 4. The power quality and EMI emission are affected by the power routing, and hence the impact of different power routing strategies on these factors needs to be investigated in detail. The graph theory based optimization methods provide the opportunity to consider such objectives in the optimization function. Therefore, it is worth pursuing more research to explore this topic.

8 References

[1] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, March 2014.

[2] H. Wang and F. Blaabjerg, "Power electronics reliability: State of the art and outlook," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020.

[3] B. K. Bose, "Global energy scenario and impact of power electronics in 21st century," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2638–2651, 2013.

[4] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor power devices: physics, characteristics, reliability*. Springer Science & Business Media, 2011.

[5] M. Rausand and H. Arnljot, *System reliability theory: models, statistical methods, and applications*. John Wiley & Sons, 2004, vol. 396.

[6] M. Liserre, M. Andresen, L. Costa, and G. Buticchi, "Power routing in modular smart transformers: Active thermal control through uneven loading of cells," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43–53, Sept 2016.

[7] N. Sintamarean, F. Blaabjerg, H. Wang, F. Iannuzzo, and P. de Place Rimmen, "Reliability oriented design tool for the new generation of grid connected pv-inverters," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2635–2644, 2015.

[8] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17–26, June 2013.

[9] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441–1451, May 2011.

[10] M. Pecht, A. Dasgupta, D. Barker, and C. T. Leonard, "The reliability physics approach to failure prediction modelling," *Quality and Reliability Engineering International*, vol. 6, no. 4, pp. 267–273, 1990.

[11] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of igbt modules - various factors influencing lifetime," in *5th International Conference on Integrated Power Electronics Systems*, March 2008, pp. 1–6.

[12] D. A. Murdock, J. E. R. Torres, J. J. Connors, and R. D. Lorenz, "Active thermal control of power electronic modules," *IEEE Transactions on Industry Applications*, vol. 42, no. 2, pp. 552–558, March 2006.

[13] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg, and M. Saeedifard, "Mission profile-based system-level reliability prediction method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6916–6930, 2020.

[14] K. Ma, U. M. Choi, and F. Blaabjerg, "Prediction and validation of cumulative distribution function for power semiconductor devices with mission profiles in motor drive application," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[15] M. Andresen, "Active thermal control of power electronic modules in smart transformer applications," Ph.D. dissertation, 2017. [Online]. Available: https://macau.uni-kiel.de/receive/diss_mods_00021296

[16] J. Falck, M. Andresen, and M. Liserre, "Thermal-based finite control set model predictive control for igbt power electronic converters," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–7.

[17] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3. IEEE, 2003, pp. 6–pp.

[18] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE transactions on power electronics*, vol. 30, no. 1, pp. 37–53, 2014.

[19] P. Zumel, L. Ortega, A. Lázaro, C. Fernández, A. Barrado, A. Rodríguez, and M. M. Hernando, "Modular dual-active bridge converter architecture," *IEEE Transactions on industry Applications*, vol. 52, no. 3, pp. 2444–2455, 2016.

[20] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 mw power rating and 17-level-output-voltage," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No. 04CH37551)*, vol. 4. IEEE, 2004, pp. 2572–2576.

[21] M. Andresen, L. F. Costa, G. Buticchi, and M. Liserre, "Smart transformer reliability and efficiency through modularity," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 3241–3248.

[22] J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage multilevel converters," in *2013 IEEE Energy Conversion Congress and Exposition*, Sep. 2013, pp. 359–366.

[23] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Solid-state transformer and mv grid tie applications enabled by 15 kv sic igbts and 10 kv sic mosfets based multilevel converters," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3343–3360, 2015.

[24] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, Jan 2015.

[25] L. Ferreira Costa, "Modular power converters for smart transformer architectures," Ph.D. dissertation, 2019. [Online]. Available: https://macau.uni-kiel.de/receive/diss_mods_00026108

[26] F. Camci, "System maintenance scheduling with prognostics information using genetic algorithm," *IEEE Transactions on Reliability*, vol. 58, no. 3, pp. 539–552, Sept 2009.

[27] Y. Ting, S. de Haan, and B. Ferreira, "Modular single-active bridge dc-dc converters: Efficiency optimization over a wide load range," *IEEE Industry Applications Magazine*, vol. 22, no. 5, pp. 43–52, Sept 2016.

[28] P. O'Connor and A. Kleyner, *Practical reliability engineering*. John Wiley & Sons, 2012.

[29] M. Liserre, G. Buticchi, J. I. Leon, A. Marquez Alcaide, V. Raveendran, Y. Ko, M. Andresen, V. G. Monopoli, and L. Franquelo, "Power routing: A new paradigm for maintenance scheduling," *IEEE Industrial Electronics Magazine*, vol. 14, no. 3, pp. 33–45, 2020.

[30] V. Raveendran, M. Andresen, and M. Liserre, "Lifetime control of modular smart transformers considering the maintenance schedule," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2018, pp. 60–66.

[31] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, 2013.

[32] J. Falck, C. Felgemacher, A. Rojko, M. Liserre, and P. Zacharias, "Reliability of power electronic systems: An industry perspective," *IEEE Industrial Electronics Magazine*, vol. 12, no. 2, pp. 24–35, June 2018.

[33] L. M. Moore and H. N. Post, "Five years of operating experience at a large, utility-scale photovoltaic generating plant," *Progress in Photovoltaics: Research and Applications*, vol. 16, no. 3, pp. 249–259, 2008.

[34] D.-I. R. Amro, "Power cycling capability of advanced packaging and interconnection technologies at high temperature swings," 2006.

[35] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, "Semikron application manual power semiconductors," *Ilmenau: ISLE*, 2011.

[36] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics reliability*, vol. 42, no. 4-5, pp. 653–667, 2002.

[37] J. Rudzki, M. Becker, R. Eisele, M. Poech, and F. Osterwald, "Power modules with increased power density and reliability using cu wire bonds on sintered metal buffer layers," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, Feb 2014, pp. 1–6.

[38] K. Takao and S. Kyogoku, "Ultra low inductance power module for fast switching sic power devices," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 313–316.

[39] A. Hamidi, N. Beck, K. Thomas, and E. Herr, "Reliability and lifetime evaluation of different wire bonding technologies for high power igbt modules," *Microelectronics reliability*, vol. 39, no. 6-7, pp. 1153–1158, 1999.

[40] U. Scheuermann, "Reliability challenges of automotive power electronics," *Microelectronics Reliability*, vol. 49, no. 9-11, pp. 1319–1325, 2009.

[41] K. B. Pedersen, "Igbt module reliability. physics-of-failure based characterization and modelling," 2014.

[42] H. Oh, B. Han, P. McCluskey, C. Han, and B. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 2413–2426, 2015.

[43] H. Y. and S. Y.H., "Condition monitoring techniques for electrical equipment-a literature survey," *IEEE Transactions on Power Delivery*, vol. 18, pp. 4–13, 2003.

[44] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *Power Electronics, IEEE Transactions on*, vol. 25, pp. 2734–2752, 2010.

[45] M. H. M. Sathik, J. Pou, S. Prasanth, V. Muthu, R. Simanjorang, and A. K. Gupta, "Comparison of igbt junction temperature measurement and estimation methods-a review," in *2017 Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, Oct 2017, pp. 1–8.

[46] S. Beczkowski, P. Ghimre, A. R. de Vega, S. Munk-Nielsen, P. Th *et al.*, "Online vce measurement method for wear-out monitoring of high power igbt modules," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*. IEEE, 2013, pp. 1–7.

[47] S. Beczkowski, P. Ghimre, A. R. de Vega, S. Munk-Nielsen, B. Rannestad, and P. Thï¿½gersen, "Online vce measurement method for wear-out monitoring of high power igbt modules," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–7.

[48] Yong-Seok Kim and Seung-Ki Sul, "On-line estimation of igbt junction temperature using on-state voltage drop," in *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, vol. 2, 1998, pp. 853–859 vol.2.

[49] G. Coquery, R. Lallemand, D. Wagner, M. Piton, H. Berg, and K. Sommer, "Reliability improvement of the soldering thermal fatigue with alsic technology on traction high power igbt modules," in *Conférence EPE, Lausanne*, 1999.

[50] L. Fratelli, G. Giannini, B. Cascone, and G. Busatto, "Reliability test of power igbts for railway traction," in *Proc. EPE*, 1999, pp. 1–7.

[51] D. Barlini, M. Ciappa, M. Mermet-Guyennet, and W. Fichtner, "Measurement of the transient junction temperature in mosfet devices under operating conditions," *Microelectronics Reliability*, vol. 47, no. 9-11, pp. 1707–1712, 2007.

[52] A. Forsyth, S. Yang, P. Mawby, and P. Igic, "Measurement and modelling of power electronic devices at cryogenic temperatures," *IEE Proceedings-Circuits, Devices and Systems*, vol. 153, no. 5, pp. 407–415, 2006.

[53] H. Lu, T. Tilford, C. Bailey, and D. R. Newcombe, "Lifetime prediction for power electronics module substrate mount-down solder interconnect," in *2007 International Symposium on High Density packaging and Microsystem Integration*. IEEE, 2007, pp. 1–10.

[54] J. Lehmann, M. Netzel, R. Herzer, and S. Pawel, "Method for electrical detection of bond wire lift-off for power semiconductors," in *ISPSD'03. 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs, 2003. Proceedings.* IEEE, 2003, pp. 333–336.

[55] RELIAWIND, "Reliability focused research on optimizing wind energy systems design, operation and maintenance: Tools, proof of concepts, guidelines and methodologies for a new generation," 2011.

[56] J. Bell, "Condition based maintenance plus dod guidebook," *Department of Defense: Washington, DC, USA*, 2008.

[57] Z. Lv, J. Wang, G. Zhang, and H. Jiayang, "Prognostics health management of condition-based maintenance for aircraft engine systems," in *2015 IEEE Conference on Prognostics and Health Management (PHM)*, June 2015, pp. 1–6.

[58] Z. Li, J. Guo, and R. Zhou, "Maintenance scheduling optimization based on reliability and prognostics information," in *2016 Annual Reliability and Maintainability Symposium (RAMS)*, Jan 2016, pp. 1–5.

[59] A. Alghassi, S. Perinpanayagam, M. Samie, and T. Sreenuch, "Computationally efficient, real-time, and embeddable prognostic techniques for power electronics," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2623–2634, 2015.

[60] Y. Ko, "Thermally-compensated modulation strategies for modular power converters," Ph.D. dissertation, 2019. [Online]. Available: https://macau.uni-kiel.de/receive/diss_mods_00025229

[61] M. Andresen, J. Kuprat, V. Raveendran, J. Falck, and M. Liserre, "Active thermal control for delaying maintenance of power electronics converters," *Chinese Journal of Electrical Engineering*, vol. 4, no. 3, pp. 13–20, 2018.

[62] X. Wang, Z. Zhao, and L. Yuan, "Current sharing of igbt modules in parallel with thermal imbalance," in *2010 IEEE Energy Conversion Congress and Exposition*, Sep. 2010, pp. 2101–2108.

[63] Liang Wu and A. Castellazzi, "Temperature adaptive driving of power semiconductor devices," in *2010 IEEE International Symposium on Industrial Electronics*, July 2010, pp. 1110–1114.

[64] C. Sintamarean, H. Wang, F. Blaabjerg, and F. Iannuzzo, "The impact of gate-driver parameters variation and device degradation in the pv-inverter lifetime," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2014, pp. 2257–2264.

[65] P. Hofer, N. Karrer, and C. Gerster, "Paralleling intelligent igbt power modules with active gate-controlled current balancing," in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, vol. 2, June 1996, pp. 1312–1316 vol.2.

[66] X. Wang, Y. Wang, and A. Castellazzi, "Reduced active and passive thermal cycling degradation by dynamic active cooling of power modules," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 309–312.

[67] W. J. Choy, A. Castellazzi, and P. Zanchetta, "Adaptive cooling of power modules for reduced power and thermal cycling," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, Aug 2011, pp. 1–10.

[68] P. Kumar Prasobhu, V. Raveendran, G. Buticchi, and M. Liserre, "Active thermal control of gan-based dc/dc converter," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3529–3540, 2018.

[69] P. K. Prasobhu, V. Raveendran, G. Buticchi, and M. Liserre, "Active thermal control of a dc/dc gan-based converter," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 1146–1152.

[70] *Top-side cooled 650 V E-mode GaN transistor*, GaN Systems Inc., 2018, rev 180424.

[71] M. Andresen, G. Buticchi, J. Falck, M. Liserre, and O. Muehlfeld, "Active thermal management for a single-phase h-bridge inverter employing switching frequency control," in *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, May 2015, pp. 1–8.

[72] J. Falck, M. Andresen, and M. Liserre, "Active thermal control of igbt power electronic converters," in *Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE*. IEEE, 2015, pp. 000 001–000 006.

[73] J. Wu, L. Zhou, P. Sun, and X. Du, "Smooth control of insulated gate bipolar transistors junction temperature in a small-scale wind power converter," *IET Power Electronics*, vol. 9, no. 3, pp. 393–400, 2016.

[74] D. Kaczorowski, M. Mittelstedt, and A. Mertens, "Investigation of discontinuous pwm as additional optimization parameter in an active thermal control," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sep. 2016, pp. 1–10.

[75] J. Lemmens, J. Driesen, and P. Vanassche, "Dynamic dc-link voltage adaptation for thermal management of traction drives," in *2013 IEEE Energy Conversion Congress and Exposition*, Sep. 2013, pp. 180–187.

[76] K. Ma, M. Liserre, and F. Blaabjerg, "Reactive power influence on the thermal cycling of multi-mw wind power inverter," *IEEE Transactions on Industry Applications*, vol. 49, no. 2, pp. 922–930, March 2013.

[77] J. I. McCool, *Using the Weibull distribution: reliability, modeling, and inference*. John Wiley & Sons, 2012, vol. 950.

[78] F. Blaabjerg, K. Ma, and D. Zhou, "Power electronics and reliability in renewable energy systems," in *2012 IEEE International Symposium on Industrial Electronics*, May 2012, pp. 19–30.

[79] M. Musallam, C. Yin, C. Bailey, and M. Johnson, "Mission profile-based reliability design and real-time life consumption estimation in power electronics," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2601–2613, May 2015.

[80] J. G. McLeish, "Enhancing mil-hdbk-217 reliability predictions with physics of failure methods," in *2010 Proceedings - Annual Reliability and Maintainability Symposium (RAMS)*, 2010, pp. 1–6.

[81] M. Krasich, "How to estimate and use mttf/mtbf would the real mtbf please stand up?" in *2009 Annual Reliability and Maintainability Symposium*. IEEE, 2009, pp. 353–359.

[82] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, "Fast power cycling test of igbt modules in traction application," in *Proceedings of Second International Conference on Power Electronics and Drive Systems*, vol. 1, May 1997, pp. 425–430 vol.1.

[83] U. Scheuermann and U. Hecht, "Power cycling lifetime of advanced power modules for different temperature swings," *PCIM Nuremberg*, vol. 5964, 2002.

[84] U. Scheuermann and R. Schmidt, "A new lifetime model for advanced power modules with sintered chips and optimized al wire bonds," in *Proc. PCIM*, 2013, pp. 810–813.

[85] Y. Zhang, H. Wang, Z. Wang, Y. Yang, and F. Blaabjerg, "Impact of lifetime model selections on the reliability prediction of igbt modules in modular multilevel converters," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2017, pp. 4202–4207.

[86] A. Sangwongwanich, Y. Yang, D. Sera, and F. Blaabjerg, "Lifetime evaluation of grid-connected pv inverters considering panel degradation rates and installation sites," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1225–1236, Feb 2018.

[87] K. Ma, H. Wang, and F. Blaabjerg, "New approaches to reliability assessment: Using physics-of-failure for prediction and design in power electronics systems," *IEEE Power Electronics Magazine*, vol. 3, no. 4, pp. 28–41, 2016.

[88] S. E. De Leon-Aldaco, H. Calleja, F. Chan, and H. R. Jimenez-Grajales, "Effect of the mission profile on the reliability of a power converter aimed at photovoltaic applications - a case study," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2998–3007, 2012.

[89] F. Sossan, E. Namor, R. Cherkaoui, and M. Paolone, "Achieving the dispatchability of distribution feeders through prosumers data driven forecasting and model predictive control of electrochemical storage," *IEEE Transactions on Sustainable Energy*, vol. 7, no. 4, pp. 1762–1777, 2016.

[90] M. Pignati, M. Popovic, S. Barreto, R. Cherkaoui, G. D. Flores, J.-Y. Le Boudec, M. Mohiuddin, M. Paolone, P. Romano, S. Sarri *et al.*, "Real-time state estimation of the epfl-campus medium-voltage grid by using pmus," in *Innovative Smart Grid Technologies Conference (ISGT), 2015 IEEE Power & Energy Society*. IEEE, 2015, pp. 1–5.

[91] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 590–602, Feb 2015.

[92] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, no. 1, pp. 97–114, March 2014.

[93] U. Drofenik and J. W. Kolar, "A general scheme for calculating switching-and conduction-losses of power semiconductors in numerical circuit simulations of power electronic systems," in *Proceedings of the 2005 International Power Electronics Conference (IPEC-05), Niigata, Japan, April*. Citeseer, 2005, pp. 4–8.

[94] X. Kang, A. Caiafa, E. Santi, J. L. Hudgins, and P. R. Palmer, "Parameter extraction for a power diode circuit simulator model including temperature dependent effects," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, vol. 1, March 2002, pp. 452–458 vol.1.

[95] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-coupled multiport zvs bidirectional dc/dc converter with wide input range," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 771–781, 2008.

[96] M. Tariq, A. I. Maswood, A. C. Moreddy, C. J. Gajanayake, M. Y. Lee, and A. K. Gupta, "Reliability, dead-time, and feasibility analysis of a novel modular tankless zcs inverter for more electric aircraft," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 4, pp. 843–854, Dec 2017.

[97] M. Andresen, M. Schloh, G. Buticchi, and M. Liserre, "Computational light junction temperature estimator for active thermal control," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–7.

[98] C. H. van der Broeck, M. Conrad, and R. W. De Doncker, "A thermal modeling methodology for power semiconductor modules," *Microelectronics Reliability*, vol. 55, no. 9-10, pp. 1938–1944, 2015.

[99] *1200 V three phase PIM IGBT module*, Infineon Technologies AG, 10 2013, rev. 2.0.

[100] L. R. GopiReddy, L. M. Tolbert, B. Ozpineci, and J. O. P. Pinto, "Rainflow algorithm-based lifetime estimation of power semiconductors in utility applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3368–3375, 2015.

[101] K. Mainka, M. Thoben, and O. Schilling, "Lifetime calculation for power modules, application and theory of models and counting methods," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–8.

[102] B. Wang, J. Cai, X. Du, and L. Zhou, "Review of power semiconductor device reliability for power converters," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 101–117, 2017.

[103] I. Rychlik, "A new definition of the rainflow cycle counting method," *International journal of fatigue*, vol. 9, no. 2, pp. 119–121, 1987.

[104] D. R. Jones and M. F. Ashby, *Engineering materials 1: An introduction to properties, applications and design*. Elsevier, 2011.

[105] U. Choi, K. Ma, and F. Blaabjerg, "Validation of lifetime prediction of igbt modules based on linear damage accumulation by means of superimposed power cycling tests," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3520–3529, 2018.

[106] G. Zeng, C. Herold, T. Methfessel, M. Schï¿½fer, O. Schilling, and J. Lutz, "Experimental investigation of linear cumulative damage theory with power cycling test," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4722–4728, 2019.

[107] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of bond wire fatigue of igbts in a pv inverter under a long-term operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7171–7182, 2016.

[108] D. Zhou, H. Wang, F. Blaabjerg, S. K. Koer, and D. Blom-Hansen, "System-level reliability assessment of power stage in fuel cell application," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8.

[109] C. Bailey, T. Tilford, and H. Lu, "Reliability analysis for power electronics modules," in *2007 30th International Spring Seminar on Electronics Technology (ISSE)*, 2007, pp. 12–17.

[110] V. Raveendran, M. Andresen, and M. Liserre, "Improving onboard converter reliability for more electric aircraft with lifetime-based control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5787–5796, July 2019.

[111] M. Novak, A. Sangwongwanich, and F. Blaabjerg, "Monte carlo based reliability estimation methods in power electronics," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, 2020, pp. 1–7.

[112] Y. Yang, A. Sangwongwanich, and F. Blaabjerg, "Design for reliability of power electronics for grid-connected photovoltaic systems," *CPSS Transactions on Power Electronics and Applications*, vol. 1, no. 1, pp. 92–103, 2016.

[113] R. Pena-Alzola, G. Gohil, L. Mathe, M. Liserre, and F. Blaabjerg, "Review of modular power converters solutions for smart transformer in distribution system," in *2013 IEEE Energy Conversion Congress and Exposition*, Sept 2013, pp. 380–387.

[114] M. M. Steurer, K. Schoder, O. Faruque, D. Soto, M. Bosworth, M. Sloderbeck, F. Bogdan, J. Hauer, M. Winkelnkemper, L. Schwager, and P. Blaszczyk, "Multifunctional megawatt-scale medium voltage dc test bed based on modular multilevel converter technology," *IEEE Transactions on Transportation Electrification*, vol. 2, no. 4, pp. 597–606, Dec 2016.

[115] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A nonconventional power converter for plasma stabilization," *IEEE Transactions on Power Electronics*, vol. 5, no. 2, pp. 212–219, 1990.

[116] P. W. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Transactions on Industry Applications*, vol. 33, no. 1, pp. 202–208, 1997.

[117] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on industrial electronics*, vol. 54, no. 6, pp. 2930–2945, 2007.

[118] A. K. Jain and R. Ayyanar, "Pwm control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1215–1227, April 2011.

[119] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63–73, 1991.

[120] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 124–137, Jan 2015.

[121] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. D. Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 124–137, Jan 2015.

[122] S. Falcones, R. Ayyanar, and X. Mao, "A dc/dc multiport-converter-based solid-state transformer integrating distributed generation and storage," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2192–2203, May 2013.

[123] C. Gu, Z. Zheng, L. Xu, K. Wang, and Y. Li, "Modeling and control of a multiport power electronic transformer (pet) for electric traction applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 915–927, Feb 2016.

[124] G. Buticchi, M. Andresen, L. Costa, and M. Liserre, "Modular dc/dc converter structure with multiple power flow paths for smart transformer applications," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–9.

[125] M. B. Shadmand, R. S. Balog, and H. Abu-Rub, "Model predictive control of pv sources in a smart dc distribution system: Maximum power point tracking and droop control," *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 913–921, Dec 2014.

[126] I. Prodan and E. Zio, "A model predictive control framework for reliable microgrid energy management," *International Journal of Electrical Power & Energy Systems*, vol. 61, pp. 399–409, 2014.

[127] J. Druant, T. Vyncke, F. De Belie, P. Sergeant, and J. Melkebeek, "Adding inverter fault detection to model-based predictive control for flying-capacitor inverters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 4, pp. 2054–2063, April 2015.

[128] J. Falck, G. Buticchi, and M. Liserre, "Thermal stress based model predictive control of electric drives," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1513–1522, March 2018.

[129] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2745–2760, July 2012.

[130] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional dc dc converter based on dual-phase-shift control for dc distribution application," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1711–1727, April 2013.

[131] H. Renaudineau, A. Houari, A. Shahin, J. Martin, S. Pierfederici, F. Meibody-Tabar, and B. Gerardin, "Efficiency optimization through current sharing for paralleled dc dc boost converters with parameter estimation," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 759–767, Feb 2014.

[132] C. M. Lai, C. T. Pan, and M. C. Cheng, "High-efficiency modular high step-up interleaved boost converter for dc-microgrid applications," *IEEE Transactions on Industry Applications*, vol. 48, no. 1, pp. 161–171, Jan 2012.

[133] K. Ma and F. Blaabjerg, "Thermal optimised modulation methods of three-level neutral-point-clamped inverter for 10 mw wind turbines under low-voltage ride through," *IET Power Electronics*, vol. 5, no. 6, pp. 920–927, July 2012.

[134] K. Ma, M. Liserre, and F. Blaabjerg, "Reactive power influence on the thermal cycling of multi-mw wind power inverter," *Industry Applications, IEEE Transactions on*, vol. 49, no. 2, pp. 922–930, March 2013.

[135] G. Adinolfi, G. Graditi, P. Siano, and A. Piccolo, "Multiobjective optimal design of photovoltaic synchronous boost converters assessing efficiency, reliability, and cost savings," *IEEE Transactions on Industrial Informatics*, vol. 11, no. 5, pp. 1038–1048, Oct 2015.

[136] J. Sakly, A. Bennani Ben Abdelghani, I. Slama Belkhodja, and H. Sammoud, "Reconfigurable dc/dc converter for efficiency and reliability optimization," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1216–1224, Sep. 2017.

[137] P. Yi, T. Zhu, G. Lin, and Q. Zhang, "Routing renewable energy using electric vehicles in mobile electrical grid," in *2013 IEEE 10th International Conference on Mobile Ad-Hoc and Sensor Systems*, Oct 2013, pp. 19–27.

[138] R. Wang, J. Wu, Z. Qian, Z. Lin, and X. He, "A graph theory based energy routing algorithm in energy local area network," *IEEE Transactions on Industrial Informatics*, vol. 13, no. 6, pp. 3275–3285, 2017.

[139] H. Guo, F. Wang, L. Li, J. Zhang, and J. Luo, "A minimum loss routing algorithm based on real-time transaction in energy internet," *IEEE Transactions on Industrial Informatics*, pp. 1–1, 2019.

[140] R. Ahlswede, N. Cai, S. Y. R. Li, and R. W. Yeung, "Network information flow," *IEEE Transactions on Information Theory*, vol. 46, no. 4, pp. 1204–1216, Jul 2000.

[141] T. Elperin, I. Gertsbakh, and M. Lomonosov, "Estimation of network reliability using graph evolution models," *IEEE Transactions on Reliability*, vol. 40, no. 5, pp. 572–581, Dec 1991.

[142] F. Maloberti and A. C. Davies, *A Short History of Circuits and Systems: From Green, Mobile, Pervasive Networking to Big Data Computing*. Stylus Publishing, LLC, 2016.

[143] J. A. Bondy, U. S. R. Murty *et al.*, *Graph theory with applications*. Citeseer, 1976, vol. 290.

[144] F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, "Thermal analysis and balancing for modular multilevel converters in hvdc applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1985–1996, March 2018.

[145] C. Gu, Z. Zheng, L. Xu, K. Wang, and Y. Li, "Modeling and control of a multiport power electronic transformer (pet) for electric traction applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 915–927, Feb 2016.

[146] D. Dujic, C. Zhao, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer-low voltage prototype," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5522–5534, 2013.

[147] J. Martin, P. Ladoux, B. Chauchat, J. Casarin, and S. Nicolau, "Medium frequency transformer for railway traction: Soft switching converter with high voltage semiconductors," in *2008 International Symposium on Power Electronics, Electrical Drives, Automation and Motion*. IEEE, 2008, pp. 1180–1185.

[148] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *2007 European Conference on Power Electronics and Applications*. IEEE, 2007, pp. 1–10.

[149] A. Q. Huang, M. L. Crow, G. T. Heydt, J. P. Zheng, and S. J. Dale, "The future renewable electric energy delivery and management (freedm) system: The energy internet," *Proceedings of the IEEE*, vol. 99, no. 1, pp. 133–148, 2011.

[150] S. Bifaretti, P. Zanchetta, A. Watson, L. Tarisciotti, and J. C. Clare, "Advanced power electronic conversion and control system for universal and flexible power management," *IEEE Transactions on Smart Grid*, vol. 2, no. 2, pp. 231–243, 2011.

[151] J.-S. Lai, A. Maitra, A. Mansoor, and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 3. IEEE, 2005, pp. 1893–1899.

[152] D. Grider, M. Das, A. Agarwal, J. Palmour, S. Leslie, J. Ostop, R. Raju, M. Schutten, and A. Hefner, "10 kv/120 a sic dmosfet half h-bridge power modules for 1 mva solid state power substation," in *2011 IEEE Electric Ship Technologies Symposium*. IEEE, 2011, pp. 131–134.

[153] S. E. Networks. Lv engine. [Online]. Available: https://www.spenergynetworks.co.uk/pages/lv_engine.aspx

[154] G. De Carne, "Analysis of smart transformer features for electric distribution," Ph.D. dissertation, 2018. [Online]. Available: https://macau.uni-kiel.de/receive/diss_mods_00022905

[155] L. F. Costa, G. Buticchi, and M. Liserre, "Modular smart transformer architectures: An overview and proposal of a interphase architecture," in *2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. IEEE, 2017, pp. 1–7.

[156] C. S. Byington, M. J. Roemer, and T. Galie, "Prognostic enhancements to diagnostic systems for improved condition-based maintenance [military aircraft]," in *Proceedings, IEEE Aerospace Conference*, vol. 6, 2002, pp. 6–2815–6–2824 vol.6.

[157] M. Andresen, V. Raveendran, G. Buticchi, and M. Liserre, "Lifetime-based power routing in parallel converters for smart transformer application," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[158] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Thermally compensated discontinuous modulation strategy for cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[159] ——, "Power routing for cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9435–9446, Dec 2017.

[160] J. Su and C. Liu, "A novel phase-shedding control scheme for improved light load efficiency of multiphase interleaved dc dc converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4742–4752, Oct 2013.

[161] A. Costabeber, P. Mattavelli, and S. Saggini, "Digital time-optimal phase shedding in multiphase buck converters," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2242–2247, Sep. 2010.

[162] H. Chen, "Interleaved current sensorless control for multiphase boost-type switch-mode rectifier with phase-shedding operation," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 766–775, Feb 2014.

[163] J. Su and C. Liu, "A novel phase shedding control scheme for improved light load efficiency of multiphase interleaved dc dc converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4742–4752, Oct 2013.

[164] M. Andresen. Active thermal control of power electronic modules in smart transformer applications. [Online]. Available: https://macau.uni-kiel.de/servlets/MCRFileNodeServlet/dissertation_derivate_00007205/dissertation_ma_final.pdf

[165] M. Liserre. The highly efficient and reliable smart transformer (heart). [Online]. Available: http://www.heart.tf.uni-kiel.de/

[166] T. Zhao *et al.*, "Design and control of a cascaded h-bridge converter based solid state transformer (sst)." 2010.

[167] J. A. Barrena, L. Marroyo, M. ï. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for pwm cascaded h-bridge converter-based statcom," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 21–29, Jan 2008.

[168] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded h-bridge inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2691–2699, Aug 2010.

[169] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded h-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4399–4406, Nov 2009.

[170] T. Zhao, G. Wang, S. Bhattacharya, and A. Q. Huang, "Voltage and power balance control for a cascaded h-bridge converter-based solid-state transformer," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1523–1532, April 2013.

[171] H. Iman-Eini, J. L. Schanen, S. Farhangi, and J. Roudet, "A modular strategy for control and voltage balancing of cascaded h-bridge rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2428–2442, Sept 2008.

[172] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved vscs and pwm schemes for flux minimization," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7534–7546, 2015.

[173] R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, "A new control structure for grid-connected lcl pv inverters with zero steady-state error and selective harmonic compensation," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, vol. 1, 2004, pp. 580–586 Vol.1.

[174] S. Pugliese, M. Andresen, R. A. Mastromauro, G. Buticchi, S. Stasi, and M. Liserre, "A new voltage balancing technique for a three-stage modular smart transformer interfacing a dc multibus," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2829–2840, March 2019.

[175] S. Shirinivas, S. Vetrivel, and N. Elango, "Applications of graph theory in computer science an overview," *International journal of engineering science and technology*, vol. 2, no. 9, pp. 4610–4621, 2010.

[176] D. Mehta, A. Ravindran, B. Joshi, and S. Kamalasadan, "Graph theory based online optimal power flow control of power grid with distributed flexible ac transmission systems (d-facts) devices," in *2015 North American Power Symposium (NAPS)*, Oct 2015, pp. 1–6.

[177] R. Wang, J. Wu, Z. Qian, Z. Lin, and X. He, "A graph theory based energy routing algorithm in energy local area network," *IEEE Transactions on Industrial Informatics*, vol. 13, no. 6, pp. 3275–3285, Dec 2017.

[178] V. Raveendran, M. Andresen, M. Liserre, and G. Buticchi, "Lifetime-based power routing of smart transformer with chb and dab converters," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 3523–3529.

[179] Y. Ahn, I. Jeon, and J. Roh, "A multiphase buck converter with a rotating phase-shedding scheme for efficient light-load control," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2673–2683, Nov 2014.

[180] J. Fan, K. C. Yung, and M. Pecht, "Physics-of-failure-based prognostics and health management for high-power white light-emitting diode lighting," *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 3, pp. 407–416, Sep. 2011.

[181] J. Fan, K. Yung, and M. Pecht, "Lifetime estimation of high-power white led using degradation-data-driven method," *IEEE Transactions on Device and Materials Reliability*, vol. 12, no. 2, pp. 470–477, June 2012.

[182] P. Asimakopoulos, K. D. Papastergiou, T. Thiringer, M. Bongiorno, and G. L. Godec, "On vce method: in-situ temperature estimation and aging detection of high-current igbt modules used in magnet power supplies for particle accelerators," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2018.

[183] K. Emadi and M. Ehsani, "Aircraft power systems: technology, state of the art, and future trends," *IEEE Aerospace and Electronic Systems Magazine*, vol. 15, no. 1, pp. 28–32, Jan 2000.

[184] J. A. Rosero, J. A. Ortega, E. Aldabas, and L. Romeral, "Moving towards a more electric aircraft," *IEEE Aerospace and Electronic Systems Magazine*, vol. 22, no. 3, pp. 3–9, March 2007.

[185] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 54–64, June 2015.

[186] M. Sinnett, "787 no-bleed systems: Saving fuel and enhancing operational efficiencies," http://www.boeing.com/commercial/aeromagazine, boeing,Aero Magazine,QTR-4.07.

[187] V. Hilderman and T. Baghi, *Avionics certification: a complete guide to DO-178 (software), DO-254 (hardware)*. Avionics Communications, 2007.

[188] J. Hale, "Boeing 787 from the ground up," *Aero*, vol. 4, no. 24, p. 7, 2006.

[189] R. D. Telford, S. J. Galloway, and G. M. Burt, "Evaluating the reliability amp; availability of more-electric aircraft power systems," in *2012 47th International Universities Power Engineering Conference (UPEC)*, Sept 2012, pp. 1–6.

[190] C. EASA, "Certification specifications for large aeroplanes," 2009.

[191] J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage ac-dc converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 213–232, March 2017.

[192] G. Buticchi, L. Costa, and M. Liserre, "Improving system efficiency for the more electric aircraft: A look at dcdc converters for the avionic onboard dc microgrid," *IEEE Industrial Electronics Magazine*, vol. 11, no. 3, pp. 26–36, Sept 2017.

[193] F. Gao, S. Bozhko, G. Asher, P. Wheeler, and C. Patel, "An improved voltage compensation approach in a droop-controlled dc power system for the more electric aircraft," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7369–7383, Oct 2016.

[194] T. Schroeter and D. Schulz, "An approach for the mathematical description of aircraft electrical systems' load characteristics including electrical dependences validation," in *Electrical Systems for Aircraft, Railway and Ship Propulsion*, Oct 2010, pp. 1–6.

[195] F. Camci, "System maintenance scheduling with prognostics information using genetic algorithm," *IEEE Transactions on Reliability*, vol. 58, no. 3, pp. 539–552, Sept 2009.

[196] Z. Li, J. Guo, and R. Zhou, "Maintenance scheduling optimization based on reliability and prognostics information," in *2016 Annual Reliability and Maintainability Symposium (RAMS)*, Jan 2016, pp. 1–5.

[197] S. Bifaretti, L. Tarisciotti, A. Watson, P. Zanchetta, A. Bellini, and J. Clare, "Distributed commutations pulse-width modulation technique for high-power ac/dc multilevel converters," *IET Power Electronics*, vol. 5, no. 6, pp. 909–919, July 2012.

[198] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Power routing for cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9435–9446, Dec 2017.

[199] Y. Ko, V. Raveendran, M. Andresen, and M. Liserre, "Discontinuous modulation based power routing for modular smart transformers," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 1084–1090.

[200] A. Dell'Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, "Overview of pi-based solutions for the control of dc buses of a single-phase h-bridge multilevel active rectifier," *IEEE Transactions on Industry Applications*, vol. 44, no. 3, pp. 857–866, May 2008.

[201] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[202] Y. Ko, V. Raveendran, M. Andresen, and M. G. Liserre, "Thermally-compensated discontinuous modulation for mvac/lvdc building blocks of modular smart transformers," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[203] V. G. Monopoli, A. Marquez, J. I. Leon, Y. Ko, G. Buticchi, and M. Liserre, "Improved harmonic performance of cascaded h-bridge converters with thermal control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 4982–4991, July 2019.

[204] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a pwm converter system," *IEEE Transactions on Industry Applications*, vol. 27, no. 6, pp. 1063–1075, 1991.

[205] Qunjing Wang, Quan Chen, Weidong Jiang, and Cungang Hu, "Analysis and comparison of conduction losses in neutral-point-clamped three-level inverter with pwm control," in *2007 International Conference on Electrical Machines and Systems (ICEMS)*, Oct 2007, pp. 143–148.

[206] B. Wu and M. Narimani, *High-power converters and AC drives*. John Wiley & Sons, 2017.

[207] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[208] V. M. Iyer, S. Gulur, and S. Bhattacharya, "Optimal design methodology for dual active bridge converter under wide voltage variation," in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2017, pp. 413–420.

[209] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*. John Wiley & Sons, 2011, vol. 29.

[210] S. Pugliese, M. Andresen, R. Mastromauro, G. Buticchi, S. Stasi, and M. Liserre, "Voltage balancing of modular smart transformers based on dual active bridges," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 1–6.

Appendices

A Modeling of Selected Converter Topologies

In this section, the electrical models of the converter topologies considered for the reliability studies are presented.

1.1 Inverter Modeling

In case of three-phase inverter as shown in Fig. A.1, it is assumed that the power in each phase of the inverter are balanced. Therefore, without the loss of generality, loss calculation of a single phase or a half-bridge is performed and extended to other phases.

A sinusoidal modulation reference signal V_{ref} having the desired amplitude and frequency is compared with the triangular carrier waveform with converter switching frequency to generate Sinusoidal Pulse Width Modulation (SPWM) signals. The reference signal is given by the equation (A.1) [204];

$$V_{ref} = \frac{V_{DC,inv}}{2} M sin(\omega t + \phi) \tag{A.1}$$

where M is the modulation index, ω is the frequency and ϕ denotes the power factor angle. Under the assumption that the switching frequency is much larger than the modulation signal frequency, the average output voltage over a switching period can be considered to be constant [205]. Therefore, the effective duty cycle of the IGBT, d_{IGBT} is given by

$$d_{IGBT} = \frac{T_{on}}{T_{sw}} = \frac{1}{2}[1 + M sin(\omega t + \phi)] \tag{A.2}$$

The effective duty cycle of the diode can be calculated by considering the fact that its conduction period is complementary and is expressed as

$$d_{diode} = 1 - \frac{T_{on}}{T_{sw}} = \frac{1}{2}[1 - M sin(\omega t + \phi)] \tag{A.3}$$

By calculating the duty cycle of the IGBT and diode for each switching cycle, the device current is computed for each switching period. Once the device current is known, the conduction and switching losses are calculated as described in Section 2.5.4. However, the method of calculating the average losses may be adequate for many applications, but is misleading while studying thermal behavior or lifetime analysis. When the losses are averaged with the modulating frequency, for e.g., $50/60Hz$ in case of grid applications, the junction temperature fluctuations during this duration are also neglected. Therefore, in this thesis, for inverter modeling, the conduction losses and switching losses are calculated at every switching instant.

1.2 CHB Modeling

For the cascaded H-bridge converter, the electro-thermal model is developed considering the phase-shifted modulation technique [206]. The investigated system is based on unipolar modulation method with multiple carrier signals for each H-bridge of the CHB and the carrier signals are phase shifted by an angle of $\frac{360^\circ}{n_{CHB}}$, where n_{CHB} is the number of H-bridges in CHB converter. As the fundamentals of CHB converter has already been covered in Section 3.1, only the loss modeling is discussed here.

The multi-level CHB converter modeling is different from the inverter modeling since the power loss in each CHB cell depends not only on the power processed by that cell, but also on the total system power. The cells in CHB are connected in series, resulting in the same current to flow through each cell irrespective of the power processed by individual cells. Even when a cell processes lower power share, the resulting losses are not proportionally lower compared to the other cells, since equal current flows through the series connected CHB cells. A single H-bridge cell of the CHB converter connected to an AC grid is shown in Fig. A.2.

For equal power-sharing, the modulation index of a CHB cell, $M_{CHB,eq}$, is given as

$$M_{CHB,eq} = \frac{\sqrt{2}V_g}{n_{CHB}V_{DC,i}}, \tag{A.4}$$

where V_g is the rms AC grid voltage for a phase and $V_{DC,i}$ represents the DC-link voltage of each CHB cell.

The power share of individual CHB cells can be controlled through the modulation index of that cell [159]. Therefore, the modulation index of each CHB cell i is represented as

$$M_{CHB,i} = \frac{\hat{V_{ref,i}}}{V_{DC,i}} \; with \; 0 \leq M_{CHB,i} \leq 1, \tag{A.5}$$

where $\hat{V_{ref,i}}$ is the amplitude of the reference voltage of the cell i and $V_{DC,i}$ is the corresponding DC-link voltage.

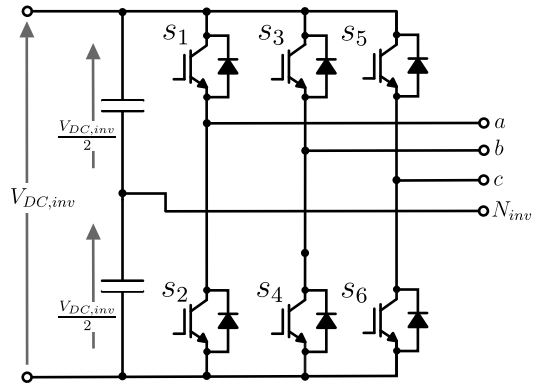


Figure A.1: Schematic of a three-phase inverter.

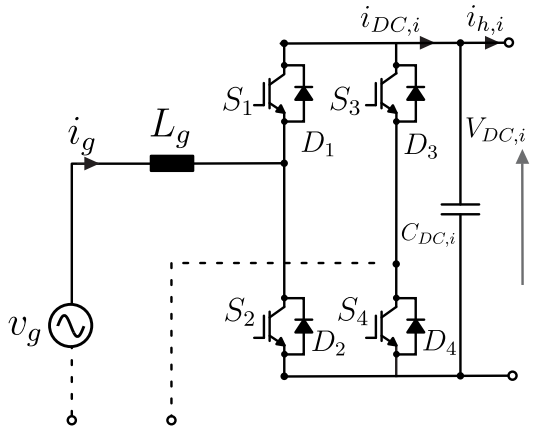


Figure A.2: Schematic of the H-bridge in a CHB converter.

In time domain, the modulating signal of a CHB cell i at an instant t, considering the fundamental frequency component of the AC voltage is expressed as

$$m_{CHB,i} = M_{CHB,i} sin(\omega t). \tag{A.6}$$

Based on the averaged model for the switching period T_{sw}, the output voltage of the CHB converter ($V_{CHB,out}$) and the current in the DC-link ($i_{DC,i}$) of cell i are given as

$$V_{CHB,out} = \sum_{i=1}^{N} m_{CHB,i} V_{DC,i}, \tag{A.7}$$

$$i_{DC,i} = m_{CHB,i} i_g. \tag{A.8}$$

In (A.8), the i_g represents the AC current or the grid current. The grid current can be represented as

$$i_g = \hat{I}_g sin(\omega t - \theta), \tag{A.9}$$

where $\hat{I}_g$ is the amplitude of grid current, and θ is the phase angle between the grid current and the CHB converter output voltage.

In short, the currents and voltages in the AC and DC side of the CHB in Fig. 4.20 are modeled using the following equations [207].

$$L_g \frac{di_L}{dt} = \sum_{i=1}^{N} (m_{CHB,i}) V_{DC,i} - (\sqrt{2} V_{AC} sin(\omega t)) \tag{A.10}$$

$$C_{DC,i} \frac{dV_{DC,i}}{dt} = i_{h,i} - i_{DC,i}. \tag{A.11}$$

When the power processed by each H-bridge is equal, the modulation indexes applied to each of them are also equal. In case of power unbalance, the modulation indexes of the H-bridges are unequal [207]. Since the H-bridges are connected in series in the CHB, the total current flowing through each H-bridge remains the same. However, depending on the

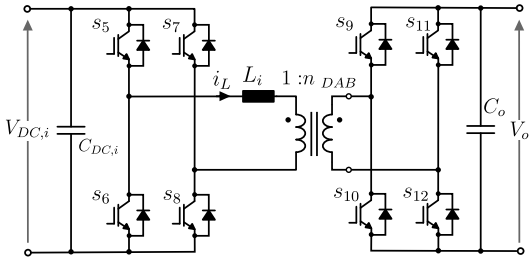


Figure A.3: Schematic of a DAB cell.

modulation index, the current sharing among the diodes and IGBTs changes. Therefore, the power unbalance in CHB changes mainly the loss distribution among diodes and IGBTs.

1.3 DAB Modeling

Since the fundamentals of DAB converter have already been introduced in Section 3.1, the focus here is mainly on the modeling of DAB converter for simulating the electrical and thermal behavior according to the given mission profile. In this thesis, the most commonly used phase shift modulation for the power flow control is considered for DAB modeling. In phase shift modulation technique, the primary and secondary bridges are operated with a phase shift ϕ over the switching period $T_{sw,DAB}$. In an ideal case, the gate signals generate square wave AC voltages with 50 % duty cycle at the primary and secondary side of the transformer as illustrated in Fig A.4. The voltage gain M_{DAB} of a DAB cell is given by

$$M_{DAB} = \frac{V_o}{V_{in} \cdot n_{DAB}}. \tag{A.12}$$

Here, n_{DAB}, V_{in} and V_o denotes the transformer turns ratio, DAB input and output voltages respectively. Schematic of a single cell of modular DAB converter is shown in Fig. A.3. In modular ST topology with CHB and DAB converters, the DC output of the CHB cell is connected as the input for the DAB cell as shown in Fig. 3.10. Hence, the input voltage V_{in} in (A.12) is taken as $V_{DC,i}$ for modeling.

Considering phase shift modulation for DAB cell i, the power processed by the DAB is given by

$$P_i = \frac{M_{DAB,i} V_{DC,i}^2 D_i (1 - D_i) T_{sw,DAB}}{2L_i}, \tag{A.13}$$

where $D_i = \frac{\phi}{\pi}$, P_i is the power processed by DAB cell i, $M_{DAB,i}$ is the voltage gain of the cell DAB_i, $V_{DC,i}$ is the input DC voltage, L_i is the leakage inductance and $T_{sw,DAB}$ is the switching time period. Since the input dc voltage, leakage inductance, switching frequency and the voltage gain are fixed values defined by the design of the DAB converter, equation (A.13) gives the phase shift of the DAB corresponding to the power requirement according to the mission profile.

Typical bridge voltages at the primary (V_{pri}) and secondary side (V_{sec}) of the high frequency transformer, and the inductor current waveform for a DAB are depicted in Fig. A.4. From

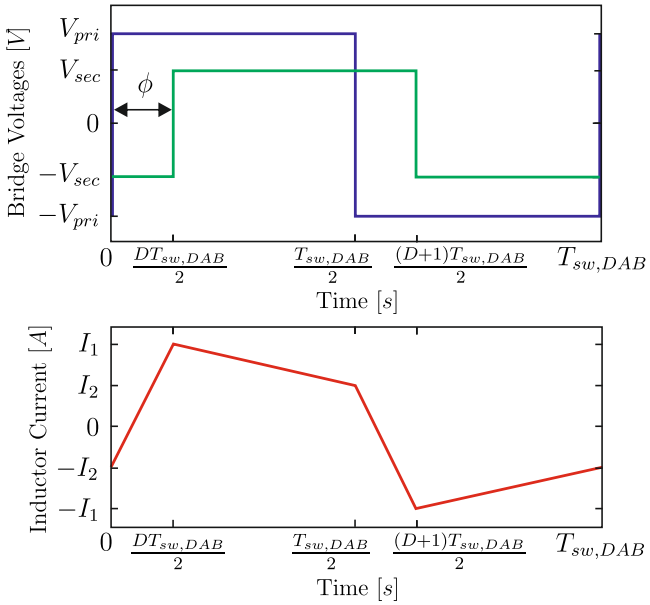


Figure A.4: Typical DAB voltage and current waveforms [208].

Table A.1: ZVS operating modes of DAB

Case	Primary Bridge	Secondary Bridge
$I_1 > 0$ and $I_2 > 0$	ZVS	ZVS
$I_1 > 0$ and $I_2 < 0$	non-ZVS	ZVS
$I_1 < 0$ and $I_2 > 0$	ZVS	non-ZVS

the phase shift, the inductor currents at the switching instants $\frac{D_i T_{sw,DAB}}{2}$ and $\frac{T_{sw,DAB}}{2}$ can be calculated using (A.14) and (A.15) respectively.

$$I_1 = [(2D-1)+M]\frac{V_{DC,i}T_{sw,DAB}}{4L_i} \tag{A.14}$$

$$I_2 = [1+M(2D-1)]\frac{V_{DC,i}T_{sw,DAB}}{4L_i} \tag{A.15}$$

The ZVS condition of the primary and secondary bridge can be inferred from the inductor currents at switching instants, I_1 and I_2, and are tabulated in Table A.1. Since the currents at the switching instants, I_1 and I_2, and the ZVS conditions are known, switching losses can be calculated following the method explained in Section 2.5.4.

From the inductor current waveform, the rms current at the primary side ($I_{rms,pri}$) and secondary side ($I_{rms,sec}$) of the transformer are calculated using

$$I_{rms,pri} = \sqrt{\frac{I_1^2 + I_2^2 + I_1 I_2(1-2D)}{3}}, \tag{A.16}$$

$$I_{rms,sec} = \frac{I_{rms,pri}}{n_{DAB}}. \tag{A.17}$$

Subsequently, the rms current in the primary and secondary side devices are obtained as

$I_{device,pri} = \frac{I_{rms,pri}}{\sqrt{2}}$ and $I_{device,sec} = \frac{I_{rms,sec}}{\sqrt{2}}$ [118]. Using the rms currents flowing through the device, the conduction losses can be calculated.

B CHB control system design

For the control system design, a cascaded control structure shown in Fig. 4.10 is considered. For the current control loop, Proportional-Resonant (PR) current controller is used and a PI controller is used for the outer voltage loop.

For the current control, the plant can be considered as the filter inductor L_g together with its own resistance R_g and is represented by the transfer function $G_f(s)$.

$$G_f(s) = \frac{1}{L_g s + R_g} \tag{B.1}$$

The delay in the system is denoted by the transfer function $G_{delay}(s)$ and is composed of the computation delay T_s and the PWM delay $0.5T_s$ where T_s is the sampling time.

$$G_{delay}(s) = \frac{1}{1.5T_s s + 1} \tag{B.2}$$

The proportional resonant controller is usually represented in Laplace domain as $G_{pr,norm}(s)$, where ω_0 is the resonant frequency of the PR controller.

$$G_{pr,mod}(s) = K_p + K_r \frac{s}{s^2 + \omega_0^2} \tag{B.3}$$

Theoretically, resonant controller as represented by $G_{pr,mod}(s)$ offers infinite gain at the resonant frequency, which may cause stability problems in the system. Therefore, a modified PR controller with a cutoff frequency ω_c is used, where ω_c is usually chosen between 5 and 15.

$$G_{pr,mod}(s) = K_p + K_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{B.4}$$

The tuning of the PR controller is similar to the tuning of a PI controller and the value of K_p is calculated using (B.5) for optimal damping [209].

$$K_p = \frac{L_g}{3T_s} \tag{B.5}$$

The resonant gain K_r acts on the bandwidth of the resonant. A low K_r leads to a very narrow bandwidth while a high K_r leads to a wider band. Thus, the Kr can be tuned according to the needs and the bandwidth must be chosen to consider the deviations and stability of the system. The open loop transfer function $G_{ol,current}$ of the current controller is obtained as

$$G_{ol,current} = G_{pr,mod}(s) G_{delay}(s) G_f(s). \tag{B.6}$$

The bode plot for the open loop current control transfer function $G_{ol,current}$ with the system parameters in Table 4.3 is shown in Fig. B.1 considering value of K_p using (B.5), and K_r as 750. From the bode diagram, it can be seen that the closed loop system is stable with a phase margin of 54.2° at $491\,Hz$.

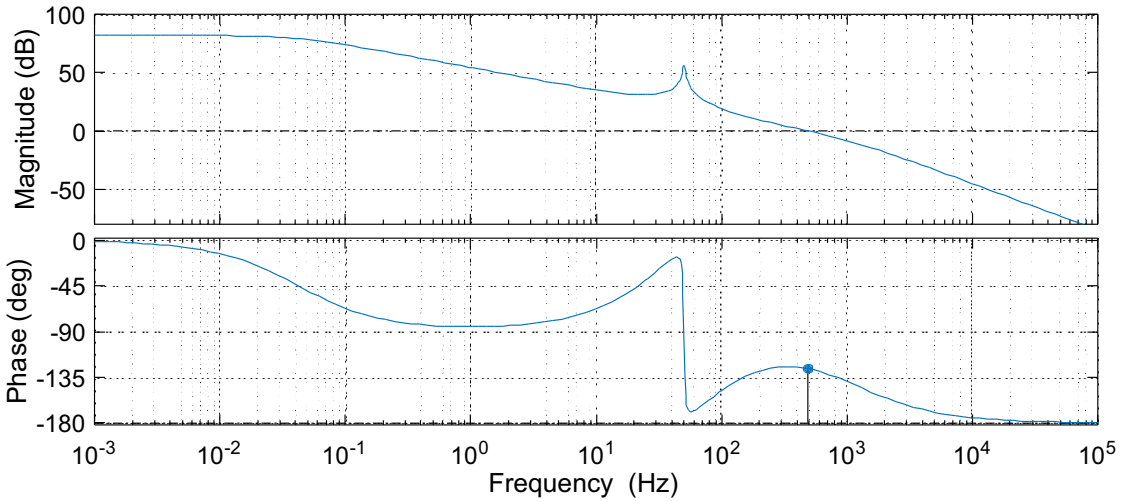


Figure B.1: Open loop bode diagram of the plant with current controller $G_{ol,current}$ with phase margin of 54.2° at 491 Hz.

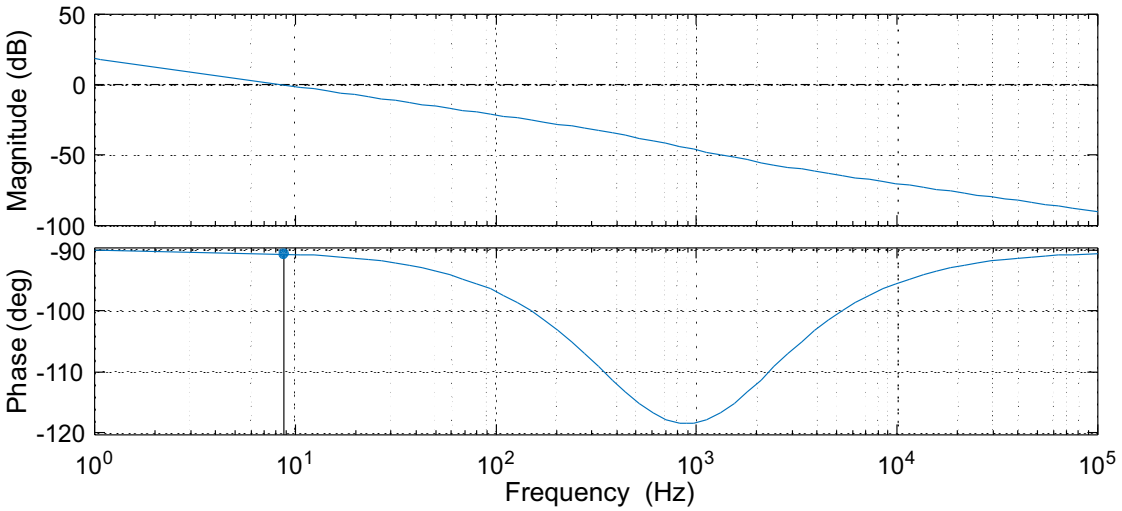


Figure B.2: Open loop bode diagram of the plant with current controller $G_{ol,voltage}$ with phase margin of 89.1° at 13 Hz.

For the design of the voltage control loop, the dynamics of the current control loop can be approximated by a first order transfer function if the current control loop is optimally damped and the bandwidth of the current controller is much bigger than that of the voltage controller [209]. The voltage control loop is responsible for keeping the total dc-link voltage equal to the reference value and a Proportional Integral (PI) controller is employed. The plant transfer function for the voltage controller comprising PI voltage controller, first-order current loop transfer function and voltage loop transfer function is given by [210]

$$G_{ol,voltage}(s) = \left(\frac{K_{p,vdc}(T_i s+1)}{T_i s}\right)\left(\frac{1}{3T_i s+1}\right)\left(\frac{N\bar{V_{dc}}(T_z s+1)}{\bar{I_g}(T_p s+1)}\right), \tag{B.7}$$

where $K_{p,vdc}$ is the proportional gain and T_i is the integral time constant of the PI controller, $\bar{V_{dc}}$, $\bar{I_g}$ and $\bar{M}$ are the dc-link voltage, grid current and modulation index respectively, of the

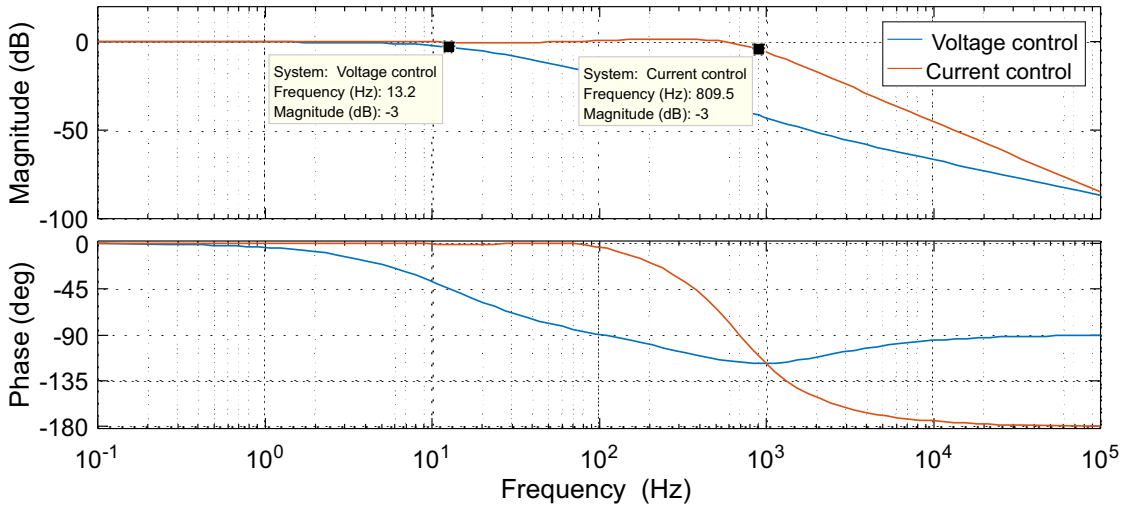


Figure B.3: Closed loop bode plots of voltage and current control loops with bandwidths $13.2\,Hz$ and $809.5\,Hz$ respectively.

selected operating point. The time constants T_z and T_p are given as

$$T_z = \frac{\bar{I}_g L_g}{N\bar{V}_{dc}\bar{M}} \quad T_p = \frac{2\bar{V}_{dc}C_{dc}}{\bar{I}_g\bar{M}}. \tag{B.8}$$

Using the pole-zero cancellation technique, the integral time constant T_i is set equal to the plant time constant T_p. The tuning of $K_{p,vdc}$ is performed according to [210] to obtain the bandwidth of the voltage controller lower than that of the current controller. For the tuning procedure, the dynamics of T_z can be neglected when the T_z value is small and the zero is located at high frequency. Considering perfect pole-zero cancellation and using the system parameters from Table 4.3, the open loop bode plot the system $G_{ol,voltage}$ is given in Fig. B.2. It can be interpreted from the bode plot that the closed loop system is stable with a phase margin of 89.1° at $13\,Hz$.

The closed loop voltage controller transfer function is given as

$$G_{cl,voltage}(s) = \frac{K_{p,vdc}\bar{M}N(T_z s+1)}{3T_s s^2 + (kT_z+1)s + k}. \tag{B.9}$$

The bode plots of the closed loop voltage and current controller are illustrated in Fig. B.3. The decoupling condition between the current and voltage control loop dynamics can be identified by comparing the bandwidths of the two systems with at least a frequency of one decade between them. Here, the bandwidth of current controller is $809.5\,Hz$, whereas the voltage loop bandwidth is $13.2\,Hz$, ensuring the decoupling of both control loops.

C Laboratory experimental setups

The setup shown in Fig. C.1 is used to implement and verify the power unbalance limits for CHB with the selected modulation methods. The setup consists of the seven-level Cascaded H-Bridge converter controlled by the micro-processor *MPC5643L* and the power analyzer *Yokogawa WT1800* to measure the loading power of each cell. The voltage and current waveforms are captured with the oscilloscope *Tektronic DPO3014* and the load used is a resistive load with maximum current carrying capacity of 29 A.

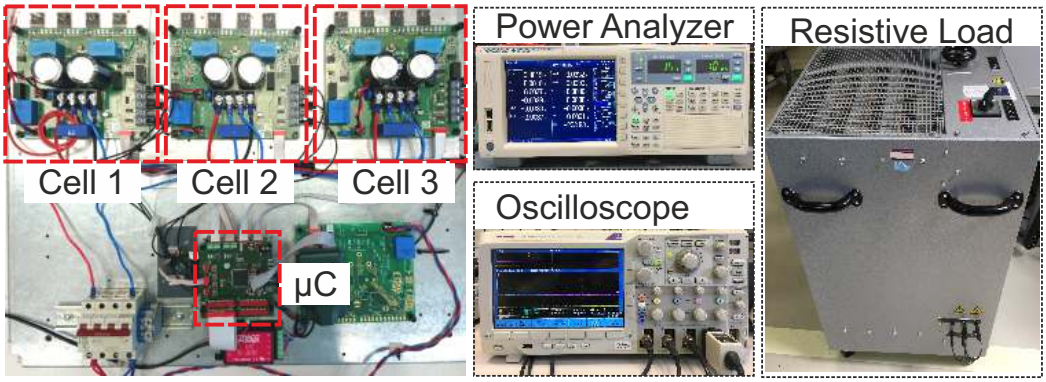


Figure C.1: Experimental setup with 7 level CHB.

A modular converter with three parallel converters with open IGBT modules sharing the same DC link and having single phase inductors at the output of each phase is illustrated in Fig. C.2. The IGBT modules, *Danfoss DP25H1200T101667-10166* are not filled with gel for direct measurement of the junction temperature. The infrared camera, *InfraTec ImageIR*

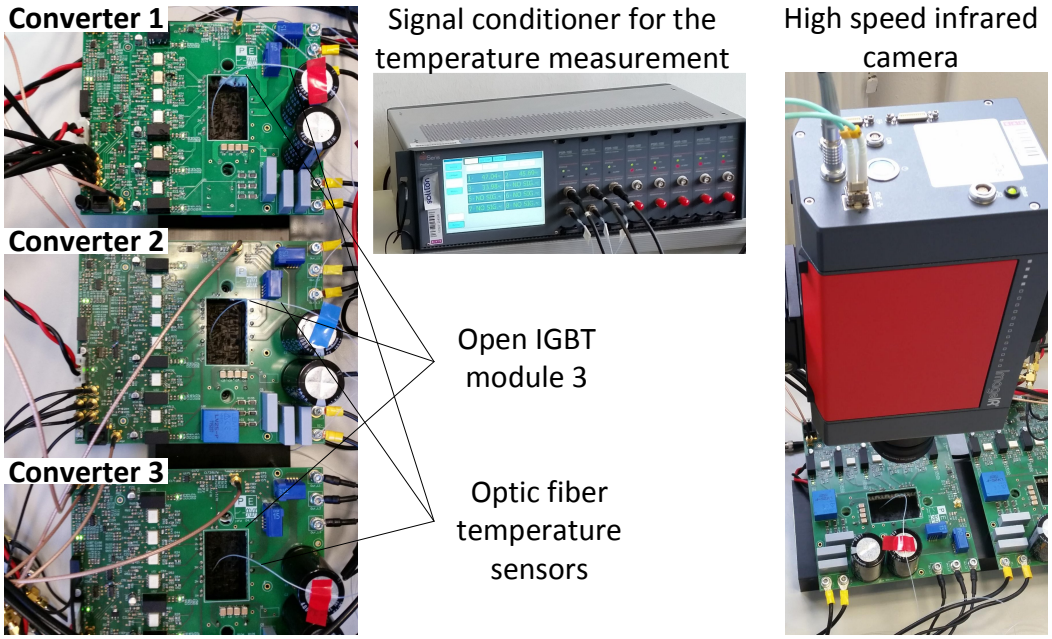


Figure C.2: Experimental setup for modular converter with 3 parallel LVDC to LVAC converters with open IGBT modules, Infrared camera and Optic fiber sensors for thermal measurements.

is used to detect the hottest spots in the power electronic module. The temperatures of the IGBTs are also measured using the fiber optic sensors *OTG-F* and signal conditioning system from *Prosens*. A three phase resistive load is fed by the modular converter cells.

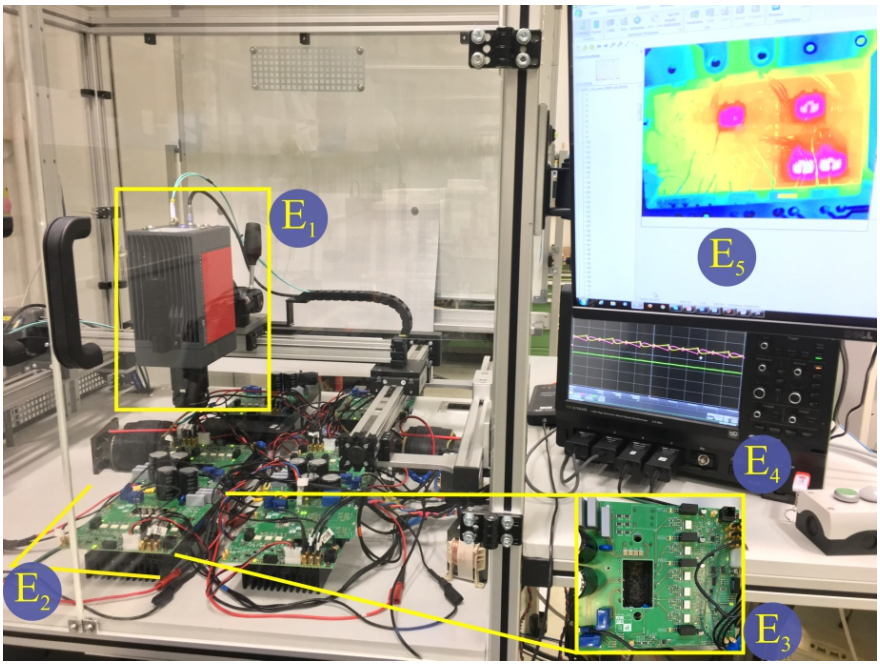


Figure C.3: The experimental setup (E_1 - High Speed Thermal Camera, E_2 - CHB and DABs, E_3 - Open Module, E_4 - Oscilloscope, E_5 - Thermal image.

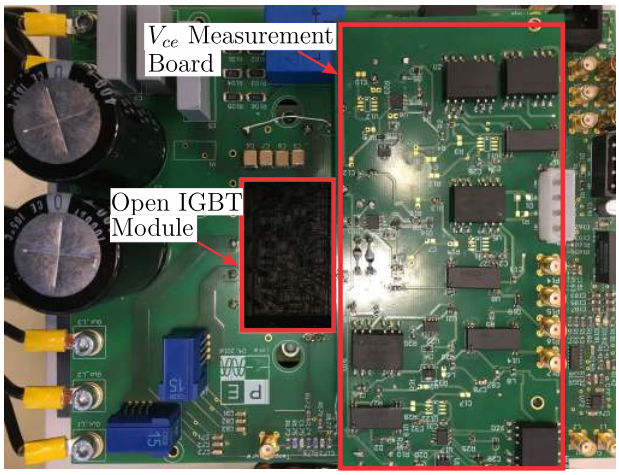


Figure C.4: Open IGBT module with V_{ce} measurement.

The multi-stage modular architecture with CHB and DAB converters with open IGBT modules is shown in Fig. C.3. The setup has open IGBT modules, thermal camera and optic fiber thermal measurement system similar to that of Fig. C.2. In addition, converter cells are also integrated with a V_{ce} sensing circuit for junction temperature estimation as shown in Fig. C.4.

The prototype of DC/DC buck converter with two-step gate driver is shown in Fig. C.5. The semiconductor device used is GS66508T; top side cooled GaN High Electron Mobility Tran-

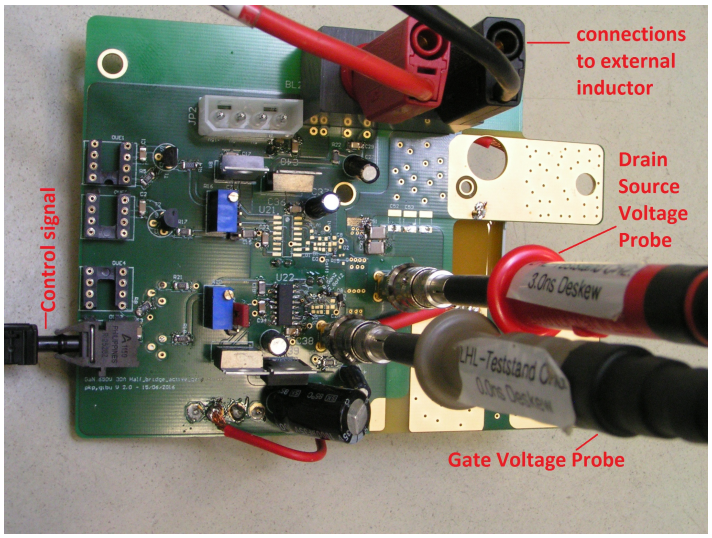


Figure C.5: Buck DC/DC converter with two-step gate driver unit and GaN HEMTs

sistor (HEMT) device from GaNSystems [70]. The case temperature measurement is carried out using a fiber optic temperature sensor which has a response time of 1s and signal conditioner *ProSens*. Control signals for the buck converter is provided from the microcontroller *MPC5643L* for active gate driving.

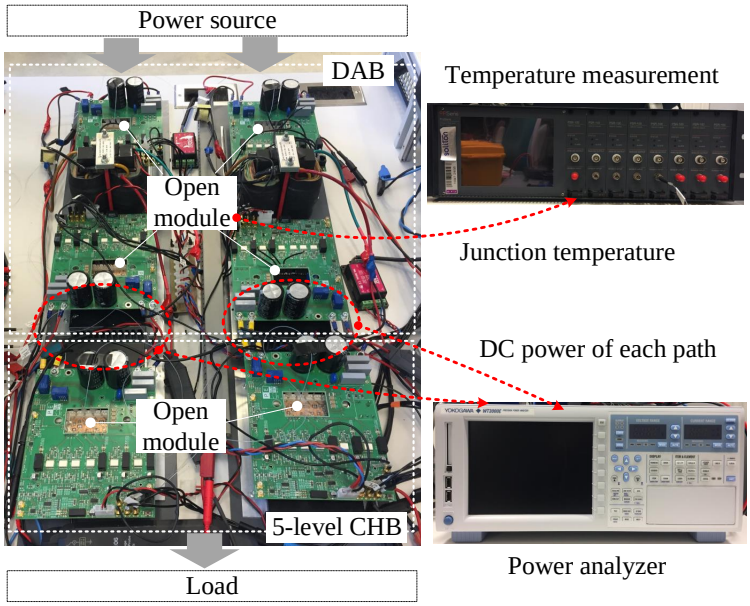


Figure C.6: Experimental setup consisting of 5-level CHB and DAB converters.

Advanced Discontinuous Pulse Width Modulation based active thermal control strategy is validated with a developed experimental setup, which consists of 5-level CHB converter and two Dual Active Bridge DC/DC converters as shown in Fig. C.6. The power of each power path is measured by a power analyzer *Yokogawa WT3000E* and the open power modules (part number: *DP25H1200T101667*) are employed, which enables to directly access to power semiconductors. The junction temperature is measured through optic fiber sensors *OTG-F* with signal conditioner *ProSens* as shown in Fig. C.6.