

Impedance Spectroscopy on Hafnium Oxide-Based Memristive Devices

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Memristive devices for neuromorphic computing have been attracting ever growing attention over the last couple of years. In neuromorphic electronics, memristive devices with multi-level resistance states are required to accurately reproduce synaptic weights. Here, a memristive device based on a multilayer oxide system (Nb/NbO_x/Al₂O₃/HfO₂/Au), which features a filamentary-free, homogenous interfacial resistive switching mechanism, is investigated. To gain a deeper insight into the switching mechanism, impedance spectroscopy (ImpSpec), X-ray photoelectron spectroscopy (XPS), and transmission electron microscopy (TEM) are exploited. While this work focuses on the analysis of impedance and current-voltage characteristics, XPS and TEM investigations can be found in a companion paper (Zahari et al.). In the course of this investigation, potentiodynamic impedance spectroscopy (PD-ImpSpec) and time resolved impedance spectroscopy (TR-ImpSpec) in combination with transient analysis are used. Evidence is presented of switching kinetics at voltages above 2.1 V directly related to changes in Schottky barrier resistance. These switching kinetics can in turn be interpreted by the charging and discharging of double positively charged oxygen vacancies $V_{O}^{+2} \approx 0.9$ eV. The results of the impedance analysis are translated into a more general model for memristive devices to map the physical processes during switching.

1. Introduction

Memristive devices have been attracting considerable interest for applications in advanced computing architectures, such as in-memory computing or neuromorphic circuits.^[1–4] A memristive device, which is based on resistive switching, typically consists of a metal-insulator-metal capacitor-like structure.^[5] A special feature of memristive devices is that they can display several resistance states which can be adjusted by suitable current or voltage signals.^[6] Although at first glance memristive devices are simple structures, the underlying elementary physical and chemical mechanisms leading to resistive switching are notoriously complicated. Furthermore, the development of highly integrated circuits is challenging as many material systems cannot be technologically integrated into the prevailing silicon technology, while the devices exhibit often high variability.

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DOI: 10.1002/aelm.202201227

To overcome these hurdles, a deep and detailed understanding of the underlying resistive switching effects is mandatory for the fabrication and integration of memristive devices in electronic systems.

Impedance spectroscopy (ImpSpec) has proven to be a powerful electrical diagnostic tool to analyze the origin of resistive switching due to its potential for probing the dynamics of trapped and mobile charges in both bulk and interfacial regions.^[7] As a result, it is possible to collect pertinent information about redox processes, defect structures, and barrier properties related to resistive switching by ImpSpec.^[8–13]

While ImpSpec can provide insight regarding carrier transport mechanisms, the interpretation of impedance data remains challenging, particularly in oxide-based memristive devices due to time-dependent resistance reduction which is often seen as positive impedance phase shifts.^[11] In these devices, the resistance change is usually attributed to the displacement of oxygen vacancies^[14,15] or charging and discharging of traps,^[16–18] and several equivalent circuits^[13] have been proposed. Interpretations for positive impedance phase shifts vary, ranging from inductance^[9] to negative RC-elements.^[19] To correctly interpret a system's ImpSpec response and identify the dominating physical mechanism, an equivalent circuit (EC) diagram that accurately represents such a device is mandatory. A thorough understanding of the physical processes behind the switching mechanisms is important as it will allow for the efficient tuning of memristive devices.

This study aims to develop a realistic EC diagram for the hafnium oxide-based memristive devices. Starting from a simplified Randles circuit,^[20] the model is extended and a complex EC diagram tailored to the memristive device is proposed. While potentiodynamic ImpSpec (PD-ImpSpec) is employed to characterize current transport dynamics for different switching states, time resolved ImpSpec (TR-ImpSpec) is used to access slower time constants that are outside the used frequency spectrum via transient analyses in the time domain. In this context, a positive phase shift, also called “inductive” behavior, is discussed.

In particular, we aim to better understand the complex physics of Nb/NbO_x/Al₂O₃/HfO₂/Au memristive devices, which show a filament-free interface-type, analog resistive switching, a high current–voltage (I – V) non-linearity, and a low power consumption, comparable to other oxide multi-layer devices.^[16,18,21,22] In particular, devices based on a similar material stack but with NbO_y instead of HfO₂ were reported in the past.^[18,21] The analog switching dynamics and the possibility to emulate the functionality of biological synapses were investigated in detail on the device level,^[22] and the integration into passive crossbar-arrays together with an experimental realization of a bio-inspired learning scheme has already been shown.^[23] Furthermore, the switching process was modeled with kinetic Monte Carlo simulations^[24] and the device-to-device and cycle-to-cycle variability was modeled with a cloud-in-a-cell (CIC) scheme.^[25] The correspondence between the memristive behavior of those oxide multi-layer devices can be concluded from the area-dependent switching (Figure 2b in Zahari et al.^[26]), the diode-like I – V characteristics, a high device resistance (even in the low resistive state (LRS)), and the analog switching process.

For homogeneous switching devices, the I – V behavior and the switching mechanism have been attributed to various causes. First, a distinction is made between the existence of one or more potential barriers and their interaction with charge carrier flow.^[14,16,27,28] Second, the diffusion of ions and the change of the charge state of electron traps are discussed as the cause of the memristive effect.^[16,17,27,29,30] In this work, clear evidence of the existence of a single potential barrier and the charging and discharging of electron traps as the origin of the memristive effect is presented for the discussed device.

Since multiple spectroscopy characterizations are required for a comprehensive memristive device analysis, as suggested by Yang et al.,^[31] the X-ray photoelectron spectroscopy (XPS) and electron energy loss spectroscopy (EELS) in the transmission electron microscopy (TEM) are results presented in detail in the companion paper Zahari et al.^[26] While only a brief summary is given here, the results of the companion paper will be discussed in more detail in comparison to the ImpSpec data in the course of this work. EELS analyses by Zahari et al.^[26] show a NbO_x oxidation state from a mixture of Nb₂O₅ and NbO₂ with decreasing oxygen content toward the bottom electrode. Using the hard X-ray photoelectron spectroscopy (HAXPES) data, a space charge region (SCR) in the HfO₂ and Al₂O₃ can be excluded. In addition, core level shifts, which are dependent on the memristive state of the device, indicate charge and discharge of electron traps as a memristive mechanism. No evidence of ionic drifts is found in the HAXPES data.

2. Material and Methods

2.1. Electrical Measurements

This work aimed to carry out transient analyses of individual impedance parameters during the switching process of the memristive devices. A homemade impedance spectrometer based on the fast Fourier transform (FFT) of time-domain data was used to obtain the complete impedance spectrum over all excitation frequencies in a very short time interval, instead of the commonly used frequency response analysis (FRA). As sketched in **Figure 1**, a multi sine perturbation signal was applied to the sample as perturbation voltage. Both the applied voltage perturbation and the current response of the sample were simultaneously recorded and subsequently transformed into the frequency domain by FFT. This allows the individual Fourier components to be determined and the impedance of the sample to be calculated.^[32] The impedance data experimentally obtained were validated by comparing the response spectrum to the perturbation spectrum.^[33,34] An adjustable bias voltage V_{bias} in the range of –5 to +5 V could additionally be applied and the respective DC was measured. The sample holder was temperature-controlled in the range from –5 to 80 °C. The FFT-impedance spectrometer was designed and built by one of the authors in our laboratory. A schematic of the experimental setup can be seen in **Figure 1**. The perturbation signal used for all measurements in the stationary voltage region had an amplitude of 55 mV, and the frequency range was from 600 mHz to 20 kHz. Agreement with linear response theory was verified after each

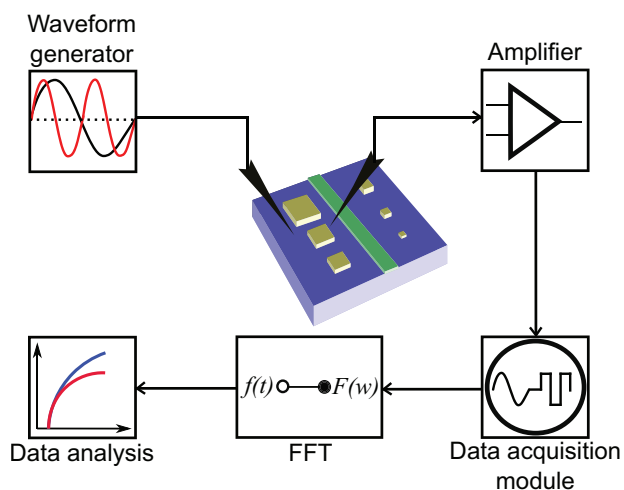


Figure 1. Principle of the ImpSpec setup which uses a preamplifier and a FFT.

measurement. For measurements at a higher voltage bias, or for TR-ImpSpec measurements, a narrower frequency band was used to improve the resolution at lower frequencies (2 Hz - 1 kHz). The design was adapted to the specific properties of particularly highly resistive memristive devices. Two essential requirements had to be taken into account: i) high amplification for the current response (up to 10^9 – 10^{12}); ii) matching the perturbation spectrum to the characteristic slow time constants of the memristive devices. More detailed information on the ImpSpec measurement setup can be found in ref. [31#32] by Popkirov and Schindler.

2.2. Memristive Device

The hafnium oxide-based memristive devices consisted of a partially oxidized (NbO_x (5 nm)) Nb back electrode assumed to be semiconducting (Figure 2a), followed by an insulating double oxide layer (Al_2O_3 (2–7 nm)/ HfO_2 layer (4.5 nm)) and a Au top electrode. Al and Nb layers were deposited by DC magnetron sputtering in an inert Ar plasma, before depositing the HfO_2 layer using an active O_2/Ar plasma. The reactive plasma leads to an oxidation of Al and partly of Nb, as shown in the companion paper (Zahari et al.)^[26] and also for similar devices.^[35] For the Al_2O_3 layer, a varying layer thickness and a roughness in the nano-scale could be observed at the interface with NbO_x (Figure 2a). An explanation of how the roughness at the interface of Al_2O_3 and NbO_x was determined can be found in Supporting Information S1. A detailed analysis of the TEM data can be found in Figure 3 in Zahari et al.^[26]

The device showed a homogeneous area-dependent switching behavior, suggesting a non-filamentary switching mechanism.^[28] Switching from the high resistive state (HRS) to the LRS could be achieved by applying a positive voltage to the top electrode with respect to the bottom electrode and inversely for switching back to HRS (Figure 2b). An illustration of the I – V characteristics of the memristive device depending on various voltage ramp speeds to switch the device are shown in Figure 2b. The corresponding I – V curves for reading the

resistive state are shown in the inset. It can be seen that the switching dynamics can be manipulated in the millisecond to second range and that the resistive state is reduced by using longer switching periods. A variance in memristive behavior among devices can be taken from Figure 2a in Zahari et al.^[26]

3. Results and Discussion

3.1. Steady-State Analysis by PD-ImpSpec

To obtain information about the electronic transport phenomena, an impedance analysis is performed in a steady-state voltage range where no resistive switching can be induced. Here, the operating point is systematically varied by adjusting V_{bias} (PD-ImpSpec). This allows insight into the voltage dependence of the particular EC elements. For the steady-state case, a single semicircle can be found in the Nyquist graph of the recorded impedance spectra with an offset on the real axis (Figure 3). This hints toward the existence of a single RC—element for the EC for the stationary voltage region. Since

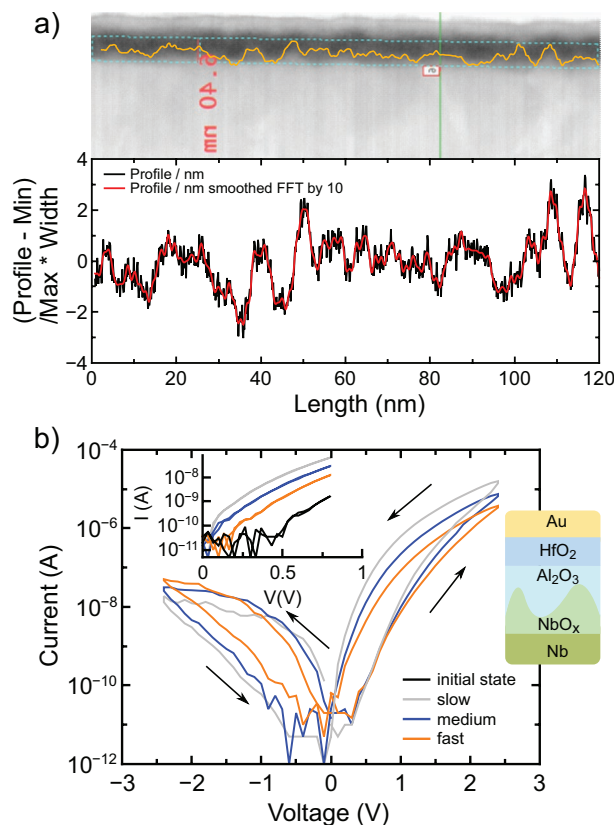


Figure 2. a) STEM image showing the cross section of the device. The roughness at the interface between Al_2O_3 and NbO_x is indicated. The roughness profile was estimated by the intensity of the cross-sectional scan. b) Characteristic I – V curves of a memristive device switching from the HRS to the LRS and back. Voltage ramps at three different speeds: grey—slow— 43.6 mV s^{-1} , blue—medium— 480 mV s^{-1} , orange—fast— 4.8 V s^{-1} . Inset: Read-out I – V characteristics of different resistance states depending on the ramp speed of the switching. A sketch of the layer stack of the memristive device is given on the right side. All measurements were performed on the same device.

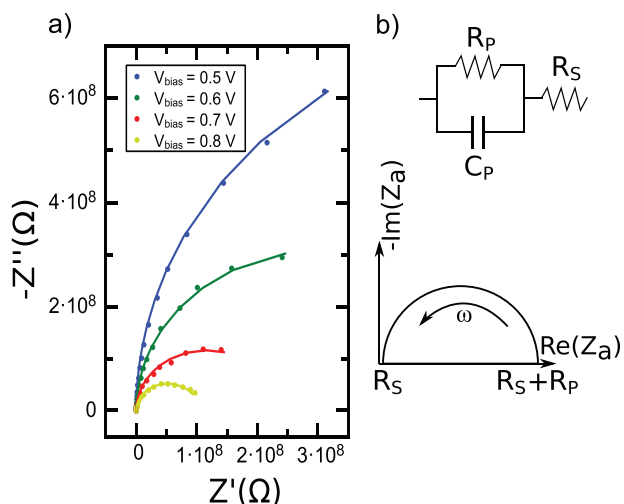


Figure 3. a) Nyquist diagram of the PD-ImpSpec of the memristive device for V_{bias} ranging from 0.5 to 0.8 V. b) Simulated Nyquist graph for the simplified Randles circuit.

the Nyquist curves do not pass through the origin, it can be assumed that the associated EC must be an arrangement of two resistors and one capacitor.

The usual EC, which is most commonly used for such an impedance spectrum, is the simplified Randles circuit^[20] and consists of a serial resistance followed up by an RC element (Figure 3b). The impedance of such a simplified Randles circuit in a Voigt configuration^[7] is described by:

$$Z = R_s + \frac{1}{\frac{1}{R_p} + j\omega C_p} \quad (1)$$

with R_s as serial ohmic component, and R_p and C_p as parallel RC element. A frequent observation in impedance analyses of solid electrolytes is a frequency dispersion, which can be represented by a constant phase element (CPE).^[36] The impedance of such a CPE is described as:

$$Z_{CPE} = \frac{1}{Q(j\omega C)^\phi} \quad (2)$$

where Q is related to the electrode capacitance ($Fs^{\phi-1} \text{ cm}^{-2}$) and ϕ is the constant phase exponent ($0 < \phi < 1$).^[37] A CPE of 1 reduces Equation (2) to the definition of an ideal capacitor. Frequency dispersions are often a result of inhomogeneity, which can originate from both material composition and layer thickness.^[37] Using a CPE instead of a capacitance to fit the presented data results in a phase exponent ϕ of nearly 1 (>0.99). A CPE was therefore not used for the following data fits. Furthermore, a linear area dependence for all fitted EC elements is found (Figure S2, Supporting Information). The simplicity of the physical EC is surprising for such a complex stack of conducting, semiconducting, and insulating layers and suggests current transport is affected by a single barrier. In addition, the accuracy of the fits presented in Figure 3 shows that the proposed EC is an appropriate choice.

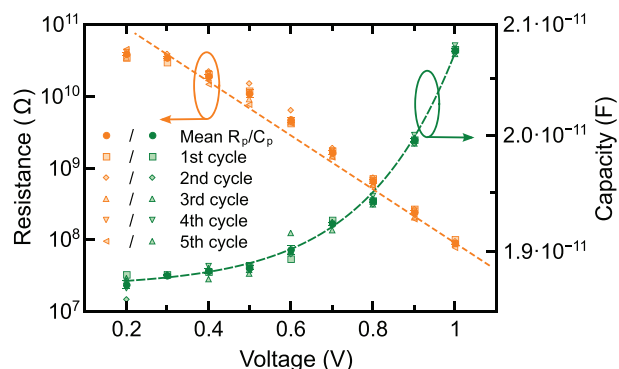


Figure 4. Parameters of the differential RC (R_p , C_p) element of the PD-ImpSpec of the memristive device versus applied V_{bias} . R_p (yellow) is displayed on a semi logarithmic scale on the left axis and C_p (green) is displayed on a linear scale on the right axis. The measurements were performed for five cycles on a single device.

To assign the discrete circuit elements of the EC to physical mechanisms within the memristive device that determine the current transport, it is necessary to take a closer look at functional relations between the elements and the varying parameters. For this purpose, the $R - V$ and $C - V$ curves of the single EC elements provide insight into the nature of the EC elements. In Figure 4, such an analysis is presented for each Randles circuit element in Voigt configuration. The PD-ImpSpec is performed in a bias voltage range from 200 to 1000 mV. Since no voltage dependence can be found for the serial resistance R_s , it can be described as a strictly real non-differential resistor. In addition, a serial resistance of $R_s \approx 12 \text{ k}\Omega$ is determined, about two orders of magnitude larger than the expected lead resistances for the electrode and contact materials. This phenomenon hints at bulk resistances and will be discussed in more detail in a later part of this study. Moreover, a clear voltage dependence can be seen for the serial RC elements R_p and C_p , as depicted in Figure 4. Here, a diode-like characteristic is obtained for the parallel differential resistor R_p . This exponential voltage dependence can be described by the thermionic emission model of a Schottky barrier:^[38,39]

$$I_D = I_S (e^{\frac{qV_D}{nk_B T}} - 1) \quad (3)$$

where k_B is the Boltzmann factor and T is the temperature. The elementary charge q is the reverse current I_S described below, and V_D is the voltage drop across the diode. As most real Schottky diodes show deviations from the ideal thermionic emission, a dimensionless correction factor n is inserted. By fitting the slope of the logarithmic current through the parallel resistor R_p , the ideality factor can be determined according to:

$$n = \frac{q}{k_B T} \frac{dV}{d(\ln I)} \quad (4)$$

The fits of the PD-ImpSpec analysis presented in Figure 4 show a remarkably small deviation from the data, attesting to the accuracy of the mathematical model employed in this study. For the parallel resistor R_p , an ideality factor of 3.71 is

determined, which gives insight into the voltage drop across the depletion region of the diode.

Various explanations for the ideality factor can be found in the literature. One possibility is the partitioning of the current transport into different paths, for example, a superposition of thermionic emission and thermionic-field emission where n describes the partitioning ratio between the different paths.^[40] Assuming a single current transport mechanism associated with a SCR, n can be used to describe the position of the mean generation of charge carriers within the SCR. For $n = 2$, the average generation of charge carriers in the center of the SCR is derived.^[41] Lateral fluctuations in barrier height and inhomogeneities in the depletion layer are possible causes for ideality factors much larger than unity.^[42–46] An alternative cause of an ideality factor greater than 1 may be a superposition of recombination currents via thermionic emission, or the presence of an interfacial layer together with surface states.^[47,48]

The reverse current I_s mentioned in Equation (3) is given by

$$I_s = A^* AT^2 e^{-\frac{\phi_{B,eff} q}{k_B T}} \quad (5)$$

where $\phi_{B,eff}$ is the effective barrier height, A the contact area, and A^* is the Richardson constant (usually approximated with $1.20173 \times 10^6 \text{ Am}^{-2}\text{K}^{-2}$ ^[49]). The occurrence of excess currents indicated by the high ideality factor, whether due to inhomogeneities or superposition of other charge transport processes, impedes accurate barrier height determination. For this reason, the barrier height determined here is referred to as the effective barrier height. Van Otterloo and Gerritsen suggest that the total barrier height $\phi_{B,r}$ can be defined as the product of n and $\phi_{B,eff}$.^[50]

The equation for calculating the effective barrier height can be derived from the reverse current definition in Equation (5):

$$\phi_{B,eff} = -\frac{k_B T}{q} \ln \left(\frac{A^* AT^2}{I_s} \right) \quad (6)$$

For the PD-ImpSpec shown in Figure 4, we find an effective barrier height of 0.84 eV for the HRS of the device. An evaluation of impedance data is more suitable for determining a barrier height than quasi-static $I - V$ curves, since series resistances and other artifacts do not have to be taken into account.

The analysis of the R_p for the steady-state case together with the rectifying behavior of the static $I - V$ curve (Figure 2b) shows a clear indication of the presence of a SCR in the memristive device, which affects the charge carrier flow in the measured voltage range. Operation of the diode in the forward direction when a positive voltage is applied to the top electrode, together with the high gold work function, suggests the formation of an SCR with an n -type semiconductor.

For the $C - V$ analysis of the memristive device, we find that the capacitance increases with V_{bias} , indicating a reduction in the SCR width due to the applied field. However, no typical asymptotic dependence of the measured capacitance is found in the voltage range investigated here which suggests that not all potential charges have been accumulated in the capacitance at this point. Instead, an exponential relationship extended by

a dimensionless divisor between voltage and measured capacitance is found, described as:

$$C_p(V) = C_j(0) + C_i^{mc} \frac{V}{V_0} \quad (7)$$

with an offset $C_j(0) = 1.92 \cdot 10^{-11}$ F, the initial capacitance $C_i = 2.66 \cdot 10^{-14}$ F, and the dimensionless parameter $m_{HRS} = 0.247$ and $m_{LRS} = 0.221$. This observation together with the voltage independence of C_p for negative voltage range implies a superposition of the SCR capacitance with another geometric capacitance. The latter is shown by the added offset, which is additionally influenced by the double oxide layer and arranged parallel to the SCR capacitance. The voltage dependence of the capacitance of an SCR can be expressed by the solution of Poisson's equation for a defined distribution of space charges:

$$-\frac{d^2 \varphi(x)}{dx^2} = \frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon_0 \epsilon_s} = \frac{qN(x)}{\epsilon_0 \epsilon_s} \quad (8)$$

Here, φ describes the electrostatic potential, E the electric field, ρ the total electric spatial charge density, $N(x)$ the doping concentration, x the position relative to the SCR transition, and ϵ_0 and ϵ_s the permittivity of the vacuum and the relative static permittivity, respectively. A derivation of the solution for an arbitrary doping profile yields:^[51]

$$C_s(V) = \frac{C_j(0)}{(1 - V / v_{bi})^p} \quad (9)$$

where v_{bi} is the built-in potential and p is the grading coefficient of the doping profile. Finally $N(x)$ is given by:

$$N(x) = N_D \left(\frac{x}{d} \right)^{\frac{1}{p-2}} \quad (10)$$

with N_D as donor doping concentration and d as length scale for donors.^[52]

Therefore, in the conventional representation of the SCR capacitance, a plot of the reciprocal of C_p versus applied voltage is used. However, this ideal model assumes a charge distribution in the SCR as described in Equation (10), which is often disturbed by the presence of serial resistors or oxide interlayers between the semiconductor and the metal, which lead to charge reversal phenomena at the interfaces due to surface states.^[53,54] In addition, the high roughness at the interface with Al_2O_3 (Figure 2a) leads to a superposition of both geometric and space charge capacitances. Due to these factors, capacitance–voltage plots often deviate from the given expectation.

A visualization of the arrangement of the capacitors and the other EC elements, which summarizes the findings of this work and the companion paper Zahari et al.^[26] can be seen in Figure 12. This geometric capacitance is largely determined by the Al_2O_3 layer due to its geometry ($d = 2\text{--}7$ nm) and permittivity (≈ 9.1) and can be estimated to be $C_{\text{Al}_2\text{O}_3} \approx 1.26 \times 10^{-11}$ F. A higher capacitance is obtained for the HfO_2 layer ($C_{\text{HfO}_2} \approx 4 \times 10^{-11}$ F, with $\epsilon_{\text{HfO}_2} = 25$ and

$d_{\text{HfO}_2} = 4.5 \text{ nm}$), suggesting that the capacitance of the Al_2O_3 layer in a series interconnection is dominant. An increased capacitance value compared to the estimated one as well as the parallel arrangement of the capacities can be explained by the roughness at the $\text{NbO}_x/\text{Al}_2\text{O}_3$ interface. Together with the roughness seen in TEM analyses (Figure 2a) and by using spatial averaging,^[55] an excess capacitance of $C_{\text{geo}} \approx 1.6 \times C_{\text{smooth}}$ can be computed. The roughness determined from the cross-sectional TEM analysis may differ from the actual roughness, due to the thickness of the lamella (approximately 30–60 nm). While the capacitances comprised in $C_j(0)$ cannot be accurately deconvoluted, it can be assumed that the largest fraction is given by the Al_2O_3 layer and smaller fractions are due to HfO_2 , the SCR in NbO_x , and possible surface states.

The lack of insight regarding time constants associated with the double oxide layer in this analysis may be due to the spectrum of the signal being limited to 20 kHz. Therefore, it is not possible to resolve smaller time constants (with $R_{\text{ox}} < 10^5 \Omega$, $C_{\text{ox}} \approx 10^{-11} \text{ F} \rightarrow \tau_{\text{ox}} < 100 \text{ ns}$) that would possibly describe the RC elements of the double oxide layer. Since the current flow is dominated by only one barrier, which has already been defined as the Schottky barrier inside the NbO_x , there must be a sufficiently small resistance in the following double oxide layer to limit the current to high field strengths only. From the TEM results (Figure 2a) and the previously mentioned high serial ohmic ratio, we can assume that there is a high spatial density of current paths (shunt resistors) in the oxide double layer (Figure 12).

To further understand the dependence of circuit parameters on the memristive switching mechanisms of the device, steady-state PD-ImpSpec is performed for the HRS and LRS of the device. For this purpose, a positive voltage ramp ($V_{\text{max}} = 3.2 \text{ V}$) is applied to set the device from HRS to LRS between the PD-ImpSpec measurements. For both states, the same symmetry in the Nyquist graphs of the impedance could be observed, revealing that the EC describing the measured data is not affected by changing the state. Thus, the charge carrier transport appears to quantitatively vary due to the change in state but continues to be described qualitatively by the same physical process, which is further confirmed by the accuracy of the fits seen in Figure 5. Both R_p and C_p are significantly affected by switching from HRS to LRS. In particular, a change in R_p of up to two orders of magnitude can be observed for low voltage ranges. Thus, we can conclude that the diode interface is sensitive to the memristive state of the device. The parameters for the HRS and LRS states determined using Equations (4), (6), and (7) and their percentage change between the states are given in Table 1.

For the resistive part of the diode interface, represented by the differential R_p , there is a significant reduction in the effective barrier height of around 17%, and the accompanying increase in n of about 13% which suggests a low variation in total barrier height compared to the effective barrier height. The aforementioned changes lead to the drop in total resistance shown in Figure 5b) on a semi-logarithmic scale for R_p . The increase in total capacity obtained when switching from HRS to LRS, together with the reduction in effective barrier height, can be explained by a reduction in the SCR width. According to the simulations on metal-insulator-semiconductor diodes by Green

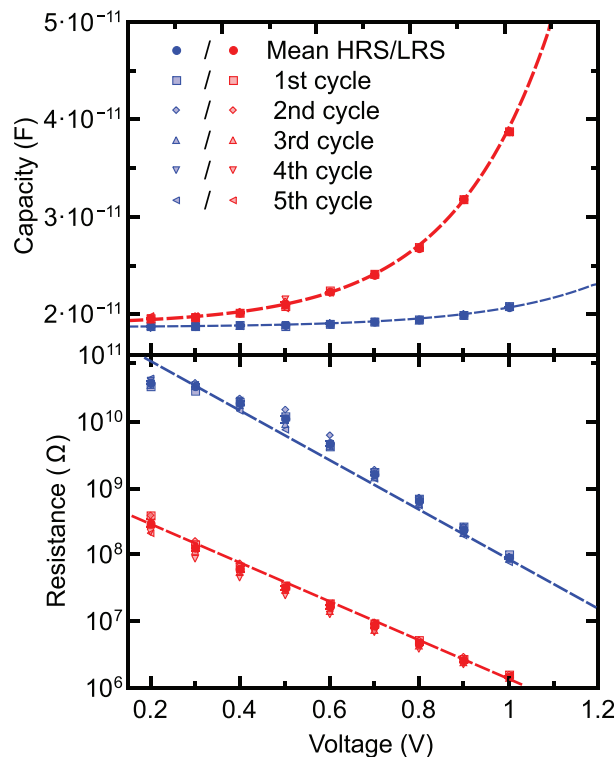


Figure 5. HRS (blue) versus LRS (red) analysis of fitted circuit parameters C_p (a) and R_p (b). C_p is shown on a linear scale in the upper graph and R_p is displayed on a semi logarithmic scale in the lower graph. The measurements were performed for five cycles on a single device.

and Shewchun, the change in the slope of the $C - V$ curves after switching indicates an increase in the amount of surface states at the insulator–semiconductor interface.^[53] The $C - V$ data are again fitted with Equation (7) and the voltage pre-factor m is determined and shown to vary proportionally to the reciprocal of the ideality factor n (Table 1). Since the inhomogeneous voltage drop across the SCR of a diode is defined via the ideality factor, which is often caused by parallel charge carrier transport mechanisms, it is necessary to introduce this parameter when analyzing the diode capacitance.

3.2. Temperature Variation

In addition to the electric field dependence, a temperature change influences most charge carrier transport phenomena. The temperature dependencies of the state-sensitive diode are determined by heating the memristive device while performing

Table 1. Calculated values of $\phi_{\text{B,eff}}$, n , m for HRS and LRS, and percentage variation between both states.

State	$\phi_{\text{B,eff}}$ (eV)	n	m
HRS	0.866 ± 0.013	3.98 ± 0.18	0.247
LRS	0.716 ± 0.007	4.49 ± 0.16	0.221
Change(%)	17.3	12.8	11.7

PD-ImpSpec. Since this device suffers dielectric breakdown under applied bias even for moderate heating, a small temperature range up to 50 °C is chosen.

For this purpose, a temperature variation from 20 up to 50 °C was performed five times in steps of 5 °C and under different voltages V_{bias} . The plot of the logarithmic current flow versus different voltages through the EC element R_p at different temperatures is shown in **Figure 6a**. Fitting the curves with a linear function gives information about the ideality factor and

the reverse bias current of the Schottky-like diode, while the effective barrier height is determined for each temperature using Equation (6).

Figure 6a shows a current increase with temperature, consistent with charge carrier transport by thermionic emission. The parameters determined from these curves show a decrease in the effective barrier height and an increase in the ideality factor with increasing temperature, in accordance with literature.^[56,57] The decrease in effective barrier height with

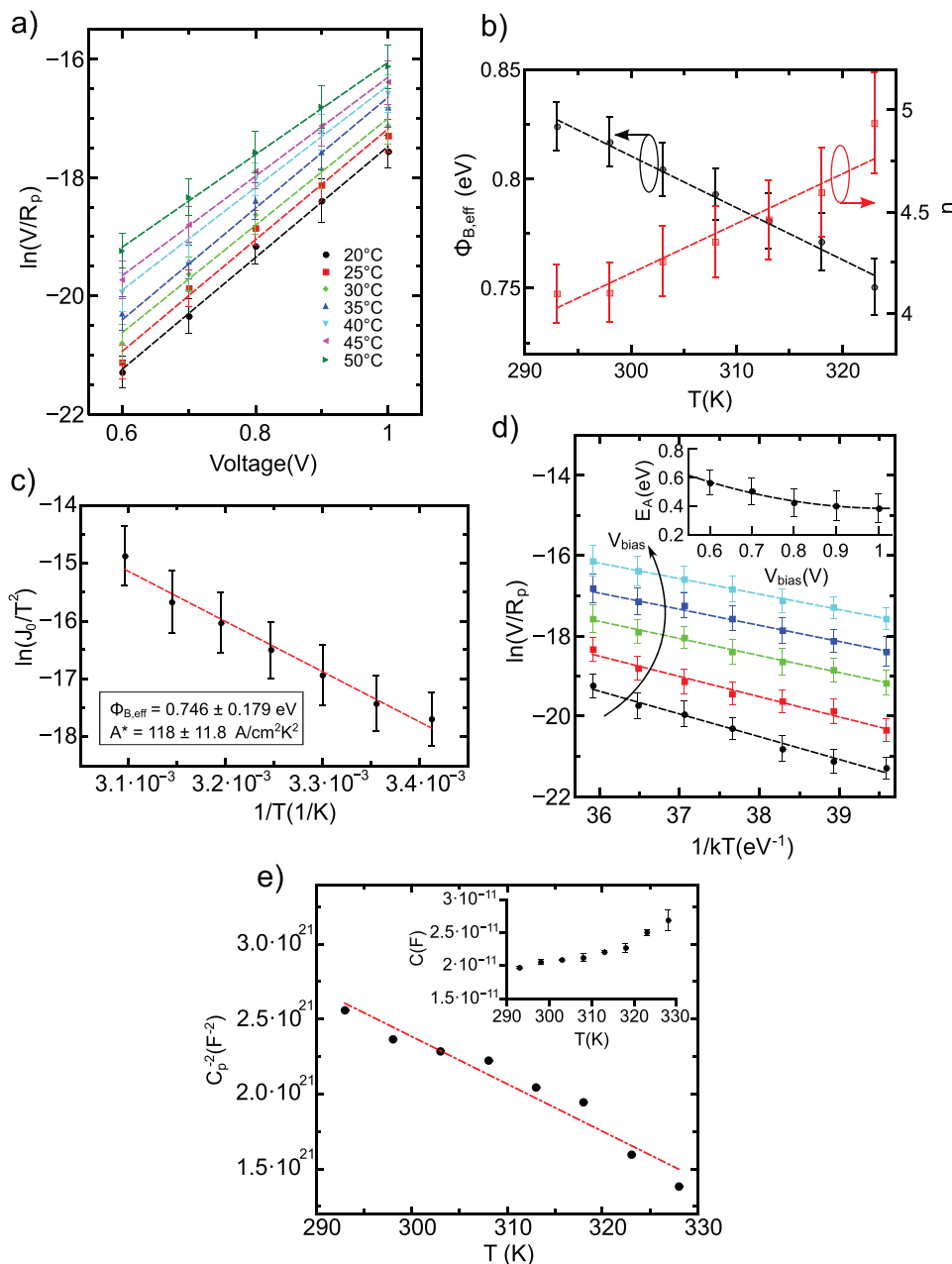


Figure 6. a) Linear plot of the natural logarithm of the current flow through R_p versus the applied voltage V_{bias} at different sample temperatures for the HRS. The temperature measurements were performed five times for one device. b) Barrier height $\Phi_{B,eff}$ and ideality factor n of the diode interface extracted from fitted $I - V$ characteristics in Figure 6a versus temperature. c) Richardson plot of the reverse current of V/R_p . d) Current-temperature characteristics of a memristive device at applied voltages V_{bias} between 0.6 and 1 V plotted linearly as the natural logarithm of the current flow through R_p . Inset: Activation energy as a function of V_{bias} . e) Modified Mott plot of C_p^{-2} versus temperature. Inset: Differential parallel capacity as a function of temperature.

increasing temperature can be explained by a change in the band gap E_g .^[58] According to Werner and Güttler,^[59] after linearizing the temperature dependence of E_g , a linear behavior of the Schottky barrier height is obtained:

$$\phi_B(T) = \phi_B(T = 293) + T\alpha_\phi \quad (11)$$

Together with Tersoff's theoretical prediction of the Schottky barrier height,^[60] a reduction of barrier height with increasing temperature with a temperature coefficient

$$\alpha_\phi(T) = \frac{d\phi_B}{dT} = \frac{dE_g}{2dT} \quad (12)$$

follows. From the linear fit of the effective barrier height as a function of temperature (Figure 6b), the temperature coefficient can be determined using Equations (11) and (6): $\alpha_\phi = 2.38 \pm 0.46 \times 10^{-3} \text{ eV K}^{-1}$ for the reduction of the barrier height ($d\phi_B/dT$) and effective barrier height at room temperature $\phi_B(T = 293) = 0.82 \text{ eV}$.^[61]

TEM images show local inhomogeneity in the barrier (Figure 2a) that most likely causes spatial potential fluctuations and thus leads to an effective barrier increase with temperature.^[42] Yet, this effect seems to be dominated by band narrowing (Varshni shift^[62]), which can be explained by two causes. First, semiconductors show a higher band-narrowing coefficient at temperatures above room temperature, along with a decrease in local inhomogeneities. Second, the presented studies show an unusually high band-narrowing coefficient, which is considerably larger than observed by Sakai et al.^[63]

Since transport mechanisms such as field emission and trap-assisted tunneling strongly depend on the effective barrier height, they become dominating charge transport mechanisms, as illustrated by the increase of the ideality factor with decreasing effective barrier height. Furthermore, at low temperatures, the ideality factor would be expected to approach unity, since superimposed charge carrier transport processes would cancel out.

An effective barrier height of 0.746 eV, determined from the Richardson plot (Figure 6c), is in agreement with the effective barrier height calculated from the $I - V$ data. The estimated Richardson constant of $A^* = 1.18 \times 10^6 \text{ Am}^{-2} \text{ K}^{-2}$ ^[46,64] is in good agreement with the usually used value $1.20173 \times 10^6 \text{ Am}^{-2} \text{ K}^{-2}$.^[49] Small deviations from the commonly used value of $1.20173 \times 10^6 \text{ Am}^{-2} \text{ K}^{-2}$ should not affect the calculations, since the barrier height is not particularly sensitive to a deviation in the Richardson constant (Equation (6)), a 100% increase of A^* at room temperature will only cause an increase of 0.018 eV in ϕ_B .^[49] A correction of the previously calculated barrier heights with the newly determined Richardson constant would therefore barely impact the result.

As shown in Figure 6d, the current follows an Arrhenius-type^[65] temperature dependence at all voltages according to

$$\frac{V}{R_p} = A \times e^{-\frac{E_A}{k_B T}} \quad (13)$$

where A is the pre-exponential factor and E_A is the activation energy. The temperature data can be fitted using a single linear

function, indicating only one activation energy for the entire temperature range investigated here. This indicates the presence of a single potential barrier.

From the inset in Figure 6d, it can be seen that the activation energy decreases with increasing applied voltage which may be due to the lowering of the potential barrier. The zero-field activation energy $E_A(E = 0) \approx 1.21 \text{ eV}$ can be calculated from Figure 6d.^[66,67] Since the investigations are in a stationary voltage and temperature range, the determined activation energies can be understood as the barrier height of a single potential barrier.

As the temperature increases, the band gap decreases along with the built-in potential. The reduction of the built-in potential affects the width of the SCR and thus causes an increase in capacitance with increasing temperature (Figure 6e, inset). Alternatively, the capacitance increase can be attributed to a change in the charge states of electron traps in HfO_2 following an SCR narrowing. This change would have a great influence on the SCR width due to the lack of charges. This last hypothesis is the most probable since indications of surface states can already be found in the voltage-dependent capacitance characteristics.

3.3. Verification of ImpSpec Parameters

Since a derivation of the results from an AC to DC configuration is valid for the EC elements of the serial resistor and the diode, a first model can be created from the previous analysis. Since the previously shown $I - V$ curve (Figure 2b) already shows a diode reach-through due to the high reverse current, the diode model with serial resistance is extended by the dimensionless transfer coefficient α .^[41] This transfer coefficient is then fitted by the quasi-static $I - V$ curve. The resulting current of this model is described as:

$$I = I_s \times \left(e^{\frac{\alpha(V - (R_s I)q)}{nk_B T}} - e^{-\frac{(1-\alpha)(V - (R_s I)q)}{nk_B T}} \right) \quad (14)$$

The reverse current I_s is defined in Equation (5). For the fit of the static $I - V$ curve, the parameter α is varied in the range $0 < \alpha < 1$, while R_s and n are set to 12 k Ω and 3.71, respectively, as previously determined from the ImpSpec-analysis. From the static $I - V$ curve, we focus on the data recorded in the LRS (Figure 7) as they allow for a wider range of positive voltage values to be used for fitting without considering the memristive set behavior, which is not implemented in this model. From the fit, shown in Figure 7, a reach-through parameter of 0.77 can be determined. A fit of the data presented in Figure 7, taking into account an additional current transport by thermionic-field emission in addition to the assumed transport by thermionic emission, according to Rideout,^[40] showed no agreement. Thus, we can conclude that the fitted ideality factor refers to a generation of charge carriers within an SCR and not to the division of the current between thermionic emission and thermionic-field emission.

An adequate description of the charge carrier transport for stationary states of the device is obtained by fitting with the function described in Equation (14), thus confirming that the current is dominated by a diode interface for the DC case. In

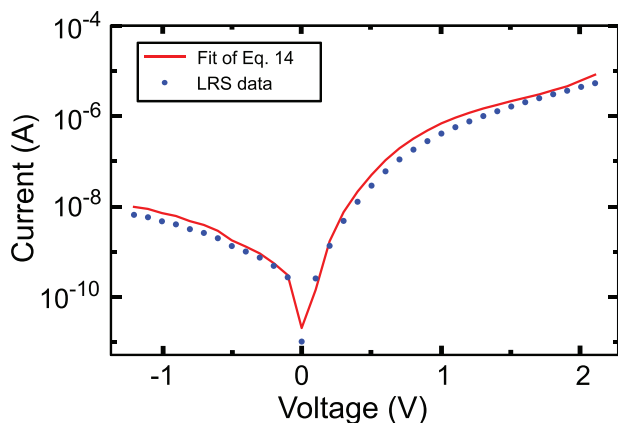


Figure 7. Fit of the quasi-static $I - V$ curve of the LRS of a memristive device with Equation (14) and extracted ImpSpec parameters in a semi-logarithmic plot.

addition, we are able to determine a reach-through parameter that, together with the ideality factor, provides information about the imperfection of this diode.

To further characterize the memristive device, a deeper understanding of the switching mechanism is required, as discussed in the following section.

3.4. Non-Stationary Analysis

Applying a voltage above 1 V can cause a resistance change in the memristive device. A distinction is made between a short and long-term resistance change. Hansen et al.^[28] attribute a short-term change in the state of a similar device to charging and discharging of interfacial trap states, while long-term retention is associated with ionic motion.

To gain insight into the mechanisms involved in the non-stationary region, two different DC voltages (1.2 and 2.1 V) are applied to the device in the HRS while ImpSpec is carried out at 1 s intervals. Such a TR-ImpSpec has two main advantages. First, slow time constants that would otherwise be outside the detection range can be resolved since slow kinetic processes are not able to follow the frequencies. Second, saturation processes can be tracked. This methodology allows a combined investigation in the frequency and time domain within a single measurement.

The impedance spectra presented in **Figure 8** indicate a change in the differential resistance R_p for a low setting voltage (1.2 V) measured after applying the voltage bias 1 and 30 s. The complex plane plot of higher setting voltage (2.1 V) shows a second semicircle with a positive imaginary part, which is often misleadingly referred to in the literature as an “inductive” feature and therefore called “inductive loop.”^[68] Splitting the impedance characteristics into quadrants shows that the additionally occurring time constant τ_{mem} must be considerably smaller than that of the already observed Schottky-like interface. From the part of the impedance with a positive phase shift, a transition to a smaller total resistance can be obtained, starting with a time constant of $\tau_{mem} = 10^{-2}$ s going down to 10^{-4} s after roughly one second at 2.1 V.

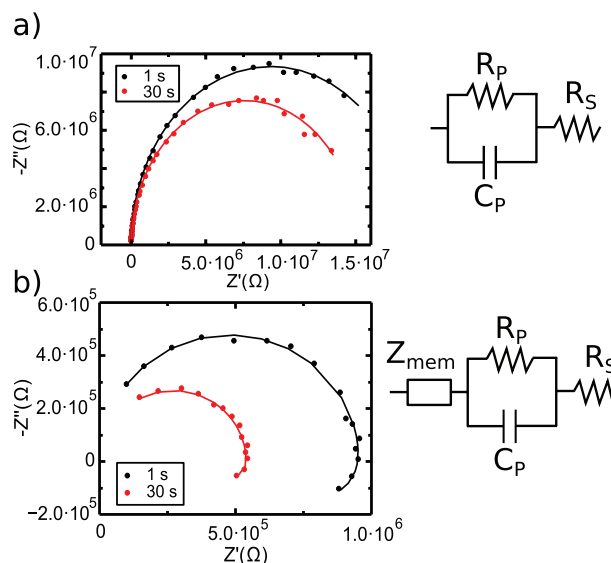


Figure 8. Nyquist TR-ImpSpec graphs showing an “inductive” loop after applying a) 1.2 V for 1 and 30 s, and b) 2.1 V for 1 and 30 s.

Such impedance behavior is often found in memristive device analyses, regardless of whether they display binary or analog switching,^[8–10] and is most commonly attributed to memristive switching. The “inductive” loop decreases when the memristive devices change from the HRS to LRS. Such behavior can be seen in the TR-ImpSpec of the examined memristive device. Usually, the additional semicircle in memristive devices is explained as an inductivity^[68] or mem-inductivity.^[9] However, inductance in such memristive thin-film systems is inconceivable, simply because of the geometric conditions. Implementing windings of an inductance of corresponding size (>10 mH), in a multi-layer system of about 10 nm thickness, is physically impossible.

A much more appropriate assumption was made by Taibl et al.^[19] who studied epitaxial SrTiO₃ thin films (100–413 nm) at temperatures between 325 and 700 °C employing ImpSpec. In this work, an “inductive” loop is found which affects the overall resistance of the thin film and shows a dependency on the applied DC-bias. Taibl et al. discuss an additional impedance feature showing as a semicircle in the complex plane plot as a frequency-dependent transport process of charged carriers that is responsible for a varying resistance Z_{mem} , which can either be positive or negative depending on the resistance change direction.^[19] Like every transport process, this follows the Boltzmann equation and consists of a resistance R_{mem} and a capacitance C_{mem} , needed to mathematically model this slower process. Consequently, the RC element must have a negative sign if it is used for the modeling of the “inductive” loop. The transfer function of this slow resistance changing process can be defined as:

$$F(\omega) = \frac{1}{1 + j\omega C_{mem} R_{mem}} \quad (15)$$

Thus, an “inductive” loop can be defined as a decrease in resistance over time under an applied voltage that follows slow frequencies, and in our case describes the kinetics of the

slow setting process. Bou and Bisquert^[11] already predicted the existence of a time-dependent resistance reduction in their memristive device modeling approach together with three different general EC memristor models, which are analogous to the assumptions made by Taibl et al. The model developed in this work is in agreement with both aforementioned models but extended by the sensitive Schottky-like interface and a geometric capacitance. Similar to the stationary analysis, the Schottky-like contact is affected by device switching. It is therefore evident that the RC element of the Z_{mem} slow process is in series with the Schottky-like contact. As a result, the EC diagram, created with the results of the stationary impedance measurement, can be expanded by adding Z_{mem} , represented by an additional RC element (see Figure 8). The extended EC is thus close to an EC developed by Yan et al. in 2010,^[69] which describes the memristive switching of a binary switching memristive device with an additional RC-Element. However, the interpretation and relevance of the individual EC elements is somewhat different, since Yan et al. analyzed a filamentary switching memristive device ion movement as memristive cause.^[69]

To gain further insights into the physical processes related to Z_{mem} , an additional modified TR-ImpSpec measurement is carried out. For this measurement, a device in the HRS is used and set to the LRS, while impedance measurements are acquired under different bias voltages. As sketched in Figure 9, the measurement series consists of 30 alternating read (0.6 V_{bias} /1.8 s) and set measurements (2.1 V_{bias} /0.3 s), starting with a read measurement to determine the initial state (HRS) of the device.

In addition to the time-dependent resistance reduction occurring at low frequencies, two further time constants of the

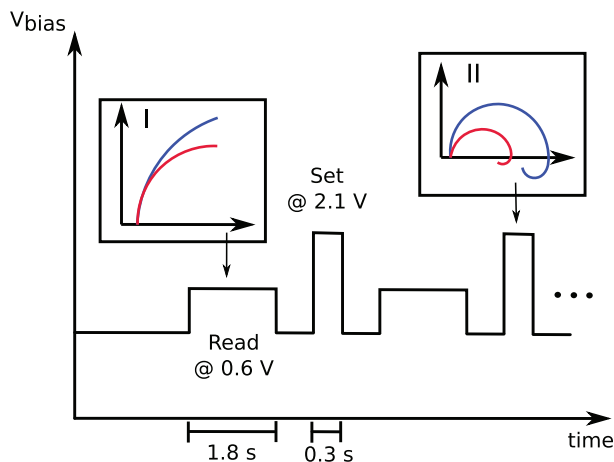


Figure 9. Principle sketch of the measurement sequence of a TR-ImpSpec experiment for a read voltage (0.6 V) and a set voltage (2.1 V). I) Sketch of the impedance data of the read voltage which show a single time constant with negative phase shift, while (II) sketch of the impedance data of the set voltage reveal a further time constant with positive phase shift. The blue curve describes the beginning of the measurement sequence (start interval), whereas the red curve describes a later interval of the sequence. A total of 13 measurement points were recorded for the set voltage and another 13 measurement points for the read voltage. A visualization of the impedance data together with the fits can be found in Supporting Information S5.

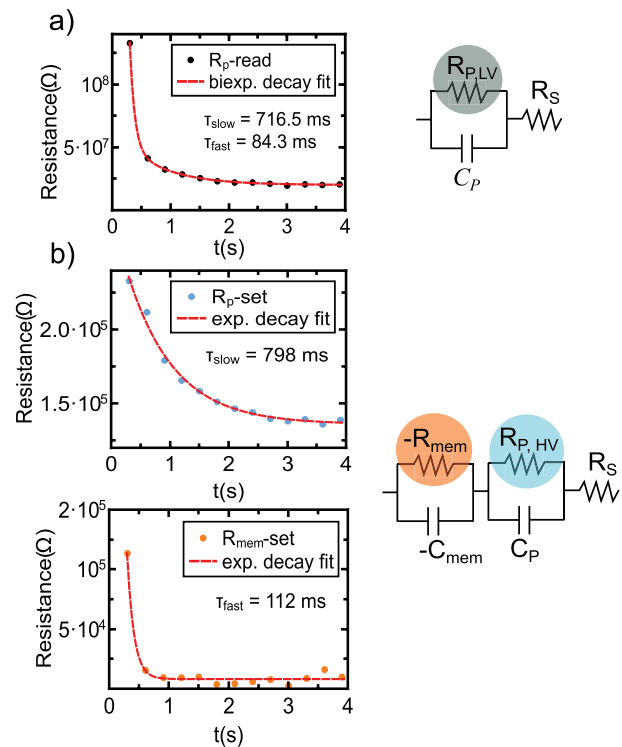


Figure 10. Resistance decay over time extracted from TR-ImpSpec and displayed in a semi-logarithmic plot. The measurement sequence consists of 15 set pulses, each combined with a read pulse. a) $R_{p,LV}$ resistance change at 0.6 V over time fitted with a second order exponential decay (red) for the corresponding EC. b) $R_{p,HV}$ and $-R_{mem}$ variation over time at 2.1 V fitted with a first order exponential decay for the corresponding EC.

setting mechanism can be identified. These can be determined by transient analysis of the impedance spectra at set and read voltages. In addition, this method can be used to obtain information about the arrangement of the EC elements. Thus, a serial arrangement of the memristive elements in the EC can be directly inferred instead of a parallel one. The impedance data of the EC element $R_{p,LV}$ captured during the lower read voltage (LV) of the TR-ImpSpec sequence follows a second-order exponential decay over time (Figure 10a),

$$\gamma = \gamma_0 + a_1 \frac{-x}{\tau_{slow,LV}} + a_2 \frac{-x}{\tau_{fast,LV}} \quad (16)$$

where the time constants $\tau_{slow,LV} = 716$ ms and $\tau_{fast,LV} = 84$ ms can be extracted from the transient analysis. For the set voltage, the previously mentioned feature of a positive phase shift for low frequencies can be observed (Figures 8 and 9). Therefore, the EC is further extended by the RC term defined in Equation (15). The transients of the two EC elements $-R_{mem}$ and $R_{p,HV}$ measured at a higher set voltage (HV) can be fitted by a first-order exponential decay.

$$\gamma = \gamma_0 + a \frac{-x}{\tau} \quad (17)$$

The two time constants $\tau_{fast,HV} = 112$ ms and $\tau_{slow,HV} = 798$ ms are derived from $-R_{mem}$ and $R_{p,HV}$ in the transient analyses

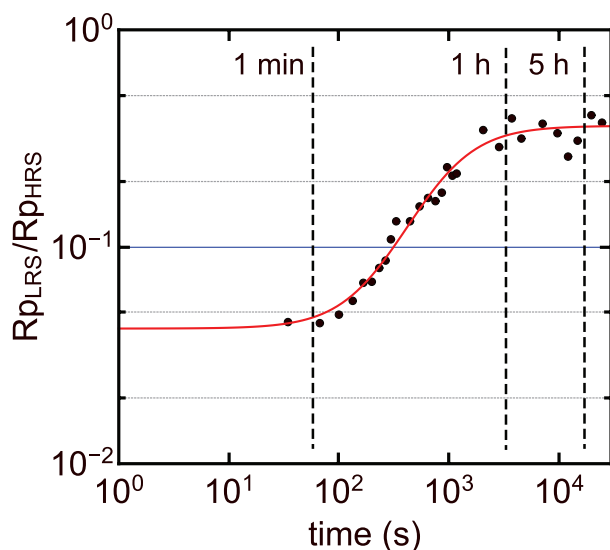


Figure 11. Retention measurement at 500 mV for the status sensitive differential resistance R_p over a period of 8 h displayed in a double logarithmic plot, and fitted with a biexponential growth.

(Figure 10b). These results match the quasi-static $I - V$ measurements of the memristive devices, where the voltage ramp time changes from 4.8 V s^{-1} to 480 mV s^{-1} , strongly influencing the magnitude of the switching process (Figures S3 and S4, Supporting Information).

A comparison of the transient analyses for the read and set measurements show excellent agreement between the determined time constants $\tau_{fast, HV}$ and $\tau_{fast, LV}$, as well as $\tau_{slow, HV}$ and $\tau_{slow, LV}$. This shows that an increased voltage makes it possible to separate two processes occurring at lower voltages and combined within $R_{p, LV}$.

Retention measurements are conducted to relate the time constants of the set process to the resetting of the device back to its initial state. For these measurements, the initial HRS of the memristive device is first determined, before setting the device in the LRS using a positive voltage ramp. Subsequently, the temporal state change is studied with a 0.5 V read pulse. The change in the $R_{p, LRS} / R_{p, HRS}$ ratio over time during the reset process is shown in **Figure 11**.

From the biexponential fit of the retention measurements, two time constants $\tau_{r1} = 133 \text{ s}$ and $\tau_{r2} = 896 \text{ s}$ are determined. When comparing the time constants for the set processes ($\tau_{set, fast}$) and ($\tau_{set, slow}$) and the back drift (τ_{r1}) and (τ_{r2}), the same scale factor of three orders of magnitude lies between the respective processes (**Table 2**). This suggests that both the slow and fast set process are caused by similar phenomena.

Since indications of surface states were found in the capacitance analysis of the impedance, the measured time constants are assigned to electron traps. The time constants for

Table 2. Extracted time constants from transient analysis of set and back drift process.

Constants	LV _{set} [ms]	HV _{set} [ms]	Retention [s]
τ_{slow}	716	798	896
τ_{fast}	84	112	133

the electron discharging from defects at an energy E_t below the conduction band E_C can be described using the Shockley–Read–Hall model^[70] as follows:^[71]

$$\tau_e = \frac{1}{N_C \sigma v_{th}} \exp\left(\frac{E_C - E_t}{k_B T}\right) \quad (18)$$

with N_C as effective density of states, σ as capture cross section, and v_{th} as average carrier thermal velocity.

A twofold time constant in a current transient for discharging of electron traps was previously reported for Si/SiO_x junctions.^[72] The existence of two time constants for switching into the LRS and drifting back into the HRS can be attributed to an energetic and spatial distribution of electron traps.^[73] The same scale factor between the two-time constants for switching and drifting back suggests that the electron traps can be separated into two types, with different discharging prefactors and the same exponential factors. Since both the density of states and the thermal velocity of the charge carriers can be assumed to be constant at the same temperature, this observation can be attributed to a change in the capture cross section. Possible spatial distribution of electron traps between bulk HfO₂ and the HfO₂/Al₂O₃ interface would affect the capture cross section and thus lead to a dispersion of the time constants for the capture and discharging of electrons. If the expected electron trap depth is determined from the retention measurement using Equation (18) with the following parameters: $N_C = 10^{19} \text{ cm}^{-3}$ ^[74] $\sigma = 1.8 \times 10^{-14} \text{ cm}^2$ ^[75]/ $2.4 \times 10^{-15} \text{ cm}^2$,^[76] $v_{th} = 3.7 \times 10^7 \frac{\text{cm}}{\text{s}}$,^[77] two different electron trap capture cross sections are assumed for the switching processes in the HfO₂ layer. The electron traps with $\sigma_B = 1.8 \times 10^{-14} \text{ cm}^2$ are expected to be located in the bulk of the HfO₂ and are responsible for a short storage time, while the traps with $\sigma_I = 2.4 \times 10^{-15} \text{ cm}^2$ are supposed to be located at the interface with the Al₂O₃ and maintain the state over a longer time scale. An evaluation of the amplitudes of the biexponential fits shows a clear majority of the traps located in the bulk with a 4 to 1 ratio compared to the interface traps. This conclusion assumes spatial non-uniformity and does not consider spatial energetic non-uniformity. A trap depth of about 0.89 eV, which is between those of 0.6 and 1 eV previously reported for HfO₂-based memristive devices,^[16] can be directly correlated to double positively charged ($V_o^{+2} \approx 0.9 \text{ eV}$) oxygen vacancies.^[78] The formation of such defects in the HfO₂ can potentially be explained by high energetic negatively charged oxygen ions in the sputter process plasma,^[79] with a density of $\rho \approx 10^{19} \text{ cm}^{-3}$ in the physical vapour deposition processes.^[80]

Furthermore, the consistency with the Shockley–Read–Hall model (Equation (18)) indicates an exponential dependence of the Boltzmann factor, which would not be expected according to Fick's diffusion laws for the movement of ions.^[81]

The conclusion of this ImpSpec study and the proposed physical model are in good agreement with those of the companion paper Zahari et al.^[26] Both analyses provided strong evidence of electron trap charging and discharging being the cause of the memristive switching process and concluded on their influence on an SCR. Additionally, the spatial arrangement of the SCR and electron traps can be inferred from the results of Zahari et al.^[26] Since depth-resolved HAXPES measurements reported by Zahari et al.^[26] (Figure 5c) show an increase in the binding

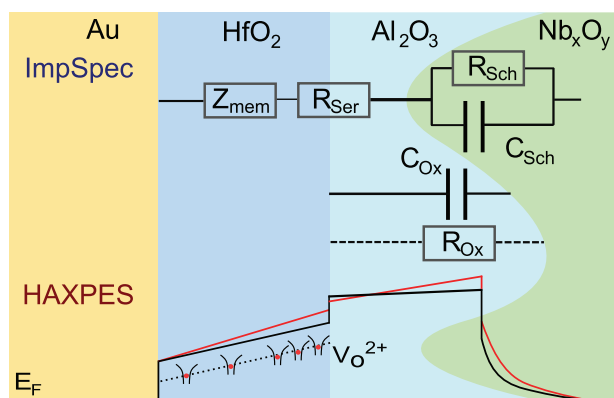


Figure 12. Model of the memristive device in terms of the spectroscopy methods used. Top: Complete EC of the memristive device in spatial order determined by ImpSpec. Bottom: Band diagram determined by HAXPES proposed by Zahari et al.^[26] (Figure 7).

energy of the HfO_2 layer toward the Au electrode, the formation of an SCR with an n-type semiconductor inside the HfO_2 can be excluded. TEM investigations reveal a mixture of Nb_2O_5 and NbO_2 in the partly oxidized back electrode (Figure 2a)), suggesting that the Schottky-like behavior described in detail in this work originates from the SCR located in the NbO_x . This is further reinforced by replacing the Nb with Hf, leading to significantly different I - V characteristics (Figure 6b in Zahari et al.^[26]).

Combining both observations lead to a physical model depicted in Figure 12 along with a sketched band diagram of the memristive device. A rough Schottky-like transition at the NbO_x/Al_2O_3 provides a parallel superposition of the capacitances of the SCR and the bulk oxide. The flow of charge carriers through the double oxide layer is enabled by a large number of shunt resistors at thinner junction parts, which can be modeled as a serial linear ohmic component. Z_{mem} serves as a description of the differential resistance representing the charging and discharging of traps in the HfO_2 , in turn influencing the space charge of the Schottky interface. The SCR in the NbO_x is affected by this net charge change in the HfO_2 layer and thus acts as an amplifier for the charging and discharging of electron traps. This can be described as a trap-assisted field effect that alters the Schottky barrier height. Thus, the existence of an SCR is necessary for a high LRS/HRS ratio in the switching behavior of such a memristive device. A possible further development of the memristive components described here, which with high probability also have a positive influence on the poor temperature stability, can be found in section 3.3 in Zahari et al.^[26]

4. Conclusions

In summary, we show that the ImpSpec analysis of memristive devices offers a comprehensive understanding of the state-sensitive interfaces and their functionalities. Using PD-ImpSpec at room temperature and under heating, a single barrier due to an imperfect Schottky contact is identified, with a SCR sensitive to the state of the device. Furthermore, we present evidence of electron traps by examining the capacitance

analysis and the interconnection between the time constants of switching states and relaxation, as a dependency on the Boltzmann factor is revealed.

The occurrence of an “inductive” loop in the non-stationary analysis is correlated to the switching state of the device. Employing TR-ImpSpec together with retention analysis, the kinetics of this state-switching process are described in more detail, revealing the contribution of two processes. The time constants ratio of these processes inferred a common trap depth or species (V_0^{2+}) with different capture cross sections. Therefore, trap-assisted field-effect altering the SCR is identified as the dominant switching mechanism for the HfO_2 -based memristive device investigated here, which behaves like an amplifier for the charge state change of the traps. The ImpSpec results are in good agreement with the HAXPES and TEM experiments presented by Zahari et al.^[26] and combining both allows to construct a more complete picture of the physical process.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was funded by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation)—Project number RU 2093 and Project-ID 434434223—SFB 1461. G.K. is thankful for a postdoctoral fellowship from the Alexander von Humboldt foundation.

Open access funding enabled and organized by Projekt DEAL.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

Keywords

analog memristive devices, combining methods, electron traps, impedance spectroscopy HfO_2

Received: November 11, 2022

Revised: February 10, 2023

Published online: April 24, 2023

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