

© 2024 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

Digital Object Identifier 10.1109/TIE.2023.3344851

IEEE Transactions on Industrial Electronics

A Fault-Tolerant Method Based on a Modified Selective Harmonic Mitigation Technique for Modular Multilevel Converter

Mahdi Aslanian
Yousef Neyshabouri
Ashkan Raki
Hossein Iman-Eini
Marco Liserre

Suggested Citation

M. Aslanian, Y. Neyshabouri, A. Raki, H. Iman-Eini and M. Liserre, "A Fault-Tolerant Method Based on a Modified Selective Harmonic Mitigation Technique for Modular Multilevel Converter," in IEEE Transactions on Industrial Electronics.

A Fault-Tolerant Method Based on a Modified Selective Harmonic Mitigation Technique for Modular Multilevel Converter

Mahdi Aslanian, Yousef Neyshabouri, *Member, IEEE*, Ashkan Raki, and Hossein Iman-Eini, *Senior Member, IEEE*, Marco Liserre, *Fellow, IEEE*

Abstract— This paper deals with the post-fault operation of a modular multilevel converter (MMC) with multiple submodules (SMs) failures. A selective harmonic mitigation (SHM) based fault-tolerant method is proposed where the modulation references of MMC phase arms are modified in post-fault conditions to achieve the maximum possible balanced line-to-line voltages using unbalanced phase voltages. In addition to mitigating the low-order harmonics, a set of constraints are defined in SHM equations so that over-modification is avoided after modification of modulation references. The suggested method optimizes the MMC capacity to provide the highest attainable line-to-line voltages with a suitable harmonic profile in post-fault conditions. Furthermore, the proposed method reduces the peak value of common mode voltage (PCMV) and high-frequency components of common mode voltage (HF-CMV). This function decreases the CMV's adverse impact on the converter and the load. Comparative simulation and experimental results are provided to validate the feasibility and effectiveness of the proposed method.

Index Terms— Fault-tolerant, Modular multilevel converter (MMC), Selective harmonic mitigation (SHM).

I. INTRODUCTION

Nowadays, multilevel inverters (MLIs) are widely utilized in various industrial applications such as medium voltage (MV) motor drives, high-voltage direct current (HVDC) systems, flexible AC transmission systems (FACTS), and renewable energy sources [1-3]. Modular multilevel converter (MMC) is of the promising MLIs offering outstanding advantages such as high modularity and controllability, no need for separate DC sources, and transformerless operation [4, 5]. There are several series-connected submodules (SMs) in each phase of the MMC, making the medium-voltage levels available using low-voltage power switches. However, the probability of failure drastically increases due to the large number of power switches used in the MMC. Therefore, it is essential to guarantee the appropriate operation of the converter under faulty conditions. In addition to disturbing the operation of the converter, a faulty SM can also cause damage to the

healthy parts of the converter. This issue makes the operation of the MMC in faulty conditions a topic of interest [6-8].

Once a fault occurs in any SM of the MMC, it should be detected and localized quickly using fault detection methods [9, 10]. When the faulty switch is diagnosed, the faulty SM is bypassed using a parallel bypass switch, and a fault-tolerant approach is hired to preserve the continuous operation of the converter in post-fault conditions [11].

The fault-tolerant methods are categorized into two types, i.e., software-based and hardware-based strategies [12-27]. In hardware-based methods, one or more redundant SMs are inserted in each leg of the MMC [12-15]. This makes the converter costly and bulky. In addition, it takes considerable time to charge the redundant SM capacitors to the rated value, which results in distortion in the output voltage waveform. To reduce the cost of the converter, a new scheme is introduced in [14], where the redundant SMs can be shared among the upper and lower arms of the MMC phases. To reduce the charging time, a spinning reserve method is presented in [15], where all redundant SMs work as the other SMs in normal operation. When a fault occurs, the F faulty SMs are bypassed, and the healthy SM capacitor voltages are increased by the ratio of $(N+M)/(N+M-F)$. Unlike the hardware-based methods, extra devices are not required in the software-based methods, and the modulation and control technique of the converter is modified to keep the continuous operation of the converter with maximum capability [16].

The zero-sequence voltage injection (ZSVI) method is the most well-known software-based strategy to balance line-to-line voltages [21-28]. By applying this method, a common mode voltage (CMV) is generated. The ZSVI methods are categorized into two general groups: Waveform-based (WB) methods [24-28] and vector-based (VB) methods [16, 21-23].

There are some VB methods presented in [16, 17, 21-23]. The VB methods calculate the proper angles between phase voltage references to achieve balanced line-to-line voltages in post-fault conditions. A simple VB method, named fundamental phase-shift compensation (FPSC), is presented in [16]. However, using this approach, a guaranteed solution is not

always available for some fault cases. An extended FPSC method has been suggested in [17] to guarantee the solution for all fault cases. These methods provide a sinusoidal CMV with a high peak value, increasing the load's voltage stress. Also, the high-frequency component of CMV (HF-CMV) may cause the flow of bearing current and higher electromagnetic interference (EMI) [18, 19]. In [21], the VB technique is first applied to the converter. Then, the DC-link voltage is increased to maintain the full performance of the converter. However, this strategy increases the voltage stress on healthy SMs. In [22, 23], VB methods based on half-wave symmetry and non-symmetrical selective harmonic elimination (SHE) modulation techniques are introduced to increase the attainable line-to-line voltages. Nevertheless, the peak value of the CMV (PCMV) remains high by using these strategies. In addition, in these methods, the switching angles for each phase of the converter are different, resulting in an increased implementation complexity.

Various WB methods have been presented in [24-28]. A ZSV term is injected into the phase voltage references in WB methods to guarantee balanced line-to-line voltages. Unlike the VB methods, the ZSV term in the WB methods includes fundamental and non-fundamental components. Hence, the WB methods provide a greater maximum attainable line-to-line voltage than the VB methods [25]. In [24], a WB method named the geometric approach has been presented. In [25], an improved WB (IWB) method is presented to decrease the fundamental component of CMV (FCMV) in a variable-speed drive application. Besides, [26] and [27] introduce modified WB fault-tolerant methods to reduce FCMV and the power imbalance among the phase legs in the cascaded H-bridge (CHB) converter. Ref [28] utilizes a clamping technique as a WB method in the static synchronous compensator (STATCOM) application.

Like VB methods, the high PCMV and HF-CMV in the WB methods have undesirable impacts on the load and its insulation, and may increase EMI problems. Furthermore, in some faulty cases, the post-fault line-to-line voltages are much lower than the pre-fault values. Hence, it is essential to increase the output voltage as much as possible to make the post-fault operation as close to the normal condition.

This paper proposes a software-based fault-tolerant method based on an enhanced selective harmonic mitigation (SHM) technique for the MMC. New constraints are determined for the switching angles in the proposed method to provide advantages such as:

- 1) generating the highest attainable post-fault line-to-line voltage among the software-based techniques. This aim is achieved by modifying the modulated waveforms and deriving of the relevant switching angles.

- 2) reducing the PCMV and HF-CMV by applying the modified SHM modulation strategy to the MMC. By doing so, the CMV impact on the load and the converter can be reduced.

Moreover, the proposed method provides

- fault tolerance against multiple SM failures without imposing extra costs on the converter.
- less calculation burden, as the switching angles for each phase of the converter, are the same; thus, implementing the proposed strategy becomes simpler.

II. THE OPERATING PRINCIPLE OF MMC

A. Normal Operation

The structure of a typical three-phase MMC converter is shown in Fig. 1. Each phase of the MMC inverter consists of two arms, each of which contains $2N$ series connected SMs, an arm inductor, and an arm resistor. The arm inductor is used to limit the circulating current and DC side fault current. The SM structure used in this paper is a half-bridge converter, the most common SM structure in MMC. Each half-bridge SM consists of two switching devices and a DC-link capacitor. By considering $V_{dc}/(2N)$ as the base value in the following equations, the per-unit values of the fundamental component of output voltages (v_{ig}) and arm voltages of the MMC phases (v_{Ui} and v_{Li}) would be calculated as follows.

$$v_{ig} = Nm \sin(\omega t + \varphi_i), \quad \forall i \in \{a, b, c\} \quad (1)$$

$$v_{Ui} = N - v_{ig} \quad (2)$$

$$v_{Li} = N + v_{ig} \quad (3)$$

Where m is the modulation index and represents the ratio of the fundamental amplitude of the output voltage to $0.5V_{dc}$.

This paper uses a quarter-wave symmetry SHM modulation technique to generate the MMC inverter's output voltage. Using this modulation technique, the Fourier series of a $(2N+1)$ -level voltage waveform can be written as follows [29].

$$v(\omega t) = \sum_{n=1,3,\dots}^{\infty} \frac{4}{n\pi} (\cos(n\alpha_1) + \dots + \cos(n\alpha_N)) \sin(n\omega t) \quad (4)$$

Where α_x represents the x^{th} switching angle.

B. Post-fault Operation

When a fault occurs, the fault detection method detects and localizes the defective SMs. Then, the faulty SMs must be bypassed in a short time to prevent more catastrophic failures.

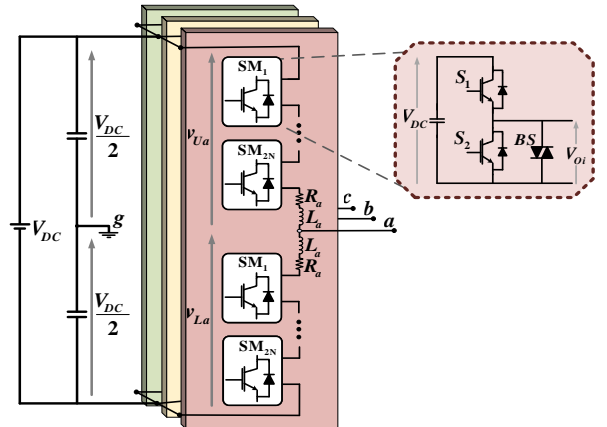


Fig. 1. Three-phase $(2N+1)$ -level MMC inverter

In the post-fault condition, by considering N_{Ui}^f and N_{Li}^f as the number of faulty SMs in each phase's upper and lower arms, the maximum attainable peak values of the inverter phase voltages (MPVs) will be calculated as (5).

$$N_i^f = N - \max\{N_{Ui}^f, N_{Li}^f\}, \forall i \in \{a, b, c\} \quad (5)$$

By injecting an appropriate CMV into the phase voltage references, the maximum balanced line-to-line voltage ($v_{ll-\max}$) can be achieved. The $v_{ll-\max}$ can be calculated as follows [25].

$$v_{ll-\max} = N_a^f + N_b^f + N_c^f - \max\{N_a^f, N_b^f, N_c^f\} = N_{\min} + N_{\text{mid}} \quad (6)$$

where N_{mid} and N_{\min} represent the middle and minimum values of the MPVs.

III. PROPOSED FAULT-TOLERANT CONTROL SCHEME

A. SHM-Based waveform modification method

This paper calculates the switching angles based on a quarter-wave symmetry SHM modulation technique. Using the switching angles, the modulated references (MRs) are generated, as shown in Fig. 2(a). To reach a balanced output voltage, the MRs of phases b and c are obtained by shifting the MR of phase a by $2\pi/3$ and $4\pi/3$ radians, respectively. As seen in Fig. 2(a), in pre-fault conditions, the maximum peak value of the MR is N_{\max} . Now let us consider the faulty case (N_{\min} - N_{\max} - N_{\max}) where the MPVs of phases a , b , and c are N_{\min} , N_{\max} , and N_{\max} , respectively, i.e., $N_a^f = N_{\min}$, $N_b^f = N_{\max}$, and $N_c^f = N_{\max}$. After fault occurrence, the MPV of phase a must be limited to N_{\min} . Hence, the modified modulated reference (MMR) of phase a is obtained by clamping the levels higher than N_{\min} in N_{\min} and lower than $-N_{\min}$ in $-N_{\min}$. The MMR and the cropped waveform from the MR (CMR) of phase a (v_a^{CMR}) are demonstrated in Fig. 2(b), and (c), respectively.

To keep the line-to-line voltages balanced, the CMR of phase a must be reduced from the MRs of the other phases. Hence, the MMRs are obtained as (7).

$$v_i^{\text{MMR}}(t) = v_i^{\text{MR}}(t) - v_a^{\text{CMR}}(t), \forall i \in \{a, b, c\} \quad (7)$$

Where v_i^{MR} is the modulated reference of phase i . By modifying the MRs, the MMRs of the phases b and c may exceed the range $[-N_{\max}, N_{\max}]$, and cause over-modulation in the converter. Hence, to avoid over-modulation, MMRs must be limited to $[-N_{\max}, N_{\max}]$ interval. Accordingly, the following constraint is considered.

$$-N_{\max} \leq v_i^{\text{MMR}}(t) \leq N_{\max}, \forall i \in \{b, c\} \quad (8)$$

When v_a^{CMR} is zero, (8) is satisfied. When v_a^{CMR} is equal to an arbitrary level of h , i.e., v_a^{MR} is equal to $(N_{\min}+h)$, the corresponding phase angle ωt should be in the range:

$$\omega t \in [\alpha_{(N_{\min}+h)}, \alpha_{(N_{\min}+h+1)}] \cup [\pi - \alpha_{(N_{\min}+h+1)}, \pi - \alpha_{(N_{\min}+h)}] \quad (9)$$

In this interval, the v_i^{MMR} equals $(v_i^{\text{MR}}-h)$ according to (7). Substituting this value in (8), results (10).

$$\begin{aligned} -N_{\max} + h &\leq v_i^{\text{MR}}(t) \leq N_{\max} + h, \\ \forall i \in \{b, c\}, h &\in \{1, \dots, N_{\max} - N_{\min}\} \end{aligned} \quad (10)$$

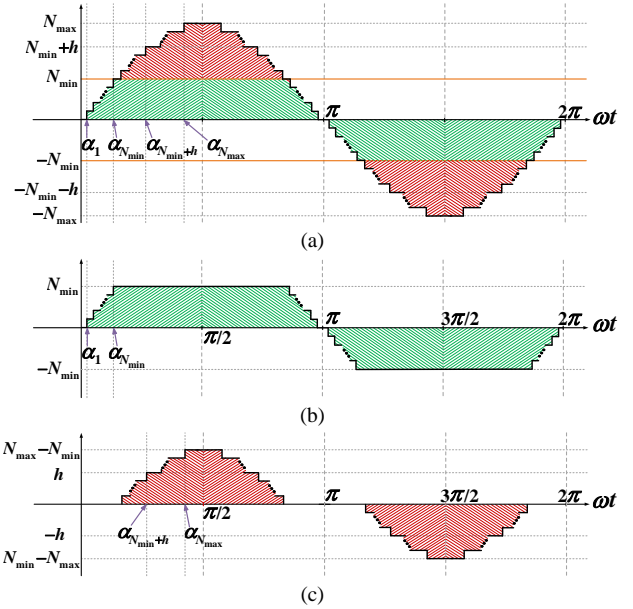


Fig. 2. The modulation and modification waveforms of phase a . (a) MR waveform. (b) MMR waveform. (c) CMR waveform

Similar to the first half-cycle, when the v_a^{MR} is equal to $(-N_{\min}-h)$ at the second half-cycle, the following constraint is obtained.

$$\begin{aligned} -N_{\max} - h &\leq v_i^{\text{MR}}(t) \leq N_{\max} - h, \\ \forall i \in \{b, c\}, h &\in \{1, \dots, N_{\max} - N_{\min}\} \end{aligned} \quad (11)$$

The upper limit of (10) and the lower limit of (11) are always fulfilled. Hence, by intersecting (10) and (11), (12) is resulted.

$$\begin{aligned} -N_{\max} + h &\leq v_i^{\text{MR}}(t) \leq N_{\max} - h, \\ \forall i \in \{b, c\}, h &\in \{1, \dots, N_{\max} - N_{\min}\} \end{aligned} \quad (12)$$

Eq. (12) indicates that the amplitude of the MRs of phases b and c must be lower than $(N_{\max}-h+1)$ and higher than $(-N_{\max}+h-1)$ levels when v_a^{CMR} is equal to h . In other words, the switching angles in phases b and c must comply with the constraints of (13) and (14), respectively.

$$\omega t < 2\pi/3 + (\pi + \alpha_{(N_{\max}-h+1)}) \text{ or } 2\pi/3 - \alpha_{(N_{\max}-h+1)} < \omega t \quad (13)$$

$$\omega t < -2\pi/3 + (\pi + \alpha_{(N_{\max}-h+1)}) \text{ or } -2\pi/3 - \alpha_{(N_{\max}-h+1)} < \omega t \quad (14)$$

Substituting (9) into (13) and (14), the following constraints are derived.

$$2\pi/3 < \alpha_{(N_{\max}-h+1)} + \alpha_{(N_{\min}+h)}, \forall h \in \{1, \dots, N_{\max} - N_{\min}\} \quad (15)$$

With consideration (15) in the proposed SHM technique, the over-modulation is avoided during the modification of MRs.

For a better understanding of the proposed technique, let us consider the faulty case of 3-5-5. The MRs of phase voltages are depicted in Fig. 3(a), including five switching angles, $\alpha_1, \alpha_2, \dots, \alpha_5$. To derive these angles, two goals are considered: **1)** The fundamental component of line-to-line voltage is set to the desired value, while low-order harmonics must be mitigated as the general rule of the SHM technique. This aim is considered in (16). **2)** The constraint of (15) must be met for α_4 and α_5 . For this fault case, (15) can be simplified as (17). This constraint will avoid over-modulation in v_b^{MMR} and v_c^{MMR} after modification of modulated references. The MMRs are shown in

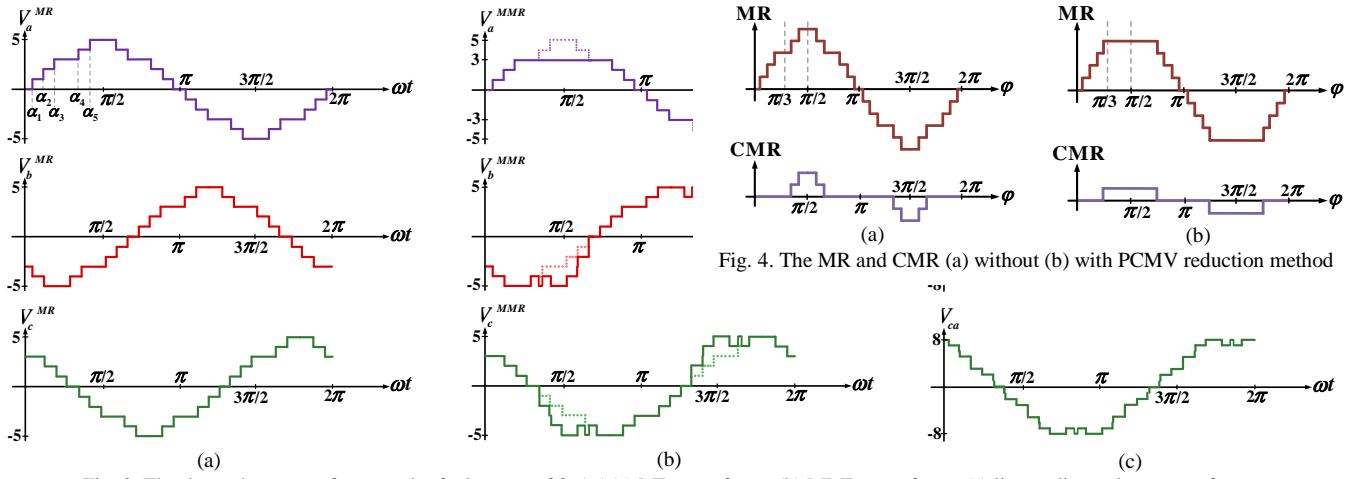


Fig. 3. The three phase waveforms under faulty case of 3-5-5 (a) MR waveforms (b) MMR waveforms (c) line-to-line voltage waveforms

Fig. 3(b). It can be seen that v_a^{MMR} is limited to $[-3, 3]$ and v_b^{MMR} and v_c^{MMR} are in the permissible range of $[-5, 5]$. Fig. 3(c) shows the line-to-line voltages by applying the MMRs to the MMC phase arms. As seen, the line-to-line voltages remain balanced despite unbalanced phase voltages.

$$\begin{cases} H_1 = m = \frac{4}{\pi}(\cos(\alpha_1) + \dots + \cos(\alpha_5)) \\ H_1 L_n > H_n = \frac{4}{n\pi}(\cos(n\alpha_1) + \dots + \cos(n\alpha_5)), n = 3, \dots, M \end{cases} \quad (16)$$

$$2\pi/3 < \alpha_4 + \alpha_5 \quad (17)$$

In (16), m is the modulation index, and L_n is the mitigation coefficient of the n^{th} harmonic.

In the above analysis, the fault condition was assumed as $(N_{\min}-N_{\max}-N_{\max})$. In a more general case, the post-fault condition can be considered as $(N_{\min}-N_{\text{mid}}-N_{\max})$. In such a case, phase b cannot generate voltage levels higher than N_{mid} ; thus, the switching angles for the voltage levels between N_{mid} and N_{\max} must comply with (15) in a similar process. In this condition, (15) is rewritten as (18).

$$2\pi/3 < \alpha_{(N_{\max}-h+1)} + \alpha_{(N_{\min}+N_{\text{mid}}-N_{\max}+h)}, \forall h \in \{1, \dots, 2N_{\max} - N_{\text{mid}} - N_{\min}\} \quad (18)$$

Therefore, constraint (18) should be considered to calculate the appropriate switching angles of MRs in the SHM modulation technique. By doing so, the over-modulation is avoided after modification of the MRs. In this condition, the maximum peak value of the CMR is obtained as (19).

$$N_{CMR-\max} = N_{\max} - N_{\min} \quad (19)$$

B. Maximum attainable post-fault line-to-line voltage

The fundamental component of the MR shown in Fig. 2(a) is calculated as (20).

$$v^1(\omega t) = \frac{4}{\pi}(\cos(\alpha_1) + \dots + \cos(\alpha_{N_{\max}}))\sin(\omega t) \quad (20)$$

Therefore, the fundamental component of the line-to-line voltage is obtained as follows.

$$v_{ll}^1(\omega t) = \frac{4\sqrt{3}}{\pi}(\cos(\alpha_1) + \dots + \cos(\alpha_{N_{\max}}))\sin(\omega t + \frac{\pi}{3}) \quad (21)$$

Since the CMR is subtracted from all three phases' MRs, the line-to-line voltages remain unchanged after the waveform modification. To obtain the upper limit of $v_{ll-\max}$, (21) is maximized by considering the constraint of (18) that leads to (22).

$$\text{Maximize}(\cos(\alpha_1) + \dots + \cos(\alpha_{N_{\max}})) \mid Eq.(18) \quad (22)$$

The optimal values of the switching angles, which make the line-to-line voltage maximum, are derived as follows.

$$\begin{cases} \alpha_x = 0 & \forall x \in \{1, \dots, N_{\min} + N_{\text{mid}} - N_{\max}\} \\ \alpha_x = \pi/3 & \forall x \in \{N_{\min} + N_{\text{mid}} - N_{\max}, \dots, N_{\max}\} \end{cases} \quad (23)$$

Therefore, the upper limit of $v_{ll-\max}$ in the proposed method is obtained as,

$$v_{ll-\max} = \frac{4\sqrt{3}}{\pi}(\frac{N_{\min} + N_{\text{mid}}}{2}) = 1.103(N_{\min} + N_{\text{mid}}) \quad (24)$$

Which is 10.3% higher than the maximum attainable line-to-line voltage obtained in (6). It is also worth noting that the maximum attainable line-to-line voltage ($v_{ll-\max}$) depends on the standard, which is considered in the SHM technique. In a code with slightly easier conditions, the maximum attainable voltage will be closer to the upper limit given in (24).

C. Reduction of the PCMV

High PCMV and CMV step changes may significantly disturb the system function. It imposes undesirable voltage stress on ac motor loads. These voltage terms induce the bearing current, which affects the bearing aging rate, and decreases the system's overall reliability. In addition, they increase mechanical vibrations and electromagnetic interferences, which are undesirable [17-19].

To decrease the PCMV in the proposed method, the MR levels are reduced as much as possible. By doing so, the number of levels of the cropped waveform (as a major part of CMV) is decreased, leading to the reduction of the PCMV. For this purpose, one level is removed from every two levels of the MR whose switching angles must follow (18). By doing so, the remaining level's switching angle must not be limited by (18) because all phases can generate one more level than MR levels

without entering the over-modulation region. Therefore, the maximum peak value of the MR ($N_{l-\max}$) and the maximum number of the non-limited levels ($N_{\alpha_{nl}}$) are obtained as (25).

$$\begin{cases} N_{l-\max} = N_{\max} - \left\lfloor \frac{2N_{\max} - N_{\text{mid}} - N_{\min}}{2} \right\rfloor \\ N_{\alpha_{nl}} = (N_{\text{mid}} + N_{\min} - N_{\max}) + \left\lfloor \frac{2N_{\max} - N_{\text{mid}} - N_{\min}}{2} \right\rfloor \end{cases} \quad (25)$$

Hence, the peak value of the MR does not exceed N_{mid} . Moreover, the maximum number of limited levels ($N_{\alpha_l} = N_{l-\max} - N_{\alpha_{nl}}$) will equal 1 or 0. If N_{α_l} is equal to 1, the switching angle of that level should be greater than or equal to $\pi/3$ according to (18) to avoid over-modulation. Otherwise, if N_{α_l} equals 0, all switching angles can take a value in the range of $[0, \pi/2]$. Applying this method reduces the maximum peak value of the CMR as (26).

$$N_{\text{CMR}-\max} = (N_{\max} - N_{\min}) - \left\lfloor \frac{2N_{\max} - N_{\text{mid}} - N_{\min}}{2} \right\rfloor \quad (26)$$

The reduction of the CMR peak value results in the reduction of the PCMV. It is worth remarking that decreasing the PCMV using the proposed method does not impose extra restrictions on the maximum attainable line-to-line voltage because the upper limit of the maximum fundamental component of two levels with limited switching angles [according to (18)] is the same as the one non-limited level, and both levels can provide a fundamental component in the range of $(0, 4/\pi\pi)$.

In the proposed method, the number of required levels for the MR will be selected based on the modulation index. In fact, the minimum number of levels through which the desired modulation index can be achieved is considered in the MR to minimize the PCMV. Hence, the peak value of the expected MR waveform based on the modulation index is defined as (27).

$$N_l = \begin{cases} \left\lfloor \frac{\pi}{4} mN \right\rfloor & m < \frac{4}{\pi} \frac{N_{\alpha_{nl}}}{N} \\ N_{\alpha_{nl}} + \left\lfloor \frac{\pi}{8} mN - 0.5N_{\alpha_{nl}} \right\rfloor & \text{otherwise} \end{cases} \quad (27)$$

Thus, the number of required levels of MR equals $2N_l + 1$, which is limited to $2N_{l-\max} + 1$ in faulty conditions. For better understanding, suppose that the modulation index of 0.8 is expected in the faulty case of 3-5-5. Without applying the PCMV reduction method, the $N_{\alpha_{nl}}$ and N_{α_l} would be equal to 3 and 2, respectively. In this condition, the MR and CMR would be similar to the waveforms of (Fig. 4(a)). However, by using the PCMV reduction method, the $N_{\alpha_{nl}}$ and N_{α_l} are equal to 4 and 0 (according to (25)). The N_l is also equal to 4 based on (27). Hence, the MR waveform of Fig. 4(b) is chosen instead of the conventional waveform of Fig. 4(a), and the switching angles will be calculated based on this waveform. By doing so, the CMR becomes similar to the waveform shown in Fig. 2(b). It is observed that the proposed method reduces the PCMV by reducing the peak value of CMR from 2 p.u. to 1 p.u..

The overall fault-tolerant control block diagram is illustrated in Fig. 5. After a fault, the faulty SMs are bypassed, and the number of faulty SMs in each phase's upper and lower arms is determined through fault detection. After that, the MPVs are determined according to (5). In the next step, the $N_{l-\max}$ and $N_{\alpha_{nl}}$ are calculated using (25) to imply the minimum value of the PCMV. Afterward, the number of required levels for the desired modulation index is calculated using (27). By knowing the values of the $N_{l-\max}$, N_l , $N_{\alpha_{nl}}$, and m , the switching angles are obtained. If N_l is lower than $N_{\alpha_{nl}}$, the switching angles that are calculated using the conventional SHM modulation technique are extracted from the corresponding look-up table. Otherwise, if N_l is greater than $N_{\alpha_{nl}}$, the switching angles that are calculated by considering the constraint (18), which limits the angles of the levels greater than $N_{\alpha_{nl}}$, are extracted from the relevant look-up table. The look-up table size by considering 32-bit for each switching angle is obtained as follows.

$$\text{LUT Size} = [(N+1) \times N / 2 + (N+1)] \times 9 \times 32 \text{ (bit)} \quad (28)$$

Furthermore, the look-up table has a negligible impact on the execution time of the algorithm. Then, the three-phase MRs are generated using the switching angles. Afterwards, by reducing the CMR from the MRs, the MMRs are produced. By obtaining MMRs as the expected inverter phase voltages, the sorting algorithm determines the gate switching signals of the SM switches to maintain the SM capacitor voltages balanced.

IV. COMPARATIVE ANALYSIS

A comparison between the proposed and previous fault-tolerant methods is made to verify the performance of the proposed method. The results of the comparison are depicted in Table I.

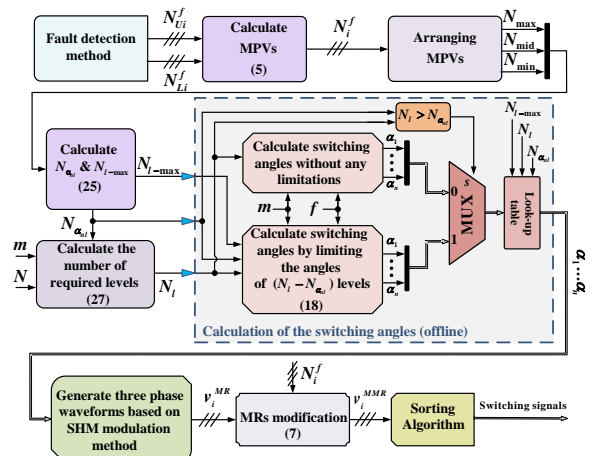


Fig. 5. Block diagram of the overall fault-tolerant control strategy

TABLE I. COMPARISON OF DIFFERENT FAULT-TOLERANT METHODS

Methods Items	Hardware-based methods		Software-based methods							
	Shared redundancy [14]	Semi-hot redundancy [13]	SVM [20]	VB & dc-bus control [21]	VB-PWM [11],[17]	VB-SHE [22]	VB-SHE [23]	IWB [25]	[26]	Proposed method
v_{ll-max} (p.u.)	Related to the num. of redundant SMs (low)	Related to the num. of redundant SMs (low)	Related to over-design (low)	Related to over-design (low)	5.97	5.99	6.08	6	6	6.38
PCMV (p.u.)	-	-	-	-	2.33	2.66	2.33	2.33	2	2
HF-CMV	-	-	-	-	High	Medium	Medium	High	High	Low
Applicable fault number	Related to the num. of redundant SMs (low)	Related to the num. of redundant SMs (low)	Related to over-design (low)	Related to over-design (low)	Multiple	Multiple	Multiple	Multiple	Multiple	Multiple
Switching losses	High	High	High	High	High	Medium	Medium	High	High	Low
complexity	Almost no	Almost no	High	Low	Low	High	High	Low	Low	Medium
Add. cost	Yes	Yes	Yes	Yes	No	No	No	No	No	No

The hardware-based strategies use redundant SMs, imposing additional costs on the system [13, 14]. Additionally, these strategies are only effective for a limited number of faults, and the v_{ll-max} would be limited because of its dependency on the number of redundant SMs. Unlike the hardware-based methods, the software-based methods do not require additional SMs. In [20, 21], however, the capacitor and the switches of the SMs should be over-designed for the desired voltages. Thus, they can only tolerate a limited number of faults, which limits the v_{ll-max} in case of multiple SM failures. Also, these methods suffer from high switching losses due to their high-frequency modulation techniques. In WB and VB methods, a ZSV is injected into the inverter phase voltages to generate v_{ll-max} . In the VB methods, the non-fundamental harmonics cannot be injected into the phase voltage references. Thus, the v_{ll-max} is lower. For the case study of 5-4-2, the VB-PWM method generates the v_{ll-max} of 5.97, which is lower than other methods. The VB-SHE methods increase the v_{ll-max} to 5.99 and 6.08 p.u. by injecting a CMV with the PCMV of 2.66 and 2.33 p.u.. In these methods, the switching angles for three phases should be calculated separately to generate three different modulated waveforms. This fact increases the complexity of VB-SHE methods. The WB method in [25] generates the v_{ll-max} of 6 p.u. by injecting a CMV with the PCMV of 2.33 p.u.. An improved WB method in [26] decreases the PCMV to 2 p.u. by generating the same v_{ll-max} (6 p.u.). The high HF-CMV causes the flow of bearing current and EMI problems in motor drives. The high-frequency modulation methods in [17, 25, and 26] cause higher HF-CMV and switching losses.

Compared to the existing works, Table I shows that the proposed method provides the v_{ll-max} of 6.38 p.u., which is the highest value. This implies that the proposed method efficiently uses the remaining healthy capacity of the converter under fault conditions through which the lowest voltage drop occurs on the ac side of MMC in post-fault operation. These aims are achieved without imposing an extra cost on the converter. In terms of CMV, the suggested method limits the PCMV to 2 p.u. On the other hand, the proposed fault-tolerant method is based on a quarter-wave symmetry SHM strategy, which is a low-frequency modulation technique. Thus, it leads to low HF-CMV and low switching losses in the converter. Regarding complexity, the switching angles based on the SHM technique need to be calculated, making the computational burden higher than PWM-based fault-tolerant techniques such as [17, 26]. But, in the proposed method, as the switching angles for the three phases of the converter are obtained from a reference phase, e.g., phase a , the number of nonlinear equations and the implementation complexity is lower than the methods of [22, 23]. In addition, third-order harmonics are eliminated naturally, reducing the number of switching angles. Thus, the complexity of the proposed method is less than existing SHE-based fault-tolerant techniques introduced in [22, 23]. It is remarkable that the proposed method is not restricted to a specific number of SMs and can be employed for MMCs with varying numbers of SMs and diverse fault conditions and applications.

V. SIMULATION RESULTS

A three-phase 11-level MMC is simulated in MATLAB/Simulink to verify the proposed fault-tolerant method. The system parameters are listed in Table II. In this study, it is assumed that the fault case of 5-4-2 has occurred. At first, the MMC works in normal condition with a modulation index of 1. The fault occurs at $t=0.04$ s, and the PFO1 (conventional VB method [17]), PFO2 (IWB method [25]), PFO3 (VB-SHE method [22]), and the proposed method are applied, respectively.

Two scenarios are provided to evaluate the performance of the system. In the first scenario, fault-tolerant methods are

TABLE II. SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Simulation	Experimental
DC-link voltage	10 kV	230 V
SM capacitor voltage	1 kV	57.5 V
Number of SMs per arm (2N)	10	4
Arm parameters (R_{arm} , L_{arm})	0.5 Ω , 2 mH	2 mH
SM capacitor	3300 μ F	3600 μ F
Base voltage (Peak)	1000 V	50 V
Base current (Peak)	160 A	2 A
Fundamental frequency	50 Hz	50 Hz
Load impedance	25+0.06j	50+14j Ω

TABLE III. THE SWITCHING SNGLES FOR PRE- AND POST-FAULT CONDITIONS

Scenario	Pre- or post-fault	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9
1	Pre-fault	6.92	13.61	16.01	17.16	28.41	43.08	67.68	73.14	73.14
	Post-fault	5.54	8.64	8.64	15.22	21.14	23.82	23.82	38.27	38.27
2	Pre-fault	12.09	19.05	19.05	35.42	60.72	63.57	63.57	87.21	87.21
	Post-fault	12.09	19.05	19.05	35.42	60.72	63.57	63.57	87.21	87.21

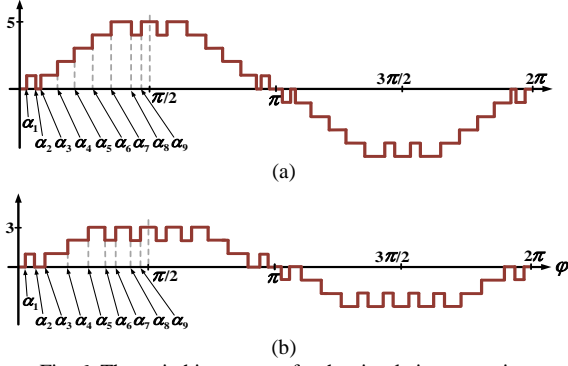


Fig. 6. The switching pattern for the simulation scenarios

utilized to achieve the v_{ll-max} . In the second scenario, the line-to-line voltage is set to 5 p.u. In the proposed method, using the SHM-PWM strategy, up to 25th harmonics are mitigated to meet the EN50160 standard that is in agreement with CIGRE WG 36-05. After fault occurrence, the mentioned methods are applied sequentially. Fig. 6 shows the switching pattern of the MR waveforms for the normal (pre-fault) and post-fault conditions for both scenarios. In addition, the values of the switching angles are listed in Table III for these two scenarios.

Scenario 1 ($v_{ll}=v_{ll-max}$): The inverter phase voltages are modified by applying fault-tolerant methods, as shown in Fig. 7(a). The MMC load phase and line-to-line voltages are exhibited in Fig. 7(b) and Fig. 7(c), respectively. It is observed that the fault-tolerant methods can keep the line-to-line voltages and phase voltages of the load balanced. Based on the FFT analysis, the fundamental term of the line-to-line voltages in PFO1, PFO2, PFO3, and the proposed methods are equal to 5.97, 6, 5.99, and 6.38 p.u., respectively. Hence, as expected, the proposed method provides greater line-to-line voltage than previous methods. The load currents are illustrated in Fig. 7(e). As seen, the load currents have remained balanced, and the proposed method provides greater load currents as a result of the higher output voltages. The CMV at the neutral point of the load is depicted in Fig. 7(d). It is observed that the PCMV in the proposed method is 2 p.u., while in the previous works, it is

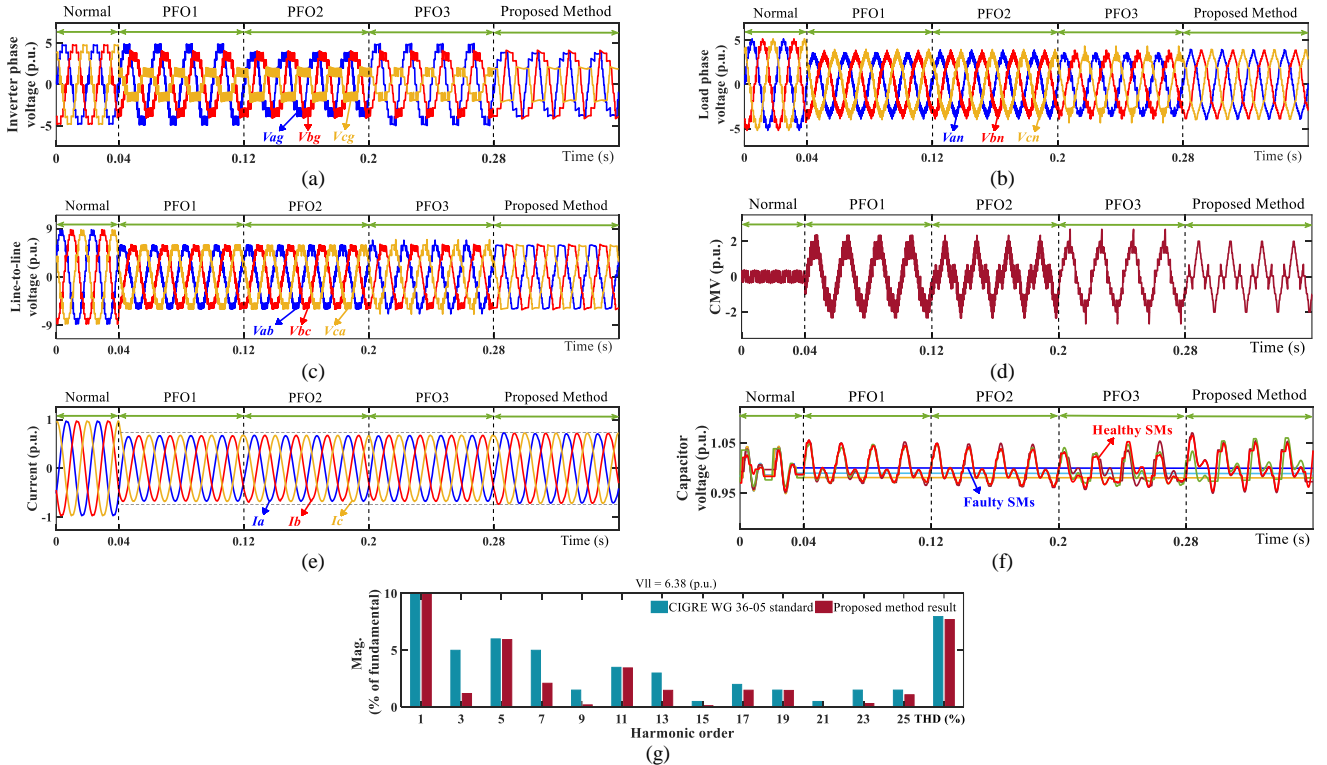


Fig. 7. Generating the maximum attainable line-to-line voltage during normal and post-fault operation of the MMC using different fault-tolerant methods. (a) Inverter phase voltage. (b) Load phase voltage. (c) Line-to-line voltage. (d) CMV. (e) Output current. (f) SM capacitor voltages (g) Line-to-line voltage harmonic spectrum

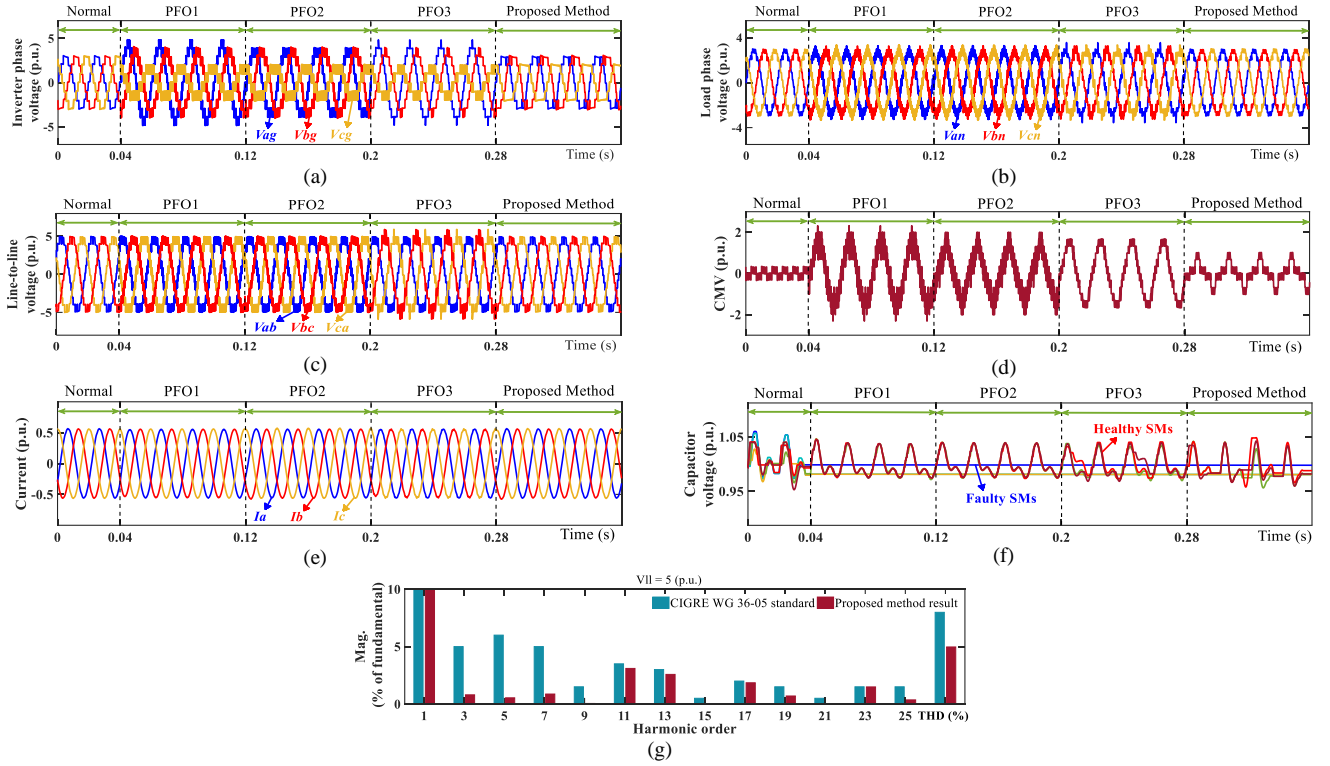


Fig. 8. Generating line-to-line voltage of 5 p.u. during normal and post-fault operation of the MMC using different fault-tolerant methods. (a) Inverter phase voltage. (b) Load phase voltage. (c) Line-to-line voltage. (d) CMV. (e) Output current. (f) SM capacitor voltages. (g) Line-to-line voltage harmonic spectrum.

2.33, 2.33, and 2.66 p.u., respectively. Therefore, the proposed method provides lower PCMV than the other methods. The RMS value of CMV harmonics higher than the 10th order in the previous methods is 0.44, 0.4, and 0.39 p.u., respectively. However, it is 0.2 p.u. in the proposed method, which indicates lower HF-CMV compared to previous works. Fig. 7(f) indicates that the bypassed SM capacitor voltages have remained constant, and the voltage stress of the healthy SMs has not increased in post-fault conditions. From Fig. 7(g), the harmonics successfully meet the standard requirements that validate the proper operation of the SHM technique.

Scenario 2 ($v_{ll}=5$ p.u.): During this scenario, the modulation index is reduced to 0.577, and the sinusoidal references are modified to generate the line-to-line voltage of 5 p.u.. Fig. 8(a) and (b) show the inverter and load phase voltages by applying different fault-tolerant methods. As seen, the load phase voltages become balanced by injecting a CMV to the neutral point of the load, resulting in the balanced line-to-line voltages and load currents as shown in Fig. 8(c) and (e). From Fig. 8(f), the bypassed SM capacitor voltages remain constant, and the voltages of the healthy SMs remain unchanged by applying fault-tolerant methods. Also, the standards are fulfilled according to Fig. 8(g). Fig. 8(d) shows that the proposed method reduces the PCMV compared to previous methods. In this case, the PCMV in the proposed method is 1 p.u., while the PCMV in the other three methods is 2.33, 2, and 1.66 p.u., respectively. Furthermore, the RMS value of higher than 10th order harmonics of the CMV in the previous methods is 0.48,

0.5, and 0.25 p.u., respectively, while its value in the proposed method is 0.24 p.u.. Hence, the proposed method offers the lowest HF-CMV.

VI. EXPERIMENTAL RESULTS

The 5-level MMC-MLI of Fig. 9 is adopted to validate the proposed method. The prototype parameters are reported in Table II. The proposed fault-tolerant control method is implemented on a Zync-7000 SoC, the prototype's central control unit. First, the MMC works in normal conditions with a modulation index of 1 for 40 ms. Afterward, a fault occurs in one SM of phase *a*, and the introduced fault-tolerant method is applied for the fault case of 1-2-2 (for 40 ms). Then, another fault happens in phase *b*, and the proposed method tries to generate the maximum output voltage in the fault case of 1-1-2 (for 40 ms). Satisfying EN50160 and CIGRE WG 36-05 standards is also considered in experimental results.

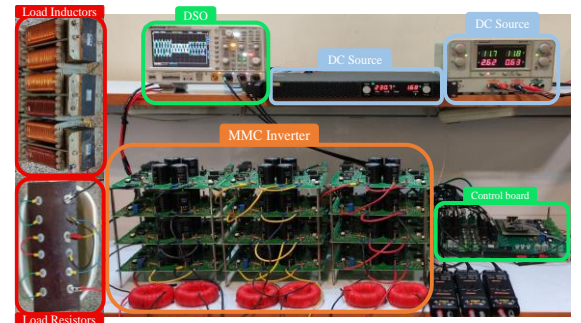


Fig. 9. Hardware prototype of three-phase five-level MMC inverter

The experimental results are presented in Fig. 10. As shown in Fig. 10(a), the inverter phase voltages are unbalanced during the fault case 1-2-2, while they are balanced in the fault case 1-1-2. This observation is because the $N_{l-\max}$ is reduced to 1 (meaning the number of levels of the MR waveforms should equal 3), and all phases can generate the MR waveforms. Applying these voltages to the MMC leads to balanced line-to-line voltages and thus balanced load phase voltages, as depicted in Fig. 10(b) and (c). The proposed method generates the $v_{ll-\max}$ of 3.18 p.u. for the fault condition 1-2-2. However, the methods of [25] and [26] provide the $v_{ll-\max}$ of 3 p.u., based on (6). Also, it is estimated from the equations that the method of [17] can generate the $v_{ll-\max}$ of 2.8 p.u. by shifting the phase voltages. The VB-SHE methods of [22] and [23] can provide the $v_{ll-\max}$ of 2.96 and 3 p.u., respectively. In the fault case of 1-1-2, the proposed method provides the $v_{ll-\max}$ of 2.127 p.u., while the methods of [17], [23], [25], and [26] all can provide the $v_{ll-\max}$ of 2 p.u.. Therefore, the proposed method increases the line-to-line voltages compared to previous works. The balanced line-to-line voltages lead to the balanced output currents as shown in Fig. 10(d). The CMV is shown in Fig. 10(e) during this scenario. It can be seen that the PCMV in the proposed method is 1.15 p.u. and 0.38 p.u., respectively. The PCMV in methods of [17], [22], [23], [25], and [26] are equal to 1.53, 1.91, 1.53, 1.53, 1.15 p.u. for the faulty case of 1-2-2, and 1.15, 1.15, 1.15, 0.76, and 0.38 p.u. for the faulty case of 1-1-2, respectively. Therefore, by applying the proposed method, the PCMV has remained as low as possible. Moreover, the HF-CMV is low due to the low-frequency modulation technique. The SM capacitor voltages of the upper leg of phase a are depicted in Fig. 10(f). It is observed that the voltage ripple of the healthy SM capacitors is not changed noticeably in faulty conditions. Fig. 10(g) and (h) show that the line-to-line voltages in the post-fault conditions meet the EN50160 and CIGRE WG 36-05 standards.

VII. CONCLUSION

This paper presented an enhanced fault-tolerant method to tolerate multiple SM failures in the MMC converter. After any switch failure, the faulty SM is isolated using a parallel bypass switch. Then, the continuous operation of the converter is maintained by healthy SMs and the proposed method. The switching angles of the modulated waveforms are calculated offline, considering two goals: **1)** mitigating the low-order harmonics (as the general rule of SHM), and **2)** generating appropriate references for MMC phase arms by modifying the modulated references, as well as preventing over-modulation in the converter.

The equations and constraints representing the above goals were derived and added to the enhanced SHM technique to calculate the switching angles on this basis and stored in look-up tables. This research offers the following advantages compared to existing works:

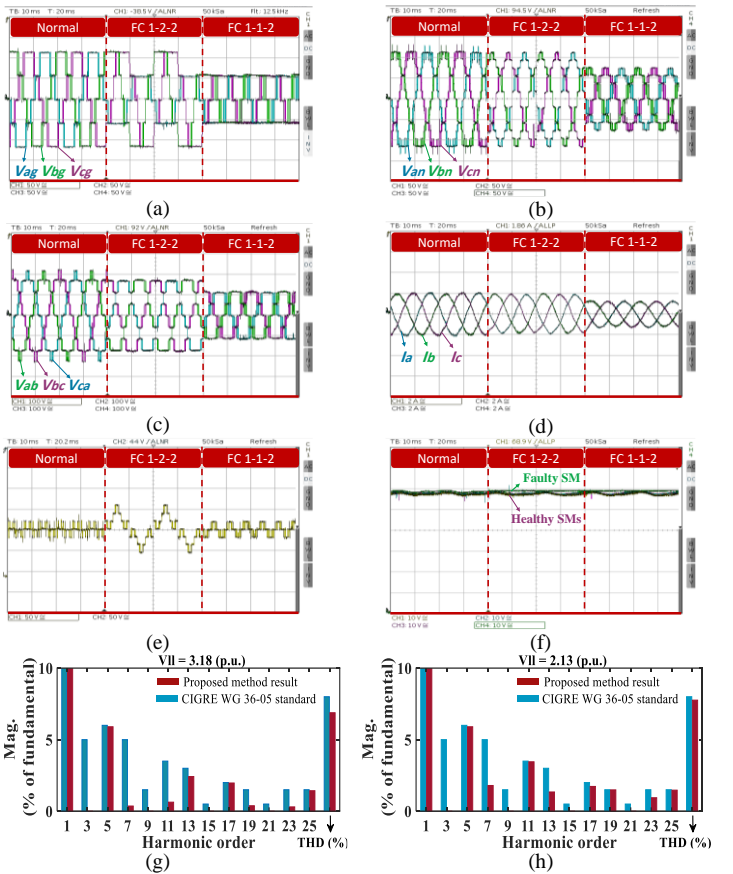


Fig. 10. Normal and post-fault operation of the 5-level MMC inverter using the proposed method. (a) Inverter phase voltage. (b) Load phase voltage. (c) Line-to-line voltage. (d) Output current. (e) CMV. (f) Phase a upper leg SM capacitor voltages (g) Output voltage harmonic spectrum in fault case of 1-2-2 (h) Output voltage harmonic spectrum in fault case of 1-1-2

- A fault-tolerant method was presented based on the SHM technique. The maximum attainable line-to-line voltage is increased compared to the existing fault-tolerant methods. For particular fault cases of 5-4-2 and 1-2-2 the attainable line-to-line voltages are 6% higher than previous works. Therefore, the post-fault output voltage would be closer to the pre-fault one, and the output voltage drop is lower under faulty conditions.
- A lower PCMV through minimizing the number of levels of the modulated reference, which reduces the voltage stress and undesired impacts on the load. In addition, the HF-CMV is reduced, decreasing the flow of bearing current and EMI issues in motor drive applications.

It is worth noting that the proposed method can be utilized in multiple SM faults without imposing extra cost and over-design on the converter. The simulation and experimental results confirmed the effectiveness of the proposed method.

REFERENCES

- [1] Y. S. Kumar and G. Poddar, "Balanced Submodule Operation of Modular Multilevel Converter-Based Induction Motor Drive for Wide-Speed Range," *IEEE Trans. on Power Electron.*, vol. 35, no. 4, pp. 3918-3927, Apr. 2020.
- [2] W. Xiang, S. Yang, G. P. Adam, H. Zhang, W. Zuo and J. Wen, "DC Fault Protection Algorithms of MMC-HVDC Grids: Fault Analysis, Methodologies, Experimental Validations, and Future Trends," in *IEEE Trans. on Power Electron.*, vol. 36, no. 10, pp. 11245-11264, Oct. 2021.

- [3] S. Wu, Z. Liu, Z. Li, H. Zhang and X. Hu, "Impedance Modeling and Stability Analysis in Vehicle-Grid System with CHB-STATCOM," in *IEEE Trans. on Power Systems*, vol. 35, no. 4, pp. 3026-3039, July 2020.
- [4] N. Tashakor, Z. Li and S. M. Goetz, "A Generic Scheduling Algorithm for Low-Frequency Switching in Modular Multilevel Converters With Parallel Functionality," in *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2852-2863, March 2021.
- [5] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Trans. on Power Electron.*, vol. 30, no. 1, pp. 4-17, Jan. 2015.
- [6] B. Mirafzal, "Survey of Fault-Tolerance Techniques for Three-Phase Voltage Source Inverters," *IEEE Trans. on Ind. Electron.*, vol. 61, no. 10, pp. 5192-5202, Oct. 2014.
- [7] J. Wang and Y. Tang, "A Fault-Tolerant Operation Method for Medium Voltage Modular Multilevel Converters With Phase-Shifted Carrier Modulation," *IEEE Trans. on Power Electron.*, vol. 34, no. 10, pp. 9459-9470, Oct. 2019.
- [8] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke and H. S. Krishnamoorthy, "Survey on Fault-Tolerant Techniques for Power Electronic Converters," *IEEE Trans. on Power Electron.*, vol. 29, no. 12, pp. 6319-6331, Dec. 2014.
- [9] M. Aslanian, H. Iman-Eini and Y. Neyshabouri, "An Open-Circuit Fault Detection and Localization Scheme for Switch Failures in Modular Multilevel Converter Based on Arm Voltage Analysis," *PEDSTC*, pp. 503-508, 2022.
- [10] Z. Geng, M. Han, Z. W. Khan and X. Zhang, "Detection and Localization Strategy for Switch Open-Circuit Fault in Modular Multilevel Converters," *IEEE Trans. on Power Deliv.*, vol. 35, no. 6, pp. 2630-2640, Dec. 2020.
- [11] S. P. Gautam, M. Jalhotra, L. K. Sahu, M. R. Kumar and K. K. Gupta, "A Survey on Fault Tolerant and Diagnostic Techniques of Multilevel Inverter," in *IEEE Access*, vol. 11, pp. 60866-60888, 2023.
- [12] B. Li, Y. Zhang, R. Yang, R. Xu, D. Xu and W. Wang, "Seamless Transition Control for Modular Multilevel Converters When Inserting a Cold-Reserve Redundant Submodule," *IEEE Trans. on Power Electron.*, vol. 30, no. 8, pp. 4052-4057, Aug. 2015.
- [13] Yang L, Jia L, Zou Y, Zhang M, Yang H. "Semi-hot redundant control method for modular multilevel converter-based high-voltage direct current systems under submodules fault." *IET Power Electron.*, 2023.
- [14] S. Farzamkia, H. S. Rizi, A. Q. Huang and H. Iman-Eini, "Shared Redundancy Strategy to Improve the Reliability and Fault-Tolerant Capability of Modular Multilevel Converter," *IEEE Trans. on Ind. Electron.*, Online early access.
- [15] B. Li *et al.*, "Fault Diagnosis and Tolerant Control of Single IGBT Open-Circuit Failure in Modular Multilevel Converters," *IEEE Trans. on Power Electron.*, vol. 31, no. 4, pp. 3165-3176, Apr. 2016.
- [16] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. on Ind. Electron.*, vol. 52, no. 4, pp. 1080-1085, Aug. 2005.
- [17] P. Lezana and G. Ortiz, "Extended Operation of Cascade Multicell Converters Under Fault Condition," *IEEE Trans. on Ind. Electron.*, vol. 56, no. 7, pp. 2697-2703, Jul. 2009.
- [18] W. Jiang *et al.*, "A Novel Virtual Space Vector Modulation With Reduced Common-Mode Voltage and Eliminated Neutral Point Voltage Oscillation for Neutral Point Clamped Three-Level Inverter," *IEEE Trans. on Ind. Electron.*, vol. 67, no. 2, pp. 884-894, Feb. 2020.
- [19] M. S. Hassan, A. Abdelhakim, M. Shoyama, J. Imaoka and G. M. Dousoky, "Three-Phase Split-Source Inverter-Fed PV Systems: Analysis and Mitigation of Common-Mode Voltage," *IEEE Trans. on Power Electron.*, vol. 35, no. 9, pp. 9824-9838, Sept. 2020.
- [20] M. Aleenejad, H. Mahmoudi, S. Jafarishadeh and R. Ahmadi, "Fault-Tolerant Space Vector Modulation for Modular Multilevel Converters With Bypassed Faulty Submodules," *IEEE Trans. on Ind. Electron.*, vol. 66, no. 3, pp. 2463-2473, March 2019.
- [21] S. Farzamkia, M. Noushak, H. Iman-Eini, A. Khoshkbar-Sadigh and S. Farhangi, "Fault-Tolerant Method to Reduce Voltage Stress of Submodules in Postfault Condition for Regenerative MMC-Based Drive," *IEEE Trans. on Ind. Electron.*, vol. 68, no. 6, pp. 4718-4726, June 2021.
- [22] M. Aleenejad, H. Mahmoudi and R. Ahmadi, "Multifault Tolerance Strategy for Three-Phase Multilevel Converters Based on a Half-Wave Symmetrical Selective Harmonic Elimination Technique," *IEEE Trans. on Power Electron.*, vol. 32, no. 10, pp. 7980-7989, Oct. 2017.
- [23] Z. Ni, A. H. Abuelnaga and M. Narimani, "A New Fault-Tolerant Technique Based on Nonsymmetrical Selective Harmonic Elimination for Cascaded H-Bridge Motor Drives," *IEEE Trans. on Ind. Electron.*, vol. 68, no. 6, pp. 4610-4622, June 2021.
- [24] F. Carnielutti, H. Pinheiro and C. Rech, "Generalized Carrier-Based Modulation Strategy for Cascaded Multilevel Converters Operating Under Fault Conditions," *IEEE Trans. on Ind. Electron.*, vol. 59, no. 2, pp. 679-689, Feb. 2012.
- [25] S. Ouni *et al.*, "Improvement of Post-Fault Performance of a Cascaded H-bridge Multilevel Inverter," *IEEE Trans. on Ind. Electron.*, vol. 64, no. 4, pp. 2779-2788, Apr. 2017.
- [26] M. Fathi and S. A. Khajehoddin, "A Fault Compensation Scheme for Cascaded H-Bridge Inverter with Reduced Common Mode Voltage," *IEEE Trans. on Ind. Electron.*, Online early access.
- [27] A. Raki, Y. Neyshabouri, H. Iman-Eini and M. Aslanian, "Reduction of Common-Mode Voltage in Cascaded H-Bridge Inverter Under Faulty Conditions," *ICEE*, pp. 909-914, 2022.
- [28] Q. Xiao *et al.*, "An Improved Fault-Tolerant Control Scheme for Cascaded H-Bridge STATCOM With Higher Attainable Balanced Line-to-Line Voltages," *IEEE Trans. on Ind. Electron.*, vol. 68, no. 4, pp. 2784-2797, Apr. 2021.
- [29] M. Najjar, A. Moeini, M. K. Bakhshizadeh, F. Blaabjerg and S. Farhangi, "Optimal Selective Harmonic Mitigation Technique on Variable DC Link Cascaded H-Bridge Converter to Meet Power Quality Standards," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 1107-1116, Sept. 2016.



Mahdi Aslanian received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Tehran, Tehran, Iran, in 2019 and 2022, respectively. His research interests include power electronics converters and their application in renewable energy systems, HVDC systems, and transportation electrification.



Yousef Neyshabouri received the B.Sc., M.Sc. and Ph.D. degrees, all in electrical engineering from the University of Tehran, Tehran, Iran, in 2011, 2013 and 2018, respectively. He is currently an Associate Professor with the Faculty of Electrical and Computer Engineering, Urmia University, Urmia, Iran. His current research interests include multilevel power converters and their application in FACTS and renewable energy systems.



Ashkan Raki received his B.Sc. and M.Sc. degrees in Electrical Engineering from the University of Tehran, Tehran, Iran, in 2019 and 2022, respectively. His research interests include power electronics technologies with a particular focus on their application in renewable energy sources and power systems.



Hossein Iman-Eini received the Ph.D. degree in electrical engineering jointly from the University of Tehran, Tehran, Iran, and the Grenoble Alpes University, Grenoble, France, in 2009. He is a Professor of Electrical Engineering at the School of Electrical and Computer Engineering, University of Tehran. He currently follows a Heisenberg position in Chair of Power Electronics at Kiel University, Germany. His research interests include power

electronics and applications of power electronics in power systems/grids



MARCO LISERRE (S'00-M'02-SM'07-F'13) obtained the MSc and PhD degrees in Electrical Engineering from the Politecnico di Bari in 1998 and 2002 respectively. He has been Associate Professor at the Politecnico di Bari and, since 2012, Professor of Reliable Power Electronics at Aalborg University (Denmark). Since 2013 he is Full Professor and holds the Chair of Power Electronics at the University of Kiel (Germany). He has been offered and declined professorships at several universities. He has published more than 700 technical papers (1/3 of them in international refereed journals), one book and 7 granted

patents (4 with companies). These works have received more than 50,000 citations. Marco Liserre was selected as an Highly Cited Researcher in the field of Engineering (Clarivate Web of Science) from 2014 to 2021. Several of his students (MSc, PhD and post-docs) are in leading positions in industry and universities worldwide. In 2023, he joined the Fraunhofer ISIT on a part-time basis as deputy director and director of the new division "Electronic Energy Systems", as well as of the Kiel branch of the Fraunhofer ISIT.

He is a member of IAS, PELS, PES and IES. He has served all these societies in various capacities. In PELS, he is Co-Editor of the IEEE Open Access Journal in Power Electronics and Technical Committee Chairman of the Committee on Electronic Power Grid Systems. He has co-chaired several IEEE conferences being several times Chairman. He has received 16 awards from IEEE, PCIM and EPE-PEMC, including the prestigious 2018 IEEE-IES Mittelman Achievement Award and the 2023 IEEE-PELS R. David Middlebrook Achievement Award. In 2023, he was awarded the title of "Ufficiale" by the President of the Italian Republic. In 2025 he will be Chairman of Powertech 2025 in Kiel.