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A Single Carrier Rotating Modulation for Modular Multilevel Converter based Isolated DC-DC Converters in EV Charging Station

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Abstract-- A modular multilevel converter (MMC) based isolated DC-DC converter is an interesting topology enabling medium-voltage DC (MVDC) grid-connected EV charging stations, an efficient solution for reducing power conversion stages. In modulations applied to MMC based DC-DC converters, a quasi-two-level (Q2L) modulation is suitable for medium-frequency (MF) DC-DC conversion and can reduce stresses on a transformer due to a low dv/dt characteristic. However, attention must be paid to balancing DC capacitor voltages between the submodules (SMs), and it is hard to apply the existing methods in practice because of the complex balancing algorithm. Therefore, this paper proposes a new modulation with inherent SM DC capacitor voltage balancing for the MMC, which is used as a primary converter of MVDC isolated DC-DC converters. The proposed modulation can achieve the natural balancing of the DC capacitor voltages by rotating the SM insertion duration. In addition, improved balancing of SM capacitor voltages can be achieved by applying a controller to compensate for the effects of uncertain parameters such as capacitance tolerances. The effectiveness of the proposed modulation is verified with simulation and experimental results.

Index Terms—Modular Multilevel Converter, Dual-Active-Bridge DC-DC Converter, Medium-Voltage DC, Medium-frequency Transformer.

I. INTRODUCTION

Nowadays, fast charging of electric vehicles (EVs) is a major challenge, and there are demands for large-scale EV charging stations worldwide. In one hand, conventional EV charging stations, connected to medium-voltage AC (MVAC) grids through a low-frequency distribution transformer (LFDT), have limitation in hosting capacity, extremely fast charging, and also high efficiency. On the other hand, direct integration to medium-voltage DC (MVDC) grids can surpass the problem and increase power conversion efficiency [1]. Modular multilevel converter (MMC) based conversion at MVAC provides MVDC grid without the need for LFDT. Thereby, MVDC can be directly converted to LVDC by using MMC based isolated DC-DC converter employing only one medium frequency transformer as the isolation stage. In comparison to conventional charging stations based on LFDT, this will lead to higher energy efficiency conversion and hosting capacity [2], [3].

The operation of MMCs at medium-frequency (MF)

highly depends on the output voltage waveform and modulation type for achieving optimal power losses as well as balanced submodule (SM) voltages. One of the well-known modulations for MMCs is the nearest-level modulation (NLM) [4]. This modulation has been used widely for high-level MMC systems, such as for high-voltage DC transmission, because the number of submodules (SMs) is large enough to generate a current close to the ideal sinusoidal waveform. However, in the case of MMC-based isolated DC-DC converters, it is not only hard to implement the modulation for the MF quasi-two-level (Q2L) voltage waveform, but also requires a large computational burden due to the SM DC capacitor voltage balancing control based on a SM sorting algorithm. Another modulation technique is a carrier-based phase-shift modulation (PSM) [5-7]. This modulation is suitable for MF converter applications because gate signals can be generated by comparing a reference with carriers that are shifted to generate the Q2L waveform. Nevertheless, it has a chronic problem in that it is complicated for balancing the SM DC capacitor voltages, when this method is applied to the MMC-based isolated DC-DC converter. In [8], a modulation with a voltage balancing method swapping switching pattern is proposed, but this modulation is not flexible to be applied to the general MMC-based isolated DC-DC converter because it is used for voltage elevation in hybrid MMCs.

Therefore, a new modulation which has an inherent balancing capability of the SM DC capacitor voltages is proposed in this paper for the MMC-based isolated DC-DC converter. The proposed modulation is based on a single carrier for each MMC arm, and references for each SM are rotated every single period of the carrier to achieve even power distribution between SMs. Since individual references are used for the corresponding SMs, it is easy to implement rotating the references flexibly in microcontrollers. Furthermore, this paper employs an SM voltage balancing controller that can be applied to the proposed modulation, considering the SM voltage imbalance due to non-identical SM DC capacitance and load changes. The proposed modulation is verified in MATLAB simulation first. Besides, its performance is confirmed with experimental results.

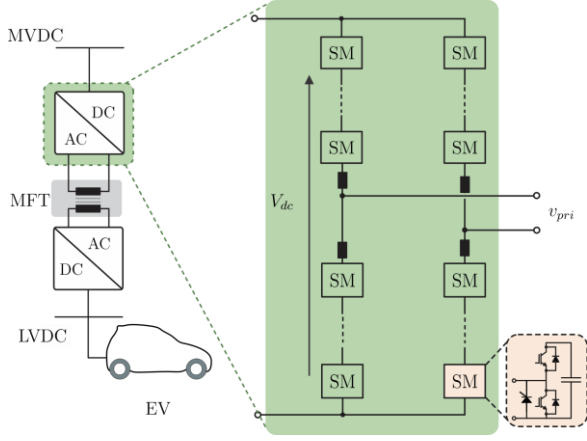


Fig. 1 (a) MVDC connected isolated DAB DC-DC converter for the EV fast charging station (b) Single-phase MMC system connected to a primary winding of MFT.

This paper is organized as follows, the MMC based isolated dual-active-bridge (DAB) DC-DC converter using a MF transformer and features of conventional modulations are introduced in Section II. To reduce complexity to implement the modulation, Single carrier-based rotating modulation (SCRM) and SM DC capacitor voltage balancing controller are described in Section III. In Section IV, the proposed modulation is verified with simulation and experimental results. Finally, this paper presents concluding remarks in Section V.

II. MMC BASED ISOLATED DC-DC CONVERTER

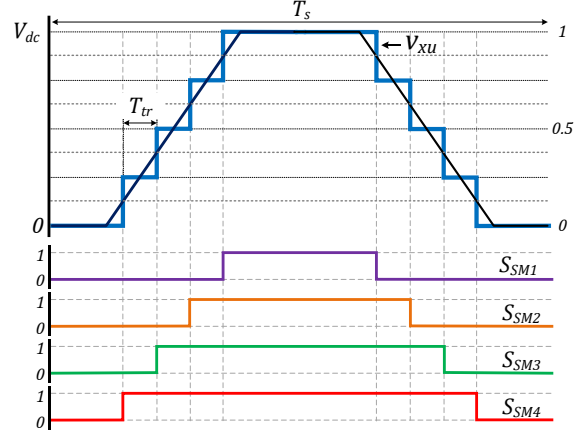
A. Topology

Fig. 1(a) shows the EV charging station with an isolated DAB DC-DC converter, which is connected to the MV DC grid. The MMC is a well-known topology for high-voltage and medium-voltage applications because it has good DC voltage scalability, modularity and high reliability. For this reason, the MMC can be placed between the MVDC grid and MF transformer (MFT), as a primary side H-bridge converter. Another H-bridge converter used as the EV charger is connected to a secondary winding of the MFT and it provides an LV DC source to EV.

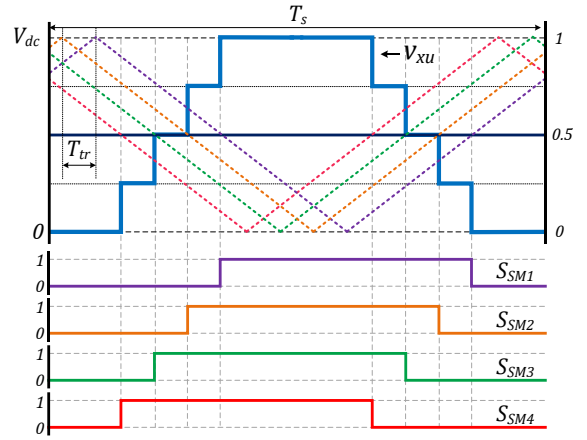
In MMC-based isolated DC-DC converters, the medium-frequency AC voltage waveform is preferred over a low-frequency sinusoidal waveform used in general MMCs because the size of arm inductors, transformer and SM capacitors can be significantly reduced. However, using a medium-frequency rectangular waveform as typical DAB converters [6] use would cause the problem with the breakdown of the galvanic isolation in the MFT. That's why a quasi-two-level (Q2L) waveform that changes the voltage level in the staircase leading to a low dv/dt is mainly used for the MMC-based isolated DAB DC-DC converter.

B. Conventional Modulations for Q2L waveform

There are two representative modulation techniques that can be applied to the MMC-based isolated DC-DC converter, nearest-level modulation (NLM) and carrier-



(a)



(b)

Fig. 2 Conventional modulations for the 5-level MMC in the DC-DC converter. (a) Nearest-level modulation; (b) Phase-shift PWM.

based phase-shift PWM (PSM). The NLM is a popular modulation for high-level AC-DC MMCs due to low switching losses compared to the PSM. As depicted in Fig. 2(a), even if gate signals input to SMs can be generated according to the trapezoidal voltage reference, but it requires a complicated process such as an SM DC capacitor voltage sorting and balancing algorithm. Furthermore, it is hard to implement this modulation for generating the MF Q2L waveform with microcontrollers, because the NLM is not based on carriers and the SM state transitions occur at a few μs interval. On the other hand, since the PSM is based on carriers shifted by the angle corresponding to the transition interval, T_{tr} , as shown in Fig. 2(b), it is simpler to implement the Q2L voltage waveform than NLM. However, like NLM, this modulation technique doesn't have the inherent voltage balancing ability. For this reason, the PSM requires an additional voltage balancing controller rotating gate signals or carriers, which is very complicated to implement.

III. PROPOSED SINGLE CARRIER ROTATING MODULATION

A. Single Carrier Rotating Modulation (SCRM)

In order to provide the MF Q2L waveform of several

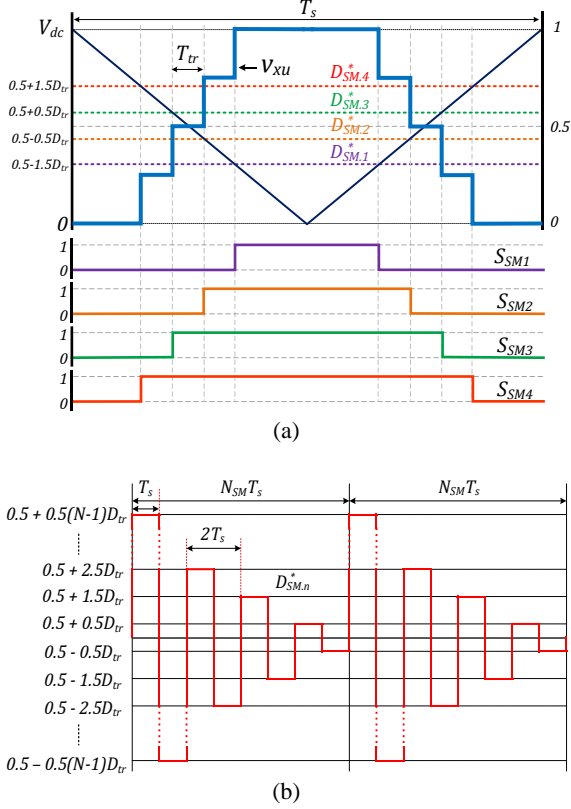


Fig. 3 SCRM for the single arm. (a) Q2L voltage waveform and SM states with comparison between carrier and references; (b) Reference rotation.

kHz or more, a carrier-based modulation is suitable for the MMC in the DC-DC converter. Although PSMs have been studied in many papers for this reason [5-7], there are concerns about unbalanced SM capacitor voltages and solutions [6-7] to address this concern are complex. Thus, this paper proposes a single carrier rotating modulation (SCRM), which can achieve inherent SM voltage balancing capability with easy implementation.

As shown in Fig. 3(a), a single carrier is used for each arm of the MMC and references, $D_{SM,n}^*$, as many as the number of SMs, N_{SM} , are compared with the carrier to generate gate signals. As expressed in (1), the references are defined with the different duty ratio, D_{tr} , corresponding to the transition time (T_{tr}), which is defined in (2) to generate the Q2L waveform.

$$D_{SM,n}^* = 0.5 - \{0.5(N_{SM} - 1) + (n - 1)\}D_{tr} \quad (1)$$

$$D_{tr} = 2T_{tr}/T_s \quad (2)$$

Where T_s is one period of the PWM.

However, the different insertion time of each SM cause an imbalance in the SM voltages. To solve this problem, the rotation of the references is applied, as shown in Fig. 3(b). The references are changed at every cycle of the PWM, and, after one full cycle, $N_{SM}T_s$, the average value of the references applied to each SM is equal to 0.5. This means the average current flowing through the DC

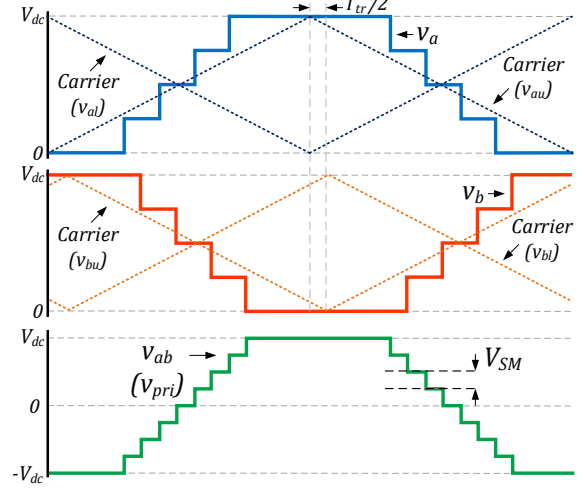


Fig. 4 Output voltage of the MMC, v_{ab} , with phase shifted ($T_{tr}/2$) carriers.

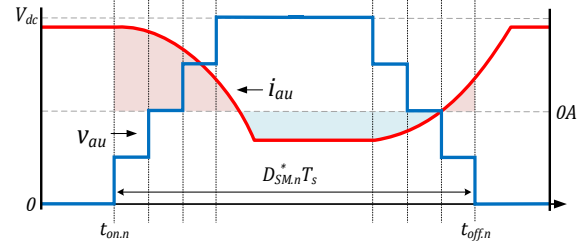


Fig. 5 Upper arm voltage and current in phase 'A' for a cycle of PWM.

capacitor in SMs is the same as each other. To achieve further voltage balancing condition, the rotation profile is designed like zigzag so that the insertion time for two periods ($2T_s$) can be 50% of T_s .

As shown in Fig. 4, in addition, carriers applied to lower arms have a 180° phase shift difference from that of the upper arms to generate the voltage by each leg from 0V to V_{dc} . For phase 'B', carriers are shifted by about 180° compared with the aforementioned leg to generate the voltage, v_{ab} , from $-V_{dc}$ to V_{dc} . Furthermore, a phase shift corresponding to $0.5T_{tr}$ can achieve a lower dv/dt characteristic of the output voltage.

B. Analysis on SM Voltage Balancing

As known well, the SM DC capacitor voltages of the MMC are affected by the arm current when the SM is inserted to generate the arm voltage [4]. Under the bypass condition of SM, however, there is no change in the SM voltage. The SM voltage change during one period of the PWM can be defined as (3), considering arm voltage and current in Fig. 5.

$$\Delta V_{SM,n}(D_{SM,n}^*T_s) = \frac{1}{C_{SM}} \int_{t_{on,n}}^{t_{off,n}} i_{arm} dt \quad (3)$$

$$D_{SM,n}^*T_s = t_{off,n} - t_{on,n} \quad (4)$$

Where C_{SM} is the capacitance of SMs, i_{arm} is arm current, and $t_{on,n}$ and $t_{off,n}$ are the moment inserting

and removing the SM_n , respectively. The time difference between the two moments is related to the insertion duration of the corresponding SM, as given in (4).

From (3), the change in the SM voltage per PWM cycle is related to the duration when the same arm current is applied. During the single period, the voltage changes of each SM are different because the duration for each SM is not equal to each other. When the rotation is applied, as depicted in Fig. 3, the average insertion duration for all SMs is equal to 0.5, as expressed in (5).

$$\frac{1}{N_{SM}} \sum_{k=1}^{N_{SM}} D_{SM,n}^*(k) = 0.5 \quad (5)$$

Since the average duration for a single rotation is the same between the SMs, it is deduced from (3) that the amount of change in voltage will be the same if the same arm current flows during the rotation.

C. SM Voltage Balancing Controller

Although the duration and power distribution for all SMs can be achieved with the rotating modulation, the SM voltages can be unbalanced due to parameter difference in capacitors and semiconductors, and output power changes. For these reasons, this paper applies a voltage balancing controller, in addition to the proposed SCRМ.

Since each SM operates by the corresponding reference that is rotated, rapid voltage imbalance doesn't occur. Hence, the applied controller can be based on the average capacitor voltage of all SMs and each SM for every single rotation ($4T_s$), $V_{SM,avg}$ and $V_{SMn,avg}$, respectively, and outputs additional duration, $D_{VB,n}^*$, through a proportional controller with a gain, K_p . As presented in (3) and Fig. 5, the longer average insertion duration of the SM causes the average SM voltage to increase. Thus, a modified reference for the insertion duration can be defined as (6). $D_{VB,n}^*$ is a controller output through a limiter that is used to keep the proper Q2L voltage waveform, as given in (7).

$$D_{SMVB,n}^* = D_{SM,n}^* + D_{VB,n}^* \quad (6)$$

$$D_{VB,n}^* = K_p(V_{SM,avg} - V_{SMn,avg}) \quad (7)$$

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation

Simulation with MATLAB Simulink is carried out to validate the proposed modulation, and simulation conditions are presented in Table I. In the simulation, each arm consists of 10 SMs and the rated SM DC capacitor voltage is 600V. It is worth noting that MF voltage output not only leads to smaller SM capacitance, which is designed as 100 μ F, than general MMCs, but also, there is little concern about circulating current.

Fig. 6 shows simulation results of the proposed modulation about waveforms of primary and secondary side converter output voltage, v_{pri} and v_s , and the two arm currents of phase A, i_{au} and i_{al} , when the output power at LVDC link is 36kW. It can be seen the Q2L waveform output by the MMC and a low dv/dt feature can

Table I Simulation Conditions

Parameters	Values
DC voltage at MV grid (V_{MVDC})	6,000V
LV DC voltage (V_{LVDC})	600V
Maximum output power	36kW
Number of SMs in each arm (N_{SM})	10
SM DC capacitance (C_{SM})	100 μ F
Arm Inductor	2mH
Leakage inductor	500 μ H
Output voltage frequency	1kHz
Transition interval (T_{tr})	10 μ s

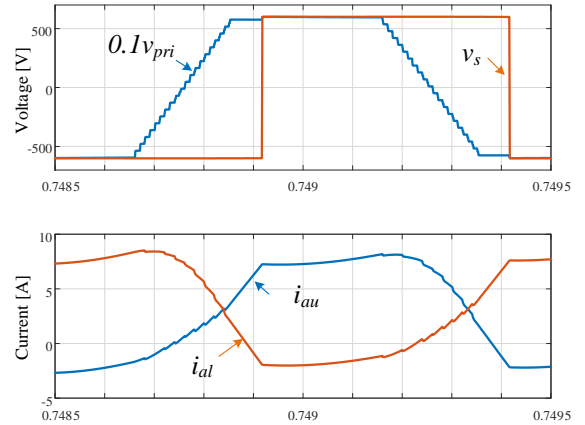


Fig. 6 Voltage waveforms output by two converters in the DAB converter and two arm current waveforms in phase A.

be achieved with 20 voltage steps, when the output voltage changes between $-V_{MVdc}$ to V_{MVdc} .

Fig. 7 presents the SM capacitor voltages of the upper and lower arms in phase A, and its voltage distribution comparison according to the SM voltage balancing control. Since the proposed SCRМ has the inherent balancing ability by the reference rotation, it is confirmed in Fig. 7(a) that the voltage waveforms seem roughly balanced without the proposed balancing control. In Fig. 7(b), however, the average voltage of each SM is far apart from the average of all SM voltages, and the maximum voltage difference between them is up to 4V. On the other hand, in the case of the proposed voltage balancing control, it is confirmed that the SM voltage waveforms in Fig. 7(c) are more balanced than that of Fig. 7(a). Moreover, the average voltage of 10 SMs converges to the average value of all SM voltages and their maximum difference is less than 0.5V, as shown in Fig. 7(d). From these results, the proposed SCRМ has the inherent balancing capability, and SM voltage balancing control is effective in balancing the SM voltages on average.

Fig. 8 shows the effect of the output load change on balancing SM voltages. As the output DC current on the LVDC side varies as shown in Fig. 8(a), Fig. 8(b) and (c) present the overall SM voltages inside the arms are balanced, although the level and voltage ripple of the overall voltage changes.

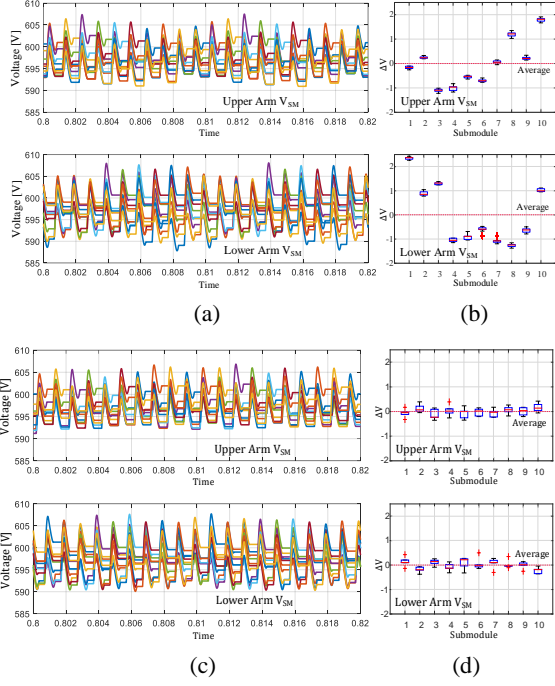


Fig. 7 SM DC capacitor voltage waveforms and the average voltage distribution. (a) and (b) without the proposed SM voltage balancing controller. (c) and (d) with the proposed SM voltage balancing controller.

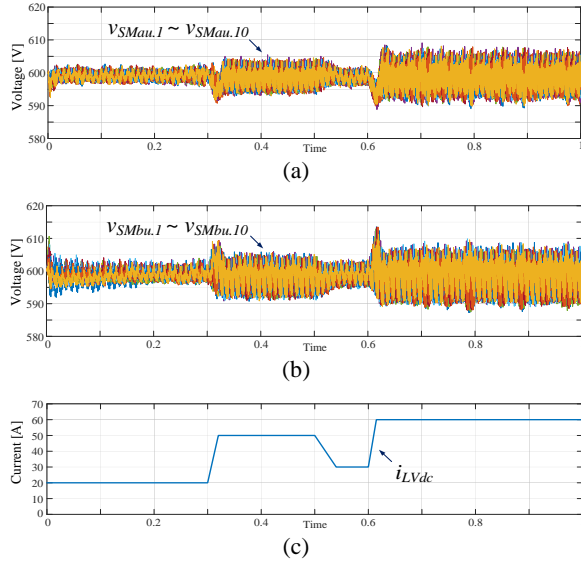


Fig. 8 SM DC capacitor voltage waveforms with the LVDC load current changes. (a) Phase A upper arm SM voltages. (b) Phase A lower arm SM voltages. (c) LVDC load current.

B. Experiment

In Fig. 9, a three-phase 5-level MMC setup used for the experiment is shown. Among three phases, two phases used as the H-bridge converter of the DAB converter. In the experiment, the MMC is connected to resistive load just to confirm the proposed modulation. Table II shows the specification and conditions for the experiment.

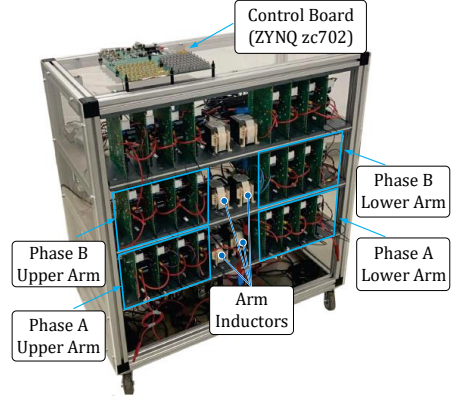


Fig. 9 5-level MMC prototype used for experiment

Table II Experimental Conditions

Parameters	Values
DC supply voltage	80V
Number of SMs in each arm (N_{SM})	4
SM DC capacitance (C_{SM})	2mF
Arm Inductor	1.8mH
Output voltage frequency	1kHz
Transition interval (T_{tr})	10 μ s
Resistive load	100 Ω

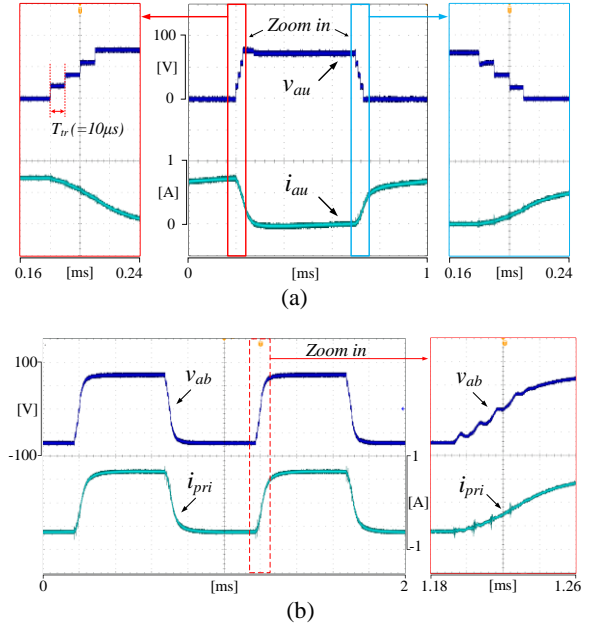


Fig. 10 Voltage and current waveforms of MMC for the DAB DC-DC converter. (a) Phase A upper arm voltage and current. (a) output voltage and current.

Fig. 10 shows the voltage and current waveforms of the MMC used as the DAB converter. Each arm generates the Q2L voltage waveform like Fig. 10(a) and this voltage cascading up for 40 μ s because there are 4 SMs and T_{tr} is set as 10 μ s. From a result shown in Fig. 10(b), the voltage (v_{ab}) across the primary winding of the MF transformer has a low dv/dt features.

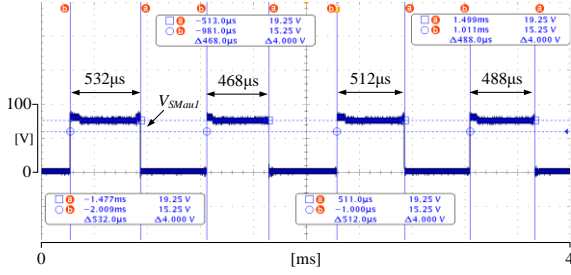


Fig. 11 SM voltage output for 4 PWM periods ($4T_s$).

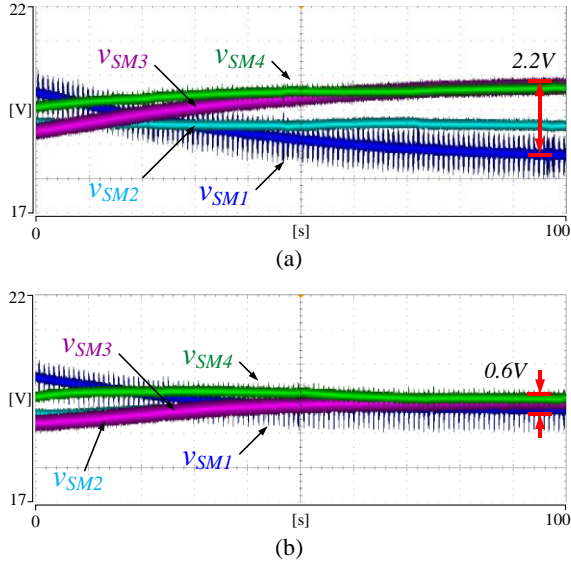


Fig. 12 Effect of the SM voltage balancing control. (a) Without balancing controller. (b) With balancing controller.

Fig. 11 shows the SM voltage output for 4 PWM cycles. As described in Fig. 3, the proposed modulation employs zigzag rotation, which can be seen in the waveform. Even though the duration difference between cycles is not the same due to the effect of the dead-time and voltage balancing controller, there is about $20\mu\text{s}$ difference between PWM periods, and the average duration of the first and last two periods is about $500\mu\text{s}$, which is 50% duty cycle.

Fig. 12 shows the effect of the SM voltage balancing control. The initial condition of all SM voltages is not balanced well. When the SCRМ is applied without the balancing controller, SM voltages are unbalanced more, and the imbalance voltage is about 2.2V in the end of the experiment, as shown in Fig. 12(a), even if the voltages do not diverge more. This imbalance is due to unbalanced parameters between SMs. On the other hand, Fig 12(b) shows the effect of the proposed controller. Although the SM voltages are unbalanced initially, all voltages are balanced in the end, and its voltage difference is about 0.6V.

V. CONCLUSIONS

This paper proposes the SCRМ for the MMC used in the MV isolated DAB DC-DC converter for the EV charging stations. The limitation of existing modulation,

such as NLM and PSM, for the DC-DC converters and the need to develop a new modulation suitable for the DC-DC converter are described in this paper. The proposed modulation is based on a single carrier for each arm and uses the rotation of the references for all SMs to provide the natural SM DC capacitor voltage balancing capability. Moreover, the voltage balancing controller is applied to balance the average voltage of SMs. In the simulation results, it is validated the proposed modulation has the inherent voltage balancing feature and the effectiveness of the proposed controller by reducing the difference in the average SM voltage by approximately 90%. Furthermore, in the experimental results, it is verified the proposed modulation has the ability to suppress the SM voltage imbalance and the proposed balancing controller is effectively reduce this imbalance by 73%.

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