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Design of the Dual Active Bridge Converter to Minimize RMS Current in Supercapacitor Interface Applications

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Abstract—In applications employing energy storage systems based on supercapacitors (SCs), there are challenges in designing the power converter to interface the SCs due to their inherent terminal voltage variation. Unlike other dc/dc topologies, the dual active bridge (DAB) topology is suitable for SC interfacing. However, to improve efficiency, a design strategy is required to mitigate conduction losses caused by the wide variation in SC terminal voltage. This paper proposes a DAB design methodology that defines an optimal turns ratio to minimize the RMS current over SC charging and discharging cycles. The design formulation aims to reduce the DAB RMS current for a general modulation scheme and is implemented for single phase-shift (SPS) modulation. Circuit simulations and experiments on a laboratory prototype with an output power of 250 W demonstrate the reduction in RMS current achieved by the proposed design.

Index Terms—design optimization, dual active bridge, gradient descent, supercapacitor.

I. INTRODUCTION

Supercapacitors (SCs) possess properties suitable for short-term energy storage applications. However, since the terminal voltage of SCs varies with their state of charge, an interfacing dc/dc converter is essential to the integration of SC-based storage with power processing systems [1]. The limited operating voltage of commercially available SCs motivates the use of converters with a high voltage gain, popularizing transformer-coupled alternatives [2]. In particular, the isolated dual active bridge (DAB) converter offers scope for efficient high-gain operation [3], and is employed in SC interfacing efforts in the literature [4]–[8].

Owing to the strong voltage dependence of the state of charge of SCs, optimized SC stacks typically operate over a wide range of terminal voltage [9]. This poses challenges to the design of the interfacing DAB. Since the transformer primary and secondary voltages are significantly unmatched over the range of operating voltage of the SC, a high RMS current of the DAB results and aggravates conduction losses [10]. In addition to improved modulation methods [4], [11], the transformer turns ratio provides a degree of freedom to reduce these losses.

The studies detailed in [4]–[6] select a turns ratio that matches transformer primary and secondary voltages at the nominal condition. Although these works focus on other aspects of the SC/DAB system, the matching of voltage at an intermediate SC operating point holds intuitive promise. The turns ratio is selected to improve the soft switching range of the DAB in [8]. However, soft switching is influenced more significantly by the modulation strategy than the turns ratio, as demonstrated in subsequent studies [12]. Conduction loss reduction through an optimal turns ratio is thus open to exploration. Since the conduction loss is a quadratic function of the DAB RMS current, the reduction of RMS current over a charge/discharge cycle reduces these losses and consequently, improves the efficiency of the DAB interfaced SC.

Methods existing in the literature for the circuit design optimization of the DAB address concerns of soft switching and RMS current over an operating range [13], [14]. In [13], a search is performed over the design space to minimize the RMS current of the DAB over the entire operating range. This general method can be refined in the present application, where the weightage of operating points is fixed by the terminal parameters of the SC. Similarly, the method outlined in [14] employs a mixed analytical and numerical technique to minimize the worst-case RMS current in the DAB. However, the minimization of the RMS value of the current over the entire operating interval, rather than the worst-case RMS current considered in [14], is relevant to SC interfacing applications.

This paper presents a circuit design method to minimize the RMS current of an SC interface DAB over the entire operating interval. Since SCs operate over a range of terminal voltages, the entire charging or discharging interval is considered instead of a single operating point. The contributions of the paper are:

- 1) the formulation of a general DAB design method to minimize the RMS current during SC charging and discharging,
- 2) the implementation of the design for a selected single phase shift (SPS) modulation scheme, and
- 3) the verification of results in circuit simulation and experiment.

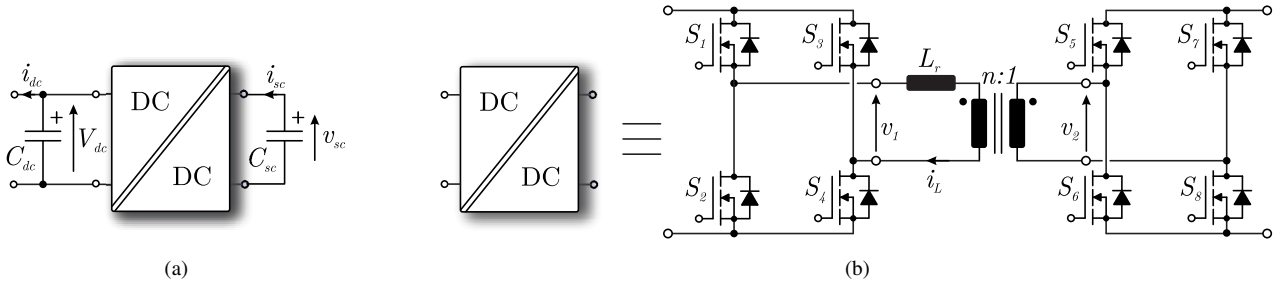


Fig. 1: (a) Schematic, and (b) circuit diagram of a DAB converter interfacing an SC to a DC bus.

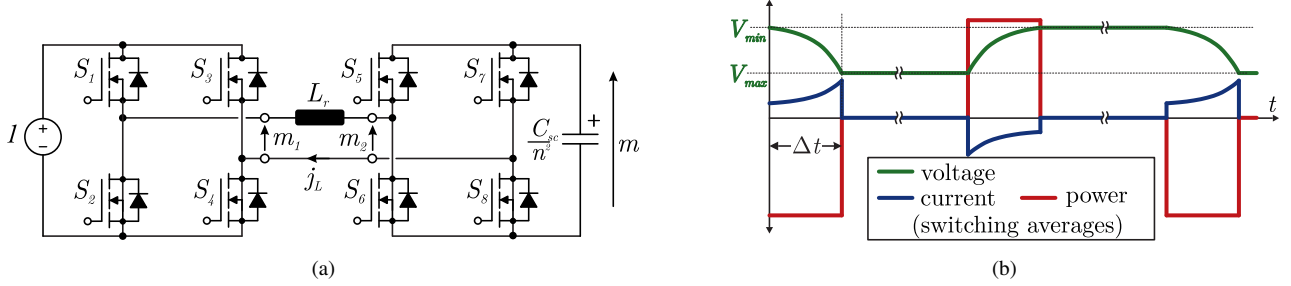


Fig. 2: (a) Normalized equivalent circuit of the DAB. (b) Waveforms of SC quantities illustrating charge/discharge operation.

The paper is organized as follows. The minimization objective of the design problem is formulated in section II for a generic modulation strategy. The optimization procedure, along with applicable constraints, is described in section III, and the execution of this procedure is demonstrated for SPS modulation in section IV. Simulation and experimental results validating the results of the design optimization are presented in section V. Section VI concludes the paper.

II. RMS CURRENT-BASED DESIGN OBJECTIVE FORMULATION

The schematic of an SC stack (C_{sc}) interfaced to a DC bus is shown in Fig. 1a. The interface DAB, shown in Fig. 1b, comprises primary (S_1 – S_4) and secondary (S_5 – S_8) side MOSFET full bridges coupled through an inductor (L_r) and an $n : 1$ transformer. The circuit design process involves the selection of the parameters ($\{n, L_r\}$) to achieve the desired operation over a range of SC voltage (v_{sc}).

The voltages produced by the primary- and secondary-side full bridges, v_1 and v_2 , respectively, and the primary-side inductor current (i_L) describe the operation of the DAB. To normalize these quantities, the base voltage (V_B) is chosen equal to the nominal DC bus voltage (V_{dc}). The impedance of the coupling inductor at switching frequency (f_{sw}) is selected as the base impedance (Z_B), as (1).

$$Z_B = 2\pi f_{sw} L_r \quad (1)$$

Further, all quantities are referred to the transformer primary side through a turns-ratio transformation. The normalized quantities are presented in the equivalent circuit of Fig. 2a, and their corresponding expressions are given in Table I.

Key operating waveforms of the SC during charging and discharging are illustrated in Fig. 2b. When required, the SC

TABLE I
EXPRESSIONS FOR NORMALIZED CIRCUIT QUANTITIES OF THE DAB

Normalized quantity	Expression
Primary full bridge voltage, m_1	v_1/V_B
Secondary full bridge voltage, m_2	v_2/nV_B
AC link current, j_L	$i_L Z_B/V_B$
Output (SC) voltage, m	v_{sc}/nV_B
Output (SC) power, p	$P_{sc} Z_B/V_B^2$

stack supports a power requirement at the DC bus through the DAB and is discharged in the process. The stack is then recharged to its capacity and maintained in this state until the next discharge. In the present analysis, the charging and discharging of the SC are considered to take place at a constant magnitude of power (P_{sc}). A non-constant P_{sc} with a known profile may be represented as a train of pulses ($\sum_i P_{sc,i}$).

As shown in Fig. 2b, the DAB operates over a range ($[V_{min}, V_{max}]$) of output voltage. This range is defined by the design of the SC stack along with the load power profile [15] and support duration requirements [9]. The nature of operation of the SC is inherently transient, so that the DAB operates at each value of v_{sc} only for an instant. Hence, the total conduction loss over the entire operating interval, rather than that at a specific operating point, is to be mitigated.

The conduction loss at a particular operating condition depends on the switching-cycle RMS value ($i_{L,rms}$) of the inductor current. The quantity, $i_{L,rms}$, also varies over the operating interval. Therefore, the design objective is to minimize the RMS value, I_{rms} , of inductor current over the entire interval. Assuming quasi-steady state, I_{rms} is equal to the square mean of $i_{L,rms}$ over the duration (Δt) of SC charging

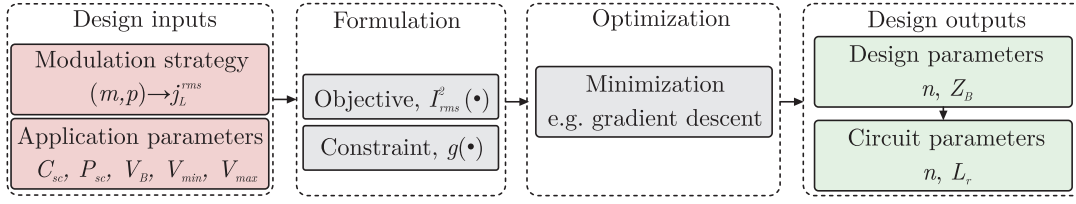


Fig. 3: Flowchart of the proposed design methodology.

TABLE II
EXPRESSIONS FOR THE RMS CURRENT IN THE DAB OVER THE SC OPERATING INTERVAL FOR SPS MODULATION

Equations	
$I_{rms}(n, Z_B) = \sqrt{\frac{\pi^2 C_{sc} V_B^4}{12 n^2 Z_B^2 P_{sc} \Delta t} \int_{\frac{n V_{min}}{V_B}}^{\frac{n V_{max}}{V_B}} \left[m^3 + m - \left(2m + \frac{4 P_{sc} Z_B}{\pi V_B^2} \right) \sqrt{m^2 - \frac{4 P_{sc} Z_B m}{\pi V_B^2}} \right] dm} \quad (2)$	
$I_{rms}(n, Z_B) = \sqrt{f\left(\frac{n V_{max}}{V_B}\right) - f\left(\frac{n V_{min}}{V_B}\right)} \quad (3)$	
$f(m) \triangleq \frac{\pi^2 C_{sc} V_B^4}{12 n^2 Z_B^2 P_{sc} \Delta t} \left(\frac{m^4}{4} + \frac{m^2}{2} - \frac{2}{3} (m^2 - 2mq)^{3/2} - 2q(m-q)\sqrt{m^2 - 2mq} + 2q^3 \log \left[(m-q) + \sqrt{m^2 - 2mq} \right] \right), \quad q \triangleq \frac{2 P_{sc} Z_B}{\pi V_B^2}$	

or discharging operation, as in (4).

$$I_{rms} \triangleq \sqrt{\frac{1}{\Delta t} \int_0^{\Delta t} i_{L,rms}^2 dt} \quad (4)$$

A steady-state terminal condition of the DAB is specified by the normalized SC voltage, m , and the normalized SC power, p . However, the waveform of the inductor current, and hence, its RMS value, depend on the modulation strategy of the full bridges. Thus, a given modulation strategy maps the normalized DAB terminal condition, (m, p) , to a value of the normalized switching cycle averaged RMS current, $j_{L,rms}(m, p)$.

The dynamics of the SC voltage are slow compared to the switching time scale by design. This permits the use of steady state relations for $j_{L,rms}$. The normalization expression for j_L in Table I is used to rewrite the expression for I_{rms} in (4), as (5).

$$I_{rms} = \sqrt{\frac{1}{\Delta t} \int_0^{\Delta t} \left(\frac{V_B}{Z_B} \right)^2 j_{L,rms}^2(m, p) dt} \quad (5)$$

Neglecting the drop in the equivalent series resistance (ESR) of the SC, the normalized output power of the DAB is related to the normalized terminal voltage dynamics of the SC, as

$$p = \frac{C_{sc} Z_B}{n^2} m \frac{dm}{dt}. \quad (6)$$

The expression for p in Table I is substituted in (6), and the resulting expression is rearranged to obtain (7).

$$\frac{P_{sc}}{V_B^2} = \frac{C_{sc}}{n^2} m \frac{dm}{dt} \quad (7)$$

The time variable in (5) is eliminated using (7). Further, the definition of the quantity, p , in Table I, is used to reformulate

(5) in terms of the design parameter, Z_B . Thus, the expression for I_{rms} is obtained as (8).

$$I_{rms} = \sqrt{\frac{C_{sc} V_B^4}{n^2 Z_B^2 P_{sc} \Delta t} \int_{\frac{n V_{min}}{V_B}}^{\frac{n V_{max}}{V_B}} j_{L,rms}^2(m, Z_B) m dm} \quad (8)$$

The proposed design method targets the minimization of the RMS current of the DAB over the entire interval of operation. The expression for I_{rms} given in (8) therefore serves as a general objective function to be minimized over the space of design parameters, (n, Z_B) .

III. DESIGN OPTIMIZATION METHODOLOGY

The objective to be minimized is derived in a general form in section II. Considerations such as soft switching requirements constrain the design space further. These are represented in general using an inequality,

$$g(n, Z_B) < 0. \quad (9)$$

The design optimization problem described by the objective in (8) and the constraint in (9) is stated formally as (10).

$$(n^*, Z_B^*) = \underset{n, Z_B}{\operatorname{argmin}} I_{rms} |_{g < 0} \quad (10)$$

The inputs to this optimization problem are

- 1) application dependent parameters, represented by the quantities, P_{sc} , C_{sc} , V_B , V_{max} , V_{min} , and Δt ,
- 2) the modulation strategy, represented by the quantity, $j_{L,rms}(\cdot)$, and
- 3) further design preferences such as soft switching constraints, represented by the quantity, $g(\cdot)$.

The complexity of the expression for I_{rms} is influenced by the term inside the integral in (8). This term depends

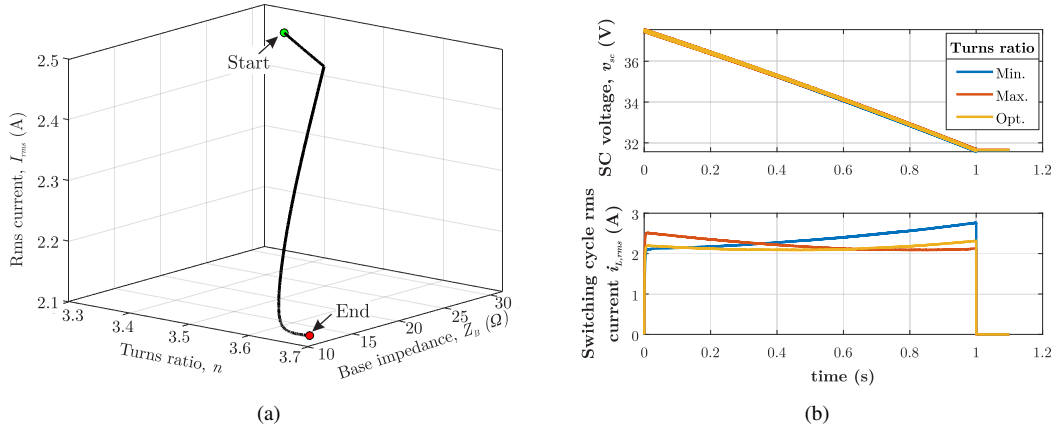


Fig. 4: (a) Optimization trajectory in the space of design parameters for the proposed optimization for SPS modulation. (b) Simulated waveforms of SC discharge operation showing SC voltage (v_{sc}) and switching cycle RMS current ($i_{L,rms}$) for minimum turns ratio (Min.), maximum turns ratio (Max.), and proposed optimal (Opt.) designs.

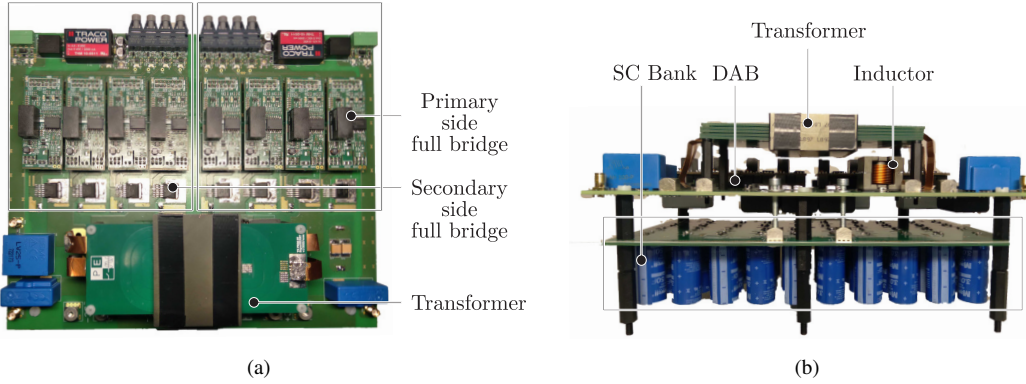


Fig. 5: (a) Top view, and (b) front view of fabricated laboratory prototype of the SC interface DAB.

on the modulation strategy. In the simplest case of SPS modulation, the analytical minimization requires the solution of a transcendental equation. Modulation schemes employing more control variables, e.g. that in [14], are expected to involve greater analytical complexity. Thus, a numerical optimization approach based on the gradient descent method is adopted.

The initial guess for the turns ratio, n_0 , is selected using the existing methodology, i.e., $n_0 = V_g/V_{max}$. The initial guess, $Z_{B,0}$, for Z_B is selected to limit the worst-case phase shift to $\pi/4$ radians. Since the gradient descent method identifies local minima, the design obtained from this set of initial parameters achieves a reduction in RMS current with respect to existing design methods. The update rule for the parameters $[x_1 \ x_2] = [n \ Z_B]$ at the k -th iteration step is given by (11).

$$x_i^{(k+1)} = \begin{cases} x_i^{(k)} - \gamma_i \frac{\partial(I_{rms}^2)}{\partial x_i}, & \text{if } g_i^{(k)} < 0 \\ x_i^{(k)}, & \text{otherwise} \end{cases} \quad (11)$$

$$\text{where } g_i^{(k)} \triangleq g\left(x_i^{(k)} - \gamma_i \frac{\partial(I_{rms}^2)}{\partial x_i}, x_j^{(k)}\right); i = 1, 2; j \neq i$$

The constraint $g(\cdot)$ is checked prior to update and enforced by preventing the update of the violating parameter. The gradient gains (γ_1, γ_2) are tuned by trial and error. The proposed design flow is illustrated in Fig. 3.

IV. DESIGN EXAMPLE USING SINGLE PHASE SHIFT MODULATION

For the SPS modulation scheme [11], the full bridges are operated to produce square-wave voltages with a phase shift (ϕ). The phase shift required to achieve a given operating condition (m, p) is given by

$$\phi = \frac{\pi}{2} \left(1 - \sqrt{1 - \frac{4p}{m\pi}} \right). \quad (12)$$

The expressions in [11] yield $j_{L,rms}$ as (13).

$$j_{L,rms} = \frac{\pi}{\sqrt{12}} \sqrt{m^2 + 1 - m \left(2 + \frac{4p}{\pi m} \right) \sqrt{1 - \frac{4p}{\pi m}}} \quad (13)$$

The substitution of (13) into the general expression in (8), yields (2), given in Table II. The expression in (2) is evaluated using standard integration tables to obtain the closed-form expression for I_{rms} as (3), also given in Table II.

Since moderate phase shifts are preferable in SPS, setting $\phi \leq 45^\circ$ yields the constraint $g(\cdot)$ as (14).

$$\frac{Z_B}{n} - \frac{3\pi}{16} \frac{V_B V_{min}}{P_{sc}} \leq 0 \quad (14)$$

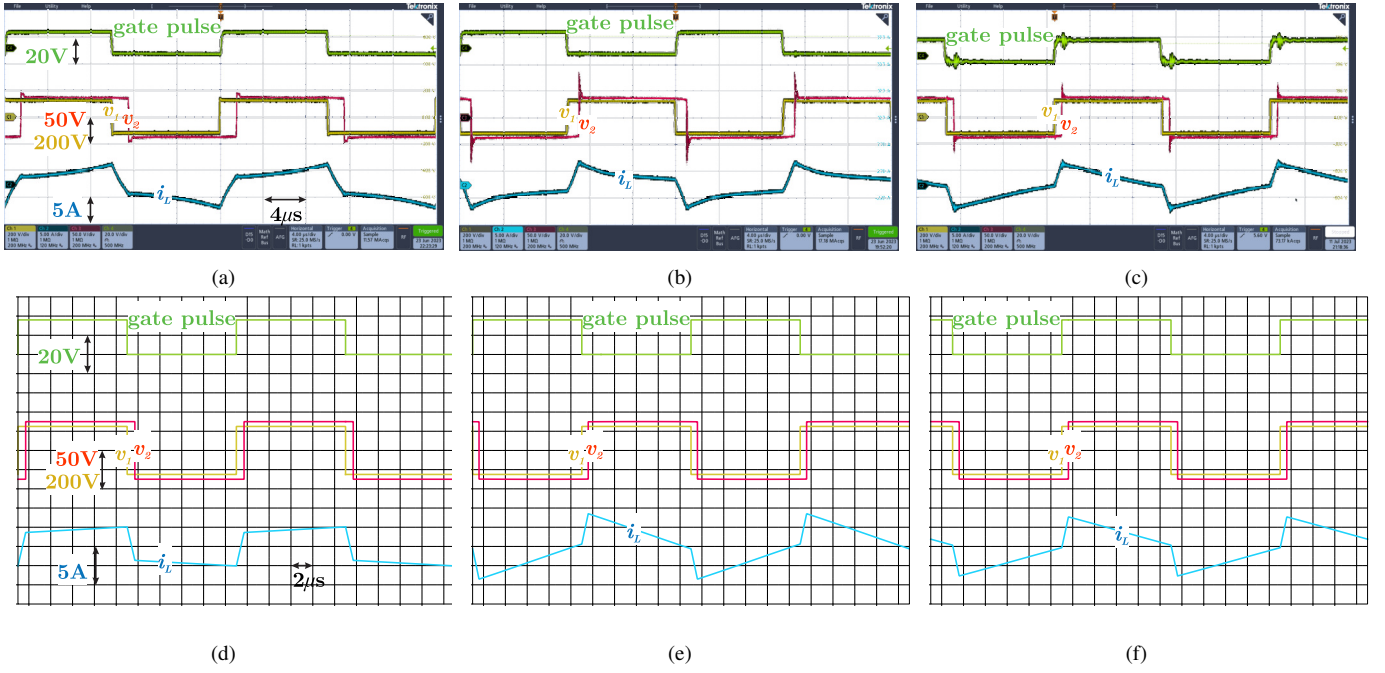


Fig. 6: DAB operating voltage in charging mode at maximum SC voltage, $v_{sc}=37.5$ V, and $P_{sc}=250$ W. Experimental waveforms for (a) Min., (b) Max., and (c) Opt. designs. Simulated waveforms for (d) Min., (e) Max., and (f) Opt. designs.

Eqs. (3) and (14) define the optimization problem for SPS modulation. The RMS current, I_{rms} , is minimized for these relations using the methodology described in section III.

V. SIMULATION AND EXPERIMENTAL RESULTS

The preceding formulation and design process are verified in circuit simulation and in experiment for SPS modulation. An SC stack interfaced to a constant-voltage DC bus is considered for verifying the proposed design methodology. The ratings of the system and the parameters of the circuit are given in Table III and Table IV, respectively.

TABLE III
RATINGS OF THE DAB INTERFACED SC

DC bus voltage, V_{dc}	125 V
Switching frequency, f_{sw}	50 kHz
SC power, P_{sc}	250 W
Support duration, Δt	1.0 s
Maximum SC voltage, V_{max}	37.5 V
Minimum SC voltage, V_{min}	31.9 V

TABLE IV
CIRCUIT PARAMETERS OF THE DAB INTERFACED SC

SC capacitance, C_{sc}	1.25 F
SC ESR, R_{ESR}	0.4 Ω
DC bus capacitance, C_{dc}	22 μ F

The design optimization procedure is executed for these ratings and parameters according to the procedure described in section III. The optimization trajectory in the design space is presented in Fig. 4a. The circuit parameters for the optimized design (Opt.) are tabulated in Table V. The parameters obtained from the conventional design technique, that matches

transformer voltages at the nominal SC condition are also tabulated. This design is designated ‘Min.’ due to its low turns ratio. Finally, the parameters obtained from an unoptimized design with the maximum (Max.) turns ratio that matches transformer voltages at the lowest SC voltage condition, are also recorded. The value of the inductance is kept the same for all designs to obtain a fair comparison and eliminate the possibility of RMS current reduction due to phase shift alone.

To compare the proposed method with existing design approaches, SC discharging as per the ratings of Table III and the capacitance parameter of the SC given in Table IV is simulated for the three designs tabulated in Table V. Simulated waveforms of the SC voltage (v_{sc}), and switching cycle RMS current ($i_{L,rms}$) are presented in Fig. 4b, with the the reduction achieved by the proposed design method evident from the $i_{L,rms}$ waveform over the discharging interval.

The designs tabulated in Table V are also realized on a hardware prototype, shown in Figs. 5a and 5b. The same 40 μ H inductor is used in the three cases. The optimized design is realized using a planar transformer, while the remaining designs are realized as litz-wire-wound transformers. The turn ratios of the wound designs are adjusted using half- or quarter-turn adjustments. The turn ratios measured in the prototype transformers are recorded in Table V. Other circuit parameters of the prototype are presented in Table IV.

The RMS currents over the charging interval of the SC obtained from analysis, simulation, and experiment are presented in Table VI. The parameter values realized in the hardware are used to evaluate the analytical and simulated values of RMS current. The improvement obtained through the

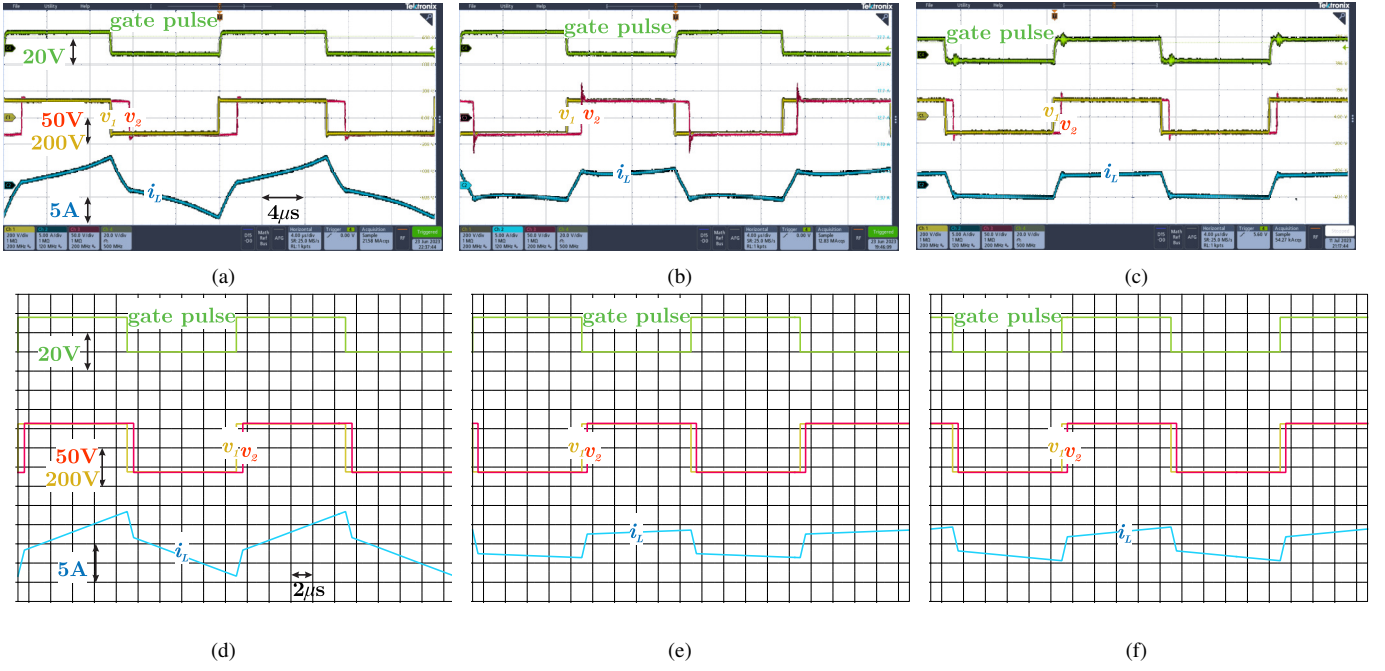


Fig. 7: DAB operating voltage in charging mode at minimum SC voltage, $v_{sc}=31.9$ V, and $P_{sc}=250$ W. Experimental waveforms for (a) Min., (b) Max., and (c) Opt. designs. Simulated waveforms for (d) Min., (e) Max., and (f) Opt. designs.

TABLE V
COMPARISON OF ANALYTICAL AND SIMULATED DAB RMS CURRENTS FOR EXISTING AND PROPOSED DESIGN METHODS

Design method	Design Outcome		Hardware Realization	
	Turns ratio, n	Inductance, L_r (μ H)	Turns ratio, n	Inductance, L_r (μ H)
Minimum turns ratio [4]–[6] (Min.)	3.33	38.5	3.25	40.0
Maximum turns ratio (Max.)	3.92		3.85	
Proposed optimization (Opt.)	3.67		3.75	

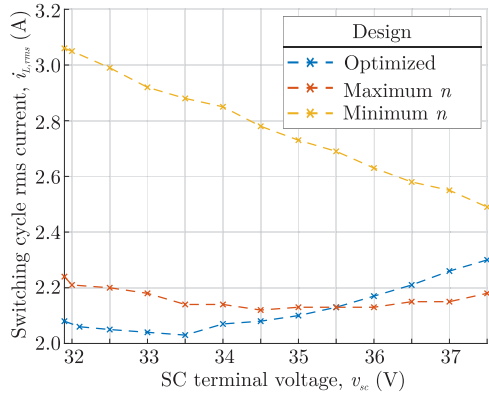


Fig. 8: Comparison of experimental switching cycle RMS currents for the optimized (Opt.), maximum turns ratio (Max.), and minimum turns ratio (Min.) designs, over the SC voltage range.

proposed design is also recorded and validates the optimization procedure. The improvement in the ‘Opt.’ design, with respect to ‘Min.’, is consistent but low due to the relatively small difference in the values of the parameters of the corresponding realized designs. The analysis and simulation agree closely, but deviate from experiment at higher values of RMS current due to the presence of non-idealities. Among these, the ESR of

the SC is a significant non-ideality. The worst-case analytical and simulated errors with respect to experiment are about 14 % and 11%, respectively.

Simulated and experimental steady-state waveforms for SC charging operation at the maximum and minimum SC voltage conditions are presented in Figs. 6 and 7, respectively. The nature of transformer primary and secondary voltage matching at each operating point is illustrated by the waveforms of the inductor current (i_L) in the respective design cases. The variation of the experimental RMS current over the entire range of SC operating voltages is presented in Fig. 8 for the three designs in Table V, demonstrating the lower RMS current in the proposed design. The closeness of parameter values results in similar RMS currents for the ‘Min.’ and ‘Opt.’ cases.

Experimental voltage and current waveforms at the SC terminals and at the DC bus are presented in Fig. 9 for the optimized design. Thus, operating the system with the optimized design satisfies the load requirements in Table III.

VI. CONCLUSION

In this paper, a design procedure for an SC interface DAB is proposed to minimize the RMS current over the charging/discharging interval. The process is developed as

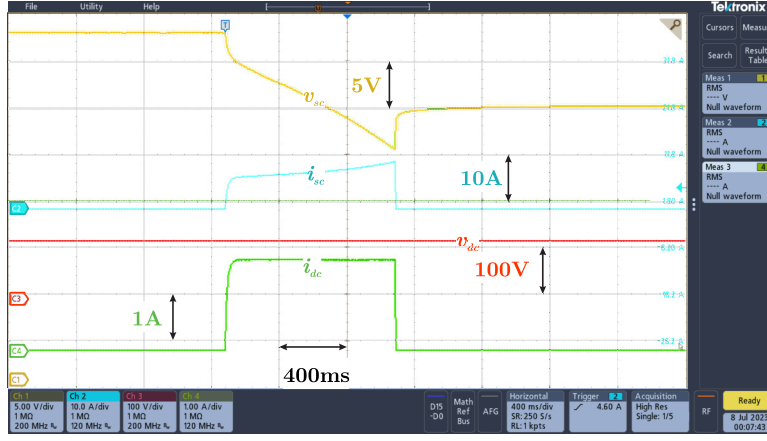


Fig. 9: Experimental waveforms illustrating SC discharging with the optimized design of the DAB to supply a 250 W load for 1 s at the DC bus.

TABLE VI

COMPARISON OF ANALYTICAL (AN.), SIMULATED (SIM.) AND EXPERIMENTAL (EXP.) DAB RMS CURRENTS FOR EXISTING (MIN.), UNOPTIMIZED (MAX.), AND PROPOSED (OPT.) DESIGN METHODS, ALONG WITH THE ERROR (ERR.) WITH RESPECT TO EXPERIMENT AND THE REDUCTION IN RMS CURRENT ACHIEVED BY THE OPTIMIZATION IN EACH CASE

Design	RMS current, I_{rms}					% reduction in Opt.		
	An. (A)	Err. (%)	Sim. (A)	Err. (%)	Exp. (A)	An.	Sim.	Exp.
Min.	2.40	14.2	2.48	11.4	2.80	12.1	13.3	24.2
Max.	2.15	0.5	2.18	0.9	2.16	1.8	1.4	1.9
Opt.	2.11	0.5	2.15	1.4	2.12	-	-	-

an optimization problem in the design parameters, namely, turns ratio and coupling inductance. A general formulation of the minimization objective is presented for an arbitrary modulation scheme. The analysis and numerical optimization are executed in detail for SPS modulation. The improvement with respect to existing design methods is verified with a reduction of 13% and 24%, respectively, in the simulated and experimental values of RMS current over the entire charging interval. The proposed design process exploits information about the SC voltage variation to select the turns ratio to minimize RMS current. The principal strengths of the process are the numerical implementation and the scope of integration with arbitrary modulation strategies.

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