Active Thermal Control and Digital Twin-based Observation of Hybrid Grids-Feeding Smart Transformers

Dissertation

zur Erlangung des akademischen Grades
Doktor der Ingenieurwissenschaften
(Dr.-Ing.)
Technische Fakultät
der Christian-Albrechts-Universität zu Kiel
vorgelegt von

***Johannes Kuprat*, M. Sc.**

aus

Neumünster
2023

Erklärung

Ich erkläre an Eides statt, dass ich die Dissertation zum Thema:

Active Thermal Control and Digital Twin-based Observation of Hybrid Grids-Feeding Smart Transformers

abgesehen von der Betreuung durch Herrn Prof. Marco Liserre selbstständig und ohne Hilfe angefertigt habe und bisher weder ganz noch zum Teil an einer anderen Stelle im Rahmen eines Prüfungsverfahrens vorgelegt, veröffentlicht oder zur Veröffentlichung eingereicht habe. Weiterhin versichere ich hiermit, dass mir kein akademischer Grad entzogen wurde, ich die vorliegende Arbeit unter Einhaltung der Regeln guter wissenschaftlicher Praxis der Deutschen Forschungsgemeinschaft angefertigt habe und alle von anderen Autoren wörtlich übernommenen Stellen, wie auch die sich an die Gedankengänge anderer Autoren eng anlehnenden Ausführungen meiner Arbeit besonders gekennzeichnet und die entsprechenden Quellen angegeben sind.

Kiel, den 22. August 2023

Johannes Kuprat

1. Gutachter:	Prof. Marco Liserre, Ph.D.
2. Gutachter:	Prof. Sibylle Dieckerhoff, Dr.-Ing.
3. Gutachter:	Prof. Maryam Saeedifard, Ph.D.
Datum der mündlichen Prüfung:	18.06.2024

To my wife Benita

Acknowledgment

I would like to thank Prof. Marco Liserre for the supervision and guidance during my doctorate. I learned a lot during the time at the Chair of Power Electronics, which finally resulted in this dissertation.

Further, I would like to thank Prof. Sibylle Dieckerhoff for reviewing my dissertation and participating in my disputation.

Additionally, I would like to thank Prof. Maryam Saeedifard for reviewing my dissertation.

Thanks to Markus and Vivek for introducing me to the scientific work in power electronics during my time as a student.

A big thanks goes to Marius for the support and all the important discussions. Also, a big thanks to Joscha for all the times we spent together in the laboratory as well as the collaborative works and discussions. Thanks to Max for the advice in hardware topics. And to all for the shared laughs and the friendship.

Thanks to Yoann, Karthik, Sante, and Ko for the joint works.

A big thanks to my family, especially my parents, who always supported me in my time as a student and in my doctorate.

In the end, a huge thanks to my wife, who always had my back during my doctorate.

Neumünster, September 2024
Johannes Kuprat

Contents

Deutsche Kurzfassung der Arbeit

Die zunehmende Integration von dezentralen erneuerbaren Energiequellen (EE) und Ladesystemen für Elektrofahrzeuge (LEF) in das Stromnetz stellt Herausforderungen für den Umgang mit hohen Schwankungen bei Erzeugung und Verbrauch dar. Der Einsatz eines hybriden Verteilungssystems - das Gleichstromnetze in die bestehende Wechselstromnetzstruktur einbettet - kann eine Integration von EE und LEF mit hohem Wirkungsgrad über Gleichstromnetze mit den etablierten Schutzmechanismen von Wechselstromnetzen kombinieren. Die Bereitstellung einer flexiblen Wechsel- und Gleichstromverteilung und möglicher Netzdienstleistungen kann durch den Smart Transformator (ST) ermöglicht werden, dies ist ein Leistungs-elektronik-basierter Transformator mit fortschrittlichen Regelungsfunktionen. Zwei Haupt-bedenken bestehen, welche die Einführung von STs für das Verteilungssystem behindern: Wirkungsgrad und Zuverlässigkeit.

Diese Arbeit trägt zur Verbesserung des Wirkungsgrades und der Zuverlässigkeit des STs bei, indem sie eine optimierte ST-Topologie für hohe Wirkungsgrade bei der Bereitstellung von hybriden Netzen vorschlägt, Konzepte digitaler Zwillinge für die Beobachtung des thermischen Verhaltens von Leistungsmodulen entwickelt und für die Unterstüzung eines zuverlässigen ST-Betriebs wesentliche Ansätze zur aktiven thermischen Regelung ausarbeitet.

Zunächst werden die Vorteile und Anforderungen von hybriden Netzen und die geeigneten ST-Architekturen vorgestellt. Außerdem werden leistungselektronische Stromrichter eingeführt, welche zur Realisierung von ST-Topologien verwendet werden.

Eine konfigurierbare ST-Topologie für einen optimalen Wirkungsgrad bei vorgegebenem hybriden Netzbetriebsprofil wird vorgeschlagen. Es werden ein auf Betriebsprofilen basierendes Entwurfsverfahren für die Stromrichterleistungen und die Möglichkeit zur konfigurationsbedingten Verkleinerung des Vermaschungsstromrichters vorgestellt.

Leistungshalbleiter gehören zu den fehleranfälligsten Komponenten in leistungselektronischen Systemen. Ihr thermisches Verhalten ist ein Faktor, der zur Überwachung ihres Gesundheitszustandes herangezogen werden kann. Daher sind thermische Echtzeitmodelle, deren Parameter auf der Grundlage des Vergleichs von geschätzten Temperaturen mit Mess-ungen am physischen System optimiert werden, - thermische Digitale Zwillinge - von Vorteil. In dieser Arbeit werden zwei Ansätze entwickelt, die auf einer Partikel-Schwarm-Optimier-ung und einem dualen erweiterten Kalman-Filter basieren.

Die Reduzierung und Verlagerung der thermischen Belastung von Leistungshalbleitern durch aktive thermische Regelung (ATR) kann einen zuverlässigen ST-Betrieb unterstützen. Diese Arbeit gibt einen Überblick über ATR-Methoden und geht auf zwei für den ST wesentliche Methoden ein - Graphentheorie-basierte Leistungsverteilung und diskontinuierliche Modulation. Außerdem wird vorgeschlagen, die geringere Stromrichterbelastung in der vermaschten ST-Topologie für zusätzliche Fehlertoleranz zu nutzen.

English Summary

The increasing integration of distributed renewable energy sources (RES) and electric vehicle (EV) charging systems into the electricity grid poses challenges in handling high generation and demand variability. The utilization of a hybrid distribution system - which embeds dc grids inside the existing ac grid structure - could combine an efficient integration of RES and EV charging stations via dc grids with the established protection mechanisms of ac grids. The provision of a flexible ac and dc distribution and further possible grid services can be enabled by the Smart Transformer (ST), which is a power electronics-based transformer with advanced control functionalities. However, two major concerns impeding the adoption of STs for the distribution system are the efficiency and reliability.

This work contributes to the advancement of efficiency and reliability in the ST by proposing an optimized ST topology for efficiently establishing hybrid grids, developing digital twin approaches for observing the thermal behavior of power modules, and elaborating on active thermal control approaches essential to support a reliable ST operation.

The advantages and requirements of hybrid grids and the suitable ST architectures are presented as a first step. Further, power electronics converters to realize ST topologies based on these architectures are introduced.

Based on these fundamentals, an interconnected ST topology whose configuration can be adjusted to provide optimized efficiency for a hybrid grid mission profile is proposed. Furthermore, a mission profile-based design procedure for the converter power ratings in the proposed topology is presented and the opportunity for downsizing the interconnecting converter based on the configuration revealed.

Power semiconductors are among the components most prone to failure in power electronics systems. Their thermal behavior is one factor which can be used to monitor their health condition. Therefore, thermal digital real time models whose parameters are optimized based on the comparison of estimated temperatures with measurements on the physical system - thermal digital twins - are advantageous. This work develops two approaches based on a particle swarm optimization and a dual extended Kalman filter.

Reducing and relocating the thermal stress on power semiconductors via active thermal control (ATC) can support a reliable ST operation. This work gives an overview on ATC methods and elaborates on two essential ones for the ST - graph theory-based power routing and discontinuous modulation. Further, utilizing the lower converter loading in the interconnected ST topology for additional failure tolerance is proposed.

Used symbols and abbreviations

General symbols

General notations

$x(t), x$	Time-variant variable
$x(y)$	Variable x depends on variable y
$f(y)$	Function that depends on variable y
$\boldsymbol{x}$, $\boldsymbol{X}$	Vector or matrix
$\bar{x}$	Average value
$\hat{x}$	Estimated value
$\dot{x}$	Time derivative
$P_{j,k}$	Power flow from node j to node k in a directed graph
$W_{j,k}$	Weight of the arc from node j to node k in a directed graph
(j,k)	Arc originating in node j and ending in node k in a directed graph
$(P_{\mathrm{LVac}}\, P_{\mathrm{LVdc}})$	Hybrid grid operation point

Superscripts

$*$	Indicates reference variables
$'$	Indicates compensated variables
$+$	Indicates variables after the correction step in a Kalman filter
$-$	Indicates variables before the correction step in a Kalman filter
conv	Indicates variables that converged to a steady value
CS	Indicates variables referring to a current source
DAB	Indicates variables referring to a dual active bridge
filt	Indicates variables that a smoothing filter was applied to
graphic	Indicates variables referring to a graphical representation
max	Maximum value
max, graphic	Maximum value that can be read from the graphical representation
min	Minimum value

Subscripts

a	Index of variables referring to an ambient condition
ac	Index of variables referring to an alternating current

ac, rms, ph	Index of variables referring to a root mean square alternating current value between line and neutral conductor
amp	Index of variables referring to an amplitude value
aux	Index of auxiliary variables for case distinction
AWE	Index of variables referring to the average weighted system efficiency
block	Index of variables referring to the blocking state of a semiconductor
block, ref	Index of variables referring to a reference value of the blocking state of a semiconductor
buck	Index of variables referring to a buck converter
c	Index of variables referring to the collector
cauer	Index of variables referring to a Cauer network
cc	Maximum value at the collector
ce	Index of variables between collector and emitter
cell	Index of variables referring to one cell of a cascaded H-bridge
ce(sat)	Saturation value between collector and emitter
CHB	Index of variables referring to a cascaded H-bridge
CHB, dc	Index of variables referring to a direct current value of a cascaded H-bridge
CHB, ph	Index of variables referring to one phase of a cascaded H-bridge
CHB, rms	Index of variables referring to a root mean square value of a cascaded H-bridge
CHB, rms, fund	Index of variables referring to a root mean square value at fundamental frequency of a cascaded H-bridge
chip	Index of variables referring to a chip of a power semiconductor module
cl	Index of variables referring to the clamped operated cell of a cascaded H-bridge
cl, 1st	Index of variables referring to the clamped operated cell of a cascaded H-bridge for first harmonic clamped modulation method
cl, 3rd	Index of variables referring to the clamped operated cell of a cascaded H-bridge for third harmonic clamped modulation method
CoM	Index of variables referring to the center of the mission profile
con	Index of variables referring to the conduction
con, diode	Index of variables referring to the conduction of a diode
con, IGBT	Index of variables referring to the conduction of an insulated gate bipolar transistor
cond, pri	Index of variables referring to the conductor on the primary side of a transformer
cond, sec	Index of variables referring to the conductor on the secondary side of a transformer
core	Index of variables referring to the core of a transformer

core, win	Index of variables referring to a transformer core window
cr	Index of variables referring to a cross section
CS, in	Index of variables referring to the virtual input of a current source
CS, out	Index of variables referring to the output of a current source
C_{th}	Index of variables referring to a thermal capacitor
Cu	Index of variables referring to copper
Cu, pri	Index of variables referring to copper on the primary side of a transformer
Cu, sec	Index of variables referring to copper on the secondary side of a transformer
d	Index of variables referring to the damping part of a controller
D	Index of variables referring to a diode
DAB	Index of variables referring to a dual active bridge
DAB, NIT	Index of variables referring to the low voltage direct current dual active bridge in the non-interconnected topology
DAB, in	Index of variables referring to the input of a dual active bridge
DAB, IT	Index of variables referring to the interconnecting dual active bridge in the interconnected topology
DAB, out	Index of variables referring to the output of a dual active bridge
dc	Index of variables referring to a direct current
dc − link	Index of variables referring to the direct current-link
dia	Index of variables referring to a diameter
exe	Index of variables referring to the execution of an electrical simulation
f	Index of variables referring to the failure of a device
g	Index of variables referring to a grid
ge	Index of variables between gate and emitter
ge(th)	Threshold value between gate and emitter
gg	Maximum value at the gate
i	Index of variables referring to the interconnecting dual active bridge
icl	Index of variables referring to the inverse clamped operated cell of a cascaded H-bridge
icl, 1st	Index of variables referring to the inverse clamped operated cell of a cascaded H-bridge for first harmonic clamped modulation method
icl, 3rd	Index of variables referring to the inverse clamped operated cell of a cascaded H-bridge for third harmonic clamped modulation method
in	Index of variables referring to the input of a system
inv	Index of variables referring to an inverter
j	Index of variables referring to the junction of a transistor
L	Index of variables referring to an inductor
L_{buck}	Index of variables referring to the inductance of a buck converter

link	Index of variables referring to a link between converters
load	Index of variables referring to a load
load, rms	Index of variables referring to a root mean square value of a load
loss	Index of variables referring to losses
loss, const	Index of variables referring to constant losses
loss, core	Index of variables referring to transformer core losses
loss, Cu, pri	Index of variables referring to copper losses on the primary side of a transformer
loss, Cu, sec	Index of variables referring to copper losses on the secondary side of a transformer
loss, interDAB	Index of variables referring to the losses of the interconnecting dual active bridge
loss, inv	Index of variables referring to the losses of the inverter
loss, PEBB, $1-\xi$	Index of variables referring to the losses of medium voltage alternating current power electronics building blocks connected to the direct current-link
loss, PEBB, ξ	Index of variables referring to the losses of medium voltage alternating current power electronics building blocks connected to the low voltage direct current feeder
loss, rr	Index of variables referring to reverse recovery losses of a diode
loss, sw	Index of variables referring to switching losses of an insulated gate bipolar transistor
LVac	Index of variables referring to a low voltage alternating current grid
LVac, CoM	Index of variables referring the low voltage alternating current grid part of the center of the mission profile
LVdc	Index of variables referring to a low voltage direct current grid
LVdc, CoM	Index of variables referring the low voltage direct current grid part of the center of the mission profile
max	Maximum value
MB	Index of variables referring to the multibus
MB, dc − link	Index of variables referring to the multibus cells connected to the direct current-link
MB, LVdc	Index of variables referring to the multibus cells connected to the low voltage direct current feeder
mc	Index of variables referring to a multichip version of the dual extended Kalman filter based thermal digital twin
meas	Index of variables referring to measurements
min	Minimum value
MVac	Index of variables referring to the medium voltage alternating current grid

MVac, PEBB	Index of variables referring to a medium voltage alternating current power electronics building block
n	Index of variables referring to a normally operated cell of a cascaded H-bridge
obj	Index of variables referring to an objective
obj, best	Index of variables referring to a best value for an objective
obj, ref	Index of variables referring to a reference objective
off	Index of variables referring to the turn-off of a transistor
on	Index of variables referring to the turn-on of a transistor
op, DEKF	Index of variables referring to the mathematical operations in a dual extended Kalman filter
op, PSO	Index of variables referring to the mathematical operations in the particle-swarm-optimization
opt	Index of variables referring result of an optimization
out	Index of variables referring to the output of a system
P	Index of variables referring to proportional part of a controller
ph	Index of variables referring to one phase of an inverter
	grid
pri	Index of variables referring to the primary side of a transformer
pri, rms	Index of variables referring to a root mean square value on the primary side of a transformer
pri, rms, max	Index of variables referring to a maximum root mean square value on the primary side of a transformer
pk	Peak value
PSO	Index of variables referring to the particle-swarm-optimization
PSO, best	Index of variables referring to best values in the particle-swarm-optimization
PSO, d	Index of variables referring to derivative in the particle-swarm-optimization
r	Index of variables referring to rising behavior
R	Index of variables referring to a resistor
rated	Index of variables referring to a rating
ref	Reference variable index
res	Index of variables referring to the resonant part of a controller
rr	Index of variables referring to the reverse recovery of a diode
s	Index of variables referring to a source
sec	Index of variables referring to the secondary side of a transformer
sec, rms	Index of variables referring to a root mean square value on the secondary side of a transformer
sec, rms, max	Index of variables referring to a maximum root mean square value on

	the secondary side of a transformer
stm	Index of variables referring to the Steinmetz equation
sw	Index of variables referring to the switching of transistors
sw, CHB	Index of variables referring to the switching of transistors in a cascaded H-bridge
sw, DAB	Index of variables referring to the switching of transistors in a dual active bridge
sys	Index of variables referring to the whole system
sys, in	Index of variables referring to the total input of a system
sys, loss	Index of variables referring to the total losses of a system
sys, loss, FCC	Index of variables referring to the total losses of a system calculated assuming the flow conservation constraint
sys, loss, NCF	Index of variables referring to the total losses of a system calculated with non-conserved flows
sys, loss, rel	Index of variables referring to the relative difference between total losses of a system calculated under consideration of the flow conservation constraint and without it
sys, out	Index of variables referring to the total output of a system
T	Index of variables referring to a transistor
th	Index of variables referring to the thermal behavior
th, cr	Index of variables referring to the thermal cross coupling effect
winding	Index of variables referring to a winding
0	Index of variables referring to base value
$1-\xi$	Index of variables referring to the counterpart of the link ratio

Special symbols

a	Running index
A	Set of arcs of a directed graph
$A_{\text{cond,pri}}$	Cross section of the conductor on the primary side of a transformer
$A_{\text{cond,sec}}$	Cross section of the conductor on the secondary side of a transformer
$A_{\text{core,win}}$	Area of one window in a transformer core
A_{cr}	Cross sectional area of a transformer core
b	Running index
B	Running index
b_{dia}	Diameter of a bond wire
B_{pk}	Peak value of the magnetic flux density of the transformer core material without saturation

B_{PSO}	Number of particles in the particle-swarm-optimization
c	Coefficient in a formula
C	Electrical capacitance
C_{cell}	Electrical capacitance of one cell of a cascaded H-bridge
$C_{\mathrm{DAB,in}}$	Electrical input capacitance of a dual active bridge
$C_{\mathrm{DAB,out}}$	Electrical output capacitance of a dual active bridge
$C_{\mathrm{dc-link}}$	Electrical direct current-link capacitance
c_{form}	Coefficient which describes the impact of the applied electrical waveforms on the saturation of the transformer core
C_{LVdc}	Electrical low voltage direct current grid capacitance
c_{PSO}	Coefficient in the particle-swarm-optimization
$c_{\mathrm{PSO,d}}$	Weighting coefficient of the derivative part of the objective function in the particle-swarm-optimization
c_{stm}	Coefficient of the Steinmetz equation
C_{th}	Thermal capacitance
$\hat{C}_{\mathrm{th}}$	Estimated thermal capacitance
$\hat{C}_{\mathrm{th}}^{\mathrm{conv}}$	Estimated thermal capacitance that converged to a steady value
D	Dual active bridge duty cycle
D_{buck}	Buck converter duty cycle
d_{exe}	Electrical simulation time step
d_{PSO}	Particle-swarm-optimization execution time step
d_{th}	Thermal simulation time step
$\boldsymbol{E}$	Identity matrix
E_{off}	Energy converted to heat during one turn-off of an insulated gate bipolar transistor
E_{on}	Energy converted to heat during one turn-on of an insulated gate bipolar transistor
E_{rr}	Energy converted to heat during one reverse recovery of a diode
f	Frequency
$\boldsymbol{F}$	Jacobian matrix of system state functions
$\boldsymbol{f}(\boldsymbol{x},\boldsymbol{u})$	System state functions
f_{ac}	Alternating current fundamental frequency
$\boldsymbol{F}_{\mathrm{mc}}$	Jacobian matrix of system state functions of the multichip version of the dual extended Kalman filter based thermal digital twin
f_{obj}	Objective function
$f_{\mathrm{obj,best}}$	Best achieved objective function value
$f_{\mathrm{obj,ref}}$	Reference objective function
f_{ref}	Reference frequency
f_{sw}	Switching frequency of transistors
$f_{\mathrm{sw,CHB}}$	Switching frequency of transistors in a cascaded H-bridge

$f_{\mathrm{sw,DAB}}$	Switching frequency of transistors in a dual active bridge
G	Directed graph
G_{DAB}	Voltage gain of a dual active bridge
$\boldsymbol{H}$	Jacobian matrix of system output functions
$\boldsymbol{h}(\boldsymbol{x})$	System output functions
$h_{\mathrm{core,win}}$	Height of a core window
i	Alternating current
I	Direct current
$\hat{i}$	Estimated alternating current
i^*	Alternating reference current
I^*_{amp}	Alternating reference current amplitude
I_{amp}	Amplitude of an alternating current
i_{c}	Collector current
i_{D}	Diode current
i_{L}	Inductor current
$i_{L_{\mathrm{buck}}}$	Current of the inductance of a buck converter
I_{load}	Constant load current
$I_{\mathrm{load,rms}}$	Root mean square current of a load
i_{ph}	Phase current
i_{pri}	Primary side current of a transformer
$I_{\mathrm{pri,rms}}$	Root mean square current on the primary side of a transformer
$I_{\mathrm{pri,rms,max}}$	Maximum root mean square current on the primary side of a transformer
i_{sec}	Secondary side current of a transformer
$I_{\mathrm{sec,rms}}$	Root mean square current on the secondary side of a transformer
$I_{\mathrm{sec,rms,max}}$	Maximum root mean square current on the secondary side of a transformer
i_{T}	Transistor current
j	Running index
k	Running index
$\boldsymbol{K}$	Kalman gain in a Kalman filter
K_{d}	Damping gain of a controller
K_{P}	Proportional gain of a controller
K_{res}	Resonant gain of a controller
L	Inductance
L_{buck}	Buck converter inductance
L_{DAB}	Dual active bridge inductance
L_{g}	Grid inductance
l_{pri}	Length of the conductor on the primary side of a transformer
$\boldsymbol{l}_{\mathrm{PSO,best}}$	Locally best set of parameters of neighbor particles in the particle-swarm-optimization

l_{sec}	Length of the conductor on the secondary side of a transformer
M	Set of operation points of a hybrid grid mission profile
m	Modulation signal
m_{CHB}	Modulation signal of a cascaded H-bridge
m_{cell}	Modulation signal a cell of a cascaded H-bridge
m_{cl}	Modulation signal of the clamped operated cell of a cascaded H-bridge
$m_{\mathrm{cl,1st}}$	Modulation signal of the clamped operated cell of a cascaded H-bridge for first harmonic clamped modulation method
$m_{\mathrm{cl,3rd}}$	Modulation signal of the clamped operated cell of a cascaded H-bridge for third harmonic clamped modulation method
m_{icl}	Modulation signal of the inverse clamped operated cell of a cascaded H-bridge
$m_{\mathrm{icl,1st}}$	Modulation signal of the inverse clamped operated cell of a cascaded H-bridge for first harmonic clamped modulation method
$m_{\mathrm{icl,3rd}}$	Modulation signal of the inverse clamped operated cell of a cascaded H-bridge for third harmonic clamped modulation method
m_{n}	Modulation signal of a normally operated cell of a cascaded H-bridge
M_{n}	Amplitude modulation ratio of a normally operated cell of a cascaded H-bridge
n	Turns ratio of a transformer
n_{f}	Counted number of cycles for specific thermal cycle
N	Set of nodes of a directed graph
N_{cauer}	Number of chain elements of a Cauer network
N_{CHB}	Number of cells in one phase of a cascaded H-bridge
N_{f}	Number of cycles to the failure of a device
N_{MB}	Number of multibus cells in one phase
$N_{\mathrm{MB,dc-link}}$	Number of multibus cells connected to the direct current-link
$N^{\mathrm{CS}}_{\mathrm{MB,dc-link}}$	Number of multibus cells connected to the direct current-link emulated by current sources in the laboratory
$N^{\mathrm{DAB}}_{\mathrm{MB,dc-link}}$	Number of multibus cells connected to the direct current-link realized by dual active bridges in the laboratory
$N_{\mathrm{MB,LVdc}}$	Number of multibus cells connected to the low voltage direct current feeder
$N^{\mathrm{CS}}_{\mathrm{MB,LVdc}}$	Number of multibus cells connected to the low voltage direct current feeder emulated by current sources in the laboratory
$N^{\mathrm{DAB}}_{\mathrm{MB,LVdc}}$	Number of multibus cells connected to the low voltage direct current feeder realized by dual active bridges in the laboratory
$N_{\mathrm{op,DEKF}}$	Number of mathematical operations in a dual extended Kalman filter
$N_{\mathrm{op,PSO}}$	Number of mathematical operations in the particle-swarm-optimization
N_{pri}	Number of windings on the primary side of a transformer

N_{sec}	Number of windings on the secondary side of a transformer
$N_{\hat{\boldsymbol{x}}}$	Number of states and estimated parameters in a dual extended Kalman filter
$N_{\boldsymbol{y}}$	Number of chip temperature measurements on the physical system in a thermal digital twin
$\boldsymbol{O}^{-}$	Estimated error covariance matrix before the correction step in a Kalman filter
$\boldsymbol{O}^{+}$	Estimated error covariance matrix after the correction step in a Kalman filter
P	Power flow
P_{aux}	Auxiliary variable for case distinction
$\bar{P}_{\mathrm{cell}}$	Average power processed by one cell of a cascaded H-bridge
$P_{\mathrm{CHB,ph}}$	Power processed in one phase of a cascaded H-bridge
P_{con}	Conduction power losses
$\bar{P}_{\mathrm{con,diode}}$	Average conduction losses of a diode
$\bar{P}_{\mathrm{con,IGBT}}$	Average conduction losses of an insulated gate bipolar transistor
$P_{\mathrm{CS,in}}$	Virtual input power of a current source
$P'_{\mathrm{CS,in}}$	Compensated virtual input power of a current source
$P_{\mathrm{CS,out}}$	Output power of a current source
$\bar{P}_{\mathrm{DAB}}$	Average power processed by a dual active bridge
$P_{\mathrm{DAB,in}}$	Input power of a dual active bridge
$P'_{\mathrm{DAB,in}}$	Compensated input power of a dual active bridge
$P_{\mathrm{DAB,IT}}$	Power of the interconnecting dual active bridge in the interconnected topology
$P_{\mathrm{DAB,IT}}^{\mathrm{graphic}}$	Power of the interconnecting dual active bridge in the interconnected topology that can be read from the low voltage power plane
$P_{\mathrm{DAB,IT}}^{\mathrm{max}}$	Maximum power of the interconnecting dual active bridge in the interconnected topology
$P_{\mathrm{DAB,IT}}^{\mathrm{max,graphic}}$	Maximum power of the interconnecting dual active bridge in the interconnected topology that can be read from the low voltage power plane
$P_{\mathrm{DAB,NIT}}^{\mathrm{max}}$	Maximum power of the low voltage direct current dual active bridge in the non-interconnected topology
$P_{\mathrm{DAB,out}}$	Output power of a dual active bridge
P_{in}	Input power of a system
$P_{\mathrm{inv}}^{\mathrm{max}}$	Maximum power of the inverter
P_{loss}	Power losses
$\boldsymbol{P}_{\mathrm{loss}}$	Power losses vector
$\hat{P}_{\mathrm{loss}}$	Estimated power losses
$P_{\mathrm{loss,const}}$	Constant power losses

$P_{\text{loss,core}}$	Transformer core losses
$P_{\text{loss,Cu,pri}}$	Copper losses of the conductor on the primary side of a transformer
$P_{\text{loss,Cu,sec}}$	Copper losses of the conductor on the secondary side of a transformer
$P_{\text{loss,interDAB}}$	Power losses of the interconnecting dual active bridge
$P_{\text{loss,inv}}$	Power losses of the inverter
$P_{\text{loss,PEBB},1-\xi}$	Power losses of medium voltage alternating current power electronics building blocks connected to the direct current-link
$P_{\text{loss,PEBB},\xi}$	Power losses of medium voltage alternating current power electronics building blocks connected to the low voltage direct current feeder
$\bar{P}_{\text{loss,rr}}$	Average reverse recovery losses of a diode
$\bar{P}_{\text{loss,sw}}$	Average switching losses of an insulated gate bipolar transistor
P_{LVac}	Active power of the low voltage alternating current grid
$P_{\text{LVac}}^{\text{max}}$	Maximum active power of the low voltage alternating current grid
$P_{\text{LVac,CoM}}$	Low voltage alternating current active power at the center of the mission profile
P_{LVdc}	Power of the low voltage direct current grid
$P_{\text{LVdc}}^{\text{max}}$	Maximum power of the low voltage direct current grid
$P_{\text{LVdc,CoM}}$	Low voltage direct current power at the center of the mission profile
P_{MVac}	Active power of the medium voltage alternating current grid
$P_{\text{MVac,PEBB}}^{\text{max}}$	Maximum power of one medium voltage alternating current power electronics building block
P_{out}	Output power of a system
P_{ph}	Power processed by one phase of an inverter
$\boldsymbol{p}_{\text{PSO}}$	Set of parameters of a particle in the particle-swarm-optimization
$\boldsymbol{p}_{\text{PSO,best}}$	Set of parameters of a particle in the particle-swarm-optimization which achieved a best objective function value of the particle
P_{R}	Power consumed by a resistor
P_{rated}	Rated power of a converter
$P_{\text{sys,in}}$	Total input power of a system
$P_{\text{sys,loss}}$	Total power losses of a system
$P_{\text{sys,loss,FCC}}$	Total power losses of a system calculated assuming the flow conservation constraint
$P_{\text{sys,loss,NCF}}$	Total power losses of a system calculated with non-conserved flows
$P_{\text{sys,out}}$	Total output power of a system
$\boldsymbol{Q}$	Noise covariance matrix of the system states in a Kalman filter
$Q_{\hat{C}_{\text{th}}}$	Entry of the noise covariance matrix of the system states in a Kalman filter for an estimated thermal capacitance
$\boldsymbol{Q}_{\text{mc}}$	Noise covariance matrix of the system states in the multichip version of the dual extended Kalman filter based thermal digital twin
$Q_{\text{mc},\hat{C}_{\text{th}}}$	Entry of the noise covariance matrix of the system states in the multichip

	version of the dual extended Kalman filter based thermal digital twin for an estimated thermal capacitance
$Q_{\mathrm{mc},\hat{R}_{\mathrm{th}}}$	Entry of the noise covariance matrix of the system states in the multichip version of the dual extended Kalman filter based thermal digital twin for an estimated thermal resistance
$Q_{\mathrm{mc},\hat{R}_{\mathrm{th,cr}}}$	Entry of the noise covariance matrix of the system states in the multichip version of the dual extended Kalman filter based thermal digital twin for an estimated thermal resistance which models a thermal cross coupling effect
$Q_{\mathrm{mc},\hat{T}}$	Entry of the noise covariance matrix of the system states in the multichip version of the dual extended Kalman filter based thermal digital twin for an estimated temperature
$Q_{\mathrm{mc},\hat{T}_{\mathrm{chip}}}$	Entry of the noise covariance matrix of the system states in the multichip version of the dual extended Kalman filter based thermal digital twin for an estimated chip temperature
$Q_{\hat{R}_{\mathrm{th}}}$	Entry of the noise covariance matrix of the system states in a Kalman filter for an estimated thermal resistance
$Q_{\hat{R}_{\mathrm{th,cr}}}$	Entry of the noise covariance matrix of the system states in a Kalman filter for an estimated thermal resistance which models a thermal cross coupling effect
$Q_{\hat{T}}$	Entry of the noise covariance matrix of the system states in a Kalman filter for an estimated temperature
$Q_{\hat{T}_{\mathrm{chip}}}$	Entry of the noise covariance matrix of the system states in a Kalman filter for an estimated chip temperature
R	Electrical resistance
R_{ac}	Electrical alternating current resistance
R_{cell}	Electrical load resistance of one cell of a cascaded H-bridge
$R_{\mathrm{Cu,pri}}$	Resistance of conductor copper on the primary side of a transformer
$R_{\mathrm{Cu,sec}}$	Resistance of conductor copper on the secondary side of a transformer
R_{dc}	Electrical alternating current resistance
R_{load}	Electrical load resistance
r_{PSO}	Randomly generated number in the particle-swarm-optimization
R_{th}	Thermal resistance
$\hat{R}_{\mathrm{th}}$	Estimated thermal resistance
$\hat{R}_{\mathrm{th}}^{\mathrm{conv}}$	Estimated thermal resistance that converged to a steady value
$R_{\mathrm{th,cr}}$	Thermal resistance modeling a thermal cross coupling effect
$\hat{R}_{\mathrm{th,cr}}$	Estimated thermal resistance modeling a thermal cross coupling effect
r_{winding}	Radius of a winding
s	Variable of the Laplace transformation

$\boldsymbol{S}$	Noise covariance matrix of the measurements in a Kalman filter
$\boldsymbol{s}_{\text{meas}}$	Measurement noise
$S_{T_{\text{chip}}}$	Entry of noise covariance matrix of the measurements in a Kalman filter for a chip temperature
t	Time
t_{r}	Time of the temperature rise (heating time)
T	Temperature
$\hat{T}$	Estimated temperature
$\hat{\boldsymbol{T}}$	Vector of estimated temperatures
T_{a}	Ambient temperature
T_{chip}	Chip temperature
$\hat{T}_{\text{chip}}$	Estimated chip temperature
$T_{C_{\text{th}}}$	Temperature of a thermal capacitor
T_{j}	Junction temperature
$\bar{T}_{\text{j}}$	Average junction temperature
$T_{\text{j}}^{\text{max}}$	Maximum junction temperature
$T_{\text{j}}^{\text{min}}$	Minimum junction temperature
$\bar{T}_{\text{j}}$	Average junction temperature
$T_{\text{j}}^{\text{max}}$	Maximum junction temperature
$T_{\text{j}}^{\text{min}}$	Minimum junction temperature
T_{ref}	Reference temperature
$\boldsymbol{T}_{\text{ref}}$	Reference temperature vector
$\boldsymbol{u}$	Inputs of a system
$\boldsymbol{u}_{\text{mc}}$	Inputs of the multichip version of the dual extended Kalman filter based thermal digital twin
v	Voltage
$\hat{v}$	Estimated voltage
v_{ac}	Alternating current voltage, grid voltage
$V_{\text{ac,rms,ph}}$	Root mean square alternating current voltage between line and neutral conductor
V_{block}	Blocking state voltage of a semiconductor
$V_{\text{block,ref}}$	Reference value of the blocking state voltage of a semiconductor
V_{cc}	Voltage between collector and emitter in blocking state
v_{ce}	Voltage between collector and emitter
v_{cell}	Alternating current voltage of one cell of a cascaded H-bridge
$V_{\text{ce(sat)}}$	Saturation voltage between collector and emitter
v_{CHB}	Alternating current voltage of a cascaded H-bridge
$V_{\text{CHB,dc}}$	Direct current part of the alternating current voltage of a cascaded H-bridge
$V_{\text{CHB,rms}}$	Root mean square of the alternating current voltage of a cascaded

	H-bridge
$V_{\mathrm{CHB,rms,fund}}$	Root mean square of the alternating voltage at fundamental frequency of a cascaded H-bridge
V_{core}	Volume of the core of a transformer
v_{D}	Forward voltage of a diode
V_{dc}	Direct current voltage
V_{dc}^{*}	Direct current reference voltage
$V_{\mathrm{dc}}^{\mathrm{filt}}$	Direct current voltage that a smoothing filter has been applied to
$V_{\mathrm{dc-link}}$	Direct current-link voltage
$V_{\mathrm{dc-link}}^{*}$	Direct current-link reference voltage
v_{ge}	Voltage between gate and emitter
$V_{\mathrm{ge(th)}}$	Threshold voltage between gate and emitter
V_{gg}	Designed operation voltage between gate and emitter
V_{in}	Input direct current voltage
v_{L}	Inductor voltage
$v_{L_{\mathrm{buck}}}$	Voltage of the inductance of a buck converter
$v_{L_{\mathrm{DAB}}}$	Voltage of the inductance of a dual active bridge converter
V_{link}	Direct current voltage of a link between converters
V_{load}	Direct current load voltage
V_{LVdc}	Low voltage direct current grid voltage
V_{LVdc}^{*}	Low voltage direct current grid reference voltage
V_{out}	Output direct current voltage
V_{pri}	Root mean square voltage on the primary side of a transformer
$\boldsymbol{v}_{\mathrm{PSO}}$	Set of parameter velocities of a particle in the particle-swarm-optimization
V_{rated}	Rated voltage of semiconductor
v_{ref}	Reference voltage
V_{s}	Voltage of a direct current source
V_{sec}	Root mean square voltage on the secondary side of a transformer
W	Set of weights of the arcs in a directed graph
$\boldsymbol{w}$	Process noise
$w_{\mathrm{core,win}}$	Width of a core window
$\boldsymbol{x}$	States of a system
$\boldsymbol{x}_0$	Initial states of a system
$\hat{\boldsymbol{x}}$	Estimated states of a system
$\hat{\boldsymbol{x}}_{\mathrm{mc}}$	Estimated states of the multichip version of the dual extended Kalman filter based thermal digital twin
$\hat{\boldsymbol{x}}^{-}$	Estimated states of a system before the correction step in a Kalman filter
$\hat{\boldsymbol{x}}^{+}$	Estimated states of a system after the correction step in a Kalman filter
$\boldsymbol{y}$	Outputs of a system

$\hat{\boldsymbol{y}}$	Estimated outputs of a system
$\hat{\boldsymbol{y}}_{\mathrm{mc}}$	Estimated outputs of the multichip version of the dual extended Kalman filter based thermal digital twin
Z_{th}	Thermal impedance
$\dot{Z}_{\mathrm{th}}$	Time derivative of the thermal impedance
$\dot{\boldsymbol{Z}}_{\mathrm{th}}$	Time derivative of the thermal impedance matrix
α	Unspecific angle
γ	Distortion factor of the coordinate transformation in the low voltage power plane by the link ratio for the interconnected topology
$\Delta P_{\mathrm{sys,loss,rel}}$	Relative difference between total power losses of a system calculated under consideration of the flow conservation constraint and without it
ΔT	Temperature difference
ΔT_{j}	Junction temperature swing
η	Efficiency
η_{DAB}	Efficiency of a dual active bridge
$\eta_{j,\mathrm{b}}$	Efficiency for backward power flow in a converter described by node j in a directed graph
$\eta_{j,\mathrm{f}}$	Efficiency for forward power flow in a converter described by node j in a directed graph
η_{sys}	Efficiency of the whole system
$\bar{\eta}_{\mathrm{sys}}$	Average weighted efficiency of the whole system
ϑ	Angle in a periodic signal
ξ	Link ratio of the interconnected topology
ξ_{AWE}	Link ratio chosen according to the average weighted system efficiency
ξ_{CoM}	Link ratio chosen according to the location of the center of the mission profile
ξ_{opt}	Link ratio of the interconnected topology to provide optimal efficiency
ρ_{Cu}	Specific resistance of copper
τ	Specific time period
τ_{th}	Thermal time constant
ϕ	Clamping angle
φ	Phase shift of a dual active bridge
φ_{i}	Phase shift of the interconnecting dual active bridge
φ_{LVac}	Phase shift between voltage and current in a low voltage alternating current grid
φ_{MVac}	Phase shift between voltage and current in a medium voltage alternating current grid
$\varphi_{1-\xi}$	Angle in the low voltage power plane connected to the counterpart of the link ratio
ω	Angular frequency

ω_0	Base angular frequency
ω_g	Grid angular frequency
ω_{PSO}	Inertia weight in the particle-swarm-optimization

Abbreviations

ac	Alternating current
ATC	Active thermal control
ATR	Aktive thermische Regelung
AWE	Average weighted system efficiency
BESS	Battery energy storage system
c	Converter node in a directed graph
CHB	Cascaded H-bridge
CM	Condition monitoring
CoM	Center of the mission profile
CTE	Coefficient of thermal expansion
D	Diode
DAB	Dual active bridge
dc	Direct current
DCB	Direct copper bond
DEKF	Dual extended Kalman filter
DSP	Digital signal processor
DT	Digital twin
E	End/sink node in a directed graph
EE	Erneuerbare Energiequellen
EV	Electric vehicle
FCC	Flow conservation constraint
HIL	Hardware-in-the-loop
IGBT	Insulated gate bipolar transistor
IPOP	Input parallel output parallel
ISOP	Input series output parallel
IT	Interconnected topology
L1	First line of an alternating current three phase grid
L2	Second line of an alternating current three phase grid
L3	Third line of an alternating current three phase grid
LEF	Ladesysteme für Elektrofahrzeuge
LV	Low voltage
LVac	Low voltage alternating current

LVdc	Low voltage direct current
MAB	Multiple active bridge
MV	Medium voltage
MVac	Medium voltage alternating current
N	Neutral line of a grid
NCF	Non-conserved flows
NIT	Non-interconnected topology
NP	Neutral point
PE	Power electronics
PEBB	Power electronics building block
PI	Proportional-integral
PLL	Phase-locked loop
PR	Proportional-resonant
PSO	Particle-swarm-optimization
p.u.	Per unit
PV	Photo voltaic
PWM	Pulse width modulation
RES	Renewable energy sources
RMS	Root mean square
RR	Reverse recovery
RTS	Real-time simulation
RUL	Remaining useful lifetime
S	Source node in a directed graph
SOGI	Second-order generalized integrator
SoH	State of health
ST	Smart transformer
SST	Solid state transformer
T	Transistor
THD	Total harmonic distortion
TSEP	Temperature sensitive electrical parameter
v	Virtual node in a directed graph
ZVS	Zero voltage switching

1. Introduction

This chapter introduces the motivation of the main directions in this work. The first main direction is the *design of hybrid grids-feeding Smart Transformers*, which is related to the efficiency of power electronics. The second main direction is *active thermal control and thermal observation*, which is composed of two directions: *observation of the thermal behavior of power modules* and *active thermal control of power electronics converters*. This second main direction is related to the reliability of power electronics.

The efficiency and reliability are essential for power electronics applications. The research proposal of this work - given after the motivation - contains three targets, which are:

- Design optimization of hybrid grids-feeding Smart Transformers for improved efficiency and reduced converter loading,
- Development of thermal digital twin approaches for observation of the thermal behavior of power modules,
- Elaboration on active thermal control methods for hybrid grids-feeding Smart Transformers.

Afterwards, the structure of the work in terms of chapters, sections, and related publications is presented and an overview of the content of the different chapters is given. Finally, the publications associated with this work are listed.

1.1. Motivation of hybrid grids-feeding Smart Transformers

The increasing integration of distributed renewable energy sources (RES) and electric vehicle (EV) charging systems into the power grid poses challenges in handling high generation and demand variability [1–3]. Hybrid ac/dc distribution systems are considered as a major possibility in order to facilitate the integration of the needed flexibility in the future distribution grid [4, 5]. The utilization of hybrid distribution systems - which embed dc grids inside the existing ac grid structure - could combine an efficient integration of RES, EV charging stations, and battery energy storage systems (BESS) [6] via dc grids with the established protection mechanisms of ac grids.

The provision of hybrid distribution grids can be realized via power electronics-based transformers [7], which are able to provide connectivity to dc grids as well as to build the joint between ac grids on medium and low voltage levels. Furthermore, the concept of the Smart Transformer (ST) can play an important role for the provision and the management of hybrid distribution grids [8, 9]. This concept of the ST is defined in [10] as:

The ST is a power electronics-based transformer with advanced control functionalities to allow flexible ac and dc distributions, and the possibility to provide grid services.

One service the ST can provide for the grids is to improve the voltage profile of the medium voltage (MV) grid by injecting reactive power via the converter connected to the MV grid [11]. Herein, using an active power control of the low voltage (LV) grids fed by the ST - utilizing the voltage-dependency of the loads - leads to a lower voltage drop in the MV grid due to the reduced active current, and at the same time more reactive power can be injected via the converter connected to the MV grid. The load control in the LV grids fed by the ST can also be used for primary frequency regulation in the MV grid [12]. Herein, the possibility to decrease or increase the consumption in the LV grids is utilized as a power reserve during frequency variations. Further, the load control in the ST-fed LV grids can be used to reduce the consumption in order to prevent an overload of the ST or to apply a soft load reduction of all consumers to mitigate the execution of load shedding [13].

1.2. Motivation of observation of the thermal behavior of power modules

The reliability of power electronics systems is crucial in order to guarantee a high availability of them in failure-critical applications - e.g. more electric aircrafts [14] - and future power electronics-based grids [10]. To guarantee a high availability of power electronics applications, the reliability of power modules is essential, because the power semiconductors are - besides the capacitors - main failure components in power electronics systems [15, 16]. Monitoring the health condition of power modules [15] enables the application of prognostic maintenance [17], which can reduce the downtime of the systems due to power module failure-caused unscheduled maintenance.

Thermo-mechanical stress of power modules due to varying system utilization is a major factor causing their degradation [17]. Furthermore, the thermal behavior of power modules changes with degradation and can be used to monitor their health condition [15]. The observation of the thermal behavior of power modules allows to monitor the temperatures in order to evaluate if the converter is within safe operation conditions or might be damaged by over-temperatures. Detecting over-temperatures is the first step to initiate measures in order to protect the power modules from harm. Another possibility that is enabled by the observation of the thermal behavior of power modules is the provision of the temperature as essential input for lifetime models in order to estimate their state of health and the remaining useful lifetime [18]. The estimation of the state of health and the remaining useful lifetime allows to adjust the maintenance schedule in order to increase the reliability of power modules. An additional way, that could be combined with the estimation made by lifetime models, is to

carry out condition monitoring based on the thermal behavior in order to access the state of health of power modules. Further, observing the thermal behavior of power modules can provide the temperature as a feedback signal for active thermal control algorithms.

1.3. Motivation of active thermal control of power electronics converters

As presented in the motivation of observation of the thermal behavior of power modules, the reliability of power modules is important and thermo-mechanical stress leads to their degradation. Beyond monitoring the health condition of power modules, actively influencing the thermo-mechanical stress that power modules are exposed to by active thermal control of power electronics converters can be desirable. This is especially the case for power electronics systems which are costly to reach for maintenance due to a difficult accessibility, for example subsea applications [19] or offshore wind power farms [20].

Active thermal control methods approach to increase the reliability of power modules in power electronics converters in different ways [21]. One possibility is to apply active thermal control methods which reduce the losses within power modules while operating close to the thermal limits of the power electronics converters. This can enable a safe operation of power electronics converters close to their limits and increase their overload capability.

Another way of trying to increase the reliability and the lifetime of power modules via active thermal control methods is their application for thermal cycle reduction. Herein, the losses of the power module are reduced for temperatures above the mean temperature and increased for temperatures below the mean temperature. By reducing the temperature swings in this way, the damage done to the power module is lower and their lifetime could be prolonged [17].

Further, active thermal control methods can be implemented in order to balance the thermal stress of power devices in multichip modules, parallel power modules, or in special topologies with redundant switching states such as active neutral point clamped converters. Balancing the thermal stress can benefit a uniform degradation of the power semiconductor devices and relieve degraded devices with high temperatures from thermal stress [22–24].

Another way active thermal control methods can try to improve the reliability of power electronics converter systems is to control the thermal stress of devices in different building blocks. Herein, the thermal stress is relocated from further degraded system parts to less degraded system parts, which attempts to increase the reliability of the power electronics converter system and reduce the required maintenance appointments [25].

1.4. Research proposal

The targets of the research proposal of this work are the following ones:

Target I: Optimization of the design of hybrid grids-feeding Smart Transformers for improved efficiency and reduced converter loading

The first research objective is to optimize the design of ST topologies for the provision of hybrid distribution grids. The design of the ST topologies should consider requirements found for hybrid ac/dc distribution/micro grids. An adjustable configuration of the ST topologies should allow to optimize the ST efficiency according to a given mission profile of the hybrid distribution grid. Adjusting the configuration of the ST topologies should also be able to provide a reduced converter loading for a given mission profile of the hybrid distribution grid. This reduced converter loading could be used to downsize the converter power rating, insert additional failure tolerance for the ST, or combine these two.

Target II: Development of thermal digital twin approaches for observation of the thermal behavior of power modules

The second research objective is the development of thermal digital twin (DT) approaches of power modules based on different methods. The thermal digital twin approaches should be able to observe the thermal behavior of power modules, which could be checked by identifying the thermal parameters of a digital reference model in a real time simulation without previous knowledge about these parameters. The developed thermal DT approaches should be compared for suitable criteria, which consider possible advantages and disadvantages of their application in the field as well as efforts required for further research on the approaches. The more appropriate thermal DT approach should be extended for the observation of multiple semiconductor chips with thermal cross coupling effects inside a power module. It should be verified that this thermal DT approach for multiple semiconductor chips is able to replicate the temperatures of a real power module in the laboratory.

Target III: Elaboration on active thermal control methods for hybrid grids-feeding Smart Transformers

The third research objective is to elaborate on active thermal control (ATC) methods for hybrid grids-feeding STs. By reviewing ATC methods used for power electronics converters, it should be evaluated which methods are most relevant for the application case ST. Those methods identified should be elaborated to be made suitable for the requirements of the hybrid grids-feeding ST topologies that should be found in the first objective of this work. A simultaneous and independent operation of the methods in the ST should be considered.

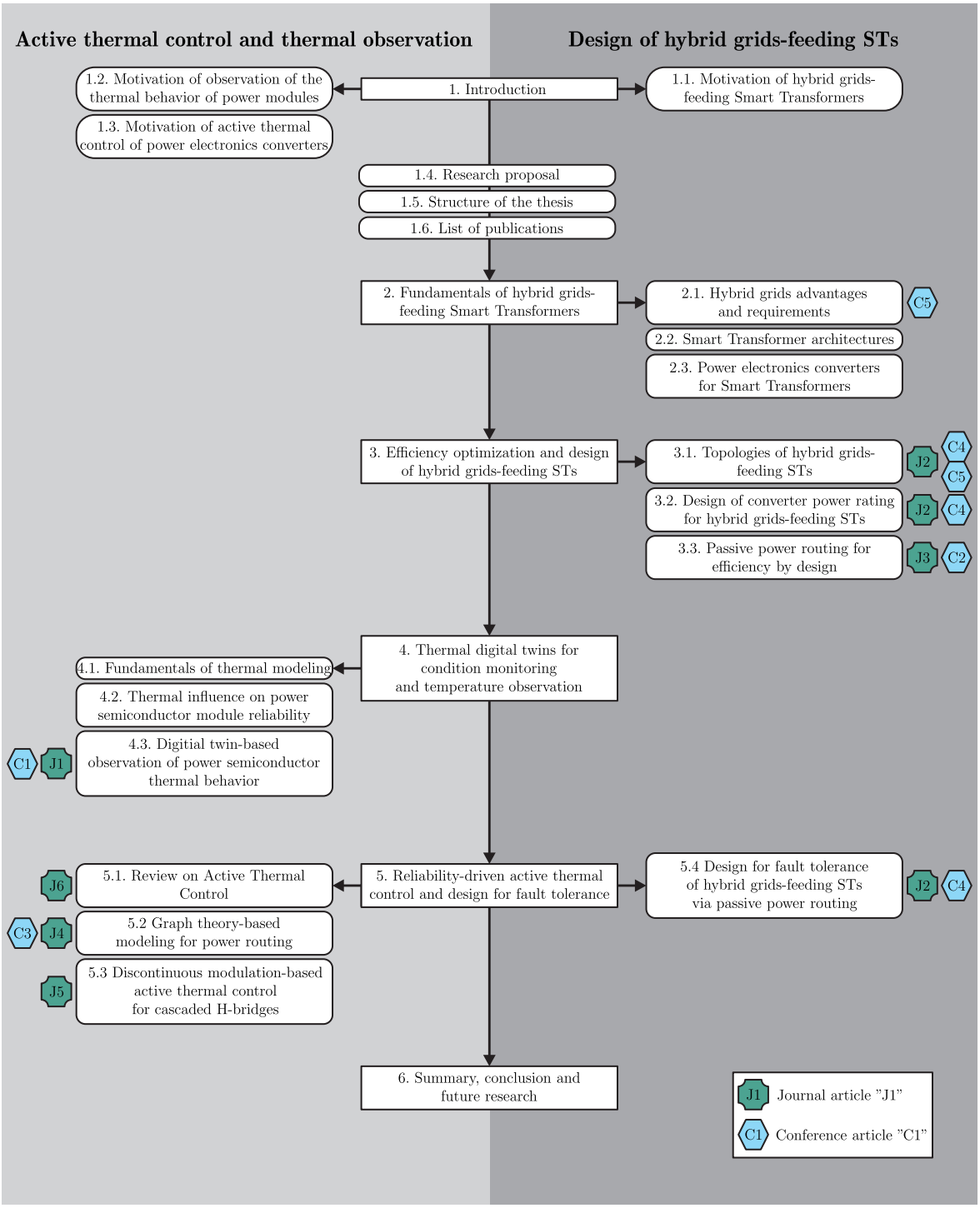


Fig. 1.1: Structure of the work with related publications.

1.5. Structure of this work

The structure of this work in terms of chapters, sections, and related publications is illustrated in Fig. 1.1.

Chapter 2 is structured as follows: based on [26], advantages and requirements of hybrid grids are presented in Section 2.1. Section 2.2 shows ST architectures and discusses which of them can fulfill the requirements of hybrid grids. The basics of loss calculation and the

power electronics converters used to realize ST topologies from the architectures in this work are introduced in Section 2.3. A summary and the conclusions of Chapter 2 can be found in Section 2.4.

Chapter 3 is structured as follows: the topologies presented in [26–28], which are the base for the optimal configuration of the hybrid grids-feeding ST, are introduced in Section 3.1. Based on [27, 28], Section 3.2 proposes a mission profile-based design procedure for the power rating of all converters in the topologies, examines the opportunity to downsize one specific converter, and a Monte Carlo-based sensitivity analysis of the derived converter power ratings against deviations of the assumed mission profiles is executed. In Section 3.3, the efficiency influence of the configuration in one of the basis topologies is presented, two approaches to derive this configuration for optimal efficiency of mission profiles are proposed according to [29, 30], and a laboratory validation of the efficiency influence of the configuration choice is given. A summary and the conclusions of Chapter 3 can be found in Section 3.4.

Chapter 4 is structured as follows: The fundamentals of thermal modeling are given in Section 4.1. Section 4.2 describes the thermal influence on power semiconductor module reliability by explaining the degradation mechanism evoked by thermal cycles, showing existing lifetime models and their limitations, and giving a review on condition monitoring methods for power semiconductors via the thermal behavior. Afterwards, Section 4.3 proposes the DT-based observation of the power semiconductor thermal behavior by describing the basic principle of a thermal DT, developing DT approaches based on a particle-swarm-optimization (PSO) - based on [31] - and a dual extended Kalman filter (DEKF), comparing both approaches, and extending the DEKF-based thermal DT to a multichip representation, which considers thermal cross coupling effects. Furthermore, the capability of the DEKF-based multichip thermal DT to represent the thermal behavior in real-time is validated on a laboratory setup. A summary and the conclusions of Chapter 4 can be found in Section 4.4.

Chapter 5 is structured as follows: Based on [21], a review of ATC methods used in power electronics systems as well as an evaluation of these methods for the use in the ST are given in Section 5.1. Section 5.2 elaborates on the graph theory-based modeling used for power routing on basis of [32, 33] by introducing the basics of graph theory-based modeling of power electronics converter systems, describing its application in hybrid grids-feeding STs, as well as revealing and validating a modeling method with higher accuracy for the loss description than the state-of-the-art method. Next, a new third harmonic clamped modulation method - originally presented in [34] - is described, theoretically compared with the first harmonic clamped modulation method, and validated in the laboratory in Section 5.3. Afterwards, Section 5.4 carries out a mission profile-based failure analysis for the hybrid grids-feeding ST topologies and reveals the opportunity for additional failure tolerance in one of the topologies, based on [27, 28]. A summary and the conclusions of Chapter 5 can

be found in Section 5.5.

Chapter 6 gives a summary and the conclusions of this work. Further, potential topics for future research based on this work are listed.

1.6. List of publications

The scientific publications associated with this work, to which Fig. 1.1 refers, are listed here:

Journal publications

J1 **J. Kuprat**, K. Debbadi, J. Schaumburg, M. Liserre and M. Langwasser, "Thermal Digital Twin of Power Electronics Modules for Online Thermal Parameter Identification," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2023.3328219.

J2 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Mission Profile-Tailored Design and Control of an Interconnected Hybrid Grid Connecting Converter Architecture," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2023.3278082.

J3 J. Schaumburg, **J. Kuprat**, M. Langwasser and M. Liserre, "Efficiency Optimization via Mission Profile-Based Power Routing by Design of Hybrid Grid Connecting Converter Architecture," in *IEEE Open Journal of Power Electronics*, doi: 10.1109/OJPEL.2023.3241778.

J4 Y. Li, **J. Kuprat**, Y. Li and M. Liserre, "Graph-Theory-Based Derivation, Modeling and Control of Power Converter Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2022.3143437.

J5 Y. Ko, **J. Kuprat**, S. Pugliese and M. Liserre, "Modulation Strategies for Thermal Stress Control of CHB Inverters," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3515-3527, March 2022, doi: 10.1109/TPEL.2021.3117917.

J6 **J. Kuprat**, C. H. van der Broeck, M. Andresen, S. Kalker, M. Liserre and R. W. De Doncker, "Research on Active Thermal Control: Actual Status and Future Trends," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6494-6506, Dec. 2021, doi: 10.1109/JESTPE.2021.3067782.

Conference publications

C1 **J. Kuprat**, Y. Pascal and M. Liserre, "Real-Time Thermal Characterization of Power Semiconductors using a PSO-based Digital Twin Approach," *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022, pp. P.1-P.8.

C2 J. Schaumburg, **J. Kuprat**, M. Langwasser and M. Liserre, "Efficiency Optimization via Mission Profile-Based Design of a Hybrid Grids-Feeding Smart Transformer," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-6, doi: 10.1109/PEDG54999.2022.9923058.

C3 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Improved Graph-Theory Based Modeling of the Smart Transformer for Hybrid Grids," *2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, 2022, pp. 1-6, doi: 10.1109/CPE-POWERENG54966.2022.9880867.

C4 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Mission-Profile Based Design of a Hybrid-Grids Feeding Smart Transformer," *2021 6th IEEE Workshop on the Electronic Grid (eGRID)*, 2021, pp. 01-08, doi: 10.1109/eGRID52793.2021.9662152.

C5 **J. Kuprat**, M. Andresen, V. Raveendran and M. Liserre, "Modular Smart Transformer Topology for the Interconnection of Multiple Isolated AC and DC Grids," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4836-4841, doi: 10.1109/ECCE44975.2020.9236136.

2. Fundamentals of hybrid grids-feeding Smart Transformers

This chapter introduces the fundamentals of hybrid grids-feeding Smart Transformers (STs) for optimizing their efficiency and design in Chapter 3. For this purpose, the definition of hybrid grids referred to in this work as well as their advantages and requirements are presented. Further, ST architectures are shown and their ability to fulfill the requirements is discussed. Moreover, the power electronics converters, which are used in this work, to realize topologies from the architectures are introduced.

The chapter is organized as follows: based on [26], advantages and requirements of hybrid grids are presented in Section 2.1. Section 2.2 shows ST architectures and discusses which of them can fulfill the requirements of hybrid grids. The basics of loss calculation and the power electronics converters used to realize ST topologies from the architectures in this work are introduced in Section 2.3. A summary and the conclusions of the chapter can be found in Section 2.4.

2.1. Hybrid grids advantages and requirements

This section presents what the term *hybrid grids* refers to in this work. Next, the advantages enabled by the utilization of hybrid grids are shown. Afterwards, the requirements for a safe implementation of hybrid grids, which realizes the shown advantages, are given.

2.1.1. Hybrid grids definition

In this work, the term *hybrid grids* refers to embedding dc grids inside the existing ac grid structure. In particular, the integration of LVdc grids on a low voltage level - up to 750 V dc between power line and neutral conductor - is considered besides the existing LVac grids.

The existing MVac grids are considered as primary distribution grid on a medium voltage level. The STs investigated in this work build a substation to connect an MVac primary distribution grid with a hybrid secondary distribution grid consisting of LVac and LVdc grids.

2.1.2. Hybrid grids advantages

The advantages of hybrid grids are the benefits from LVac as well as LVdc grids, which can be both exploited by using hybrid LV grids [35]. These benefits of LVac grids compared to LVdc grids and vice versa are presented in Fig. 2.1. A main benefit of LVdc grids compared

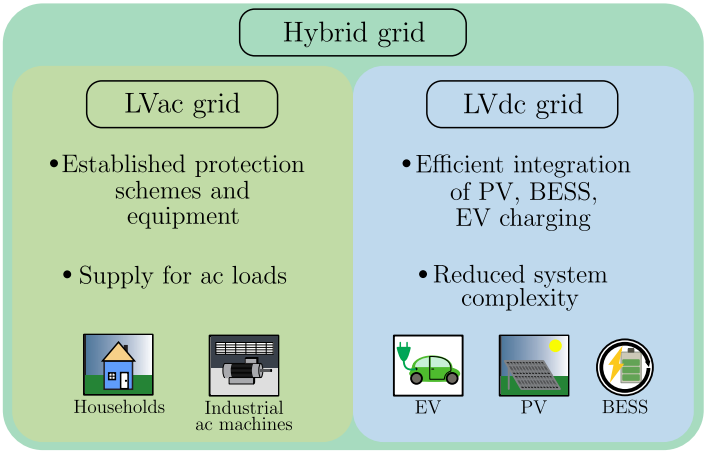


Fig. 2.1: Benefits of LVac and LVdc grids combinable via a hybrid grid.

to LVac grids is the lower number of conversion stages for the integration of electric vehicle (EV) charging stations, photo voltaic (PV) power generation plants, and battery energy storage systems (BESS) into a dc grid compared to their integration into an ac grid. Less conversion stages lead to less losses and, therefore, a higher efficiency of the distribution system [36, 37]. A further benefit of LVdc grids compared to LVac grids is the reduced system complexity due to the fact that management of reactive power and grid frequency is not needed [38].

The main benefit of LVac grids compared to LVdc grids is the availability of established protection schemes and equipment, which is especially important for areas where inexperienced users connect and disconnect electrical devices frequently, such as in households. Another benefit of LVac grids compared to LVdc grids is the efficient connection of ac loads, such as industrial ac machines, without the necessity of installing an inverter.

2.1.3. Hybrid grids requirements

The first requirement, which needs to be fulfilled to provide the possibility to operate a hybrid secondary distribution grid safely, is the provision of galvanic isolation between the grids. Galvanic isolation between the MVac primary distribution grid and the LV secondary distribution grids is required to guarantee the safety of persons and equipment in facilities connected to the LV secondary distribution grids. Furthermore, galvanic isolation is also required between the LVac and LVdc secondary distribution grids. Absence of galvanic isolation between LVac and LVdc secondary distribution grids can lead to high fault and body currents due to the common mode voltage between the LV grids [39] and limits the flexibility of choosing appropriate grounding schemes [40, 41].

The second requirement is to choose an appropriate hybrid grids connecting converter architecture in order to realize the full potential for increasing the efficiency of the system by the utilization of hybrid secondary distribution grids. The hybrid grids connecting converter

architectures investigated in this work are the Smart Transformer architectures, which are introduced in Section 2.2.

2.2. Smart Transformer architectures

This section shows general ST architectures at first. Next, ST architectures, which are suitable for the provision of hybrid LV secondary distribution grids and fulfill the requirement of galvanic isolation between this LV grids, are presented. Afterwards, a review on hybrid grids-feeding ST topologies proposed in research articles is given and the ST architectures they refer to are identified. In this work, ST topologies describe the realization of ST architectures with specific power electronics converters.

2.2.1. General ST architectures

The general ST architectures to connect an MVac primary distribution grid to an LVac or an LVdc secondary distribution grid are shown in Fig. 2.2. A two stage ST architecture does not allow provision of a galvanic isolation between an MVac primary distribution grid and an LVac secondary distribution grid (Fig. 2.2 (a)), to insert galvanic isolation a three stage ST architecture is needed (Fig. 2.2 (c)). For the connection of an MVac primary distribution grid and an LVdc secondary distribution grid, a two stage ST architecture is sufficient to provide galvanic isolation between these grids (Fig. 2.2 (b)).

2.2.2. Hybrid grids-feeding ST architectures

A hybrid grids-feeding ST architecture fulfilling the galvanic isolation requirement between the grids could be created by utilizing the three stage ST architecture shown in Fig. 2.2 (c)

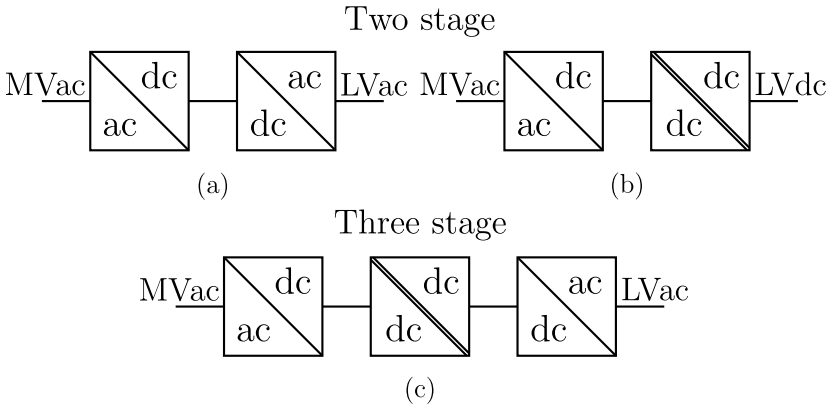


Fig. 2.2: ST architectures providing connection between MVac and a single LV grid, (a) two-stage unisolated MVac-LVac, (b) two-stage isolated MVac-LVdc, and (c) three stage isolated MVac-LVac architecture.

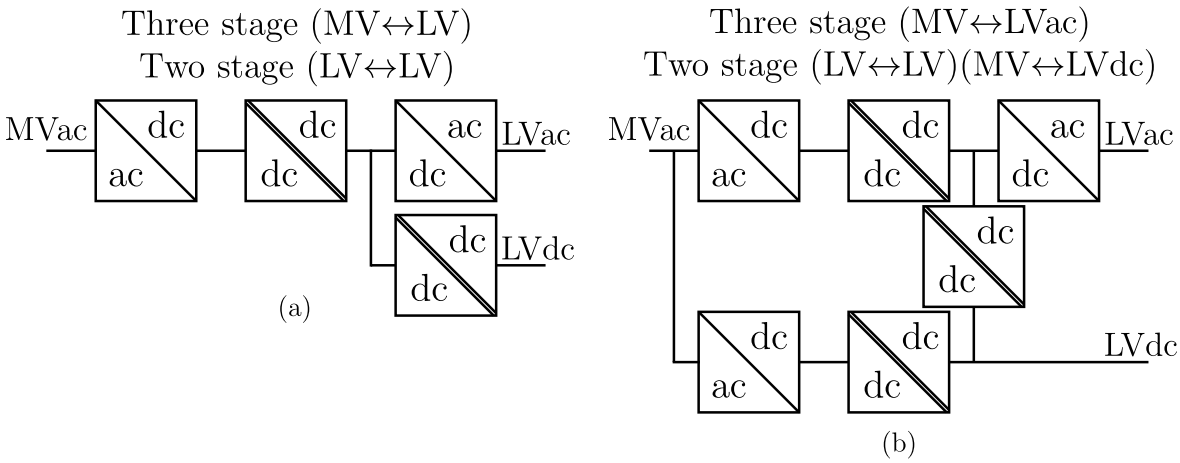


Fig. 2.3: ST architectures for the connection between MVac and a hybrid LV grid fulfilling the galvanic isolation requirements, (a) non-interconnected architecture and (b) interconnected architecture.

for the connection of MVac and LVac grids and the two stage ST architecture shown in Fig. 2.2 (b) for the connection of MVac and LVdc grids. However, this would result in five conversion stages for the power transfer between the LV grids, which would lead to high losses and low hybrid grids connecting converter efficiency.

A hybrid grids-feeding ST architecture fulfilling the galvanic isolation requirement between the grids can also be created by connecting an isolated dc/dc converter to the LV side dc-link of the three stage ST architecture, as shown in Fig. 2.3 (a). This results in two conversion stages between the LV grids and three conversion stages between MVac grid and LV grids. A further possibility is the interconnected architecture shown in Fig. 2.3 (b), which provides only two conversion stages between MVac and LVdc grids.

The potential of the interconnected architecture will be investigated in this work and the ST architecture shown in Fig. 2.3 (a), which is referred to as non-interconnected architecture, will be used as benchmark for comparison.

2.2.3. Review on hybrid grids-feeding ST topologies

Most topologies of hybrid grids-feeding STs proposed in research articles are based on the three stage architecture shown in Fig. 2.2 (c). Topologies with cascaded H-bridge (CHB) converter for the MVac connection, dual active bridge (DAB) converters for the dc/dc isolation stage, two-level three phase inverter for the LVac grid provision, and a direct connection of the LVdc grid to the dc-link on the LV side have been proposed in [9, 42–44]. Further, using quadruple active bridge converters for the dc/dc isolation stage has been proposed in [9]. A topology with neutral point clamped converter for the MVac connection is proposed in [45] and an active rectifier is used in [46, 47]. In these articles, the isolation stage is realized

via DAB converters and the LVac provision via a two-level three phase inverter. Direct connections of an MVdc grid on the dc-link of the MV side and of an LVdc grid on the dc-link of the LV side are proposed. Furthermore, different topology realizations of the three stage architecture shown in Fig. 2.2 (c) have been proposed in [7] and work with this architecture without specifying a topology has been conducted in [48]. Also in these articles, a direct connection of the LVdc grid on the dc-link of the LV side has been considered.

None of the hybrid grids-feeding ST topologies proposed in [7, 9, 42–48] fulfill the requirement of galvanic isolation between LVac and LVdc grids needed for a safe operation of hybrid secondary distribution grids - as described in Section 2.1.

A topology based on a CHB for the MVac connection, a multiple active bridge (MAB) converter for the isolation stage, and a two-level three phase inverter for the provision of the LVac grid has been proposed in [49]. The LVdc grid connection is proposed as one port of the MAB converter, which provides galvanic isolation between the grids. This topology is based on the interconnected architecture shown in Fig. 2.3 (b), herein, all dc/dc isolation stages are realized via the MAB converter. However, utilization of an MAB converter with a high number of inputs and outputs raises challenges in terms of its design and control.

Therefore, DAB converters are considered in this work to realize the different dc/dc isolation stages of the interconnected architecture shown in Fig. 2.3 (b). Further, the MVac connection is realized via a CHB and the LVac grid provision via a two-level three phase inverter.

2.3. Power electronics converters for Smart Transformers

This section introduces the power electronics converters, which will be used in Section 3.1 to realize ST topologies based on the non-interconnected and interconnected ST architectures presented in Section 2.2. The focus of the presentation of the power electronics converters is the calculation of their losses depending on the power processed by them.

In this section, the calculation of semiconductor and transformer losses are introduced at first. Next, the topology and operation principle of a DAB converter is introduced, equations to describe the electrical waveforms are derived, and the calculation of the DAB losses is explained. Then, the topology and operation principle of a two-level three phase inverter is introduced, equations to describe the electrical waveforms are given, and the calculation of the inverter losses is explained. Afterwards, the topology and operation principle of a CHB converter is introduced, equations to describe the electrical waveforms are given, and the calculation of the CHB losses is explained.

2.3.1. Semiconductor losses

In the converters used in the work two kinds of power semiconductors will be used: insulated gate bipolar transistors (IGBTs) - as devices which can be turned on and off actively - and diodes, which allow current flow only in one direction. The semiconductor losses considered in this work are:

- conduction losses of IGBTs and diodes,
- switching losses of IGBTs,
- reverse recovery losses of diodes.

The conduction losses of IGBTs and diodes arise whenever current flows through the power semiconductors. The switching losses of IGBTs occur when they are turned on or off and none of the zero voltage or zero current soft switching conditions shown in Fig. 2.4 is present. The reverse recovery losses of diodes occur whenever switching an IGBT applies a voltage in blocking direction of a diode while the diode carries current.

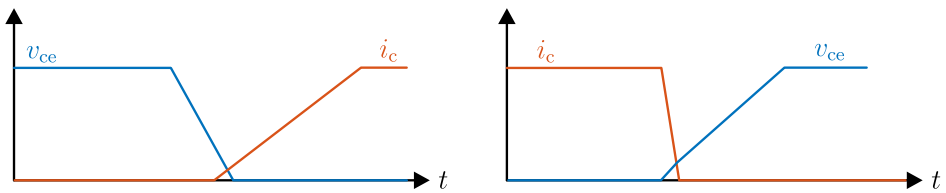
The average conduction losses of an IGBT for a specific period τ, such as the time span from $t_2 = 0$ to $t_3 = \tau$ in Fig. 2.5, can be calculated by

$$\overline{P}_{\text{con,IGBT}} = \frac{1}{\tau} \int_0^{\tau} v_{\text{ce}}(t) i_{\text{c}}(t) \, \mathrm{d}t \ . \tag{2.1}$$

Herein, the collector current of the IGBT $i_{\text{c}}(t)$ can be determined via an electrical simulation/ calculation of the converter behavior or by measurements on a real system. The characteristic of the IGBT collector emitter voltage $v_{\text{ce}}(t)$ depending on the collector current is specified in the manufacturer's data sheet.

The average conduction losses of a diode for a specific period τ can be calculated by

$$\overline{P}_{\text{con,diode}} = \frac{1}{\tau} \int_0^{\tau} v_{\text{D}}(t) i_{\text{D}}(t) \, \mathrm{d}t \ . \tag{2.2}$$



Zero current turn-on (a) Zero voltage turn-off (b)

Fig. 2.4: Collector current and collector emitter voltage behavior during (a) zero current turn-on, and (b) zero voltage turn-off (adapted from [50]).

Herein, the current through the diode $i_D(t)$ can be determined via an electrical simulation/ calculation of the converter behavior or by measurements on a real system. The characteristic of the diode forward voltage $v_D(t)$ depending on the diode current is specified in the manufacturer's data sheet.

The energy converted to heat during one turn-on of an IGBT, schematically shown in Fig. 2.5, can be calculated by

$$E_{on}(i_c(t_2), V_{block,ref}) = \int_{t_1}^{t_2} i_c(t) v_{ce}(t)\, dt \ . \tag{2.3}$$

Herein, the collector current and the collector emitter voltage during the turn-on and, therefore, the energy converted to heat depend on the current that is commutated by the IGBT $i_c(t_2)$ and the collector emitter voltage over the IGBT during the off-state V_{cc}. The collector emitter voltage over the IGBT during the off-state used for the characterization of the switching losses is the reference blocking voltage $V_{block,ref}$. The characteristic of the energy converted to heat during one turn-on of an IGBT depending on the current commutated by the IGBT for a specific reference blocking voltage $V_{block,ref}$ is given in the manufacturer's data sheet.

The energy converted to heat during one turn-off of an IGBT, schematically shown in Fig. 2.5,

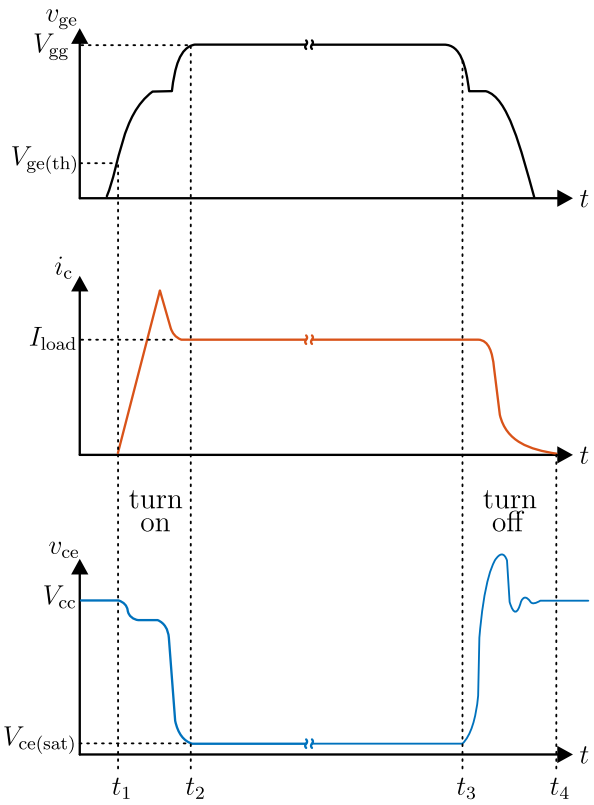


Fig. 2.5: Gate emitter voltage, collector current and collector emitter voltage waveforms for an IGBT during turn on ($t_1 < t < t_2$), conduction ($t_2 < t < t_3$) and turn off ($t_3 < t < t_4$) (adapted from [50]).

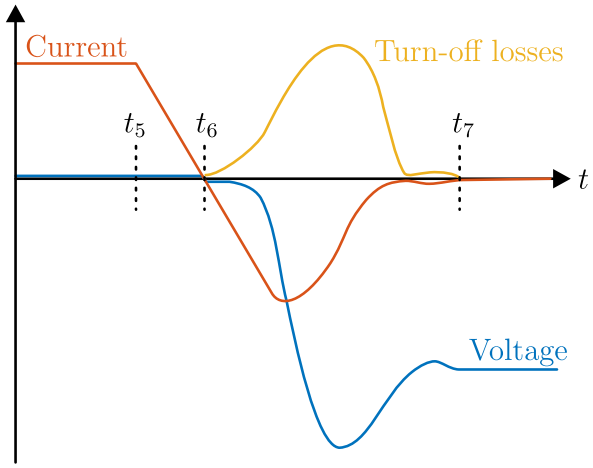


Fig. 2.6: Current, voltage and turn-off losses behavior during diode reverse recovery (adapted from [50]).

can be calculated by

$$E_{\text{off}}(i_{\text{c}}(t_3), V_{\text{block,ref}}) = \int_{t_3}^{t_4} i_{\text{c}}(t) v_{\text{ce}}(t)\, \mathrm{d}t \tag{2.4}$$

Herein, the collector current and the collector emitter voltage during the turn-off and, therefore, the energy converted to heat depend on the current through the IGBT when the turn-off starts $i_{\text{c}}(t_3)$ and the collector emitter voltage over the IGBT during the off-state. The characteristic of the energy converted to heat during one turn-off of an IGBT depending on the current through the IGBT when the turn-off starts for a specific reference blocking voltage $V_{\text{block,ref}}$ is given in the manufacturer's data sheet.

For adjusting the values of the energy converted to heat during turn-on and turn-off to other blocking voltages V_{block} than the one that was used during the characterization, a linear scaling is used

$$E_{\text{on}}(i_{\text{c}}(t_2), V_{\text{block}}) = E_{\text{on}}(i_{\text{c}}(t_2), V_{\text{block,ref}}) \frac{V_{\text{block}}}{V_{\text{block,ref}}} \tag{2.5}$$

$$E_{\text{off}}(i_{\text{c}}(t_3), V_{\text{block}}) = E_{\text{off}}(i_{\text{c}}(t_3), V_{\text{block,ref}}) \frac{V_{\text{block}}}{V_{\text{block,ref}}} \,. \tag{2.6}$$

The average IGBT switching losses for a specific period τ with B_1 turn-on events and B_2 turn-off events can be calculated by

$$\overline{P}_{\text{loss,sw}} = \frac{1}{\tau} \left(\sum_{b=1}^{B_1} E_{\text{on}}(i_{\text{c}}(b), V_{\text{block}}) + \sum_{b=1}^{B_2} E_{\text{off}}(i_{\text{c}}(b), V_{\text{block}}) \right) \,. \tag{2.7}$$

The energy converted to heat during one reverse recovery of a diode, schematically shown in Fig. 2.6, can be calculated by

$$E_{\text{rr}}(i_{\text{D}}(t_5), V_{\text{block,ref}}) = \int_{t_6}^{t_7} i_{\text{D}}(t) v_{\text{D}}(t)\, \mathrm{d}t \tag{2.8}$$

Herein, the diode current and the diode voltage in forward direction during the reverse recovery and, therefore, the energy converted to heat depend on the current that flows initially through the diode $i_{\mathrm{D}}(t_5)$ and the final voltage blocked by the diode. The final voltage blocked by the diode that is used for the characterization of the reverse recovery losses is the reference blocking voltage $V_{\mathrm{block,ref}}$. The characteristic of the energy converted to heat during one reverse recovery of a diode depending on the current that flows initially through the diode for a specific reference blocking voltage $V_{\mathrm{block,ref}}$ is given in the manufacturer's data sheet.

For adjusting the values of the energy converted to heat during reverse recovery to other blocking voltages V_{block} than the one that was used during the characterization, a linear scaling is used

$$E_{\mathrm{rr}}(i_{\mathrm{D}}(t_5), V_{\mathrm{block}}) = E_{\mathrm{rr}}(i_{\mathrm{D}}(t_5), V_{\mathrm{block,ref}}) \frac{V_{\mathrm{block}}}{V_{\mathrm{block,ref}}} \quad . \tag{2.9}$$

The average diode reverse recovery losses for a specific period τ with B reverse recovery events can be calculated by

$$\overline{P}_{\mathrm{loss,rr}} = \frac{1}{\tau} \left(\sum_{b=1}^{B} E_{\mathrm{rr}}(i_{\mathrm{D}}(b), V_{\mathrm{block}}) \right) \quad . \tag{2.10}$$

2.3.2. Transformer losses

A DAB contains a medium frequency transformer in order to provide galvanic isolation between its input and output. Therefore, it is also necessary to consider the losses of the medium frequency transformer in order to calculate the losses of a DAB. The transformer losses considered in this work are:

- copper losses of the conductor windings,
- core losses of the magnetic core material.

The copper losses of the conductor windings depend on the currents flowing through them on the primary and secondary side of the transformer. Therefore, they change with the power processed by the DAB, whereas the core losses are independent from the processed power.

The copper losses of the conductor windings can be calculated via the resistance of the windings and the primary and secondary currents of the transformer. The primary and secondary currents of the transformer can be derived by electrical simulation/ calculation of the DAB converter. The way of calculating the resistances of the conductor windings based on the DAB design is presented in the following passage.

The first step to determine the resistance of the conductor windings is to calculate the length of the conductor on the primary and on the secondary side. For this purpose, the number

of windings on the primary side N_{pri} needs to be chosen and the number of windings on the secondary side is calculated by

$$N_{\text{sec}} = \frac{V_{\text{sec}}}{V_{\text{pri}}} N_{\text{pri}} = \frac{1}{n} N_{\text{pri}} \ . \tag{2.11}$$

Herein, the turns ratio of the transformer $n = \frac{N_{\text{pri}}}{N_{\text{sec}}}$ is designed to the ratio of the design values of primary RMS voltage V_{pri} to secondary RMS voltage V_{sec} of the transformer. The cross sectional area of the transformer core A_{cr} required to avoid saturation of the core material is calculated by

$$A_{\text{cr}} = \frac{V_{\text{pri}}}{N_{\text{pri}} c_{\text{form}} f_{\text{sw}} B_{\text{pk}}} \ . \tag{2.12}$$

Herein, c_{form} is a coefficient which describes the impact of the applied electrical waveforms on the saturation of the core, for the DAB waveforms $c_{\text{form}} = 4$ is considered. f_{sw} is the applied switching frequency of the DAB and B_{pk} is the peak value of the magnetic flux density of the core material without saturation - in this work N87 ferrite is considered as core material. The length of one turn of the conductor windings is approximated as shown in Fig. 2.7 by a circle with the radius

$$r_{\text{winding}} = \sqrt{2} \frac{\sqrt{A_{\text{cr}}}}{2} \ . \tag{2.13}$$

Herein, it is assumed that the cross sectional area of the core is a square. The length of the conductor on the primary side can be determined by

$$l_{\text{pri}} = N_{\text{pri}} 2\pi r_{\text{winding}} \tag{2.14}$$

and the length of the conductor on the secondary side by

$$l_{\text{sec}} = N_{\text{sec}} 2\pi r_{\text{winding}} \ . \tag{2.15}$$

The cross sections of the conductors are chosen to have a maximum current density of

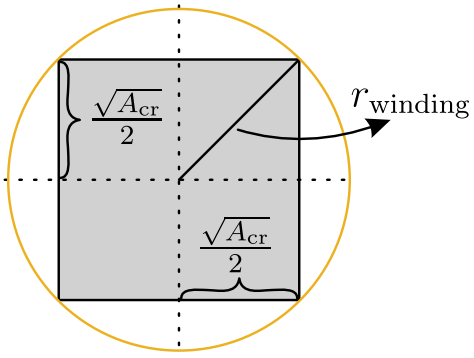


Fig. 2.7: Approximation of wire length for one turn on the transformer core.

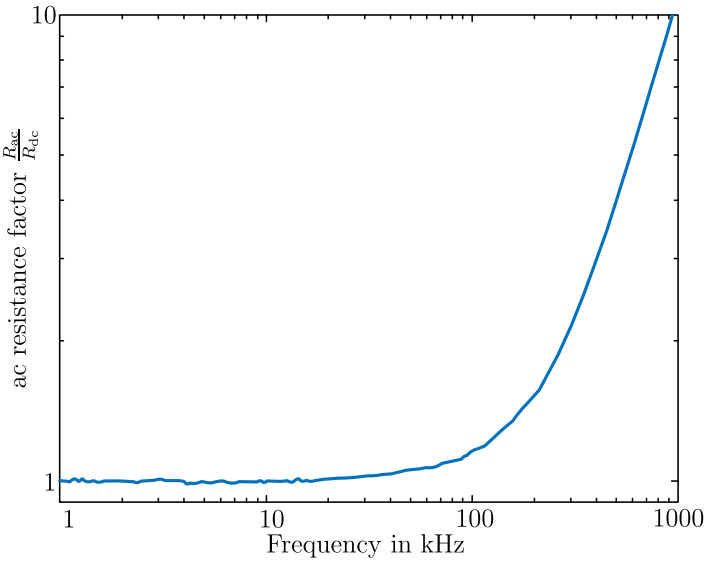


Fig. 2.8: Measured ac resistance factor of 125 strands of 0.16 mm diameter magnet wire constructed as "'true litz"' $5 \times 5 \times 5$ (adapted from [51]).

$6\,\frac{\mathrm{A}}{\mathrm{mm}^2}$

$$A_{\mathrm{cond,pri}} = \frac{I_{\mathrm{pri,rms,max}}}{6\,\frac{\mathrm{A}}{\mathrm{m}^2}\,10^6} \tag{2.16}$$

$$A_{\mathrm{cond,sec}} = \frac{I_{\mathrm{sec,rms,max}}}{6\,\frac{\mathrm{A}}{\mathrm{m}^2}\,10^6} \quad . \tag{2.17}$$

Herein, the maximum RMS currents on the primary side $I_{\mathrm{pri,rms,max}}$ and the secondary side $I_{\mathrm{sec,rms,max}}$ are determined based on electrical simulation/ calculation of the DAB at the designed rated power. The resistances of the conductors are calculated based on the conductor length, their cross section and the specific resistance of copper ρ_{Cu}

$$R_{\mathrm{Cu,pri}} = \rho_{\mathrm{Cu}} \frac{l_{\mathrm{pri}}}{A_{\mathrm{cond,pri}}} \tag{2.18}$$

$$R_{\mathrm{Cu,sec}} = \rho_{\mathrm{Cu}} \frac{l_{\mathrm{sec}}}{A_{\mathrm{cond,sec}}} \quad . \tag{2.19}$$

The impact of skin and proximity effects on the losses are neglected in this work, because they can have insignificant impact on the copper losses for switching frequencies below 20 kHz, as shown in Fig. 2.8. The copper losses are then calculated via the resistances of a specific DAB and transformer design and the RMS currents from the electrical simulation/ calculation, which depend on the power processed by the DAB,

$$P_{\mathrm{loss,Cu,pri}} = R_{\mathrm{Cu,pri}} I^2_{\mathrm{pri,rms}} \tag{2.20}$$

$$P_{\mathrm{loss,Cu,sec}} = R_{\mathrm{Cu,sec}} I^2_{\mathrm{sec,rms}} \quad . \tag{2.21}$$

The core losses of the magnetic transformer core material, which include hysteresis losses

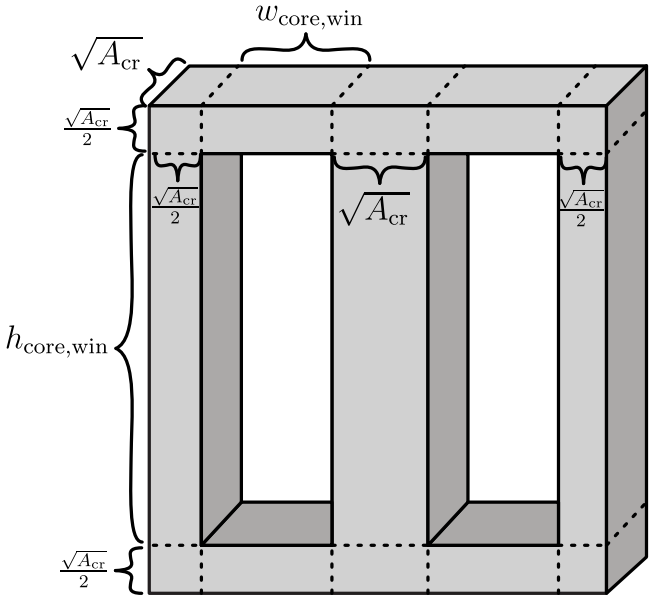


Fig. 2.9: Assumed transformer core geometry for volume calculation.

as well as eddy current losses, are considered via the Steinmetz equation

$$P_{\mathrm{loss,core}} = c_{\mathrm{stm,1}} f_{\mathrm{sw}}^{c_{\mathrm{stm,2}}} B_{\mathrm{pk}}^{c_{\mathrm{stm,3}}} V_{\mathrm{core}} \ . \tag{2.22}$$

Herein, f_{sw} is the switching frequency of the DAB, B_{pk} is the peak magnetic flux density considered in (2.12), V_{core} is the volume of the transformer core, and $c_{\mathrm{stm,1}}$, $c_{\mathrm{stm,2}}$, $c_{\mathrm{stm,3}}$ are coefficients for the specific core material (N87 ferrite). For the volume calculation of the transformer core, an E-core is considered which has primary as well as secondary conductor windings on the middle leg of the core. A window utilization factor of 0.3 is assumed, which means that the copper of the conductor windings in each of the two windows of the E-core is considered as 30 % of the window area

$$A_{\mathrm{core,win}} = \frac{A_{\mathrm{cond,pri}} N_{\mathrm{pri}} + A_{\mathrm{cond,sec}} N_{\mathrm{sec}}}{0.3} \ . \tag{2.23}$$

Further, it is assumed that the windows height is three times the windows width, which gives

$$h_{\mathrm{core,win}} = \sqrt{3 A_{\mathrm{core,win}}} \ , \tag{2.24}$$

$$w_{\mathrm{core,win}} = \sqrt{\frac{A_{\mathrm{core,win}}}{3}} \ . \tag{2.25}$$

The previously made assumptions result in a transformer core geometry as shown in Fig. 2.9. The volume of this transformer core geometry can be calculated by

$$V_{\mathrm{core}} = 2 A_{\mathrm{cr}} h_{\mathrm{core,win}} + 2 A_{\mathrm{cr}} w_{\mathrm{core,win}} + 2 A_{\mathrm{cr}} \sqrt{A_{\mathrm{cr}}} \ . \tag{2.26}$$

The calculated transformer volume for a specific DAB design can be used in (2.22) to con-

sider the core losses of the medium frequency transformer. These core losses are static, which means that they do not change with the processed power of the DAB.

The considered calculation of the transformer losses is simple, which is sufficient in this work, because the accuracy gain by more complex modeling methods of the transformer losses, e.g. [52, 53], would have insignificant impact on the investigated phenomena.

2.3.3. Dual active bridge

The topology of a DAB contains two full bridges, a medium frequency transformer, and an inductor, as shown in Fig. 2.10. Both full bridges are operated in square wave mode with a duty cycle of 50 % at a switching frequency f_{sw}, which means that alternating plus and minus the dc voltages are applied to the ac sides of the full bridges, which are coupled with the inductor and the medium frequency transformer. The power transferred by the DAB is controlled by inserting a phase shift φ between the primary and secondary modulation signals.

The current and voltage waveforms of a DAB with power flow from input to output are shown in Fig. 2.11 and in Fig. 2.12 for reverse power flow. Based on this electrical waveforms, the conduction intervals of the semiconductors as well as the occurrence of hard switching events can be identified, which are used to calculate the semiconductor losses as explained previously in this section. Also the transformer losses can be calculated based on these electrical waveforms.

In order to execute the loss calculation it is necessary to derive the electrical waveforms in dependency of the phase shift φ at first. For this purpose, the evolution of the inductor current i_{pri} is described depending on the voltage drop over the inductor, as it is shown in Fig. 2.10,

$$\frac{\mathrm{d}i_{\mathrm{pri}}(t)}{\mathrm{d}t} = \frac{v_{L_{\mathrm{DAB}}}}{L_{\mathrm{DAB}}} = \frac{v_1(t) - nv_2(t)}{L_{\mathrm{DAB}}} \quad . \tag{2.27}$$

The inductor current is described for one period by substituting $t = \frac{\vartheta}{2\pi f_{\mathrm{sw}}}$. Due to the half period point symmetry of the inductor current, describing a half period is sufficient.

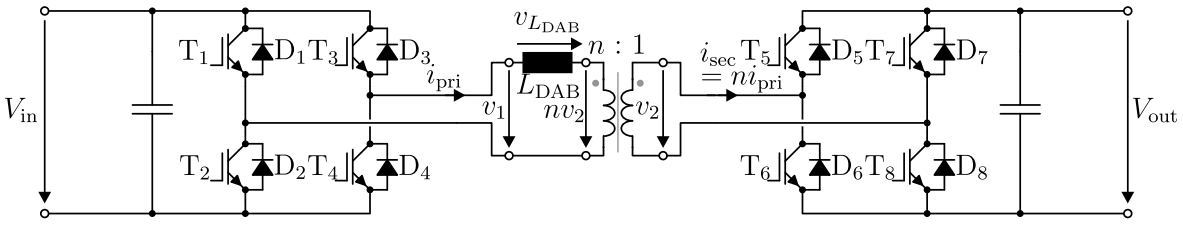


Fig. 2.10: Dual active bridge topology.

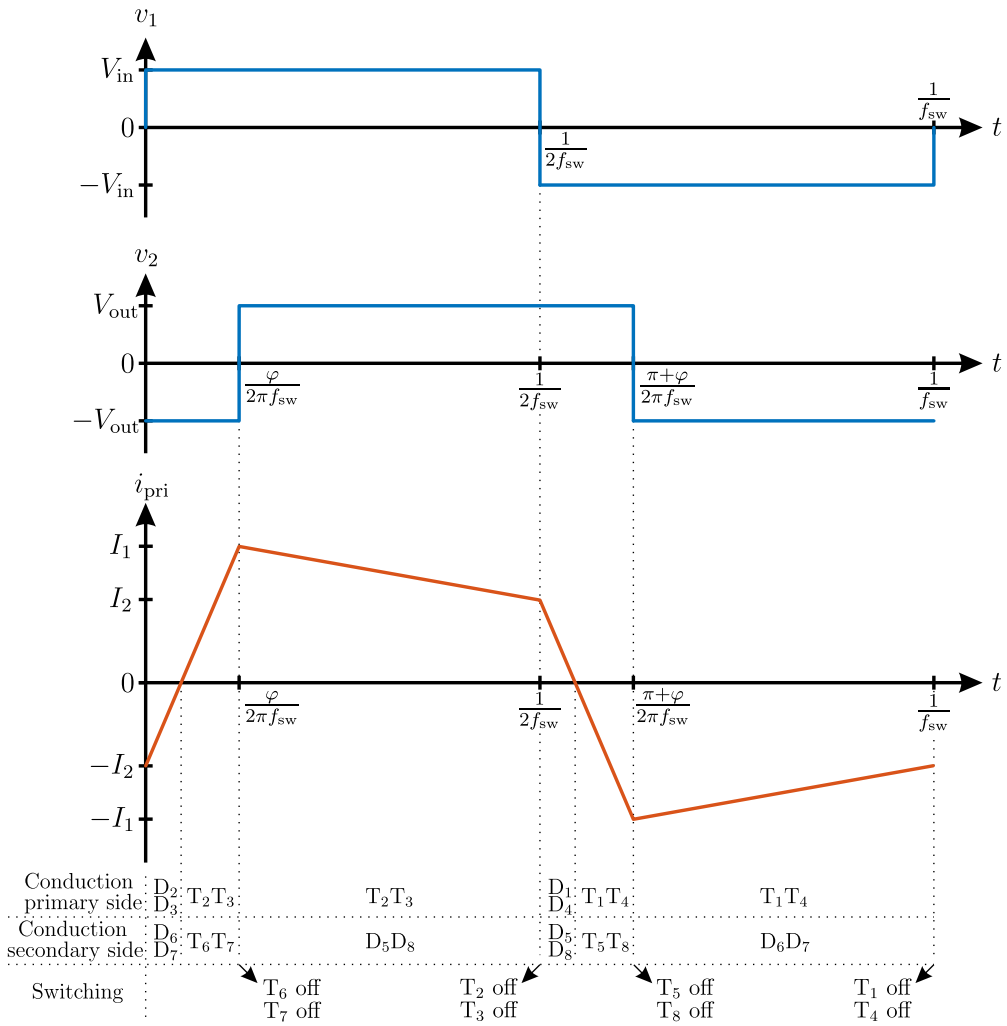


Fig. 2.11: Voltage and current waveforms of a dual-active bridge with positive power flow and indication of conducting semiconductors and switching events without ZVS.

For positive phase shifts $0 \leq \varphi \leq \pi$, the inductor current is

$$i_{pri}(\vartheta) = \begin{cases} \frac{V_{in}+nV_{out}}{2\pi f_{sw} L_{DAB}} \vartheta + i_{pri}(0) & \text{for } 0 \leq \vartheta \leq \varphi \\ \frac{V_{in}-nV_{out}}{2\pi f_{sw} L_{DAB}} (\vartheta - \varphi) + i_{pri}(\varphi) & \text{for } \varphi \leq \vartheta \leq \pi \end{cases} . \tag{2.28}$$

Herein, the inductor currents at φ and π can be expressed as

$$i_{pri}(\varphi) = \frac{V_{in} + nV_{out}}{2\pi f_{sw} L_{DAB}} \varphi + i_{pri}(0) \tag{2.29}$$

and

$$i_{pri}(\pi) = \frac{V_{in} - nV_{out}}{2\pi f_{sw} L_{DAB}} (\pi - \varphi) + i_{pri}(\varphi) \ . \tag{2.30}$$

Without dc offset in the inductor current waveform and due to the half wave point symmetry

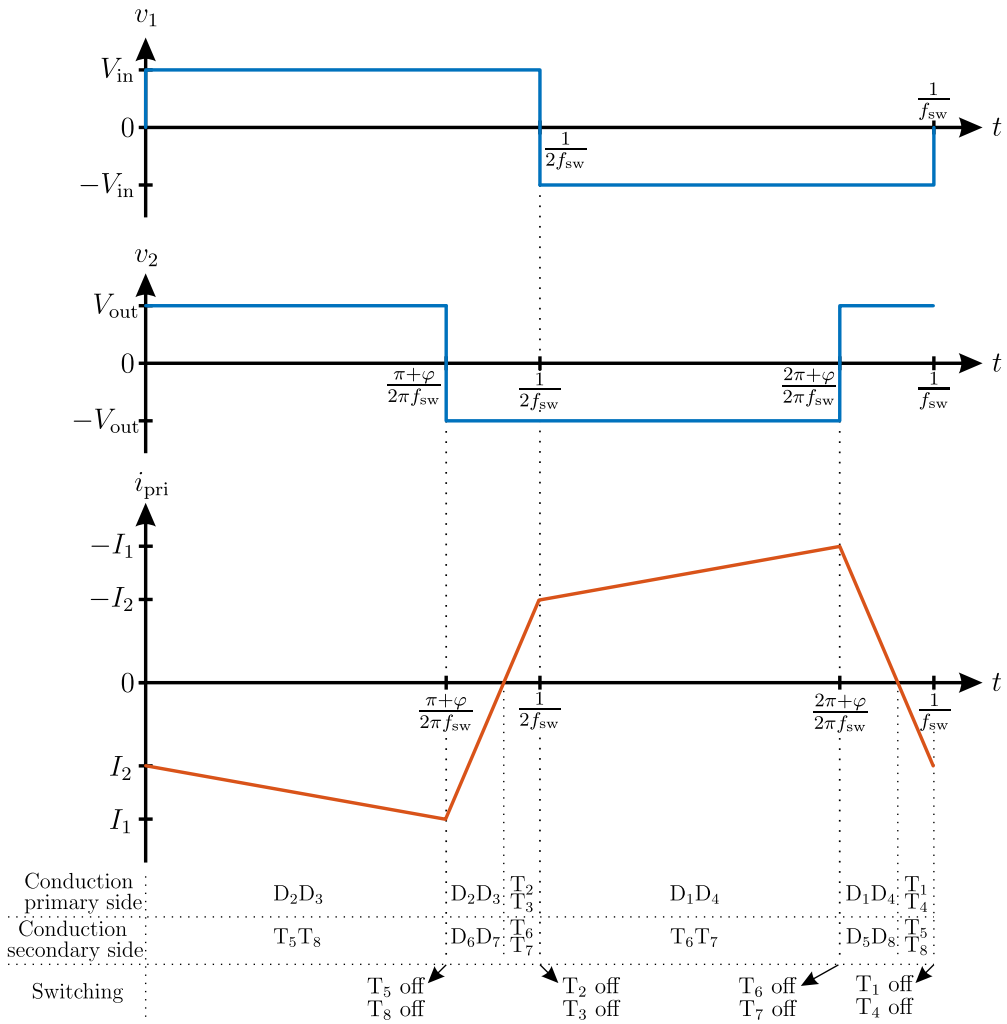


Fig. 2.12: Voltage and current waveforms of a dual-active bridge with negative power flow and indication of conducting semiconductors and switching events without ZVS.

$i_{pri}(0) = -i_{pri}(\pi)$ applies. Therefore, the inductor currents at φ and π can be specified as

$$\begin{aligned} i_{pri}(\varphi) &= \frac{V_{in}+nV_{out}}{2\pi f_{sw}L_{DAB}}\varphi - \frac{V_{in}-nV_{out}}{2\pi f_{sw}L_{DAB}}(\pi-\varphi) - i_{pri}(\varphi) \\ \Leftrightarrow i_{pri}(\varphi) &= \frac{V_{in}+nV_{out}}{4\pi f_{sw}L_{DAB}}\varphi - \frac{V_{in}-nV_{out}}{4\pi f_{sw}L_{DAB}}(\pi-\varphi) \end{aligned} \tag{2.31}$$

and

$$\begin{aligned} i_{pri}(\pi) &= \frac{V_{in}-nV_{out}}{2\pi f_{sw}L_{DAB}}(\pi-\varphi) + \frac{V_{in}+nV_{out}}{4\pi f_{sw}L_{DAB}}\varphi - \frac{V_{in}-nV_{out}}{4\pi f_{sw}L_{DAB}}(\pi-\varphi) \\ &= \frac{V_{in}-nV_{out}}{4\pi f_{sw}L_{DAB}}(\pi-\varphi) + \frac{V_{in}+nV_{out}}{4\pi f_{sw}L_{DAB}}\varphi \ . \end{aligned} \tag{2.32}$$

This results in a description of the inductor current by

$$i_{pri}(\vartheta) = \begin{cases} \frac{V_{in}+nV_{out}}{2\pi f_{sw}L_{DAB}}\vartheta - \frac{V_{in}-nV_{out}}{4\pi f_{sw}L_{DAB}}(\pi-\varphi) - \frac{V_{in}+nV_{out}}{4\pi f_{sw}L_{DAB}}\varphi & \text{for } 0 \le \vartheta \le \varphi \\ \frac{V_{in}-nV_{out}}{2\pi f_{sw}L_{DAB}}(\vartheta-\varphi) + \frac{V_{in}+nV_{out}}{4\pi f_{sw}L_{DAB}}\varphi - \frac{V_{in}-nV_{out}}{4\pi f_{sw}L_{DAB}}(\pi-\varphi) & \text{for } \varphi \le \vartheta \le \pi \ . \end{cases} \tag{2.33}$$

In this work, it is assumed that the DABs are operated at a gain $G_{\mathrm{DAB}} = \frac{nV_{\mathrm{out}}}{V_{\mathrm{in}}} = 1$. This assumption reduces (2.33) to

$$i_{\mathrm{pri}}(\vartheta) = \begin{cases} \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\vartheta - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi & \text{for } 0 \leq \vartheta \leq \varphi \\ \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi & \text{for } \varphi \leq \vartheta \leq \pi \end{cases} . \tag{2.34}$$

The average power processed by the DAB can be calculated by

$$\bar{P}_{\mathrm{DAB}} = \frac{1}{\pi}\int_0^{\pi} v_1(\vartheta) i_{\mathrm{pri}}(\vartheta)\,\mathrm{d}\vartheta \ . \tag{2.35}$$

Herein, $v_1(\vartheta)$ is V_{in} for $0 \leq \vartheta \leq \pi$. Inserting this and (2.34) into (2.35) results in

$$\begin{aligned} \bar{P}_{\mathrm{DAB}} &= \frac{V_{\mathrm{in}}}{\pi}\left(\int_0^{\varphi} \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\vartheta - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi\,\mathrm{d}\vartheta + \int_{\varphi}^{\pi} \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi\,\mathrm{d}\vartheta\right) \\ &= \frac{V_{\mathrm{in}}}{\pi}\left(\left[\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\frac{1}{2}\vartheta^2 - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi\vartheta\right]_0^{\varphi} + \left[\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi\vartheta\right]_{\varphi}^{\pi}\right) \\ &= \frac{V_{\mathrm{in}}}{\pi}\left(\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\frac{1}{2}\varphi^2 - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi^2 + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi(\pi-\varphi)\right) \\ &= \frac{V_{\mathrm{in}}}{\pi}\left(\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\varphi(\pi-\varphi)\right) \ . \end{aligned} \tag{2.36}$$

With $V_{\mathrm{in}} = nV_{\mathrm{out}}$, the processed power of the DAB for positive φ and $G_{\mathrm{DAB}} = 1$ can be described by

$$\bar{P}_{\mathrm{DAB}}(\varphi) = \varphi\left(1 - \frac{\varphi}{\pi}\right)\frac{V_{\mathrm{in}}V_{\mathrm{out}}n}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}} \quad \text{for } 0 \leq \varphi \leq \pi \wedge G_{\mathrm{DAB}} = 1 \ . \tag{2.37}$$

For negative phase shifts $-\pi \leq \varphi \leq 0$, the inductor current is

$$i_{\mathrm{pri}}(\vartheta) = \begin{cases} \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}\vartheta + i_{\mathrm{pri}}(0) & \text{for } 0 \leq \vartheta \leq \pi+\varphi \\ \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}(\vartheta - (\pi+\varphi)) + i_{\mathrm{pri}}(\pi+\varphi) & \text{for } \pi+\varphi \leq \vartheta \leq \pi \end{cases} . \tag{2.38}$$

Herein, the inductor currents at $\pi+\varphi$ and π can be expressed as

$$i_{\mathrm{pri}}(\pi+\varphi) = \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}(\pi+\varphi) + i_{\mathrm{pri}}(0) \tag{2.39}$$

and

$$i_{\mathrm{pri}}(\pi) = \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}} L_{\mathrm{DAB}}}(\pi - (\pi+\varphi)) + i_{\mathrm{pri}}(\pi+\varphi) \ . \tag{2.40}$$

Without dc offset in the inductor current and due to the half wave point symmetry $i_{\mathrm{pri}}(0) =$

$-i_{\mathrm{pri}}(\pi)$ applies. Therefore, the inductor currents at $\pi+\varphi$ and π can be specified as

$$\begin{aligned} i_{\mathrm{pri}}(\pi+\varphi) &= \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi+\varphi) - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(-\varphi) - i_{\mathrm{pri}}(\pi+\varphi) \\ \Leftrightarrow i_{\mathrm{pri}}(\pi+\varphi) &= \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi+\varphi) + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi \end{aligned} \tag{2.41}$$

and

$$\begin{aligned} i_{\mathrm{pri}}(\pi) &= \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(-\varphi) + \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi+\varphi) + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi \\ &= \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi+\varphi) - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi \ . \end{aligned} \tag{2.42}$$

This results in a description of the inductor current by

$$i_{\mathrm{pri}}(\vartheta) = \begin{cases} \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\vartheta - \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi-\varphi) + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi & \text{for } 0 \le \vartheta \le \pi+\varphi \\ \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\vartheta-(\pi+\varphi)) + \frac{V_{\mathrm{in}}-nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi+\varphi) + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi & \text{for } \pi+\varphi \le \vartheta \le \pi \ . \end{cases} \tag{2.43}$$

With the assumption of $G_{\mathrm{DAB}} = \frac{nV_{\mathrm{out}}}{V_{\mathrm{in}}} = 1$ (2.43) is reduced to

$$i_{\mathrm{pri}}(\vartheta) = \begin{cases} \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi & \text{for } 0 \le \vartheta \le \pi+\varphi \\ \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\vartheta-(\pi+\varphi)) + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi & \text{for } \pi+\varphi \le \vartheta \le \pi \ . \end{cases} \tag{2.44}$$

Also here, $v_1(\vartheta)$ is V_{in} for $0 \le \vartheta \le \pi$. Inserting this and (2.44) into (2.35) results in

$$\begin{aligned} \bar{P}_{\mathrm{DAB}} =& \frac{V_{\mathrm{in}}}{\pi}\left(\int_0^{\pi+\varphi} \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi \,\mathrm{d}\vartheta + \int_{\pi+\varphi}^{\pi} \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\vartheta-(\pi+\varphi)) \right. \\ & \left. + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi \,\mathrm{d}\vartheta \right) \\ =& \frac{V_{\mathrm{in}}}{\pi}\left(\left[\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi\vartheta \right]_0^{\pi+\varphi} + \left[\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\frac{1}{2}\vartheta^2 - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi+\varphi)\vartheta \right. \right. \\ & \left. \left. + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi\vartheta \right]_{\pi+\varphi}^{\pi} \right) \\ =& \frac{V_{\mathrm{in}}}{\pi}\left(\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi(\pi+\varphi) + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\frac{1}{2}\pi^2 \right. \\ & - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\frac{1}{2}(\pi^2-2\pi\varphi+\varphi^2) + \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{2\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}(\pi+\varphi)\varphi \\ & \left. - \frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi^2 \right) \\ =& \frac{V_{\mathrm{in}}}{\pi}\left(\frac{V_{\mathrm{in}}+nV_{\mathrm{out}}}{4\pi f_{\mathrm{sw}}L_{\mathrm{DAB}}}\varphi(\pi+\varphi) \right) \ . \end{aligned} \tag{2.45}$$

With $V_{\text{in}} = nV_{\text{out}}$, the processed power of the DAB for negative φ and $G_{\text{DAB}} = 1$ can be described by

$$\bar{P}_{\text{DAB}}(\varphi) = \varphi\left(1+\frac{\varphi}{\pi}\right)\frac{V_{\text{in}}V_{\text{out}}n}{2\pi f_{\text{sw}}L_{\text{DAB}}} \quad \text{for} \quad -\pi \leq \varphi \leq 0 \wedge G_{\text{DAB}} = 1 \ . \tag{2.46}$$

Combining (2.37) and (2.46) gives

$$\bar{P}_{\text{DAB}}(\varphi) = \varphi\left(1-\left|\frac{\varphi}{\pi}\right|\right)\frac{V_{\text{in}}V_{\text{out}}n}{2\pi f_{\text{sw}}L_{\text{DAB}}} \quad \text{for} \quad -\pi \leq \varphi \leq \pi \wedge G_{\text{DAB}} = 1 \ . \tag{2.47}$$

The specific current points I_1 and I_2 of the DAB inductor current waveform can be generally described with $V_{\text{out}}n = G_{\text{DAB}}V_{\text{in}}$ by

$$I_1(\varphi) = i_{\text{pri}}(\varphi)\Big|_{0\leq\varphi} = i_{\text{pri}}(\pi+\varphi)\Big|_{\varphi\leq 0} = \frac{V_{\text{in}}}{4\pi f_{\text{sw}}L_{\text{DAB}}}\left(2\varphi+\frac{\varphi}{|\varphi|}\pi(G_{\text{DAB}}-1)\right) \tag{2.48}$$

and

$$I_2(\varphi) = i_{\text{pri}}(\pi)\Big|_{0\leq\varphi} = i_{\text{pri}}(0)\Big|_{\varphi\leq 0} = \frac{V_{\text{in}}}{4\pi f_{\text{sw}}L_{\text{DAB}}}\left(2G_{\text{DAB}}\varphi+\frac{\varphi}{|\varphi|}\pi(1-G_{\text{DAB}})\right) \ . \tag{2.49}$$

The design of the DAB inductance for a specific rated power of the DAB can be determined by assuming a maximum phase shift of $\frac{35^\circ\pi}{180^\circ}$ in (2.47). The phase shift φ for a specific processed power of a given DAB design can be calculated by reformulating (2.47). Herein, always two phase shifts would lead to the same processed power, the phase shift closer to 0 should be taken, because it provides lower reactive power inside the DAB.

2.3.4. Two-level three phase inverter

The topology of a two-level three phase inverter with neutral wire is shown in Fig. 2.13. For the calculation of the losses, it is sufficient to consider the electrical waveforms of one phase of the two-level inverter (Fig. 2.14). For the half-bridge, the modulation index m is derived by dividing the reference voltage v_{ref} by half of the dc-link voltage $\frac{V_{\text{dc}}}{2}$.

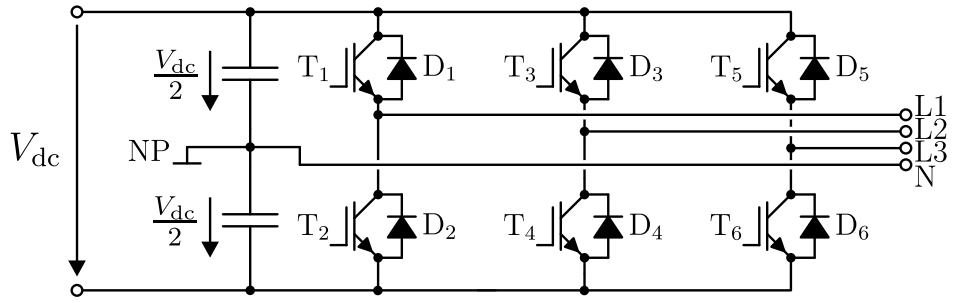


Fig. 2.13: Two-level three phase inverter topology with neutral wire.

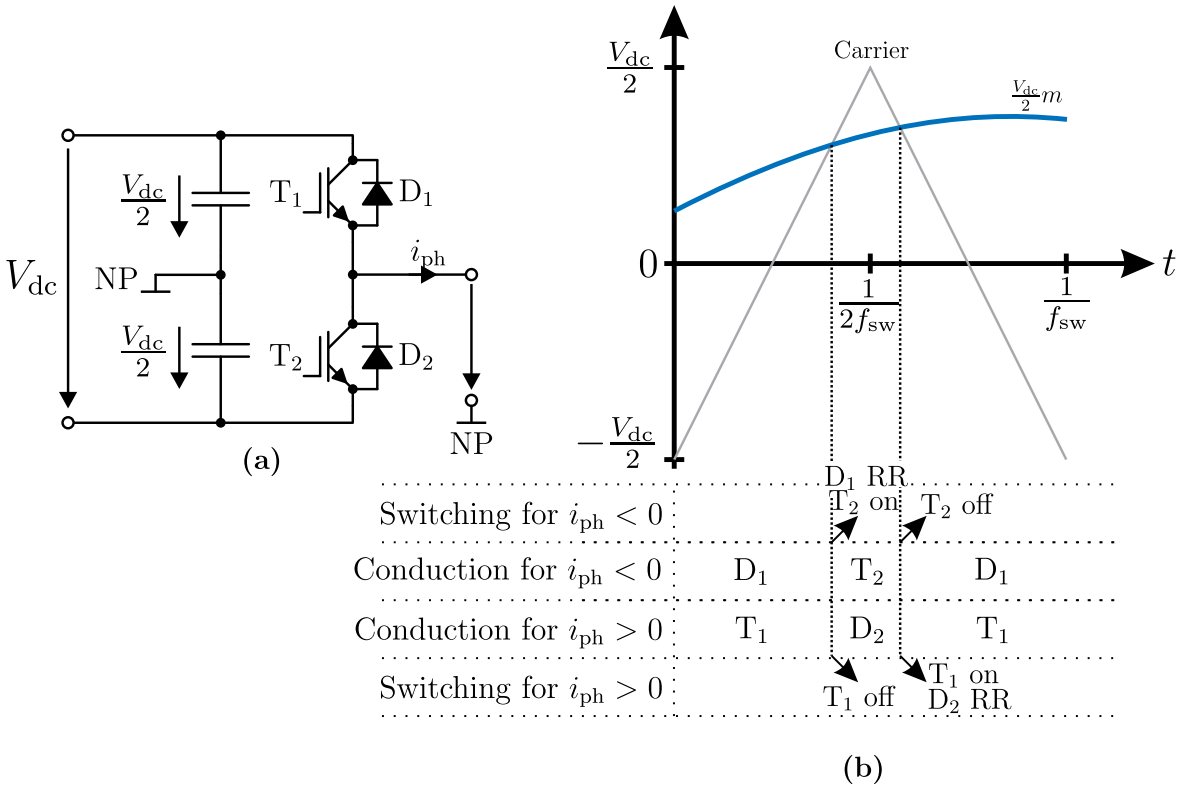


Fig. 2.14: Single phase of a two-level inverter: (a) topology and (b) PWM modulation and indication of conducting semiconductors and switching events.

The considered reference voltage for the LVac grid, with $\omega_g = 2\pi 50\,\text{Hz}$, is

$$v_{ref}(t) = \sqrt{2} \cdot 230\,\text{V} \sin(\omega_g t) \ . \tag{2.50}$$

The phase current i_{ph} considered for the calculation of the losses is

$$i_{ph}(t) = \sqrt{2} \frac{P_{ph}}{|\cos(\varphi_{LVac})| 230\,\text{V}} \sin(\omega_g t - \varphi_{LVac}) \ . \tag{2.51}$$

Herein, P_{ph} is the power consumed or generated in one phase of the LVac grid and φ_{LVac} is the angle between voltage reference and the current of the same phase. An equal distribution of the LVac power on each of the three phases is assumed.

The conduction intervals of the semiconductors and the occurrence of switching events, such as turn-on and turn-off of the IGBTs as well as the reverse recovery (RR) of the diodes, need to be identified for each period of the carrier $\frac{1}{f_{sw}}$, as shown in Fig. 2.14. The loss calculation is done for each period of the carrier in a half period of the reference voltage, as shown exemplarily in Fig. 2.15. Considering half of the period is sufficient due to the point symmetry of the electrical waveforms of the other half of the period. The average losses over one half period of the reference voltage calculated for one phase of the two-level inverter are up-scaled to three phases at the end.

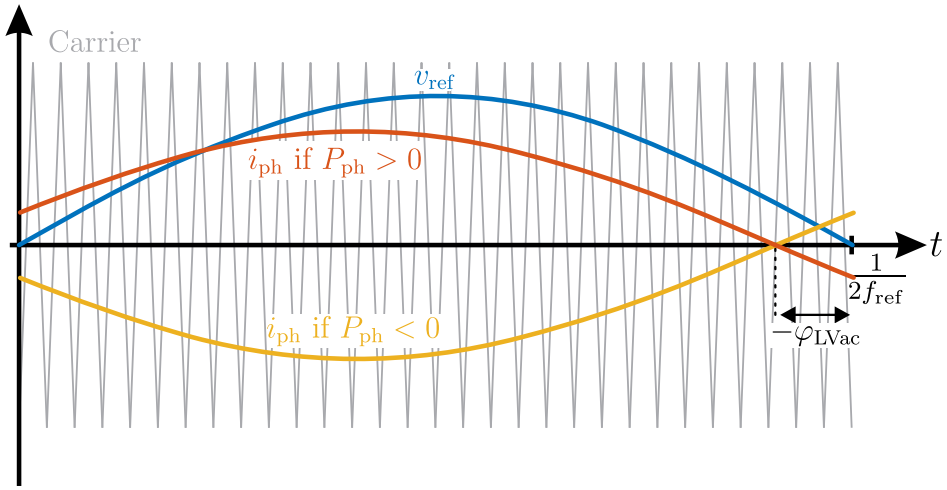


Fig. 2.15: Single phase reference voltage and phase current.

2.3.5. Cascaded H-Bridge

The topology of a seven-level single phase CHB is shown in Fig. 2.16. The CHB consists of full bridge cells which are cascaded (in series connected) on the ac side. The number of output voltage levels is the number of cells in one phase N_{CHB} times two plus one -

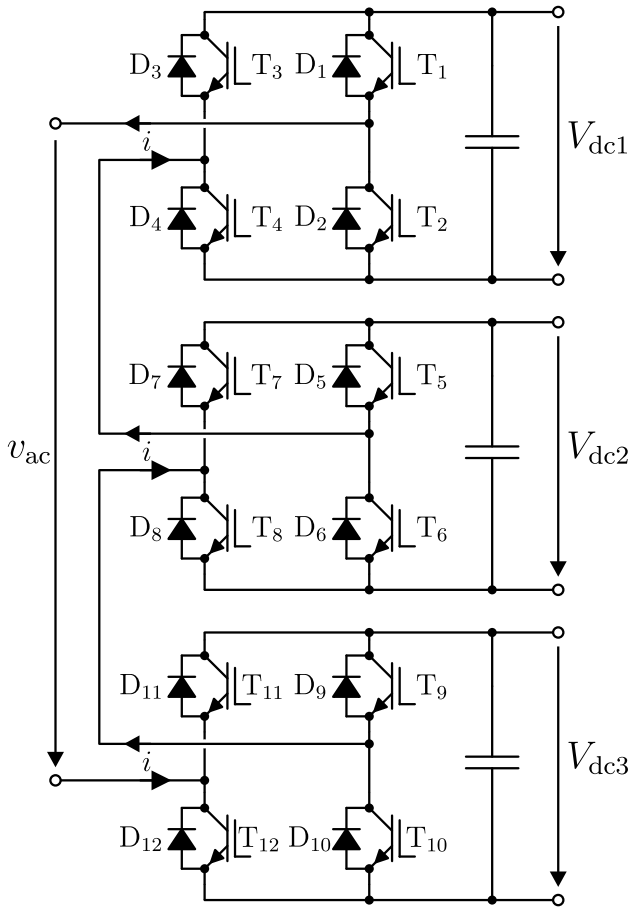


Fig. 2.16: Cascaded H-bridge topology, single phase with three cells.

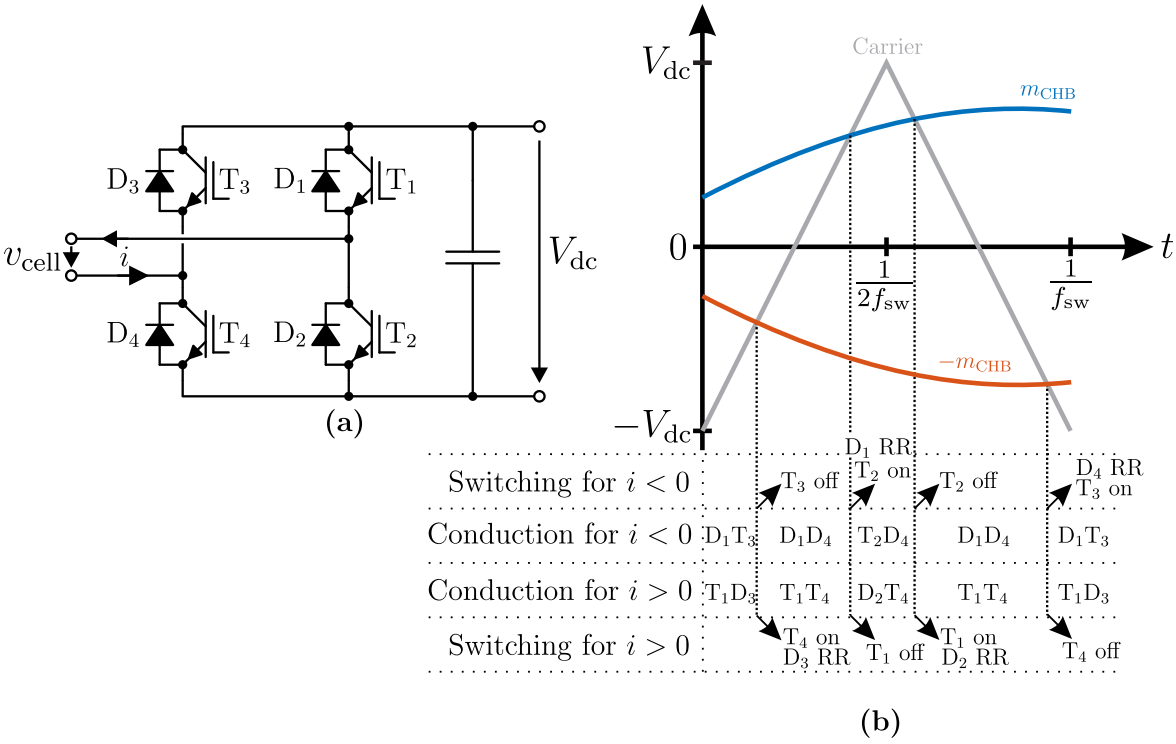


Fig. 2.17: Full bridge converter: (a) topology and (b) unipolar PWM modulation and indication of conducting semiconductors and switching events.

which gives seven levels for the three shown CHB cells. For laboratory implementation in Section 5.3, a phase shifted carrier modulation is applied to the CHB, which means that a unipolar modulation is applied to each of the cells whereby the carrier signals of the cells are shifted by $\frac{180^\circ}{N_{\mathrm{CHB}}}$ to each other.

However, only one full bridge cell is considered for the loss calculation of the CHB (Fig. 2.17). The modulation index of the full bridge cell is

$$m_{\mathrm{CHB}} = \frac{\sqrt{2}V_{\mathrm{ac,rms,ph}}\sin(\omega_{\mathrm{g}}t)}{N_{\mathrm{CHB}}V_{\mathrm{dc}}} \quad . \tag{2.52}$$

Herein, $V_{\mathrm{ac,rms,ph}}$ is the RMS line to neutral voltage of the grid connected to the ac side of the CHB, which is $\frac{1}{\sqrt{3}}$ of the line to line voltage. The phase current of the CHB considered for the calculation of the losses is

$$i = \frac{\sqrt{2}P_{\mathrm{CHB,ph}}}{V_{\mathrm{ac,rms,ph}}|\cos(\varphi_{\mathrm{MVac}})|}\sin(\omega_{\mathrm{g}}t - \varphi_{\mathrm{MVac}}) \quad . \tag{2.53}$$

Herein, $P_{\mathrm{CHB,ph}}$ is the power fed into or drawn from one phase of the MVac grid and φ_{MVac} is the angle between voltage reference and the current of the same phase. An equal distribution of the MVac power on each of the three phases is assumed.

The conduction intervals of the semiconductors and the occurrence of switching events need to be identified for each period of the carrier $\frac{1}{f_{\mathrm{sw}}}$, as shown in Fig. 2.17. As in the case of the

two-level inverter, the loss calculation is done for each period of the carrier in a half period of the modulation index m_{CHB}. The average losses over one half period of the modulation index m_{CHB} of one CHB cell is up-scaled to the number of CHB cells in one phase N_{CHB} and then to three phases.

2.4. Summary and conclusions of the chapter

This chapter introduced the definition of hybrid grids as referred to in this work at first in Section 2.1. The advantages of hybrid secondary distribution grids were presented, which combine benefits of LVac as well as LVdc grids. The benefits of LVac grids are utilization of established protection schemes and equipment as well as supply of ac loads, whereas those of LVdc grids are an efficient integration of photovoltaic power plants, battery energy storage systems, and electric vehicle charging stations as well as a reduced system complexity. Further, the requirements of hybrid grids were shown, which are galvanic isolation between the grids and an efficient hybrid grids connection converter architecture.

Architectures for Smart Transformers (STs) were presented in Section 2.2. Herein, the general ST architectures were shown at first. Then, hybrid grids-feeding ST architectures were proposed, which fulfill the galvanic isolation requirement between the grids. Afterwards, a review on hybrid grids-feeding ST topologies proposed in research articles was given and the architectures these topologies are based on were identified.

The power electronics converters used to realize ST topologies from the ST architectures in this work were described in Section 2.3. The focus of the converter description is to calculate their power losses depending on the power processed by them. For this purpose, the calculation of semiconductor and transformer losses was explained at first. Afterwards, the derivation of the electrical waveforms of a dual active bridge, a two-level three phase inverter, and a cascaded H-bridge was given and it was shown which semiconductors of the converters need to be taken into account for the calculation of the losses at which part of the electrical waveforms.

3. Efficiency optimization and design of hybrid grids-feeding STs

This chapter deals with one of the two major challenges for the application of STs - the efficiency. Especially, the optimal design of the ST to provide hybrid low voltage grids for the secondary distribution - via LVac and LVdc - is in focus. This optimal design of the hybrid grids-feeding ST contributes to the realization of the advantages discussed in Section 2.1. The optimality of the design is investigated in terms of the required converter power ratings as well as the efficiency of the ST. The investigated ST topologies are based on the architectures and converters presented in Section 2.2 and 2.3.

The chapter is organized as follows: the topologies presented in [26–28], which are the base for the optimal configuration of the hybrid grids-feeding ST, are introduced in Section 3.1. Based on [27, 28], Section 3.2 proposes a mission profile-based design procedure for the power rating of all converters in the topologies, examines the opportunity to downsize one specific converter, and a Monte Carlo-based sensitivity analysis of the derived converter power ratings against deviations of the assumed mission profiles is executed. In Section 3.3, the efficiency influence of the configuration in one of the basis topologies is presented, two approaches to derive this configuration for optimal efficiency of mission profiles are proposed according to [29, 30], and a laboratory validation of the efficiency influence of the configuration choice is given. A summary and the conclusions of the chapter can be found in Section 3.4.

3.1. Topologies of hybrid grids-feeding STs

This section introduces the topologies used to find an optimal configuration of the hybrid grids-feeding ST. These topologies are the realization of the non-interconnected and the interconnected hybrid grids-feeding ST architectures presented in Section 2.2 with the converters from Section 2.3. They will be called Non-Interconnected Topology (NIT) and Interconnected Topology (IT) in this work.

In this section, the NIT and the IT are introduced at first. Afterwards, the method to calculate the efficiency of the converter systems for specific LVac and LVdc power generation or consumption is presented.

3.1.1. Non-interconnected topology

The NIT is presented in Fig. 3.1 (a) and its representation as a general graph - with the different voltage levels and forms as nodes and the converters or converter combinations connecting them as arcs - is shown in Fig. 3.1 (b).

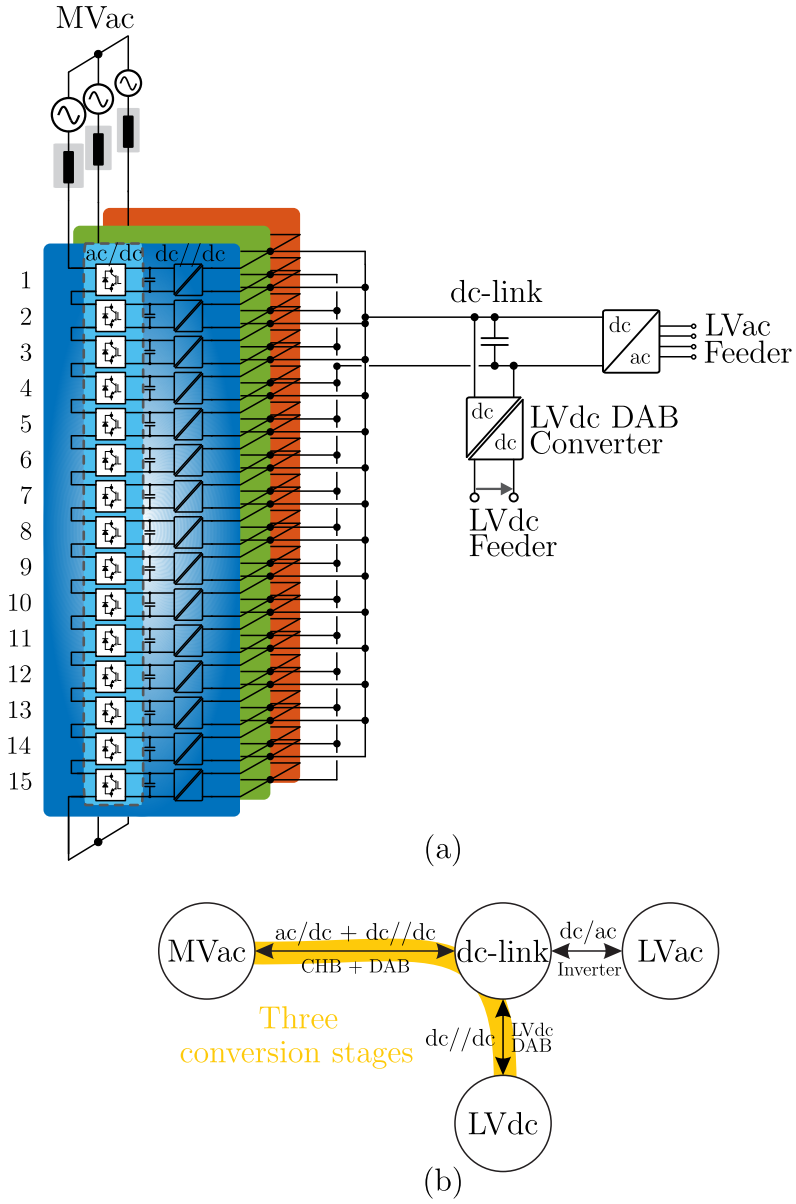


Fig. 3.1: (a) Non-interconnected topology and (b) graph representation.

The connection to the MVac grid (frequency of 50 Hz and an RMS phase-to-phase voltage of 11 kV) is realized with a three-phase CHB with 15 cells in each phase. The dc side of each cell of the CHB (voltage of 800 V) is connected to a DAB, which provides galvanic isolation between the MV and the LV grids. The combination of one CHB cell with the DAB connected to it will be referred to as MVac Power Electronics Building Block (PEBB). The outputs of all these DABs are connected in parallel to the dc-link (voltage of 800 V). Therefore, the combination of all MVac PEBBs builds an Input-Series-Output-Parallel (ISOP) converter structure for the NIT.

The connection between the dc-link and the LVac grid (frequency of 50 Hz and an RMS phase-to-neutral voltage of 230 V) is realized with a two-level three-phase converter, which is acting as inverter when power consumption and as active rectifier when power generation dominates in the LVac grid. For simplicity, this converter is named three phase inverter in

this work.

The connection between dc-link and the LVdc grid (750 V) is realized with a DAB, which provides the possibility to adapt the voltage as well as galvanic isolation between the grounding schemes of the LVac and LVdc grids. This DAB will be referred to as LVdc grid for the NIT.

As the graph of the NIT in Fig. 3.1 (b) highlights, power transfer between MVac and LVdc grid always requires three conversion stages - CHB and DAB of the MVac PEBBs plus the LVdc DAB.

3.1.2. Interconnected topology

The IT is shown in Fig. 3.2 (a) and its general graph description is presented in Fig. 3.2 (b).

The converters used to build the IT are the same used for the NIT: a CHB for the MVac connection, DABs on each CHB cell to provide galvanic isolation between MV and LV grids, a three phase inverter to connect dc-link and LVac grid, and a DAB which provides galvanic isolation and voltage adaptability between dc-link and LVdc grid. However, the essential difference between the IT and the NIT is the connection of the DABs of the MVac PEBBs. While all of the MVac PEBBs are connected in parallel to the dc-link for the NIT, the MVac PEBBs are subdivided in two groups for the IT. One of these groups with $N_{\mathrm{MB,dc-link}}$ MVac PEBBs in each of the three phases is connected to the dc-link, such as in the NIT. The other group with $N_{\mathrm{MB,LVdc}}$ MVac PEBBs in each of the three phases is connected directly to the LVdc feeder. Therefore, the combination of all MVac PEBBs builds a dc-multibus (MB) converter structure for the IT.

The configuration of the IT is described by the split into these two groups via the link ratio ξ, which is the number of MVac PEBBs connected to the LVdc feeder in one phase $N_{\mathrm{MB,LVdc}}$ divided by the number of all MVac PEBBs in one phase N_{MB}

$$\xi = \frac{N_{\mathrm{MB,LVdc}}}{N_{\mathrm{MB}}} \quad . \tag{3.1}$$

The same configuration for each of the three phases and 15 MVac PEBBs in each phase ($N_{\mathrm{MB}} = 15$) are assumed in this work. Therefore, there are 14 possible link ratios for the IT in the range

$$\frac{1}{N_{\mathrm{MB}}} \leq \xi \leq \frac{N_{\mathrm{MB}} - 1}{N_{\mathrm{MB}}} \quad . \tag{3.2}$$

Choosing $\xi = 0$ describes the NIT, which is used as benchmark for comparison. The link ratio $\xi = 1$ describes another non-interconnected topology, where all MVac PEBBs are connected directly to the LVdc feeder. This second non-interconnected topology is excluded in this work.

The DAB between the dc-link and the LVdc feeder builds an interconnection between the two dc buses created by the dc-multibus converter structure in the IT. Therefore, this DAB in the IT is referred to as interconnecting DAB in this work.

As the graph of the IT in Fig. 3.2 (b) highlights, power transfer between MVac and LVdc grids is possible with only two conversion stages - CHB and DAB of the MVac PEBBs connected directly to the LVdc feeder. This provides the possibility of advanced efficiency of IT compared to the NIT as well as a reduced power rating of the interconnecting DAB compared to the LVdc DAB.

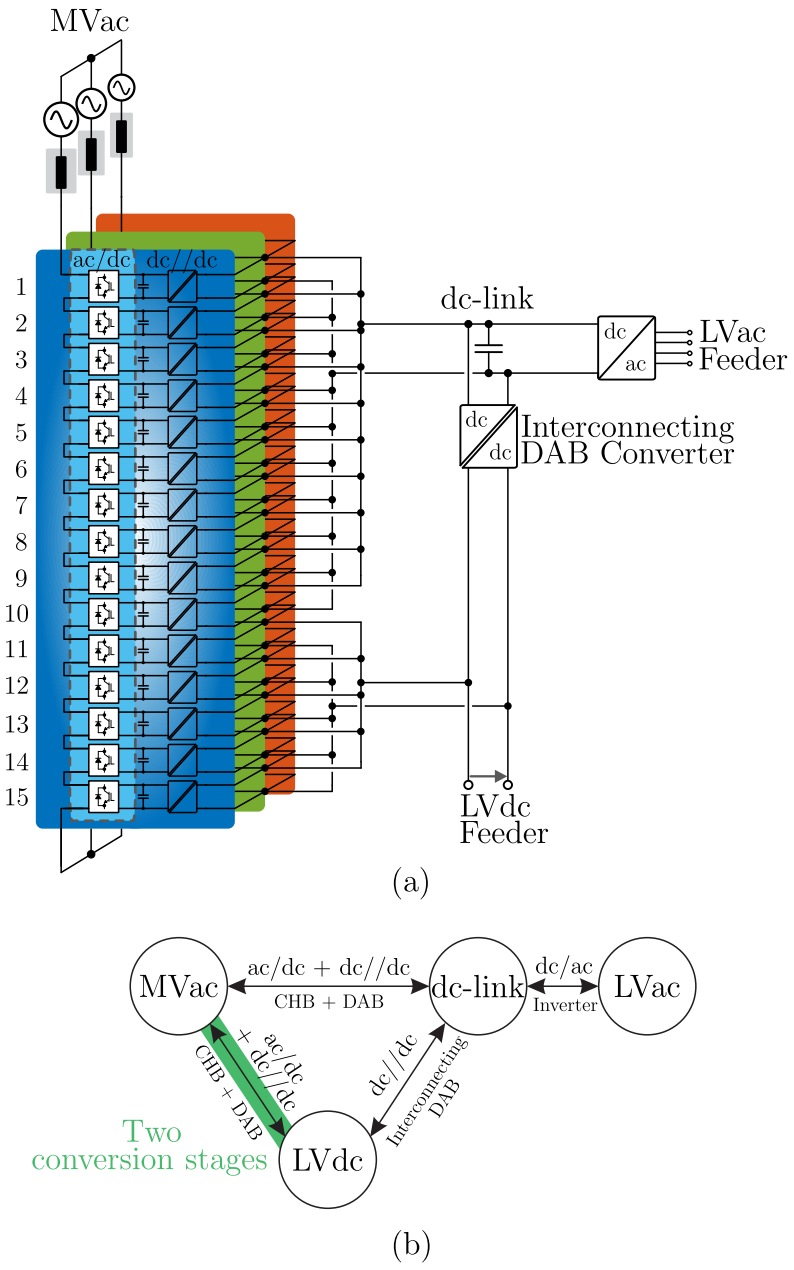


Fig. 3.2: (a) Interconnected topology (example for $\xi = \frac{1}{3}$) and (b) graph representation.

3.1.3. Method for system efficiency calculation

The method that is used for the calculation of the system efficiency of the ST topologies contains two main steps:

- **Main step 1:** Calculation of efficiency curves, which describe the dependency of the converter efficiency on its output power, for each of the converters.
- **Main step 2:** Execution of a non-conserved power flow analysis, which means that the losses of converters are added to the power loading of other converters, via utilization of the efficiency curves from main step 1.

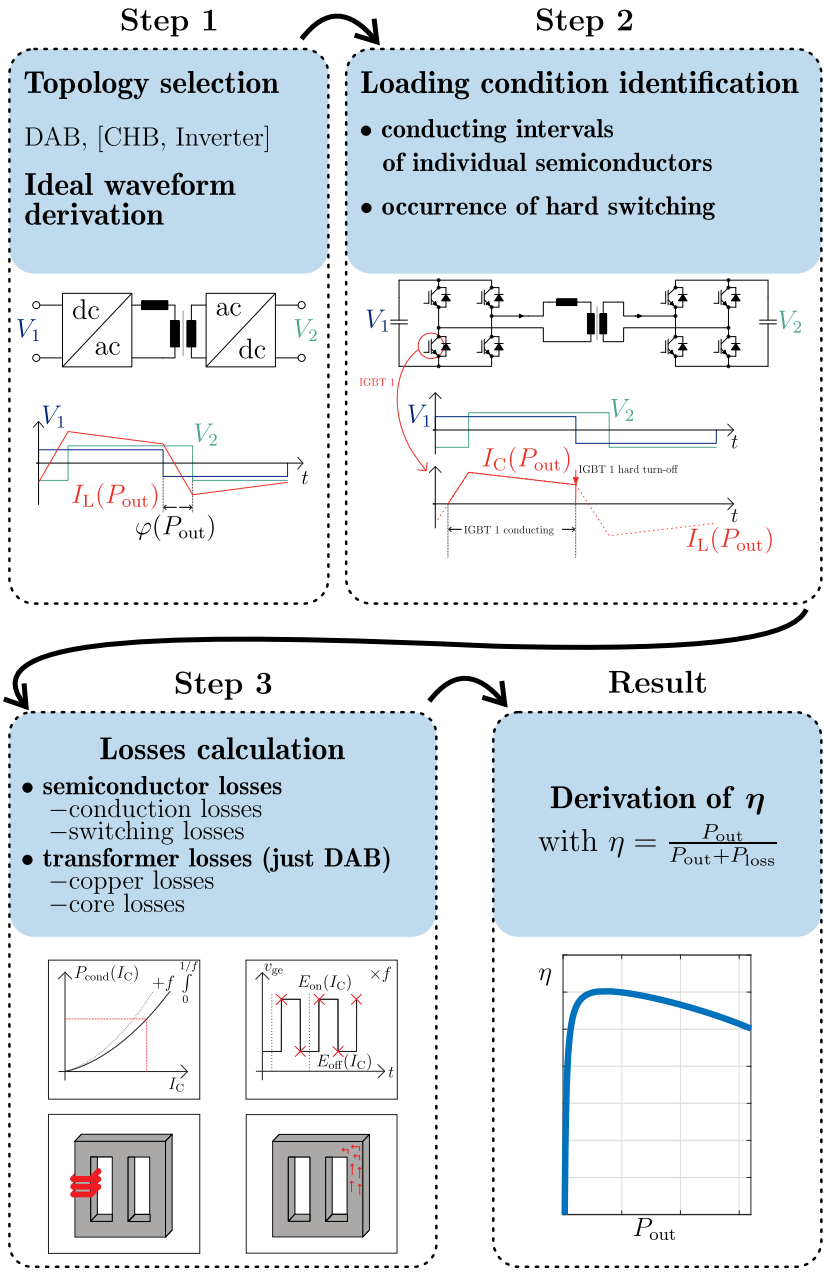


Fig. 3.3: Modeling method to derive efficiency curves of the converters.

The substeps to calculate the efficiency curves of the converters in main step 1 are illustrated in Fig. 3.3 on the example of a DAB. After selecting the converter topology, the ideal waveforms of the converter are derived in dependency on the output power of the converter P_{out} in the first substep. These ideal waveforms of the converters can be calculated based on the equations given in Section 2.3. The second substep is the identification of the loading conditions on the semiconductors during hard switching and of the conducting intervals. Afterwards, the semiconductor conduction and switching losses as well as the copper and core losses of the transformer are calculated in the third substep. These calculations of the losses are done as explained in Section 2.3. Finally, the converter efficiency can be calculated based on the output power P_{out} and the losses of the converter P_{loss}. An output power depending efficiency curve of the converter can be received by repeating this procedure for different output powers of the converter

$$\eta(P_{\text{out}}) = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{loss}}(P_{\text{out}}) + P_{\text{out}}} \quad . \tag{3.3}$$

The efficiency curves of the different converters that are necessary for the execution of the non-conserved power flow analysis in main step 2 are shown in the graphs of the NIT and the IT in Fig. 3.4. The system efficiencies of the NIT and the IT are calculated for all considered

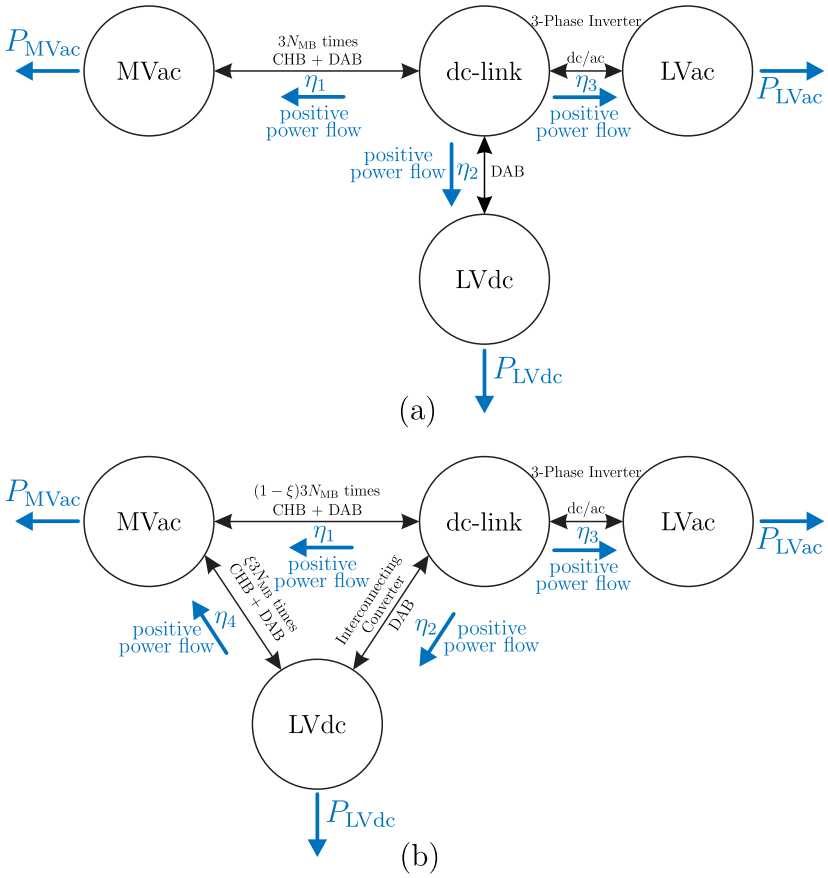


Fig. 3.4: Graph representation with converter efficiency curves and their power direction for (a) the non-interconnected topology and (b) the interconnected topology.

combinations of power consumption and generation in LVac and LVdc grid (P_{LVac} and P_{LVdc}). Depending on which grids provide power input to the system $P_{\mathrm{sys,in}}$ and which power output $P_{\mathrm{sys,out}}$, the efficiency of the converter system can be calculated by

$$\eta_{\mathrm{sys}}(P_{\mathrm{LVac}},P_{\mathrm{LVdc}}) = \frac{P_{\mathrm{sys,out}}}{P_{\mathrm{sys,in}}} = \begin{cases} \frac{P_{\mathrm{LVac}}+P_{\mathrm{LVdc}}}{|P_{\mathrm{MVac}}|} & \text{if } P_{\mathrm{LVac}} \geq 0 \wedge P_{\mathrm{LVdc}} \geq 0 \\ \frac{P_{\mathrm{LVdc}}}{|P_{\mathrm{LVac}}+P_{\mathrm{MVac}}|} & \text{if } P_{\mathrm{LVac}} \leq 0 \wedge P_{\mathrm{LVdc}} \geq 0 \wedge P_{\mathrm{MVac}} \leq 0 \\ \frac{P_{\mathrm{LVdc}}+P_{\mathrm{MVac}}}{|P_{\mathrm{LVac}}|} & \text{if } P_{\mathrm{LVac}} \leq 0 \wedge P_{\mathrm{LVdc}} \geq 0 \wedge P_{\mathrm{MVac}} \geq 0 \\ \frac{P_{\mathrm{LVac}}}{|P_{\mathrm{LVdc}}+P_{\mathrm{MVac}}|} & \text{if } P_{\mathrm{LVac}} \geq 0 \wedge P_{\mathrm{LVdc}} \leq 0 \wedge P_{\mathrm{MVac}} \leq 0 \\ \frac{P_{\mathrm{LVac}}+P_{\mathrm{MVac}}}{|P_{\mathrm{LVdc}}|} & \text{if } P_{\mathrm{LVac}} \geq 0 \wedge P_{\mathrm{LVdc}} \leq 0 \wedge P_{\mathrm{MVac}} \geq 0 \\ \frac{P_{\mathrm{MVac}}}{|P_{\mathrm{LVac}}+P_{\mathrm{LVdc}}|} & \text{if } P_{\mathrm{LVac}} \leq 0 \wedge P_{\mathrm{LVdc}} \leq 0 \end{cases} . \tag{3.4}$$

The active power that is drawn from or fed into the MVac grid P_{MVac} results from the LV powers and the losses in the converter system, which are considered via the efficiency curves of the converters. For the NIT, the active power that is drawn from or fed into the MVac grid P_{MVac} can be calculated by

$$P_{\mathrm{MVac}} = \begin{cases} \frac{-\left(\frac{P_{\mathrm{LVac}}}{\eta_3}+\frac{P_{\mathrm{LVdc}}}{\eta_2}\right)}{\eta_1} & \text{if } P_{\mathrm{LVac}} \geq 0 \wedge P_{\mathrm{LVdc}} \geq 0 \\ \frac{-\left(P_{\mathrm{LVac}}\eta_3+\frac{P_{\mathrm{LVdc}}}{\eta_2}\right)}{\eta_1} & \text{if } P_{\mathrm{LVac}} \leq 0 \wedge P_{\mathrm{LVdc}} \geq 0 \wedge |P_{\mathrm{LVac}}\eta_3| \leq \frac{P_{\mathrm{LVdc}}}{\eta_2} \\ \left(|P_{\mathrm{LVac}}\eta_3| - \frac{P_{\mathrm{LVdc}}}{\eta_2}\right)\eta_1 & \text{if } P_{\mathrm{LVac}} \leq 0 \wedge P_{\mathrm{LVdc}} \geq 0 \wedge |P_{\mathrm{LVac}}\eta_3| \geq \frac{P_{\mathrm{LVdc}}}{\eta_2} \\ \frac{-\left(\frac{P_{\mathrm{LVac}}}{\eta_3}+P_{\mathrm{LVdc}}\eta_2\right)}{\eta_1} & \text{if } P_{\mathrm{LVac}} \geq 0 \wedge P_{\mathrm{LVdc}} \leq 0 \wedge |P_{\mathrm{LVdc}}\eta_2| \leq \frac{P_{\mathrm{LVac}}}{\eta_3} \\ \left(|P_{\mathrm{LVdc}}\eta_2| - \frac{P_{\mathrm{LVac}}}{\eta_3}\right)\eta_1 & \text{if } P_{\mathrm{LVac}} \geq 0 \wedge P_{\mathrm{LVdc}} \leq 0 \wedge |P_{\mathrm{LVdc}}\eta_2| \geq \frac{P_{\mathrm{LVac}}}{\eta_3} \\ |P_{\mathrm{LVac}}\eta_3 + P_{\mathrm{LVdc}}\eta_2|\,\eta_1 & \text{if } P_{\mathrm{LVac}} \leq 0 \wedge P_{\mathrm{LVdc}} \leq 0 \end{cases} . \tag{3.5}$$

For the IT, the calculation of P_{MVac} is more complex than for the NIT, because of the link ratio configuration ξ that has to be taken into account. Furthermore, additional auxiliary variables are needed to distinguish the cases of forward and backward power flow through the interconnecting DAB

$$P_{\mathrm{aux,1}} = \left| \frac{1}{1-\xi} \frac{-\frac{P_{\mathrm{LVac}}}{\eta_3}}{\eta_1} \right| , \tag{3.6}$$

$$P_{\mathrm{aux,2}} = \left| \frac{1}{\xi} \frac{-P_{\mathrm{LVdc}}}{\eta_4} \right| , \tag{3.7}$$

$$P_{\mathrm{aux,3}} = \frac{1}{1-\xi} \left(-(P_{\mathrm{LVac}}\eta_3)\right) \eta_1 , \tag{3.8}$$

$$P_{\mathrm{aux,4}} = \frac{1}{\xi}(-P_{\mathrm{LVdc}})\eta_4 . \tag{3.9}$$

The active power that is drawn from or fed into the MVac grid P_{MVac} can be calculated for

the IT by solving one of following equations depending on the operation point

$$
\begin{aligned}
&\text{If } P_{\text{LVac}} \geq 0 \wedge P_{\text{LVdc}} \geq 0 \wedge P_{\text{aux,1}} \geq P_{\text{aux,2}}: \\
&\quad ((\xi P_{\text{MVac}})\eta_4 + P_{\text{LVdc}})\,\eta_2 + ((1-\xi)P_{\text{MVac}})\eta_1 + \frac{P_{\text{LVac}}}{\eta_3} = 0 \\
&\text{If } P_{\text{LVac}} \geq 0 \wedge P_{\text{LVdc}} \geq 0 \wedge P_{\text{aux,1}} \leq P_{\text{aux,2}}: \\
&\quad P_{\text{LVdc}} - \left(-((1-\xi)P_{\text{MVac}})\eta_1 - \frac{P_{\text{LVac}}}{\eta_3}\right)\eta_2 + (\xi P_{\text{MVac}})\eta_4 = 0 \\
&\text{If } P_{\text{LVac}} \leq 0 \wedge P_{\text{LVdc}} \geq 0 \wedge |P_{\text{LVac}}\eta_3| \leq \frac{P_{\text{LVdc}}}{\eta_2}: \\
&\quad \frac{P_{\text{LVdc}} + (\xi P_{\text{MVac}})\eta_4}{\eta_2} + P_{\text{LVac}}\eta_3 + ((1-\xi)P_{\text{MVac}})\eta_1 = 0 \\
&\text{If } P_{\text{LVac}} \leq 0 \wedge P_{\text{LVdc}} \geq 0 \wedge |P_{\text{LVac}}\eta_3| \geq \frac{P_{\text{LVdc}}}{\eta_2}: \\
&\quad P_{\text{MVac}} - \frac{1}{1-\xi}\left(|P_{\text{LVac}}\eta_3| - \frac{P_{\text{LVdc}} + \frac{\xi P_{\text{MVac}}}{\eta_4}}{\eta_2}\right)\eta_1 = 0 \\
&\text{If } P_{\text{LVac}} \geq 0 \wedge P_{\text{LVdc}} \leq 0 \wedge |P_{\text{LVdc}}\eta_2| \leq \frac{P_{\text{LVac}}}{\eta_3}: \\
&\quad (P_{\text{LVdc}} + (\xi P_{\text{MVac}})\eta_4)\eta_2 + \frac{P_{\text{LVac}}}{\eta_3} + ((1-\xi)P_{\text{MVac}})\eta_1 = 0 \\
&\text{If } P_{\text{LVac}} \geq 0 \wedge P_{\text{LVdc}} \leq 0 \wedge |P_{\text{LVdc}}\eta_2| \geq \frac{P_{\text{LVac}}}{\eta_3}: \\
&\quad P_{\text{MVac}} - \frac{1}{\xi}\left(|P_{\text{LVdc}}| + \frac{-\left(\frac{P_{\text{LVac}}}{\eta_3} + \frac{(1-\xi)P_{\text{MVac}}}{\eta_1}\right)}{\eta_2}\right)\eta_4 = 0 \\
&\text{If } P_{\text{LVac}} \leq 0 \wedge P_{\text{LVdc}} \leq 0 \wedge P_{\text{aux,3}} \geq P_{\text{aux,4}}: \\
&\quad P_{\text{MVac}} - \frac{1}{1-\xi}\left(|P_{\text{LVac}}\eta_3| - \frac{P_{\text{LVdc}} + \frac{\xi P_{\text{MVac}}}{\eta_4}}{\eta_2}\right)\eta_1 = 0 \\
&\text{If } P_{\text{LVac}} \leq 0 \wedge P_{\text{LVdc}} \leq 0 \wedge P_{\text{aux,3}} \leq P_{\text{aux,4}}: \\
&\quad P_{\text{MVac}} - \frac{1}{\xi}\left(|P_{\text{LVdc}}| + \frac{-\left(P_{\text{LVac}}\eta_3 + \frac{(1-\xi)P_{\text{MVac}}}{\eta_1}\right)}{\eta_2}\right)\eta_4 = 0 \qquad .
\end{aligned}
\tag{3.10}
$$

A trust-region-dogleg algorithm in Matlab is used to solve these equations. Whenever a multiplication by an efficiency curve in the calculation of P_{MVac} for NIT or IT takes place, it must be taken into account that the efficiency curves defined by (3.3) are related to the output power of the converter. However, when multiplying the efficiency curve, the input power of the converter is available and its output power is searched for. Therefore, it is necessary to calculate the output power multiple times - always considering the efficiency value for the latest output power calculated. This iteration is repeated until a low deviation between the resulting output power and the output power of the taken efficiency value is reached.

3.2. Design of converter power rating for hybrid grids-feeding STs

This section deals with the design of the power rating of the converters in the NIT and the IT. Fig. 3.5 shows the general form of the borders of the possible operation due to the limitations by the power ratings of the different converters for both topologies and how their combination leads to the permissible operation areas (marked in yellow). Herein, the borders by the CHB and the three phase inverter are equal for NIT and IT. However, the borders by the interconnecting DAB of the IT change not only based on the power rating of the converter, but also with readjusting the configuration of the topology via the link ratio ξ. Choosing higher link ratios rotates the line of unloaded interconnecting DAB operation (dashed black line in Fig. 3.5 (b)) around the origin of the coordinate system from the x-axis (LVac power) towards the y-axis (LVdc power). The borders due to the interconnecting DAB rating rotate as well and stay parallel to this line of unloaded operation. The NIT does not have a configuration choice. Therefore, the borders by the LVdc DAB only depend on its power rating.

In this section, the mission profile-based design procedure for determining the power rating of the converters, the evaluation of the downsizing possibility of the interconnecting DAB compared to the LVdc DAB and the Monte Carlo-based sensitivity analysis of the derived converter power ratings against deviations of the considered mission profiles are made considering the following assumptions:

- **Assumption 1:** Conserved power flows are considered to facilitate the analysis, which means that the losses of converters are not added to the loading of other converters (system input power equal to system output power). Errors due to this simplification can be handled via the safety margin that should be applied to converter power ratings after the design procedure.
- **Assumption 2:** An equal distribution of the MVac active power over all MVac PEBBs is considered. This equal distribution will be ensured via balancing control schemes during normal operation. However, if advanced control algorithms like active power

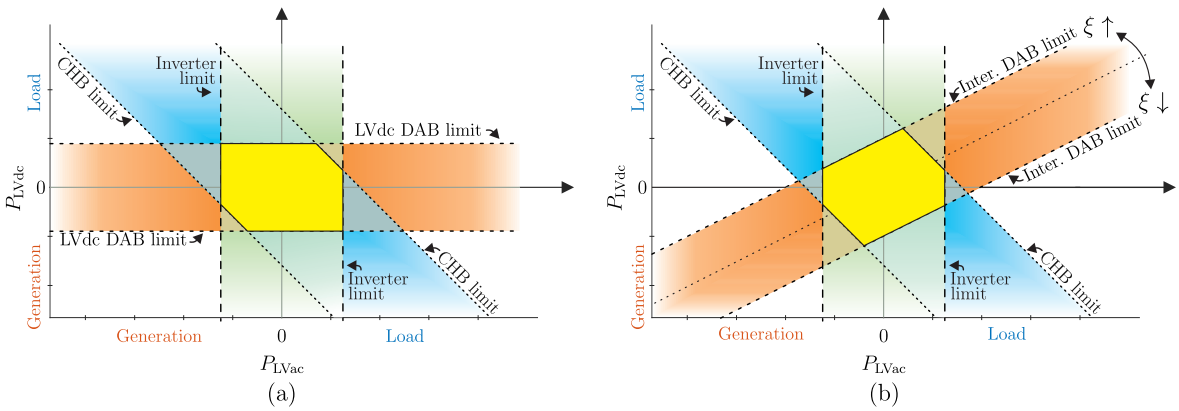


Fig. 3.5: General form of the borders of the possible operation due to converter power limitations for (a) the NIT and (b) the IT as well as the resulting permissible operation areas (marked in yellow).

routing [54] are applied, caution not to overload single PEBBs must be taken when operating the system close to its maximum rated power.

3.2.1. Mission profile-based converter power rating design

The hybrid mission profile considered for the design of the power ratings of the converters in NIT and IT consist of a set M of operation points, which are described via 2-tuples $(P_{\mathrm{LVac}}\ P_{\mathrm{LVdc}})$ of the active LVac power P_{LVac} and the LVdc power P_{LVdc}. This information of one operation point under the assumptions made is sufficient to determine the loading (processed active power) of all converters in this operation point. The active power of the MVac grid P_{MVac} results from the necessity to have the same active input power as active output power (assumption 1 made for this section). The power ratings of the converters are derived via calculation of the converter loadings in all operation points and extraction of the maximum loadings.

The power ratings of converters which result in borders of the operation area parallel to one of the axes (Fig. 3.5) only depend on one of the profiles P_{LVac} or P_{LVdc}, but are not dependent on how these profiles are combined to a hybrid mission profile. This is the case for the three phase inverter as well as the LVdc DAB in the NIT. The power rating of the three phase inverter $P_{\mathrm{inv}}^{\mathrm{max}}$, which is equal for NIT and IT, only depends on the power profile of the LVac grid

$$P_{\mathrm{inv}}^{\mathrm{max}} = P_{\mathrm{LVac}}^{\mathrm{max}} = \max_{(P_{\mathrm{LVac}}\ P_{\mathrm{LVdc}})\in M} \left\{ |P_{\mathrm{LVac}}| \right\} \ . \tag{3.11}$$

Further, the power rating of the LVdc DAB $P_{\mathrm{DAB,NIT}}^{\mathrm{max}}$ in the NIT only depends on the power profile of the LVdc grid

$$P_{\mathrm{DAB,NIT}}^{\mathrm{max}} = P_{\mathrm{LVdc}}^{\mathrm{max}} = \max_{(P_{\mathrm{LVac}}\ P_{\mathrm{LVdc}})\in M} \left\{ |P_{\mathrm{LVdc}}| \right\} \ . \tag{3.12}$$

The power rating of the CHB cells as well as of the DABs in series to each CHB cell (both together forming an MVac PEBB) $P_{\mathrm{MVac,PEBB}}^{\mathrm{max}}$ depends on the combined hybrid mission profile

$$P_{\mathrm{MVac,PEBB}}^{\mathrm{max}} = \max_{(P_{\mathrm{LVac}}\ P_{\mathrm{LVdc}})\in M} \left\{ |P_{\mathrm{LVac}} + P_{\mathrm{LVdc}}| \right\} \frac{1}{3\,N_{\mathrm{MB}}} \ . \tag{3.13}$$

Deriving the required power rating of a single MVac PEBB considers an equal power distribution among the $3\,N_{\mathrm{MB}}$ MVac PEBBs (assumption 2 made for this section). The power rating of the MVac PEBBs is equal for NIT and IT, because it depends only on the total output power of the system.

The active power flowing through the interconnecting DAB $P_{\mathrm{DAB,IT}}$ in the IT changes not only based on the operation points of the hybrid mission profile, but is also dependent on the configuration of the IT described by the link ratio ξ introduced in Section 3.1. All power

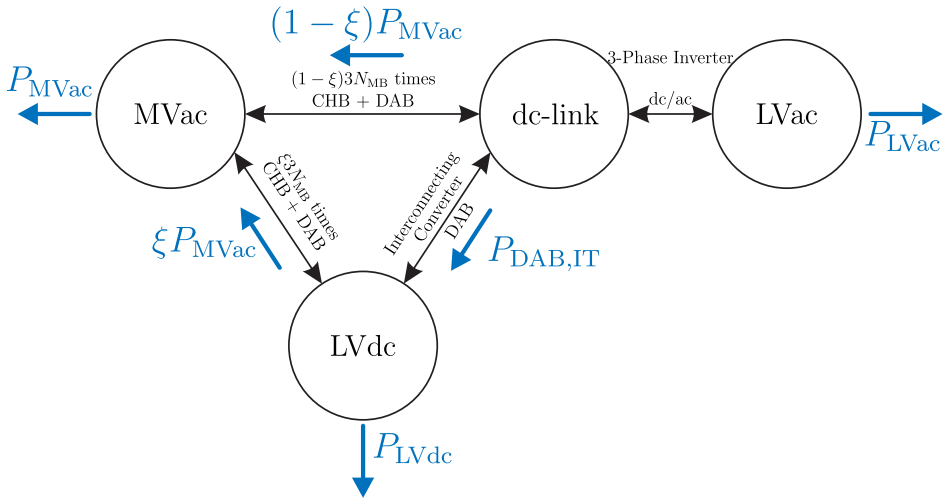


Fig. 3.6: Graph representation of the IT with power flows to derive interconnecting DAB loading.

flows in the IT can be seen in Fig. 3.6, where the positive direction of the power flows is always defined as flowing out of the converter system. According to assumption 1 made for this section, the sum of the active MVac, LVac and LVdc power results in

$$P_{\mathrm{MVac}} + P_{\mathrm{LVac}} + P_{\mathrm{LVdc}} = 0 \ . \tag{3.14}$$

Further, the sum of the part of the MVac power exchanged with the LVdc feeder, which is defined by the link ratio, the power consumed by the LVdc grid and the power flowing from dc-link to the LVdc feeder needs to be

$$\xi P_{\mathrm{MVac}} + P_{\mathrm{LVdc}} - P_{\mathrm{DAB,IT}} = 0 \ . \tag{3.15}$$

Inserting (3.14) into (3.15) gives

$$\xi(-P_{\mathrm{LVac}} - P_{\mathrm{LVdc}}) + P_{\mathrm{LVdc}} - P_{\mathrm{DAB,IT}} = 0 \ . \tag{3.16}$$

By rearranging (3.16) the power flow through the interconnecting DAB can be expressed as

$$P_{\mathrm{DAB,IT}} = (1-\xi)P_{\mathrm{LVdc}} - \xi P_{\mathrm{LVac}} \ . \tag{3.17}$$

The power rating of the interconnecting DAB $P^{\mathrm{max}}_{\mathrm{DAB,IT}}(\xi)$ for each link ratio depending on the hybrid mission profile is

$$P^{\mathrm{max}}_{\mathrm{DAB,IT}}(\xi) = \max_{(P_{\mathrm{LVac}}\, P_{\mathrm{LVdc}}) \in M} \left\{ \left| (1-\xi)P_{\mathrm{LVdc}} - \xi P_{\mathrm{LVac}} \right| \right\} \ . \tag{3.18}$$

After deriving the power ratings for the converters a safety margin should be added to counteract deviations of the real profiles from the considered hybrid mission profile and compen-

sating errors by the simplification of considering conserved power flows (assumption 1 made for this section).

3.2.2. Downsizing opportunity of interconnecting dual active bridge

The dependency of the interconnecting DAB power rating on the configuration of the IT in (3.18) provides the possibility of a downsizing compared to the LVdc DAB power rating in the NIT (3.12). A link ratio for optimal downsizing of the interconnecting DAB power rating can be found for each hybrid mission profile considered.

The downsizing potential for all combinations of LVac and LVdc profiles shown in Fig. 3.7 is examined. The considered load profiles for the LVac grid are from the German Association of Energy and Water Industries [55]. They give the standard power consumption for different consumer groups with 15 minutes resolution.

- The G0 standard profile represents the power consumption of general commercial loads.
- The G6 standard profile represents the power consumption of companies with high consumption on weekends, such as restaurants.
- The H0 standard profile represents the power consumption of private households.

All profiles are divided by the maximum power consumption within each of the standard profiles to have scalable profiles in per unit system. A factor of 0.64 is applied to all ac profiles (Fig. 3.7 (b)). The considered load profiles for the LVdc grid are derived via linear superposition of a PV power generation profile [56] and a power consumption profile of an EV charging station [57] (Fig. 3.7 (a)).

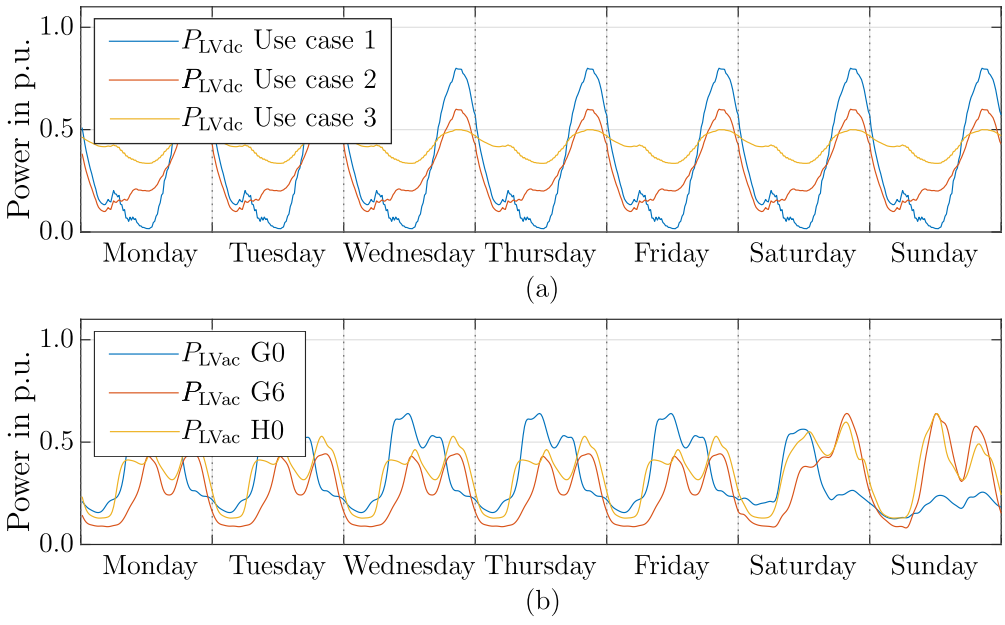


Fig. 3.7: Considered load profiles for (a) the LVdc grid and (b) the LVac grid.

- Use case 1 considers power consumption via EV charging stations and medium integration of PV generation (peak PV power generation is 33 % of peak EV charging power consumption). The maximum of the superimposed profile is scaled to 0.8 p.u..
- Use case 2 considers mainly power consumption via EV charging stations and minor integration of PV generation (maximum of PV power generation is 2 % of maximum EV charging power consumption). The maximum of the superimposed profile is scaled to 0.6 p.u..
- Use case 3 considers a constant base load of 0.4 p.u. and additional EV charging consumption and PV generation with a peak of 0.1 p.u. each.

Besides the power rating derivation for the LVdc DAB and the interconnecting DAB via (3.12) and (3.18), these power ratings can also be graphically derived or graphically represented for the purpose of comparison. For the LVdc DAB in the NIT, the line of operation points where the LVdc DAB loading is zero is on the x-axis (dashed yellow line in Fig. 3.8). The loading for specific operation points can be derived or represented by vectors parallel to the y-axis (P_{LVdc}-axis). Herein, the length of the vector can be directly converted to the LVdc DAB power loading with the scaling of the P_{LVdc}-axis.

However, if the needed converter power rating of the IT is derived or represented graphically, a distortion of the graphical length of vectors describing the interconnecting DAB loading (green vector in Fig. 3.8) must be considered. The rotation of the line of operation points with zero interconnecting DAB loading (dashed green line in Fig. 3.8) around the origin of the coordinate system can be described via the link ratio ξ

$$\varphi_{1-\xi} = \arctan\left(\frac{1-\xi}{\xi}\right) . \tag{3.19}$$

For the operation point shown in Fig. 3.8 with zero active LVac power, the length of the

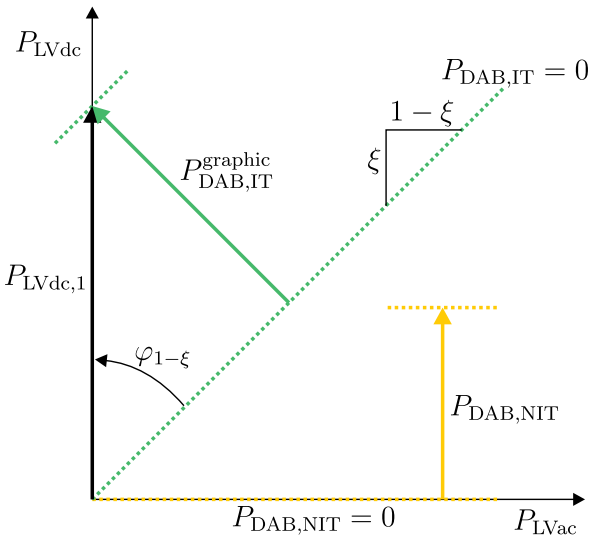


Fig. 3.8: Graphical derivation of LVdc DAB ($P_{\mathrm{DAB,NIT}}$) and interconnecting DAB ($P_{\mathrm{DAB,IT}}$) loading.

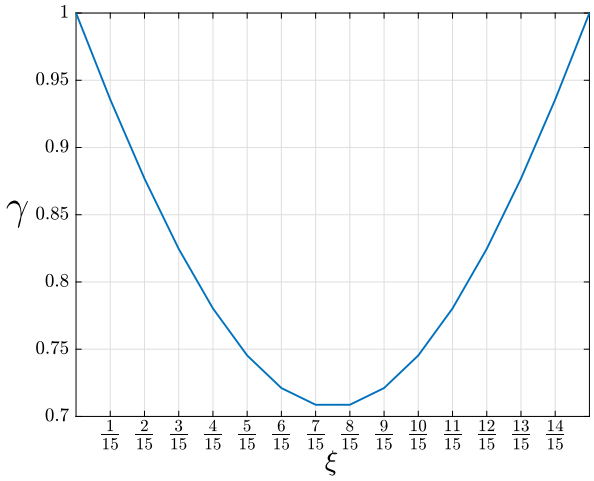


Fig. 3.9: Distortion γ between graphical and analytical derived interconnecting DAB loading dependent on ξ.

graphical interconnecting DAB loading vector, which is orthogonal to the line of operation points with zero interconnecting DAB loading, can be calculated with the LVdc power of this operation point $P_{\mathrm{LVdc},1}$ and the angle from (3.19)

$$P_{\mathrm{DAB,IT}}^{\mathrm{graphic}} = P_{\mathrm{LVdc},1} \sin\left(\varphi_{1-\xi}\right) \quad . \tag{3.20}$$

The interconnecting DAB loading of this operation point with zero active LVac power according to (3.17) is

$$P_{\mathrm{DAB,IT}} = (1-\xi) P_{\mathrm{LVdc},1}\Big|_{P_{\mathrm{LVac}=0}} \quad . \tag{3.21}$$

Inserting (3.19) and (3.21) into (3.20) provides

$$P_{\mathrm{DAB,IT}}^{\mathrm{graphic}} = P_{\mathrm{DAB,IT}} \frac{\sin\left(\arctan\left(\frac{1-\xi}{\xi}\right)\right)}{1-\xi} = \frac{P_{\mathrm{DAB,IT}}}{\sqrt{\xi^2+(1-\xi)^2}} \quad . \tag{3.22}$$

The simplification of the trigonometric functions can be made according to [58]

$$\sin(\alpha) = \frac{\tan(\alpha)}{\sqrt{1+\tan(\alpha)^2}} \quad . \tag{3.23}$$

Considering the distortion factor γ of the graphical representation in the P_{LVac}-P_{LVdc}-plane the interconnecting DAB power rating can be determined or represented graphically

$$P_{\mathrm{DAB,IT}}^{\mathrm{max,graphic}} = \frac{P_{\mathrm{DAB,IT}}^{\mathrm{max}}}{\sqrt{\xi^2+(1-\xi)^2}} = \frac{P_{\mathrm{DAB,IT}}^{\mathrm{max}}}{\gamma} \quad . \tag{3.24}$$

The values of the distortion factor γ for all considered configurations of the link ratio ξ are shown in Fig. 3.9. The graphical representation of the interconnecting DAB loading seems always bigger than it analytically is and this effect gets stronger moving towards an equal distribution of MVac PEBBs to the LVdc feeder and to the dc-link.

All combinations of the LVac power profiles with the LVdc profiles to hybrid mission profiles are evaluated concerning the downsizing possibility of the interconnecting DAB compared to the LVdc DAB. For this purpose, the graphical representation of the LVdc DAB sizing and of the interconnecting DAB sizing with link ratio for optimal downsizing together with the possibility of downsizing for all considered link ratios are shown for the combination of

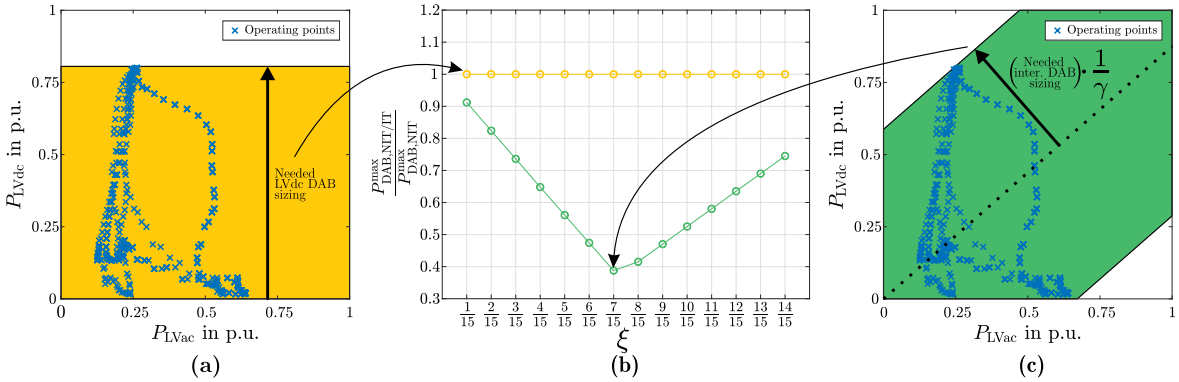


Fig. 3.10: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{7}{15}$) and (b) possibility of downsizing depending on the link ratio for G0 LVac and Use case 1 LVdc profiles.

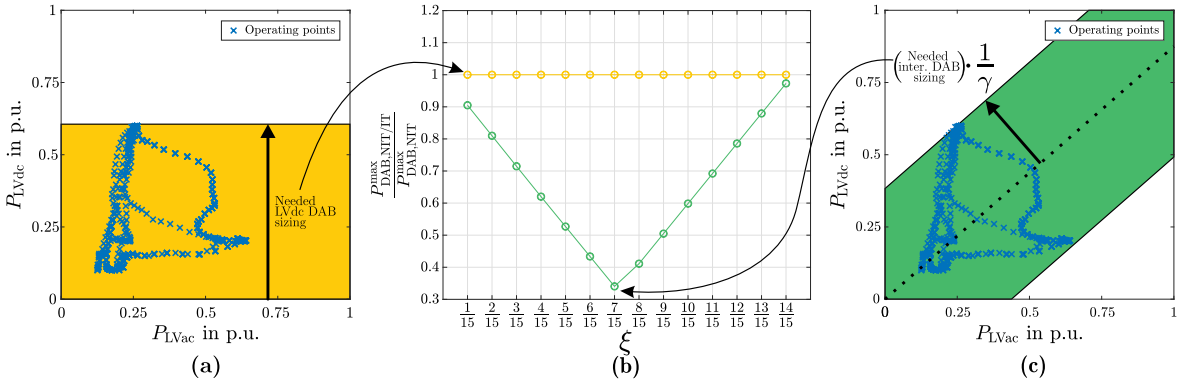


Fig. 3.11: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{7}{15}$) and (b) possibility of downsizing depending on the link ratio for G0 LVac and Use case 2 LVdc profiles.

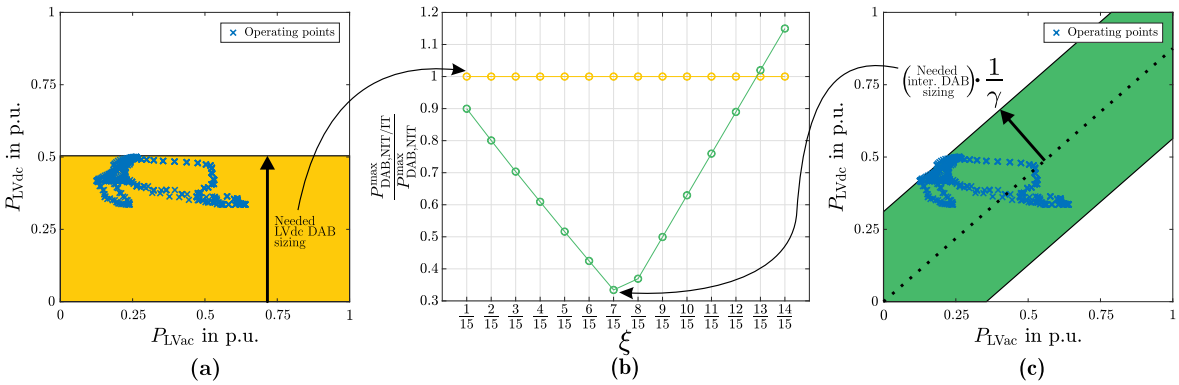


Fig. 3.12: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{7}{15}$) and (b) possibility of downsizing depending on the link ratio for G0 LVac and Use case 3 LVdc profiles.

G0 LVac and Use case 1 LVdc profiles in Fig. 3.10, the combination of G0 LVac and Use case 2 LVdc profiles in Fig. 3.11, the combination of G0 LVac and Use case 3 LVdc profiles in Fig. 3.12, the combination of G6 LVac and Use case 1 LVdc profiles in Fig. 3.13, the combination of G6 LVac and Use case 2 LVdc profiles in Fig. 3.14, the combination of G6 LVac and Use case 3 LVdc profiles in Fig. 3.15, the combination of H0 LVac and Use case

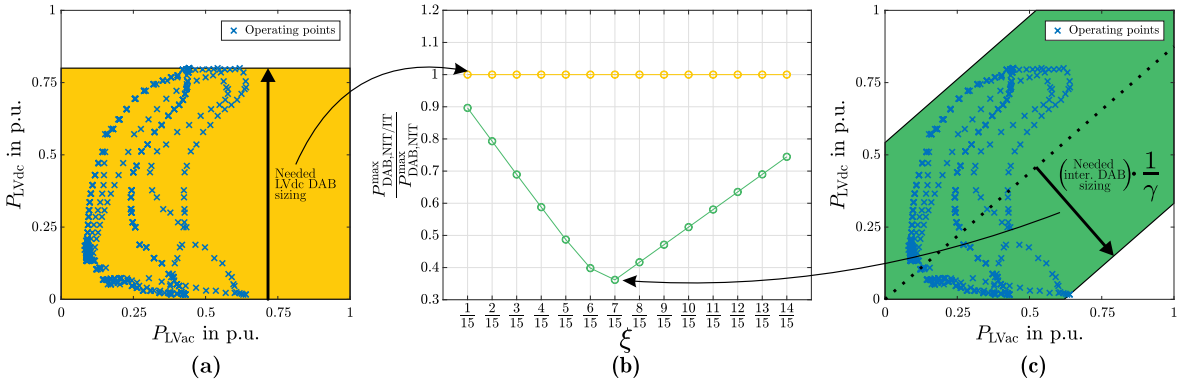


Fig. 3.13: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{7}{15}$) and (b) possibility of downsizing depending on the link ratio for G6 LVac and Use case 1 LVdc profiles.

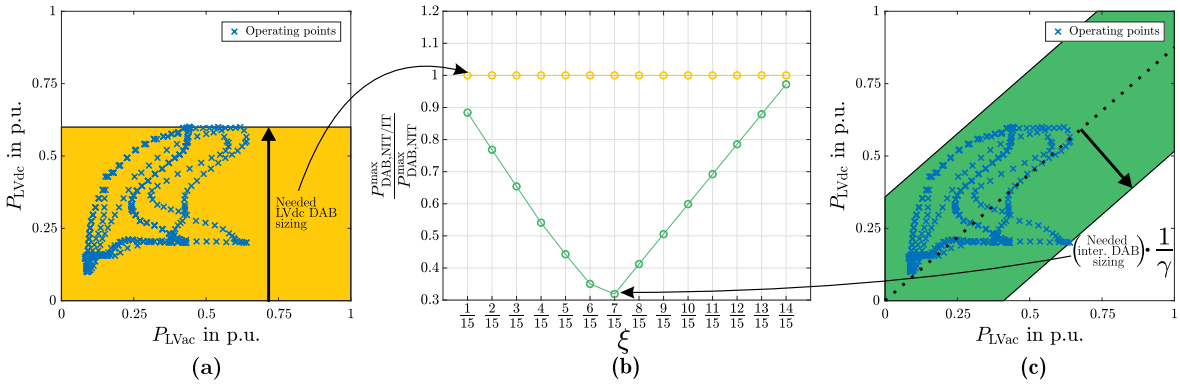


Fig. 3.14: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{7}{15}$) and (b) possibility of downsizing depending on the link ratio for G6 LVac and Use case 2 LVdc profiles.

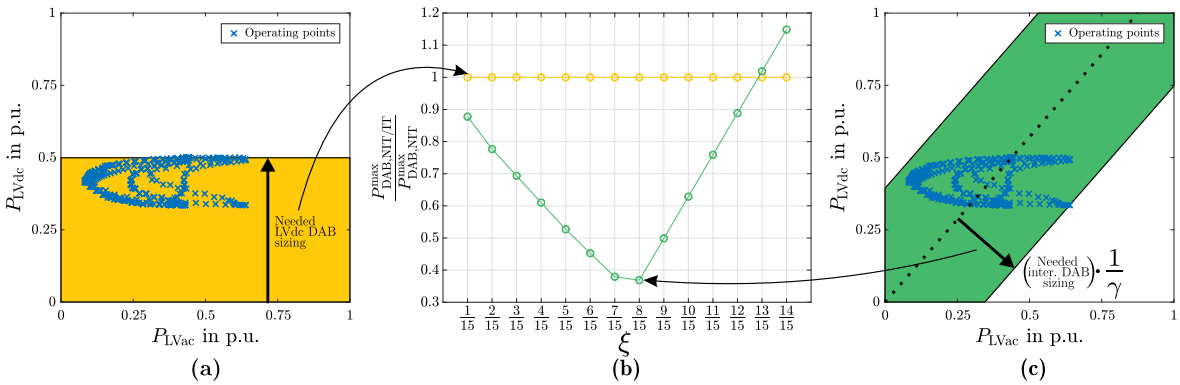


Fig. 3.15: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{8}{15}$) and (b) possibility of downsizing depending on the link ratio for G6 LVac and Use case 3 LVdc profiles.

1 LVdc profiles in Fig. 3.16, the combination of H0 LVac and Use case 2 LVdc profiles in Fig. 3.17, and the combination of H0 LVac and Use case 3 LVdc profiles in Fig. 3.18. For all considered hybrid mission profiles, a significant downsizing can be achieved by using the IT with appropriate link ratios. A downsizing of the interconnecting DAB power rating to values between 31 % (H0 LVac and Use case 2 LVdc) and 39 % (G0 LVac and Use case 1

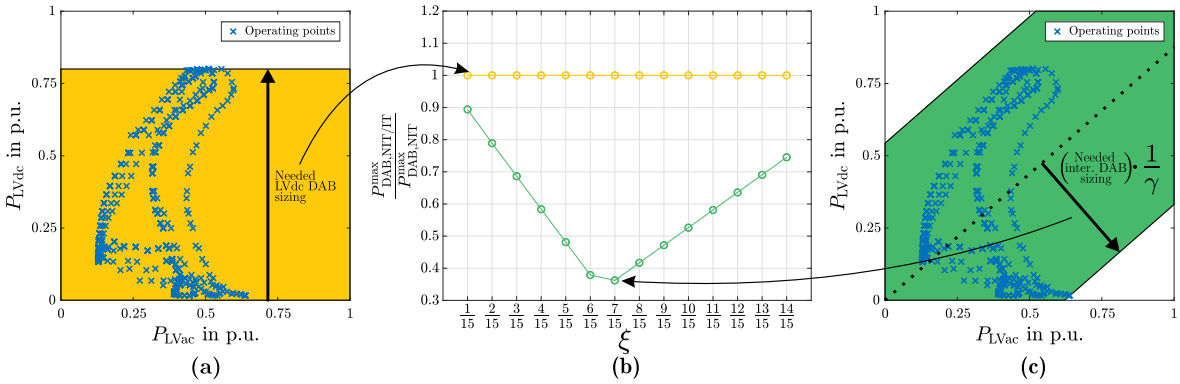


Fig. 3.16: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{7}{15}$) and (b) possibility of downsizing depending on the link ratio for H0 LVac and Use case 1 LVdc profiles.

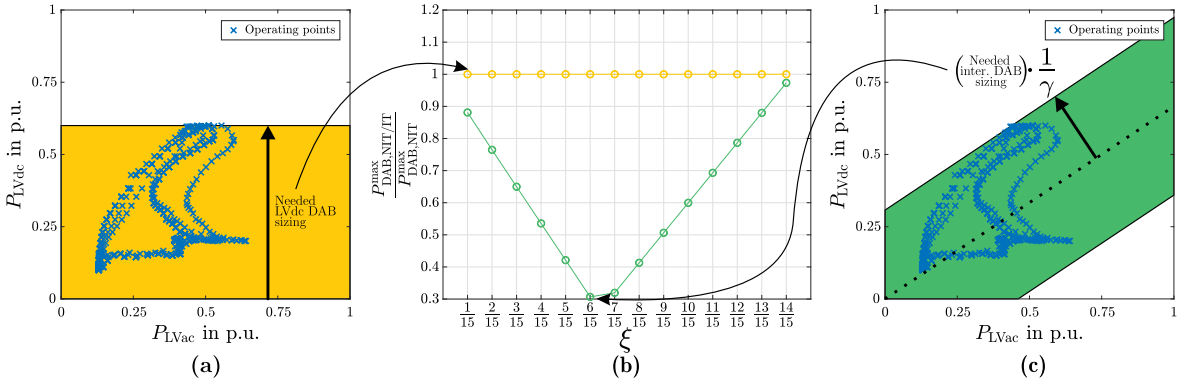


Fig. 3.17: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{6}{15}$) and (b) possibility of downsizing depending on the link ratio for H0 LVac and Use case 2 LVdc profiles.

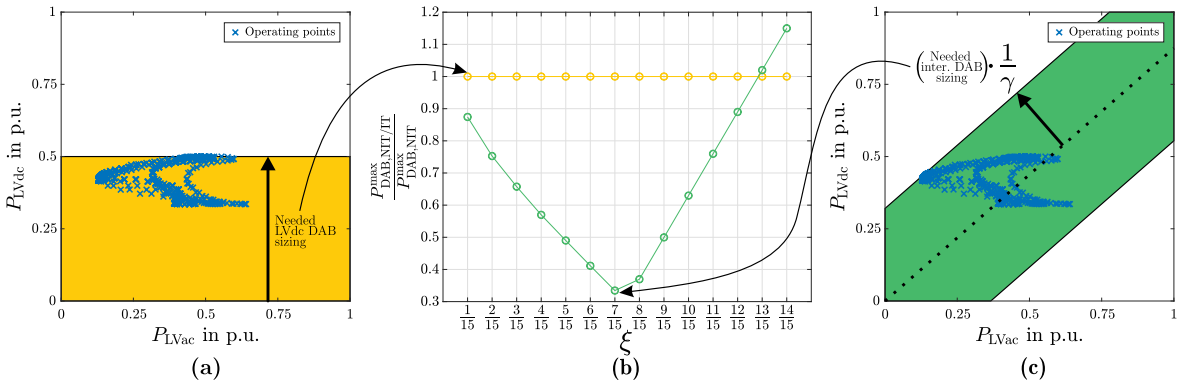


Fig. 3.18: Graphical determination of (a) LVdc DAB and (c) interconnecting DAB power rating ($\xi = \frac{7}{15}$) and (b) possibility of downsizing depending on the link ratio for H0 LVac and Use case 3 LVdc profiles.

LVdc) of the LVdc DAB power rating can be realized by choosing the optimal link ratio. However, choosing high values of the link ratio for the hybrid mission profiles - where Use case 3 is used as LVdc power profile - can lead to interconnecting DAB power ratings higher than the LVdc DAB power rating. Therefore, the knowledge of the hybrid mission profile is critical for choosing the optimal configuration of the link ratio in the IT in order to use the opportunity of downsizing.

3.2.3. Sensitivity of converter sizing against mission profile deviations

The applicability of the mission profile-based design procedure of the converter power ratings depends on the accurate knowledge of the hybrid mission profile. To handle uncertainties of the hybrid mission profile, the knowledge about the sensitivity of the converter sizing against deviation of the real hybrid mission profile from the one considered during the design is essential.

The power ratings of the converters, which only depend on one of the LV power profiles (P_{LVac} xor P_{LVdc}), are sensitive against deviations of this LV power profile and are independent of the other LV power profile. The required three phase inverter power rating (3.11) changes with the same percentage as the deviations of P_{LVac} and is independent of deviations of P_{LVdc}. The required LVdc DAB power rating (3.12) changes with the same percentage as the deviations of P_{LVdc} and is independent of deviations of P_{LVac}.

The power ratings of the MVac PEBBs (3.13) as well as of the interconnecting DAB (3.18) depend on both LV profiles. In order to investigate the sensitivity of these power ratings

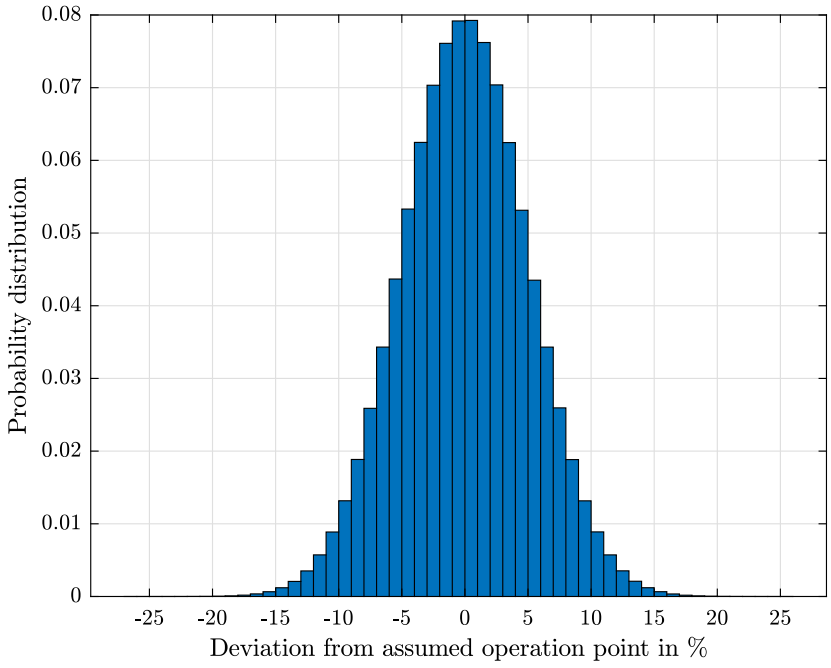


Fig. 3.19: Normal distribution with expected value of zero and three times the standard variation equal to 15 % for the Monte Carlo-based analysis of the power rating sensitivity.

towards deviations of the operation points from the assumed hybrid mission profile, a Monte Carlo-based method with dynamic parameters is utilized [59]. In this Monte Carlo-based method, deviations for the LVac as well as the LVdc powers are inserted for each single operation point. The deviations from the assumed powers are chosen randomly based on the normal distribution shown in Fig. 3.19. The resulting power ratings for the mission profiles with deviations - calculated with (3.13) and (3.18) - are one sample of the Monte Carlo-based method. For the sensitivity analysis of the converter power rating towards deviations of the assumed mission profiles, 10000 samples are considered and the distributions of resulting power ratings are evaluated for each combination of the LVac and LVdc mission profiles from Fig. 3.7.

The probability distribution as well as the cumulative distribution of the of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ are shown in Fig. 3.20 for the combination of G0 LVac and Use case 1 LVdc profiles, in Fig. 3.21 for the combination of G0 LVac and Use case 2 LVdc profiles, in Fig. 3.22 for the combination of G0 LVac and Use case 3 LVdc profiles, in Fig. 3.23 for the combination of G6 LVac and Use case 1 LVdc profiles, in Fig. 3.24 for the combination of G6 LVac and Use case 2 LVdc profiles, in Fig. 3.25 for the combination of G6 LVac and Use case 3 LVdc profiles, in Fig. 3.26 for the combination of H0 LVac and Use case 1 LVdc profiles, in Fig. 3.27 for the combination of H0 LVac and Use case 2 LVdc profiles, and in Fig. 3.28 for the combination of H0 LVac and Use case 3 LVdc profiles.

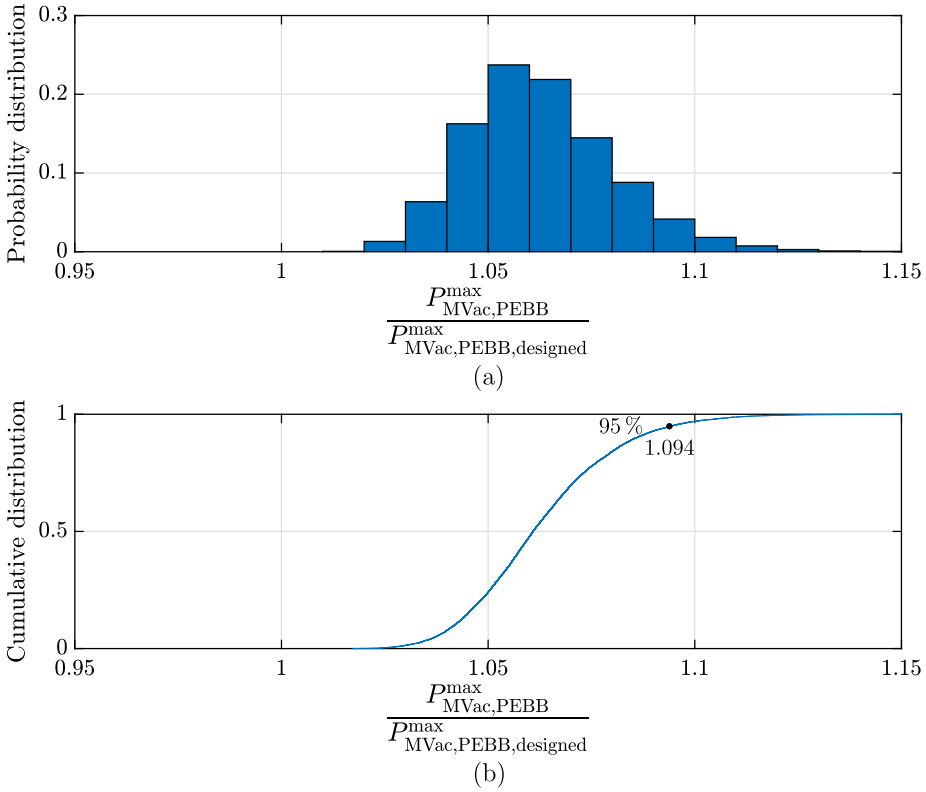


Fig. 3.20: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of G0 LVac and Use case 1 LVdc profiles.

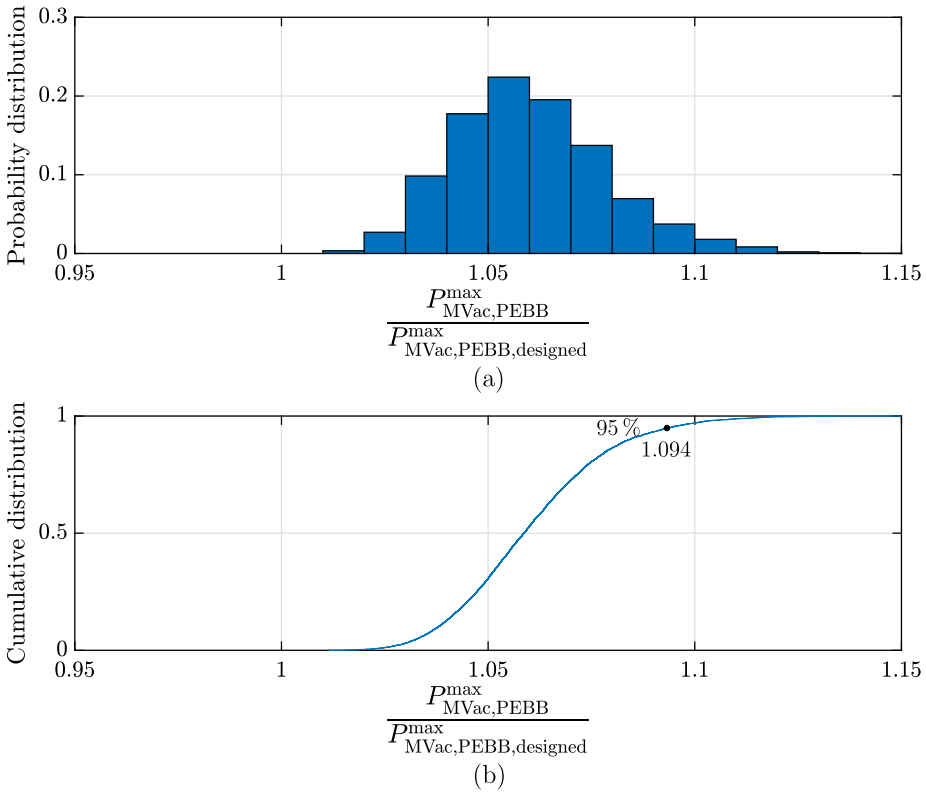


Fig. 3.21: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of G0 LVac and Use case 2 LVdc profiles.

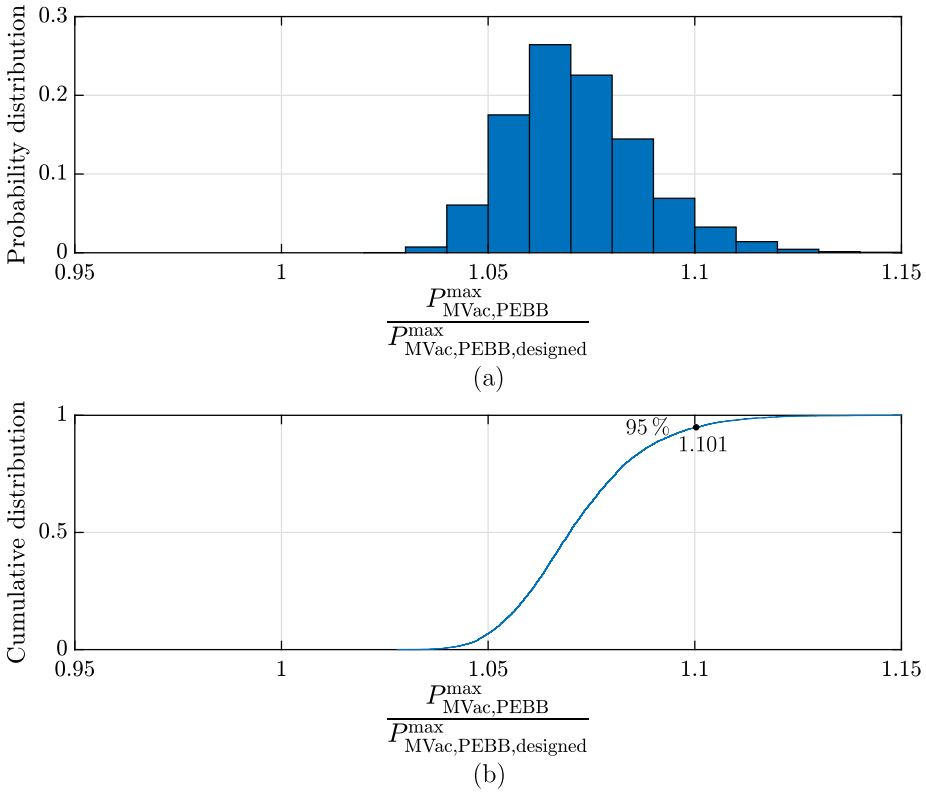


Fig. 3.22: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of G0 LVac and Use case 3 LVdc profiles.

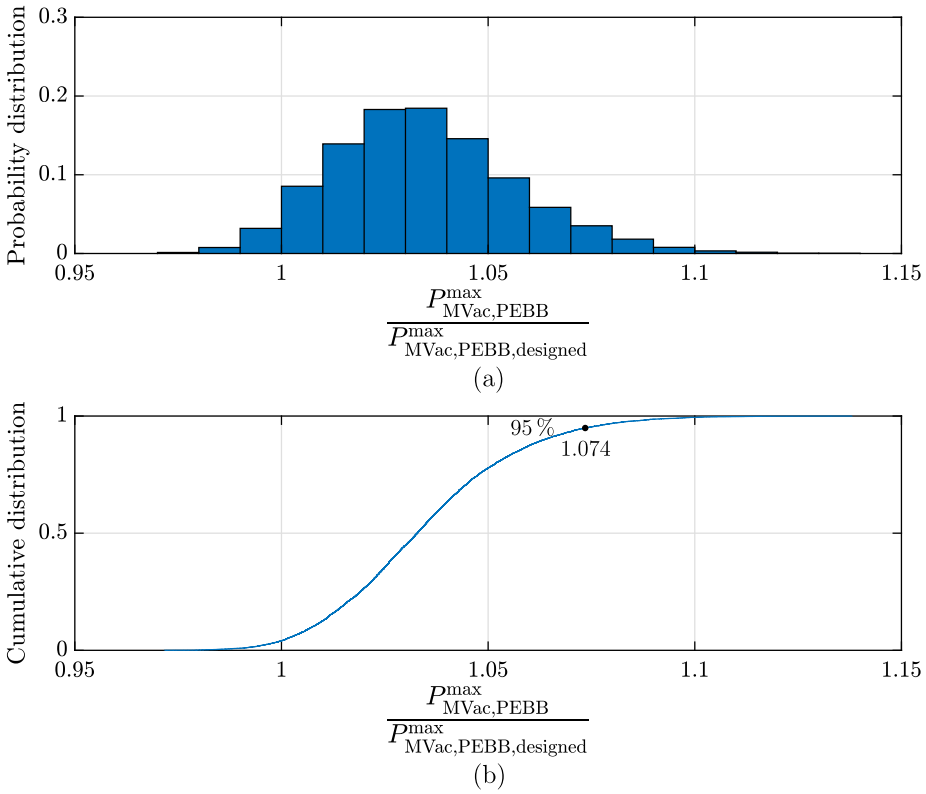


Fig. 3.23: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of G6 LVac and Use case 1 LVdc profiles.

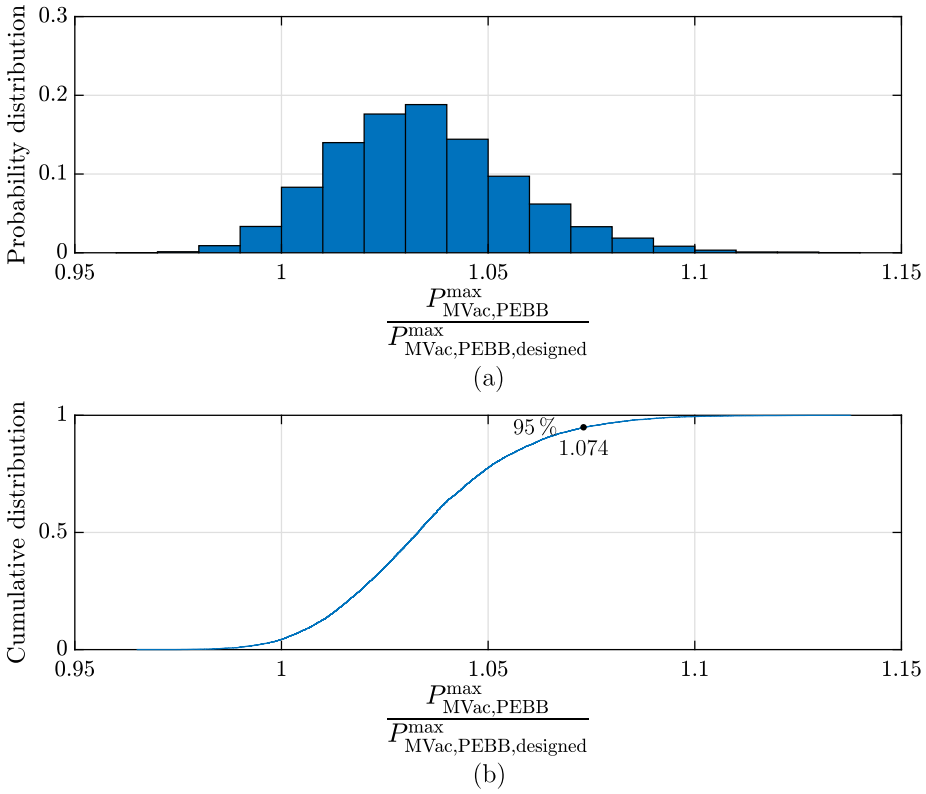


Fig. 3.24: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of G6 LVac and Use case 2 LVdc profiles.

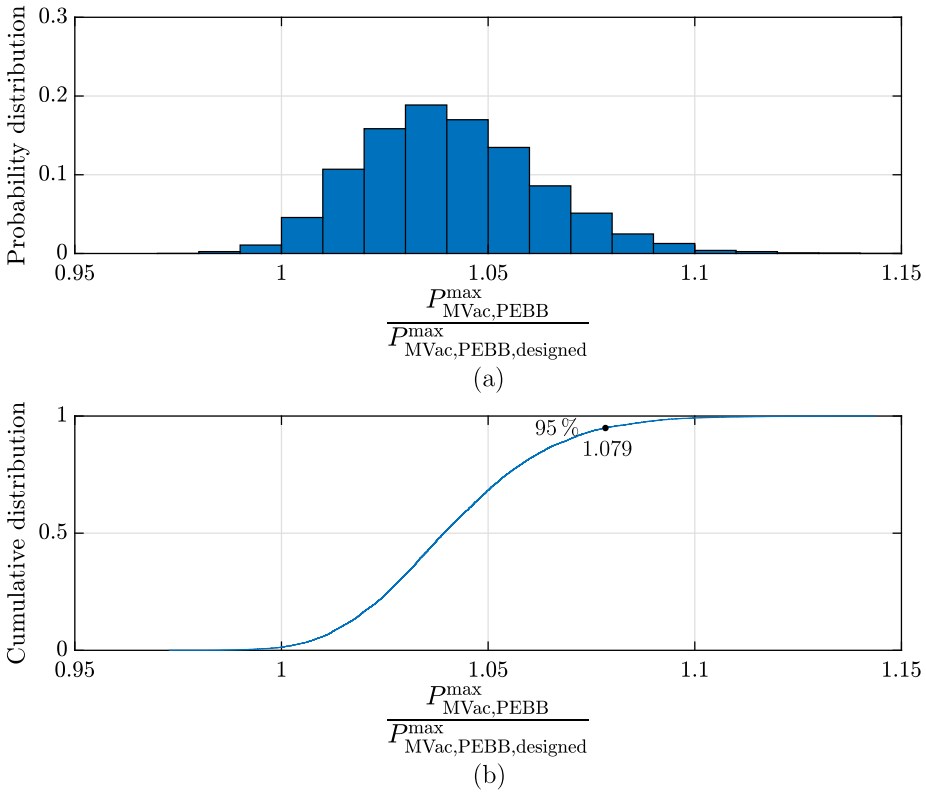


Fig. 3.25: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of G6 LVac and Use case 3 LVdc profiles.

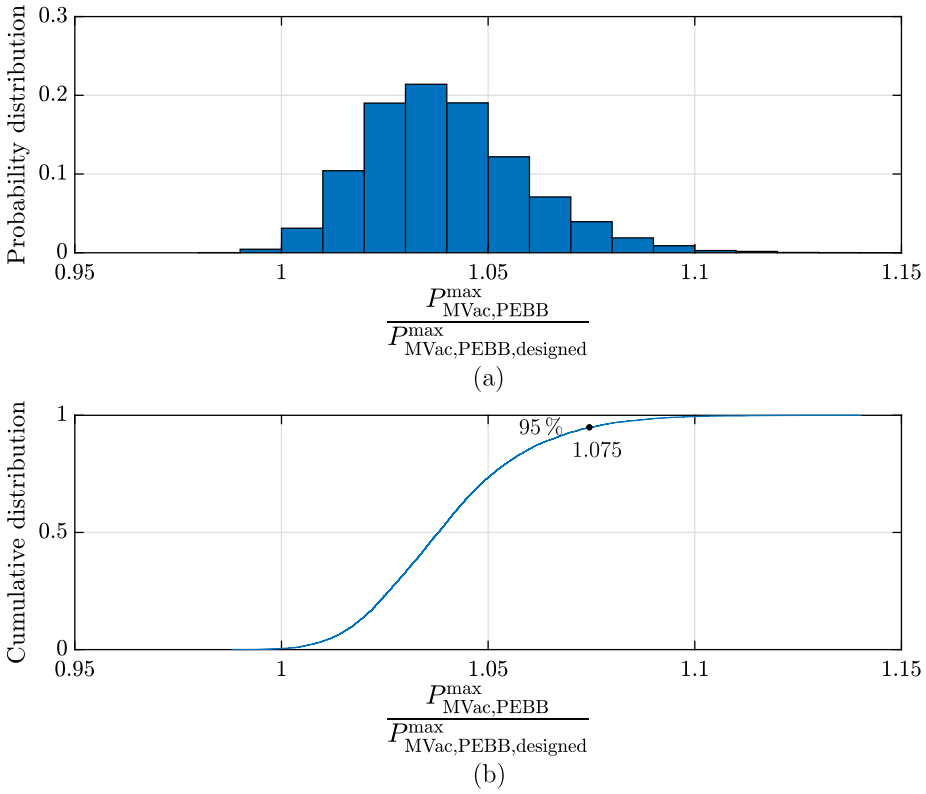


Fig. 3.26: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of H0 LVac and Use case 1 LVdc profiles.

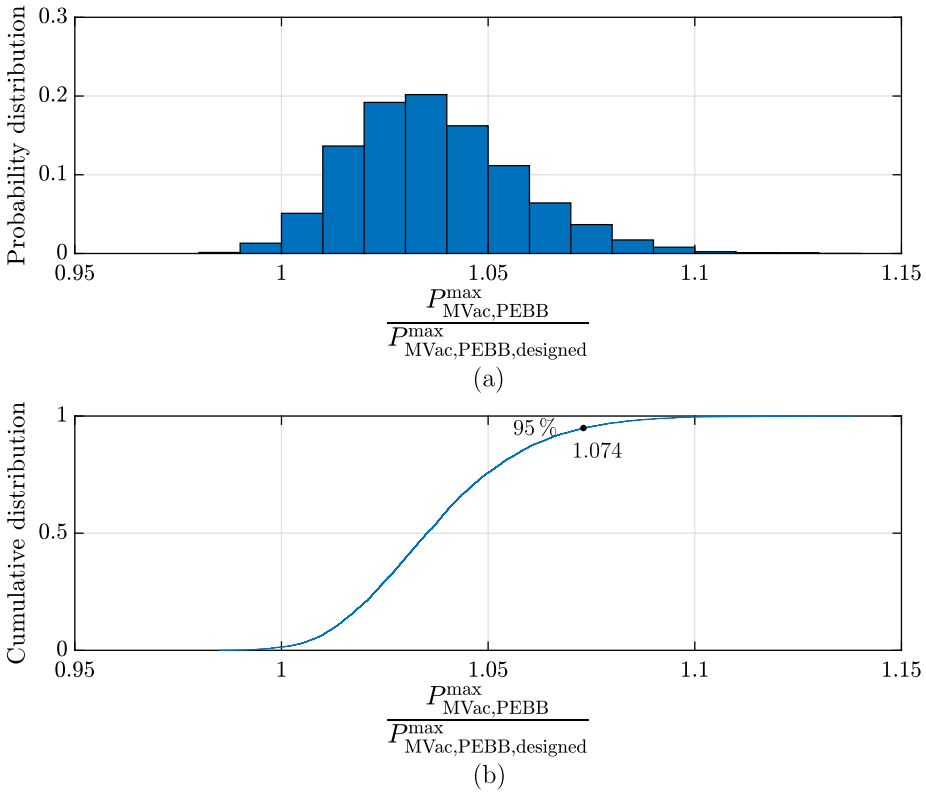


Fig. 3.27: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of H0 LVac and Use case 2 LVdc profiles.

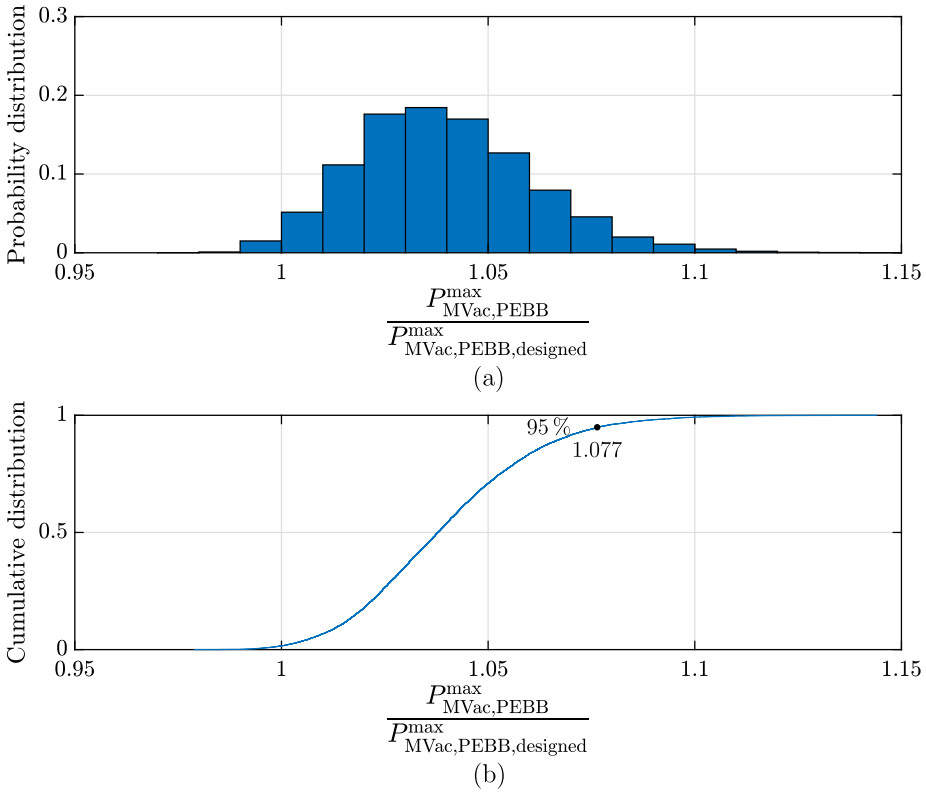


Fig. 3.28: (a) Probability distribution and (b) cumulative distribution of resulting MVac PEBB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{MVac,PEBB,designed}}$ for the combination of H0 LVac and Use case 3 LVdc profiles.

The required increase of the MVac PEBB power rating to cover 95 % of the samples from the Monte Carlo-based method is between 7.4 % - Fig. 3.23 (b), Fig. 3.24 (b), and Fig. 3.27 (b) - and 10.1 % - Fig. 3.22 (b) - for the considered operation point tolerance of 15 %. Herein, the coverage of 95 % of the samples can be taken as orientation for the rating design and the remaining samples can be covered via a safety margin.

The probability distributions of the of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\mathrm{DAB,IT,designed}}$ with and without possibility of link ratio reconfiguration are shown in Fig. 3.29 for the combination of G0 LVac and Use case 1 LVdc profiles, in Fig. 3.31 for the combination of G0 LVac and Use case 2 LVdc profiles, in Fig. 3.33 for the combination of G0 LVac and Use case 3 LVdc profiles, in Fig. 3.35 for the combination of G6 LVac and Use case 1 LVdc profiles, in Fig. 3.37 for the combination of G6 LVac and Use case 2 LVdc profiles, in Fig. 3.39 for the combination of G6 LVac and Use case 3 LVdc profiles, in Fig. 3.41 for the combination of H0 LVac and Use case 1 LVdc profiles, in Fig. 3.43 for the combination of H0 LVac and Use case 2 LVdc profiles, and in Fig. 3.45 for the combination of H0 LVac and Use case 3 LVdc profiles. The cumulative distributions of the of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\mathrm{DAB,IT,designed}}$ with and without possibility of link ratio reconfiguration are shown in Fig. 3.30 for the combination of G0 LVac and Use case 1 LVdc profiles, in Fig. 3.32 for the combination of G0 LVac and Use case 2 LVdc profiles, in Fig. 3.34 for the combination of G0 LVac and Use case 3 LVdc profiles, in Fig. 3.36 for the combination of G6 LVac and Use case 1 LVdc profiles, in Fig. 3.38 for the combination of G6 LVac and Use case 2 LVdc profiles, in Fig. 3.40 for the combination of G6 LVac and Use case 3 LVdc profiles, in Fig. 3.42 for the combination of H0 LVac and Use case 1 LVdc profiles, in Fig. 3.44 for the combination of H0 LVac and Use case 2 LVdc profiles, and in Fig. 3.46 for the combination of H0 LVac and Use case 3 LVdc profiles.

The required increase of the interconnecting DAB power rating to cover 95 % of the samples from the Monte Carlo-based method is between 10.7 % - Fig. 3.42 (a) - and 26.5 % - Fig. 3.36 (a) - without the possibility of reconfiguration of the link ratio in the application. Implementing the possibility of reconfiguration of the link ratio in the application can reduce the required power rating increase from 19.7 % to 17.5 % for the combination of G0 LVac and Use case 1 LVdc profiles (Fig. 3.30), from 21.7 % to 17.5 % for the combination of G6 LVac and Use case 3 LVdc profiles (Fig. 3.40), from 26.5 % to 18.4 % for the combination of H0 LVac and Use case 2 LVdc profiles (Fig. 3.44), and from 22.0 % to 20.5 % for the combination of H0 LVac and Use case 3 LVdc profiles (Fig. 3.46).

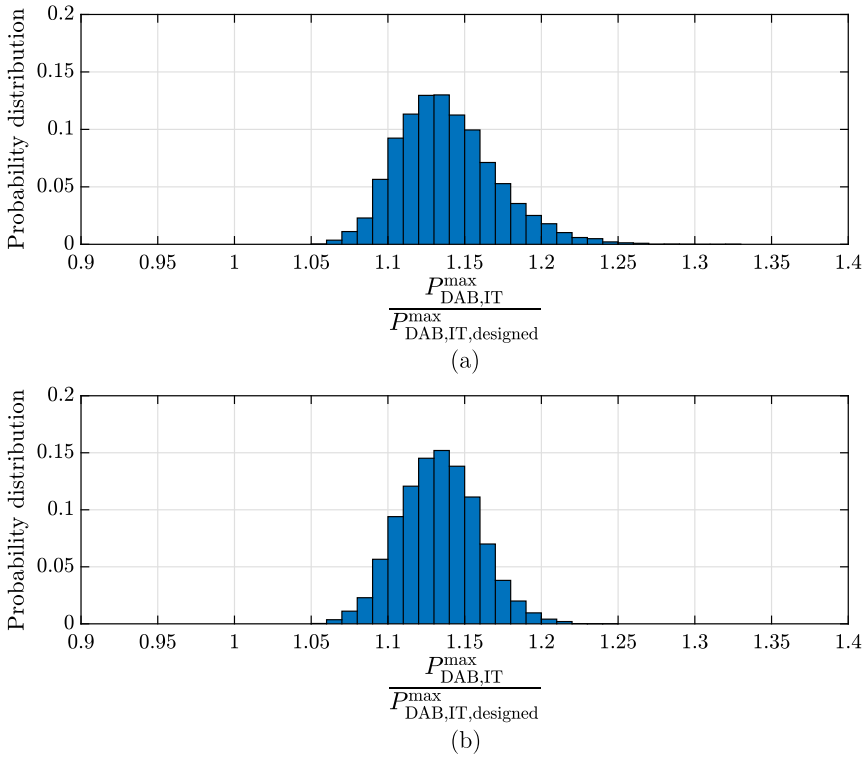


Fig. 3.29: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G0 LVac and Use case 1 LVdc profiles.

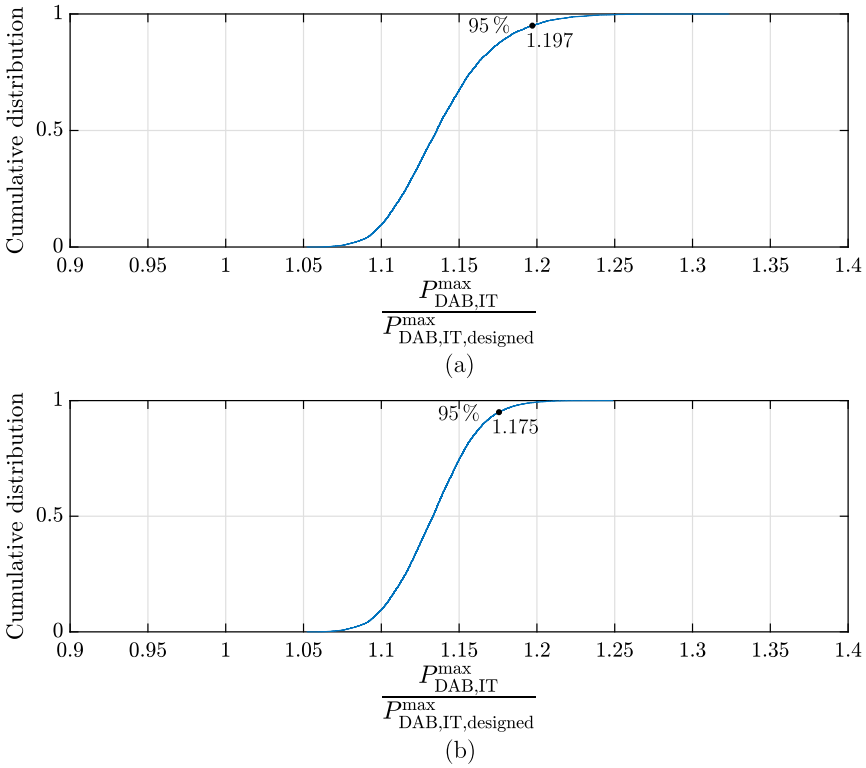


Fig. 3.30: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G0 LVac and Use case 1 LVdc profiles.

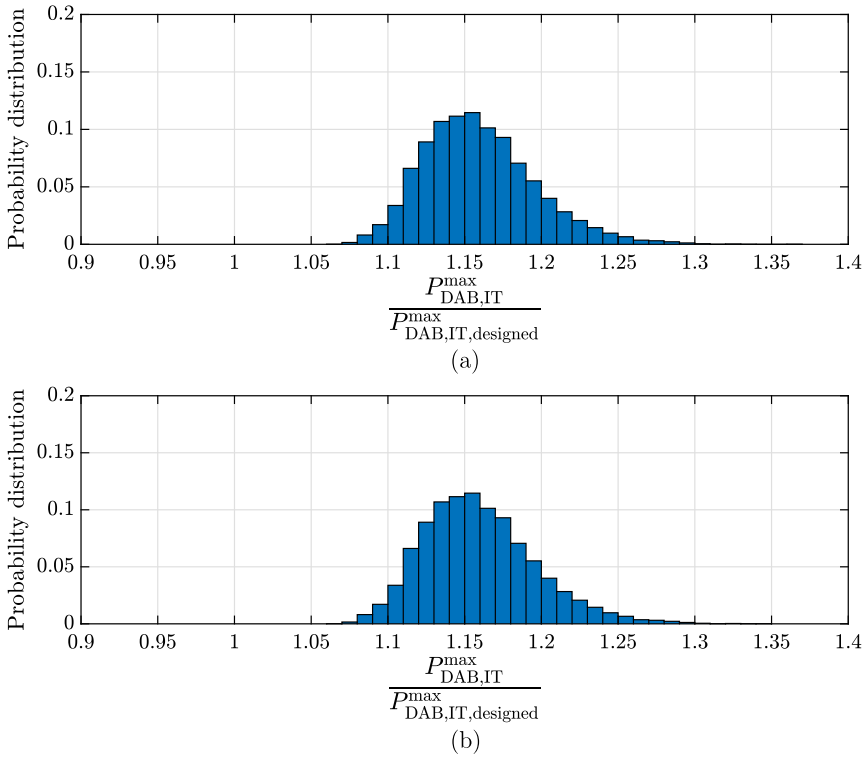


Fig. 3.31: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G0 LVac and Use case 2 LVdc profiles.

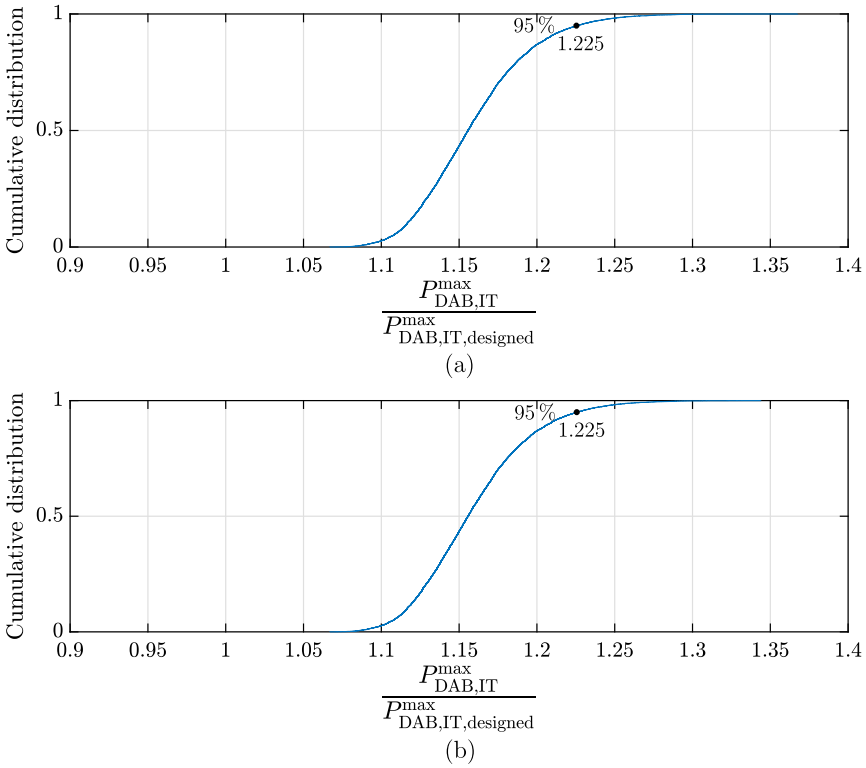


Fig. 3.32: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G0 LVac and Use case 2 LVdc profiles.

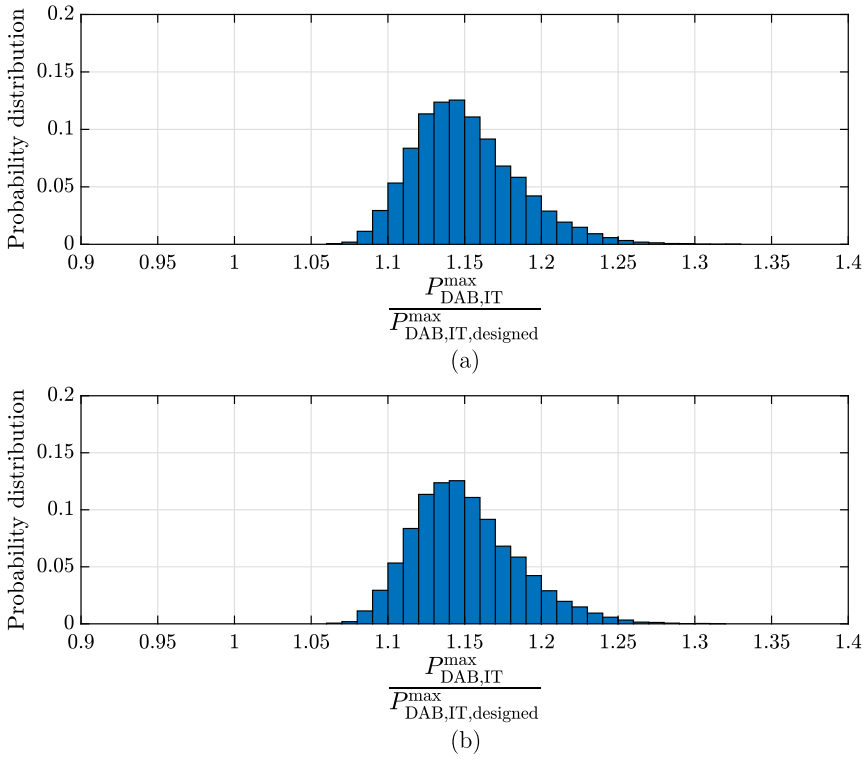


Fig. 3.33: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G0 LVac and Use case 3 LVdc profiles.

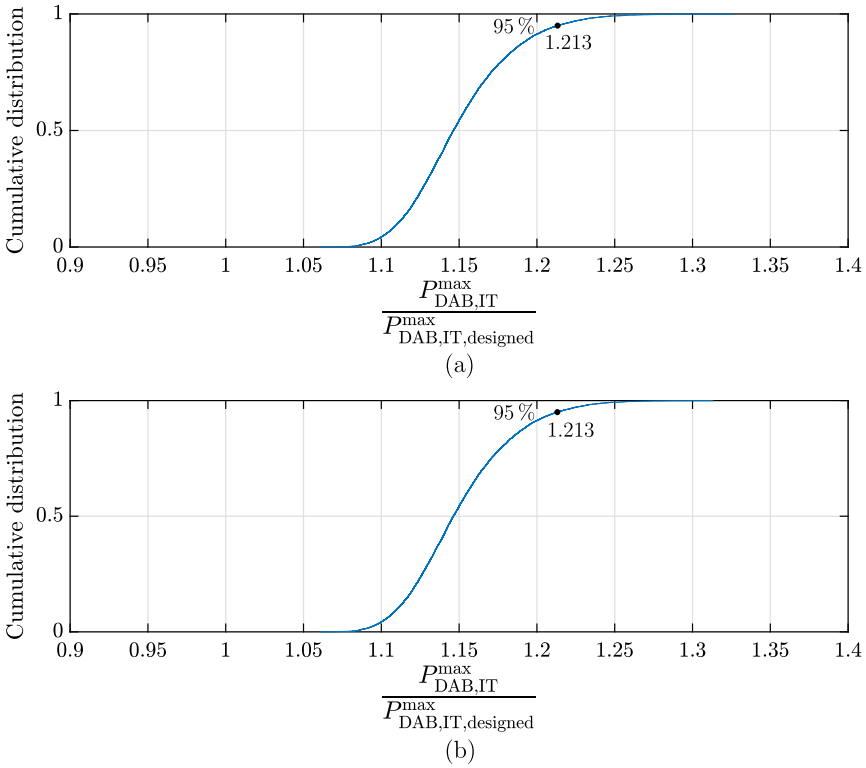


Fig. 3.34: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G0 LVac and Use case 3 LVdc profiles.

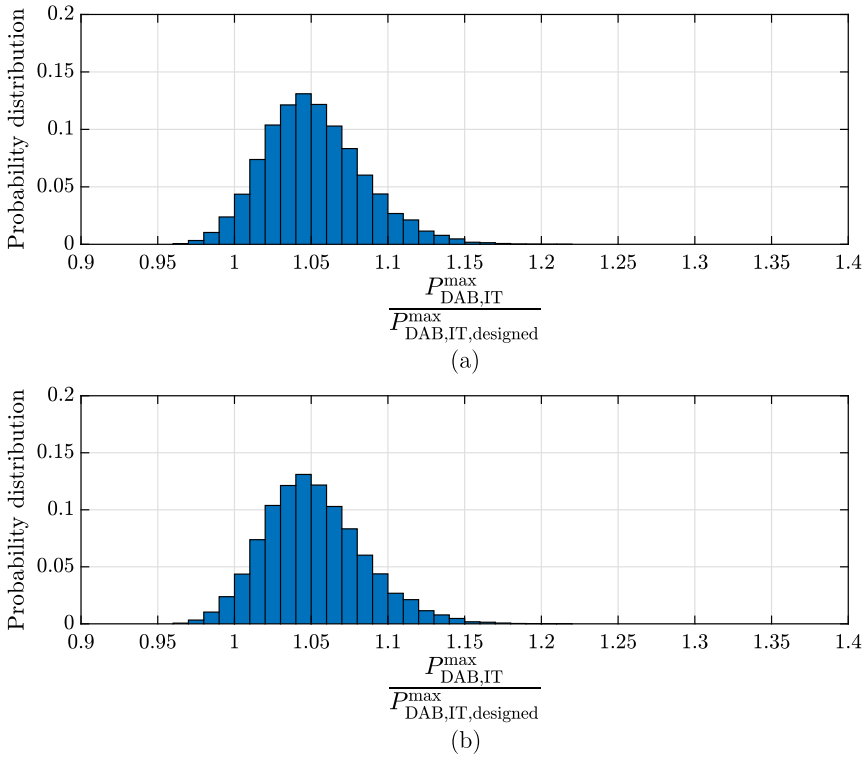


Fig. 3.35: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{DAB,IT,designed}}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G6 LVac and Use case 1 LVdc profiles.

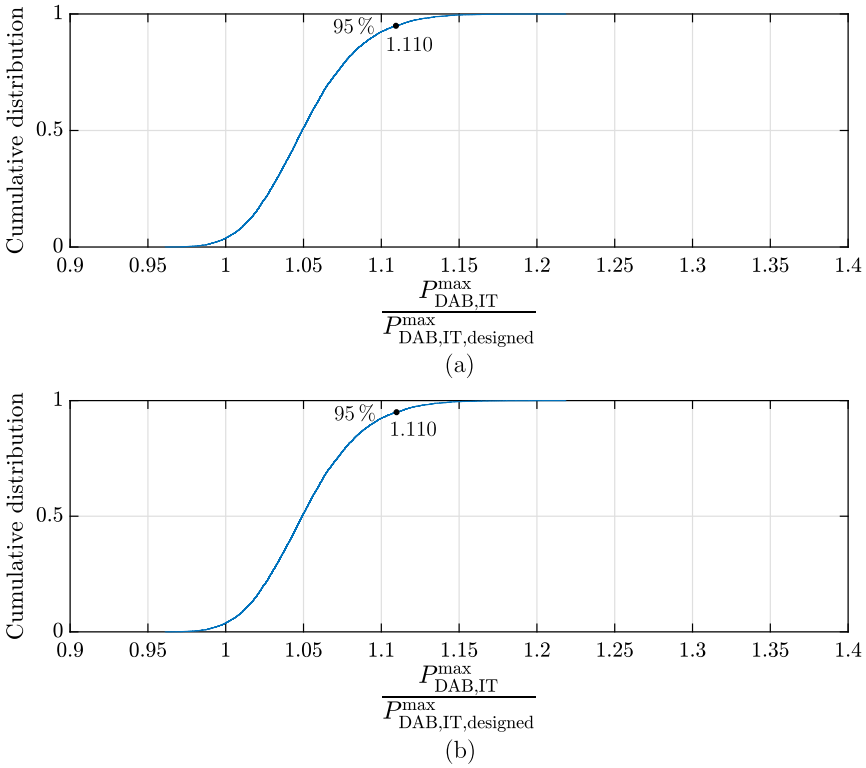


Fig. 3.36: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{DAB,IT,designed}}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G6 LVac and Use case 1 LVdc profiles.

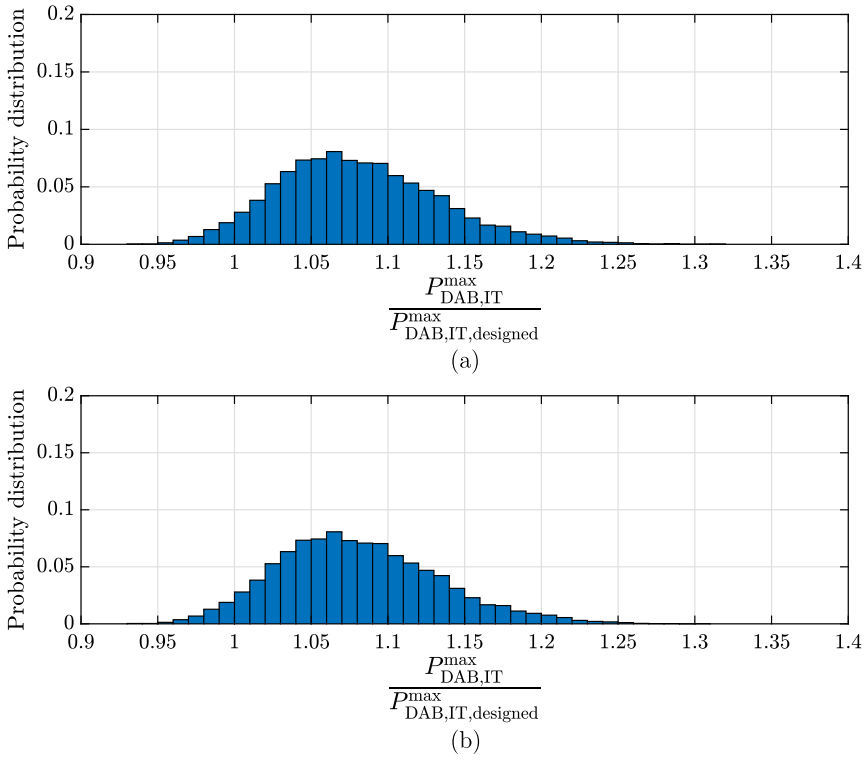


Fig. 3.37: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G6 LVac and Use case 2 LVdc profiles.

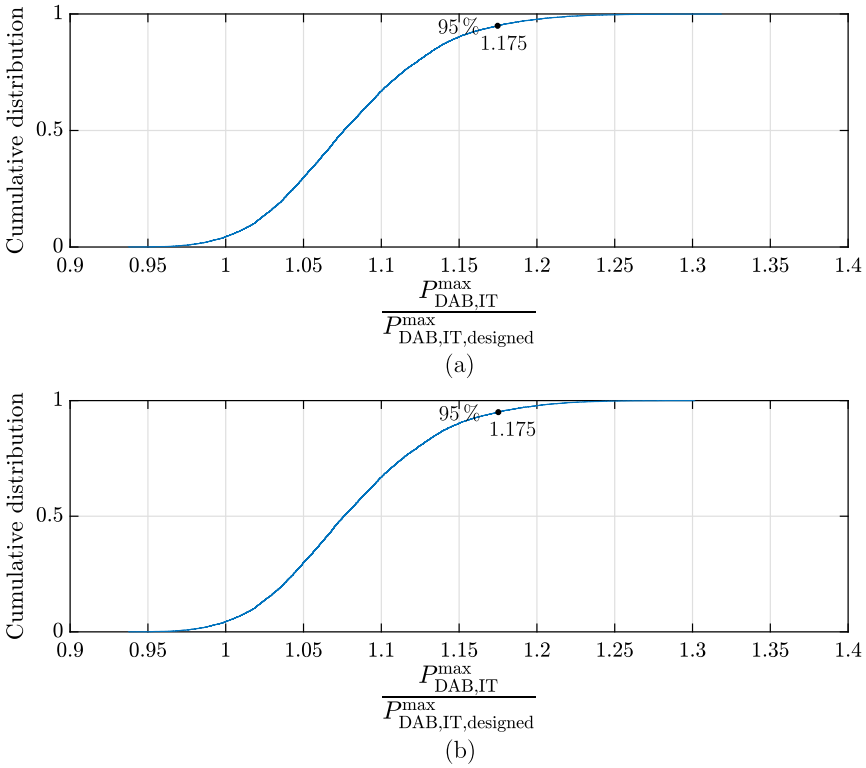


Fig. 3.38: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G6 LVac and Use case 2 LVdc profiles.

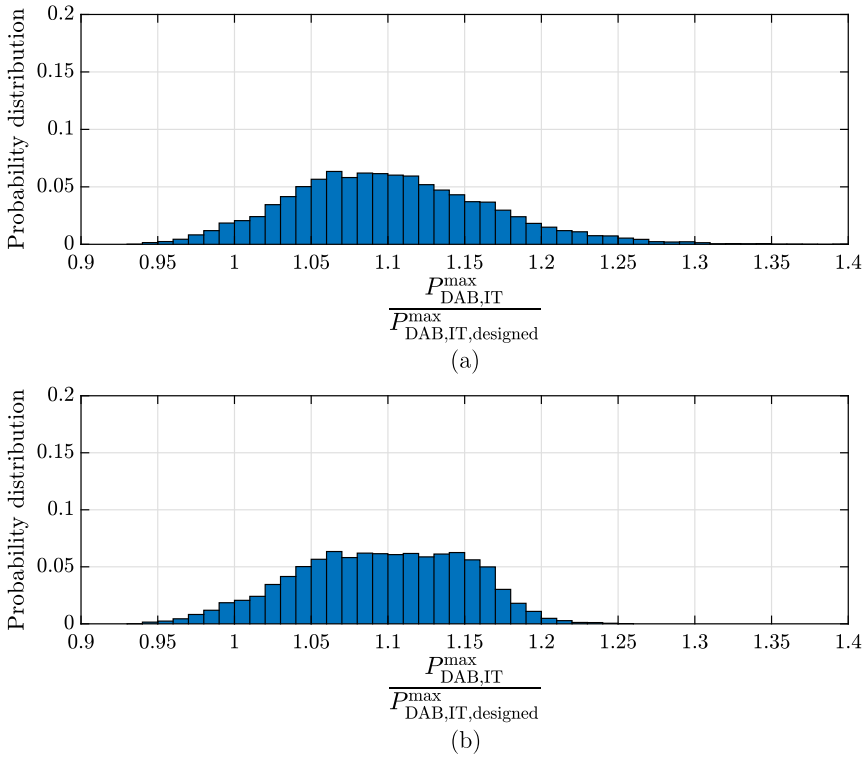


Fig. 3.39: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G6 LVac and Use case 3 LVdc profiles.

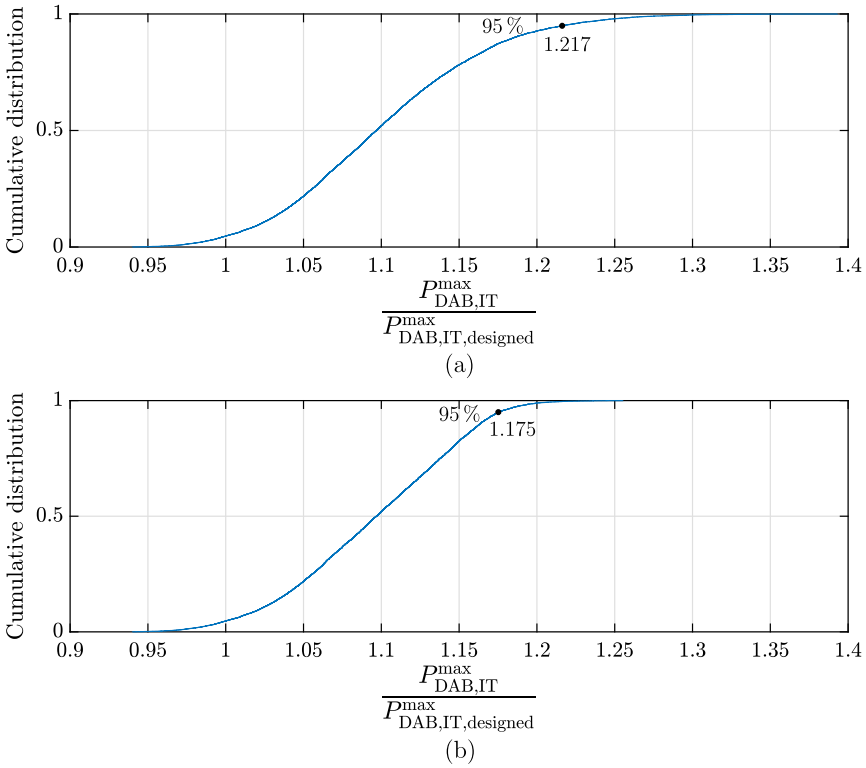


Fig. 3.40: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of G6 LVac and Use case 3 LVdc profiles.

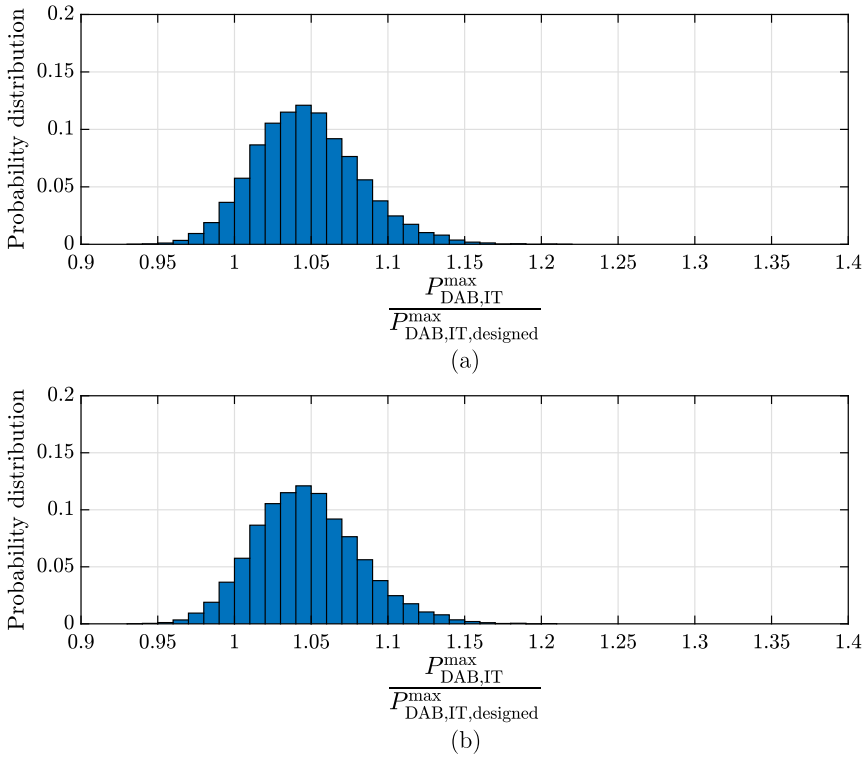


Fig. 3.41: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{DAB,IT,designed}}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of H0 LVac and Use case 1 LVdc profiles.

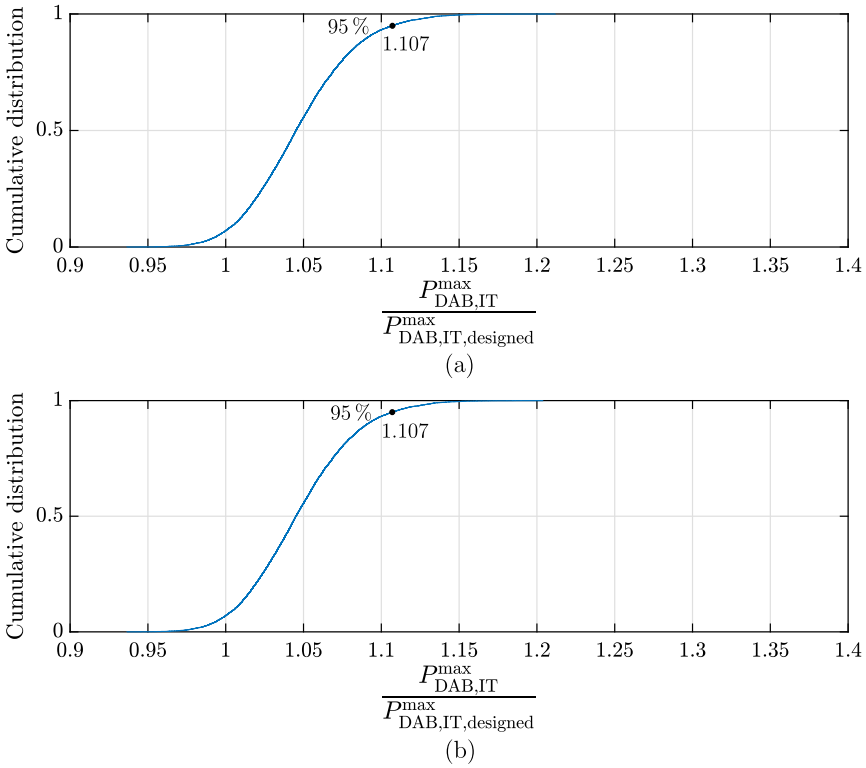


Fig. 3.42: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{DAB,IT,designed}}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of H0 LVac and Use case 1 LVdc profiles.

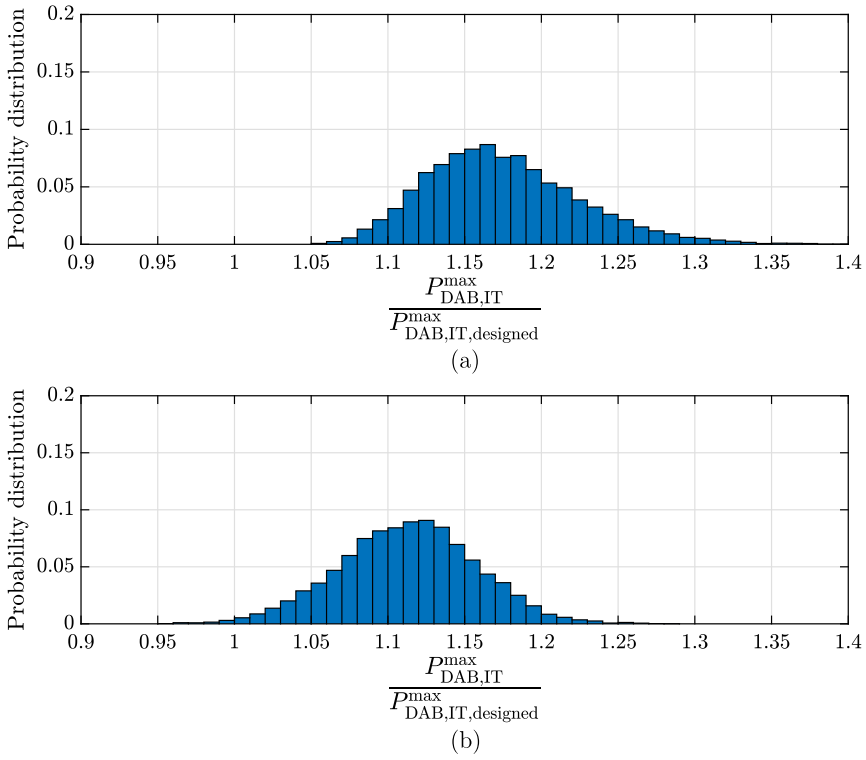


Fig. 3.43: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{DAB,IT,designed}}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of H0 LVac and Use case 2 LVdc profiles.

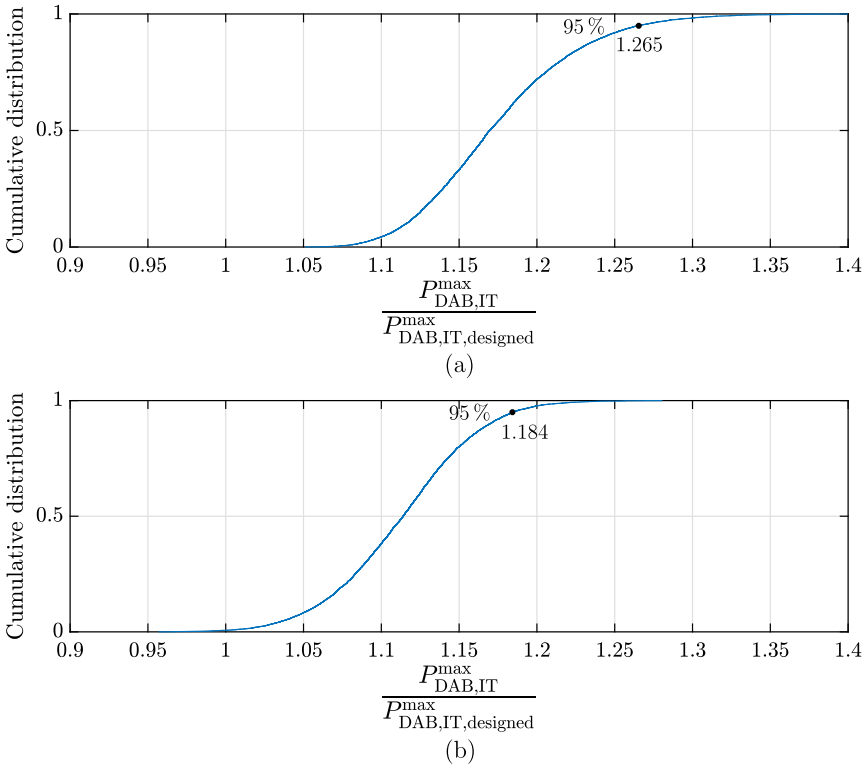


Fig. 3.44: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{\max}_{\text{DAB,IT,designed}}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of H0 LVac and Use case 2 LVdc profiles.

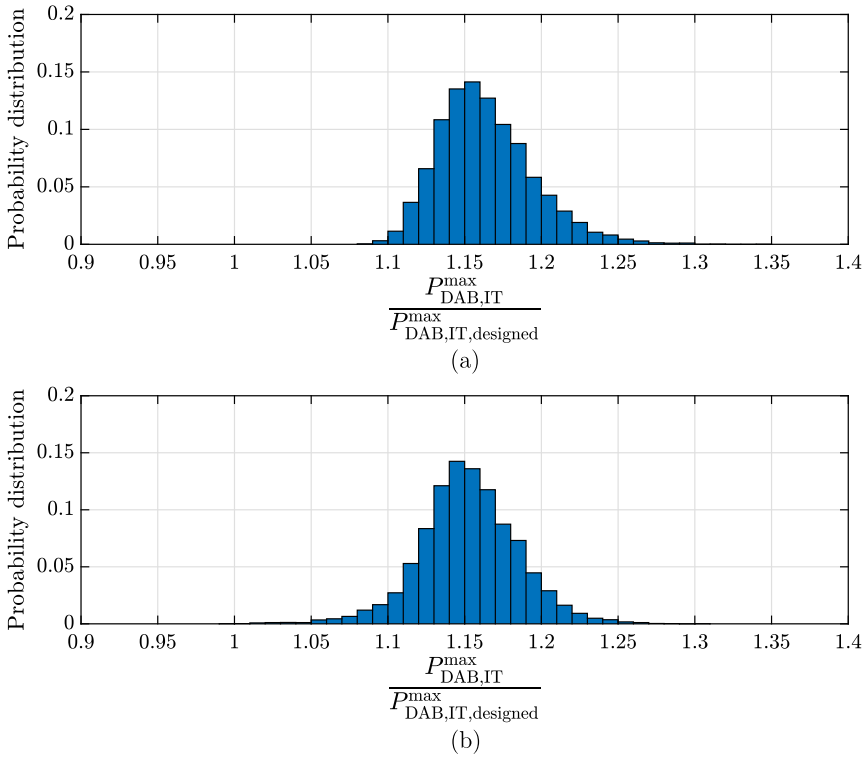


Fig. 3.45: Probability distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of H0 LVac and Use case 3 LVdc profiles.

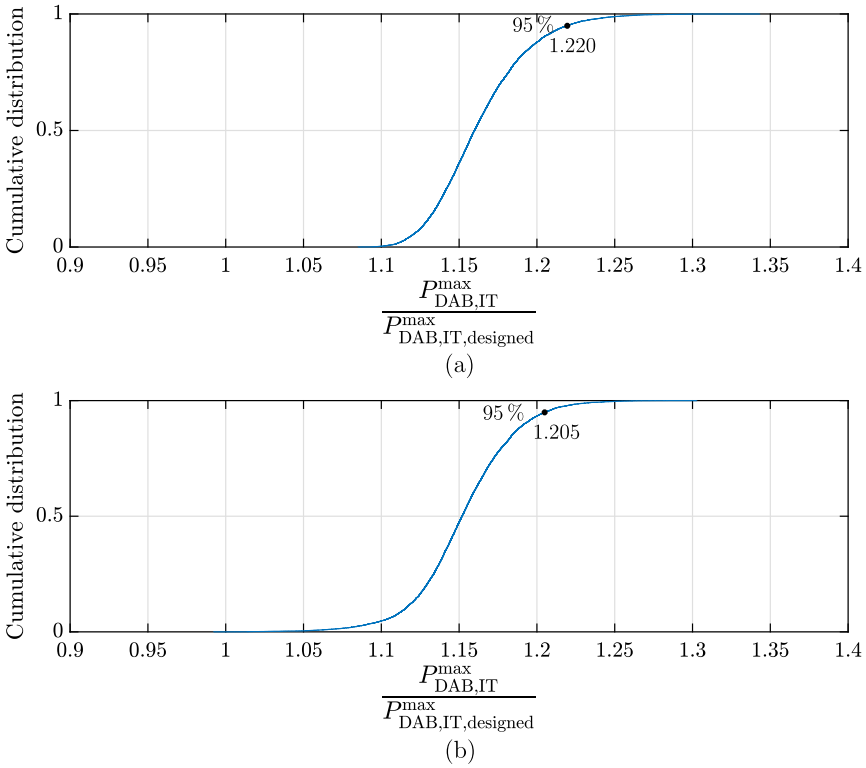


Fig. 3.46: Cumulative distribution of resulting interconnecting DAB power ratings relative to the deviation-less designed rating $P^{max}_{DAB,IT,designed}$ (a) without and (b) with possibility of link ratio reconfiguration in the IT for the combination of H0 LVac and Use case 3 LVdc profiles.

The presented Monte Carlo-based sensitivity analysis of the converter power rating against deviations of the assumed hybrid mission profile reveals that:

- The impact of the uncertain knowledge of the hybrid mission profile has to be considered for the mission profile-based design of the converter power ratings.
- Implementing the possibility of reconfiguration of the link ratio in the application can significantly reduce the impact of the hybrid mission profile uncertainty on the required sizing of the interconnecting DAB for some of the hybrid mission profiles.

3.3. Passive power routing for efficiency by design

This section investigates the impact of the link ratio choice in the IT on the system efficiency. The power flows through the IT can be redirected by adjusting the link ratio configuration. Redirecting the power flows impacts the losses highlighted in Fig. 3.47. The sum of the losses of all MVac PEBBs will change insignificantly by choosing another link ratio, if non-conserved power flows (Section 3.1.3) are considered. Therefore, the main change is the distribution in losses of MVac PEBBs connected to the dc-link $P_{\text{loss,PEBB},1-\xi}$ and those connected to the LVdc feeder $P_{\text{loss,PEBB},\xi}$. However, the losses of the interconnecting DAB $P_{\text{loss,interDAB}}$ change significantly by choosing another link ratio, because the power processed by it depends on ξ (3.17), which was also exploited for the downsizing in Section 3.7. Therefore, the efficiency of a specific operation point $(P_{\text{LVac}}\ P_{\text{LVdc}})$ is optimal for the link ratio which evokes the lowest power flow through the interconnecting DAB.

In this section, the analysis of the efficiency influence of the link ratio choice and the evaluation of the link ratio choice approaches for optimal system efficiency are made considering following assumptions:

- **Assumption 1:** The modeling method with non-conserved power flows described in Section 3.1.3 is used to calculate the efficiencies. The maximum power rating of the

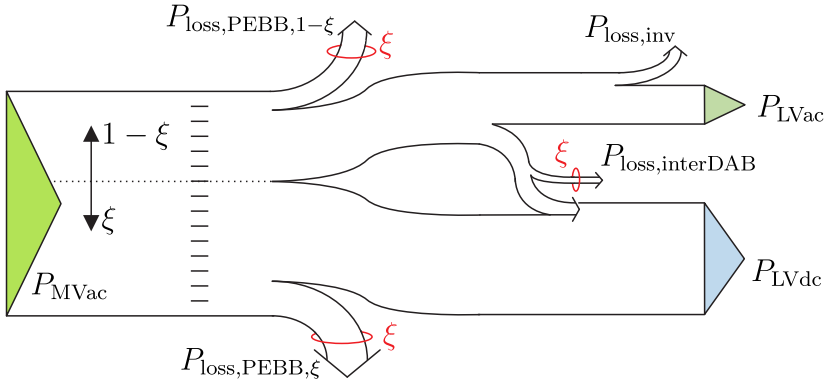


Fig. 3.47: Sankey diagram of the power flows in the IT highlighting which losses are influenced by choosing the link ratio ξ.

Table 3.1: Considered converter power ratings and power semiconductor modules for the efficiency optimization of the IT.

Converter	Power rating	Semiconductor module
CHB cell	20 kW	FP40R12KE3
DAB connected to CHB	20 kW	FP25R12KE3
All MVac PEBBs	900 kW	-
Interconnecting/LVdc DAB	800 kW	FZ800R12KE3
Three phase inverter	800 kW	FF900R12IP4

different converters and the power semiconductor modules considered are listed in Table 3.1. The power rating design is not adjusted to the mission profiles and the downsizing possibility of the interconnecting DAB is omitted in order to evaluate solely the impact of the reconfiguration on the efficiency. 500 kW are considered as 1 p.u. in this section.

- **Assumption 2:** An equal distribution of the MVac active power over all MVac PEBBs is considered. This equal distribution will be ensured via balancing control schemes during normal operation. Advanced control algorithms like active power routing [54] provide the possibility of further efficiency improvements in the IT and will be discussed in Section 5.2.

Afterwards, a laboratory validation of the influence of the link ratio on the efficiency of the IT is shown.

3.3.1. Efficiency influence of link ratio choice

The influence of the reconfiguration of the link ratio in the IT on the system efficiency can be seen in Fig. 3.48 for all considered link ratios of the IT as well as the system efficiency of the NIT. The system efficiency of the NIT (Fig. 3.48 (a)) has two peaks, one in quadrant two ($P_{\mathrm{LVac}} < 0$ and $P_{\mathrm{LVdc}} > 0$) and the other in quadrant four ($P_{\mathrm{LVac}} > 0$ and $P_{\mathrm{LVdc}} < 0$). These peaks are near the operation points where the power generation in one LV grid is equal to the power consumption in the other LV grid. In this case the power only flows through the three phase inverter and the LVdc DAB. However, the shape of the efficiency peaks is shifted towards lower values of LVdc generation or consumption, because the LVdc DAB is less efficient than the three phase LVac inverter.

The efficiencies of the IT configurations have additional peaks in quadrant one ($P_{\mathrm{LVac}} > 0$ and $P_{\mathrm{LVdc}} > 0$) and three ($P_{\mathrm{LVac}} < 0$ and $P_{\mathrm{LVdc}} < 0$) compared to the NIT. These efficiency peaks are located around the lines of operation points with unloaded interconnecting DAB,

which is approximately the case when the relation of the LV powers is

$$\frac{P_{\mathrm{LVac}}}{P_{\mathrm{LVdc}}} = \frac{N_{\mathrm{MB,LVac}}}{N_{\mathrm{MB,LVdc}}} = \frac{1-\xi}{\xi} \quad . \tag{3.25}$$

The operation points where the interconnecting DAB power is exactly zero have higher P_{LVdc} compared to (3.25) due to the three phase LVac inverter and the consideration of non-conserved power flows (assumption 1 made for this section). By selecting the link ratio, the location of the efficiency peaks in quadrant one and three can be determined. However, the location of the efficiency peaks in quadrant two and four are also influenced by changing the link ratio. The higher the selected link ratio, the more these efficiency peaks are shifted towards operation points with higher $|P_{\mathrm{LVdc}}|$ than $|P_{\mathrm{LVac}}|$.

Each operation point has a specific link ratio, which provides maximum efficiency. The operation areas in which the different link ratios provide maximum efficiency for the operation points are presented in Fig. 3.49. In quadrants one and three these operation areas are located around the operation points with unloaded interconnecting DAB of the specific link ratios. Whereas in quadrants two and four, the highest considered link ratio $\xi = \frac{14}{15}$ or the NIT are optimal. Therefore, the potential for optimization of the system efficiency is limited in quadrants two and four. Furthermore, reverse power flow from the LV grids to the MVac grid should be limited [60], which is the case in quadrant three. Due to these reasons the following system efficiency optimization via the link ratio choice is investigated for quadrant one, where both LV grids consume power.

The efficiency areas in the P_{LVac}-P_{LVdc} plane can be reduced to two dimensions by describing only the operation points with a cumulative output power of 1 p.u., which are highlighted in Fig. 3.49. Hereby, comparing the efficiencies of the different link ratios is facilitated, as shown in Fig. 3.50. The efficiency curve of each link ratio has a peak at approximately the ratio of LV powers given in (3.25). At this efficiency peak and around it the specific link ratio is the optimal choice. As P_{LVac} increases and P_{LVdc} decreases, the efficiency peaks of the optimal link ratios reduce. This is due to the losses of the three phase LVac inverter that increase with P_{LVac}.

3.3.2. Link ratio choice approaches for optimal system efficiency

The significant efficiency influence of the link ratio selection in the IT combined with the resulting optimal operation areas for the different link ratios (Fig. 3.49) provide the possibility of optimizing the system efficiency for considered hybrid mission profiles. For this purpose, two approaches to select the optimal link ratio for maximum efficiency are proposed, which are tested on the hybrid mission profiles presented in Fig. 3.7.

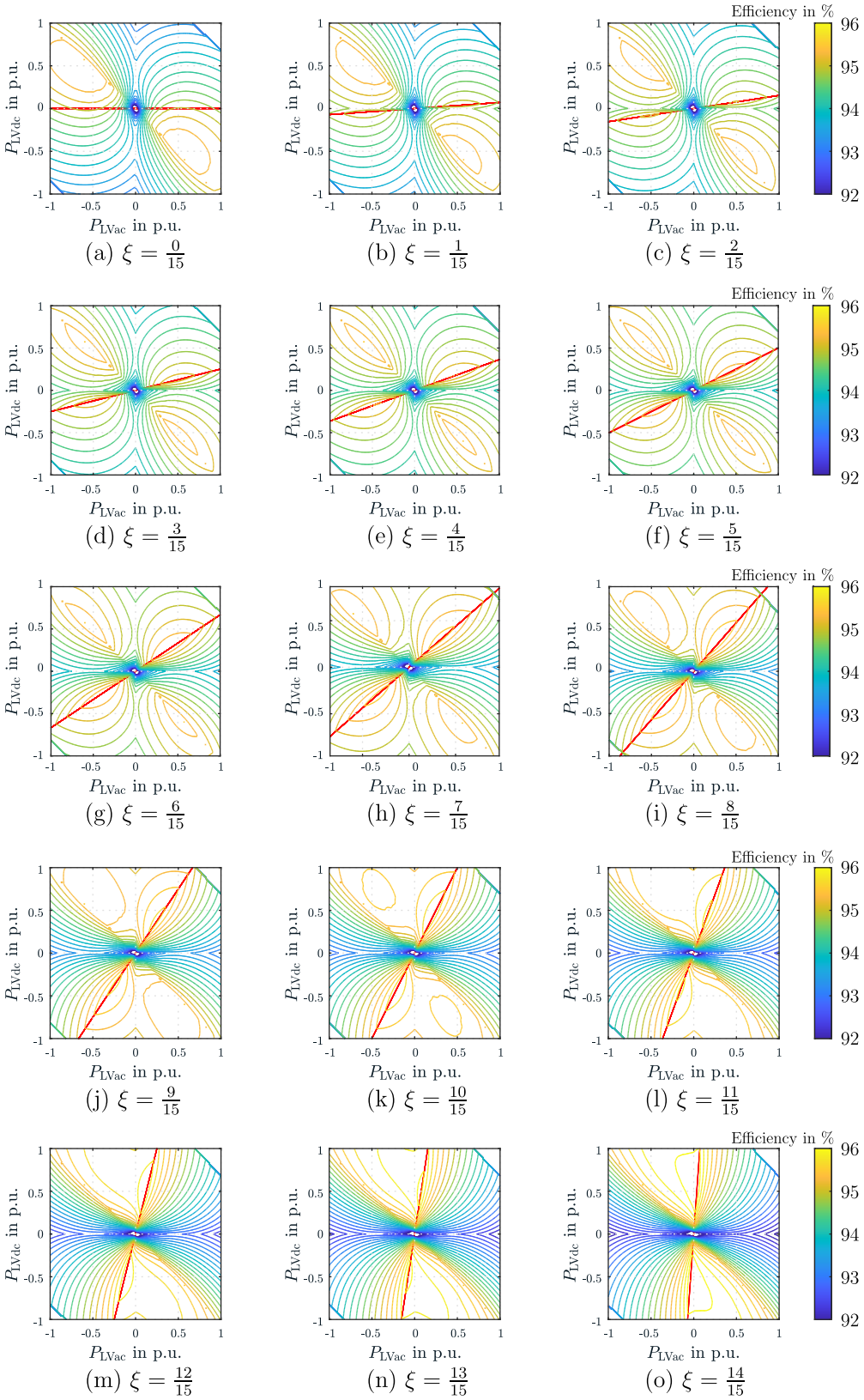


Fig. 3.48: Efficiency of (a) the NIT and the IT with different configurations (a) $\xi = \frac{1}{15}$, (b) $\xi = \frac{2}{15}$, (c) $\xi = \frac{3}{15}$, (d) $\xi = \frac{4}{15}$, (e) $\xi = \frac{5}{15}$, (f) $\xi = \frac{6}{15}$, (g) $\xi = \frac{7}{15}$, (h) $\xi = \frac{8}{15}$, (i) $\xi = \frac{9}{15}$, (j) $\xi = \frac{10}{15}$, (k) $\xi = \frac{11}{15}$, (l) $\xi = \frac{12}{15}$, (m) $\xi = \frac{13}{15}$, and (n) $\xi = \frac{14}{15}$, the operation points with approximately unloaded interconnecting/LVdc DAB are highlighted as red lines.

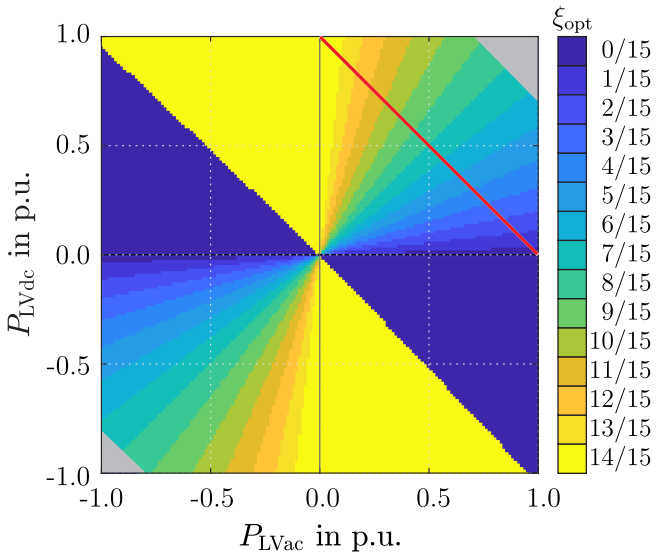


Fig. 3.49: Operation areas of optimal link ratios ξ_{opt} for maximum system efficiency and a red line highlighting the operation points with 1 p.u. cumulative output power.

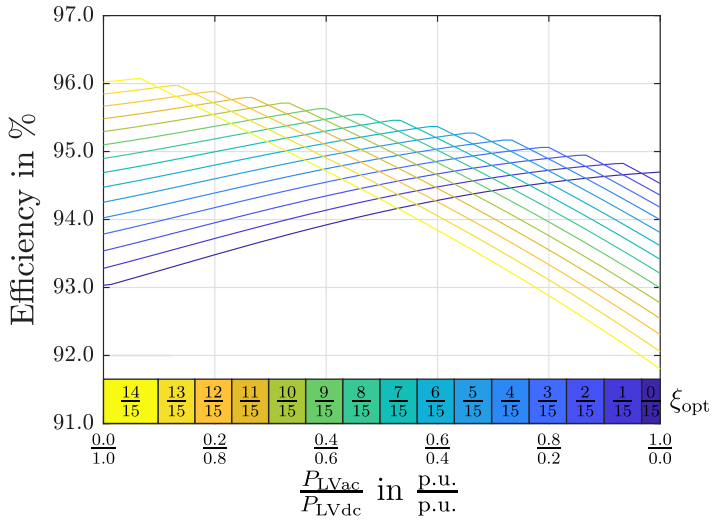


Fig. 3.50: Efficiencies of the different link ratios on operation points with 1 p.u. cumulative output power.

The first approach is based on the Average Weighted system Efficiency (AWE), which considers the efficiency $\eta_{sys}(\xi, P_{LVac}, P_{LVdc})$ at each operation point $(P_{LVac}\ P_{LVdc}) \in M$ for the considered hybrid mission profile and weights it with the total output power at this operation point

$$\bar{\eta}_{sys}(\xi) = \frac{\sum\limits_{(P_{LVac}\ P_{LVdc})\in M} P_{LVdc} + P_{LVac}}{\sum\limits_{(P_{LVac}\ P_{LVdc})\in M} \frac{P_{LVdc}+P_{LVac}}{\eta_{sys}(\xi, P_{LVac}, P_{LVdc})}} . \tag{3.26}$$

The calculation of (3.26) is executed for all considered link ratios and the link ratio with the highest AWE is chosen, exemplarily shown for the combination of G0 LVac and Use case 2 LVdc power profiles in Fig. 3.51 (a). This requires the efficiency curve modeling of all converters and the execution of the non-conserved power flow analysis described in Section 3.1.3 for each operation point and link ratio. The AWE approach requires significant modeling and

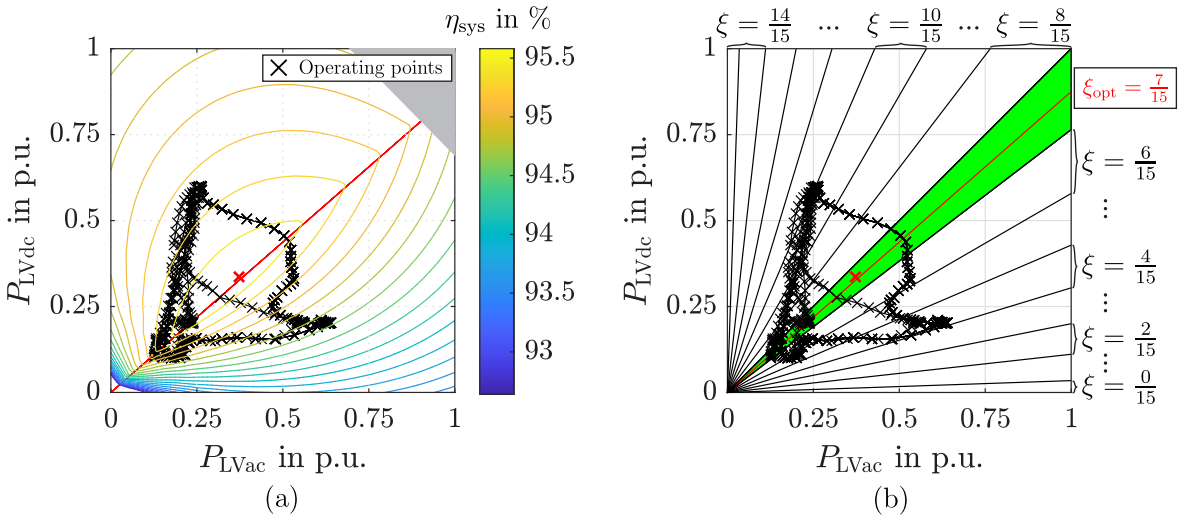


Fig. 3.51: Determination of the link ratio for optimal efficiency via (a) Average Weighted system Efficiency (AWE) approach and (b) Center of Mission profile (CoM) approach for the combination of G0 LVac and Use case 2 LVdc power profiles, CoM marked as red cross and unloaded interconnecting DAB operation as red line.

calculation effort, but always provides the link ratio which enables the minimum losses over all operation points of the hybrid mission profile according to the considered modeling.

The second approach is based on the Center of the Mission profile (CoM), which can be calculated by weighting each operation point with its total output power

$$\begin{bmatrix} P_{\mathrm{LVac,CoM}} \\ P_{\mathrm{LVdc,CoM}} \end{bmatrix} = \frac{\sum\limits_{(P_{\mathrm{LVac}}\, P_{\mathrm{LVdc}})\in M} (P_{\mathrm{LVdc}} + P_{\mathrm{LVac}}) \begin{bmatrix} P_{\mathrm{LVac}} \\ P_{\mathrm{LVdc}} \end{bmatrix}}{\sum\limits_{(P_{\mathrm{LVac}}\, P_{\mathrm{LVdc}})\in M} P_{\mathrm{LVdc}} + P_{\mathrm{LVac}}} \,. \tag{3.27}$$

Afterwards, the link ratio whose optimal operation area is covering the location of the CoM is chosen, exemplarily shown for the combination of G0 LVac and Use case 2 LVdc power profiles in Fig. 3.51 (b). The optimal operation areas shown in Fig. 3.49 can be approximated via assigning equally distributed angular sectors around the lines of unloaded interconnecting DAB operation according to (3.25) for each link ratio. The CoM approach requires only the knowledge of the hybrid mission profile, no modeling of the converter efficiencies is necessary. However, the link ratio chosen by the CoM approach can differ from the optimal link ratio found by the AWE approach, therefore, the efficiency optimization potential of the IT might be not fully exploited.

The resulting link ratios for both approaches as well as the average weighted system efficiencies, according to (3.26), realized via these link ratios are presented in Table 3.2. The CoM approach indicates the same link ratios as the AWE approach for most of the hybrid mission profiles. Only for the combinations of G0 LVac with Use case 3 LVdc and H0 LVac with Use case 1 LVdc power profiles, the resulting link ratios of the two approaches differ. However, the link ratios identified by the CoM approach ξ_{CoM} are directly next to those identified by

Table 3.3: Comparison of average weighted system efficiencies of the IT (link ratio design via AWE approach) and of the NIT ($\xi = 0$) for all combinations of LVac and LVdc power profiles.

$\bar{\eta}_{sys}(\xi_{AWE})$		LVac		
$\bar{\eta}_{sys}(\xi = 0)$		G0	G6	H0
LVdc	Use case 1	94.95 %	95.17 %	95.09 %
		94.14 %	94.00 %	94.11 %
	Use case 2	95.13 %	95.34 %	95.25 %
		94.24 %	94.13 %	94.24 %
	Use case 3	95.32 %	95.43 %	95.42 %
		94.12 %	94.05 %	94.13 %

the AWE approach ξ_{AWE}. Therefore, the differences in the average weighted system efficiency are only 0.0083 Δ% (G0 LVac with Use case 3 LVdc power profiles) and 0.0165 Δ% (H0 LVac with Use case 1 LVdc power profiles).

The comparison of the average weighted system efficiencies achieved with the link ratio design via the AWE approach for the IT with those of the NIT ($\xi = 0$) is given in Table 3.3. The improvement of the average weighted system efficiency by using the optimal configuration of the IT instead of the NIT is between 0.81 Δ% (G0 LVac and Use case 1 LVdc power profiles) and 1.37 Δ% (G6 LVac and Use case 3 LVdc power profiles). This results in a reduction of the total system losses between 13.84 % and 23.10 %. The average efficiency improvement is 1.1 Δ% and the average reduction of losses is 18.77 % among all considered hybrid mission profiles.

3.3.3. Laboratory validation of link ratio efficiency influence

The influence of the link ratio selection on the system efficiency is validated on a small scale laboratory prototype (Fig. 3.52), which contains three DABs and the equipment listed in Table 3.4. One DAB acts as the interconnecting converter of the IT and the other two

Table 3.2: Resulting link ratios and average weighted system efficiencies for (a) the AWE approach and (b) the CoM approach for all combinations of LVac and LVdc power profiles, deviations of the CoM approach from the AWE approach results are highlighted.

(a)

ξ_{AWE}		LVac		
$\bar{\eta}_{sys}(\xi_{AWE})$		G0	G6	H0
LVdc	Use case 1	8/15	9/15	9/15
		94.95 %	95.17 %	95.09 %
	Use case 2	7/15	8/15	7/15
		95.13 %	95.34 %	95.25 %
	Use case 3	9/15	9/15	8/15
		95.32 %	95.43 %	95.42 %

(b)

ξ_{CoM}		LVac		
$\bar{\eta}_{sys}(\xi_{CoM})$		G0	G6	H0
LVdc	Use case 1	8/15	9/15	8/15
		94.95 %	95.17 %	95.07 %
	Use case 2	7/15	8/15	7/15
		95.13 %	95.34 %	95.25 %
	Use case 3	8/15	9/15	8/15
		95.31 %	95.43 %	95.42 %

represent the DABs of two MVac PEBBs. The scheme of the DAB laboratory setup in Fig. 3.53 shows how the DABs, loads, and sources are connected. The CHB and the three phase LVac inverter are not included in the laboratory setup, because their impact on the system efficiency is irrelevant for the conducted validation. The interconnecting DAB losses and the link ratio configuration are the main contributors for the changing system efficiency. The dc voltage sources provide the input voltages of the MVac PEBBs V_{s1} and V_{s2}, while the current sources are used to emulate a higher number of MVac PEBBs. The power analyzers measure the load powers, input and output powers of DAB 1 and 2 as well as the powers provided by the current sources. The values of the voltages, capacitors and DAB related

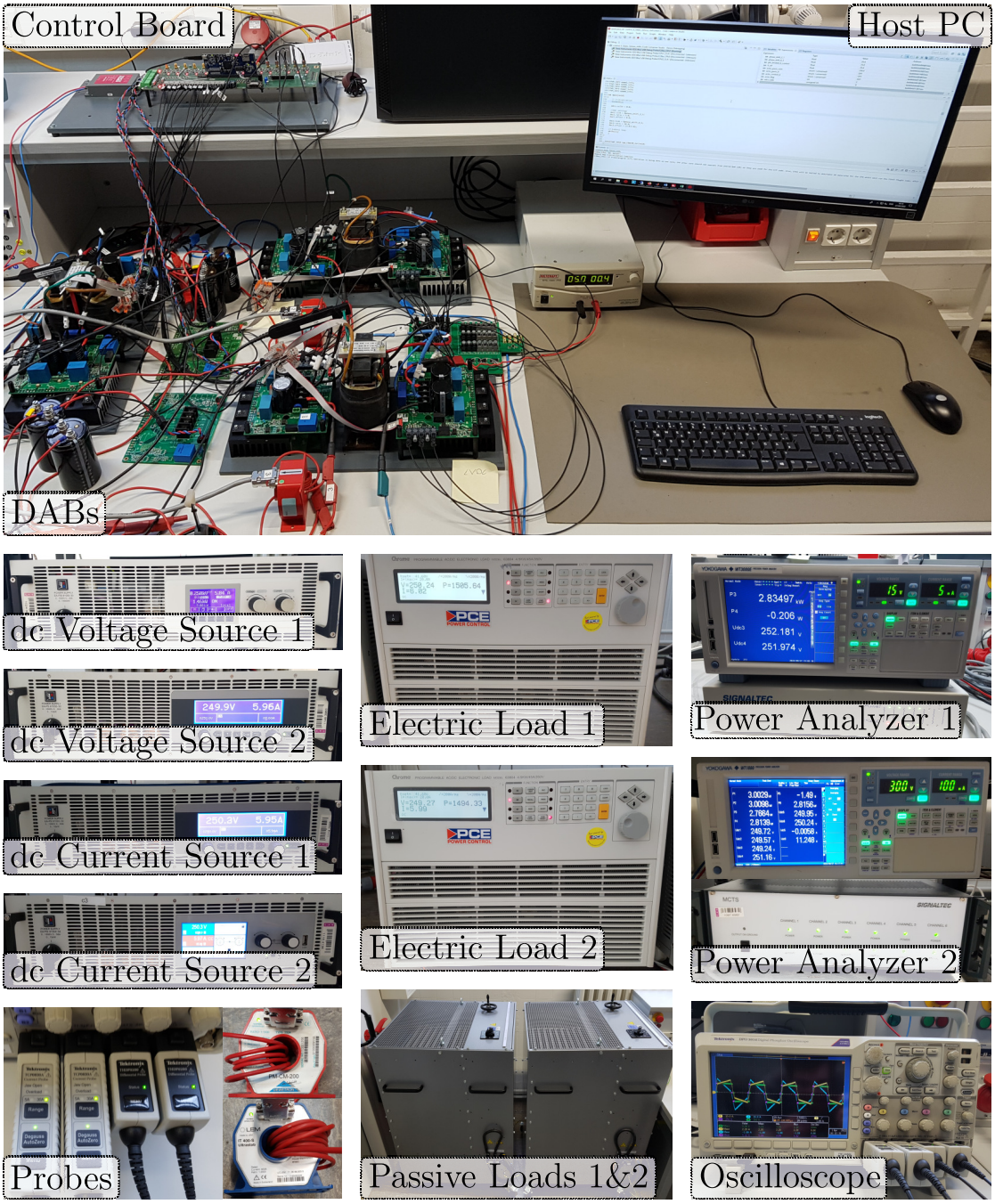


Fig. 3.52: Dual active bridge laboratory setup and equipment.

Table 3.4: Equipment used for the DAB laboratory setup.

Equipment	Manufacturer	Model
dc voltage source 1	Elektro Automatik	EA-PSI 81000-30
dc voltage source 2	Elektro Automatik	EA-PS 91000-30
dc current source 1	Elektro Automatik	EA-PS 91000-30
dc current source 2	Elektro Automatik	EA-PSI 91500-30
Digital signal processor	Texas Instruments	TMS320F28379D
Passive loads 1&2	Frizlen	BW83
Electric loads 1&2	Chroma	63804
Oscilloscope	Tektronix	DPO 3014
Current probes	Tektronix	TCP0030A
Voltage probes	Tektronix	THDP0200
Power analyzer 1	Yokogawa	WT3000E
Power analyzer 2	Yokogawa	WT1800
Signal conditioners 1&2 (current signals power analyzers)	Signaltec	MCTS
Current sensors (power analyzer 1)	LEM	IT 400-S Ultrastab
Current sensors (power analyzer 2)	Dewetron	PM-CM-200

parameters used in the setup are listed in Table 3.5.

The control scheme used for the DAB laboratory setup is presented in Fig. 3.54. DAB 1 and 2 are controlled via a combined voltage control, which gives the phase shift φ, derived by a PI controller, to both DABs in order to provide the sum of the reference voltages ($V^*_{\mathrm{dc-link}} + V^*_{\mathrm{LVdc}}$) at dc-link and LVdc feeder. The interconnecting DAB is controlled via a balancing control, which provides the phase shift φ_{i}, derived by a PI controller, in order to keep the

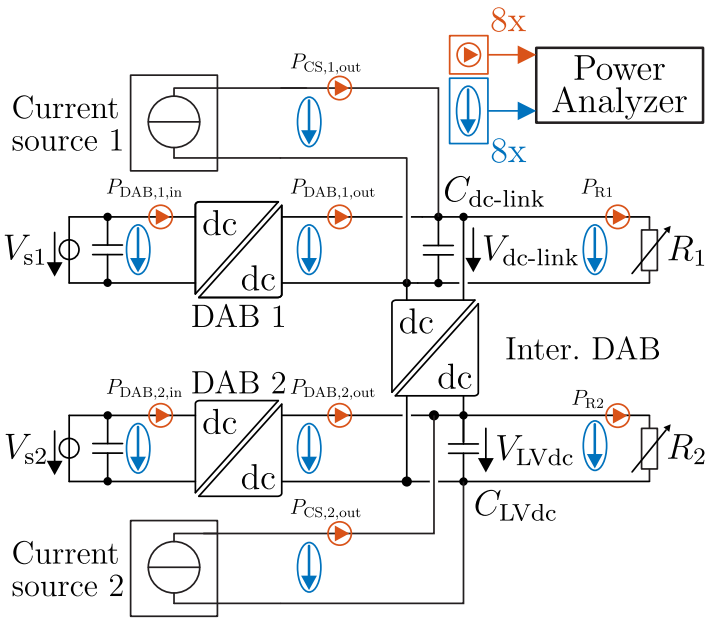


Fig. 3.53: Scheme of the dual active bridge laboratory setup.

Table 3.5: Experimental setup parameters of the DAB laboratory setup.

Symbol	Representation	Value
V_{s1}, V_{s2}	MVac PEBB cell voltages	250 V
$V_{dc-link}$ / V_{LVdc}	LV dc-link / LVdc grid voltage	250 V
$C_{dc-link}$ / C_{LVdc}	dc-link / LVdc grid capacitor	4.5 mF
L_{DAB}	DAB inductances	65 µH
n	Transformer turn ratio DABs	1
$f_{sw,DAB}$	DAB switching frequency	20 kHz

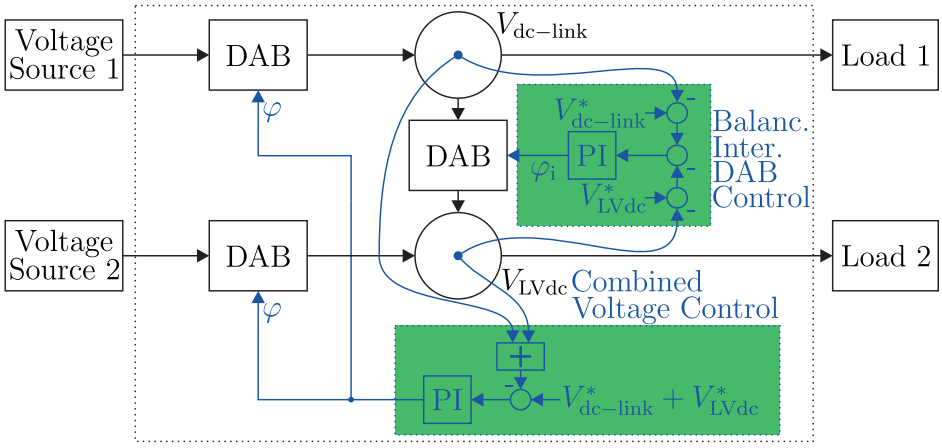


Fig. 3.54: Control scheme for the dual active bridge laboratory setup.

errors of the dc-link and LVdc voltage compared to the reference values balanced.

The link ratio configurations that are realized by the emulation of additional MVac PEBB DABs via the utilization of current sources are listed in Table 3.6. The emulation of additional MVac PEBB DABs is done by adjusting the dc currents of the current sources so that the current source output powers $P_{CS,1,out}$ or $P_{CS,2,out}$ are equal to multiples of the DAB output powers $P_{DAB,1,out}$ or $P_{DAB,2,out}$, depending on link ratio configuration to be realized. The virtual input power of the emulated MVac PEBB DABs are calculated based on the efficiency of the DAB, which is replicated by the current source, with

$$P_{CS,1,in} = P_{CS,1,out}\frac{P_{DAB,1,in}}{P_{DAB,1,out}} = \frac{P_{CS,1,out}}{\eta_{DAB,1}} \tag{3.28}$$

Table 3.6: Small scale prototype configurations via emulation of additional MVac PEBB DABs with current sources.

ξ	N_{MB}	$N^{DAB}_{MB,dc-link}$	$N^{CS}_{MB,dc-link}$	$N^{DAB}_{MB,LVdc}$	$N^{CS}_{MB,LVdc}$
1/4	4	1	2	1	0
2/4	4	1	1	1	1
3/4	4	1	0	1	2

and

$$P_{\mathrm{CS,2,in}} = P_{\mathrm{CS,2,out}} \frac{P_{\mathrm{DAB,2,in}}}{P_{\mathrm{DAB,2,out}}} = \frac{P_{\mathrm{CS,2,out}}}{\eta_{\mathrm{DAB,2}}} \,. \tag{3.29}$$

The efficiency of the DAB laboratory setup including the emulated DABs is calculated by dividing the output powers on the loads P_{R1} and P_{R2} by all input powers

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{P_{\mathrm{R1}} + P_{\mathrm{R2}}}{P_{\mathrm{CS,1,in}} + P_{\mathrm{DAB,1,in}} + P_{\mathrm{DAB,2,in}} + P_{\mathrm{CS,2,in}}} \,. \tag{3.30}$$

The waveforms of one DAB are shown in Fig. 3.55 as an example. The measurements of the power analyzers are taken in steady state operation for different load combinations. The sum of both output powers $P_{\mathrm{R1}} + P_{\mathrm{R2}}$ is kept at 6 kW to have the same degree of system utilization for better comparability. The measured efficiencies for the different link ratio configurations are presented in Fig. 3.56 as solid lines with the points of measurements marked by crosses. Comparing the operation areas where the different configurations provide maximum efficiency for the measured values with these areas calculated analytically reveals an asymmetric behavior of the DAB laboratory setup efficiency. The reason for this asymmetric behavior can be the difference in the efficiencies of DAB 1 and DAB 2, shown in Fig. 3.57. This difference is mainly caused by the manufacturing tolerances of the medium frequency transformers used in the DABs.

A compensation of the efficiency difference of DAB 1 and DAB 2 is used to validate that it is the reason for the asymmetric behavior of the DAB laboratory setup efficiency. The compensation is done by using the efficiency of DAB 2 to calculate all input powers virtually

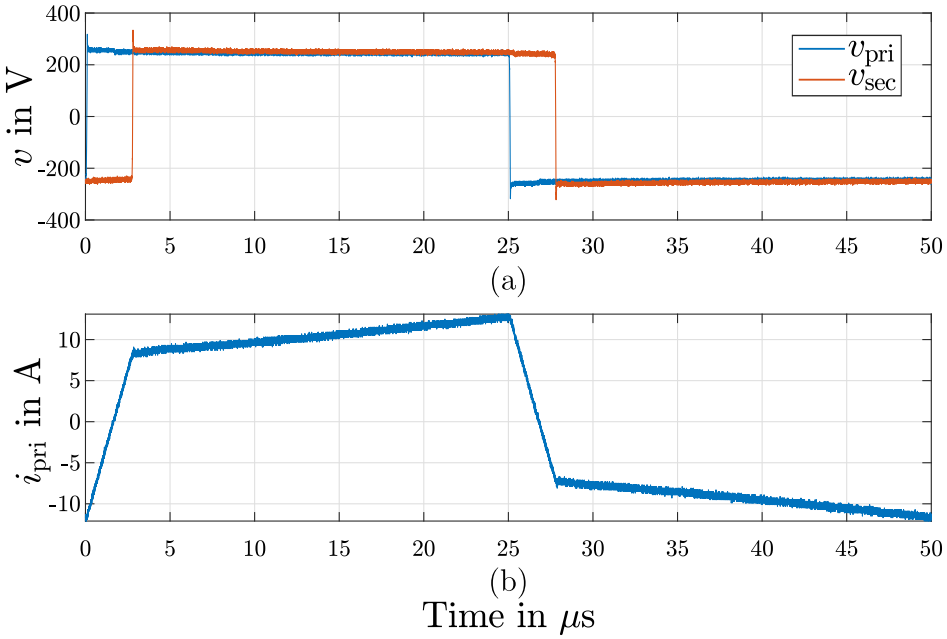


Fig. 3.55: Dual active bridge (a) primary and secondary voltage and (b) primary inductor current for operation at 2 kW output power.

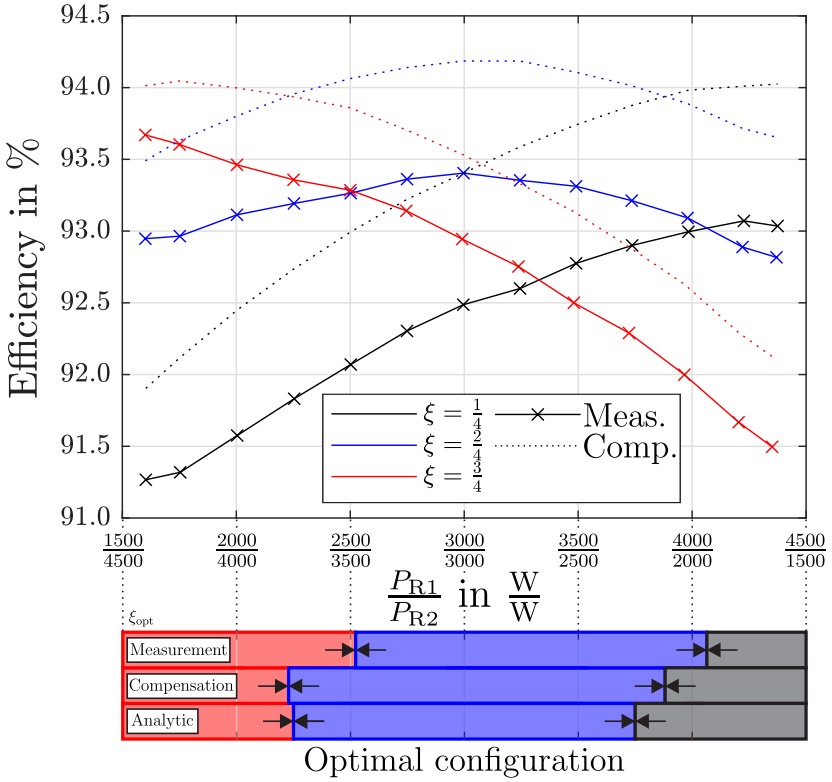


Fig. 3.56: Efficiency of the DAB setup for realization of different link ratios measured in the laboratory, results for compensation of the inequality of the DAB efficiencies, and optimal link ratios via measured, compensated and theoretical results.

via

$$P'_{\mathrm{CS},1,\mathrm{in}} = P_{\mathrm{CS},1,\mathrm{out}} \frac{P_{\mathrm{DAB},2,\mathrm{in}}}{P_{\mathrm{DAB},2,\mathrm{out}}} = \frac{P_{\mathrm{CS},1,\mathrm{out}}}{\eta_{\mathrm{DAB},2}} \tag{3.31}$$

and

$$P'_{\mathrm{DAB},1,\mathrm{in}} = P_{\mathrm{DAB},1,\mathrm{out}} \frac{P_{\mathrm{DAB},2,\mathrm{in}}}{P_{\mathrm{DAB},2,\mathrm{out}}} = \frac{P_{\mathrm{DAB},1,\mathrm{out}}}{\eta_{\mathrm{DAB},2}} \,. \tag{3.32}$$

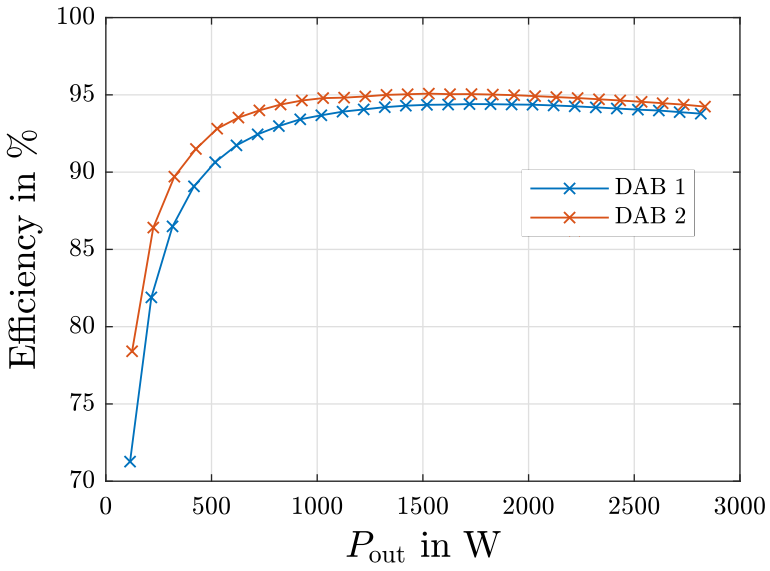


Fig. 3.57: Efficiencies of DAB 1 and DAB 2 measured in the laboratory.

These input powers are inserted with the other power values into (3.30) to calculate the dashed lines in Fig. 3.56. The optimal operation areas for the link ratios with compensated efficiencies are close to the analytical calculated ones. The remaining deviation can be explained by the fact that the output powers of DAB 1 and DAB 2 are not exactly equal for the same applied phase shift due to tolerances of the DAB inductances, which are composed of the leakage inductance of the medium frequency transformers and external inductances.

The results of the presented experiments on the small scale laboratory prototype are:

- It was validated that the link ratio selection in the IT has a significant influence on the system efficiency.
- The possibility to identify optimal operation areas of each link ratio configuration for maximum efficiency was validated.
- The borders of the optimal operation areas of the link ratio configurations will be close to those analytically calculated, if same efficiency behavior of the produced PEBBs can be achieved. Otherwise, the location of the borders can be significantly influenced by asymmetries between the efficiencies of MVac PEBBs connected to the dc-link and the ones of the MVac PEBBs connected to the LVdc feeder.

3.4. Summary and conclusions of the chapter

This chapter introduced the interconnected topology (IT) and the non-interconnected topology (NIT) at first in Section 3.1. These topologies are the realizations of the interconnected and non-interconnected ST architectures presented in Section 2.2 with the converters from Section 2.3. The IT provides an inherited advantage compared to the NIT - the possibility to adapt its configuration via the link ratio. This adaption of the link ratio can be used to realize a reduced required power rating of the interconnecting dual active bridge (DAB) compared to the LVdc DAB as well as to provide improved efficiency of the IT compared to the NIT.

Thereafter, a method to calculate the efficiency of the topologies was proposed. This method consists of two main steps. The first main step is the calculation of efficiency curves for each converter, which give the efficiency of the converter in dependency on its output power. In the second main step these converter efficiency curves are used to calculate the system efficiency based on a non-conserved power flow analysis. The system efficiencies calculated in this way are used to evaluate the design of the IT configuration for optimal efficiency in Section 3.3.

A mission profile-based design procedure for the power ratings of the converters in both topologies was proposed in Section 3.2. The topologies have three ports for MVac, LVac and LVdc grids. Therefore, two mission profiles are needed to define the loading of the system - LVac and LVdc power profiles - which are combined to a hybrid mission profile.

The loading of the interconnecting DAB does not only depend on the operation point of the hybrid mission profile but also on the configuration of the IT via the link ratio. This holds the potential to optimize the link ratio to achieve a minimum required power rating of the interconnecting DAB. For nine considered hybrid mission profiles, a downsizing of the interconnecting DAB power rating to values between 31 % and 39 % of the LVdc DAB power rating can be achieved.

Further, a Monte Carlo-based sensitivity analysis of the determined power ratings against deviations of the real power profiles compared to those assumed for the design was conducted. The analysis showed that the impact of the uncertain knowledge of the hybrid mission profile has to be considered for the mission profile-based design of the converter power ratings. It has been found that implementing the possibility of reconfiguration of the link ratio in the application can significantly reduce the impact of the hybrid mission profile uncertainty on the required sizing of the interconnecting DAB for some of the hybrid mission profiles.

The influence of the configuration of the IT via the link ratio on the efficiency of the converter system was investigated in Section 3.3. Two approaches were proposed to identify the link ratio for optimal average weighted efficiency for the assumed hybrid mission profiles. One is based on extensive modeling of all converter efficiencies as presented in Section 3.1.3. This approach is able to always find the optimal link ratio according to the applied modeling. The other approach is solely based on the knowledge of the hybrid mission profile. It requires no modeling effort and provides low computational burden, but does not always provide the optimal link ratio. However, the not realized efficiency benefit by the suboptimal link ratio choice is small, because at least a link ratio directly next to the optimal one is always chosen.

Finally, a laboratory validation of the efficiency influence of the IT configuration via the link ratio was carried out. A validation of a significant influence of the link ratio selection in the IT on the system efficiency was achieved. Also, the possibility to identify optimal operation areas of each link ratio configuration for maximum efficiency was validated. Another result is that the borders of the optimal operation areas of the link ratio configurations will be close to those analytically calculated, if same efficiency behavior of the produced power electronics building blocks (PEBBs) can be achieved. Otherwise, the location of the borders can be significantly influenced by asymmetries between the efficiencies of MVac PEBBs connected to the dc-link and the ones of the MVac PEBBs connected to the LVdc feeder.

4. Thermal digital twins for condition monitoring and temperature observation

This chapter deals with approaches to evaluate the reliability of power electronics semiconductor modules and to build the basis of a safe operation and methods to support it. Deriving an accurate real-time representation of the thermal behavior via thermal digital twins (DTs) has many synergies for these purposes. For example, it can be used for detecting over-temperatures, giving an essential input to lifetime models, carrying out condition monitoring, and providing the feedback signal for active thermal control methods, which will be addressed in Chapter 5.

The chapter is organized as follows: The fundamentals of thermal modeling are given in Section 4.1. Section 4.2 describes the thermal influence on power semiconductor module reliability by explaining the degradation mechanism evoked by thermal cycles, showing existing lifetime models and their limitations, and giving a review on condition monitoring methods for power semiconductors via the thermal behavior. Afterwards, Section 4.3 proposes the DT-based observation of the power semiconductor thermal behavior by describing the basic principle of a thermal DT, developing DT approaches based on a particle-swarm-optimization (PSO) - based on [31] - and a dual extended Kalman filter (DEKF), comparing both approaches, and extending the DEKF-based thermal DT to a multichip representation, which considers thermal cross coupling effects. Furthermore, the capability of the DEKF-based multichip thermal DT to represent the thermal behavior in real-time is validated on a laboratory setup. A summary and the conclusions of the chapter can be found in Section 4.4.

4.1. Fundamentals of thermal modeling

This section introduces the fundamentals of thermal modeling, which represents the thermal behavior by suitable models. The modeling of the thermal behavior builds the basis of the estimation of the power semiconductor chip temperature and is an essential part in temperature observers.

In this section, the analogy between electrical and thermal modeling is introduced at first. Next, thermal models to represent the thermal behavior between a point of interest and a reference point - therefore, providing the possibility to model the temperature of a single chip - are presented. Afterwards, a commonly used procedure to describe the thermal behavior of multiple chips with thermal cross coupling effects is shown.

4.1.1. Basics of thermal modeling

The different basic components used in thermal modeling are shown in Fig. 4.1 and their analogy to the corresponding components of the electrical modeling is given in Table 4.1. Thermal resistors are used to relate a flow of power losses P_{loss} (dissipated heat flux) to a temperature difference between different locations

$$\Delta T = R_{\text{th}} P_{\text{loss}} \ . \tag{4.1}$$

Thermal capacitors describe the impact of the heat flux storage capacity of materials on the temperature difference between different locations

$$\Delta T(t) = \frac{1}{C_{\text{th}}} \int_0^t P_{\text{loss}}(\tau)\,\mathrm{d}\tau + \Delta T(0) \ . \tag{4.2}$$

For power semiconductor modules, the thermal resistance and capacitance between different locations in the module depend on the properties of the used materials. However, the structure of the materials also plays an important role. For example, material layers with cracks or voids pose a higher thermal resistance for the heat dissipation.

For the heat dissipation process from the converter to the ambient, the convection is another parameter influencing the represented thermal resistance and capacitance between the heat sink and the ambient temperature. Herein, the natural convection poses higher thermal resistance than the forced air cooling - via a cooling fan - and liquid cooling - via a cooling pump - provides lower thermal resistance than forced air cooling.

The combination of multiple thermal resistors and capacitors to networks can be used to describe the complex thermal behavior of multiple thermally coupled material layers and convection processes - such as in a power semiconductor module.

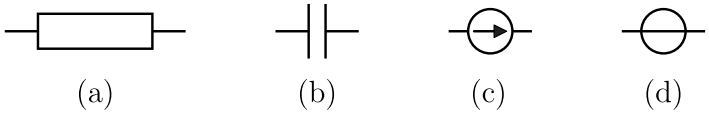


Fig. 4.1: Basic components of thermal modeling, (a) thermal resistor, (b) thermal capacitor, (c) power losses source, and (d) temperature source.

Table 4.1: Analogy between electrical and thermal modeling.

Electrical modeling	Thermal modeling
Electrical resistance R in Ω	Thermal resistance R_{th} in $\mathrm{K/W}$
Electrical capacitance C in F	Thermal capacitance C_{th} in $\mathrm{J/K}$
Current i in A	Power losses P_{loss} in W
Voltage v in V	Temperature T in K or °C

4.1.2. Single chip thermal networks

The description of the thermal behavior between a point of interest and a reference point in a power semiconductor module can be based on a Foster network (Fig. 4.2) or a Cauer network (Fig. 4.3), which are often used for thermal descriptions in a power electronics context. The point of interest is in most cases a semiconductor chip with the temperature T_1. The reference temperature T_{ref} is taken from a reference point, which is often the ambient (ambient temperature T_{a}) or the case of the power semiconductor module. The heat flux generated at the point of interest is due to the power losses of the chip P_{loss}.

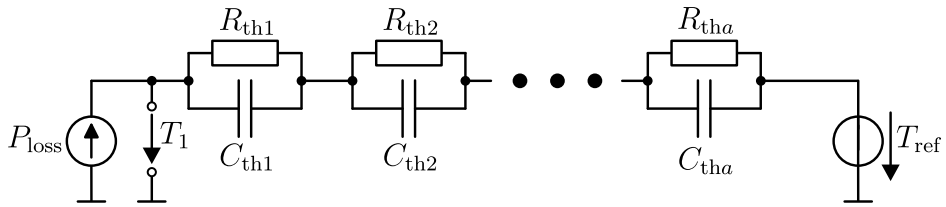


Fig. 4.2: Foster network modeling the thermal behavior of a semiconductor.

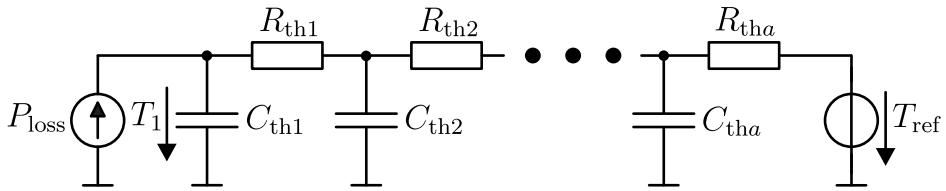


Fig. 4.3: Cauer network modeling the thermal behavior of a semiconductor.

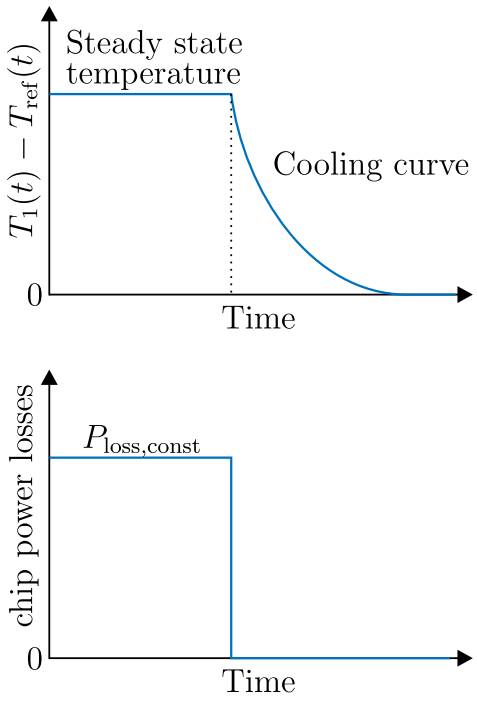


Fig. 4.4: Schematically shown cooling curve for thermal characterization after heating the power semiconductor chip with constant losses to a steady state temperature.

The thermal impedance $Z_{\mathrm{th}}(t)$ can be characterized by utilizing the cooling curve of the temperature difference between chip and reference point $T_{\mathrm{l}}(t) - T_{\mathrm{ref}}(t)$, shown in Fig. 4.4. The power semiconductor chip is heated with constant losses $P_{\mathrm{loss,const}}$ to a steady state of this temperature difference and then the semiconductor losses are turned off - for such tests an externally controlled dc current, which is flowing through the permanently turned on semiconductor (heating by the conduction losses), is utilized in most cases. After turning the losses off, the cooling curve can be recorded and the thermal impedance can be calculated by

$$Z_{\mathrm{th}}(t) = \frac{T_{\mathrm{l}}(t) - T_{\mathrm{ref}}(t)}{P_{\mathrm{loss,const}}} \ . \tag{4.3}$$

To represent the thermal impedance given by (4.3) a Foster network (Fig. 4.2) is commonly used. The thermal impedance of the Foster network can be expressed as

$$Z_{\mathrm{th}}(t) = \sum_{j=1}^{a} R_{\mathrm{th}j} \left(1 - \mathrm{e}^{-\frac{t}{\tau_{\mathrm{th}j}}} \right) \tag{4.4}$$

with

$$\tau_{\mathrm{th}j} = R_{\mathrm{th}j} C_{\mathrm{th}j} \ . \tag{4.5}$$

The thermal resistances $R_{\mathrm{th}j}$ and thermal time constants $\tau_{\mathrm{th}j}$ of the different Foster network chain elements are then adjusted by an optimization algorithm to find the optimal representation of the measured impedance during the cooling curve - found by (4.3) - via the Foster network impedance (4.4). The derivative of the characterized thermal impedance, a measurement of the reference temperature, and measurement or calculation of the losses in the chip can be used to estimate the chip temperature $\hat{T}_{\mathrm{l}}(t)$ by calculation of the convolution

$$\hat{T}_{\mathrm{l}}(t) = \dot{Z}_{\mathrm{th}}(t) * P_{\mathrm{loss}}(t) + T_{\mathrm{ref}}(t) \ . \tag{4.6}$$

If the Cauer network is used to represent the thermal impedance, the thermal resistances $R_{\mathrm{th}j}$ and thermal capacitances $C_{\mathrm{th}j}$ of the Cauer network (Fig. 4.3) are often derived by modeling the thermal properties of the different material layers between the chip and the reference point (physical modeling). The main advantage of a Cauer network derived by physical modeling compared to a Foster network fitted to measurements is that it can theoretically be used to access temperatures of intermediate material layers within the power semiconductor module, which are not accessible by sensor placement. However, the Foster network fitted to the measured thermal behavior will represent the real thermal behavior between chip and reference point more accurately. Therefore, the parameters of a Cauer network can also be fitted to the measure thermal impedance (4.3) after the physical modeling is executed - as a form of fine tuning. This in turn makes the precision of accessing the temperature of specific material layers within the power semiconductor module questionable.

Another advantage of the Cauer network compared to the Foster network is that the sequence of the different chain elements impacts the resulting thermal behavior. The importance of this property for the implementation of a thermal DT will be presented in Section 4.3. To implement the thermal network in a real-time simulation (RTS) for the realization of the thermal DT, it is necessary to have discrete formulas which are executed at the thermal RTS time step d_{th}. The Cauer network equations discretized with forward Euler method for a network with three chain elements are

$$\begin{aligned} T_1(k+1) = T_{C_{\mathrm{th1}}}(k+1) =& T_{C_{\mathrm{th1}}}(k) + \frac{P_{\mathrm{loss}}(k)d_{\mathrm{th}}}{C_{\mathrm{th1}}} - \frac{(T_{C_{\mathrm{th1}}}(k) - T_{C_{\mathrm{th2}}}(k))d_{\mathrm{th}}}{R_{\mathrm{th1}}C_{\mathrm{th1}}} \\ T_{C_{\mathrm{th2}}}(k+1) =& T_{C_{\mathrm{th2}}}(k) + \frac{(T_{C_{\mathrm{th1}}}(k) - T_{C_{\mathrm{th2}}}(k))d_{\mathrm{th}}}{R_{\mathrm{th1}}C_{\mathrm{th2}}} - \frac{(T_{C_{\mathrm{th2}}}(k) - T_{C_{\mathrm{th3}}}(k))d_{\mathrm{th}}}{R_{\mathrm{th2}}C_{\mathrm{th2}}} \\ T_{C_{\mathrm{th3}}}(k+1) =& T_{C_{\mathrm{th3}}}(k) + \frac{(T_{C_{\mathrm{th2}}}(k) - T_{C_{\mathrm{th3}}}(k))d_{\mathrm{th}}}{R_{\mathrm{th2}}C_{\mathrm{th3}}} - \frac{(T_{C_{\mathrm{th3}}}(k) - T_{\mathrm{ref}}(k))d_{\mathrm{th}}}{R_{\mathrm{th3}}C_{\mathrm{th3}}} \end{aligned} . \tag{4.7}$$

4.1.3. Multichip thermal networks

A power semiconductor module contains multiple chips, which can have significant thermal cross coupling effects [61]. Thermal cross coupling means that the temperature of the chips in relation to the reference point temperature are not only influenced by the losses inside the single chips themselves, but also by the losses dissipated in other chips of the module located near to them.

An often applied approach to model multichip power semiconductor modules with significant thermal cross coupling effects is the linear accumulation of all impacts on the temperatures by losses in the chips [62–66]. Herein, a Foster network is characterized for the impact of each source of heat flux - losses in chips - on all considered chip temperatures, as shown in Fig. 4.5. One way to characterize these Foster networks is to apply an externally controlled dc current to one of the chips until steady states for all the differences of chip temperatures to the reference temperature are reached and to record the cooling curves (Fig. 4.4) then.

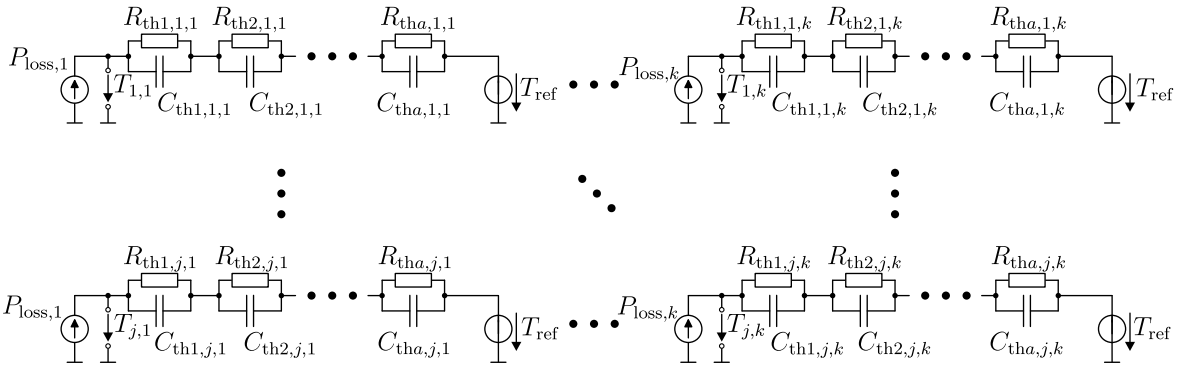


Fig. 4.5: Linear accumulation approach to model thermal cross coupling effects between multiple semiconductors via Foster networks.

With the cooling curves the thermal impedances can be calculated with (4.3) and a fitting of the Foster network impedances (4.4) can be made to characterize the Foster network parameters. This procedure is repeated for all considered sources of losses (chips) to characterize all Foster networks shown in Fig. 4.5. The derivatives of the resulting thermal impedances for self heating and thermal cross coupling are then combined in the matrix

$$\dot{\boldsymbol{Z}}_{\mathrm{th}}(t) = \begin{bmatrix} \dot{Z}_{\mathrm{th}}^{11} & \dot{Z}_{\mathrm{th}}^{12} & \cdots & \dot{Z}_{\mathrm{th}}^{1k} \\ \dot{Z}_{\mathrm{th}}^{21} & \dot{Z}_{\mathrm{th}}^{22} & & \\ \vdots & & \ddots & \vdots \\ \dot{Z}_{\mathrm{th}}^{j1} & \cdots & \cdots & \dot{Z}_{\mathrm{th}}^{jk} \end{bmatrix} (t) \ . \tag{4.8}$$

The j chip temperatures $\hat{\boldsymbol{T}}(t)$ can be estimated by calculating the convolutions of the vector of loss sources $\boldsymbol{P}_{\mathrm{loss}}(t)$ with the matrix entries of (4.8)

$$\hat{\boldsymbol{T}}(t) = \dot{\boldsymbol{Z}}_{\mathrm{th}}(t) * \boldsymbol{P}_{\mathrm{loss}}(t) + \boldsymbol{T}_{\mathrm{ref}} \ . \tag{4.9}$$

Herein, the results of the convolutions for each of the matrix rows are linearly accumulated for the respective chip temperature. In this way, the chip temperatures are calculated by superposition of the impact of each of the loss sources.

4.2. Thermal influence on power semiconductor module reliability

This section highlights the essential influence of the temperature on the reliability of power semiconductor modules. Changes of the temperature are a main reason for the wear-out of power semiconductor modules. Observing the thermal loading of power modules by temperature changes allows to estimate their expected lifetime. The thermal behavior changes with degradation of power modules and can be used to monitor their health condition.

In this section, the degradation mechanism of power modules by thermal cycles is explained at first. Next, the principle of thermal cycle-based lifetime estimation by lifetime models is presented and their limitations are discussed. Afterwards, a review on condition monitoring of power semiconductors via the thermal behavior is given.

4.2.1. Degradation mechanism

Power electronics converters need to process power depending on the supplied loads. Changes or cycles of the required load power lead to adjustment of the processed converter power. With increasing processed power of a converter the losses in the chips of its semiconductors increase. This increase of the losses leads to an increase of the chip temperature. When the

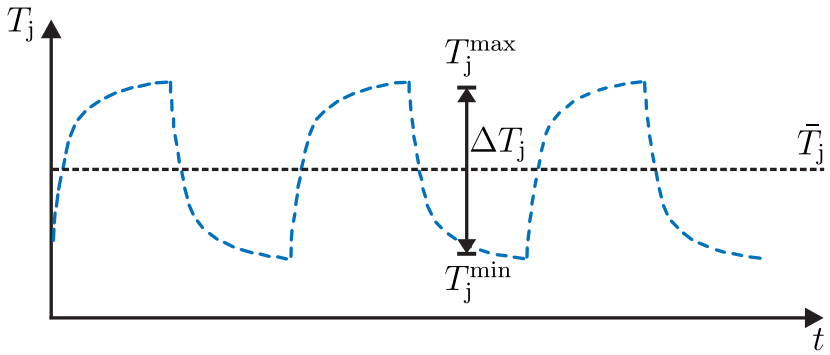


Fig. 4.6: Junction temperature cycles with characteristic values.

processed power of the converter decreases, the losses in the chips decrease and, therefore, also the chip temperature.

This means that cycles of the required load power lead to thermal cycles of the power semiconductor chips, as shown in Fig. 4.6. Two characteristic values to describe a thermal cycle are the mean junction temperature $\bar{T}_\mathrm{j}$ and the junction temperature swing ΔT_j. The word junction refers in this context to a region within the power semiconductor chip, which is expected to be the origin of the heat flux due to the losses. Accessing the junction temperature is only possible via the measurement and characterization of temperature sensitive electrical parameters (TSEPs) [67–69], such as the saturation voltage for IGBTs [70, 71]. For the characterization of the temperature dependency of a TSEP, the power semiconductor chip is heated externally to the different temperature points of the characterization in order to ensure an equal temperature distribution in the chip. Having this equal temperature distribution ensures that also the not exactly defined junction zone has this temperature. Afterwards, the TSEP is measured and related to the junction temperature via the characterization. Thereby, it is important to consider other influences on the specific TSEP as well as changes of the temperature dependent characteristic due to the wear-out process in order to evaluate or improve the accuracy of the junction temperature identification.

A power semiconductor module is built of different material layers, as schematically shown in Fig. 4.7. The used materials have different coefficients of thermal expansion (CTE) listed in Table 4.2. When the temperatures of the layers change, their geometrical sizes change to different degrees, which causes mechanical strain at the joints of the material layers. The

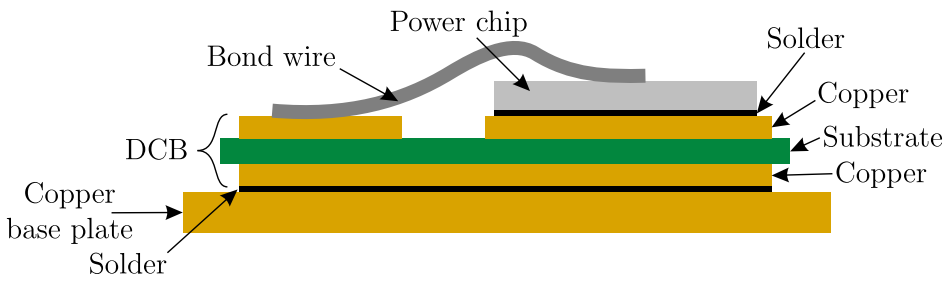


Fig. 4.7: Basic layer structure of a power electronics module.

Table 4.2: Coefficients of thermal expansion of material layers in power semiconductor modules [50].

Material	Coefficient of thermal expansion in $\frac{10^{-6}}{\mathrm{K}}$
Aluminum (bond wires)	22.5
Silicon (chips)	4.1
Solder (joints)	15.0 to 30.0
Copper (connection layers and base plate)	17.5
Aluminum oxide (insulation layer of DCB)	8.3

mechanical strain at the joints is the root cause of power semiconductor module degradation.

The degradation of the bond-wires causes higher losses and the solder degradation a higher thermal resistance of the solder layers and, therefore, higher junction temperatures. The increasing losses and reduced heat dissipation lead to higher thermal cycles on the power semiconductor modules. The higher thermal cycles lead to a faster degradation. This positive feedback loop accelerates towards the end of life of power semiconductor modules. Some of the major failures at the end of life are liftoff of the bond wires and bond wire heal cracking [72] as well as cracking of the solder joints [73].

4.2.2. Thermal cycle-based lifetime estimation

The influence of thermal cycles on the degradation of power semiconductor modules provides the possibility to estimate the lifetime based on the junction temperature. The method for this estimation is presented in Fig. 4.8. Similar to the explanation of the degradation mechanism, the first three steps are:

- The required load power (mission profile) defines what power needs to be processed by the converter.
- The converter losses result from the operation of the converter at the defined output power.
- The heat flux due to the losses together with the thermal behavior determines the junction temperature of the power semiconductors.

The following two steps relate the junction temperature profile to the degradation of the power semiconductor module:

- The rainflow counting algorithm [74] is commonly used to identify numbers of thermal cycles with certain mean junction temperature $\bar{T}_\mathrm{j}$ and junction temperature swing ΔT_j from the thermal profile.

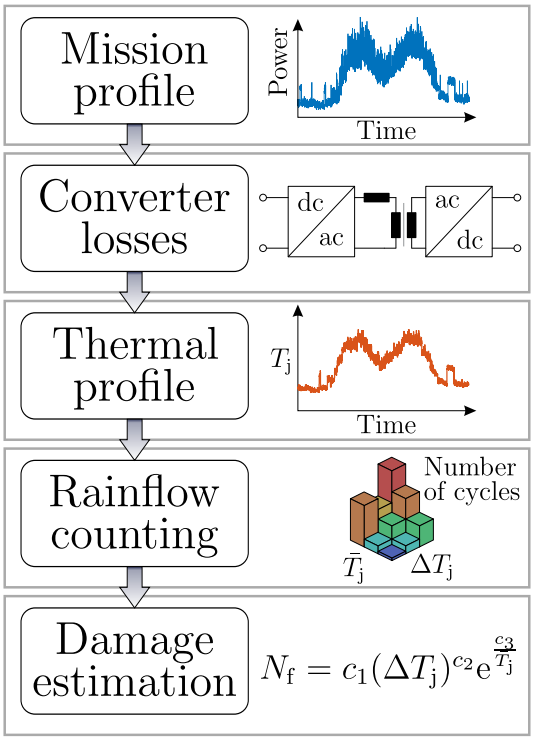


Fig. 4.8: Method for lifetime estimation of power semiconductors.

- The last step is to estimate the damage done by the identified thermal cycles via lifetime models characterized with data from power cycling tests.

The lifetime models describe the number of cycles until a failure would occur N_f for specific permanently applied operation conditions. A basic lifetime model [75] only represents the dependency of N_f on the mean junction temperature $\bar{T}_j$ and the junction temperature swing ΔT_j

$$N_{f,1} = c_{1,1}(\Delta T_j)^{c_{2,1}} e^{\frac{c_{3,1}}{\bar{T}_j}} \quad . \tag{4.10}$$

The coefficients $c_{1,1}$, $c_{2,1}$, $c_{3,1}$ are determined based on accelerated power cycling test results, shown in Fig. 4.9. In accelerated power cycling tests power semiconductor modules are exposed to high thermal swings to achieve a rapid degradation of the modules in order to have reasonable test times. The thermal swings can be evoked actively - power cycling - via an externally controlled dc current flow through the semiconductors (alternatively also the real operation mission profiles under harsh circumstances can be used for power cycling [76, 77]) or passively - thermal cycling - via a heating chamber.

While [78] confirmed these basic relations (4.10) for temperature swings of 80 K and 100 K, [18, 79, 80] identified the time of the temperature rise t_r (heating time) applied in the accelerated cycling tests as a significant influencing factor of N_f

$$N_{f,2} = c_{1,2}(\Delta T_j)^{c_{2,2}} e^{\frac{c_{3,2}}{\bar{T}_j}} \left(\frac{t_r}{1.5}\right)^{c_{4,2}} \quad . \tag{4.11}$$

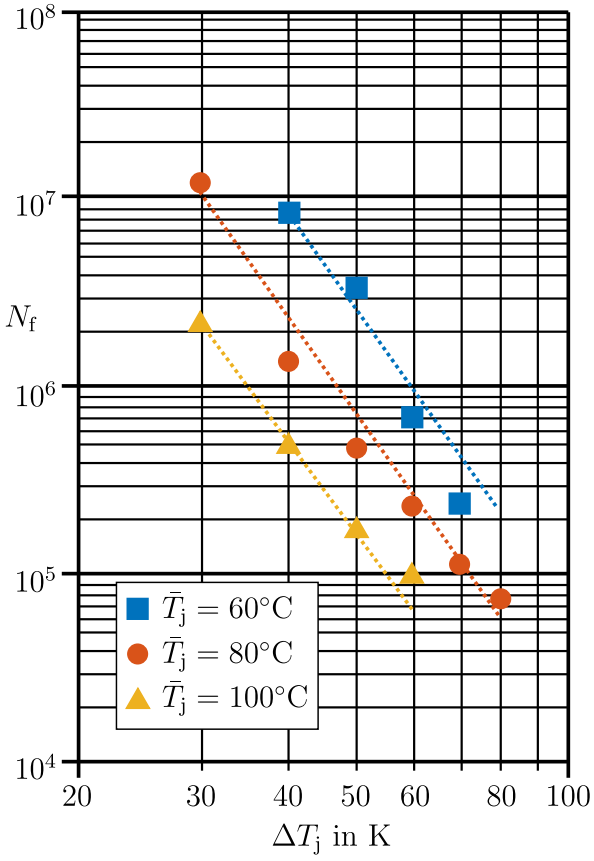


Fig. 4.9: Results of cycle to failure experiments via accelerated power cycling (adapted from [75]).

Such as for the basic lifetime model, the coefficients $c_{1,2}$, $c_{2,2}$, $c_{3,2}$, $c_{4,2}$ should be determined based on accelerated power cycling test results.

Furthermore, [81] proposed to include the influences of the dc current I used for heating in the accelerated power cycling tests, of the power semiconductor modules voltage rating V_{rated}, and of the bond wire diameter b_{dia} on N_f

$$N_{f,3} = c_{1,3}(\Delta T_j)^{c_{2,3}} \mathrm{e}^{\frac{c_{3,3}}{\bar{T}_j}} t_r^{c_{4,3}} I^{c_{5,3}} V_{\text{rated}}^{c_{6,3}} b_{\text{dia}}^{c_{7,3}} \quad . \tag{4.12}$$

Also herein, the coefficients $c_{1,3}$, $c_{2,3}$, $c_{3,3}$, $c_{4,3}$, $c_{5,3}$, $c_{6,3}$, $c_{7,3}$ should be determined based on accelerated power cycling test results.

According to Miner's rule [82], the consumption of the power semiconductor modules total lifetime is calculated by linear accumulation of the lifetime consumption calculated for each thermal cycle. When the sum of the numbers of cycles divided by the respective number of cycles to failure reaches one

$$\sum_{j=1}^{a} \frac{n_{f,j}}{N_{f,j}} = 1 \quad , \tag{4.13}$$

the power semiconductor module is expected to fail.

However, [83, 84] showed that the assumption of linear damage accumulation is not ac-

curate, because applying small thermal cycles to a degraded power semiconductor module caused an increase of the thermal resistance, while applying same thermal cycles to a new module showed no effect on the thermal resistance. Furthermore, [83–86] showed that lifetime models characterized by accelerated power cycling tests at high ΔT_j are inaccurate for temperature profiles with mostly low ΔT_j. Another concern that is raised especially for lifetime models with a high number of influencing factors, is the number of power cycling tests needed to achieve a trustworthy characterization. However, even with a high number of power cycling tests at high temperature swings, the accuracy at low temperature swings cannot be guaranteed [87].

Besides the concerns about the applicability of lifetime model, an essential requirement for the lifetime estimation with lifetime models is the availability of accurate chip temperature measurements as well as the knowledge about the thermal behavior to predict future thermal loading. The thermal behavior changes during the wear-out process of power semiconductor modules, therefore, adjusting the thermal models is important to maintain an accurate prediction of the chip temperature. Furthermore, having more accurate thermal models also brings advantages for their utilization in thermal observers [69]. Thermal observers are a combination of temperature prediction based on a thermal model - presented in Section 4.1 - and a correction based on temperature measurements - via a comparison to the estimated temperature and adjustment of the thermal model input (losses) by a correction controller. Thermal observers allow to access the temperature with low noise - due to the model-based estimation - while being still precise - due to the measurement-based correction. Further, it is possible to access the temperature without phase lag by modeling also the measurement delay of the temperature sensor and the conditioning circuit.

4.2.3. Review on condition monitoring of power semiconductors via thermal behavior

The categories of possibilities that allow monitoring solder degradation in power semiconductor modules are presented in Fig. 4.10. There are possibilities to access the solder joint

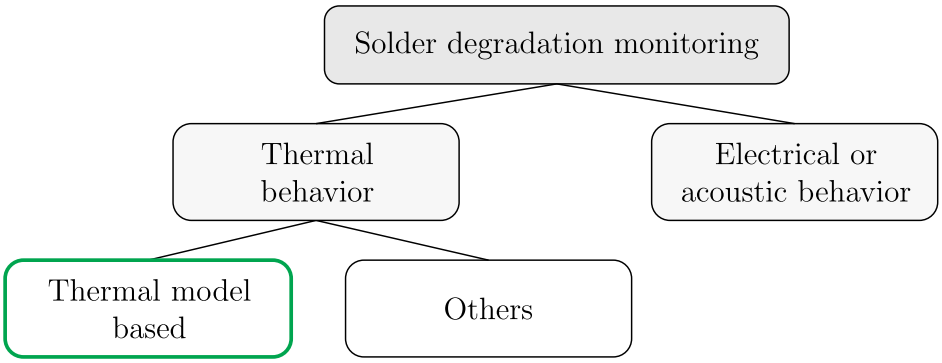


Fig. 4.10: Categories of solder degradation monitoring possibilities.

condition via the electrical or acoustic behavior of the power semiconductors. Using real-time scanning acoustic tomography [88] or acoustic emission monitoring [89–91] provides direct information about the structure of the solder joints. However, their application is limited to the laboratory, for example to monitor the solder degradation during power cycling tests. The use of time-domain reflectometry is a way to measure solder joint cracking via the electrical behavior [92], which could be theoretically also used for application in the field.

This work focuses on the thermal behavior of power semiconductors, which is important to monitor their health condition via direct measurements [15, 93–96]. One major wear-out process due to the degradation mechanism by thermal cycles is cracking of the solder joints, which changes the thermal behavior of the power semiconductors. Measuring the change of thermal behavior allows to monitor the condition of the solder joints. Besides the utilization of thermal models for monitoring, the use of neural networks [97], time series nonparametric models [98], and multiple weight function networks [99] has been proposed to detect solder layer fatigue. However, this work focuses on describing the thermal behavior via thermal models for the development of a thermal DT in Section 4.3, because the integration of established thermal models - presented in Section 4.1 - provides the possibility to limit the search area to find an optimal representation. Furthermore, the utilization of thermal models allows a direct interpretation of the model parameters.

An often used parameter to identify solder degradation in power semiconductor modules is the total thermal resistance [15, 100–110], which is the sum of R_{th} values of all chain elements of the single chip thermal models presented in Section 4.1. A wear-out criterion for $\sum_{j=1}^{a} R_{\mathrm{th}j}$ is an increment of $+20\,\%$ compared to the initial value of a new power semiconductor module [15, 100, 103, 110, 111]. Other possibilities that can be used to evaluate the solder degradation, if an accurate thermal model is available, are:

- Using the frequency response function of the thermal behavior for health monitoring of the solder joints and the cooling system [112–117].
- Using the transient thermal behavior for health monitoring of the solder joints and the cooling system [118, 119].
- Using thermal resistance as well as thermal capacitance values for health monitoring of the solder joints and the cooling system [111, 120–122].
- Using thermal resistance from module case to ambient or the case temperature difference for health monitoring of the cooling system [100, 123].
- Comparing the heat flux through the base plate with the one through the silicone gel for health monitoring of the solder joints and the cooling system [124].
- Using the thermal time constant of the heat sink cooling curve for health monitoring of the solder joints and the cooling system [125].

- Using the phase shift between losses and the junction temperature inserted by the low-pass effect of the thermal network for health monitoring of the solder joints and the cooling system [126].

For these possibilities, the thermal interface material between module base plate and heat sink is considered as part of the cooling system.

Adjusting the thermal model for an optimal representation of the real thermal behavior via the thermal DT approaches that are developed in Section 4.3 enables the use of the different methods of thermal model-based condition monitoring of power semiconductor modules. However, the change of thermal behavior will be a combination of increasing losses by bond wire degradation and higher thermal resistance by solder degradation [103]. This combination of the different degradation processes could be decoupled, if the collector emitter voltage of an insulated gate bipolar transistor (IGBT) is used as TSEP [127–129]. Another approach is to adjust the loss model instead of the thermal model [113, 116]. The scope of this work is on the adjustment of the thermal model, therefore, the additional increase of the derived thermal resistance by the losses increasing with degradation needs to be considered for defining wear-out criteria.

4.3. Digital twin-based observation of power semiconductor thermal behavior

This section develops thermal DT approaches to observe the thermal behavior of power semiconductors. The concept of DTs is of growing interest for academia as well as industry [130]. However, the term *digital twin* has not one clearly defined meaning, but describes different concepts depending on the context. In the context of representing a power electronics converter the DT concept has three main components:

- A real-time simulation (RTS) of a model describing a converter behavior (virtual).
- Comparison of the model estimates with measured quantities (physical).
- An optimization algorithm adjusting the RTS model parameters to achieve an optimal representation of the physical converter behavior by the virtual model.

For DTs of the electrical behavior of power electronics converters, different optimization algorithms have been applied, which are a PSO [131–136], polynomial chaos expansion [137], bayesian optimization [138], genetic algorithm [134], arithmetic optimization algorithm [135], and the combination of the virtual model with the optimization algorithm via a dynamic neural network [139]. [140] proposed a DT of the thermal converter behavior based on a DEKF. However, this DT is implemented with the assumption of access to temperature measurements at all nodes of the equivalent thermal circuit. Therefore, this approach either

relies on non-accessible temperature measurements within the power semiconductor modules or it has only low fitting accuracy by using a model consisting of one chain element for a high number of thermal layers. Anyway, the assumption leads to a decoupled mathematical problem where only one chain element of the Cauer network is optimized for each pair of temperature measurements individually. Other approaches providing an adaptive parameter thermal model scale the thermal resistances with aging of the power semiconductor module [141–143] or use an adaptive physical modeling of the thermal resistances and capacitances based on multiple case temperature measurements [144]. The aim of the approaches developed in this section is to provide adjustable thermal real-time models - optimizing resistance as well as capacitance values - with multiple chain elements by utilizing only chip and ambient temperature measurements and without the necessity of previous knowledge on the thermal properties of the system.

In this section, the basic principle of a thermal DT is presented at first. Next, thermal DT approaches based on a PSO and a DEKF are developed and compared. Afterwards, the DEKF-based thermal DT is extended to a multichip representation, which considers thermal cross coupling effects. Furthermore, the capability of the DEKF-based multichip thermal DT to represent the thermal behavior in real-time is validated on a laboratory setup.

4.3.1. Basic principle of a thermal digital twin

A thermal DT is a virtual real-time replica of the thermal behavior of a power semiconductor. The approaches developed in this work do not need any previous knowledge of the thermal behavior of the power semiconductor.

The general structure of a thermal DT is shown in Fig. 4.11. In the physical space there is the converter and its control, these are represented by a laboratory setup with a converter, which gets gate signals from a Digital Signal Processor (DSP) in this work. The gate signals are given to the virtual space at the same time, where they are used in an electrical RTS of the physical converter. In this work a simplified buck converter (Fig. 4.12) is considered

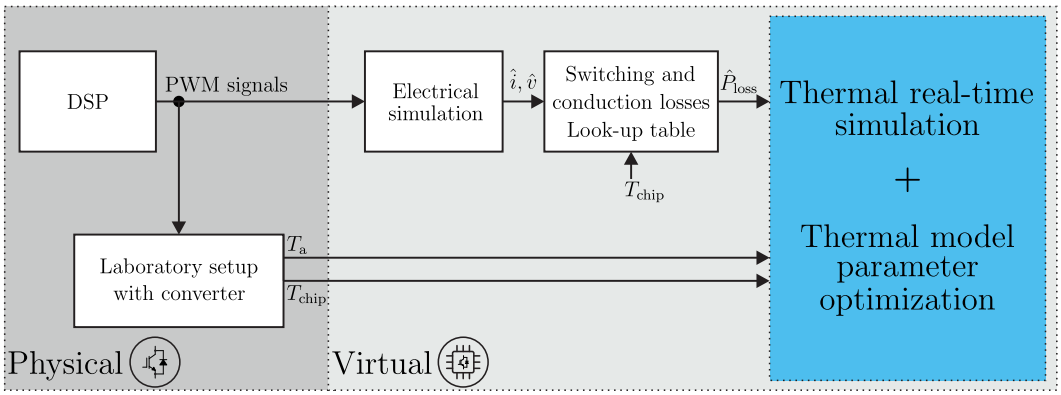


Fig. 4.11: General scheme of a thermal digital twin of a power module.

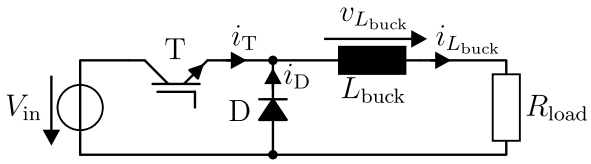


Fig. 4.12: Buck converter used for demonstration of a thermal digital twin.

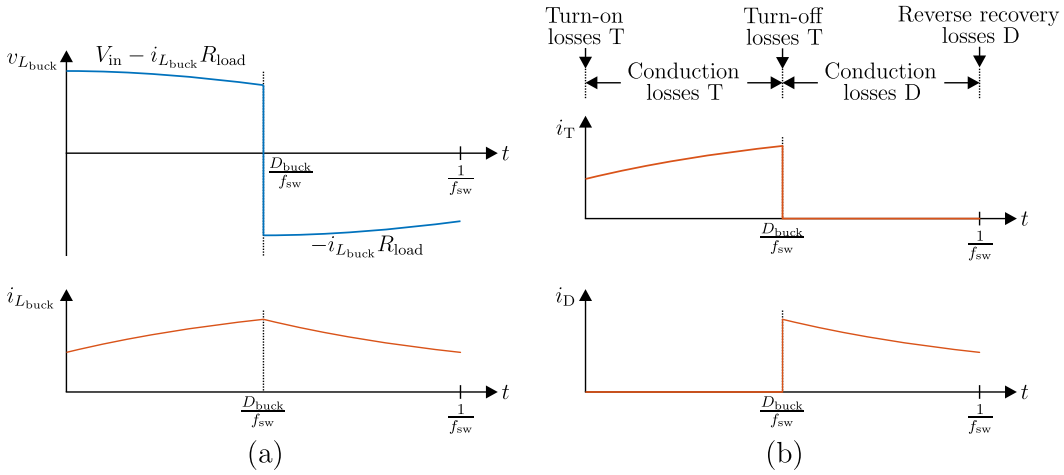


Fig. 4.13: Schematic waveforms of buck converter: (a) inductor voltage and current, (b) semiconductor currents, indication of conduction loss intervals and switching events.

for the thermal DT application, because the loading of the semiconductors can be easily adjusted via the duty cycle D_{buck} of the switch T, which is the on-time of the switch divided by the period $\frac{1}{f_{\text{sw}}}$. A schematic representation of current and voltage waveforms of this buck converter is given in Fig. 4.13. Currents $\hat{i}$ and voltages $\hat{v}$ estimated by the electrical RTS as well as information about the switching and conduction of the different semiconductors of the converter are used to estimate the switching and conduction losses $\hat{P}_{\text{loss}}$ via look-up tables.

For the calculation of the losses based on an electrical RTS, the relation between the fixed step size of the electrical RTS d_{exe} and the switching frequency f_{sw} of the converter influences the accuracy of the loss calculation. In order to demonstrate the impact of this relation on the accuracy of the loss calculation, a simulation of the electrical waveforms and the losses of the buck converter has been carried out in Matlab/Simulink with PLECs blockset (ode 3 (Bogacki-Shampine) solver) using a fixed time step of $d_{\text{exe}} = 1\,\mu\text{s}$ and comparing it with the results of a simulation with a fixed time step of 1 ns as reference. Herein, the input voltage V_{in} is 400 V, the load resistance R_{load} is 16 Ω and an operation at a chip temperature of 125 °C is assumed. The loss characteristics of an FP25R12KE3 IGBT module from Infineon are considered in this section and this module is also used in the laboratory setup of the thermal DT. The inductance of the buck converter L_{buck} is adjusted based on the used switching frequency

$$L_{\text{buck}} = 0.25 \frac{1}{f_{\text{sw}}} \frac{V_{\text{in}}}{1\,\text{A}} \quad . \tag{4.14}$$

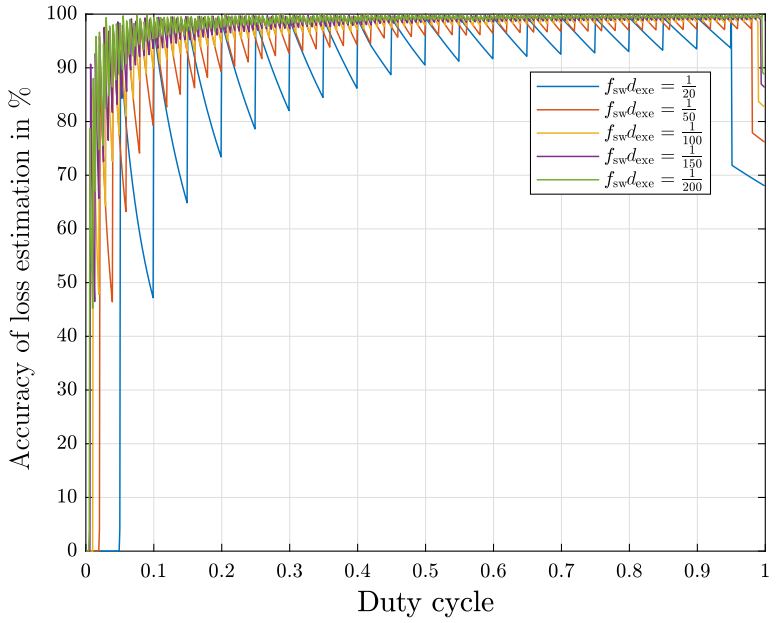


Fig. 4.14: Loss estimation accuracy of a buck converter depending on the duty cycle for different relations of switching frequency f_{sw} and discrete simulation time step d_{exe}.

The loss estimation accuracy - calculated by dividing the losses calculated with $d_{exe} = 1\,\mu s$ by those calculated with a fixed time step of $1\,ns$ - is shown in Fig. 4.14 depending on the applied duty cycle and the used switching frequency. With rising duty cycle the accuracy of the loss estimation has a sawtooth shape due to the resolution of the duty cycle. If the duty cycle value can be represented exactly in the fixed time step simulation, the accuracy of the loss estimation is high. However, the accuracy of the loss estimation drops for further rising duty cycle, because the following duty cycle values cannot be represented, until the next duty cycle that can be exactly represented is reached. How many duty cycles can be exactly represented depends on the ratio $f_{sw}d_{exe}$. This ratio also defines how far the loss estimation accuracy drops between these duty cycle values exactly represented. In this work a ratio $f_{sw}d_{exe}$ of $\frac{1}{100}$ is applied.

The estimated losses $\hat{P}_{loss}$ and the measured ambient temperature T_a are the inputs for the thermal prediction or for multiple thermal RTSs, depending on the approach used to realize the thermal DT. Measurements of one or multiple chip temperatures T_{chip} of the physical converter are used to optimize the parameters of the thermal model, which builds with its differential equations - (4.7) from Section 4.1 - the basis for the execution of the thermal prediction or the thermal RTSs. The optimization algorithms used to develop thermal DT approaches are the particle-swarm-optimization (PSO), which was used for developing multiple electrical DTs of power electronics converters [131–136], and the dual extended Kalman filter (DEKF). Extended Kalman filters have broad application in other disciplines and also shown potential for thermal modeling of power electronics converters [140, 145].

In the following subsections, the PSO- and DEKF-based DT approaches will be implemented for the single chip Cauer network with three chain elements shown in Fig. 4.15. Both ap-

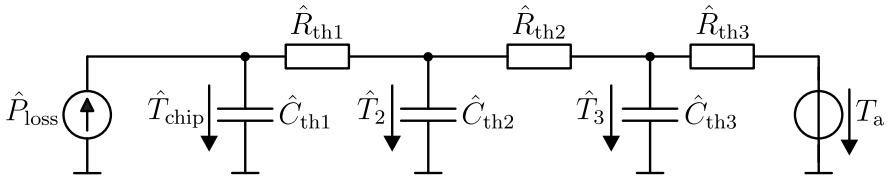


Fig. 4.15: Cauer network with three chain elements used for the thermal digital twin of a single chip.

proaches will be compared based on the results for the single chip thermal DT.

4.3.2. Particle swarm optimization-based thermal digital twin

The realization of the thermal DT via the PSO (Fig. 4.16) contains B_{PSO} thermal RTSs (particles), which are executed in parallel. All these thermal RTSs execute the differential equations of the same thermal model - (4.7) from Section 4.1 -, but each of these particles b has its own set of parameters

$$\boldsymbol{p}_{\mathrm{PSO},b} = [\hat{R}_{\mathrm{th1},b}\ \hat{C}_{\mathrm{th1},b}\ \hat{R}_{\mathrm{th2},b}\ \hat{C}_{\mathrm{th2},b}\ \hat{R}_{\mathrm{th3},b}\ \hat{C}_{\mathrm{th3},b}] \qquad \forall b \in [1, B_{\mathrm{PSO}}] \tag{4.15}$$

characterizing the thermal model shown in Fig. 4.15.

The performance of each particle is evaluated via an objective function value $f_{\mathrm{obj},b}$, which is calculated from the estimated chip temperature of the particle $\hat{T}_{\mathrm{chip},b}$ and the measured chip temperature T_{chip}

$$\begin{aligned} f_{\mathrm{obj},b} = & \frac{d_{\mathrm{th}}}{d_{\mathrm{PSO}}} \left(\sum_{k=1}^{\frac{d_{\mathrm{PSO}}}{d_{\mathrm{th}}}} \left(\left(\hat{T}_{\mathrm{chip},b}(k) - T_{\mathrm{chip}}(k) \right)^2 \right. \right. \\ & \left. \left. + \frac{c_{\mathrm{PSO,d}}}{d_{\mathrm{th}}^2} \left(\Delta\hat{T}_{\mathrm{chip},b}(k) - \Delta T_{\mathrm{chip}}(k) \right)^2 \right)^{\frac{1}{2}} \right) \qquad \forall b \in [1, B_{\mathrm{PSO}}] \ . \end{aligned} \tag{4.16}$$

Herein, d_{th} is the execution time step of the thermal simulation, d_{PSO} is the execution time

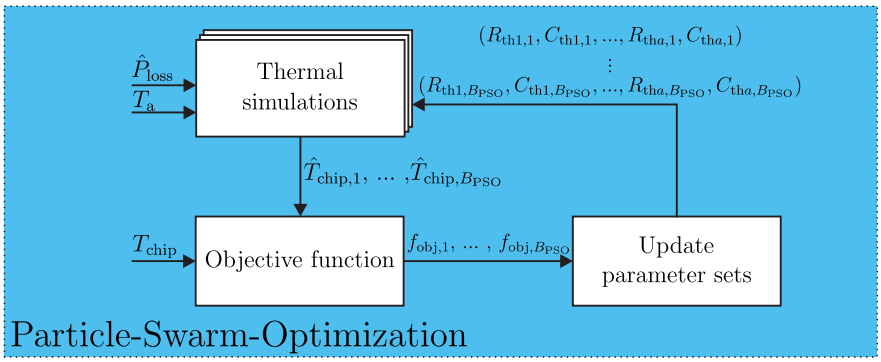


Fig. 4.16: Addition of the general scheme of a thermal digital twin of a power module for utilization of a particle-swarm-optimization.

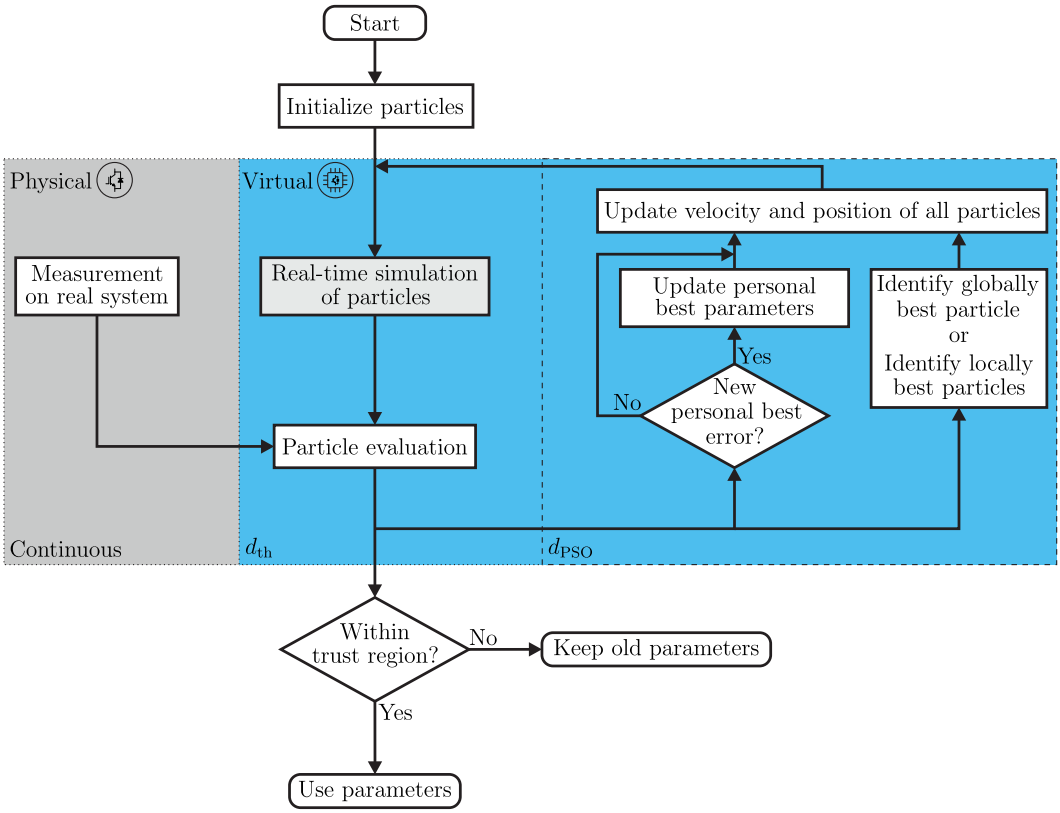


Fig. 4.17: Scheme of particle-swarm-optimization execution in the thermal digital twin.

step of the PSO, $\frac{d_{\mathrm{PSO}}}{d_{\mathrm{th}}}$ gives the number of executions of the thermal RTS during one PSO period, and $c_{\mathrm{PSO,d}}$ is the weighting coefficient of the derivative part.

The scheme of the parameter update of the PSO is shown in Fig. 4.17. Every d_{PSO} the new value of $f_{\mathrm{obj},b}$ is compared to the best objective function value $f_{\mathrm{obj,best},b}$ that was achieved by the particle itself before. If $f_{\mathrm{obj},b} < f_{\mathrm{obj,best},b}$, the particle's best parameter set $\boldsymbol{p}_{\mathrm{PSO,best},b}$ is updated. This is done for all of the B_{PSO} particles in the swarm individually.

Another orientation for the particles is given by the best other particle they know. This knowledge of other particles depends on the information topology that is used for the PSO.

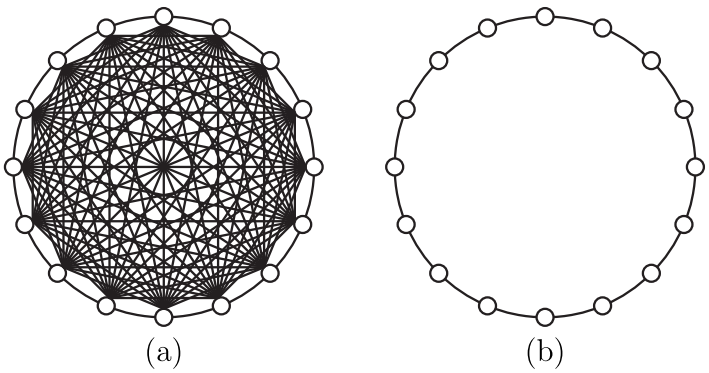


Fig. 4.18: Topologies for information exchange between the different particles in a particle-swarm-optimization: (a) global topology and (b) local topology.

There are two main information topologies for the PSO (Fig. 4.18), the global topology where all particles know all other particles of the swarm and the ring shaped local topology in which each particle only knows two neighbor particles. The global topology provides faster convergence than the local topology, however, it suffers from premature convergence. Therefore, the local topology is used for the PSO-based thermal DT and each particle orients towards the locally best parameter set $\boldsymbol{l}_{\mathrm{PSO,best},b}$.

Associated to the parameter vector $\boldsymbol{p}_{\mathrm{PSO},b}$ each particle also has a velocity vector $\boldsymbol{v}_{\mathrm{PSO},b}$, which describes how each of the parameters changes. The velocities of all parameters for each particle for the next step $k+1$ are calculated via

$$\begin{aligned}\boldsymbol{v}_{\mathrm{PSO},b}(k+1) =& \omega_{\mathrm{PSO}}\boldsymbol{v}_{\mathrm{PSO},b}(k) + c_{\mathrm{PSO},1}r_{\mathrm{PSO},1}(k)(\boldsymbol{l}_{\mathrm{PSO,best},b}(k) - \boldsymbol{p}_{\mathrm{PSO},b}(k)) \\ &+ c_{\mathrm{PSO},2}r_{\mathrm{PSO},2}(k)(\boldsymbol{p}_{\mathrm{PSO,best},b}(k) - \boldsymbol{p}_{\mathrm{PSO},b}(k)) \\ &+ c_{\mathrm{PSO},3}r_{\mathrm{PSO},3}(k)\boldsymbol{p}_{\mathrm{PSO},b}(k) \qquad \forall b \in [1, B_{\mathrm{PSO}}] \ .\end{aligned} \tag{4.17}$$

Herein, the inertia weight is denoted by ω_{PSO}, the coefficients of the PSO are $c_{\mathrm{PSO},1}$, $c_{\mathrm{PSO},2}$, and $c_{\mathrm{PSO},3}$, randomly generated numbers between 0 and 1 are given as $r_{\mathrm{PSO},1}(k)$ and $r_{\mathrm{PSO},2}(k)$, and a randomly generated number between -1 and 1 is given as $r_{\mathrm{PSO},3}(k)$. The first term describes the inertia of the particle, the second term gives the orientation towards the best neighbor particle, the third term includes the orientation towards the best historical parameter set of the particle, and the last term inserts an own vibration. The insertion of own vibration avoids that the swarm converges in local minima of the objective function, which is the case, if all particles reach the same parameter and velocity set.

The new parameters for each particle are calculated by adding the velocities to the previous parameter values

$$\boldsymbol{p}_{\mathrm{PSO},b}(k+1) = \boldsymbol{p}_{\mathrm{PSO},b}(k) + \boldsymbol{v}_{\mathrm{PSO},b}(k+1) \qquad \forall b \in [1, B_{\mathrm{PSO}}] \ . \tag{4.18}$$

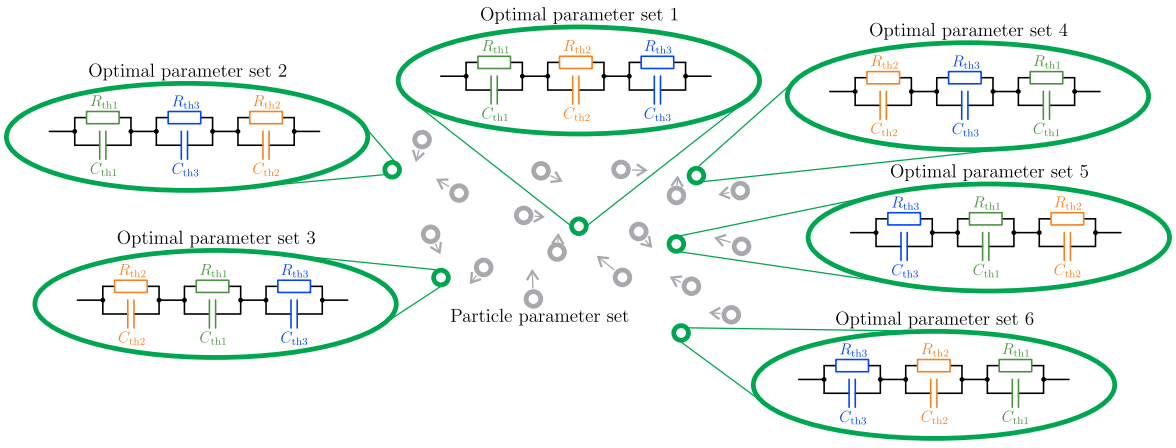


Fig. 4.19: Schematic representation of the search for optimal Foster network parameter sets via the PSO-based thermal digital twin.

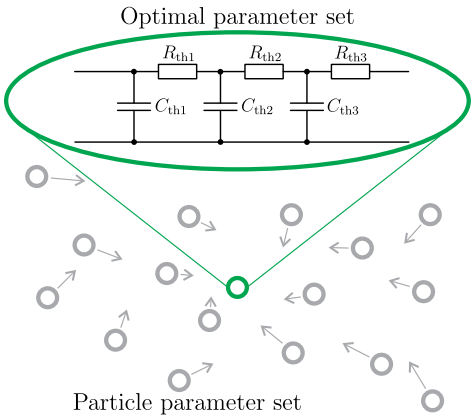


Fig. 4.20: Schematic representation of the search for the optimal Cauer network parameter set via the PSO-based thermal digital twin.

By repeating this cycle of evaluation and orientation of the particles, the particles move as a swarm through the search area of possible parameter combinations to find the optimal parameter set for the thermal model to represent the physical thermal behavior of the power semiconductor module. The search area is solely limited to appropriate values for a thermal model, which means no negative values for thermal resistances and capacitances. Further, the maximum parameter values are chosen depending on the application. This search for the optimal parameter set is one reason why Foster networks are not considered for the implementation in the thermal DTs in this work. The schematic representation of the search for optimal Foster network parameter sets - reduced to two dimensions - via the PSO-based thermal DT is presented in Fig. 4.19. For the Foster network, the sequence of the chain elements has no impact on the represented thermal behavior, therefore, multiple optimal parameter sets exist, which represent the exact same thermal behavior. The existence of multiple optimal parameter sets impedes the convergence of the particle swarm to an optimal parameter set. Contrary to this, the thermal behavior represented by a Cauer network depends on the sequence of the chain elements, therefore, only one optimal solution - the particle swarm searches for - exists (Fig. 4.20). This and the theoretical opportunity of accessing temperatures of intermediate material layers within the power semiconductor module are the reasons for the consideration of Cauer networks in this work.

The PSO-based thermal DT is implemented in an RTS executed on a Typhoon HIL402 system. In the RTS, the reference chip temperature T_{chip} is generated via a digital reference model, which has the same structure (Fig. 4.15) as used in the DT. This enables showing that the DT is able to converge to the same parameter set without previous knowledge about the parameters of the reference model.

The design of the PSO applied for the implementation of the thermal DT in the RTS is:

- The swarm consists of $B_{\text{PSO}} = 16$ particles.
- The weighting coefficient of the derivative part $c_{\text{PSO,d}}$ in the objective function (4.16)

is chosen as $0.1\,\mathrm{s}^2$.

- The inertia weight ω_{PSO} in the velocity calculation (4.17) is chosen as 0.7.
- The coefficient of the orientation towards the best neighbor particle $c_{\mathrm{PSO},1}$ in the velocity calculation (4.17) is chosen as 0.5.
- The coefficient of the orientation towards the best historical parameter set of the particle $c_{\mathrm{PSO},2}$ in the velocity calculation (4.17) is chosen as 0.5.
- The coefficient of the own vibration $c_{\mathrm{PSO},3}$ in the velocity calculation (4.17) is chosen as 0.01.

The time step of the electrical RTS d_{exe} is chosen as $10\,\mu\mathrm{s}$ and the time step of the thermal RTS d_{th} as $800\,\mu\mathrm{s}$. The input voltage of the buck converter is chosen as $400\,\mathrm{V}$, the switching frequency as $1\,\mathrm{kHz}$, the load resistor as $16\,\Omega$, and the inductor as $0.01\,\mathrm{H}$. The duty cycle of the buck converter is switched between 0.2 and 0.8, each value is applied alternating for $1\,\mathrm{s}$ - resulting in a square wave with $2\,\mathrm{s}$ period. The execution time step of the PSO d_{PSO} is set to $2\,\mathrm{s}$ in order to cover one induced thermal cycle with each evaluation of the particle performance by (4.16).

The convergence of the Cauer network parameters estimated by the PSO-based thermal DT

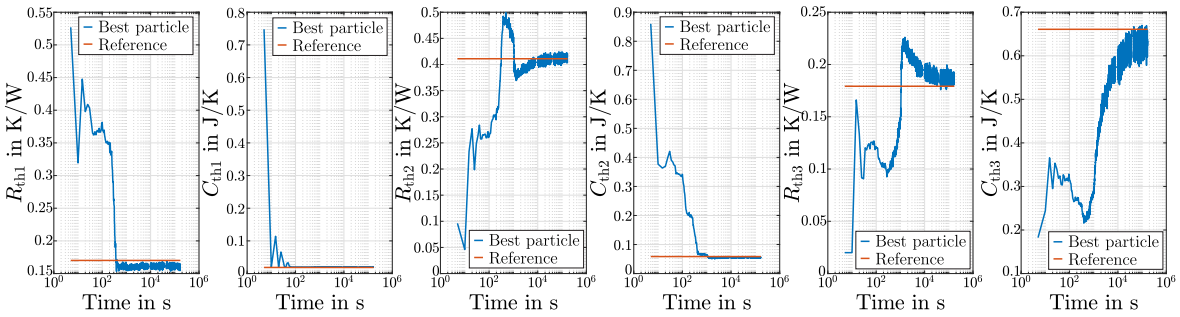


Fig. 4.21: Convergence of the Cauer network parameters to the reference values using the PSO-based thermal DT in the RTS.

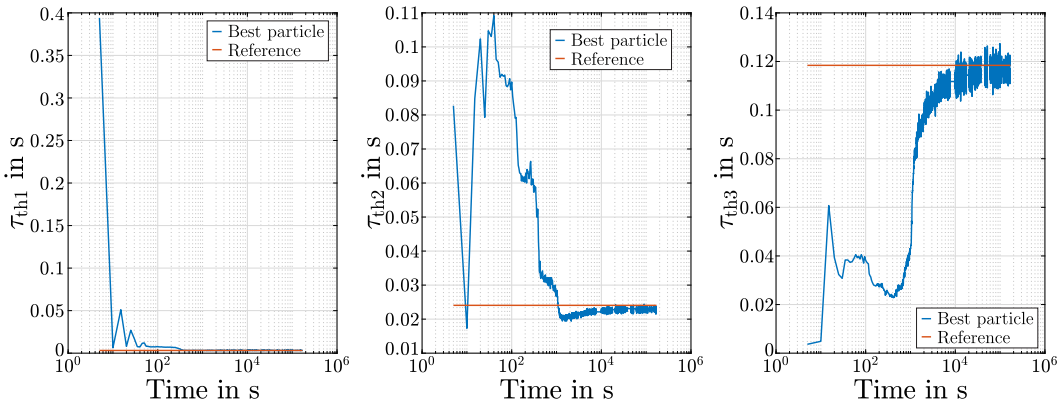


Fig. 4.22: Convergence of the time constants of the Cauer network chain elements using the PSO-based thermal DT in the RTS.

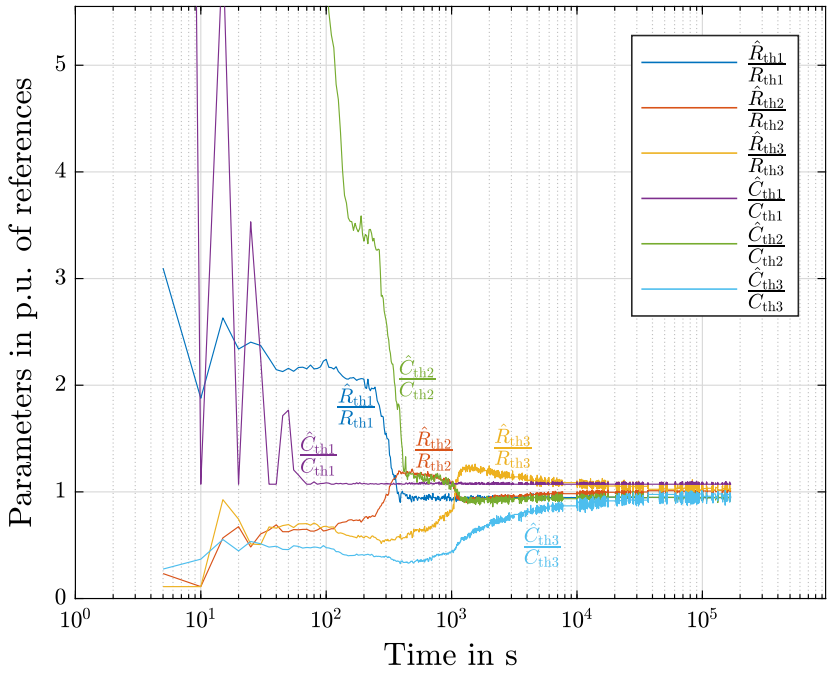


Fig. 4.23: Convergence of the Cauer network parameters in p.u. of their references using the PSO-based thermal DT in the RTS.

to the parameters of the digital reference model is shown in Fig. 4.21. The thermal time constants of the three chain elements, which are the multiplications of the thermal resistance and the thermal capacitance values of each chain element, are presented in Fig. 4.22. Another possibility to illustrate the convergence of the estimated parameters to the reference Cauer model parameters is to show the estimated parameters relative to the reference parameters, as given in Fig. 4.23. The PSO-based thermal DT is able to identify the parameter set of the reference Cauer model approximately, however, the inserted own vibration of the particles, which is necessary to avoid that the swarm gets stuck in local optima of the objective function, causes vibration around the reference values. It can be seen that the thermal parameters and thermal time constants of the chain elements closer to the chip converge faster. This is due to the fact that changing thermal parameters closer to the chip have a greater impact on the chip temperature. All parameters converged after approximately 50000 s to the reference values. With the PSO execution time of 2 s this results in approximately 25000 adaptions of the parameter sets until the convergence is reached.

The convergence of the estimated total thermal resistance, which is important for condition monitoring - as presented in Section 4.2 -, to the reference value is much faster than the convergence of all individual parameters, as shown in Fig. 4.24. The evolution of the minimum achieved objective function among all particles of the swarm is presented in Fig. 4.25. Comparing the convergence of the thermal time constants (Fig. 4.22) with the objective function evolution (Fig. 4.25) reveals that each time one of the thermal time constants of the chain elements converges towards the reference value the objective function also improves/drops.

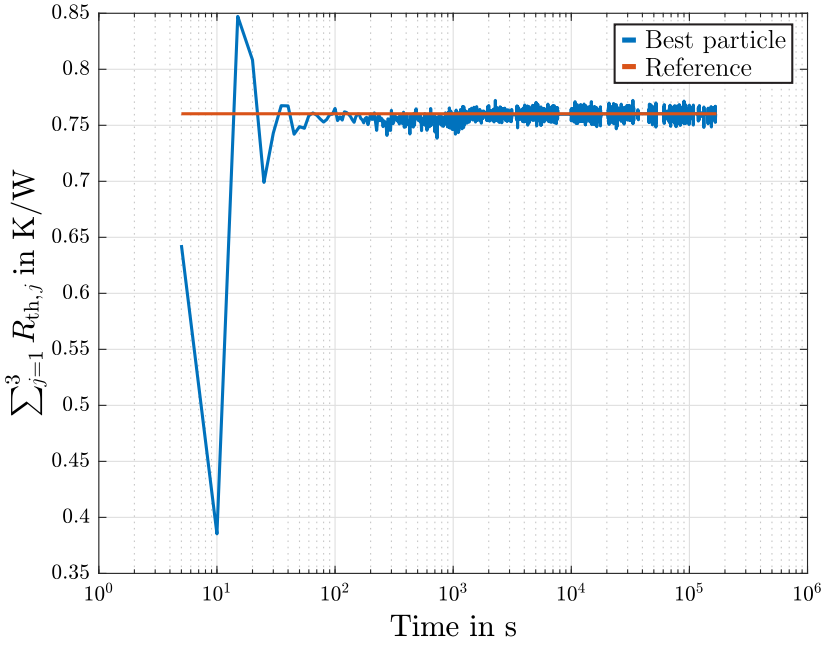


Fig. 4.24: Convergence of the total thermal resistance using the PSO-based thermal DT in the RTS.

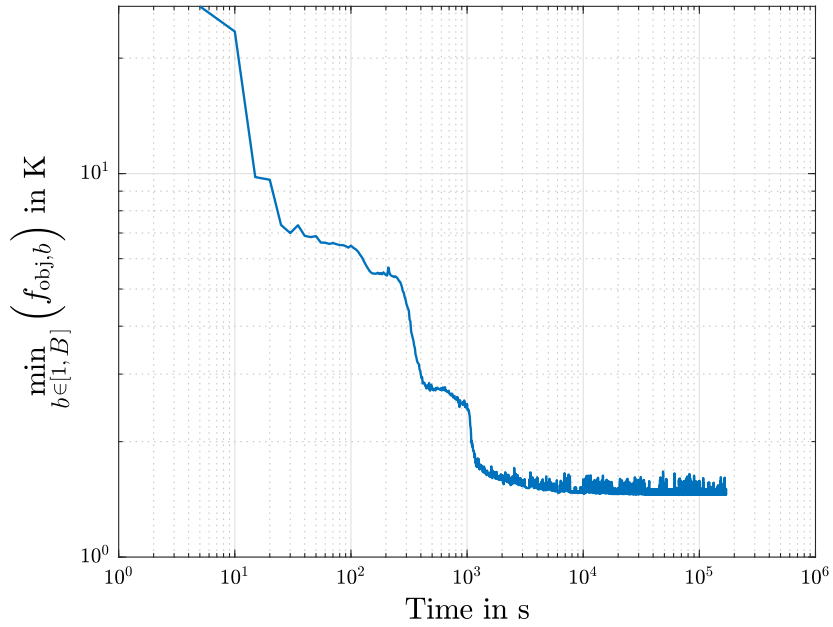


Fig. 4.25: Evolution of the minimum achieved objective function using the PSO-based thermal DT in the RTS.

4.3.3. Dual extended Kalman filter-based thermal digital twin

The realization of the thermal DT via the DEKF (Fig. 4.26) has the structure of an observer, which estimates the temperature states via input of the estimated power losses $\hat{P}_{\mathrm{loss}}$ and the measured ambient temperature T_{a} and corrects the temperature states and thermal model parameters based on a comparison of estimated $\hat{T}_{\mathrm{chip}}$ and measured chip temperature T_{chip}.

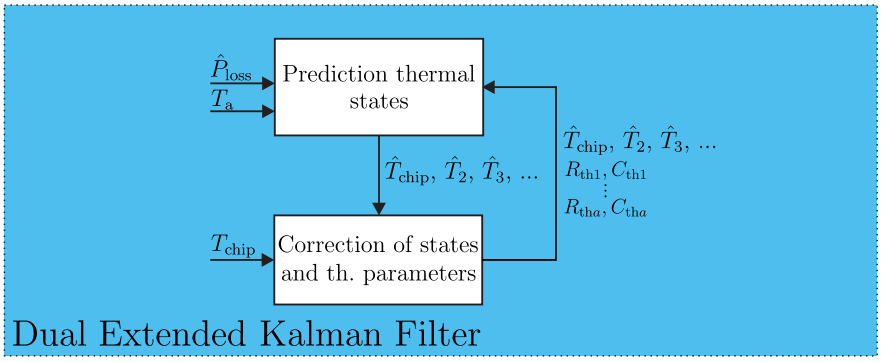


Fig. 4.26: Addition of the general scheme of a thermal digital twin of a power module for utilization of a dual extended Kalman filter.

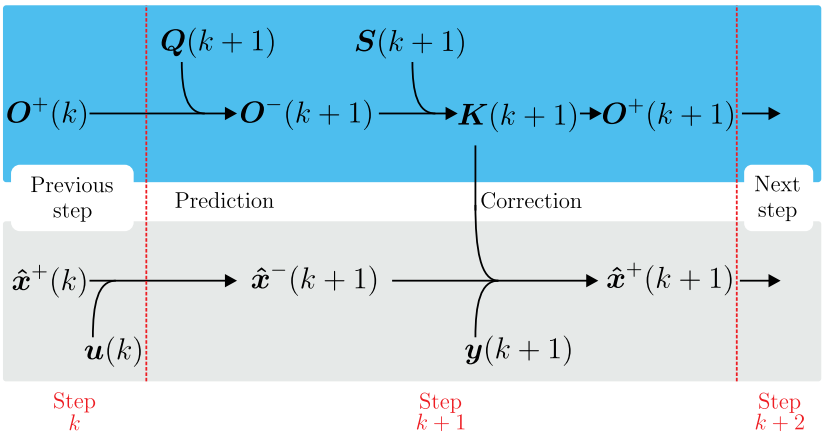


Fig. 4.27: General calculation scheme of a Kalman filter.

The general state equations of the assumed nonlinear system are given as

$$\begin{aligned} \boldsymbol{x}(k+1) &= \boldsymbol{f}(\boldsymbol{x}(k),\boldsymbol{u}(k)) + \boldsymbol{w}(k) \qquad \boldsymbol{x}_0 = \boldsymbol{x}(t_0) \\ \boldsymbol{y}(k) &= \boldsymbol{h}(\boldsymbol{x}(k)) + \boldsymbol{s}_{\text{meas}}(k) \end{aligned} \tag{4.19}$$

with process noise $\boldsymbol{w}(k) \sim \mathcal{N}(\boldsymbol{0},\boldsymbol{Q}(k))$ and measurement noise $\boldsymbol{s}_{\text{meas}}(k) \sim \mathcal{N}(\boldsymbol{0},\boldsymbol{S}(k))$ being white Gaussian noise with zero mean and covariance matrices $\boldsymbol{Q}(k)$ and $\boldsymbol{S}(k)$, respectively. The Kalman filter flow diagram is shown in Fig. 4.27, for each time instance $k+1$ the calculation consists of a prediction and a correction. The superscript indices $(-)$ and $(+)$ denote variables before and after the correction, respectively. Firstly, the predicted state estimation and the predicted covariance estimate are calculated for the upcoming step $k+1$ by

$$\hat{\boldsymbol{x}}^-(k+1) = \boldsymbol{f}(\hat{\boldsymbol{x}}^+(k),\boldsymbol{u}(k)) \tag{4.20}$$

$$\boldsymbol{O}^-(k+1) = \boldsymbol{F}(k)\boldsymbol{O}^+(k)(\boldsymbol{F}(k))^{\mathrm{T}} + \boldsymbol{Q}(k+1)\ . \tag{4.21}$$

Secondly, a correction is done, where first the Kalman gain $\boldsymbol{K}$ and afterwards corrected state and covariance state estimates are calculated from

$$\boldsymbol{K}(k+1) = \boldsymbol{O}^-(k+1)\boldsymbol{H}^{\mathrm{T}}(\boldsymbol{H}\boldsymbol{O}^-(k+1)\boldsymbol{H}^{\mathrm{T}} + \boldsymbol{S}(k+1))^{-1} \tag{4.22}$$

$$\hat{\boldsymbol{x}}^{+}(k+1) = \hat{\boldsymbol{x}}^{-}(k+1) + \boldsymbol{K}(k+1)(\boldsymbol{y}(k+1) - \boldsymbol{h}(\hat{\boldsymbol{x}}^{-}(k+1))) \tag{4.23}$$

$$\boldsymbol{O}^{+}(k+1) = (\boldsymbol{E} - \boldsymbol{K}(k+1)\boldsymbol{H})\boldsymbol{O}^{-}(k+1) \tag{4.24}$$

with the jacobian matrices

$$\boldsymbol{F}(k) = \left.\frac{\partial \boldsymbol{f}(\boldsymbol{x},\boldsymbol{u})}{\partial \boldsymbol{x}}\right|_{\hat{\boldsymbol{x}}(k),\boldsymbol{u}(k)} \qquad \boldsymbol{H}(k) = \left.\frac{\partial \boldsymbol{h}(\boldsymbol{x},\boldsymbol{u})}{\partial \boldsymbol{x}}\right|_{\hat{\boldsymbol{x}}(k)} \tag{4.25}$$

while the output matrix of the system $\boldsymbol{H}$ is constant, because the chip temperatures are extracted as outputs, which are given by state variables.

The single chip version of the DEKF-based thermal DT has the temperature states and parameters from Fig. 4.15 in vector

$$\hat{\boldsymbol{x}}(k) = [\hat{T}_{\text{chip}}(k)\ \hat{T}_2(k)\ \hat{T}_3(k)\ \hat{R}_{\text{th1}}(k)\ \hat{C}_{\text{th1}}(k)\ \hat{R}_{\text{th2}}(k)\ \hat{C}_{\text{th2}}(k)\ \hat{R}_{\text{th3}}(k)\ \hat{C}_{\text{th3}}(k)]^{\text{T}} \ . \tag{4.26}$$

The inputs are the power losses and the ambient temperature

$$\boldsymbol{u}(k) = [\hat{P}_{\text{loss}}(k)\ T_{\text{a}}(k)]^{\text{T}} \ . \tag{4.27}$$

The only output is the chip temperature

$$\hat{y}(k) = \hat{T}_{\text{chip}}(k) = [1\,0\,0\,0\,0\,0\,0\,0\,0]\,\hat{\boldsymbol{x}}(k) \ . \tag{4.28}$$

The jacobian matrix of the state equations from (4.25) is

$$\boldsymbol{F}(k) = \begin{bmatrix} \boldsymbol{F}_1(k) & \boldsymbol{F}_2(k) \\ \boldsymbol{0}_{6,3} & \boldsymbol{E}_{6,6} \end{bmatrix} \ . \tag{4.29}$$

Herein, $\boldsymbol{0}_{6,3}$ is a zero matrix with six rows and three columns, and $\boldsymbol{E}_{6,6}$ is the identity matrix with six rows and columns. Further, $\boldsymbol{F}_1(k)$ is a matrix with three rows and columns describing the partial derivatives of the temperature state equations from (4.7) by the temperature states

$$\boldsymbol{F}_1(k) = \begin{bmatrix} 1 - \frac{d_{\text{th}}}{\hat{R}_{\text{th1}}(k)\hat{C}_{\text{th1}}(k)} & \frac{d_{\text{th}}}{\hat{R}_{\text{th1}}(k)\hat{C}_{\text{th1}}(k)} & 0 \\ \frac{d_{\text{th}}}{\hat{R}_{\text{th1}}(k)\hat{C}_{\text{th2}}(k)} & 1 - \frac{d_{\text{th}}}{\hat{R}_{\text{th1}}(k)\hat{C}_{\text{th2}}(k)} - \frac{d_{\text{th}}}{\hat{R}_{\text{th2}}(k)\hat{C}_{\text{th2}}(k)} & \frac{d_{\text{th}}}{\hat{R}_{\text{th2}}(k)\hat{C}_{\text{th2}}(k)} \\ 0 & \frac{d_{\text{th}}}{\hat{R}_{\text{th2}}(k)\hat{C}_{\text{th3}}(k)} & 1 - \frac{d_{\text{th}}}{\hat{R}_{\text{th2}}(k)\hat{C}_{\text{th3}}(k)} - \frac{d_{\text{th}}}{\hat{R}_{\text{th3}}(k)\hat{C}_{\text{th3}}(k)} \end{bmatrix} \tag{4.30}$$

and $\boldsymbol{F}_2(k)$ is a matrix with three rows and six columns describing the partial derivatives of the temperature state equations from (4.7) by the predicted thermal parameters

$$\boldsymbol{F}_2(k) = \begin{bmatrix} \boldsymbol{F}_3(k) & \boldsymbol{F}_4(k) & \boldsymbol{F}_5(k) \end{bmatrix} \tag{4.31}$$

with

$$\boldsymbol{F}_3(k) = \begin{bmatrix} \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th1}}(k)}\left(\hat{T}_{\mathrm{chip}}(k) - \hat{T}_2(k)\right) & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th1}}(k)\hat{C}^2_{\mathrm{th1}}(k)}\left(\hat{T}_{\mathrm{chip}}(k) - \hat{T}_2(k) - \hat{R}_{\mathrm{th1}}(k)\hat{P}_{\mathrm{loss}}(k)\right) \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th2}}(k)}\left(\hat{T}_2(k) - \hat{T}_{\mathrm{chip}}(k)\right) & 0 \\ 0 & 0 \end{bmatrix}, \tag{4.32}$$

$$\boldsymbol{F}_4(k) = \begin{bmatrix} 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th2}}(k)}\left(\hat{T}_2(k) - \hat{T}_3(k)\right) & \frac{d_{\mathrm{th}}}{\hat{C}^2_{\mathrm{th2}}(k)}\left(\frac{\hat{T}_2(k)-\hat{T}_{\mathrm{chip}}(k)}{\hat{R}_{\mathrm{th1}}(k)} + \frac{\hat{T}_2(k)-\hat{T}_3(k)}{\hat{R}_{\mathrm{th2}}(k)}\right) \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th3}}(k)}\left(\hat{T}_3(k) - \hat{T}_2(k)\right) & 0 \end{bmatrix} \tag{4.33}$$

and

$$\boldsymbol{F}_5(k) = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th3}}(k)\hat{C}_{\mathrm{th3}}(k)}\left(\hat{T}_3(k) - T_{\mathrm{a}}(k)\right) & \frac{d_{\mathrm{th}}}{\hat{C}^2_{\mathrm{th3}}(k)}\left(\frac{\hat{T}_3(k)-\hat{T}_2(k)}{\hat{R}_{\mathrm{th2}}(k)} + \frac{\hat{T}_3(k)-T_{\mathrm{a}}(k)}{\hat{R}_{\mathrm{th3}}(k)}\right) \end{bmatrix}. \tag{4.34}$$

The entries of the covariance matrix of the process noise

$$\boldsymbol{Q} = \begin{bmatrix} Q_{\hat{T}_{\mathrm{chip}}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & Q_{\hat{T}_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & Q_{\hat{T}_3} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & Q_{\hat{R}_{\mathrm{th1}}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & Q_{\hat{C}_{\mathrm{th1}}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & Q_{\hat{R}_{\mathrm{th2}}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & Q_{\hat{C}_{\mathrm{th2}}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & Q_{\hat{R}_{\mathrm{th3}}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & Q_{\hat{C}_{\mathrm{th3}}} \end{bmatrix} \tag{4.35}$$

used in (4.21) and those of the covariance matrix of the measurement noise $\boldsymbol{S}$ used in (4.22), which is only the variable $S_{T_{\mathrm{chip}}}$ for the single chip thermal DT, are used as tuning parameters in this work.

The DEKF-based thermal DT is implemented in an RTS executed on a Typhoon HIL402 system. In the RTS, the reference chip temperature T_{chip} is generated via a digital reference model, which has the same structure (Fig. 4.15) as used in the DT. This enables showing that the DT is able to converge to the same parameter set without previous knowledge about the parameters of the reference model. The tuning parameters of the DEKF applied for the implementation of the thermal DT in the RTS are 10^{-10} for each of the entries in (4.35) and 10^{-4} for $S_{T_{\mathrm{chip}}}$. As for the implementation of the PSO-based thermal DT in the RTS, the time step of the electrical RTS d_{exe} is chosen as 10 µs and the time step of the thermal RTS d_{th} as 800 µs. The input voltage of the buck converter is chosen as 400 V, the switching frequency

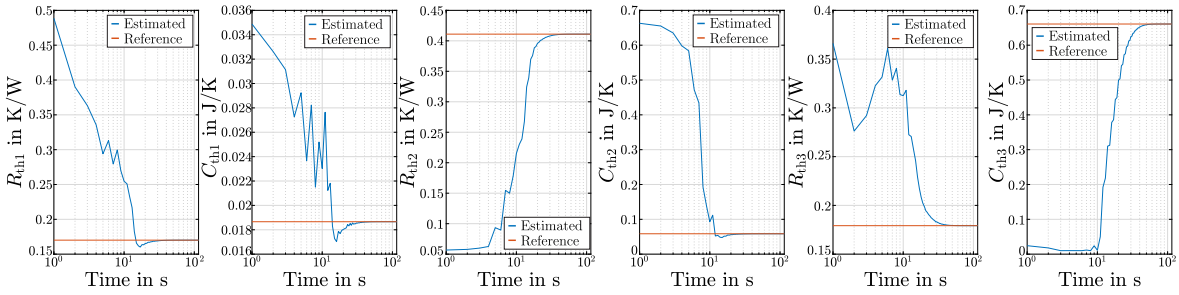


Fig. 4.28: Convergence of the Cauer network parameters to the reference values using the DEKF-based thermal DT in the RTS.

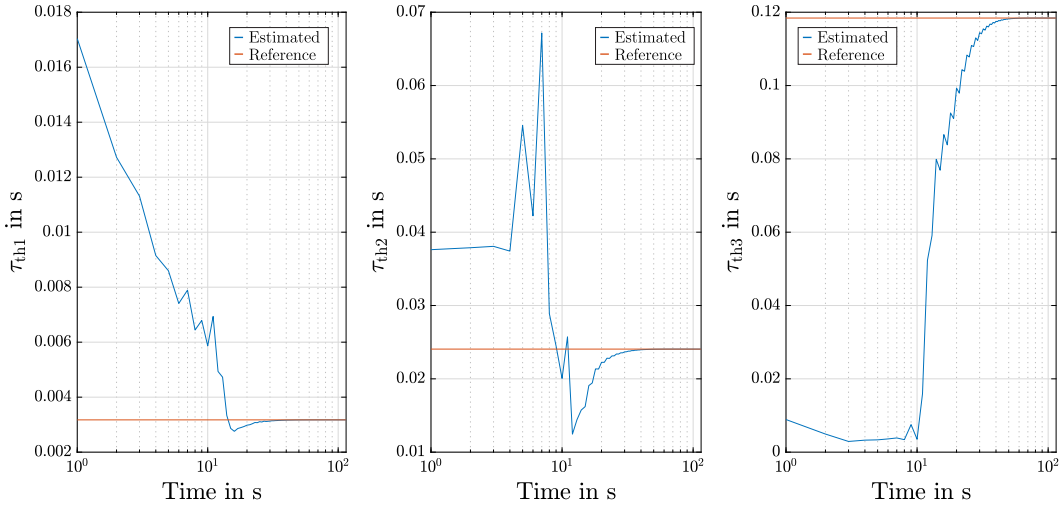


Fig. 4.29: Convergence of the time constants of the Cauer network chain elements using the DEKF-based thermal DT in the RTS.

as 1 kHz, the load resistor as 16 Ω, and the inductor as 0.01 H. The duty cycle of the buck converter is switched between 0.2 and 0.8, each value is applied alternating for 1 s - resulting in a square wave with 2 s period. The prediction and correction of the DEKF-based thermal DT is executed in each step of the thermal RTS $d_{\text{th}} = 800\,\mu\text{s}$.

The convergence of the Cauer network parameters estimated by the DEKF-based thermal DT to the parameters of the digital reference model is shown in Fig. 4.28. The thermal time constants of the three chain elements, which are the multiplications of the thermal resistance and the thermal capacitance values of each chain element, are presented in Fig. 4.29. Another possibility to illustrate the convergence of the estimated parameters to the reference Cauer model parameters is to show the estimated parameters relative to the reference parameters, as given in Fig. 4.30. The DEKF-based thermal DT is able to identify the parameter set of the reference Cauer model. It can be seen that the parameters and time constants of the two chain elements closer to the chip converge to the reference values first and afterwards those of the third Cauer network chain element. All parameters converged after approximately 50 s to the reference values. With the DEKF execution time of 800 µs this results in approximately 62500 cycles of prediction and correction until the convergence is reached.

The convergence of the estimated total thermal resistance, which is important for condition

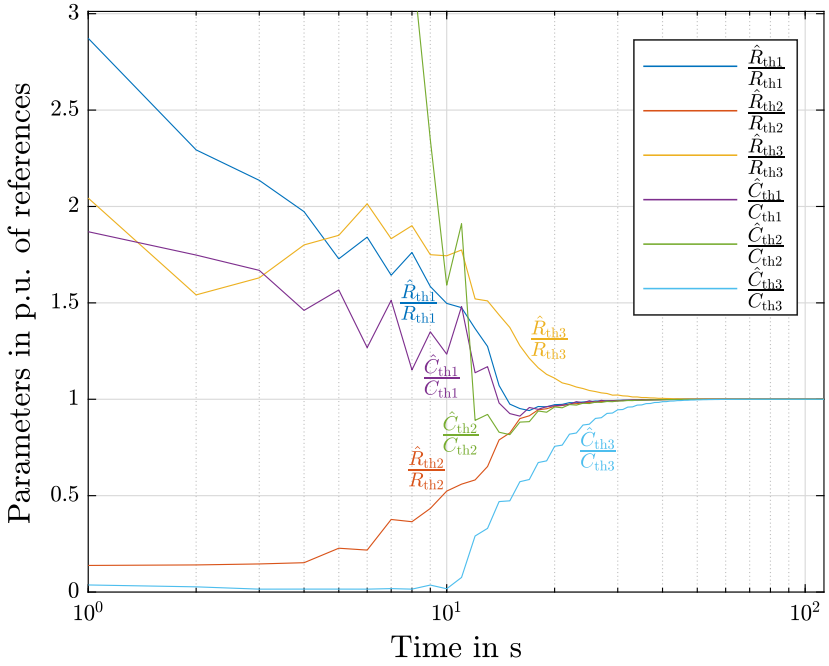


Fig. 4.30: Convergence of the Cauer network parameters in p.u. of their references using the DEKF-based thermal DT in the RTS.

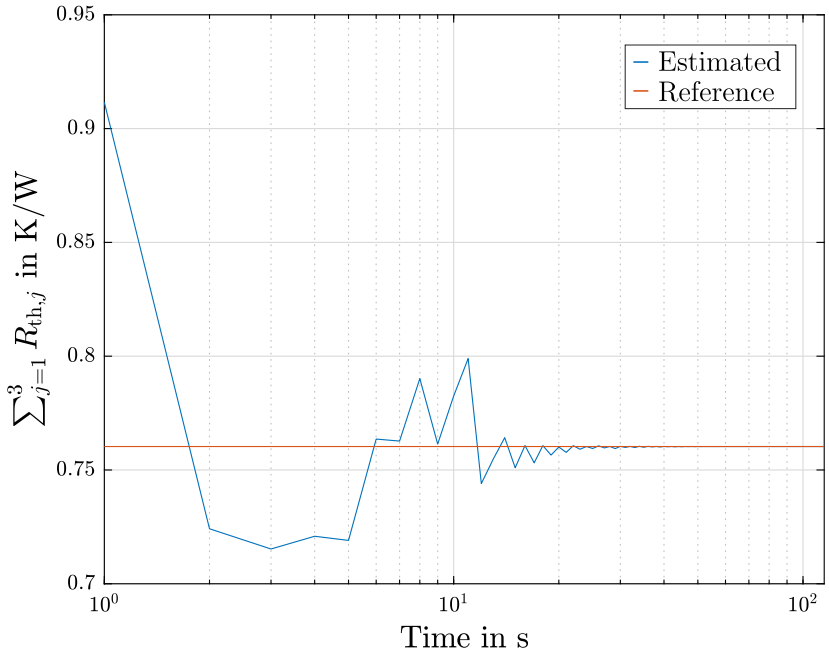


Fig. 4.31: Convergence of the total thermal resistance using the DEKF-based thermal DT in the RTS.

monitoring - as presented in Section 4.2 -, to the reference value is shown in Fig. 4.31.

4.3.4. Comparison of the thermal digital twin approaches

The comparison of PSO- and DEKF-based thermal DTs is done concerning five criteria:

- the computational burden of the DT approaches,

- the time required for convergence of the estimated thermal model parameters to the reference ones,
- the optimizer coefficient tuning range that enables convergence of the estimated thermal model parameters to the reference ones,
- the robustness of the convergence of the estimated thermal model parameters to the reference ones against input profile variations,
- the potential of applying an asynchronous execution of the optimization.

The computational burden of the DT approaches is assessed by the number of mathematical operations that need to be carried out for the basic equations of the approaches each second. The computational burden is especially important for the integration of the approaches in real-time applications, as it defines, if the computations at given simulation time step can be finished before the next time step starts to meet the real-time requirement.

The time required for convergence of the estimated thermal model parameters to the reference ones is evaluated based on the results of the RTS implementation of the thermal DT approaches. The time required for the convergence from a randomly initialized thermal model parameter set - no previous information about the thermal behavior needed - to the reference parameters (convergence speed) plays only a role at the start (initialization phase) for the implementation in a long term thermal observation. However, a high convergence speed of the thermal DT approach facilitates the research and development with the thermal DT approach.

The optimizer coefficient tuning range that enables convergence of the estimated thermal model parameters to the reference ones is evaluated by varying the single coefficients individually from the basis coefficient configurations presented before. A wider range of possible optimizer coefficient tunings makes it easier to find a coefficient configuration that allows convergence of the estimated thermal model parameters to the reference ones and makes this coefficient configuration more robust against deviations of the real thermal behavior compared with the thermal behavior considered during the design.

The robustness of the convergence of the estimated thermal model parameters to the reference ones against input profile variations is investigated by applying different duty cycle profiles to the buck converter during the thermal parameter identification. If the identification of thermal parameters is robust against input profile variations, applying the thermal DT approach does not require one specific characterization operation cycle.

The asynchronous execution of the optimization mentioned in the fifth criterion refers to changing the execution time step of the PSO or the DEKF correction relative to the RTS time steps compared to the implementations of PSO- and DEKF-based thermal DT presented before. The potential of applying such an asynchronous execution of the optimization

algorithms is evaluated theoretically by discussing the influences it could have on the other criteria.

Computational burden of the DT approaches

The number of mathematical operations that need to be carried out for the basic equations of the PSO-based thermal DT each second is calculated by

$$\begin{aligned}\frac{N_{\mathrm{op,PSO}}}{\mathrm{s}} = &\frac{1}{d_{\mathrm{th}}}\Bigg(\underbrace{B_{\mathrm{PSO}}N_{\boldsymbol{y}}\Big(\underbrace{3+(N_{\mathrm{cauer}}-1)4}_{\text{Summations}}+\underbrace{N_{\mathrm{cauer}}}_{\text{Multiplications}}+\underbrace{2+(N_{\mathrm{cauer}}-1)3}_{\text{Divisions}}\Big)}_{\text{Thermal RTSs based on (4.7)}}\\ &+\underbrace{\underbrace{B_{\mathrm{PSO}}N_{\boldsymbol{y}}4}_{\text{Summations}}+\underbrace{B_{\mathrm{PSO}}N_{\boldsymbol{y}}3}_{\text{Multiplications}}+\underbrace{B_{\mathrm{PSO}}}_{\text{Square root}}}_{\text{Operations (4.16)}}\Bigg)+\frac{1}{d_{\mathrm{PSO}}}\Bigg(\underbrace{\underbrace{B_{\mathrm{PSO}}}_{\text{Multiplications}}}_{\text{Operations (4.16)}}\\ &+\underbrace{\underbrace{B_{\mathrm{PSO}}2}_{\substack{\text{relational}\\ \text{operations}}}}_{\text{Compare } f_{\mathrm{obj}}}+\underbrace{\underbrace{B_{\mathrm{PSO}}N_{\boldsymbol{y}}(2N_{\mathrm{cauer}})5}_{\text{Summations}}+\underbrace{B_{\mathrm{PSO}}N_{\boldsymbol{y}}(2N_{\mathrm{cauer}})7}_{\text{Multiplications}}}_{\text{Operations (4.17)}}\\ &+\underbrace{\underbrace{B_{\mathrm{PSO}}N_{\boldsymbol{y}}(2N_{\mathrm{cauer}})}_{\text{Summations}}}_{\text{Operations (4.18)}}\Bigg)\ .\end{aligned} \tag{4.36}$$

Herein, d_{th} is the thermal RTS time step, B_{PSO} is the number of particles in the PSO, $N_{\boldsymbol{y}}$ is the number of chip temperature measurements on the physical system used in the thermal DT approaches, N_{cauer} is the number of chain elements of the Cauer network, and d_{PSO} is the PSO execution time step. For (4.36) as well as for the following equations for the DEKF-based thermal DT, it is assumed that $N_{\boldsymbol{y}}$ thermal Cauer networks with each having N_{cauer} chain elements are considered, which cannot be split into multiple applications of the approaches for each temperature measurement individually.

The number of mathematical operations that need to be carried out for the basic equations of the DEKF-based thermal DT each second is calculated by

$$\begin{aligned}\frac{N_{\mathrm{op,DEKF}}}{\mathrm{s}} = &\underbrace{\frac{N_{\mathrm{op,DEKF,1}}}{\mathrm{s}}}_{\substack{\text{Operations (4.20)}\\ \text{based on (4.7)}}}+\underbrace{\frac{N_{\mathrm{op,DEKF,2}}}{\mathrm{s}}}_{\text{Operations (4.21)}}+\underbrace{\frac{N_{\mathrm{op,DEKF,3}}}{\mathrm{s}}}_{\text{Operations (4.22)}}\\ &+\underbrace{\frac{N_{\mathrm{op,DEKF,4}}}{\mathrm{s}}}_{\text{Operations (4.23)}}+\underbrace{\frac{N_{\mathrm{op,DEKF,5}}}{\mathrm{s}}}_{\text{Operations (4.24)}}+\underbrace{\frac{N_{\mathrm{op,DEKF,6}}}{\mathrm{s}}}_{\substack{\text{Operations}\\ \text{update (4.25)}}},\end{aligned} \tag{4.37}$$

which contains

$$\frac{N_{\text{op,DEKF,1}}}{\text{s}} = \frac{1}{d_{\text{th}}} N_{\boldsymbol{y}} \Big(\underbrace{3+(N_{\text{cauer}}-1)4}_{\text{Summations}} + \underbrace{N_{\text{cauer}}}_{\text{Multiplications}} + \underbrace{2+(N_{\text{cauer}}-1)3}_{\text{Divisions}} \Big) \ , \tag{4.38}$$

$$\frac{N_{\text{op,DEKF,2}}}{\text{s}} = \frac{1}{d_{\text{th}}} \Bigg(\underbrace{\underbrace{2}_{\substack{\text{Number}\\ \text{matrix}\\ \text{multipli.}}} \underbrace{N_{\hat{\boldsymbol{x}}}^2}_{\substack{\text{Matrix}\\ \text{positions}}} \underbrace{N_{\hat{\boldsymbol{x}}}}_{\substack{\text{Multipli.}\\ \text{calculation}\\ \text{each position}}}}_{\text{Multiplications}} + \underbrace{\underbrace{2}_{\substack{\text{Number}\\ \text{matrix}\\ \text{multipli.}}} \underbrace{N_{\hat{\boldsymbol{x}}}^2}_{\substack{\text{Matrix}\\ \text{positions}}} \underbrace{(N_{\hat{\boldsymbol{x}}}-1)}_{\substack{\text{Summations}\\ \text{calculation}\\ \text{each position}}} + \underbrace{N_{\hat{\boldsymbol{x}}}}_{\substack{\text{Summations}\\ \boldsymbol{Q}\text{ matrix}}}}_{\text{Summations}} \Bigg) \ , \tag{4.39}$$

$$\begin{aligned} \frac{N_{\text{op,DEKF,3}}}{\text{s}} = \frac{1}{d_{\text{th}}} \Bigg(& \underbrace{\underbrace{N_{\hat{\boldsymbol{x}}} N_{\boldsymbol{y}}}_{\substack{\text{Matrix}\\ \text{positions}}} \underbrace{N_{\boldsymbol{y}}}_{\substack{\text{Multipli.}\\ \text{calculation}\\ \text{each position}}} + \underbrace{N_{\boldsymbol{y}}^2 \left(\left(\sum_{a=1}^{N_{\boldsymbol{y}}-1} \frac{(N_{\boldsymbol{y}}-1)!}{a!} \right) - 1 \right)}_{\substack{\text{Calculation}\\ \text{adjoint matrix}}}}_{\text{Multiplications}} \\ & + \underbrace{\underbrace{\left(\sum_{a=1}^{N_{\boldsymbol{y}}} \frac{(N_{\boldsymbol{y}})!}{a!} \right) - 1}_{\substack{\text{Calculation}\\ \text{determinant}}} + \underbrace{N_{\boldsymbol{y}}^2}_{\substack{\text{Multipli.}\\ \text{inverse determinant}\\ \text{adjoint matrix}}}}_{\text{Multiplications}} + \underbrace{\underbrace{1}_{\substack{\text{Calculation}\\ \text{inverse}\\ \text{determinant}}}}_{\text{Divisions}} \\ & + \underbrace{\underbrace{N_{\hat{\boldsymbol{x}}} N_{\boldsymbol{y}}}_{\substack{\text{Matrix}\\ \text{positions}}} \underbrace{(N_{\boldsymbol{y}}-1)}_{\substack{\text{Summations}\\ \text{calculation}\\ \text{each position}}} + \underbrace{N_{\boldsymbol{y}}^2 \left(\sum_{a=1}^{N_{\boldsymbol{y}}-1} \frac{(N_{\boldsymbol{y}}-1)!(a-1)}{a!} \right)}_{\substack{\text{Calculation}\\ \text{adjoint matrix}}}}_{\text{Summations}} \\ & + \underbrace{\underbrace{\left(\sum_{a=1}^{N_{\boldsymbol{y}}} \frac{(N_{\boldsymbol{y}})!(a-1)}{a!} \right)}_{\substack{\text{Calculation}\\ \text{determinant}}} + \underbrace{N_{\boldsymbol{y}}}_{\substack{\text{Summations}\\ \boldsymbol{S}\text{ matrix}}}}_{\text{Summations}} \Bigg) \ , \end{aligned} \tag{4.40}$$

$$\frac{N_{\text{op,DEKF,4}}}{\text{s}} = \frac{1}{d_{\text{th}}} \Bigg(\underbrace{\underbrace{N_{\hat{\boldsymbol{x}}}}_{\substack{\text{Vector}\\ \text{positions}}} \underbrace{N_{\boldsymbol{y}}}_{\substack{\text{Multipli.}\\ \text{calculation}\\ \text{each position}}}}_{\text{Multiplications}} + \underbrace{\underbrace{N_{\hat{\boldsymbol{x}}}}_{\substack{\text{Vector}\\ \text{positions}}} \underbrace{(N_{\boldsymbol{y}}-1)}_{\substack{\text{Summations}\\ \text{calculation}\\ \text{each position}}} + \underbrace{N_{\hat{\boldsymbol{x}}}}_{\substack{\text{Sum.}\\ \hat{\boldsymbol{x}}^-}} + \underbrace{N_{\boldsymbol{y}}}_{\substack{\text{Comparison}\\ \text{measured to}\\ \text{estimated outputs}}}}_{\text{Summations}} \Bigg) \ , \tag{4.41}$$

$$\frac{N_{\mathrm{op,DEKF,5}}}{\mathrm{s}} = \frac{1}{d_{\mathrm{th}}}\Bigg(\underbrace{\underbrace{N_{\hat{\boldsymbol{x}}}^2}_{\substack{\text{Matrix}\\\text{positions}}}\ \underbrace{N_{\boldsymbol{y}}}_{\substack{\text{Multipli.}\\\text{calculation}\\\text{each position}}} + \underbrace{N_{\hat{\boldsymbol{x}}}^2}_{\substack{\text{Matrix}\\\text{positions}}}\ \underbrace{N_{\hat{\boldsymbol{x}}}}_{\substack{\text{Multipli.}\\\text{calculation}\\\text{each position}}}}_{\text{Multiplications}} + \underbrace{\underbrace{N_{\hat{\boldsymbol{x}}}^2}_{\substack{\text{Matrix}\\\text{positions}}}\ \underbrace{(N_{\boldsymbol{y}}-1)}_{\substack{\text{Summations}\\\text{calculation}\\\text{each position}}} + \underbrace{N_{\hat{\boldsymbol{x}}}^2}_{\substack{\text{Matrix}\\\text{positions}}}\ \underbrace{(N_{\hat{\boldsymbol{x}}}-1)}_{\substack{\text{Summations}\\\text{calculation}\\\text{each position}}} + \underbrace{N_{\hat{\boldsymbol{x}}}}_{\substack{\text{Summation}\\\text{identity}\\\text{matrix}}}}_{\text{Summations}} \Bigg) , \tag{4.42}$$

and

$$\frac{N_{\mathrm{op,DEKF,6}}}{\mathrm{s}} = \frac{1}{d_{\mathrm{th}}}\Bigg(\underbrace{\underbrace{N_{\boldsymbol{y}}+N_{\boldsymbol{y}}(N_{\mathrm{cauer}}-1)4}_{\text{Multiplications}} + \underbrace{N_{\boldsymbol{y}}+N_{\boldsymbol{y}}(N_{\mathrm{cauer}}-1)4}_{\text{Divisions}} + \underbrace{N_{\boldsymbol{y}}+N_{\boldsymbol{y}}(N_{\mathrm{cauer}}-1)2}_{\text{Summations}}}_{\text{Update (4.30)}} + \underbrace{\underbrace{N_{\boldsymbol{y}}+N_{\boldsymbol{y}}(N_{\mathrm{cauer}}-1)8}_{\text{Multiplications}} + \underbrace{N_{\boldsymbol{y}}+N_{\boldsymbol{y}}(N_{\mathrm{cauer}}-1)5}_{\text{Divisions}} + \underbrace{N_{\boldsymbol{y}}+N_{\boldsymbol{y}}(N_{\mathrm{cauer}}-1)5}_{\text{Summations}}}_{\text{Update (4.31)}} \Bigg) . \tag{4.43}$$

Herein, $N_{\hat{\boldsymbol{x}}}$ is the number of states and estimated parameters within the DEKF, which is equal to $N_{\boldsymbol{y}}(3N_{\mathrm{cauer}})$ for the assumptions previously made. The number of mathematical operations per second of (4.22) is given by (4.40), if $N_{\boldsymbol{y}} \geq 2$. If $N_{\boldsymbol{y}} = 1$, one summation, one division and $N_{\hat{\boldsymbol{x}}}$ multiplications are carried out at each thermal RTS time step d_{th}. Furthermore, multiplications with -1 are excluded due to their low computational effort.

The required mathematical operations per second for execution of the PSO-based thermal DT depending on N_{cauer} and $N_{\boldsymbol{y}}$ for $B_{\mathrm{PSO}} = 16$ ($d_{\mathrm{th}} = 800\,\mu\mathrm{s}$ and $d_{\mathrm{PSO}} = 2\,\mathrm{s}$) are shown in

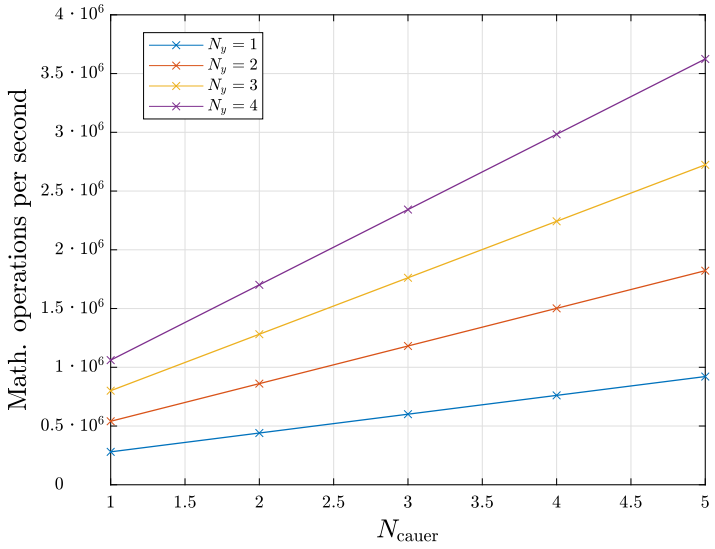


Fig. 4.32: Required mathematical operations per second for execution of the PSO-based thermal DT depending on N_{cauer} and $N_{\boldsymbol{y}}$ for $B_{\mathrm{PSO}} = 16$.

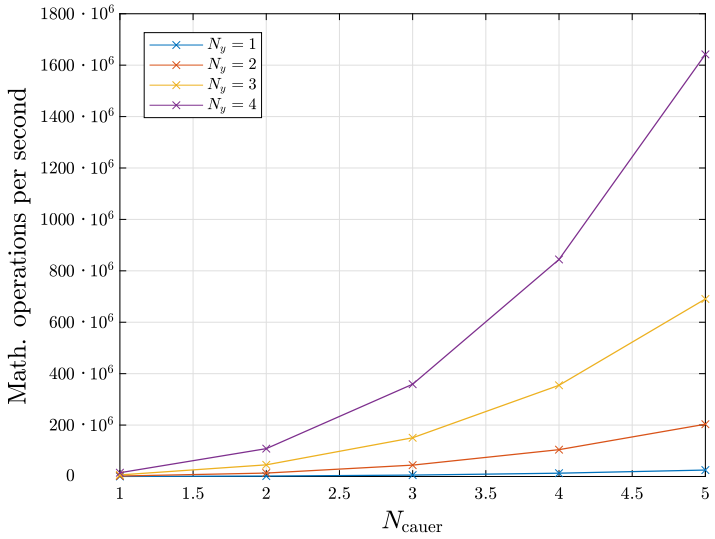


Fig. 4.33: Required mathematical operations per second for execution of the DEKF-based thermal DT depending on N_{cauer} and $N_{\boldsymbol{y}}$.

Fig. 4.32. The computational burden increases linearly with more chain elements (increasing N_{cauer}) and also with more temperature measurements (increasing $N_{\boldsymbol{y}}$).

The required mathematical operations per second for execution of the DEKF-based thermal DT depending on N_{cauer} and $N_{\boldsymbol{y}}$ are shown in Fig. 4.33. The computational burden increases quadratically with more chain elements (increasing N_{cauer}) and also with more temperature measurements (increasing $N_{\boldsymbol{y}}$). However, when a specific configuration is chosen for implementation, there is the possibility to decrease the computational burden by excluding operations with zero entries from equations containing (4.29).

Convergence speed of the DT approaches

The time required for convergence of the estimated thermal model parameters to the reference ones is evaluated based on the results of the RTS implementation of the thermal DT approaches. For the DEKF-based thermal DT, all thermal parameters converged after approximately 50 s to the reference values. With the DEKF execution time of 800 µs this results in approximately 62500 cycles of prediction and correction until the convergence is reached.

Whereas, for the PSO-based thermal DT, all thermal parameters converged after approximately 50000 s to the reference values. With the PSO execution time of $d_{\mathrm{PSO}} = 2\,\mathrm{s}$ this results in approximately 25000 adaptions of the parameter sets until the convergence is reached.

Optimizer tuning of the DT approaches

The optimizer coefficient tuning range that enables convergence of the estimated thermal model parameters to the reference ones is evaluated by varying the single coefficients in-

dividually from the basis coefficient configurations presented before. The thermal DT approaches with adjusted coefficient configurations are executed for ten minutes in the RTS with digital reference model. After ten minutes run time the performance of the coefficient configuration is evaluated using the objective function

$$f_{\mathrm{obj,ref},b} = \frac{d_{\mathrm{th}}}{d_{\mathrm{PSO}}} \left(\sum_{k=1}^{\frac{d_{\mathrm{PSO}}}{d_{\mathrm{th}}}} \sqrt{\left(\hat{T}_{\mathrm{chip},b}(k) - T_{\mathrm{chip}}(k) \right)^2} \right) \quad \forall b \in [1, B_{\mathrm{PSO}}] \ . \tag{4.44}$$

This objective function is not only applied to the estimated temperatures of the PSO particles, but also to the estimated temperature of the DEKF.

The basis coefficient configuration of the PSO-based thermal DT from which the single coefficients are varied individually is: $\omega_{\mathrm{PSO}} = 0.7$, $c_{\mathrm{PSO},1} = 0.5$, $c_{\mathrm{PSO},2} = 0.5$, $c_{\mathrm{PSO},3} = 0.01$, and $c_{\mathrm{PSO,d}} = 0.1\,\mathrm{s}^2$. The results of the PSO-based thermal DT for varying only ω_{PSO} are shown in Table 4.3, those for varying only $c_{\mathrm{PSO},1}$ are shown in Table 4.4, those for varying only $c_{\mathrm{PSO},2}$ are shown in Table 4.5, those for varying only $c_{\mathrm{PSO},3}$ are shown in Table 4.6, and those for varying only $c_{\mathrm{PSO,d}}$ are shown in Table 4.7.

Choosing low values for the PSO inertia ω_{PSO} impedes the convergence of the objective function (4.44) significantly (Table 4.3), because a low inertia will result in low velocity of

Table 4.3: Sensitivity of PSO-based thermal DT convergence to ω_{PSO} tuning.

ω_{PSO}	0.1	0.3	0.5	0.7	0.9
$\min_{b\in[1,B_{\mathrm{PSO}}]} \left(f_{\mathrm{obj,ref},b} \right)$ in K	10.97	5.84	0.33	0.33	0.41

Table 4.4: Sensitivity of PSO-based thermal DT convergence to $c_{\mathrm{PSO},1}$ tuning.

$c_{\mathrm{PSO},1}$	0.1	0.3	0.5	0.7	0.9
$\min_{b\in[1,B_{\mathrm{PSO}}]} \left(f_{\mathrm{obj,ref},b} \right)$ in K	6.65	2.43	0.33	0.24	0.31

Table 4.5: Sensitivity of PSO-based thermal DT convergence to $c_{\mathrm{PSO},2}$ tuning.

$c_{\mathrm{PSO},2}$	0.1	0.3	0.5	0.7	0.9
$\min_{b\in[1,B_{\mathrm{PSO}}]} \left(f_{\mathrm{obj,ref},b} \right)$ in K	0.44	0.43	0.33	0.23	0.42

Table 4.6: Sensitivity of PSO-based thermal DT convergence to $c_{\mathrm{PSO},3}$ tuning.

$c_{\mathrm{PSO},3}$	0.001	0.005	0.01	0.05	0.1
$\min_{b\in[1,B_{\mathrm{PSO}}]} \left(f_{\mathrm{obj,ref},b} \right)$ in K	1.12	0.19	0.33	0.36	1.17

Table 4.7: Sensitivity of PSO-based thermal DT convergence to $c_{\mathrm{PSO,d}}$ tuning.

$c_{\mathrm{PSO,d}}$ in s^2	0	0.01	0.05	0.1	0.5	1
$\min_{b\in[1,B_{\mathrm{PSO}}]}\left(f_{\mathrm{obj,ref},b}\right)$ in K	0.04	0.27	0.35	0.33	0.74	0.67

the particle parameters and, therefore, the search area in the given time is shrunk. Also low values for $c_{\mathrm{PSO,1}}$ impede the convergence significantly (Table 4.4), because a low orientation on the other particles leads to longer convergence times of the swarm. The orientation towards the best historical parameter set of the particle $c_{\mathrm{PSO,2}}$ has only minor influence on the convergence (Table 4.5). Low and high values for the own vibration of the particles $c_{\mathrm{PSO,3}}$ impede the convergence (Table 4.6). For low values of $c_{\mathrm{PSO,3}}$, the particle swarm gets stuck in local optima of the objective function (4.16). For high values of $c_{\mathrm{PSO,3}}$, the own vibration impedes the convergence to precise thermal parameters. In the time frame of ten minutes, which was chosen to have a reasonable testing time, the weighting coefficient of the derivative part $c_{\mathrm{PSO,d}}$ in the objective function (4.16) impedes the convergence of the comparison objective function (4.44). However, for longer test times up to 50 hours, it was observed that a convergence to the digital reference thermal model parameters, as shown in Fig. 4.22, is only possible with $c_{\mathrm{PSO,d}}$.

The basis coefficient configuration of the DEKF-based thermal DT from which the single coefficients are varied individually is: $S_{T_{\mathrm{chip}}} = 0.0001$, and $Q_{\hat{T}_{\mathrm{chip}}} = Q_{\hat{T}_2} = Q_{\hat{T}_3} = Q_{\hat{R}_{\mathrm{th1}}} = Q_{\hat{C}_{\mathrm{th1}}} = Q_{\hat{R}_{\mathrm{th2}}} = Q_{\hat{C}_{\mathrm{th2}}} = Q_{\hat{R}_{\mathrm{th3}}} = Q_{\hat{C}_{\mathrm{th3}}} = 10^{-10}$. The results of the DEKF-based thermal DT for varying only $S_{T_{\mathrm{chip}}}$ are shown in Table 4.8 and those for varying the entries of $\boldsymbol{Q}$ individually are shown in Table 4.9. High values of $S_{T_{\mathrm{chip}}}$ impede the convergence of the thermal parameters estimated by the DEKF-based thermal DT to the digital reference thermal model parameters. For varying the values of $\boldsymbol{Q}$, low values for $Q_{\hat{C}_{\mathrm{th2}}}$, high values for $Q_{\hat{R}_{\mathrm{th3}}}$, and low and high values for $Q_{\hat{C}_{\mathrm{th3}}}$ impede the convergence. It can be seen that the coefficient tuning for the process noise covariance matrix entries of capacitive thermal parameters further away

Table 4.8: Sensitivity of DEKF-based thermal DT convergence to $S_{T_{\mathrm{chip}}}$ variation.

$S_{T_{\mathrm{chip}}}$	0.000001	0.0001	0.000576	0.000625	0.01	1
$f_{\mathrm{obj,ref}}$ in K	0.00	0.00	0.00	0.41	0.43	1.72

Table 4.9: Sensitivity of DEKF-based thermal DT convergence ($f_{\mathrm{obj,ref}}$ in K) to $\boldsymbol{Q}$ tuning.

	$Q_{\hat{T}_{\mathrm{chip}}}$	$Q_{\hat{T}_2}$	$Q_{\hat{T}_3}$	$Q_{\hat{R}_{\mathrm{th1}}}$	$Q_{\hat{C}_{\mathrm{th1}}}$	$Q_{\hat{R}_{\mathrm{th2}}}$	$Q_{\hat{C}_{\mathrm{th2}}}$	$Q_{\hat{R}_{\mathrm{th3}}}$	$Q_{\hat{C}_{\mathrm{th3}}}$
10^{-13}	0.00	0.00	0.00	0.00	0.00	0.00	0.57	0.00	0.67
10^{-10}	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
10^{-7}	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.09	0.49

from the chip is critical, because they have less impact on the chip temperature than the other thermal parameters and are, therefore, more difficult to identify.

Input profile robustness of the DT approaches

The robustness of the convergence of the estimated thermal model parameters to the reference ones against input profile variations is investigated by applying different duty cycle profiles (Fig. 4.34) to the buck converter during the thermal parameter identification.

The influence of the duty cycle input profiles is evaluated using the objective function (4.44) after ten minutes run time of the RTS implementation of the thermal DT approaches. The basis coefficient configurations of the thermal DT approaches presented for the optimizer tuning are used. The PSO-based thermal DT converges only for having a large periodic cycle at the input (Table 4.10), whereas the DEKF-based thermal DT is able to converge for each of the considered duty cycle input profiles (Table 4.11). Therefore, it would be necessary to operate a specific characterization profile during the convergence of the PSO-based thermal DT.

Potential asynchronous execution of the DT approaches

The asynchronous execution of the optimization refers to changing the execution time step of the PSO or the DEKF correction relative to the RTS time steps compared to the implementations of PSO- and DEKF-based thermal DT presented before.

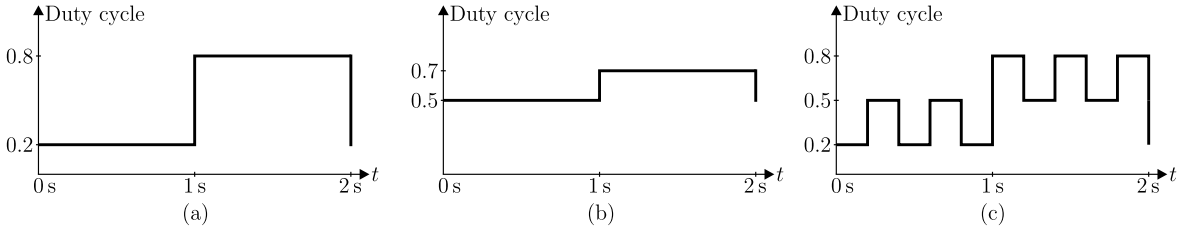


Fig. 4.34: Duty cycle input profiles for (a) large periodic load cycles, (b) low periodic load cycles, and (c) superposition of multiple periodic load cycles.

Table 4.10: Convergence of PSO-based thermal DT for different duty cycle input profiles.

Input profile	Fig. 4.34 (a)	Fig. 4.34 (b)	Fig. 4.34 (c)
$\min_{b\in[1,B_{\mathrm{PSO}}]}\left(f_{\mathrm{obj,ref},b}\right)$ in K	0.33	4.39	7.09

Table 4.11: Convergence of DEKF-based thermal DT for different duty cycle input profiles.

Input profile	Fig. 4.34 (a)	Fig. 4.34 (b)	Fig. 4.34 (c)
$f_{\mathrm{obj,ref}}$ in K	0.00	0.00	0.00

For the DEKF-based thermal DT, there would be the possibility to carry out the correction of states and parameters not each thermal RTS time step d_{th}, but for example every second step. This would decrease the computational burden of the DEKF-based thermal DT, but might also decrease the convergence speed.

For the PSO-based thermal DT, it would be possible to save one measured thermal cycle at d_{th} time steps and to execute multiple optimization epochs based on this measured and saved thermal cycle in faster than real-time. This would increase the convergence speed of the PSO-based thermal DT, but also increase the computational burden. Another opportunity that would be offered by this asynchronous implementation is that the saved and measured thermal cycle considered in the optimization could be not updated based on a fixed time interval, but when a new thermal cycle proper for the characterization has been identified. This would overcome the necessity of the PSO-based thermal DT to apply a specific characterization profile during the convergence.

Implementation of the asynchronous execution of the thermal DT approaches is out of the scope of this work.

Summary of the comparison

The strengths and weaknesses of both thermal DT approaches are illustrated in Fig. 4.35. The results of the comparison of the thermal DT approaches are:

- The PSO-based thermal DT provides a lower computational burden than the DEKF-based thermal DT. The computational burden of the PSO-based thermal DT increases linearly with extending the thermal network, whereas the one of the DEKF-based thermal DT increases quadratically.

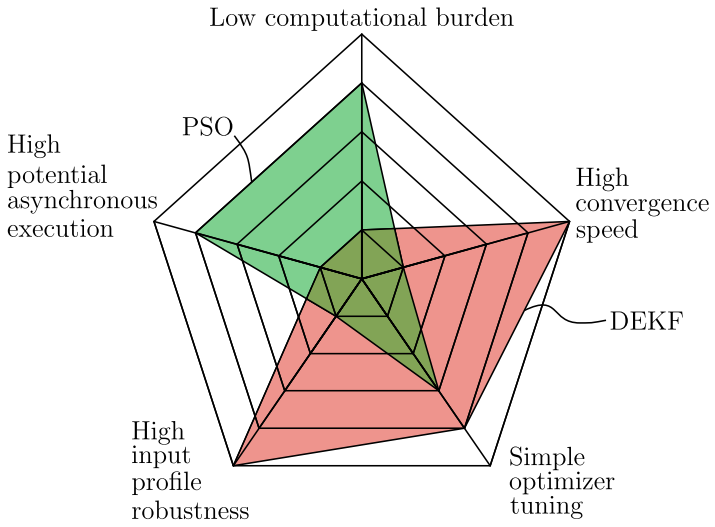


Fig. 4.35: Comparison of PSO-based and DEKF-based thermal DT.

- The DEKF-based thermal DT provides significantly higher convergence speed of the estimated thermal parameters to the reference ones than the PSO-based thermal DT.
- The optimizer coefficient tuning of the DEKF-based thermal DT provides a wider range which leads to convergence than the one of the PSO-based thermal DT.
- The convergence of the DEKF-based thermal DT shows significantly higher robustness to input profile variations compared to the one of the PSO-based thermal DT, which requires a specific characterization operation profile.
- The potential of an asynchronous execution of the optimization is higher for the PSO- compared with the DEKF-based thermal DT, because it could compensate significant drawbacks of the PSO- compared to the DEKF-based thermal DT.

4.3.5. Multichip thermal digital twin

The multichip version of the thermal DT is implemented with the DEKF-based approach. This is due to the fact that the PSO-based thermal DT has high convergence times, which would further increase with more complex multichip thermal models with consideration of thermal cross coupling effects. Furthermore, the higher input profile robustness of the DEKF- compared to the PSO-based thermal DT facilitates the implementation of a multichip thermal DT, where different input profiles for the chips have coupled impacts on the chip temperatures.

Utilization of the linear accumulation approach for modeling the thermal network of multiple chips with cross coupling effects, which was presented in Section 4.1, would lead to a high number of thermal parameters and temperature states that have to be handled. This would cause a high computational burden of the DEKF-based multichip thermal DT. Therefore, a new multichip Cauer network is proposed (Fig. 4.36), which is able to represent the

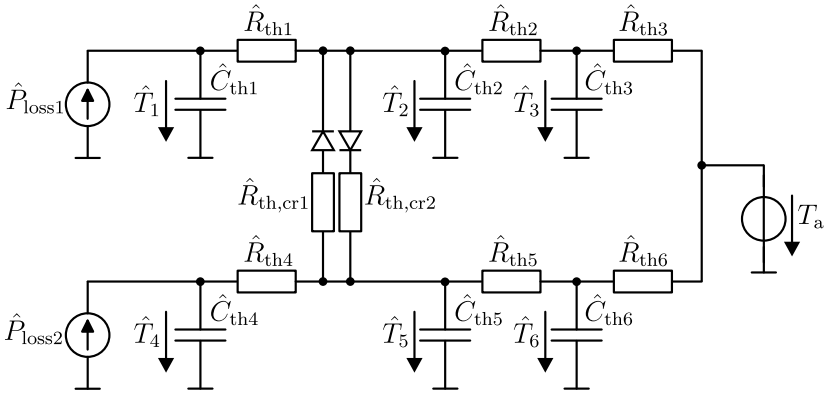


Fig. 4.36: Proposed multichip Cauer network of two chips with three chain elements each and direction dependent thermal cross coupling.

temperatures of multiple chips with cross coupling effects and provides a low number of temperature states and thermal parameters. The multichip Cauer network in Fig. 4.36 is based on a thermal network proposed in [146], which was extended with direction dependent thermal cross coupling resistances to model unsymmetrical thermal cross coupling effects due to unsymmetrical locations of the chips in the power module. The direction dependency inserts conditions in the differential equations discretized with the forward Euler method

$$\begin{aligned}
\hat{T}_1(k+1) &= \hat{T}_1(k) + \frac{\hat{P}_{\text{loss1}}(k)d_{\text{th}}}{\hat{C}_{\text{th1}}(k)} - \frac{(\hat{T}_1(k)-\hat{T}_2(k))d_{\text{th}}}{\hat{R}_{\text{th1}}(k)\hat{C}_{\text{th1}}(k)} \\
\hat{T}_3(k+1) &= \hat{T}_3(k) + \frac{(\hat{T}_2(k)-\hat{T}_3(k))d_{\text{th}}}{\hat{R}_{\text{th2}}(k)\hat{C}_{\text{th3}}(k)} - \frac{(\hat{T}_3(k)-T_{\text{a}}(k))d_{\text{th}}}{\hat{R}_{\text{th3}}(k)\hat{C}_{\text{th3}}(k)} \\
\hat{T}_4(k+1) &= \hat{T}_4(k) + \frac{\hat{P}_{\text{loss2}}(k)d_{\text{th}}}{\hat{C}_{\text{th4}}(k)} - \frac{(\hat{T}_4(k)-\hat{T}_5(k))d_{\text{th}}}{\hat{R}_{\text{th4}}(k)\hat{C}_{\text{th4}}(k)} \\
\hat{T}_6(k+1) &= \hat{T}_6(k) + \frac{(\hat{T}_5(k)-\hat{T}_6(k))d_{\text{th}}}{\hat{R}_{\text{th5}}(k)\hat{C}_{\text{th6}}(k)} - \frac{(\hat{T}_6(k)-T_{\text{a}}(k))d_{\text{th}}}{\hat{R}_{\text{th6}}(k)\hat{C}_{\text{th6}}(k)}
\end{aligned} \tag{4.45}$$

$$\begin{aligned}
&\text{If } \hat{T}_5(k) > \hat{T}_2(k) : \hat{R}_{\text{th,cr1/2}} = \hat{R}_{\text{th,cr1}}(k) \\
&\text{Else : } \hat{R}_{\text{th,cr1/2}} = \hat{R}_{\text{th,cr2}}(k) \\
&\hat{T}_2(k+1) = \hat{T}_2(k) + \frac{(\hat{T}_1(k)-\hat{T}_2(k))d_{\text{th}}}{\hat{R}_{\text{th1}}(k)\hat{C}_{\text{th2}}(k)} - \frac{(\hat{T}_2(k)-\hat{T}_3(k))d_{\text{th}}}{\hat{R}_{\text{th2}}(k)\hat{C}_{\text{th2}}(k)} + \frac{(\hat{T}_5(k)-\hat{T}_2(k))d_{\text{th}}}{\hat{R}_{\text{th,cr1/2}}\hat{C}_{\text{th2}}(k)} \\
&\hat{T}_5(k+1) = \hat{T}_5(k) + \frac{(\hat{T}_4(k)-\hat{T}_5(k))d_{\text{th}}}{\hat{R}_{\text{th4}}(k)\hat{C}_{\text{th5}}(k)} - \frac{(\hat{T}_5(k)-\hat{T}_6(k))d_{\text{th}}}{\hat{R}_{\text{th5}}(k)\hat{C}_{\text{th5}}(k)} - \frac{(T_{5,k}-T_{2,k})d}{\hat{R}_{\text{th,cr1/2}}C_{\text{th5}}(k)} \ .
\end{aligned}$$

The multichip version of the DEKF-based thermal DT has the temperature states and parameters from Fig. 4.36 in vector

$$\begin{aligned}
\hat{\boldsymbol{x}}_{\text{mc}}(k) = [&\hat{T}_1(k)\ \hat{T}_2(k)\ \hat{T}_3(k)\ \hat{T}_4(k)\ \hat{T}_5(k)\ \hat{T}_6(k)\ \hat{R}_{\text{th1}}(k)\ \hat{C}_{\text{th1}}(k) \\
&\hat{R}_{\text{th2}}(k)\ \hat{C}_{\text{th2}}(k)\ \hat{R}_{\text{th3}}(k)\ \hat{C}_{\text{th3}}(k)\ \hat{R}_{\text{th4}}(k)\ \hat{C}_{\text{th4}}(k) \\
&\hat{R}_{\text{th5}}(k)\ \hat{C}_{\text{th5}}(k)\ \hat{R}_{\text{th6}}(k)\ \hat{C}_{\text{th6}}(k)\ \hat{R}_{\text{th,cr1}}(k)\ \hat{R}_{\text{th,cr2}}(k)]^{\text{T}} \ .
\end{aligned} \tag{4.46}$$

The inputs are the power losses of both chips and the ambient temperature

$$\boldsymbol{u}_{\text{mc}}(k) = [\hat{P}_{\text{loss1}}(k)\ \hat{P}_{\text{loss2}}(k)\ T_{\text{a}}(k)]^{\text{T}} \ . \tag{4.47}$$

The outputs are the two chip temperatures

$$\begin{aligned}
\hat{\boldsymbol{y}}_{\text{mc}}(k) &= \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \hat{\boldsymbol{x}}_{\text{mc}}(k) \\
&= [\hat{T}_1(k)\ \hat{T}_4(k)]^{\text{T}} = [\hat{T}_{\text{chip1}}(k)\ \hat{T}_{\text{chip2}}(k)]^{\text{T}} \ .
\end{aligned} \tag{4.48}$$

Each time the equations of the thermal network change due to the $\hat{T}_2$-$\hat{T}_5$ relation-based con-

dition, the changed equations need to be considered when the jacobian matrix of the state equations is calculated

$$\boldsymbol{F}_{\mathrm{mc}}(k) = \begin{bmatrix} \boldsymbol{F}_{\mathrm{mc},1}(k) & \boldsymbol{F}_{\mathrm{mc},2}(k) \\ \boldsymbol{0}_{14,6} & \boldsymbol{E}_{14,14} \end{bmatrix} . \tag{4.49}$$

Herein, $\boldsymbol{0}_{14,6}$ is a zero matrix with fourteen rows and six columns, and $\boldsymbol{E}_{14,14}$ is the identity matrix with fourteen rows and columns. Further, $\boldsymbol{F}_{\mathrm{mc},1}(k)$ is a matrix with six rows and columns describing the partial derivatives of the temperature state equations from (4.45) by the temperature states

$$\boldsymbol{F}_{\mathrm{mc},1}(k) = \begin{bmatrix} \boldsymbol{F}_{\mathrm{mc},3}(k) & \boldsymbol{F}_{\mathrm{mc},4}(k) & \boldsymbol{F}_{\mathrm{mc},5}(k) \end{bmatrix} \tag{4.50}$$

with

$$\boldsymbol{F}_{\mathrm{mc},3}(k) = \begin{bmatrix} 1 - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th1}}(k)} & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th1}}(k)} \\ \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th2}}(k)} & 1 - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th2}}(k)} - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th2}}(k)} - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th,cr1/2}}(k)\hat{C}_{\mathrm{th2}}(k)} \\ 0 & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th3}}(k)} \\ 0 & 0 \\ 0 & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th,cr1/2}}(k)\hat{C}_{\mathrm{th5}}(k)} \\ 0 & 0 \end{bmatrix} , \tag{4.51}$$

$$\boldsymbol{F}_{\mathrm{mc},4}(k) = \begin{bmatrix} 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th2}}(k)} & 0 \\ 1 - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th3}}(k)} - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th3}}(k)\hat{C}_{\mathrm{th3}}(k)} & 0 \\ 0 & 1 - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th4}}(k)\hat{C}_{\mathrm{th4}}(k)} \\ 0 & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th4}}(k)\hat{C}_{\mathrm{th5}}(k)} \\ 0 & 0 \end{bmatrix} , \tag{4.52}$$

and

$$\boldsymbol{F}_{\mathrm{mc},5}(k) = \begin{bmatrix} 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th,cr1/2}}(k)\hat{C}_{\mathrm{th2}}(k)} & 0 \\ 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th4}}(k)\hat{C}_{\mathrm{th4}}(k)} & 0 \\ 1 - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th4}}(k)\hat{C}_{\mathrm{th5}}(k)} - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th5}}(k)\hat{C}_{\mathrm{th5}}(k)} - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th,cr1/2}}(k)\hat{C}_{\mathrm{th5}}(k)} & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th5}}(k)\hat{C}_{\mathrm{th5}}(k)} \\ \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th5}}(k)\hat{C}_{\mathrm{th6}}(k)} & 1 - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th5}}(k)\hat{C}_{\mathrm{th6}}(k)} - \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th6}}(k)\hat{C}_{\mathrm{th6}}(k)} \end{bmatrix} . \tag{4.53}$$

$\boldsymbol{F}_{\mathrm{mc},2}(k)$ is a matrix with six rows and fourteen columns describing the partial derivatives of

the temperature state equations from (4.45) by the predicted thermal parameters

$$\boldsymbol{F}_{\mathrm{mc},2}(k) = \begin{bmatrix} \boldsymbol{F}_{\mathrm{mc},6}(k) & \boldsymbol{F}_{\mathrm{mc},7}(k) & \boldsymbol{F}_{\mathrm{mc},8}(k) & \boldsymbol{F}_{\mathrm{mc},9}(k) & \boldsymbol{F}_{\mathrm{mc},10}(k) & \boldsymbol{F}_{\mathrm{mc},11}(k) & \boldsymbol{F}_{\mathrm{mc},12\mathrm{a/b}}(k) \end{bmatrix} \tag{4.54}$$

with

$$\boldsymbol{F}_{\mathrm{mc},6}(k) = \begin{bmatrix} \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th1}}(k)} \left(\hat{T}_1(k) - \hat{T}_2(k)\right) & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th1}}(k)\hat{C}^2_{\mathrm{th1}}(k)} \left(\hat{T}_1(k) - \hat{T}_2(k) - \hat{R}_{\mathrm{th1}}(k)\hat{P}_{\mathrm{loss},1}(k)\right) \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th1}}(k)\hat{C}_{\mathrm{th2}}(k)} \left(\hat{T}_2(k) - \hat{T}_1(k)\right) & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \tag{4.55}$$

$$\boldsymbol{F}_{\mathrm{mc},7}(k) = \begin{bmatrix} 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th2}}(k)} \left(\hat{T}_2(k) - \hat{T}_3(k)\right) & \frac{d_{\mathrm{th}}}{\hat{C}^2_{\mathrm{th2}}(k)} \left(\frac{\hat{T}_2(k) - \hat{T}_1(k)}{\hat{R}_{\mathrm{th1}}(k)} + \frac{\hat{T}_2(k) - \hat{T}_3(k)}{\hat{R}_{\mathrm{th2}}(k)} + \frac{\hat{T}_2(k) - \hat{T}_5(k)}{\hat{R}_{\mathrm{th,cr1/2}}(k)} \right) \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th2}}(k)\hat{C}_{\mathrm{th3}}(k)} \left(\hat{T}_3(k) - \hat{T}_2(k)\right) & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \tag{4.56}$$

$$\boldsymbol{F}_{\mathrm{mc},8}(k) = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th3}}(k)\hat{C}_{\mathrm{th3}}(k)} \left(\hat{T}_3(k) - T_{\mathrm{a}}(k)\right) & \frac{d_{\mathrm{th}}}{\hat{C}^2_{\mathrm{th3}}(k)} \left(\frac{\hat{T}_3(k) - \hat{T}_2(k)}{\hat{R}_{\mathrm{th2}}(k)} + \frac{\hat{T}_3(k) - T_{\mathrm{a}}(k)}{\hat{R}_{\mathrm{th3}}(k)} \right) \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \tag{4.57}$$

$$\boldsymbol{F}_{\mathrm{mc},9}(k) = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th4}}(k)\hat{C}_{\mathrm{th4}}(k)} \left(\hat{T}_4(k) - \hat{T}_5(k)\right) & \frac{d_{\mathrm{th}}}{\hat{R}_{\mathrm{th4}}(k)\hat{C}^2_{\mathrm{th4}}(k)} \left(\hat{T}_4(k) - \hat{T}_5(k) - \hat{R}_{\mathrm{th4}}(k)\hat{P}_{\mathrm{loss},2}(k)\right) \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th4}}(k)\hat{C}_{\mathrm{th5}}(k)} \left(\hat{T}_5(k) - \hat{T}_4(k)\right) & 0 \\ 0 & 0 \end{bmatrix}, \tag{4.58}$$

$$\boldsymbol{F}_{\mathrm{mc},10}(k)=\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th5}}(k)\hat{C}_{\mathrm{th5}}(k)}\left(\hat{T}_5(k)-\hat{T}_6(k)\right) & \frac{d_{\mathrm{th}}}{\hat{C}^2_{\mathrm{th5}}(k)}\left(\frac{\hat{T}_5(k)-\hat{T}_4(k)}{\hat{R}_{\mathrm{th4}}(k)}+\frac{\hat{T}_5(k)-\hat{T}_6(k)}{\hat{R}_{\mathrm{th5}}(k)}+\frac{\hat{T}_5(k)-\hat{T}_2(k)}{\hat{R}_{\mathrm{th,cr1/2}}(k)}\right) \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th5}}(k)\hat{C}_{\mathrm{th6}}(k)}\left(\hat{T}_6(k)-\hat{T}_5(k)\right) & 0 \end{bmatrix}, \tag{4.59}$$

$$\boldsymbol{F}_{\mathrm{mc},11}(k)=\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th6}}(k)\hat{C}_{\mathrm{th6}}(k)}\left(\hat{T}_6(k)-T_{\mathrm{a}}(k)\right) & \frac{d_{\mathrm{th}}}{\hat{C}^2_{\mathrm{th6}}(k)}\left(\frac{\hat{T}_6(k)-\hat{T}_5(k)}{\hat{R}_{\mathrm{th5}}(k)}+\frac{\hat{T}_6(k)-T_{\mathrm{a}}(k)}{\hat{R}_{\mathrm{th6}}(k)}\right) \end{bmatrix}, \tag{4.60}$$

and

$$\boldsymbol{F}_{\mathrm{mc},12\mathrm{a}}(k)=\begin{bmatrix} 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th,cr1}}(k)\hat{C}_{\mathrm{th2}}(k)}\left(\hat{T}_2(k)-\hat{T}_5(k)\right) & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th,cr1}}(k)\hat{C}_{\mathrm{th5}}(k)}\left(\hat{T}_5(k)-\hat{T}_2(k)\right) & 0 \\ 0 & 0 \end{bmatrix} \tag{4.61}$$

or

$$\boldsymbol{F}_{\mathrm{mc},12\mathrm{b}}(k)=\begin{bmatrix} 0 & 0 \\ 0 & \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th,cr2}}(k)\hat{C}_{\mathrm{th2}}(k)}\left(\hat{T}_2(k)-\hat{T}_5(k)\right) \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{d_{\mathrm{th}}}{\hat{R}^2_{\mathrm{th,cr2}}(k)\hat{C}_{\mathrm{th5}}(k)}\left(\hat{T}_5(k)-\hat{T}_2(k)\right) \\ 0 & 0 \end{bmatrix}. \tag{4.62}$$

Herein, $R_{\mathrm{th,cr1}}$ for $R_{\mathrm{th,cr1/2}}$ and (4.61) for $\boldsymbol{F}_{\mathrm{mc},12\mathrm{a/b}}(k)$ are taken, if $\hat{T}_5(k)$ is higher than $\hat{T}_2(k)$, and $R_{\mathrm{th,cr2}}$ and (4.62) are taken otherwise.

The DEKF-based multichip thermal DT is implemented in an RTS executed on a Typhoon HIL402 system. In the RTS, the reference chip temperatures T_{chip1} and T_{chip2} are generated via a digital reference model, which has the same structure (Fig. 4.36) as used in the multichip thermal DT. This enables showing that the DT is able to converge to the same parameter set without previous knowledge about the parameters of the reference model. The tuning parameters of the DEKF applied for the implementation of the thermal DT in the RTS are 10^{-10} for each of the entries of $\boldsymbol{Q}_{\mathrm{mc}}$, which is structured like (4.35) with entries for the states and parameters of (4.46), and 10^{-4} for $S_{T_{\mathrm{chip1}}}$ and $S_{T_{\mathrm{chip2}}}$. The time step of the electrical

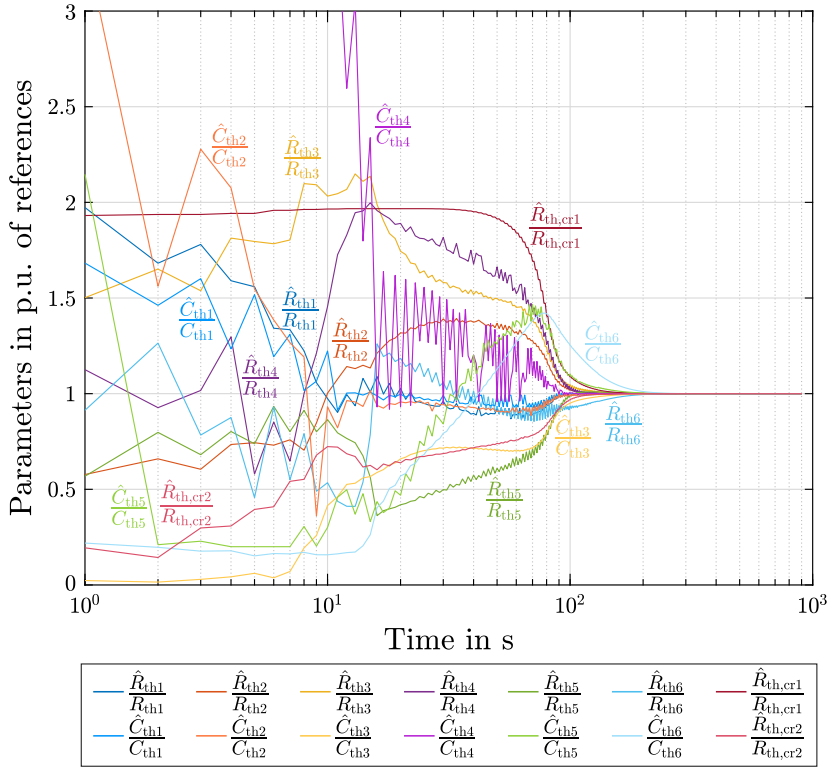


Fig. 4.37: Convergence of the multichip Cauer network parameters in p.u. of their references using the DEKF-based thermal DT in the RTS.

RTS d_{exe} is chosen as 10 µs and the time step of the thermal RTS d_{th} as 800 µs. For the electrical simulation, the IGBTs of two buck converters are considered. The input voltages of the buck converters are chosen as 400 V, the switching frequencies as 1 kHz, the load resistors as 16 Ω, and the inductors as 0.01 H. The duty cycle of the first buck converter is switched between 0.2 and 0.8, each value is applied alternating for 1 s resulting in a square wave with 2 s period. For the duty cycle of the second buck converter, the same profile shifted by 180° to the duty cycle profile of the first buck converter is applied. The prediction and correction of the DEKF-based multichip thermal DT is executed in each step of the thermal RTS $d_{\text{th}} = 800\,\mu\text{s}$.

The convergence of the parameters can be seen in Fig. 4.37. It can be seen that the parameters of the chain elements farthest away from the chip converge to the reference values later than those close to the chip. All parameters converged after approximately 250 s to the reference values. With the DEKF execution time of 800 µs this results in approximately 312500 cycles of prediction and correction until the convergence is reached.

The validation in the laboratory is done on the setup shown in Fig. 4.38. Further, Fig. 4.39 shows the connection scheme of the different components of the setup. The used equipment is listed in Table 4.12, the dc link voltage is 300 V, the loads have 18 Ω, the inductors of the buck converters have 1.8 mH. The DSP provides the gate signals to the physical converter, which is based on an open power module. The thermal DT is executed on the real-time simulator. The temperatures on the physical converter are measured with optic fiber temperature

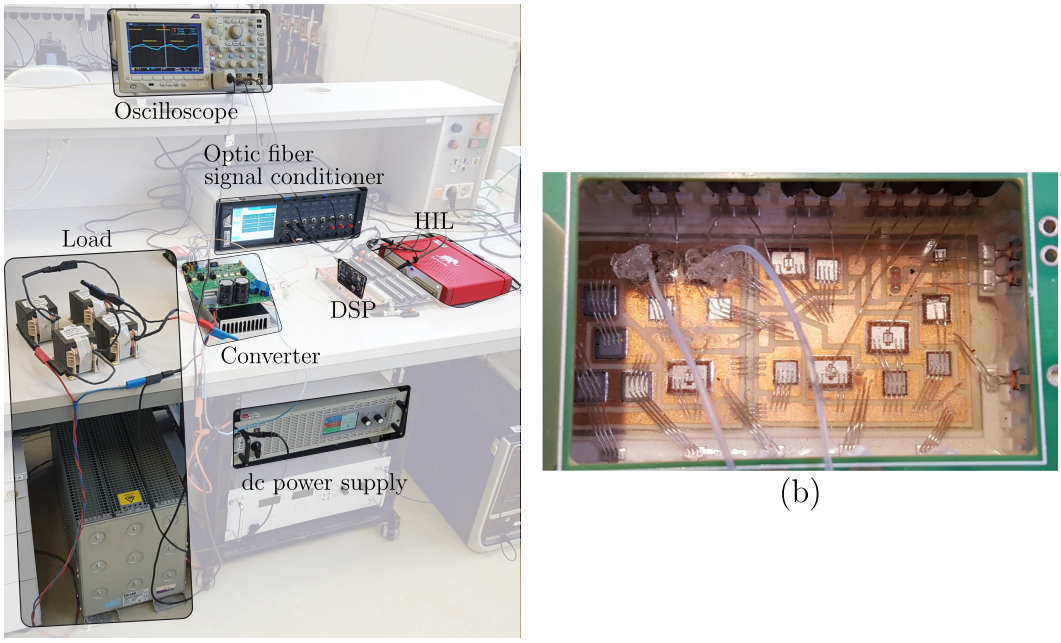


Fig. 4.38: Laboratory setup for the thermal DT with (a) general components and (b) optic fiber temperature sensor placement in the open IGBT module.

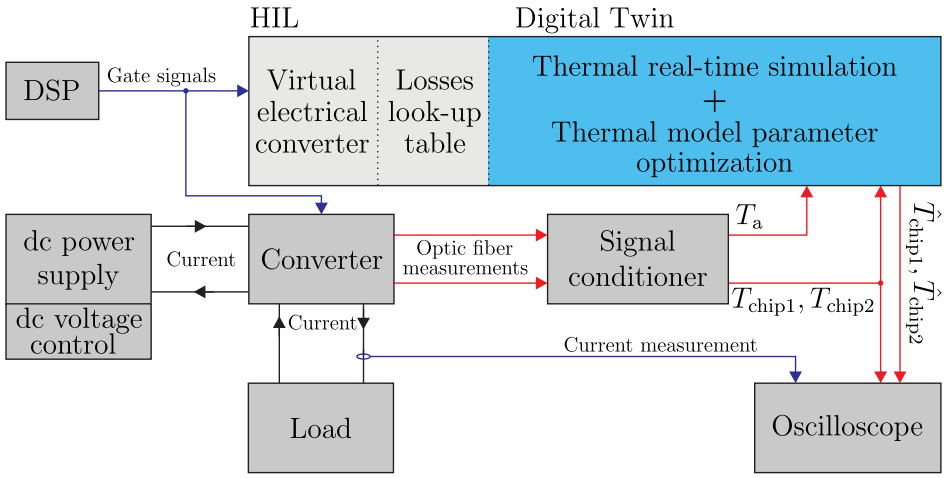


Fig. 4.39: Scheme of the connections in the laboratory setup for the thermal DT.

Table 4.12: Equipment used in the laboratory setup for the thermal DT.

Equipment	Manufacturer	Model
Real-time simulator	Typhoon HIL	HIL402
Digital signal processor	Texas Instruments	TMS320F28379D
dc voltage source	Elektro Automatik	EA-PSI 81000-30
Oscilloscope	Tektronix	DPO 3014
Current probes	Tektronix	TCP0030A
Low voltage probes	Tektronix	P6139A
Optic fiber signal conditioner	Opsens Solutions	PSC-D-N-N-N
Optic fiber temperature sensors	Opsens Solutions	OTG-A

sensors, which are connected to a signal conditioner. The delay induced by the optic fiber temperature sensors and the filtering in the signal conditioner are also modeled in the real-time simulator. For recording high sampled temperature profiles, an oscilloscope is used. The square-wave inputs for the duty cycles of the buck converters have a period of 10 s in the laboratory. The two IGBTs, which are next to each other in the power module (Fig. 4.38 (b)), are switched on for 5 s alternating.

For the laboratory implementation of the DEKF-based multichip thermal DT, a reduced thermal model (neglecting $\hat{R}_{\mathrm{th3}}$, $\hat{C}_{\mathrm{th3}}$, $\hat{R}_{\mathrm{th6}}$, and $\hat{C}_{\mathrm{th6}}$ from Fig. 4.36) is used for representing the thermal behavior of the laboratory prototype. Using more chain elements leads to a convergence of the parameters of these chain elements to regions where they have insignificant impact on the chip temperatures. The tuning parameters of the DEKF applied for the implementation of the thermal DT in the laboratory are 10^{-10} for $Q_{\mathrm{mc},\hat{T}_{\mathrm{chip1}}}$, $Q_{\mathrm{mc},\hat{T}_2}$, $Q_{\mathrm{mc},\hat{T}_{\mathrm{chip2}}}$, $Q_{\mathrm{mc},\hat{T}_5}$, $Q_{\mathrm{mc},\hat{R}_{\mathrm{th,cr1}}}$, $Q_{\mathrm{mc},\hat{R}_{\mathrm{th,cr2}}}$, 10^{-12} for $Q_{\mathrm{mc},\hat{R}_{\mathrm{th1}}}$, $Q_{\mathrm{mc},\hat{R}_{\mathrm{th4}}}$, 10^{-9} for $Q_{\mathrm{mc},\hat{C}_{\mathrm{th1}}}$, $Q_{\mathrm{mc},\hat{C}_{\mathrm{th4}}}$, 10^{-11} for $Q_{\mathrm{mc},\hat{R}_{\mathrm{th2}}}$, $Q_{\mathrm{mc},\hat{R}_{\mathrm{th5}}}$, 10^{-8} for $Q_{\mathrm{mc},\hat{C}_{\mathrm{th2}}}$, $Q_{\mathrm{mc},\hat{C}_{\mathrm{th5}}}$, and 10^{-2} for $S_{T_{\mathrm{chip1}}}$ and $S_{T_{\mathrm{chip2}}}$. Fig. 4.40 presents how the parameters converge towards their final values. The capacitances farthest from chip take longer to converge than the other thermal parameters. Further, the second thermal cross coupling resistor $\hat{R}_{\mathrm{th,cr2}}$ has only low impact on the thermal behavior, because the mean of the second chip temperature T_{chip2} (corresponding to $\hat{T}_4$ in Fig. 4.36) is higher than the mean of T_{chip1} (corresponding to $\hat{T}_1$ in Fig. 4.36). The measured and estimated chip temperatures after convergence are shown in Fig. 4.41.

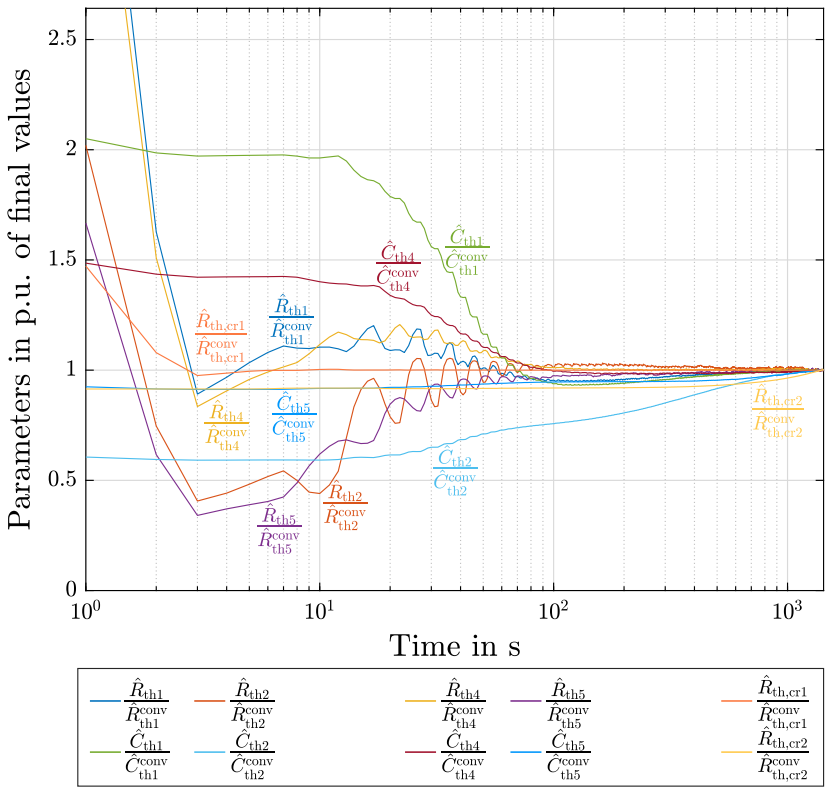


Fig. 4.40: Convergence of the multichip Cauer network parameters in p.u. of their references using the DEKF-based thermal DT in the laboratory.

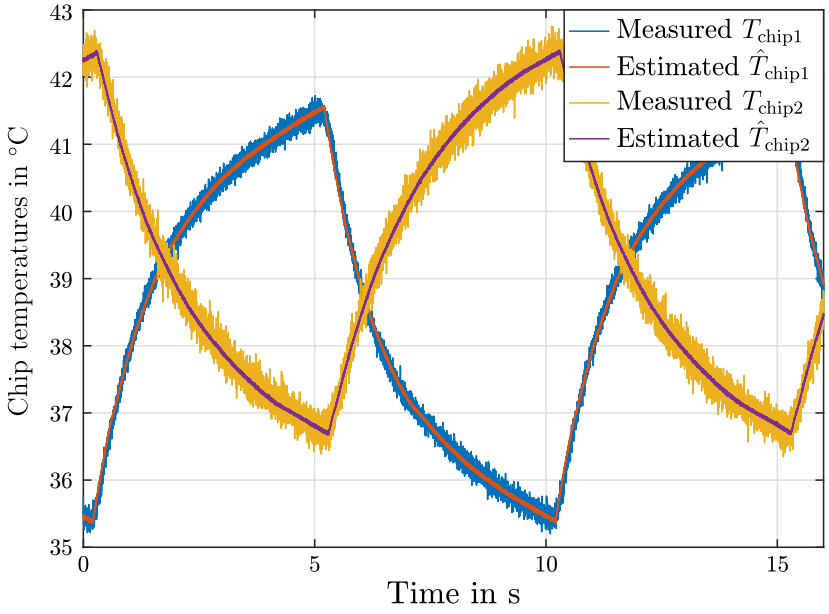


Fig. 4.41: Chip temperature measurements in the laboratory and estimations by the DEKF-based multichip thermal DT for both IGBTs.

The results of the multichip thermal DT implementation are:

- A multichip Cauer network has been proposed, which is able to represent the temperatures of multiple chips with thermal cross coupling effects and provides a low number of temperature states and thermal parameters. This makes the network suitable for the implementation in thermal DTs, as it provides a significantly lower computational burden than applying a linear accumulation of all impacts of heat sources on the temperatures with more states and parameters.
- The RTS of the multichip thermal DT with digital thermal reference model showed that the DT is able to converge to the same parameter set without previous knowledge about the parameters of the reference model.
- The implementation of the multichip thermal DT in the laboratory setup proved the ability to represent the thermal behavior of real power semiconductors precisely.

4.4. Summary and conclusions of the chapter

This chapter introduced the fundamentals of thermal modeling at first in Section 4.1. The basic components of thermal modeling and their analogy to the electrical modeling were presented. Commonly used thermal networks - Foster and Cauer networks - to represent the thermal behavior of a single chip temperature in relation to a reference point temperature have been introduced. An approach to model multiple chip temperatures with thermal cross coupling effects has been presented, it is based on the linear accumulation of all impacts of heat sources on the temperatures.

The essential influence of the temperature on the reliability of power semiconductor modules was highlighted in Section 4.2. For this purpose, the degradation mechanism evoked by thermal cycles was explained, a method for lifetime estimation of power semiconductors based on thermal cycle (rainflow) counting as well as existing lifetime models and their limitations were presented, and a review on condition monitoring possibilities for power semiconductors via their thermal behavior was given.

Section 4.3 proposed the digital twin (DT)-based observation of the power semiconductor thermal behavior. The basic principle of the thermal DT was explained and two approaches were proposed. The first approach is based on a particle-swarm-optimization (PSO) and the second approach on a dual extended Kalman filter (DEKF). It has been shown that both approaches are able to identify the thermal parameters of a digital reference model in a real-time simulation (RTS). Hereby, thermal parameters of model parts closer to the chip temperature converge faster to the parameters of the digital reference model than parameters of model parts further away from the chip temperature. This is due to the fact that parameters of model parts closer to the chip have a higher impact on the chip temperature.

Thereafter, a comparison of both approaches was carried out. The PSO-based thermal DT provides a lower computational burden than the DEKF-based thermal DT. The computational burden of the PSO-based thermal DT increases linearly with extending the thermal network, whereas the one of the DEKF-based thermal DT increases quadratically. The DEKF-based thermal DT provides significantly higher convergence speed of the estimated thermal parameters to the reference ones than the PSO-based thermal DT. The optimizer coefficient tuning of the DEKF-based thermal DT provides a wider range which leads to convergence than the one of the PSO-based thermal DT. The convergence of the DEKF-based thermal DT shows significantly higher robustness to input profile variations compared to the one of the PSO-based thermal DT, which requires a specific characterization operation profile of the converter. The potential of an asynchronous execution of the optimization is higher for the PSO- compared with the DEKF-based thermal DT, because it could compensate significant drawbacks of the PSO- compared to the DEKF-based thermal DT.

Finally, a DEKF-based multichip thermal DT was propsed. For this purpose, a new multichip Cauer network was presented, which is able to represent the temperatures of multiple chips with thermal cross coupling effects and provides a low number of temperature states and thermal parameters. This makes the network suitable for the implementation in the thermal DT, as it provides a significantly lower computational burden than applying a linear accumulation of all impacts of heat sources on the temperatures with more states and parameters. The RTS of the multichip thermal DT with digital thermal reference model showed that the DT is able to converge to the same parameter set without previous knowledge about the reference parameters. The implementation of the multichip thermal DT in the laboratory setup proved the ability to represent the thermal behavior of real power semiconductors.

5. Reliability-driven active thermal control and design for failure tolerance

This chapter mainly deals with approaches aiming to increase the reliability of STs. It considers two paths to do this - reducing or relocating the thermal stress of power semiconductors via active thermal control (ATC) methods and utilizing the lower converter loading within the interconnected topology (IT) of the ST to insert additional failure tolerance. The semiconductor temperatures derived with the thermal digital twins introduced in Section 4.3 can be used in the ATC methods as feedback signal to close the control loop.

The chapter is organized as follows: Based on [21], a review of ATC methods used in power electronics systems as well as an evaluation of these methods for the use in the ST are given in Section 5.1. Section 5.2 elaborates on the graph theory-based modeling used for power routing on basis of [32, 33] by introducing the basics of graph theory-based modeling of power electronics converter systems, describing its application in hybrid grids-feeding STs, as well as revealing and validating a modeling method with higher accuracy for the loss description than the state-of-the-art method. Next, a new third harmonic clamped modulation method - originally presented in [34] - is described, theoretically compared with the first harmonic clamped modulation method, and validated in the laboratory in Section 5.3. Afterwards, Section 5.4 carries out a mission profile-based failure analysis for the hybrid grids-feeding ST topologies and reveals the opportunity for additional failure tolerance in the IT, based on [27, 28]. A summary and the conclusions of the chapter can be found in Section 5.5.

5.1. Review on Active Thermal Control

This section deals with ATC methods reducing or relocating thermal stress of semiconductors, which induces mechanical strain between their different material layers. As presented in Section 4.2, this mechanical strain is the root-cause of semiconductor degradation and their wear-out related failure. Fig. 5.1 shows how the semiconductor reliability is addressed on different levels of the system:

- On a component level, the condition monitoring (CM) methods - such as those presented in Section 4.2.3 - can be the basis of estimating the remaining useful lifetime (RUL).
- On a converter or building block level, ATC methods can be applied to reduce the thermal stress of the semiconductors, therefore, decreasing the mechanical strain induced and extending the RUL of the converter.

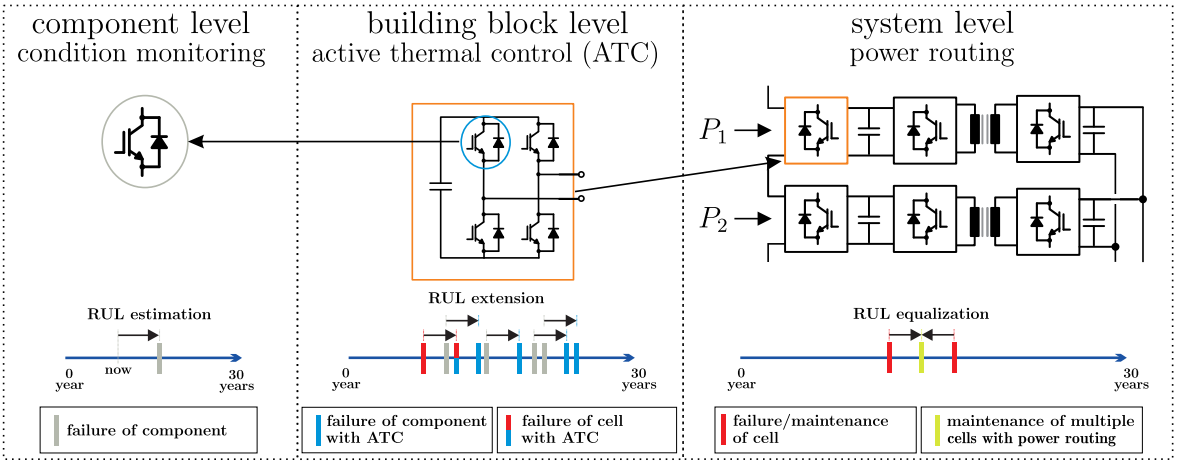


Fig. 5.1: Levels of condition monitoring (CM) and active thermal control (ATC) application and their role in estimating and influencing the remaining useful lifetime (RUL) (adapted from [147]).

- On a converter system level, ATC methods - such as power routing - can be applied to relocate the thermal stress of semiconductors from further degraded system parts to less degraded parts, the RUL of the different system parts can be equalized.

Many ATC methods require a temperature as feedback signal to close the control loop. This temperature can be provided by the thermal digital twins described in Section 4.3.

In this section, an overview of ATC methods used for power electronics systems is given. The different methods are assigned to four main challenges that are addressed in research articles in this area. Further, the potential objectives of the articles assigned to these four main challenges are presented. Afterwards, an evaluation of ATC methods for the application case ST is carried out.

5.1.1. Overview on active thermal control methods

The ATC methods presented in research articles for power electronics systems can be assigned to four main challenges, which are:

- **Increasing the overload capability** of power electronics converters.
- **Thermal cycle reduction** of power devices in power electronics converters.
- **Balancing thermal stress of power devices** within specific topologies or for parallel power devices.
- **Controlling thermal stress of devices in different building blocks** in modular and redundant power electronics systems as well as on a microgrid level.

The research articles about ATC methods for power electronics systems inspected during the literature review that could be assigned to the four main challenges are presented in Table 5.1.

Table 5.1: Possible application of active thermal control.

	Increasing overload capability	Thermal cycle reduction	Balancing thermal stress of power devices	Controlling thermal stress of devices in different building blocks
Methods	**Loss reduction at thermal limits of semiconductors** • PWM frequency reduction [148–155] • Current limit reduction [148–150, 152, 153, 156–159] • Duty ratio reduction [154, 155] • Adaption of current limit to coolant temperature and frequency [157, 160] • Adaption of dc-link voltage [161, 162]	**Switching loss manipulation** • Gate resistance manipulation [163, 164] • PWM frequency manipulation [149–151, 153, 154, 163, 165–185] • Step-wise gate drivers [186–190] • Gate voltage manipulation [191–195] • Dead time manipulation [196] • Manipulation of turn-on and turn-off time [197] • Active shoot-through [198] **Loading manipulation** • Reactive power circulation [199–203] • Adaption of current or voltage limit [153, 174, 175, 194] • Flux control of electric machines that yields optimized losses in the inverter [204, 205] • Thermal stress reduced maximum power point tracking [206–208] • Current increment in drives during low load [178–181, 209, 210] • Adjustment of deceleration slope in drives [177] • Grid load control via voltage and frequency sensitivity [211, 212] **Manipulation of the convection interface** • Cooling fan control [213–216] • Liquid cooling pump control [217, 218] • Thermoelectric cooling control [219] **Manipulation of the Modulation Process** • Discontinuous PWM [165, 175, 177, 178, 181, 194, 220–222] • Duty cycle manipulation in DAB [223] • Model predictive control [224–226] • Buffer voltage manipulation in buck active power decoupling circuit [227]	**Parallel power semiconductors** • Thermal balancing in multichip modules [22, 228–234] • Thermal balancing in parallel power modules [23, 235–237] **Balancing thermal stress within topologies** • Balancing stress of the devices in a topology [24, 238–251]	**Series connected building blocks** • Thermal balancing in modular multilevel converter [252–262] • Thermal balancing in cascaded H-bridge converters [34, 263–269] **Parallel building blocks** • Parallel converters [194, 222, 268, 270–281] • Load sharing in microgrids [282–287] **Coordinated control of specific components** • Power routing [25, 54, 147, 279, 288–295] **System level utilization of redundancy** • Power routing in multi-phase drives [296–299]

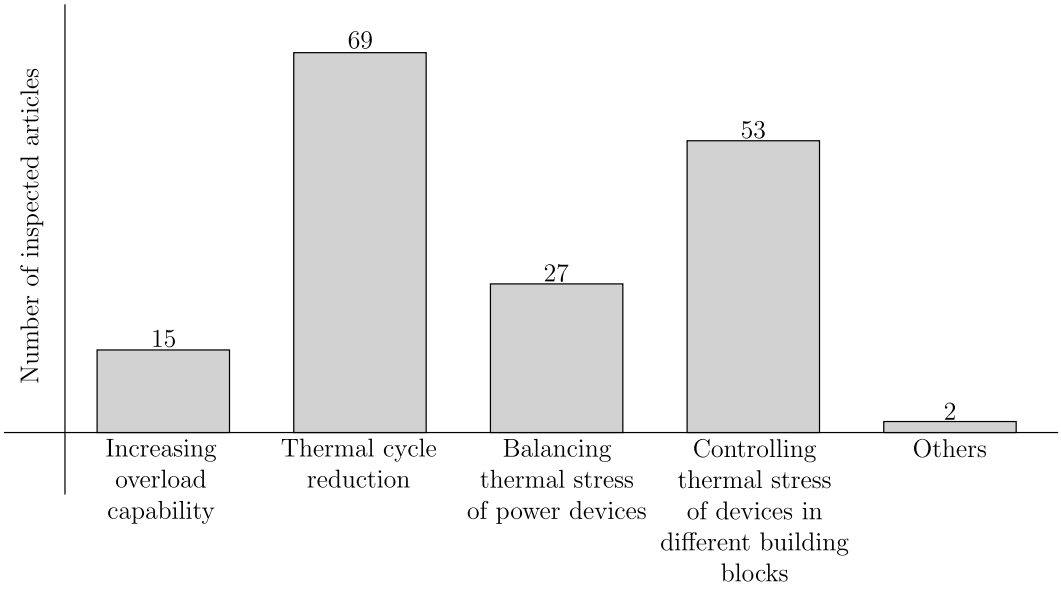


Fig. 5.2: Distribution of inspected research articles on ATC methods for power electronics systems among the different challenges addressed.

One special case, that does not fit into these four main challenges, is the challenge of increasing the temperature of the power devices in power electronics converters for more electric aircraft applications in order to reduce cosmic ray related failures [300]. Another special case is the challenge of keeping the temperature of potential cold spots above the dew point to avoid condensation in power electronics systems for offshore wind power applications [301].

The distribution of the inspected articles among the different challenges addressed in Fig. 5.2 reveals that especially the reduction of thermal cycles and the relocation of thermal stress in the system are of high interest for power electronics applications of ATC methods. Within the challenge of thermal cycle reduction the manipulation of the switching frequency to directly influence the switching losses of the power devices by reducing or increasing the number of hard switching events is often used. This is due to the simple implementation of an adjustable switching frequency on digital signal processors as well as the linear influence of changing the switching frequency on the switching losses. Within the challenge of controlling thermal stress of devices in different building blocks the method of power routing is used in different variations for parallel converters, maintenance scheduling in modular converter systems as well as in multiphase drives. The principle of power routing in all variations is that multiple parallel power paths in the system are available and the thermal stress is relocated among them by increasing the loading of some paths in order to decrease the loading on other paths.

The potential objectives of the ATC utilization concerning the four main challenges are listed in Table 5.2. Within the challenge of increasing the overload capability of power electronics converters, the potential objectives have in common that a safe operation close to the thermal limits needs to be ensured. If it is ensured, it is possible to use higher loading of the

Table 5.2: Potential control objectives of active thermal control.

	Increasing overload capability	Thermal cycle reduction	Balancing thermal stress of power devices	Controlling thermal stress of devices in different building blocks
Potential objectives	• Safe and reliable operation close to thermal limits • Reduced design margin between maximal junction temperature during operation and maximal rated junction temperature • Full utilization of the instantaneous converter power capability at given boundary conditions, e.g. EV-charger adapts its peak power • Transient operation at thermal limits, e.g. for peak torque generation of electrical drives • Provision of maximum possible short-circuit current in case of grid faults to trigger fuses	• Reducing thermal cycles induced fatigue in the converter components • Increasing the operational lifetime of power converters • Preserving reliability, safety and operational lifetime while reducing the power rating of existing power modules • Reducing the variance of fatigue that occurs in power converters, which enables smaller design margins	• Balancing thermal stress of paralleled power converter components • Homogenizing the degradation and time-to-failure of power converter components • Compensating thermal design imbalances yielding more design freedom • Relief loading from power converter components which overheat	• Controlling loading distribution on system components • Equalizing the state of health (SoH) of parallel system power paths • Controlling remaining useful lifetime (RUL) • Achieving optimized maintenance schedules

converters for different purposes. The potential objectives within the challenge of thermal cycle reduction are either directed towards an increase of the possible operational lifetime or towards reducing the power rating of the used power devices while same operational lifetime is ensured. Potential objectives related to the challenge of balancing thermal stress of power devices mainly aim to have an equal distribution of temperature in the power devices.

The potential objectives within the challenge of controlling thermal stress of devices in different building blocks differ from those related to the other challenges, because most of them need information about the state of health (SoH) or even estimation of the RUL to be achieved. Therefore, the CM methods presented in Section 4.2.3 are essential to enable the usage of the ATC methods and the accomplishment of the potential objectives related to this challenge.

5.1.2. Evaluation of active thermal control methods for the ST

The ST related significance of the four main challenges addressed by ATC methods is evaluated in a first step by discussing the potential benefits of achieving the objectives from Table 5.2 for the ST.

The relevance of the objectives related to the challenge of increasing overload capability is low, considering the normal operation of the ST, because during normal operation the

converters in the ST will not be driven close to the thermal limitations of their power devices. However, depending on the used protection schemes in the underlying low voltage grids it might be necessary to provide high overcurrent capability to trigger fuses [44, 302, 303]. In this case, using ATC to provide as much overcurrent as possible without endangering the power devices can be highly beneficial [159]. Even though this topic is of high interest for the integration of STs into the distribution system, it is out of the scope of this work.

Some of the objectives related to the challenge of thermal cycle reduction are generally relevant for the application case ST. Reducing the rating of power modules would be not suitable, because this would also reduce the possible operating area, as it can be seen in the mission profile-based converter design from Section 3.2. Increasing the lifetime of the converters in the ST would be beneficial. However, the ST is composed of many different converters, implementing ATC methods for each of the converters would result in a very high complexity of the ST control system. Furthermore, depending on the chosen ATC methods, the ATC application on each of the converters could influence the neighboring converters as well as the general system control.

The objectives related to the challenge of balancing thermal stress of power devices can be relevant for the ST, if multichip or parallel power modules or topologies which require a thermal balancing - such as an active neutral point clamped converter - are utilized. However, this does not have to be necessarily the case and the challenge is not primarily ST specific.

The relevance of the objectives related to the challenge of controlling thermal stress of devices in different building blocks is very high for the application case ST. This is due to the modular structure of the ST with multiple parallel power paths. Single converter modules could be replaced during maintenance resulting in a system composed of many differently degraded modules [25, 293]. Power routing is a suitable method to address this basic nature of the ST and especially its graph theory-based version provides the possibility of facilitated description of the STs complex converter system [279]. However, power routing is not able to change the thermal stress on the cascaded H-bridge (CHB) cells of the ST topologies presented in Section 3.1 significantly. Therefore, discontinuous modulation has been proposed to influence the thermal stress within the CHB [263–269].

Due to the high relevance for the ST, this work elaborates on the graph theory-based modeling used for power routing by adapting the methodology to be suitable for the hybrid grids-feeding ST based on [32, 33]. Further, a new discontinuous modulation method for the CHB is proposed - originally presented in [34] -, which can be applied parallelly to power routing without influencing the routing of the power.

5.2. Graph theory-based modeling for power routing

This section elaborates on the methodology of graph theory-based modeling for power routing, which has been identified as highly relevant for the application case ST in Section 5.1. The methodology is adapted to be suitable for the description of the hybrid grids-feeding ST in form of the IT presented in Section 3.1. For this purpose, the flow conservation constraint (FCC) [33, 279, 292], which is often used in graph theory, is questioned and a modeling with non-conserved flows (NCF) is proposed to be used for describing the IT via graph theory. Using NCF instead of considering FCC provides a more accurate description of the losses in the converter system, which is especially of high relevance for the IT due to its inherited opportunity of significant efficiency improvement by routing the power, as presented in Section 3.3.

In this section, the basics of graph theory-based modeling of power electronics converter systems are introduced at first. Next, the graph theory-based modeling is applied to a downscaled version of the IT and the difference between FCC- and NCF-based modeling is examined analytically. Afterwards, the impact of using NCF- instead of FCC-based modeling on the losses is validated in the laboratory.

5.2.1. Graph theory-based modeling of power electronics converter systems

The configuration of power electronics converter systems and the different power flows within these systems can be represented by directed graphs $G = (N, A)$ [304–306]. Such a direct graph G contains a set of nodes N describing converters or connection points of the system and a set of arcs A describing the connections between the nodes as well as their direction. The basic components of the graphs used in this work can be seen in Fig. 5.3. Each of the arcs (Fig. 5.3 (a)) is defined as a 2-tuple of the node it originates from and the node it ends in. A power flow is assigned to each arc, which flows from the originating node to the ending node.

There are four kinds of nodes:

- A source node S $\in N$ can be only the origin of arcs and represents a power input to the converter system.

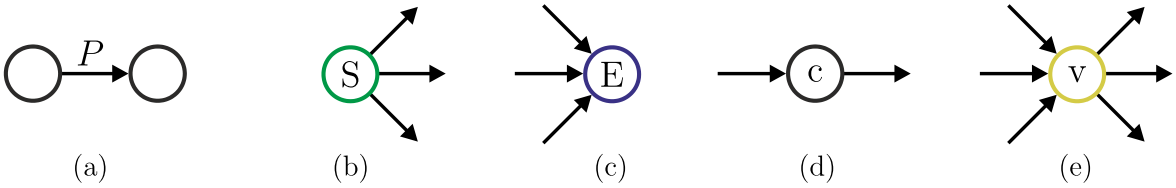


Fig. 5.3: Basic components used for graph theory-based modeling of PE converters: (a) arc with assigned power flow connecting two nodes, (b) source node, (c) sink/end node, (d) converter node, and (e) virtual node.

- A sink/end node E $\in N$ can be only the end of arcs and represents a power output of the converter system.
- A converter node c $\in N$ has one arc ending in and one arc originating from the node. In this work each converter node represents a full converter or - in case of the CHB - a cell of a converter.
- A virtual node v $\in N$ can have multiple arcs ending in and multiple arcs originating from the node. Independent of the other graph modeling constraints the sum of power flows of arcs ending in the node are equal to the sum of power flows of arcs originating from the node. Virtual nodes represent connection points of the converter system where inputs or outputs of more than two converters are linked, such as the dc-link in the IT.

If power electronics converter systems are modeled, a necessary side constraint for the directed graph is the limitation of power flows assigned to the arcs. The power flows are limited to positive values below the lowest power rating of the converters whose nodes are connected by the arc

$$0 \leq P_{j,k} \leq P_{\text{rated},j,k} \quad \text{for all } (j,k) \in A \,. \tag{5.1}$$

An often used side constraint for graphs is the FCC [33, 279, 292], which defines that the power flow of the arc ending in a converter node is equal to the power flow of the arc originating from this converter node

$$\sum_{j \in N} P_{j,k} = \sum_{j \in N} P_{k,j} \quad \text{for all } k \in N \setminus \{\text{S},\text{E}\} \,. \tag{5.2}$$

Therefore, the sum of all power flows assigned to arcs originating from source nodes is equal to the sum of all power flows assigned to arcs ending in sink nodes for considering FCC.

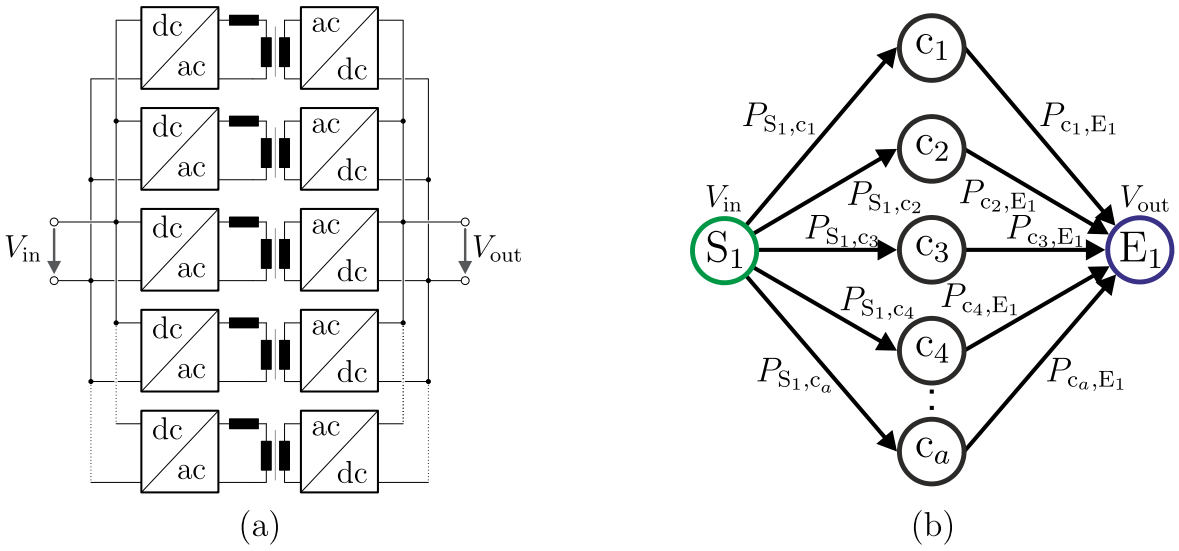


Fig. 5.4: Example of (a) an IPOP DAB converter and (b) its graph theory-based modeling.

An example for using the graph theory-based modeling of a power electronics converter system is the application of power routing for reliability [33, 279, 292] on an input-parallel-output-parallel (IPOP) connection of multiple DABs (Fig. 5.4). To insert the converter reliability in the representation by the graph a weight is assigned to each arc originating from a converter node

$$W_{j,k} = f\left(\rho_j\right) \quad \text{for all } j \in N \setminus \{S_1, E_1\} \ . \tag{5.3}$$

This weight is getting higher the further the components of the converter are degraded. To determine the degradation states and subsequently the weights, condition monitoring methods presented in Section 4.2.3 are necessary.

The optimal power routing to increase the reliability of the IPOP DAB converter can be calculated via the minimum cost convex flow problem

$$\min_{P \in \mathbb{R}^a} \left(\sum_{j \in \{\mathrm{c}_1, \mathrm{c}_2, \ldots, \mathrm{c}_a\}} W_{j,\mathrm{E}_1} P_{j,\mathrm{E}_1}^2 \right) \tag{5.4}$$

formulated as objective function based on the representation by the graph. One further constraint is that the sum of power flows assigned to arcs ending in the sink node $\mathrm{E}_1 \in N$ have to be equal to the output power of the converter system

$$\sum_{j \in \{\mathrm{c}_1, \mathrm{c}_2, \ldots, \mathrm{c}_a\}} P_{j,\mathrm{E}_1} = P_{\mathrm{out}} \ . \tag{5.5}$$

The systematic description by graph theory can facilitate the formulation of the objective function as well as the constraints for complex power electronics converter systems.

5.2.2. Graph theory-based modeling of hybrid grids-feeding Smart Transformers

The potential of using power routing in solely parallel structures of power converter systems as presented in Fig. 5.4 is mainly the equalization of SoH of the parallel power paths or to achieve optimized maintenance schedules. The efficiency plays only a minor role for such structured systems, because changing the power distribution of the total output power among the different power paths has minor impact on the system efficiency [279, 292]. Furthermore, an equal distribution of the total output power among the different power paths would give optimal efficiency for assuming that all power paths have the same loss characteristics and that the system is not in light load operation. This is due to the quadratic rising behavior of the losses with the output power of the converters. Therefore, including the efficiency of the system into the objective function of power routing would only counteract the distribution made based on the reliability of the converters to a minor degree.

The non-interconnected topology (NIT) of the hybrid grids-feeding ST presented in Section 3.1 is similar to a parallel structured power converter system. For the graph theory-based modeling of such systems, the FCC is often considered, because it makes the resulting problem much easier to solve. Using the FCC neglects that the losses of converters are added to the loading of other converters in the real system. However, if the efficiency plays only a minor role for the objective function of the power routing method, using FCC will also have only minor impact on the power distribution among the different power paths.

In opposite to the NIT, applying power routing in the IT can have a significant impact on the efficiency, as it has been shown for passive power routing in Section 3.3. Therefore, the efficiency might play a significant role in a multiobjective optimization function for power routing in the IT. So, a FCC-based graph modeling of the IT could have a significant impact on the power distribution among the different power paths in the system.

For this reason, the resulting total system losses of an FCC-based graph modeling of the IT are compared to those of a NCF-based one. The analysis is done on a down-scaled version of the IT with $\xi = \frac{1}{3}$ - shown in Fig. 5.5 - to demonstrate the graph theory-based modeling approach by nodes and arcs. For this analysis on the down-scaled version, the power ratings and semiconductor modules listed in Table 5.3 and a down-scaled MVac RMS phase-to-phase voltage of 2.2 kV are assumed. 150 kW are considered as 1 p.u. in this section.

The graphs representing the down-scaled version of the IT are shown in Fig. 5.6. A specialty

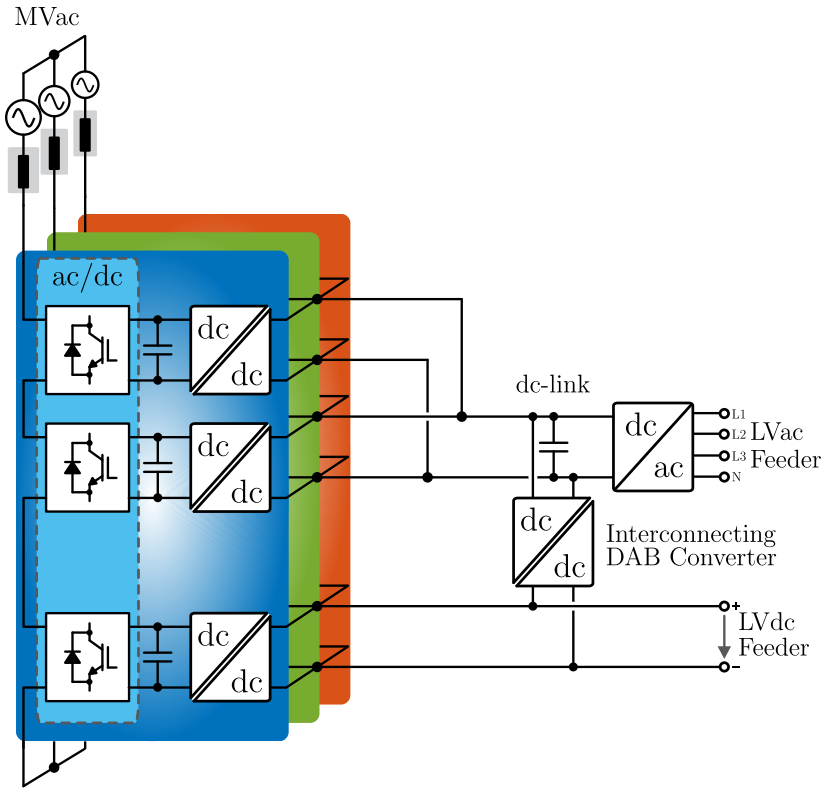


Fig. 5.5: Down-scaled version of the IT (with $\xi = \frac{1}{3}$) for demonstrating the graph theory-based modeling.

Table 5.3: Considered converter power ratings and power semiconductor modules for the graph theory-based modeling of the down-scaled IT.

Converter	Power rating	Semiconductor module
CHB cell	20 kW	FP40R12KE3
DAB connected to CHB	20 kW	FP25R12KE3
All MVac PEBBs	180 kW	-
Interconnecting DAB	160 kW	FF200R12MT4
Three phase inverter	160 kW	FF200R12MT4

in this description is that physically all CHB cells are connected in series, however, the power processed by the different cells can be controlled by giving different modulation indices to each of them. Therefore, the graphs represent the CHB cells as parallel paths to describe the power flow. Depending on the operation point of the LV grids (P_{LVac} P_{LVdc}) and if power is drawn from or fed into the MVac grid, the appropriate graph has to be chosen. Due to the high relevance of the first quadrant of the P_{LVac}-P_{LVdc}-plane shown in Chapter 3, the analysis is executed for the graph shown in Fig. 5.6 (a).

The graph contains a set of nodes

$$N = \{\mathrm{S}_1, \mathrm{E}_1, \mathrm{E}_2, \mathrm{c}_1, \mathrm{c}_2, \mathrm{c}_3, \mathrm{c}_4, \mathrm{c}_5, \mathrm{c}_6, \mathrm{c}_7, \mathrm{c}_8, \mathrm{v}_1, \mathrm{v}_2\} \tag{5.6}$$

where $\mathrm{S}_1 \in N$ represents the sourcing MVac grid, $\{\mathrm{E}_1, \mathrm{E}_2\} \in N$ represent the power consuming LVac and LVdc grids, $\{\mathrm{c}_1, \mathrm{c}_2, \mathrm{c}_3\} \in N$ represent the CHB cells and $\{\mathrm{c}_4, \mathrm{c}_5, \mathrm{c}_6\} \in N$ the MVac PEBB DABs for all three phases in balanced operation, $\mathrm{c}_7 \in N$ represents the interconnecting DAB, $\mathrm{c}_8 \in N$ represents the LVac three phase inverter, and $\{\mathrm{v}_1, \mathrm{v}_2\} \in N$ are virtual nodes used to model the dc-link and the converter connections at the LVdc feeder. Further, the graph is described by a set of arcs

$$\begin{aligned} A = \{&(\mathrm{S}_1, \mathrm{c}_1), (\mathrm{S}_1, \mathrm{c}_2), (\mathrm{S}_1, \mathrm{c}_3), (\mathrm{c}_1, \mathrm{c}_4), (\mathrm{c}_2, \mathrm{c}_5), (\mathrm{c}_3, \mathrm{c}_6), \\ &(\mathrm{c}_4, \mathrm{v}_1), (\mathrm{c}_5, \mathrm{v}_1), (\mathrm{c}_6, \mathrm{v}_2), (\mathrm{v}_1, \mathrm{c}_7), (\mathrm{c}_7, \mathrm{v}_2), \\ &(\mathrm{v}_2, \mathrm{c}_7), (\mathrm{c}_7, \mathrm{v}_1), (\mathrm{v}_2, \mathrm{E}_2), (\mathrm{v}_1, \mathrm{c}_8), (\mathrm{c}_8, \mathrm{E}_1)\} \end{aligned} \tag{5.7}$$

which define the connections between the nodes as well as their direction. To represent the losses of the converters in the graph, the arcs originating from a converter node have a related

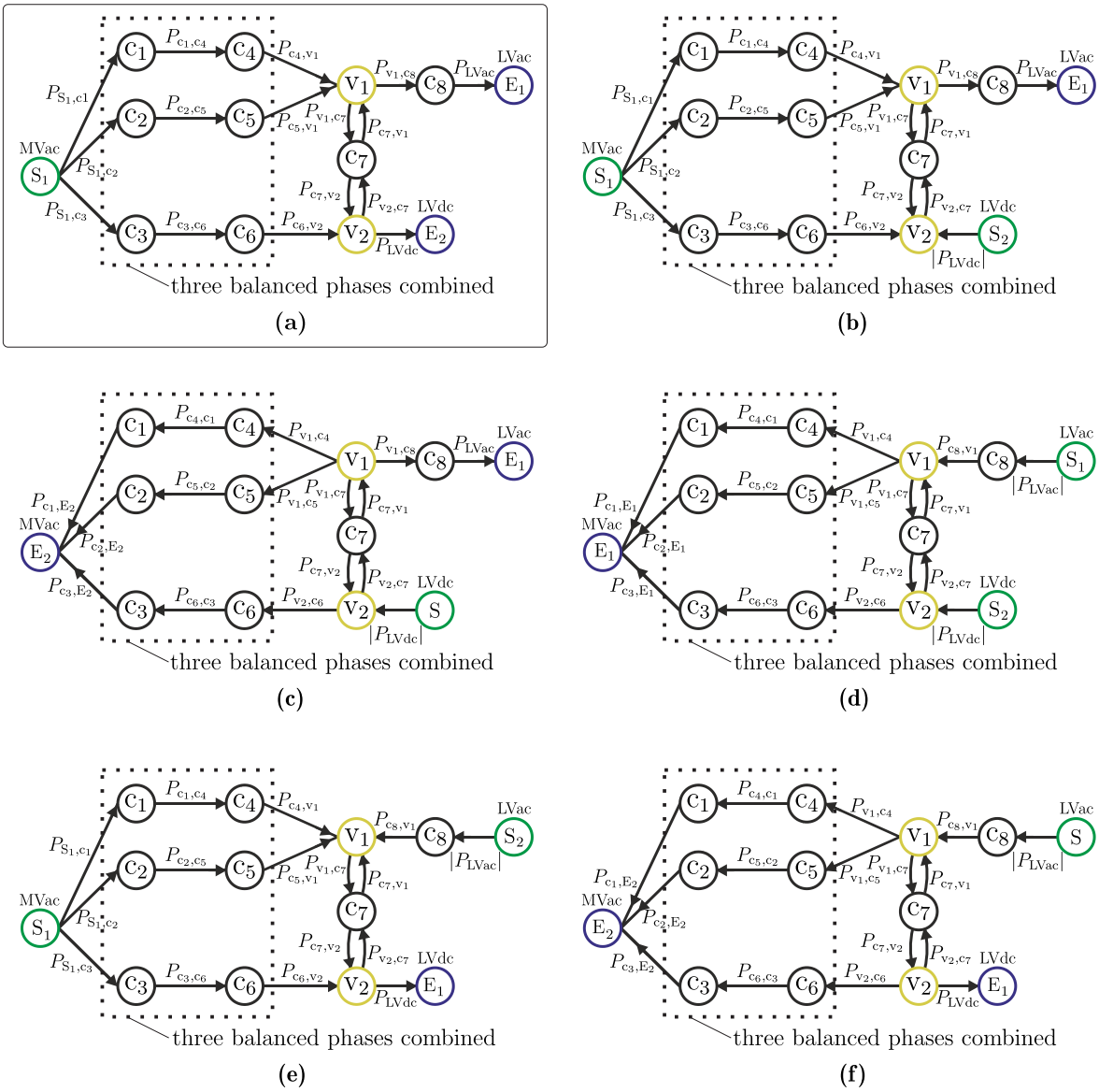


Fig. 5.6: Graph theory based modeling of the down-scaled version of the IT (with $\xi = \frac{1}{3}$) for (a) power consumption in both LV grids, (b) power consumption only in LVac grid, (c) power consumption in LVac grid and feeding power to the MVac grid, (d) only feeding power to the MVac grid, (e) power consumption only in the LVdc grid, and (f) power consumption in the LVdc grid and feeding power to the MVac grid.

non-linear weight

$$W(A) = \Bigg\{ 0,0,0,\frac{1}{\eta_{c_1,b}}-1,\frac{1}{\eta_{c_2,b}}-1,\frac{1}{\eta_{c_3,b}}-1, \\ \frac{1}{\eta_{c_4,b}}-1,\frac{1}{\eta_{c_5,b}}-1,\frac{1}{\eta_{c_6,b}}-1,0, \\ \frac{1}{\eta_{c_7,f}}-1,0,\frac{1}{\eta_{c_7,b}}-1,0,0,\frac{1}{\eta_{c_8,f}}-1 \Bigg\} \tag{5.8}$$

calculated based on the efficiency curves introduced in Section 3.1.

The initial case distinction according to Fig. 5.6 identifies most power flow directions in the graph. However, inside these cases the interconnecting DAB could still transfer power from dc-link to LVdc feeder or vice versa. Therefore, both power directions of the interconnecting DAB are modeled inside the graphs by separate arcs. However, the interconnecting DAB can only transfer power in one direction at a time. Therefore, another necessary side constraint is

$$P_{\mathrm{c}_7,\mathrm{v}_2} = 0 \vee P_{\mathrm{c}_7,\mathrm{v}_1} = 0\,. \tag{5.9}$$

Furthermore, the virtual nodes add more side constraints to the problem description

$$P_{\mathrm{c}_4,\mathrm{v}_1} + P_{\mathrm{c}_5,\mathrm{v}_1} + P_{\mathrm{c}_7,\mathrm{v}_1} = P_{\mathrm{v}_1,\mathrm{c}_8} + P_{\mathrm{v}_1,\mathrm{c}_7} \tag{5.10}$$

$$P_{\mathrm{c}_6,\mathrm{v}_2} + P_{\mathrm{c}_7,\mathrm{v}_2} = P_{\mathrm{LVdc}} + P_{\mathrm{v}_2,\mathrm{c}_7}\,. \tag{5.11}$$

The side constraints mentioned above are valid for the modeling with FCC as well as with NCF.

The following gives the further side constraints to the problem description by considering FCC. The direct implication of using FCC is that the power flow assigned to the arc that ends in a converter node is equal to the power flow assigned to the arc originating from this converter node. This results for the converter nodes of the CHB cells $\{\mathrm{c}_1,\mathrm{c}_2,\mathrm{c}_3\} \in N$ as well as those of the MVac PEBB DABs $\{\mathrm{c}_4,\mathrm{c}_5,\mathrm{c}_6\} \in N$ in the side constraints

$$\begin{pmatrix} P_{\mathrm{S}_1,\mathrm{c}_1} \\ P_{\mathrm{S}_1,\mathrm{c}_2} \\ P_{\mathrm{S}_1,\mathrm{c}_3} \end{pmatrix} = \begin{pmatrix} P_{\mathrm{c}_1,\mathrm{c}_4} \\ P_{\mathrm{c}_2,\mathrm{c}_5} \\ P_{\mathrm{c}_3,\mathrm{c}_6} \end{pmatrix} = \begin{pmatrix} P_{\mathrm{c}_4,\mathrm{v}_1} \\ P_{\mathrm{c}_5,\mathrm{v}_1} \\ P_{\mathrm{c}_6,\mathrm{v}_2} \end{pmatrix}\,. \tag{5.12}$$

For the power flows of the arcs ending in or originating from the converter node $\mathrm{c}_7 \in N$ describing the interconnecting DAB, the following side constraints are added:

$$\begin{pmatrix} P_{\mathrm{v}_1,\mathrm{c}_7} \\ P_{\mathrm{v}_2,\mathrm{c}_7} \end{pmatrix} = \begin{pmatrix} P_{\mathrm{c}_7,\mathrm{v}_2} \\ P_{\mathrm{c}_7,\mathrm{v}_1} \end{pmatrix}\,. \tag{5.13}$$

The last side constraint describes the power flows of the arcs assigned to the converter node $\mathrm{c}_8 \in N$ of the LVac three phase inverter

$$P_{\mathrm{v}_1,\mathrm{c}_8} = P_{\mathrm{LVac}}\,. \tag{5.14}$$

The simple relations between the power flows of the converter system given by the FCC-based modeling provide fast execution times for solving the problem description. However, considering FCC adds inaccuracy to the described losses, because it neglects that the losses of converters are added to the loading of other converters in the real system.

The alternative - not considering FCC - is referred to as modeling based on non-conserved flows (NCF) in this work. This consideration is realized by adding the losses of a converter to the power flow of the arc ending in the node of that converter. The losses of a converter are calculated based on the power flow assigned to the arc originating from its node - the output power of the converter - by non-linear efficiency curves as described in Section 3.1. This results for the converter nodes of the CHB cells $\{c_1, c_2, c_3\} \in N$ as well as those of the MVac PEBB DABs $\{c_4, c_5, c_6\} \in N$ in the side constraints

$$\begin{pmatrix} P_{S_1,c_1} \\ P_{S_1,c_2} \\ P_{S_1,c_3} \end{pmatrix} = \begin{pmatrix} \frac{1}{\eta_{c_1,b}} P_{c_1,c_4} \\ \frac{1}{\eta_{c_2,b}} P_{c_2,c_5} \\ \frac{1}{\eta_{c_3,b}} P_{c_3,c_6} \end{pmatrix} = \begin{pmatrix} \frac{1}{\eta_{c_1,b}} \frac{1}{\eta_{c_4,b}} P_{c_4,v_1} \\ \frac{1}{\eta_{c_2,b}} \frac{1}{\eta_{c_5,b}} P_{c_5,v_1} \\ \frac{1}{\eta_{c_3,b}} \frac{1}{\eta_{c_6,b}} P_{c_6,v_2} \end{pmatrix} . \tag{5.15}$$

For the power flows of the arcs ending in or originating from the converter node $c_7 \in N$ describing the interconnecting DAB, the following side constraints are added:

$$\begin{pmatrix} P_{v_1,c_7} \\ P_{v_2,c_7} \end{pmatrix} = \begin{pmatrix} \frac{1}{\eta_{c_7,f}} P_{c_7,v_2} \\ \frac{1}{\eta_{c_7,b}} P_{c_7,v_1} \end{pmatrix} . \tag{5.16}$$

The last side constraint describes the power flows of the arcs assigned to the converter node $c_8 \in N$ of the LVac three phase inverter

$$P_{v_1,c_8} = \frac{1}{\eta_{c_8,f}} P_{LVac} . \tag{5.17}$$

The NCF-based modeling provides a more accurate description of the converter loading in the system compared FCC-based modeling. Therefore, also the system losses calculated based on the NCF-based modeling are more accurate. However, solving the problem description based on the complex non-linear relations of the power flows - as described in Section 3.1 - requires longer execution times than solving the one using the simple FCC-based modeling.

Based on the description by the graph and the side constraints, the total losses of the converter system can be calculated by

$$P_{sys,loss} = \sum_{b \in A} W_b P_b . \tag{5.18}$$

The total losses of the converter system under the consideration

$$P_{S_1,c_1} = P_{S_1,c_2} = P_{S_1,c_3} \tag{5.19}$$

are used to evaluate the inaccuracy added by considering FCC to the loss description compared to the NCF-based modeling.

The total losses of the converter system in relation to the output power of the IT are shown

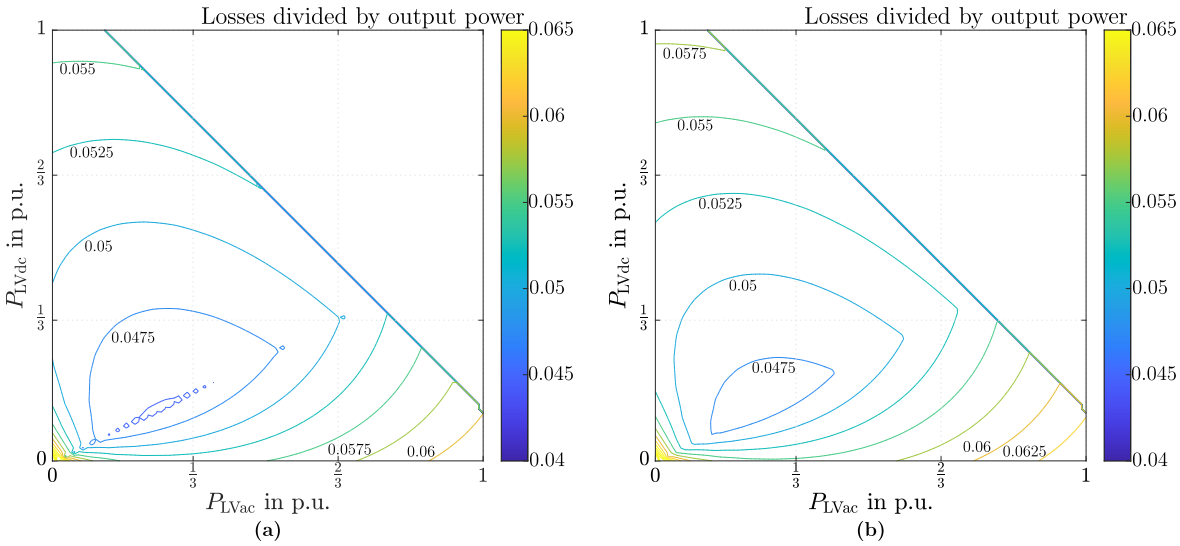


Fig. 5.7: Total system losses divided by output power of the down-scaled IT based on (a) FCC modeling and (b) NCF modeling.

in Fig. 5.7 (a) for the FCC-based and in Fig. 5.7 (b) for the NCF-based modeling. The losses calculated by the NCF-based modeling are higher than those of the FCC-based modeling, because it does not neglect the additional loading by the losses of converters on other converters in the system.

The direct comparison of the total losses calculated with both approaches in Fig. 5.8 shows how much higher the NCF-based calculated losses $P_{\mathrm{sys,loss,NCF}}$ are than the FCC-based calculated losses $P_{\mathrm{sys,loss,FCC}}$

$$\Delta P_{\mathrm{sys,loss,rel}} = \frac{P_{\mathrm{sys,loss,NCF}} - P_{\mathrm{sys,loss,FCC}}}{P_{\mathrm{sys,loss,FCC}}} 100\% \,. \tag{5.20}$$

Depending on the operation point of the LV grids considering FCC is causing up to 4 % error

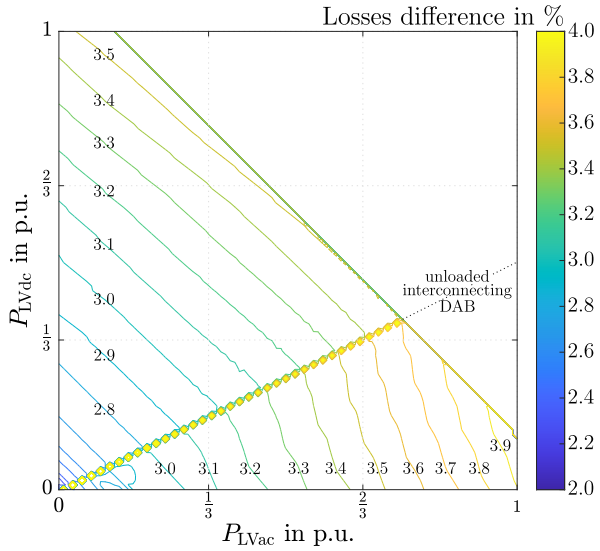


Fig. 5.8: Comparison of losses calculated with NCF to those calculated with FCC.

of the total system losses compared to a more accurate NCF-based modeling. The relative error in the losses by considering FCC increases with the power consumption in the LV grids due to the growing neglected loading by the losses. The operation points with unloaded interconnecting DAB - approximately at $\frac{P_{\mathrm{LVdc}}}{P_{\mathrm{LVac}}} = \frac{\xi}{1-\xi} = \frac{1}{2}$ - can be identified by the change in the increasing behavior of the relative losses difference. Below this line of operation points the interconnecting DAB transfers power from the LVdc feeder to the dc-link and above vice versa. For power flow from the LVdc feeder to the dc-link - below the line -, the losses of the interconnecting DAB need to be provided by the MVac PEBBs connected to the LVdc feeder, whereas for opposite power flow these losses need to be provided by the MVac PEBBs connected to the dc-link. Therefore, below the mentioned line, the losses of the interconnecting DAB need to be provided by a lower number of parallel MVac PEBBs than above this line, which causes higher additional losses considering the decreasing efficiency of the converters above their peak efficiency operation point.

The results of the graph theory-based modeling of the losses in the ST are:

- The graph modeling with flow conservation constraint can have a significant impact on the total system losses of power electronics converter systems.
- The graph modeling with non-conserved flows provides an accurate representation of the losses in power electronics converter systems and should be preferred, if losses or efficiency are an important variable in the optimization process to find the power flow distribution.

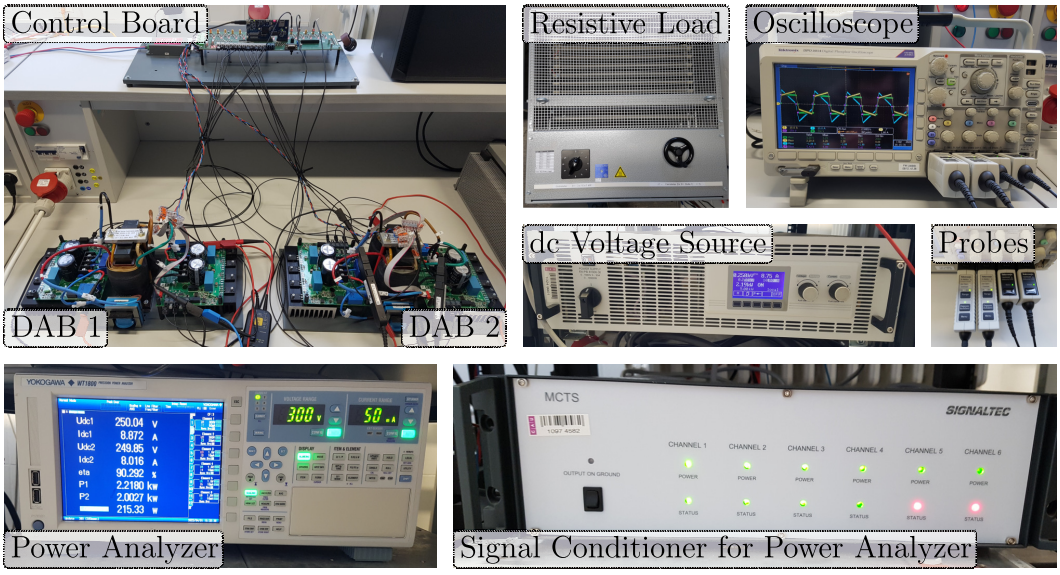


Fig. 5.9: Setup and equipment for validation of NCF-based modeling impact on losses.

Table 5.4: Equipment used for validation of NCF-based modeling impact on losses.

Equipment	Manufacturer	Model
dc voltage source	Elektro Automatik	EA-PSI 81000-30
Digital signal processor	Texas Instruments	TMS320F28379D
Passive load	Frizlen	BW83
Oscilloscope	Tektronix	DPO 3014
Current probes	Tektronix	TCP0030A
Voltage probes	Tektronix	THDP0200
Power analyzer	Yokogawa	WT1800
Signal conditioners (current signals power analyzer)	Signaltec	MCTS
Current sensors (power analyzer)	Dewetron	PM-CM-200

Table 5.5: Experimental setup parameters for validation of NCF-based modeling impact on losses.

Symbol	Representation	Value
V_s	MVac PEBB cell voltages	250 V
V_load	Load voltage	250 V
V_link	Voltage of link between DABs	250 V
$C_\mathrm{DAB,in}$ / $C_\mathrm{DAB,out}$	DAB input and output capacities	0.5 mF
L_DAB	DAB inductances	65 µH
n	Transformer turn ratio DABs	1
$f_\mathrm{sw,DAB}$	DAB switching frequency	20 kHz

5.2.3. Laboratory validation of non-conserved power flow modeling impact on losses

The laboratory validation of the NCF-based modeling impact on the total losses is done with two DABs of the DAB laboratory setup presented in Section 3.3. The setup and the equipment are shown in Fig. 5.9 and listed in Table 5.4. Further, the used parameters of the experimental setup are listed in Table 5.5.

The series connection of the two DABs is considered for the validation. The NCF-based calculation of the losses can be represented by operating the DABs also physically connected in series and measuring the input and load power of the converter system, as shown in Fig. 5.10 (a). However, for representing the FCC-based calculation of the losses with the real laboratory setup, it is necessary to recreate the condition that the first DAB has the same output power as the second one. This can be achieved by operating both of the DABs separately with the same output power, measuring the losses separately, and summing the losses of both DABs afterwards, as shown in Fig. 5.10 (b). In this way, the total converter system losses with conserved power flow through both DABs can be measured.

The total losses measured via both approaches for the representation of NCF- and FCC-based losses calculation on the laboratory setup at different output powers are shown in Fig. 5.11.

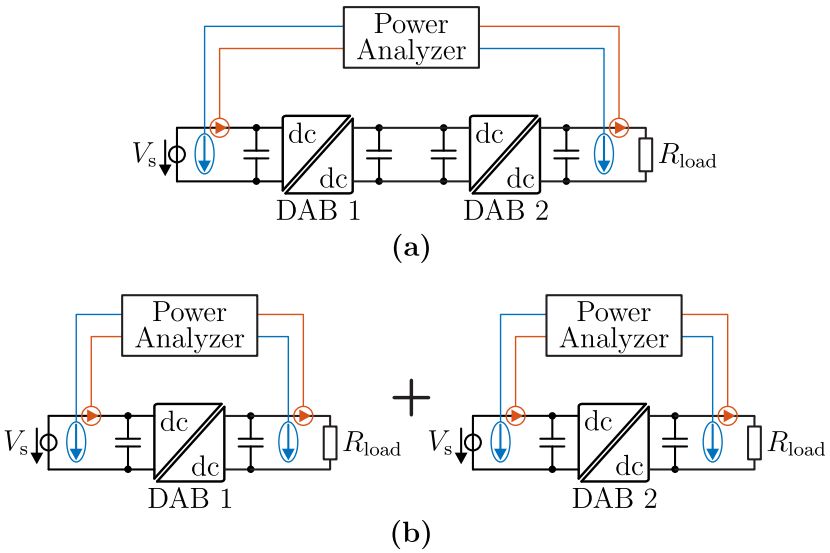


Fig. 5.10: Scheme of the laboratory setup to represent (a) NCF-based and (b) FCC-based losses calculation.

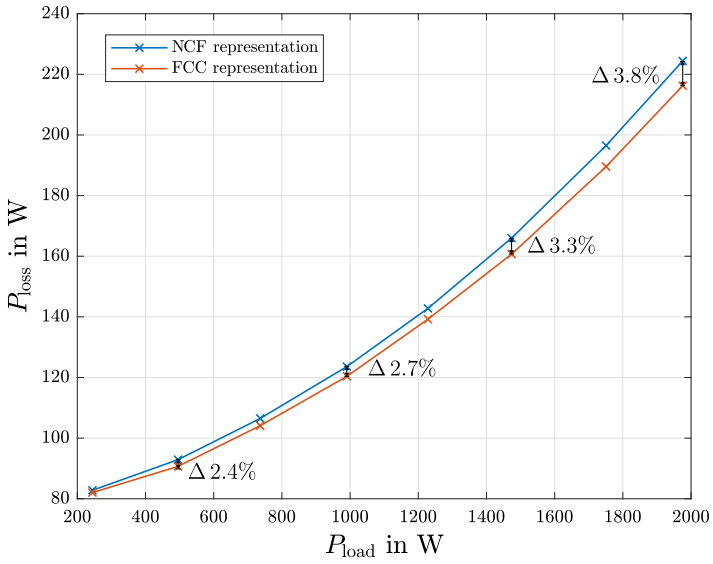


Fig. 5.11: Measured losses at different output powers for NCF and FCC representation.

These results validate that considering FCC introduces a significant error to the total system losses - up to 3.8 % for the conducted measurements. As in the analytical calculation shown in Fig. 5.8, the relative error in the total system losses by considering FCC instead of NCF increases with higher output power of the power electronics converter system.

The result of the presented experiments with the two DABs is:

- It has been validated that the graph modeling with flow conservation constraint can have a significant impact on the total system losses of power electronics converter systems.

5.3. Discontinuous modulation-based active thermal control for cascaded H-bridges

This section proposes a new discontinuous modulation-based active thermal control method for a CHB. The general operation of a CHB is described in Section 2.3. The use of discontinuous modulation to influence the thermal stress within the CHB has been found as an important topic for the ST in Section 5.1. This is due to the fact that power routing for reliability - introduced in Section 5.2 - influences mostly the thermal stress of the MVac PEBB DABs of the ST topologies presented in Section 3.1. However, all CHB cells are connected in series, therefore, the same current flows through them and their thermal stress is not significantly influenced by power routing. The discontinuous modulations proposed for the CHB [263–269] as well as some of those proposed for inverters [175, 178, 181, 220, 221] change the processed power of the CHB cell they are applied to. Therefore, these modulations would interfere with the power routing control and are not suitable to be implemented at the same time as power routing. A discontinuous modulation method which would not change the processed power of the CHB cells is the 60°-flat-top method [307], which was already used as ATC method for inverters [165, 177, 194]. A variation of the 60°-flat-top method with variable top clamped angle was proposed in [222] for inverters, however, it was not described how the modulation signals are generated or look like besides the angle of 60°. The third harmonic clamped modulation method for CHB converters proposed in this section provides a variable clamping angle to be used in ATC and fulfills the requirement of not affecting the power processed by the CHB cells. The proposed method is compared to the first harmonic clamped modulation method previously used for CHB converters [263–268].

In this section, the first harmonic and third harmonic clamped modulation methods are introduced at first. Next, a simulative comparison of the two methods is carried out in terms of influence on the losses, total harmonic distortion (THD), and impact on processed CHB cell power. Afterwards, the impact of the two methods on the processed CHB cell power as well as the ability to shape the temperature profile are validated on a laboratory prototype.

5.3.1. First harmonic clamped modulation method

The first harmonic clamped modulation method reduces the switching losses of the CHB cell it is applied to by setting the modulation function for a variable angle ϕ of a half period to the maximum or minimum of the carrier signal. This clamping angle segment ϕ is placed symmetrically around the maximum for the positive half wave or the minimum for the negative half wave of the sinusoidal modulation signal, as it can be seen in Fig. 5.12 (a). During the clamping angle segment ϕ, the CHB cell has not to switch. This has especially high impact on the overall switching losses, if the CHB current is high, which is the case at the maximum and minimum of the modulation signal for unity power factor.

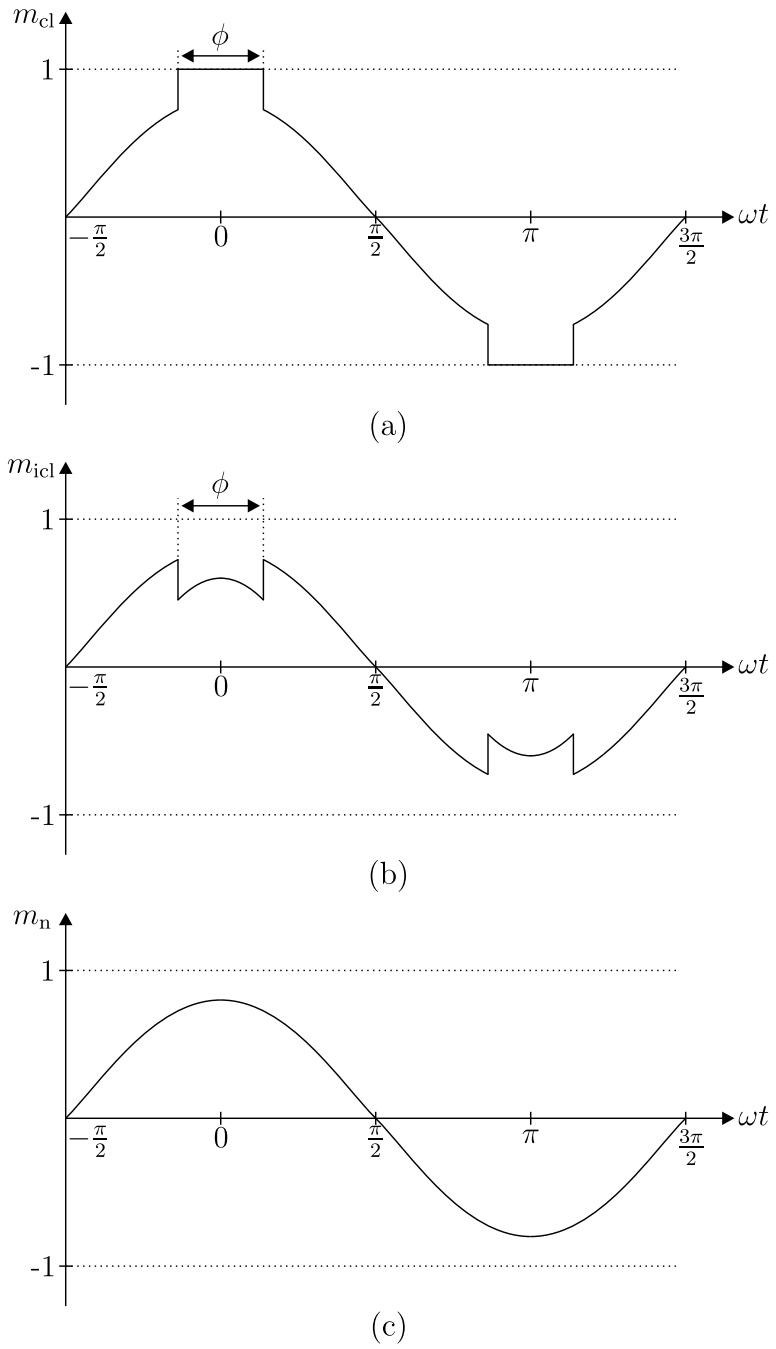


Fig. 5.12: Modulation signals of (a) clamped operated cell, (b) inverse clamped operated cell, and (c) normally operated cell for first harmonic clamped modulation method of a seven-level CHB.

Another cell of the CHB is operated with an inverse clamped modulation signal, as shown in Fig. 5.12 (b). This inverse clamped modulation signal compensates the difference between the clamped operated modulation signal (Fig. 5.12 (a)) and the normal modulation signal (Fig. 5.12 (c)) in the sum of all CHB cell modulation signals.

The generation of the modulation signals for a seven-level CHB based on the first harmonic clamped modulation method is presented in Fig. 5.13. The normal modulation signal $m_{\mathrm{n}}(t)$ given by the current controller is used for the normally operated cell. The clamped and in-

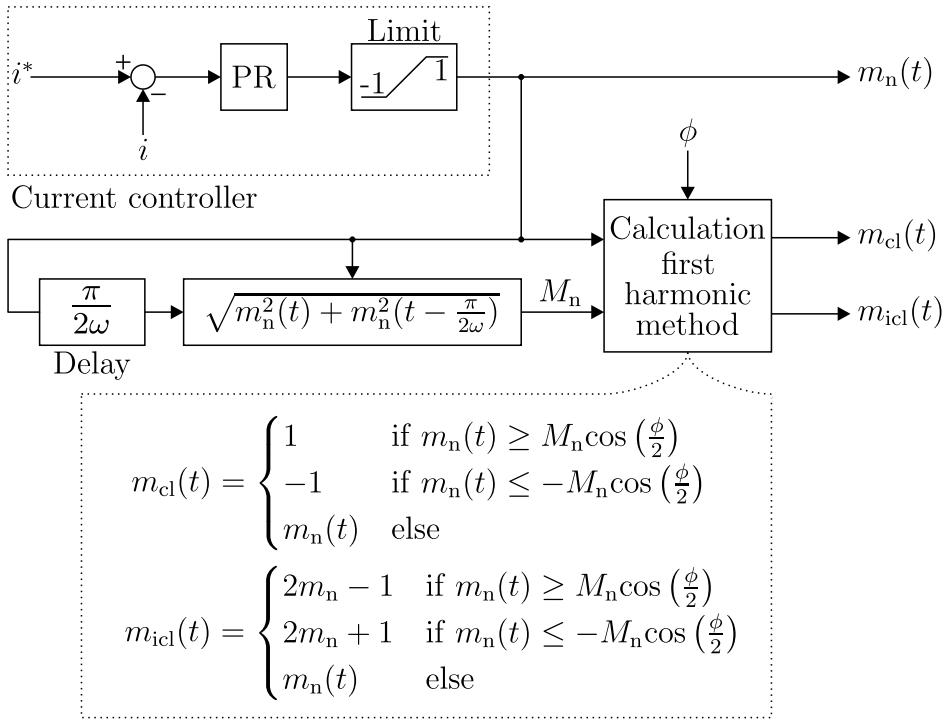


Fig. 5.13: Generation scheme of the modulation signals for first harmonic clamped modulation method of a seven-level CHB in inverter mode.

verse clamped modulation signals ($m_\mathrm{cl}(t)$ and $m_\mathrm{icl}(t)$) are derived based on $m_\mathrm{n}(t)$, the clamping angle ϕ, and the amplitude modulation ratio M_n. For sinusoidal modulation signals, the amplitude modulation ratio M_n can be derived based on $m_\mathrm{n}(t)$ and the by $\frac{\pi}{2\omega}$ delayed modulation signal $m_\mathrm{n}\left(t-\frac{\pi}{2\omega}\right)$

$$\begin{aligned} M_\mathrm{n} &= \sqrt{m_\mathrm{n}^2(t)+m_\mathrm{n}^2\left(t-\frac{\pi}{2\omega}\right)} = \sqrt{M_\mathrm{n}^2\cos^2(\omega t)+M_\mathrm{n}^2\cos^2\left(\omega t-\frac{\pi}{2}\right)} \\ &= \sqrt{M_\mathrm{n}^2\left(\cos^2(\omega t)+\sin^2(\omega t)\right)} \end{aligned} \quad . \tag{5.21}$$

The maximum clamping angle ϕ that can be applied for the first harmonic clamped modulation method is π (180°). Applying this maximum clamping angle results in a square wave signal for the clamped modulation signal. This avoids switching losses as far as possible by reducing the number of switching events per period to two - one at each zero crossing.

5.3.2. Third harmonic clamped modulation method

Also, the third harmonic clamped modulation method reduces the switching losses of the CHB cell it is applied to by setting the modulation function for a variable angle ϕ of a half period to the maximum or minimum of the carrier signal. As for the first harmonic clamped modulation method, this clamping angle segment ϕ is placed symmetrically around the maximum for the positive half wave or the minimum for the negative half wave of the

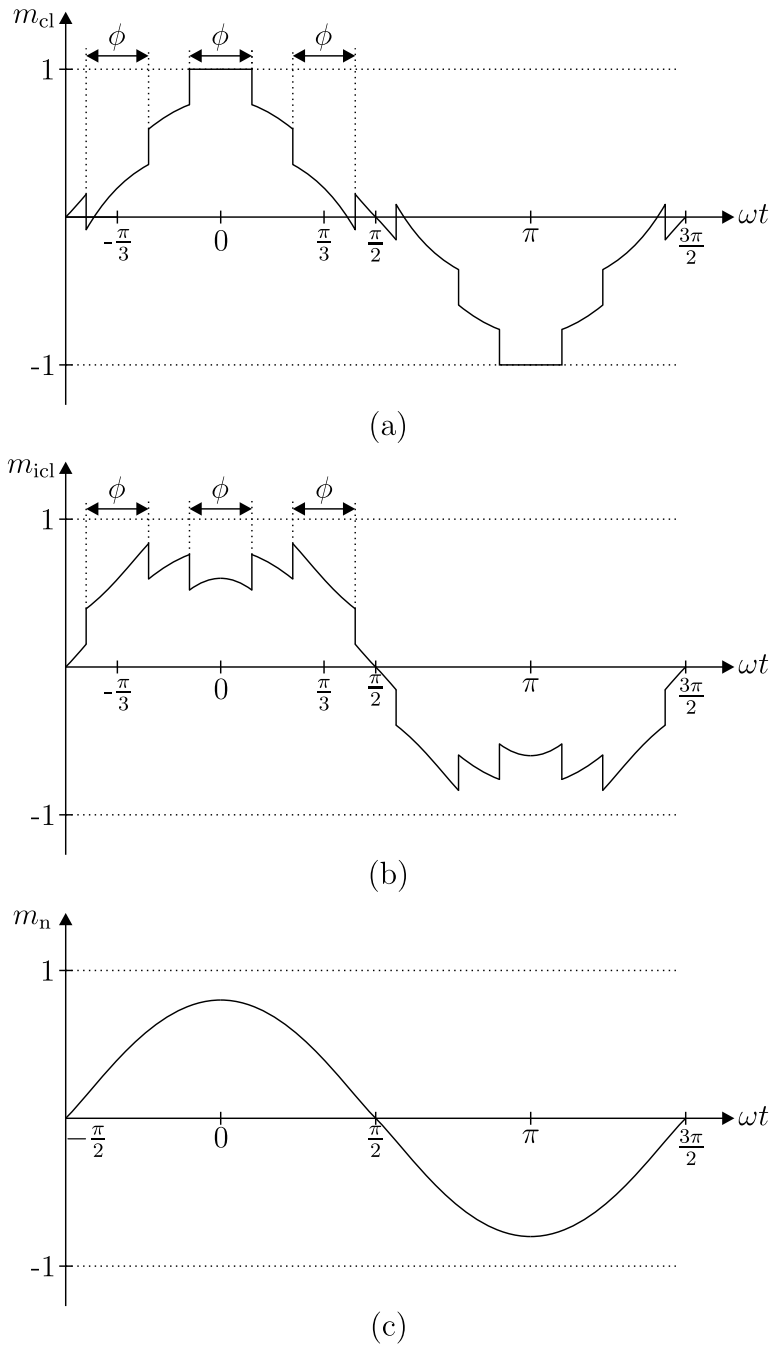
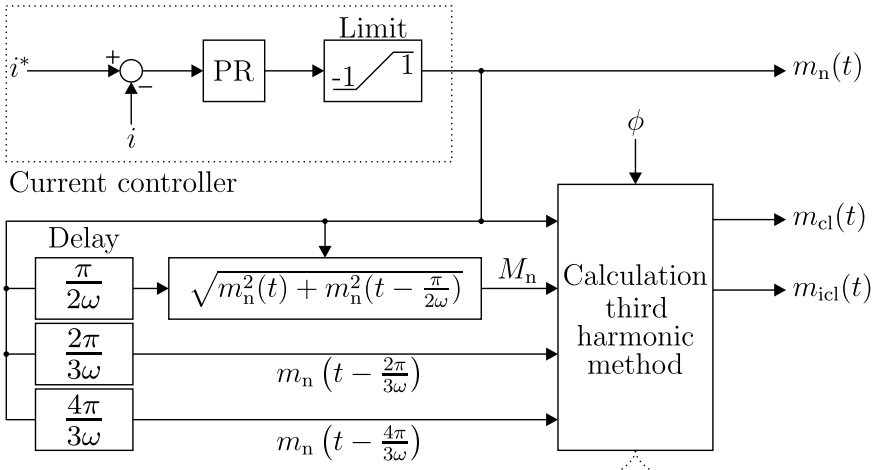


Fig. 5.14: Modulation signals of (a) clamped operated cell, (b) inverse clamped operated cell, and (c) normally operated cell for third harmonic clamped modulation of a seven-level CHB.

sinusoidal modulation signal. However, in contrast to the first harmonic clamped modulation, the clamped modulation signal of the third harmonic clamped modulation method - as it can be seen in Fig. 5.14 (a) - has two additional segments with the width of the clamping angle ϕ for positive as well as negative half wave, where the clamped modulation signal differs from the normal modulation signal m_{n} shown in Fig. 5.14 (c). The centers of these additional segments are $-\frac{\pi}{3}$ ($-60°$) and $\frac{\pi}{3}$ ($60°$) from the maximum of m_{n} for the positive or from the minimum of m_{n} for the negative half wave. For the positive half wave, the difference between maximum carrier signal level - which is one here - and m_{n} for the clamping angle segment



Case 1: $m_\mathrm{n}(t) \geq m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \wedge m_\mathrm{n}(t) \geq m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \wedge m_\mathrm{n}(t) \geq M_\mathrm{n}\cos\left(\frac{\phi}{2}\right)$

Case 2: $m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \geq m_\mathrm{n}(t) \wedge m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \geq m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \wedge m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \geq M_\mathrm{n}\cos\left(\frac{\phi}{2}\right)$

Case 3: $m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \geq m_\mathrm{n}(t) \wedge m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \geq m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \wedge m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \geq M_\mathrm{n}\cos\left(\frac{\phi}{2}\right)$

Case 4: $m_\mathrm{n}(t) \leq m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \wedge m_\mathrm{n}(t) \leq m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \wedge m_\mathrm{n}(t) \leq -M_\mathrm{n}\cos\left(\frac{\phi}{2}\right)$

Case 5: $m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \leq m_\mathrm{n}(t) \wedge m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \leq m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \wedge m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \leq -M_\mathrm{n}\cos\left(\frac{\phi}{2}\right)$

Case 6: $m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \leq m_\mathrm{n}(t) \wedge m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \leq m_\mathrm{n}(t-\frac{2\pi}{3\omega}) \wedge m_\mathrm{n}(t-\frac{4\pi}{3\omega}) \leq -M_\mathrm{n}\cos\left(\frac{\phi}{2}\right)$

$$m_\mathrm{cl}(t) = \begin{cases} 1 & \text{if Case1} \\ m_\mathrm{n}(t) - \left(m_\mathrm{n}(t-\frac{2\pi}{3\omega}) - 1\right) & \text{if Case2} \\ m_\mathrm{n}(t) - \left(m_\mathrm{n}(t-\frac{4\pi}{3\omega}) - 1\right) & \text{if Case3} \\ -1 & \text{if Case4} \\ m_\mathrm{n}(t) - \left(1 + m_\mathrm{n}(t-\frac{2\pi}{3\omega})\right) & \text{if Case5} \\ m_\mathrm{n}(t) - \left(1 + m_\mathrm{n}(t-\frac{4\pi}{3\omega})\right) & \text{if Case6} \\ m_\mathrm{n}(t) & \text{else} \end{cases}$$

$$m_\mathrm{icl}(t) = \begin{cases} 2m_\mathrm{n}(t) - 1 & \text{if Case1} \\ m_\mathrm{n}(t) + \left(m_\mathrm{n}(t-\frac{2\pi}{3\omega}) - 1\right) & \text{if Case2} \\ m_\mathrm{n}(t) + \left(m_\mathrm{n}(t-\frac{4\pi}{3\omega}) - 1\right) & \text{if Case3} \\ 2m_\mathrm{n}(t) + 1 & \text{if Case4} \\ m_\mathrm{n}(t) + \left(1 + m_\mathrm{n}(t-\frac{2\pi}{3\omega})\right) & \text{if Case5} \\ m_\mathrm{n}(t) + \left(1 + m_\mathrm{n}(t-\frac{4\pi}{3\omega})\right) & \text{if Case6} \\ m_\mathrm{n}(t) & \text{else} \end{cases}$$

Fig. 5.15: Generation scheme of the modulation signals for third harmonic clamped modulation of a seven-level CHB in inverter mode.

around the maximum of m_n is subtracted in the additional segments. For the negative half wave, this difference is added in the additional segments.

Another cell of the CHB is operated with an inverse clamped modulation signal, as shown in Fig. 5.14 (b). This inverse clamped modulation signal compensates the difference between

the clamped operated modulation signal (Fig. 5.14 (a)) and the normal modulation signal (Fig. 5.14 (c)) in the sum of all CHB cell modulation signals.

The generation of the modulation signals for a seven-level CHB based on the third harmonic clamped modulation method is presented in Fig. 5.15. The normal modulation signal $m_{\mathrm{n}}(t)$ given by the current controller is used for the normally operated cell. The clamped and inverse clamped modulation signals ($m_{\mathrm{cl}}(t)$ and $m_{\mathrm{icl}}(t)$) are derived based on $m_{\mathrm{n}}(t)$, the clamping angle ϕ, the amplitude modulation ratio M_{n}, the by $\frac{2\pi}{3\omega}$ delayed modulation signal $m_{\mathrm{n}}\left(t-\frac{2\pi}{3\omega}\right)$, and the by $\frac{4\pi}{3\omega}$ delayed modulation signal $m_{\mathrm{n}}\left(t-\frac{4\pi}{3\omega}\right)$. For sinusoidal normal modulation signal $m_{\mathrm{n}}(t)$, the cases 1, 5 and 6 shown in Fig. 5.15 occur during the positive half wave and the cases 2, 3 and 4 during the negative half wave.

The maximum clamping angle ϕ that can be applied for the third harmonic clamped modulation method is $\frac{\pi}{3}$ (60°). At this maximum clamping angle the three angle segments - with a width of ϕ each - fill the full positive or negative half wave receptively. At this maximum ϕ, the clamped modulation signal is equal to the modulation signal used in the 60°-flat-top method [165, 177, 194, 307].

5.3.3. Comparison of first and third harmonic clamped modulation method

The simulative comparison is done for the seven-level CHB operated in inverter mode - feeding power from the dc sides to an ac load -, as shown in Fig. 5.16. An open loop operation of the CHB with the parameters listed in Table 5.6 and the loss characteristics of IXYB82N120C3H1 IGBTs from IXYS are used. Simulations are carried out in Matlab/Simulink with PLECs blockset toolbox and ode23 (Bogacki-Shampine) solver. The fol-

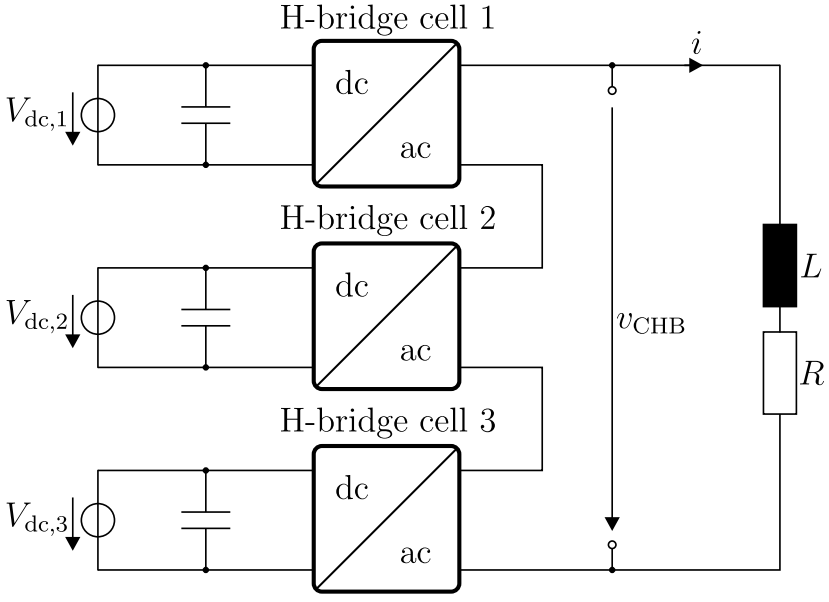


Fig. 5.16: Considered configuration of the seven-level CHB operated in inverter mode.

Table 5.6: Simulation parameters for comparison of first and third harmonic clamped modulation method.

Symbol	Representation	Value
$V_{dc,1}$, $V_{dc,2}$, $V_{dc,3}$	CHB cell dc voltages	800 V
R	Load resistance	21.217 Ω
L	Load inductance	300 µH
f_{ac}	Fundamental frequency	50 Hz
$f_{sw,CHB}$	CHB cell switching frequency	20 kHz

lowing compares the influence on the losses, the THD, and the impact on processed CHB cell power of first and third harmonic clamped modulation method.

The simulated losses of clamped and inverse clamped operated CHB cells depending on the clamping angle ϕ at different root-mean-square (RMS) values of the load current $I_{load,rms}$ are shown in Fig. 5.17 for the first harmonic clamped modulation method. The IGBT losses of the clamped operated CHB cell in Fig. 5.17 (a) - solid lines - decrease at higher clamping

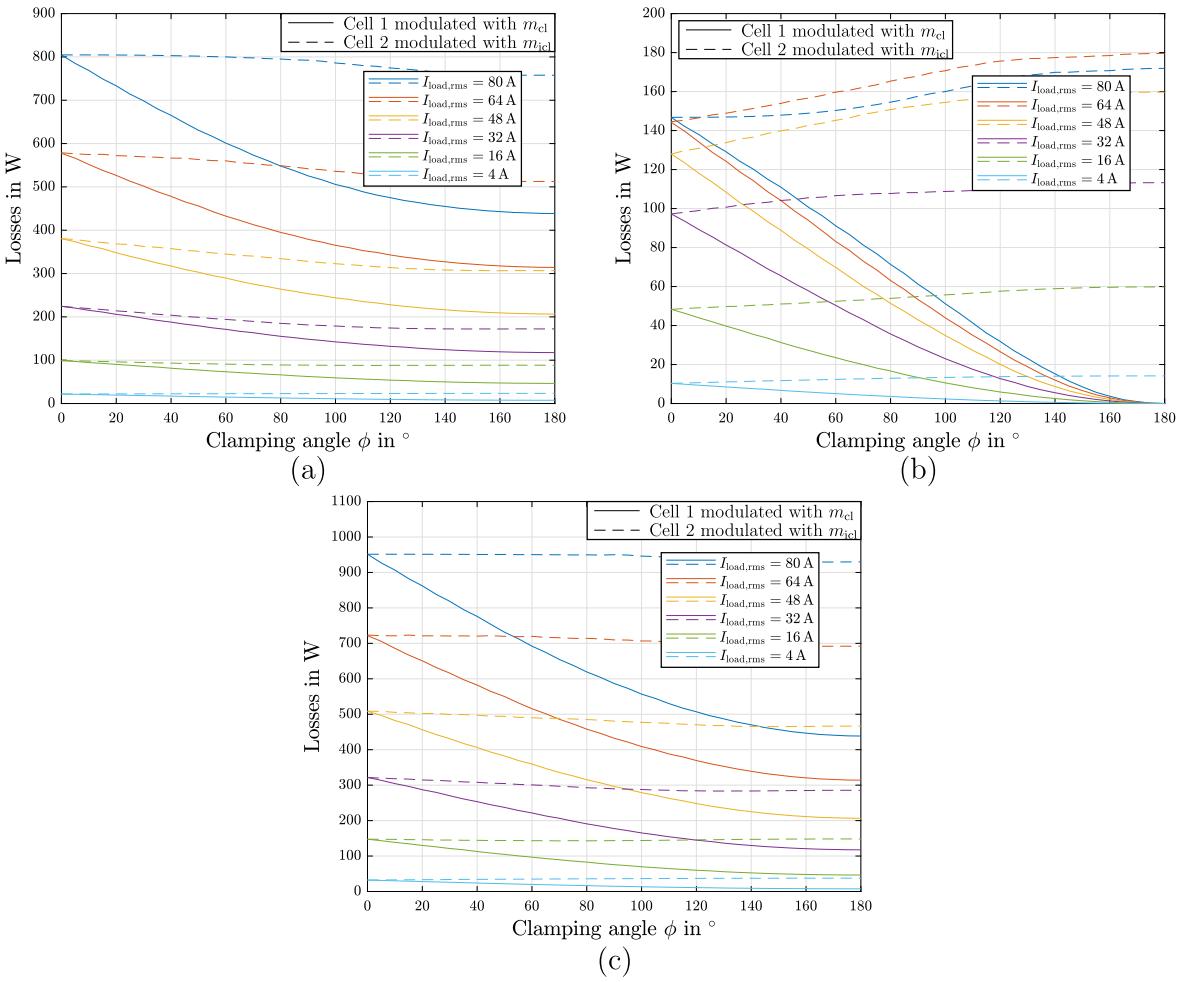


Fig. 5.17: Impact of first harmonic clamped modulation method on the losses of (a) IGBTs, (b) diodes, (c) the sum of both for the clamped operated as well as the inverse clamped operated CHB cell depending on the applied clamping angle ϕ for different load current values.

angles with a lower slope. This is due to the fact that the share of IGBT conduction compared to diode conduction enlarges with increasing clamping angle, which can be seen in the change of diode losses of the clamped operated CHB cell in Fig. 5.17 (b) that are decreasing towards zero for the maximum clamping angle of 180°. Additionally, the reduction of switching losses decreases with higher clamping angles, because the clamping segment enlarges into regions of lower sinusoidal current. The sum of IGBT and diode losses of the clamped CHB cell in Fig. 5.17 (c) also shows a decreasing slope of reduction at higher clamping angles. For the losses of the inverse clamped CHB cell in Fig. 5.17 - dashed lines -, the impact of the first harmonic clamped modulation method on the switching losses is insignificant. The marginal decrease in the sum of IGBT and diode losses of the inverse CHB cell (Fig. 5.17 (c)) is due to an enlargement of the share of diode conduction compared to IGBT conduction, which can be seen in decreasing IGBT losses (Fig. 5.17 (a)) and increasing diode losses (Fig. 5.17 (b)).

The simulated losses of clamped and inverse clamped operated CHB cells depending on the

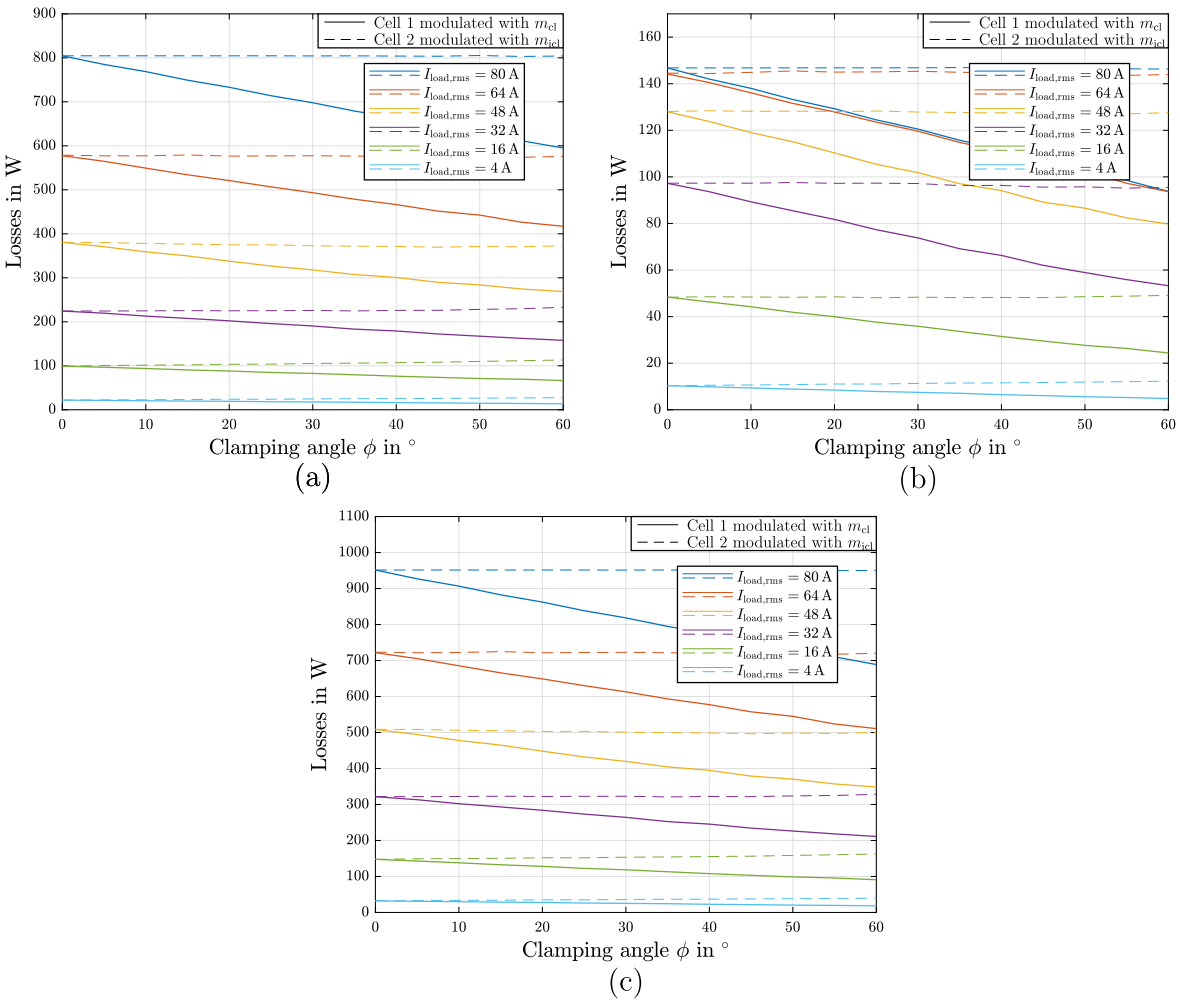


Fig. 5.18: Impact of third harmonic clamped modulation method on the losses of (a) IGBTs, (b) diodes, (c) the sum of both for the clamped operated as well as the inverse clamped operated CHB cell depending on the applied clamping angle ϕ for different load current values.

clamping angle ϕ at different RMS values of the load current $I_{\text{load,rms}}$ are shown in Fig. 5.18 for the third harmonic clamped modulation method. The IGBT losses (Fig. 5.18 (a)) as well as the diode losses (Fig. 5.18 (b)) of the clamped operated CHB cell - solid lines - change due to the reduction of switching events by the clamped angle segment ϕ, while the conduction losses are affected insignificantly, because the two additional angle segments per half wave shown in Fig. 5.14 (a) avoid shifting the share of IGBT conduction compared to diode conduction. The reduction of the sum of IGBT and diode losses (Fig. 5.18 (c)) of the clamped operated CHB cell shows a linear characteristic. The losses of the inverse clamped operated CHB cell in Fig. 5.18 - dashed lines - are affected insignificantly.

Comparing the loss reduction by the first (Fig. 5.17) and third harmonic clamped modulation methods (Fig. 5.18) shows that the potential for loss reduction is similar for the clamping angle segment where both can be operated - ϕ between 0° and 60°. The first harmonic clamped modulation method can reduce the losses further due to the higher possible clamping angle - maximum of ϕ is 180°. However, the impact of applying higher clamping angles on the losses decreases significantly at clamping angles above 100°.

The THD of both methods is also evaluated based on the simulation in Matlab/Simulink with PLECs blockset toolbox. Herein, the THD is calculated with the RMS value of the CHB output voltage $V_{\text{CHB,rms}}$, the dc offset of the CHB output voltage $V_{\text{CHB,dc}}$ - if present -, and the RMS value of the CHB output voltage at the fundamental frequency $V_{\text{CHB,rms,fund}}$ via

$$\text{THD} = \sqrt{\frac{V_{\text{CHB,rms}}^2 - V_{\text{CHB,dc}}^2 - V_{\text{CHB,rms,fund}}^2}{V_{\text{CHB,rms,fund}}^2}} \,. \tag{5.22}$$

The impact on the THD depending on the applied amplitude modulation ratio M_{n} is shown in Fig. 5.19 for the first harmonic clamped modulation method and in Fig. 5.20 for the third

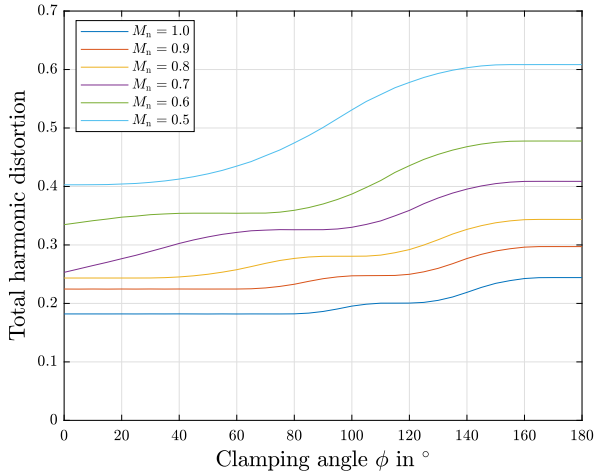


Fig. 5.19: Impact of first harmonic clamped modulation method on the total harmonic distortion of the output voltage depending on the applied clamping angle ϕ for different values of the amplitude modulation ratio M_{n}.

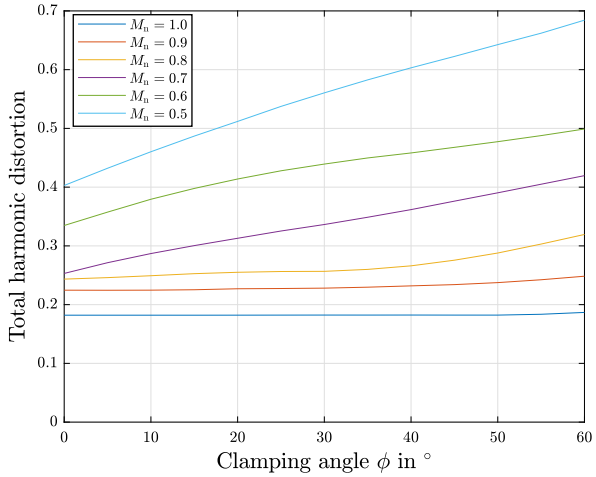


Fig. 5.20: Impact of third harmonic clamped modulation method on the total harmonic distortion of the output voltage depending on the applied clamping angle ϕ for different values of the amplitude modulation ratio M_n.

harmonic clamped modulation method. The first harmonic clamped modulation method is advantageous in terms of the impact on the THD. Especially for lower applied amplitude modulation ratios the first harmonic clamped modulation method provides significantly lower THD values than the third harmonic clamped modulation method. The increased THD values when applying the clamped modulation methods need to be considered for the design of the grid filters [308]. Therefore, application of the third harmonic clamped modulation method would require larger increase of the grid filter design than the first harmonic clamped modulation method.

Next, an analytical comparison of the impact of the clamped modulation methods on the processed power of the CHB cells is carried out. This analytical comparison is based on the approximation of the average processed CHB cell power $\bar{P}_\mathrm{cell}$ by

$$\begin{aligned}\bar{P}_\mathrm{cell} = \frac{1}{2\pi}\int_0^{2\pi} v_\mathrm{cell}(\omega t) i(\omega t)\,\mathrm{d}\omega t \approx \frac{1}{2\pi}\int_0^{2\pi} V_\mathrm{dc} m_\mathrm{cell}(\omega t) I_\mathrm{amp}\cos(\omega t)\,\mathrm{d}\omega t \\ = V_\mathrm{dc} I_\mathrm{amp}\frac{1}{2\pi}\int_0^{2\pi} m_\mathrm{cell}(\omega t)\cos(\omega t)\,\mathrm{d}\omega t\ .\end{aligned} \tag{5.23}$$

Herein, unity power factor is assumed - no phase shift between voltage and current - and switching behavior is neglected. The integral part is symmetrical in all four quarters of the period. Therefore, only the first quarter of the period is used to show the influence of varying the clamping angle on the average processed CHB cell power for first and third harmonic clamped modulation method. The average processed power of the CHB cells is given with $V_\mathrm{dc} I_\mathrm{amp}$ as 1 p.u. in the following.

The average processed power of the CHB cells for applying the first harmonic clamped modulation method can be calculated by using the information about the modulation signal generation from Fig. 5.13. The average processed power of the clamped operated CHB cell

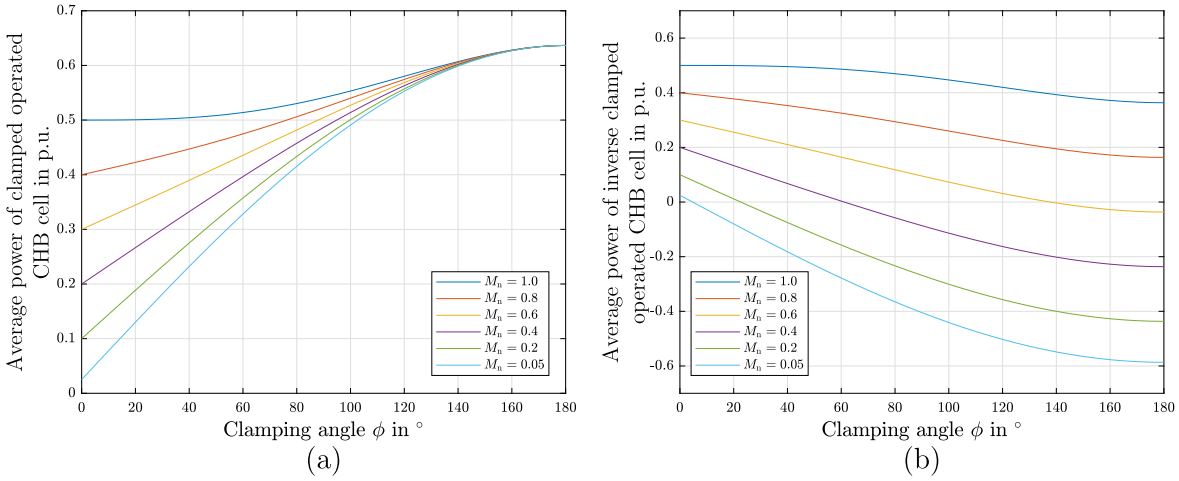


Fig. 5.21: Impact of first harmonic clamped modulation method on the power processed by (a) the clamped operated and (b) the inverse clamped operated CHB cell depending on the applied clamping angle ϕ for different values of the amplitude modulation ratio M_n.

in per unit can be calculated by

$$\frac{2}{\pi}\int_0^{\frac{\pi}{2}} m_\mathrm{cl}(\omega t)\cos(\omega t)\,\mathrm{d}\omega t = \frac{2}{\pi}\left(\int_0^{\frac{\phi}{2}} \cos(\omega t)\,\mathrm{d}\omega t + \int_{\frac{\phi}{2}}^{\frac{\pi}{2}} M_\mathrm{n}\cos^2(\omega t)\,\mathrm{d}\omega t\right) . \tag{5.24}$$

The average processed power of the inverse clamped operated CHB cell in per unit can be calculated by

$$\begin{aligned}\frac{2}{\pi}\int_0^{\frac{\pi}{2}} m_\mathrm{icl}(\omega t)\cos(\omega t)\,\mathrm{d}\omega t = \frac{2}{\pi}\Bigg(&\int_0^{\frac{\phi}{2}} 2M_\mathrm{n}\cos^2(\omega t) - \cos(\omega t)\,\mathrm{d}\omega t \\ &+ \int_{\frac{\phi}{2}}^{\frac{\pi}{2}} M_\mathrm{n}\cos^2(\omega t)\,\mathrm{d}\omega t\Bigg) .\end{aligned} \tag{5.25}$$

The results for evaluating the impact of the chosen clamping angle ϕ of the first harmonic clamped modulation method at different amplitude modulation ratios M_n on the average processed power of the CHB cells are presented in Fig. 5.21. The clamped operated CHB cell power (Fig. 5.21 (a)) increases with the chosen clamping angle and the influence of the amplitude modulation ratio on the processed power decreases until it vanishes at $\phi = 180°$. The inverse clamped operated CHB cell power (Fig. 5.21 (b)) decreases with the chosen clamping angle and even the power flow direction is reversed, if the amplitude modulation ratio is low and a high clamping angle is applied. If the power flow direction of only one of the CHB cells is reversed, power would be circulated in the ST topologies presented in Section 3.1, which should be avoided.

The average processed power of the CHB cells for applying the third harmonic clamped modulation method can be calculated by using the information about the modulation signal generation from Fig. 5.15. The average processed power of the clamped operated CHB cell

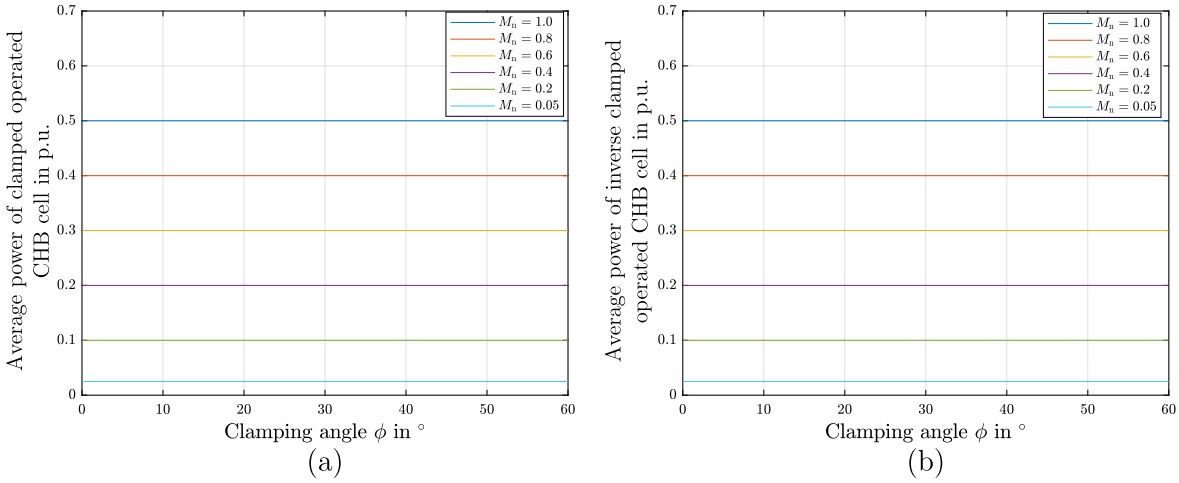


Fig. 5.22: Impact of third harmonic clamped modulation method on the power processed by (a) the clamped operated and (b) the inverse clamped operated CHB cell depending on the applied clamping angle ϕ for different values of the amplitude modulation ratio M_n.

in per unit can be calculated by

$$\begin{aligned}\frac{2}{\pi}\int_0^{\frac{\pi}{2}} m_\mathrm{cl}(\omega t)\cos(\omega t)\,\mathrm{d}\omega t = \frac{2}{\pi}\Bigg(&\int_0^{\frac{\phi}{2}} \cos(\omega t)\,\mathrm{d}\omega t + \int_{\frac{\phi}{2}}^{\frac{\pi}{3}-\frac{\phi}{2}} M_\mathrm{n}\cos^2(\omega t)\,\mathrm{d}\omega t \\ &+ \int_{\frac{\pi}{3}-\frac{\phi}{2}}^{\frac{\pi}{3}+\frac{\phi}{2}} \left(M_\mathrm{n}\cos(\omega t) - \left(1 + M_\mathrm{n}\cos\left(\omega t - \frac{4\pi}{3}\right)\right)\right)\cos(\omega t)\,\mathrm{d}\omega t \\ &+ \int_{\frac{\pi}{3}+\frac{\phi}{2}}^{\frac{\pi}{2}} M_\mathrm{n}\cos^2(\omega t)\,\mathrm{d}\omega t\Bigg)\ .\end{aligned} \tag{5.26}$$

The average processed power of the inverse clamped operated CHB cell in per unit can be calculated by

$$\begin{aligned}\frac{2}{\pi}\int_0^{\frac{\pi}{2}} m_\mathrm{icl}(\omega t)\cos(\omega t)\,\mathrm{d}\omega t = \frac{2}{\pi}\Bigg(&\int_0^{\frac{\phi}{2}} 2M_\mathrm{n}\cos^2(\omega t) - \cos(\omega t)\,\mathrm{d}\omega t \\ &+ \int_{\frac{\phi}{2}}^{\frac{\pi}{3}-\frac{\phi}{2}} M_\mathrm{n}\cos^2(\omega t)\,\mathrm{d}\omega t \\ &+ \int_{\frac{\pi}{3}-\frac{\phi}{2}}^{\frac{\pi}{3}+\frac{\phi}{2}} \left(M_\mathrm{n}\cos(\omega t) + \left(1 + M_\mathrm{n}\cos\left(\omega t - \frac{4\pi}{3}\right)\right)\right)\cos(\omega t)\,\mathrm{d}\omega t \\ &+ \int_{\frac{\pi}{3}+\frac{\phi}{2}}^{\frac{\pi}{2}} M_\mathrm{n}\cos^2(\omega t)\,\mathrm{d}\omega t\Bigg)\ .\end{aligned} \tag{5.27}$$

The results for evaluating the impact of the chosen clamping angle ϕ of the third harmonic clamped modulation method at different amplitude modulation ratios M_n on the average processed power of the CHB cells are presented in Fig. 5.22. It can be seen that the requirement of not affecting the processed power of the CHB cells is fulfilled by the third harmonic clamped modulation method for clamped operated as well as inverse clamped operated CHB cell. Therefore, it is suitable for implementation in the ST topologies presented in Section 3.1

while also power routing - addressed in Section 5.2 - is applied.

The results of the comparison of first and third harmonic clamped modulation method are:

- Both clamped modulation methods have a similar potential for loss reduction for the clamping angle range from 0° to 60° - where both can be operated.
- The first harmonic clamped modulation method provides a wider possible clamping angle range up to 180°, which can provide further loss reduction. However, the impact of applying higher clamping angles on the losses decreases significantly at clamping angles above 100°.
- The first harmonic clamped modulation method provides lower THD than the third harmonic clamped modulation method, which results in lower design of the grid filters.
- The first harmonic clamped modulation method has significant influence on the processed power of the CHB cells and can also cause problems with circulating power in the ST. It is not suitable for implementation at the same time as power routing.
- The third harmonic clamped modulation method has no influence on the processed power of the CHB cells. It is suitable for implementation at the same time as power routing.

5.3.4. Laboratory validation of clamped modulation impact on processed cascaded H-bridge cell power and temperature

The laboratory validation of the clamped modulation methods is carried out on a seven-level CHB laboratory setup, which is shown with the equipment in Fig. 5.23, the used equipment is also listed in Table 5.7. The validation of the impact of the clamped modulation methods on the processed CHB cell power is done by operating the seven-level CHB laboratory setup in active rectifier mode - shown in Fig. 5.24 - and the impact on the temperature of the semiconductors in inverter mode - shown in Fig. 5.16. The parameters used in both operation modes of the setup are listed in Table 5.8.

Table 5.7: Equipment used in the seven-level CHB laboratory setup.

Equipment	Manufacturer	Model
dc voltage source	Elektro Automatik	EA-PSI 81000-30
Digital signal processor	Texas Instruments	TMS320F28379D
Oscilloscope	Tektronix	DPO 4054
Current probes	Tektronix	TCP0030A
Voltage probes	Tektronix	TMDP0200
Optic fiber signal conditioner	Opsens Solutions	PSC-D-N-N-N
Optic fiber temperature sensors	Opsens Solutions	OTG-A

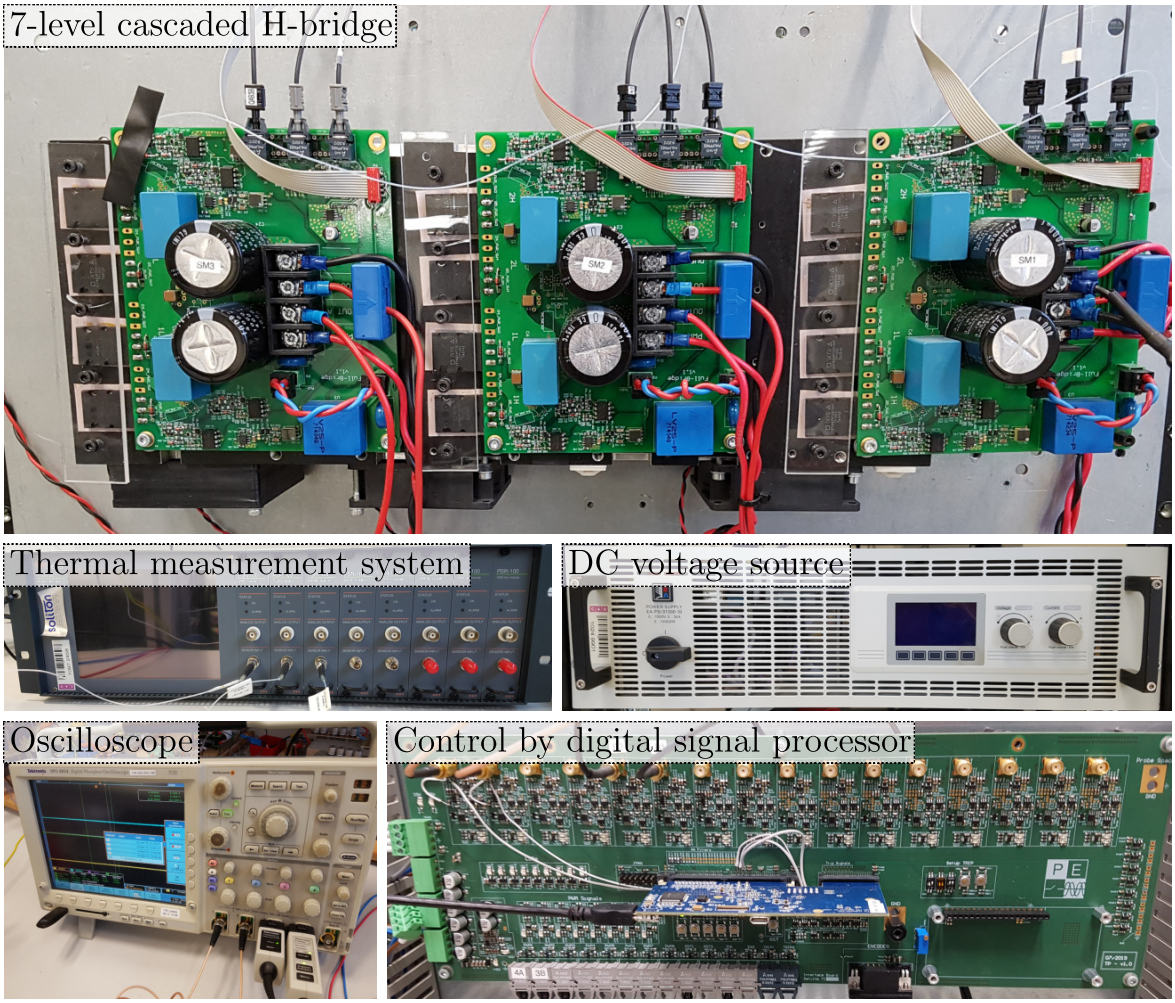


Fig. 5.23: Seven-level CHB laboratory setup and equipment.

For the validation of the impact of the clamped modulation methods on the processed CHB cell power in active rectifier mode, the grid inductance is chosen as $L_g = 7.5\,\text{mH}$ and the load resistors $R_{\text{cell},1}$, $R_{\text{cell},2}$, $R_{\text{cell},3}$ each as $100\,\Omega$. The control of the seven-level CHB laboratory setup in active rectifier mode is shown in Fig. 5.25 and Fig. 5.26. The angular frequency ω of the grid voltage v_{ac} as well as the phase of the voltage ωt are derived via a phase locked loop (PLL) - shown in Fig. 5.26 (a) -, which is based on a second-order generalized integrator (SOGI) [309]. The derived phase ωt, the reference CHB dc voltage V_{dc}^*, and the measured CHB dc voltages $V_{\text{dc},1}$, $V_{\text{dc},2}$, $V_{\text{dc},3}$ are used to give the reference current i^* via the dc voltage control, as shown in Fig. 5.26 (b). The reference current i^* and the measured CHB

Table 5.8: Parameters used in the seven-level CHB laboratory setup.

Symbol	Representation	Value
$V_{\text{dc},1}$, $V_{\text{dc},2}$, $V_{\text{dc},3}$	CHB cell dc voltages	140 V
$C_{\text{cell},1}$, $C_{\text{cell},2}$, $C_{\text{cell},3}$	CHB cell capacities	5 mF
f_{ac}	Fundamental frequency	50 Hz
$f_{\text{sw,CHB}}$	CHB cell switching frequency	20 kHz

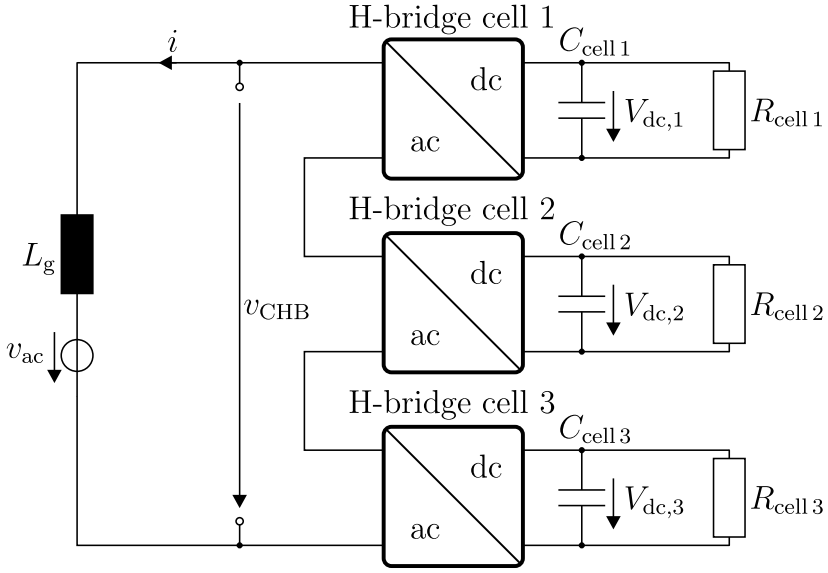


Fig. 5.24: Considered configuration of the seven-level CHB operated in active rectifier mode.

current i are then used to derive the normal modulation signal m_n via the PR current controller [309] - shown in Fig. 5.25. Herein, a start-up feedforward is added at the end, which forwards a fraction of the grid voltage v_{ac} divided by the sum of all CHB cell dc voltages $\sum_{k=1}^{3} V_{dc,k}$ and vanishes after the start-up procedure. Afterwards, the dc voltage balancing control (Fig. 5.26 (c)) compensates inequalities of the CHB dc voltages. The clamped and inverse clamped modulation signals are generated for the first harmonic clamped modulation method according to Fig. 5.27 and for the third harmonic clamped modulation method according to Fig. 5.28. The modulation signals applied to the cells $m_{1,cl}$, $m_{2,icl}$, m_3 are limited afterwards to values between -1 and 1.

The measurement results of the seven-level CHB laboratory setup operated as active rectifier for the application of the first harmonic clamped modulation method are presented in Fig. 5.29. The filtered CHB dc voltages - filtered to clearly see the transient behavior -, measured and reference current, applied clamping angle ϕ, and the modulation signals are shown for a jump of the clamping angle from 0° to 40° (Fig.5.29 (a)), operation with

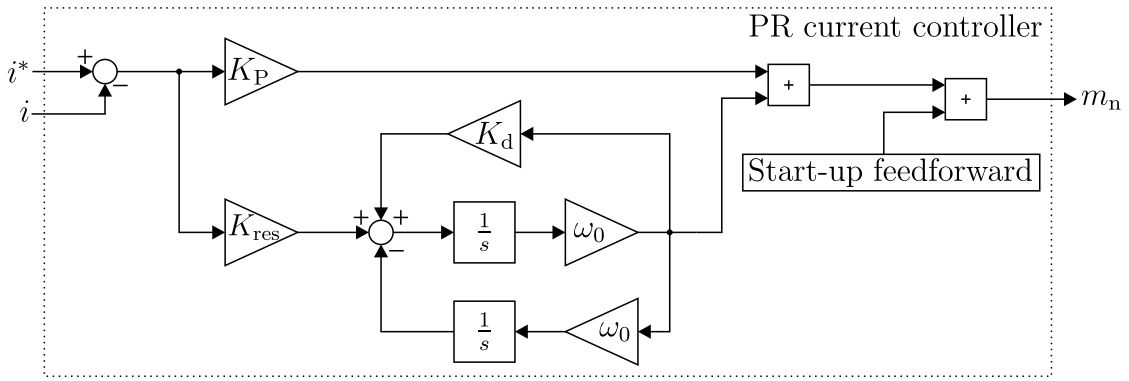


Fig. 5.25: Scheme of the PR current controller used in the seven-level CHB laboratory setup.

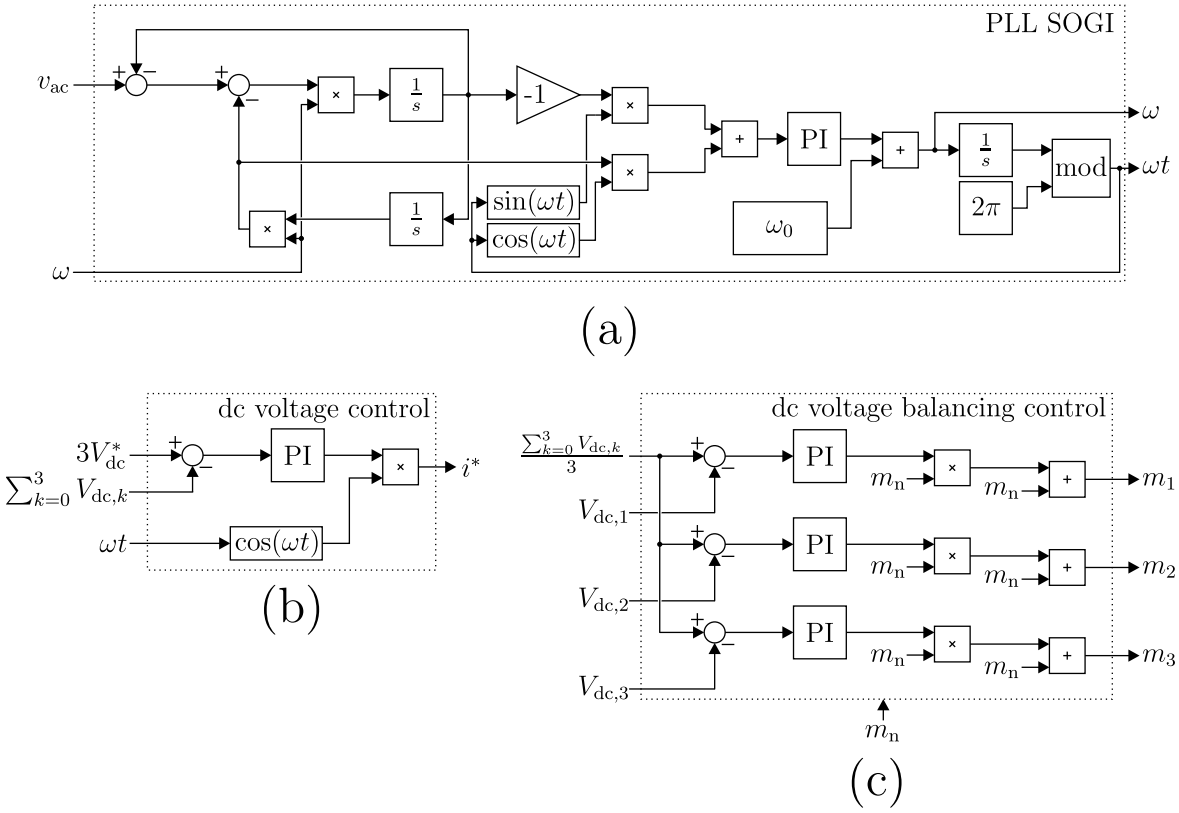
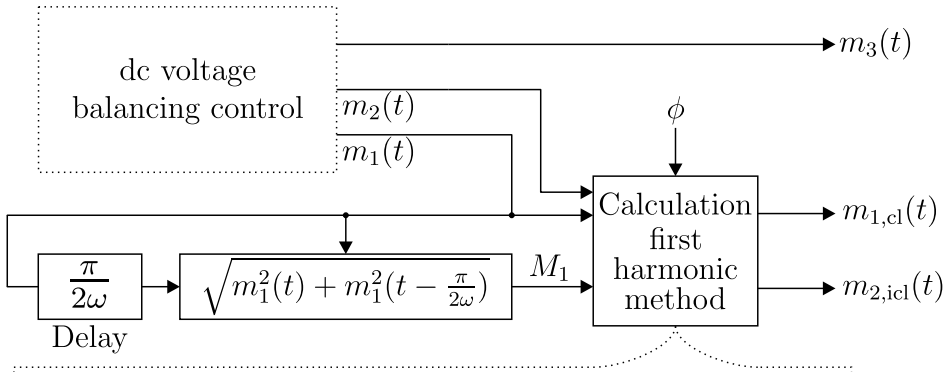


Fig. 5.26: Scheme of the (a) PLL, (b) dc voltage control, and (c) dc voltage balancing control used in the seven-level CHB laboratory setup.

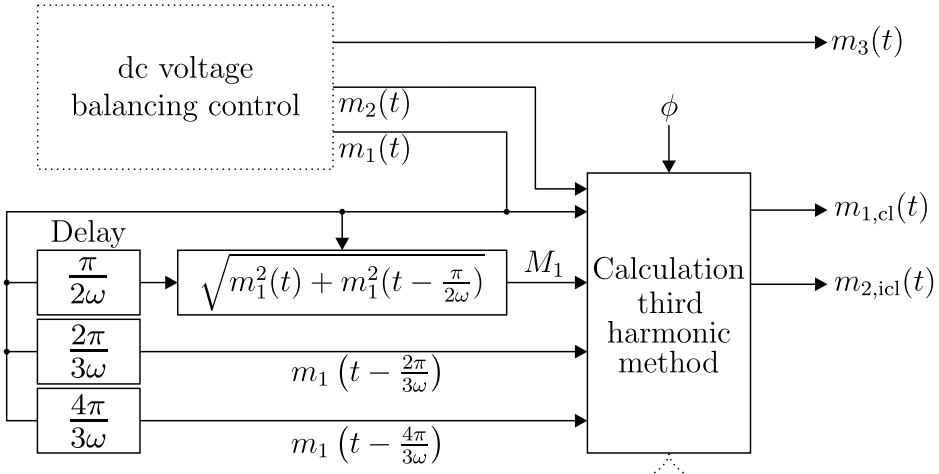
$\phi = 40°$ (Fig.5.29 (b)), and a jump of the clamping angle from 40° to 0° (Fig.5.29 (c)). After the jumps of the clamping angle in Fig.5.29 (a) and (c) transients in the CHB dc voltages can



$$m_{1,\mathrm{cl}}(t) = \begin{cases} 1 & \text{if } m_1(t) \geq M_1 \cos\left(\frac{\phi}{2}\right) \\ -1 & \text{if } m_1(t) \leq -M_1 \cos\left(\frac{\phi}{2}\right) \\ m_1(t) & \text{else} \end{cases}$$

$$m_{2,\mathrm{icl}}(t) = \begin{cases} m_2(t) - (1 - m_1(t)) & \text{if } m_1(t) \geq M_1 \cos\left(\frac{\phi}{2}\right) \\ m_2(t) - (-1 - m_1(t)) & \text{if } m_1(t) \leq -M_1 \cos\left(\frac{\phi}{2}\right) \\ m_2(t) & \text{else} \end{cases}$$

Fig. 5.27: Generation scheme of the modulation signals for first harmonic clamped modulation method of a seven-level CHB in active rectifier mode.



Case 1: $m_1(t) \geq m_1(t-\frac{2\pi}{3\omega}) \wedge m_1(t) \geq m_1(t-\frac{4\pi}{3\omega}) \wedge m_1(t) \geq M_1\cos\left(\frac{\phi}{2}\right)$

Case 2: $m_1(t-\frac{2\pi}{3\omega}) \geq m_1(t) \wedge m_1(t-\frac{2\pi}{3\omega}) \geq m_1(t-\frac{4\pi}{3\omega}) \wedge m_1(t-\frac{2\pi}{3\omega}) \geq M_1\cos\left(\frac{\phi}{2}\right)$

Case 3: $m_1(t-\frac{4\pi}{3\omega}) \geq m_1(t) \wedge m_1(t-\frac{4\pi}{3\omega}) \geq m_1(t-\frac{2\pi}{3\omega}) \wedge m_1(t-\frac{4\pi}{3\omega}) \geq M_1\cos\left(\frac{\phi}{2}\right)$

Case 4: $m_1(t) \leq m_1(t-\frac{2\pi}{3\omega}) \wedge m_1(t) \leq m_1(t-\frac{4\pi}{3\omega}) \wedge m_1(t) \leq -M_1\cos\left(\frac{\phi}{2}\right)$

Case 5: $m_1(t-\frac{2\pi}{3\omega}) \leq m_1(t) \wedge m_1(t-\frac{2\pi}{3\omega}) \leq m_1(t-\frac{4\pi}{3\omega}) \wedge m_1(t-\frac{2\pi}{3\omega}) \leq -M_1\cos\left(\frac{\phi}{2}\right)$

Case 6: $m_1(t-\frac{4\pi}{3\omega}) \leq m_1(t) \wedge m_1(t-\frac{4\pi}{3\omega}) \leq m_1(t-\frac{2\pi}{3\omega}) \wedge m_1(t-\frac{4\pi}{3\omega}) \leq -M_1\cos\left(\frac{\phi}{2}\right)$

$$m_{1,\mathrm{cl}}(t) = \begin{cases} 1 & \text{if Case1} \\ m_1(t) - \left(m_1(t-\frac{2\pi}{3\omega}) - 1\right) & \text{if Case2} \\ m_1(t) - \left(m_1(t-\frac{4\pi}{3\omega}) - 1\right) & \text{if Case3} \\ -1 & \text{if Case4} \\ m_1(t) - \left(1 + m_1(t-\frac{2\pi}{3\omega})\right) & \text{if Case5} \\ m_1(t) - \left(1 + m_1(t-\frac{4\pi}{3\omega})\right) & \text{if Case6} \\ m_1(t) & \text{else} \end{cases}$$

$$m_{2,\mathrm{icl}}(t) = \begin{cases} m_2(t) - (1 - m_1(t)) & \text{if Case1} \\ m_2(t) + \left(m_1(t-\frac{2\pi}{3\omega}) - 1\right) & \text{if Case2} \\ m_2(t) + \left(m_1(t-\frac{4\pi}{3\omega}) - 1\right) & \text{if Case3} \\ m_2(t) - (-1 - m_1(t)) & \text{if Case4} \\ m_2(t) + \left(1 + m_1(t-\frac{2\pi}{3\omega})\right) & \text{if Case5} \\ m_2(t) + \left(1 + m_1(t-\frac{4\pi}{3\omega})\right) & \text{if Case6} \\ m_2(t) & \text{else} \end{cases}$$

Fig. 5.28: Generation scheme of the modulation signals for third harmonic clamped modulation of a seven-level CHB in active rectifier mode.

be seen, which are due to the impact of the first harmonic method on the processed power of the CHB cells. After the jump of the clamping angle from 0° to 40° in Fig.5.29 (a) the dc voltage of the clamped operated CHB cell 1 rises due to the higher processed power while

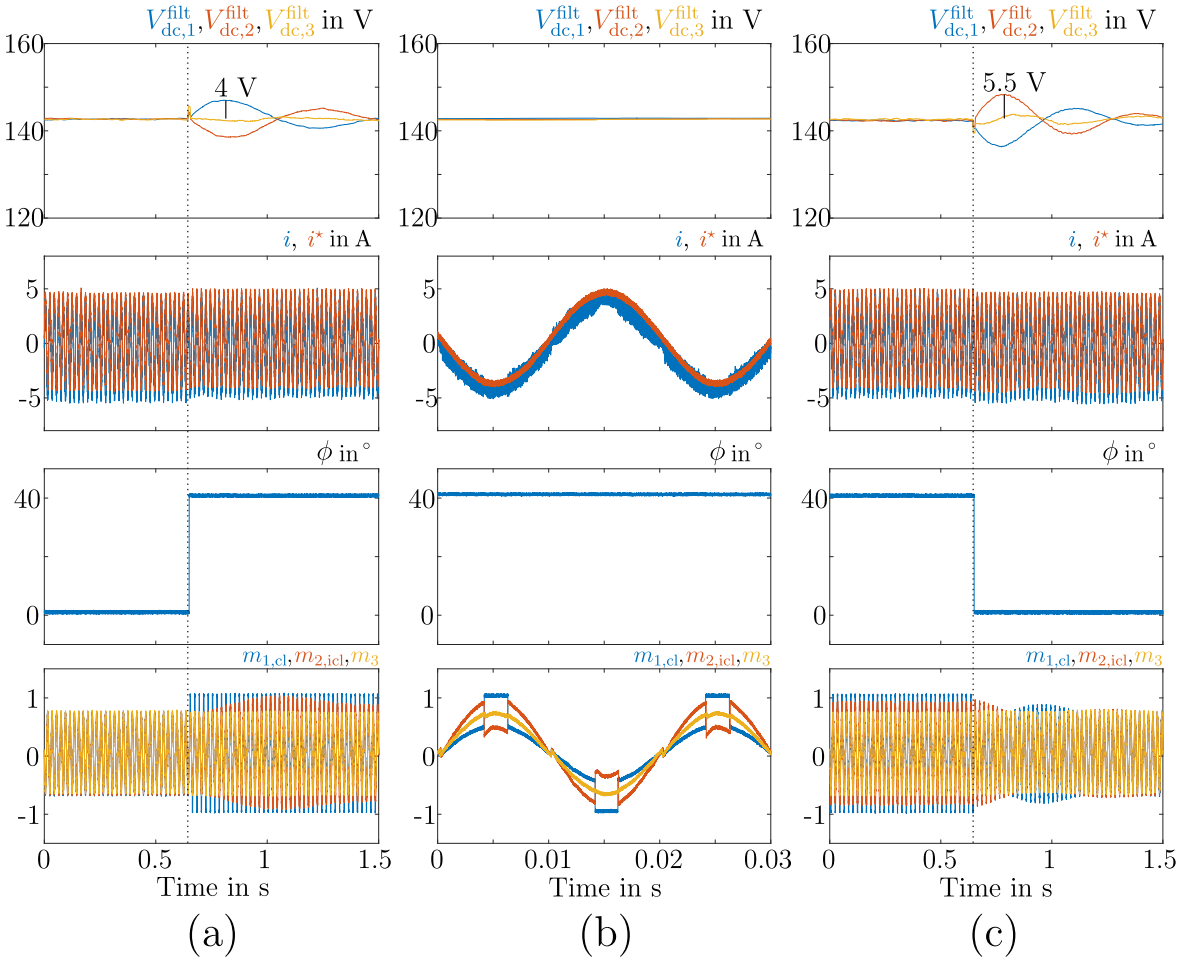


Fig. 5.29: Measurements of filtered cell voltages, CHB current as well as reference current, applied clamping angle and modulation signals with application of first harmonic clamped modulation method during (a) a jump of clamping angle from 0° to 40°, (b) operation with 40°, and (c) a jump of clamping angle from 40° to 0° for operation of the seven-level CHB laboratory setup as active rectifier.

the dc voltage of the inverse clamped operated CHB cell 2 drops due to the lower processed power. Subsequently to the jump, the dc voltage balancing control adjusts the modulation signals m_1, m_2, m_3 to find the new balance for keeping the CHB dc voltages equal. The modulation signals after the balancing can be seen in Fig. 5.29 (b). For the clamped operated CHB cell 1, a low base modulation signal m_1 is necessary and a high base modulation signal m_2 is needed for the inverse clamped operated CHB cell 2. After the jump of the clamping angle from 40° back to 0° the dc voltage of the clamped operated CHB cell 1 drops while the one of the inverse clamped operated CHB cell 2 rises, because the dc voltage balancing control needs to converge back to the base modulation signals without the shift in the processed CHB cell power by the first harmonic clamped modulation.

The measurement results of the seven-level CHB laboratory setup operated as active rectifier for the application of the third harmonic clamped modulation method are presented in Fig. 5.30. It can be seen that neither the jump of the clamping angle from 0° to 40° (Fig. 5.30 (a)) nor the the jump back from 40° to 0° (Fig. 5.30 (c)) affects the CHB dc

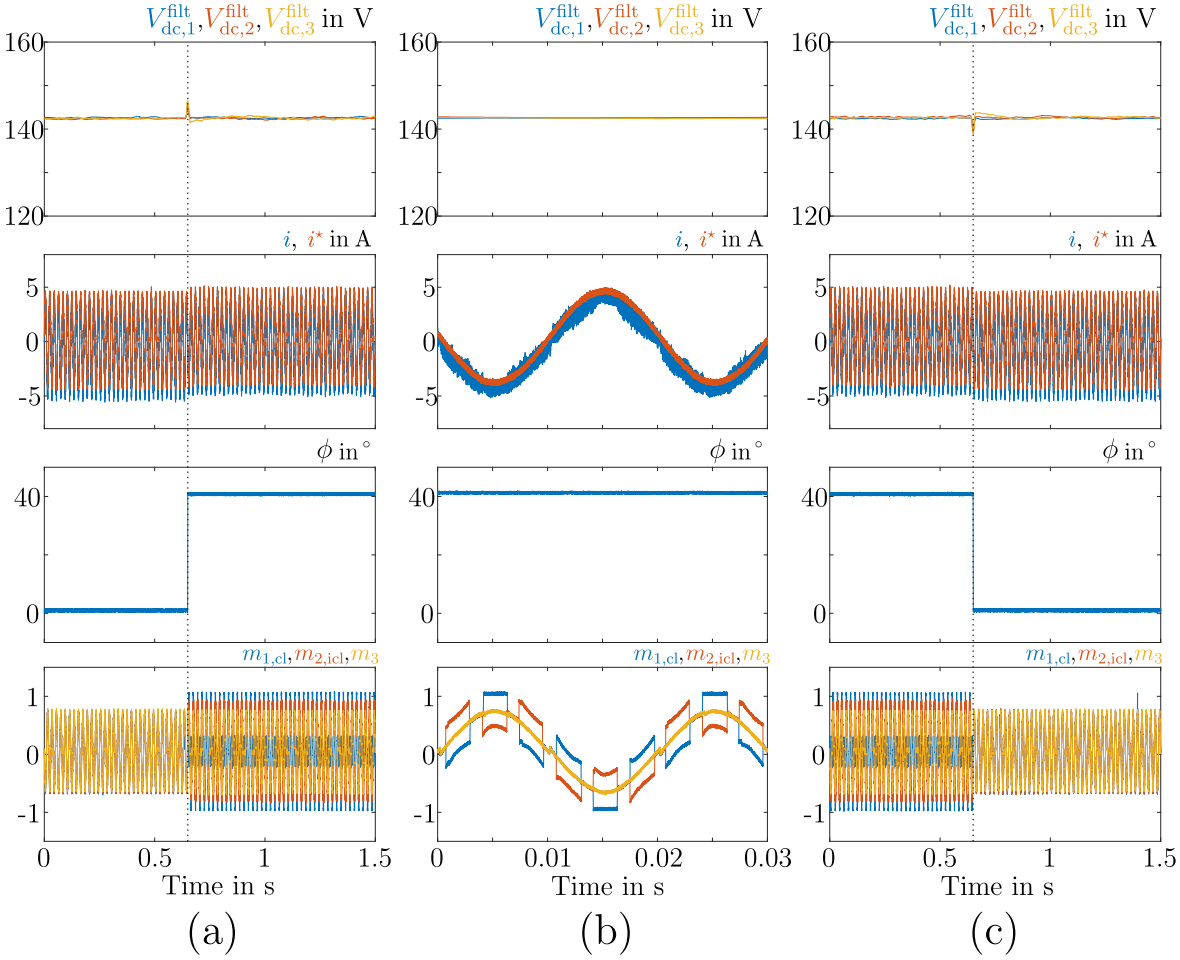


Fig. 5.30: Measurements of filtered cell voltages, CHB current as well as reference current, applied clamping angle and modulation signals with application of third harmonic clamped modulation method during (a) a jump of clamping angle from 0° to 40°, (b) operation with 40°, and (c) a jump of clamping angle from 40° to 0° for operation of the seven-level CHB laboratory setup in active rectifier mode.

voltages, because the third harmonic clamped modulation method has no impact on the processed CHB power. This can also be seen on the parts of the modulation signals that are not changed by the third harmonic clamping method in Fig. 5.30 (b), which are equal for all three modulation signals.

For the validation of the impact of the clamped modulation methods on the temperature of the CHB cell semiconductors in inverter mode, the load inductance is chosen as $L = 0.3\,\mathrm{mH}$ and the load resistor R as $30\,\Omega$. The current control of the seven-level CHB laboratory setup in inverter mode is shown in Fig. 5.25. The reference current i^* is given as a sinusoidal function with a frequency of 50 Hz and an amplitude of I^*_{amp}. The clamped and inverse clamped modulation signals are generated for the first harmonic clamped modulation method according to Fig. 5.13 and for the third harmonic clamped modulation method according to Fig. 5.15.

The measured and reference current, the applied clamping angle ϕ, and the clamped and

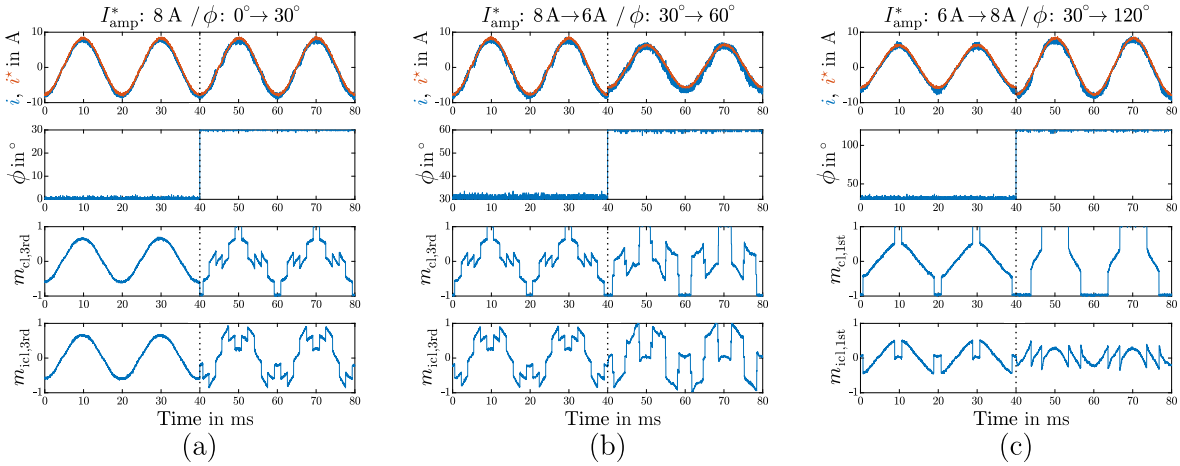


Fig. 5.31: Measurements of CHB current as well as reference current, applied clamping angle and clamped modulation signals during (a) a jump of clamping angle from 0° to 30°, (b) a jump of reference current amplitude from 8 A to 6 A and clamping angle from 30° to 60° with application of third harmonic clamped modulation method, and (c) a jump of reference current amplitude from 6 A to 8 A and clamping angle from 30° to 120° with application of first harmonic clamped modulation method for operation of the seven-level CHB laboratory setup in inverter mode.

inverse clamped modulation signals for operation of the seven-level CHB laboratory setup as inverter are presented in Fig. 5.31. The control is able to follow the reference current for the jumps of reference current amplitude and clamping angle in case of the third harmonic clamped modulation method in Fig. 5.31 (a) and (b) as well as in the case of the first harmonic clamped modulation method in Fig. 5.31 (c). The semiconductor temperatures are measured on the pin of discrete packed IGBTs in the clamped operated as well as the inverse clamped operated CHB cell. The considered IGBTs are in the same position within the CHB cell circuit. For the thermal measurements, the load power at a load current amplitude of $I^*_{amp} = 8\,A$ is considered as 100 %. The measurement of the clamped operated CHB cells IGBT

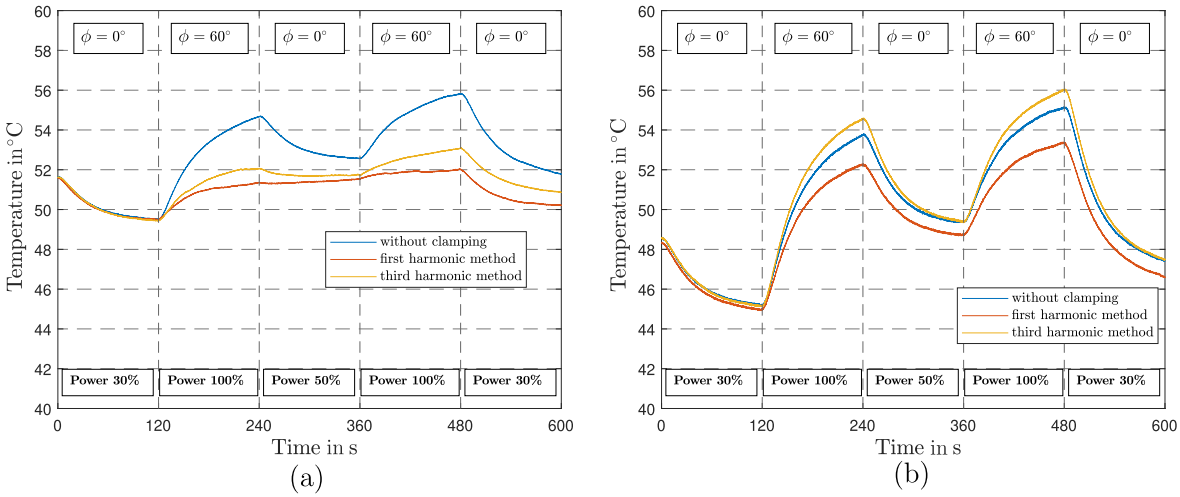


Fig. 5.32: Measurements of IGBT temperatures without and with application of first and third clamped modulation method for (a) the clamped operated cell and (b) the inverse clamped operated cell of the seven-level CHB laboratory setup in inverter mode.

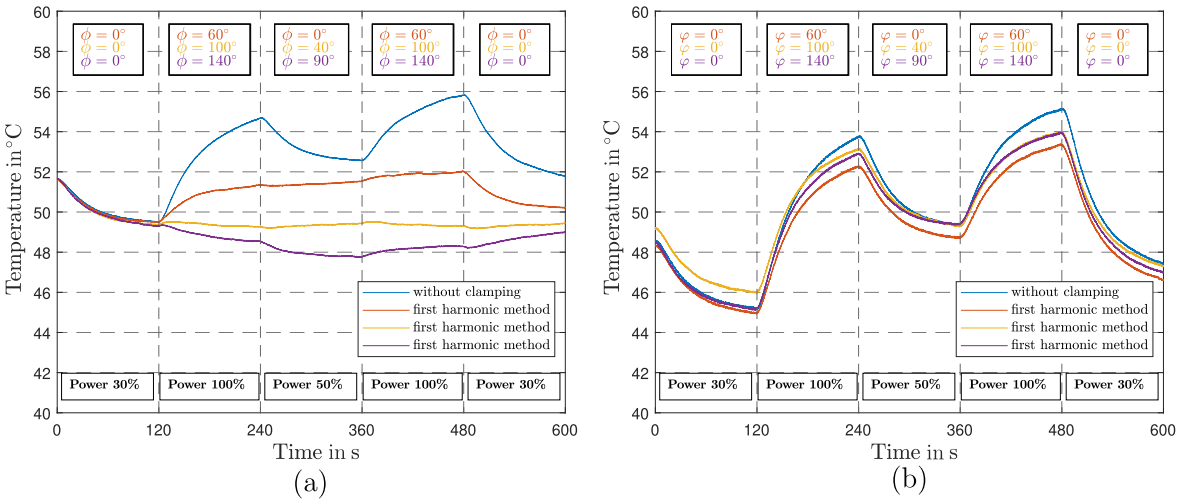


Fig. 5.33: Measurements of IGBT temperatures without and with application of first clamped modulation method for (a) the clamped operated cell and (b) the inverse clamped operated cell of the seven-level CHB laboratory setup in inverter mode.

temperature in Fig. 5.32 (a) validates the possibility to influence the temperatures via the losses adaption by the clamped modulation methods. It can be seen that it is possible to reduce the thermal swings on the IGBT of the clamped operated cell significantly. The impact of the clamped modulation methods on the IGBT temperature of the inverse clamped operated CHB cell in Fig. 5.32 (b) is minor. The thermal swings on the IGBT of the inverse clamped operated CHB cell are unaffected by the clamped modulation methods. The wider possible clamping angle range of the first harmonic method can be used to further influence the temperature, as it can be seen in Fig. 5.33. It is possible to apply a clamping angle sequence that keeps the IGBT temperature of the clamped operated CHB cell at a constant level - yellow line in Fig. 5.33 (a). However, applying higher clamping angles than in this sequence would lead to a new inserted thermal swing - violet line in Fig. 5.33 (a).

The results of the presented experiments on the seven-level CHB laboratory setup are:

- The impact of the first harmonic clamped modulation method on the processed CHB cell power has been validated.
- It has been validated that the third harmonic clamped modulation method does not affect the processed power of the CHB cells.
- The ability of both clamped modulation methods to influence the temperature and reduce thermal swings of the IGBTs in the clamped operated CHB cell has been validated.
- It has been validated that the wider clamping angle range of the first harmonic clamped modulation method can reduce the thermal swings further compared to the third harmonic clamped modulation.

5.4. Design for failure tolerance of hybrid grids-feeding STs via passive power routing

This section proposes using the possibility of the IT - presented in Section 3.1 - to provide lower loading on the interconnecting DAB depending on its configuration via the link ratio ξ for increasing the failure-tolerance of the ST, instead of applying maximum power converter downsizing - as presented in Section 3.2. The mission profile-based failure analysis carried out in this section considers cases of internal converter failures in the ST and their impact on the possible operation points. Herein, solely the removal of the power capability of the failed converters is considered. The identification of the failures and isolation of the failed converters from the system [310] is out of the scope of this work.

In this section, the considered failure cases and the structure of NIT and IT for the mission profile-based failure analysis are presented at first. Next, the impact of MVac PEBB failures on the possible operation points of the mission profiles is investigated for NIT as well as the considered link ratio configurations of the IT. Afterwards, the impact of modular LVdc and interconnecting DAB PEBB failures on the possible operation points of the mission profiles are examined and the opportunity for additional failure tolerance for a modular interconnecting DAB is revealed, which can also be combined with downsizing of the interconnecting DAB.

5.4.1. Considered failure cases and structure of the hybrid grids-feeding ST

The considered structure of NIT and IT for the mission profile-based failure analysis is similar to the one considered in Chapter 3. A three phase CHB converter with 15 cells in each phase is considered, resulting in 45 MVac PEBBs in total. However, the LVdc converter in the NIT as well as the interconnecting converter in the IT are considered as modular converters composed of 3 IPOP connected DABs. A design of the power converter rating based on the mission profile-based design procedure presented in Section 3.2 without adding safety margins is assumed for the case without failures of power converters. The opportunity for

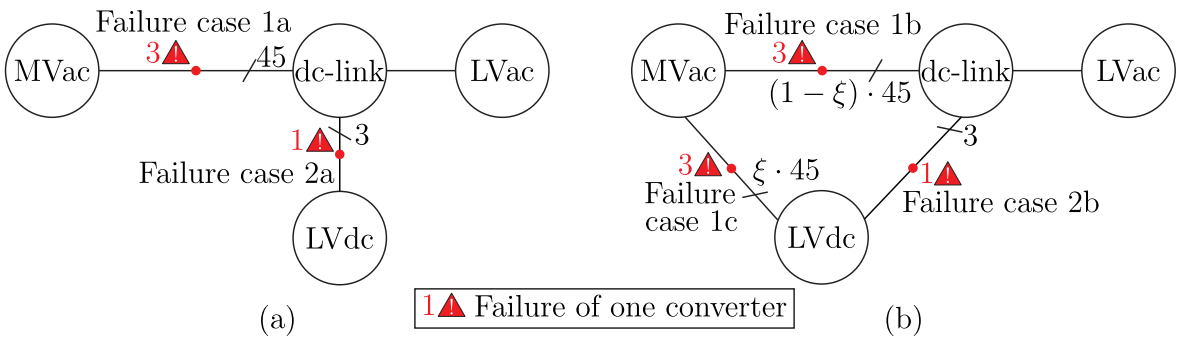


Fig. 5.34: General graphs of (a) NIT and (b) IT with considered internal failure cases.

downsizing the interconnecting converter in the IT compared to the LVdc converter in the NIT is omitted initially - interconnecting converter power rating is set equal to the one of the LVdc converter.

The considered failure cases for NIT and IT are presented in Fig. 5.34. The failure cases 1 consider a failure of three MVac PEBBs - one in each phase. While for the NIT this only results in the failure case 1a, multiple failure cases arise for the IT due to the dc-multibus structure of the MVac PEBBs. For the IT, failures of the MVac PEBBs do not only change the border of the operation area due to the power rating of the MVac PEBBs, but also the link ratio of the IT, which impacts the borders implied by the power rating of the interconnecting converter. The extreme cases for this change of the link ratio are the failure cases 1b and 1c, where only MVac PEBBs connected to the dc-link or only MVac PEBBs connected to the LVdc feeder fail. The failure cases 2 consider a failure of one of the three IPOP connected DABs of the LVdc converter (failure case 2a) or the interconnecting converter (failure case 2b).

5.4.2. Impact of MVac power electronics building block failures on possible operation points

The failure case 1a of the NIT and the failure cases 1b and 1c of the IT result in the same percentages of missed operation points - independent of the link ratio configuration of the IT - for the hybrid mission profiles presented in Fig. 3.7 of Section 3.2. However, the link ratio configuration of the IT can have an impact on the missed operation points for reduced utilization of the LVdc grid. Therefore, the hybrid mission profiles with LVdc power profiles

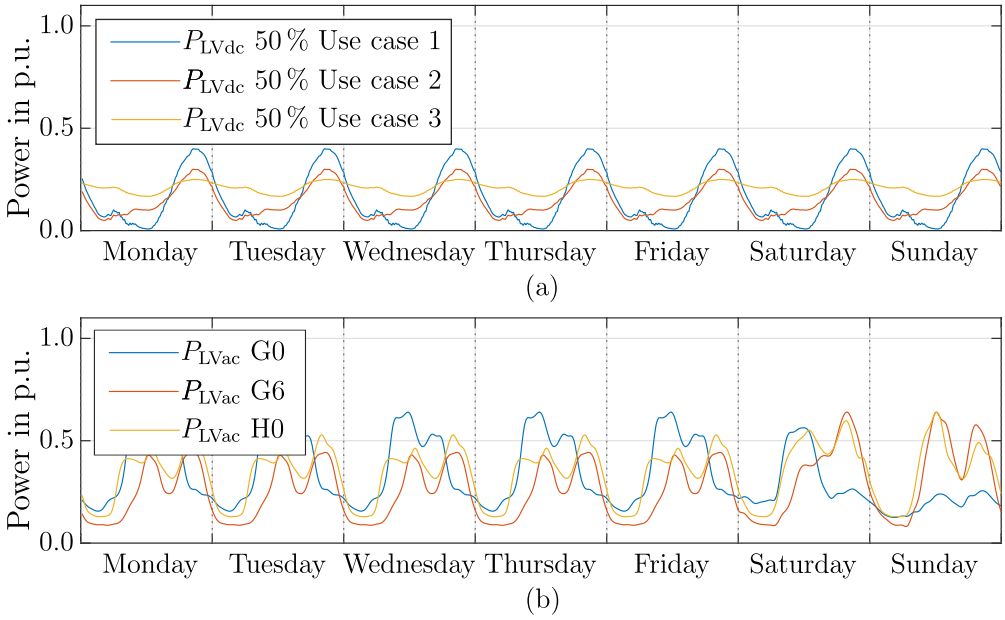


Fig. 5.35: Considered load profiles for (a) LVdc grid, reduced to 50 %, and (b) the LVac grid.

reduced to 50 % - shown in Fig. 5.35 - are used for the mission profile-based analysis of MVac PEBB failures.

The missed operation points due to the failure cases 1 for the nine combinations of LVac and LVdc power profiles from Fig. 5.35 are shown in Fig. 5.36 and Fig. 5.37 for the considered link ratio ξ configurations of the IT. For the NIT, operation points of the hybrid mission profiles are only missed due to the removal of power capability in the MVac PEBBs due to the failed converters. For medium to low link ratios of the IT, also only those operation points that are missed for the NIT cannot be operated anymore for failure cases 1b and 1c. However, for high link ratios of the IT, additional operation points of the hybrid mission profiles are missed due to the changing link ratio and its impact on the operation area borders by the interconnecting converter power rating. It can be seen that the failure case 1b, which

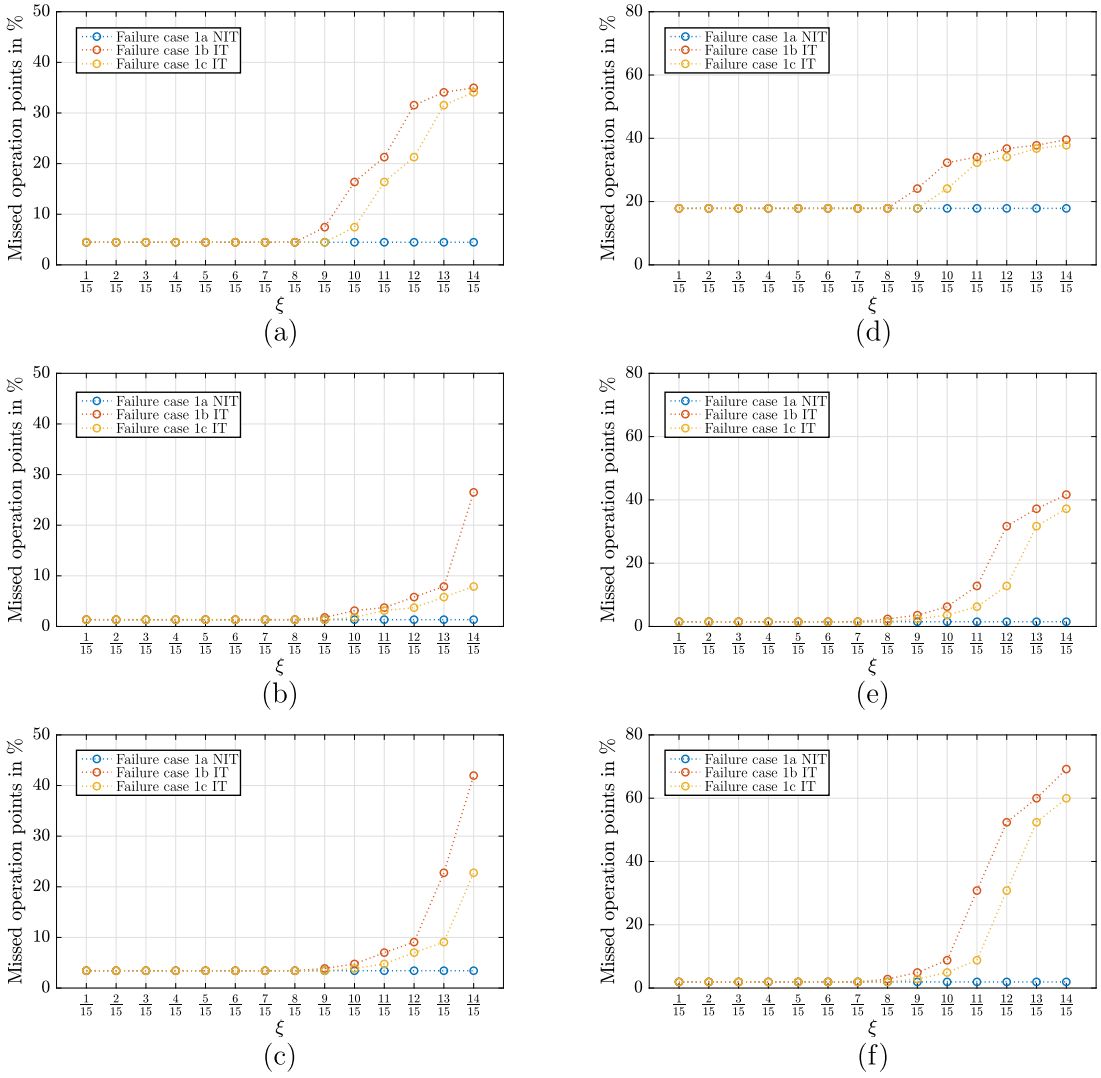


Fig. 5.36: Missed operating points for failure cases 1 for (a) G0 LVac and 50 % of Use case 1 LVdc power profiles, (b) G6 LVac and 50 % of Use case 1 LVdc power profiles, (c) H0 LVac and 50 % of Use case 1 LVdc power profiles, (d) G0 LVac and 50 % of Use case 2 LVdc power profiles, (e) G6 LVac and 50 % of Use case 2 LVdc power profiles, and (f) H0 LVac and 50 % of Use case 2 LVdc power profiles.

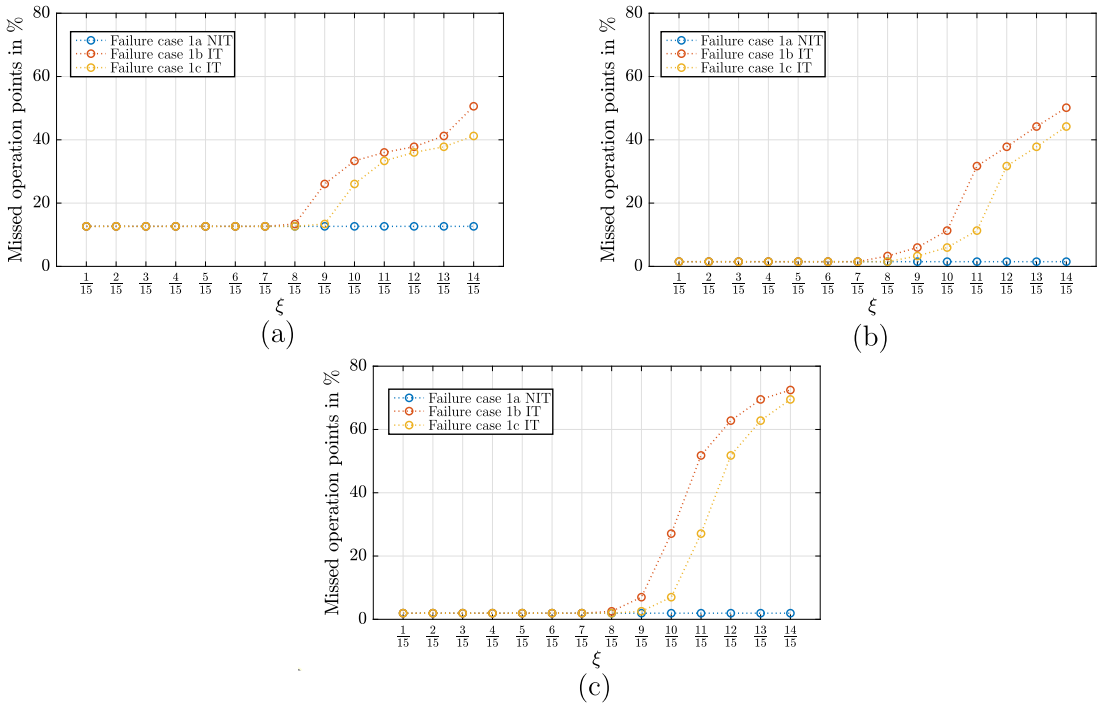


Fig. 5.37: Missed operating points for failure cases 1 for (a) G0 LVac and 50 % of Use case 3 LVdc power profiles, (b) G6 LVac and 50 % of Use case 3 LVdc power profiles, and (c) H0 LVac and 50 % of Use case 3 LVdc power profiles.

increases the link ratio of the IT, leads to more missed operation points than failure case 1c, which decreases the link ratio. It must be noted that for high link ratios of the IT, the total missed operation points are composed by those missed additionally due to the failure cases and those missed because the initial design with the LVdc converter power rating for the interconnecting converter is not sufficient to realize all operation points in the IT - even without failures.

The results of the mission profile-based analysis of MVac PEBB failures are:

- A proper design of the IT configuration via the link ratio is also important in case of MVac PEBB converter failures.
- A sufficient choice of ξ can avoid disadvantages of the IT compared to the NIT in terms of operation points that cannot be reached without overloading the remaining converters after MVac PEBB failures.

5.4.3. Impact of modular LVdc and interconnecting dual active bridge power electronics building block failures on possible operation points

The failure cases 2 are analyzed for the hybrid mission profiles presented in Fig. 3.7 of Section 3.2 at first and afterwards for the hybrid mission profiles with reduced LVdc utilization shown in Fig. 5.35. For each of the considered hybrid mission profiles, it is possible to find a

link ratio configuration of the IT which provides additional failure tolerance for the modular IPOP connected interconnecting converter, which means that one of the three DABs can fail without excluding any operation point of the mission profiles. Furthermore, for the link ratios that provide additional failure tolerance, it is still possible to downsize the interconnecting converter without losing the additional failure tolerance.

The results of the mission profile-based failure analysis of the failure cases 2 for the hybrid mission profiles presented in Fig. 3.7 of Section 3.2 are shown in Fig. 5.38 and Fig. 5.39. For link ratios between $\frac{4}{15}$ and $\frac{10}{15}$, the IT provides additional failure tolerance of the interconnecting converter for each of these hybrid mission profiles. The advantage of using the IT is especially high for those hybrid mission profiles involving the LVdc Use case 3 power pro-

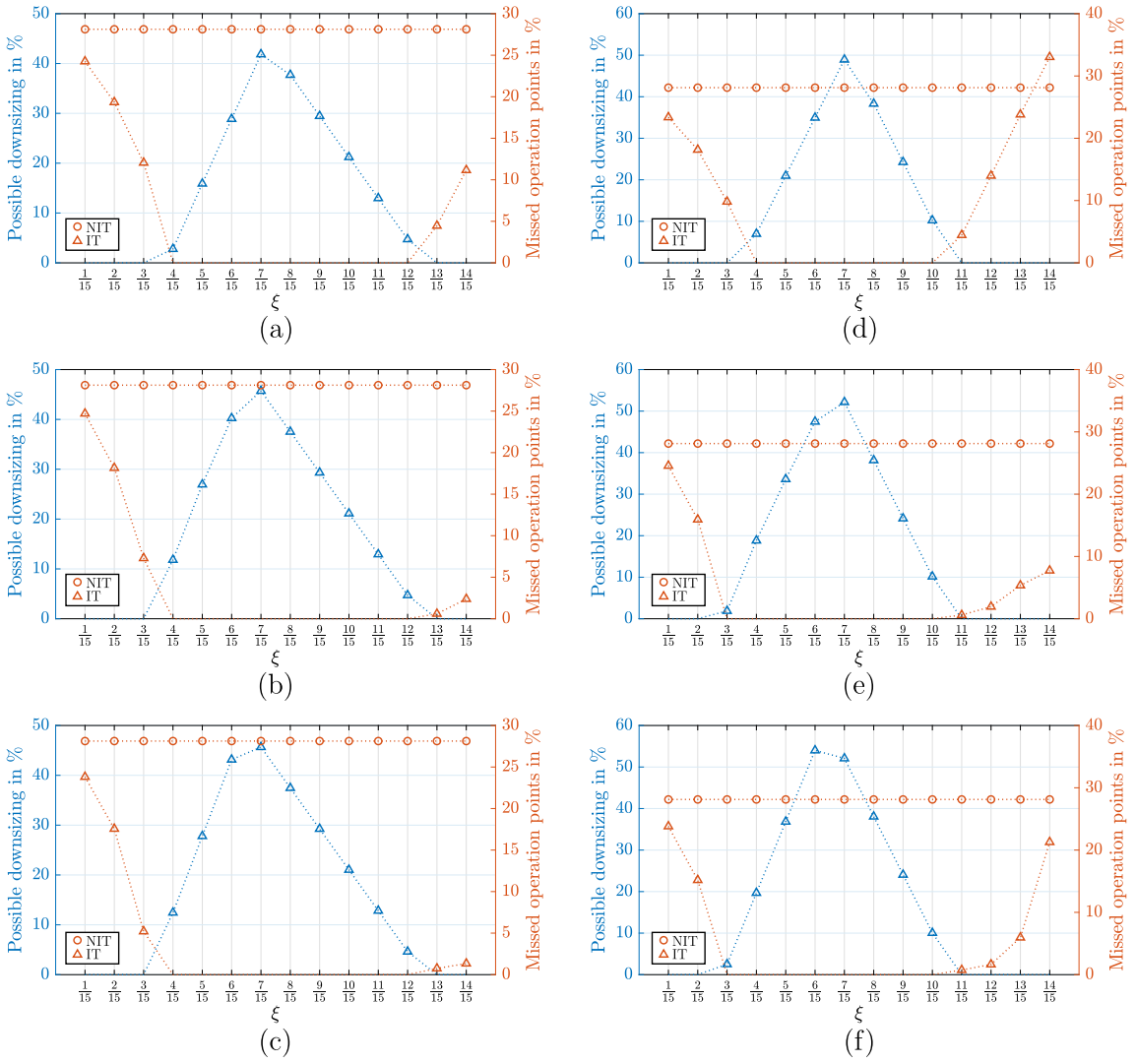


Fig. 5.38: Missed operating points for failure cases 2a and 2b with possible downsizing of interconnecting DABs while additional failure tolerance is maintained for (a) G0 LVac and Use case 1 LVdc power profiles, (b) G6 LVac and Use case 1 LVdc power profiles, (c) H0 LVac and Use case 1 LVdc power profiles, (d) G0 LVac and Use case 2 LVdc power profiles, (e) G6 LVac and Use case 2 LVdc power profiles, and (f) H0 LVac and Use case 2 LVdc power profiles.

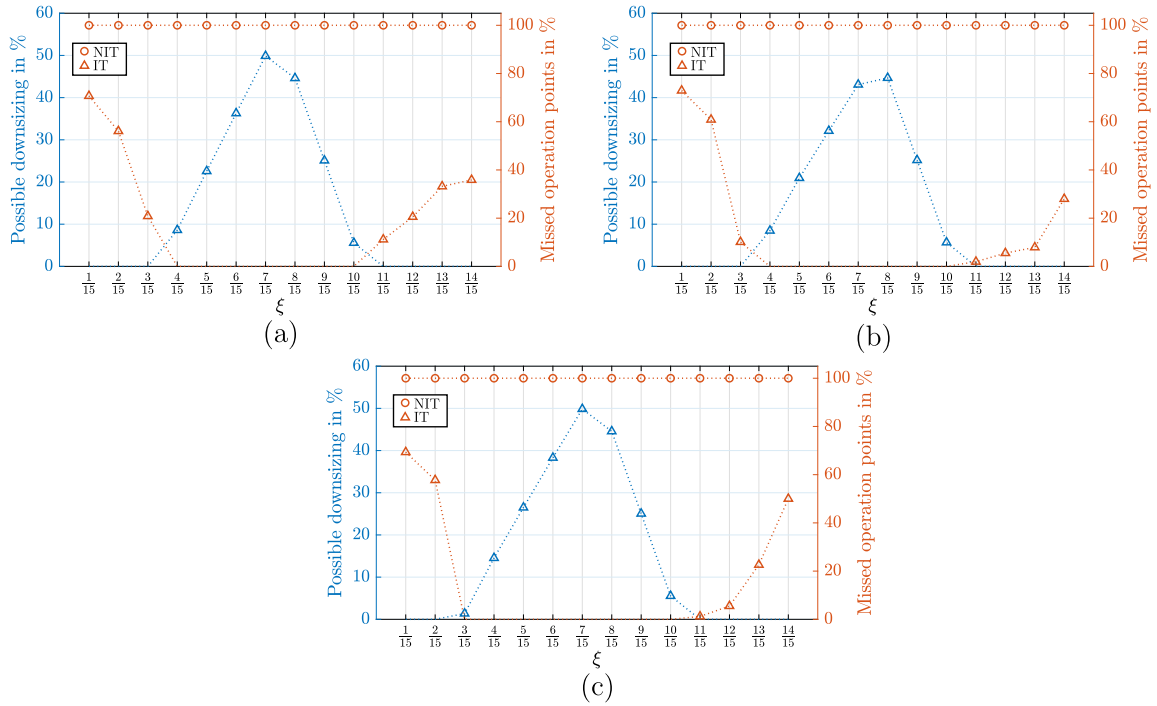


Fig. 5.39: Missed operating points for failure cases 2a and 2b with possible downsizing of interconnecting DABs while additional failure tolerance is maintained for (a) G0 LVac and Use case 3 LVdc power profiles, (b) G6 LVac and Use case 3 LVdc power profiles, and (c) H0 LVac and Use case 3 LVdc power profiles.

file (Fig. 5.39), which contains a constant base load. Whereas the NIT cannot operate at any operation point anymore, the IT with appropriate link ratio choice can operate all operation points of these hybrid mission profiles.

Furthermore, besides the additional failure tolerance of the interconnecting converter, part of the downsizing - proposed in Section 3.2 - can still be applied. The possible downsizing is given in percentage of the the LVdc converter power rating without converter failure. A possible downsizing of 40 % means that the interconnecting converter rating without converter failure only needs to be 60 % of the LVdc converter rating without converter failure in order to still ensure the availability of all operation points of the hybrid mission profile in failure case 2b. For the combination of H0 LVac and Use case 2 LVdc power profiles, only applying a downsizing of 54 % - instead of the maximum possible 69 % presented in Section 3.2 - includes additional failure tolerance of the interconnecting converter, if the optimal link ratio is chosen for the IT. For each of these hybrid mission profiles, a downsizing of at least 40 % is possible while also additional failure tolerance of the interconnecting converter is provided.

The results of the mission profile-based failure analysis of the failure cases 2 for the hybrid mission profiles with reduced LVdc utilization presented in Fig. 5.35 are shown in Fig. 5.40 and Fig. 5.41. Also for lower LVdc grid utilization than before, the IT is able to provide additional failure tolerance for each of the considered hybrid mission profiles. With lower

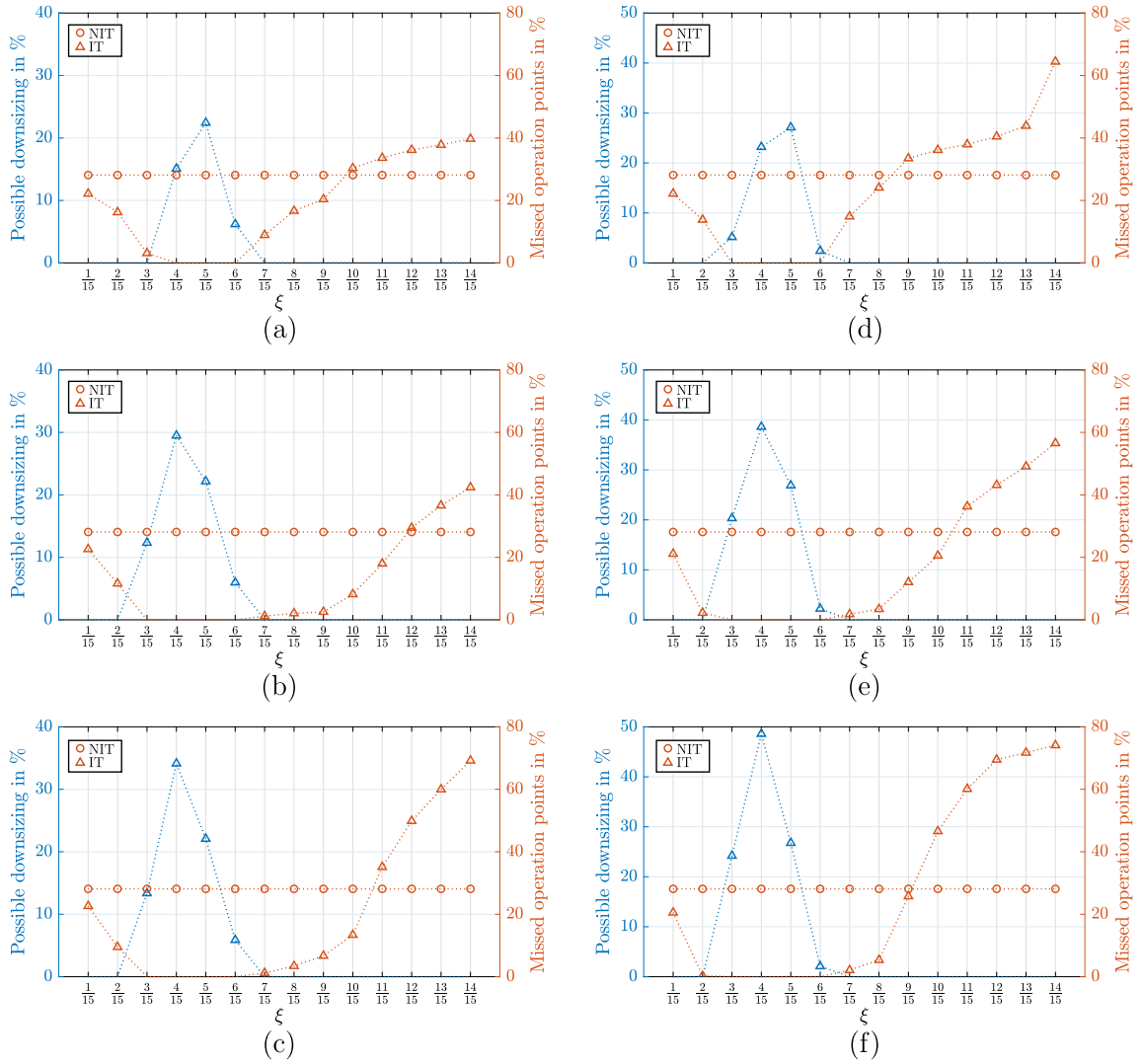


Fig. 5.40: Missed operating points for failure cases 2a and 2b with possible downsizing of interconnecting DABs while additional failure tolerance is maintained for (a) G0 LVac and 50 % of Use case 1 LVdc power profiles, (b) G6 LVac and 50 % of Use case 1 LVdc power profiles, (c) H0 LVac and 50 % of Use case 1 LVdc power profiles, (d) G0 LVac and 50 % of Use case 2 LVdc power profiles, (e) G6 LVac and 50 % of Use case 2 LVdc power profiles, and (f) H0 LVac and 50 % of Use case 2 LVdc power profiles.

LVdc grid utilization than before, the link ratio range providing additional failure tolerance of the interconnecting converter shifts to lower values than before - approximately to link ratios between $\frac{3}{15}$ and $\frac{6}{15}$. For the combination of H0 LVac and 50 % of Use case 2 LVdc power profiles, applying a downsizing of 49 % still includes additional failure tolerance of the interconnecting converter, if the optimal link ratio is chosen for the IT. For each of these hybrid mission profiles with reduced LVdc grid utilization, a downsizing of at least 20 % is possible while also additional failure tolerance of the interconnecting converter is provided. Choosing the link ratios for optimal possible downsizing besides the failure tolerance of the interconnecting converter, also ensures that the failure cases 1b and 1c of MVac PEBBs in the IT do not exclude more operation points than the failure case 1a in the NIT (Fig. 5.36 and Fig. 5.37).

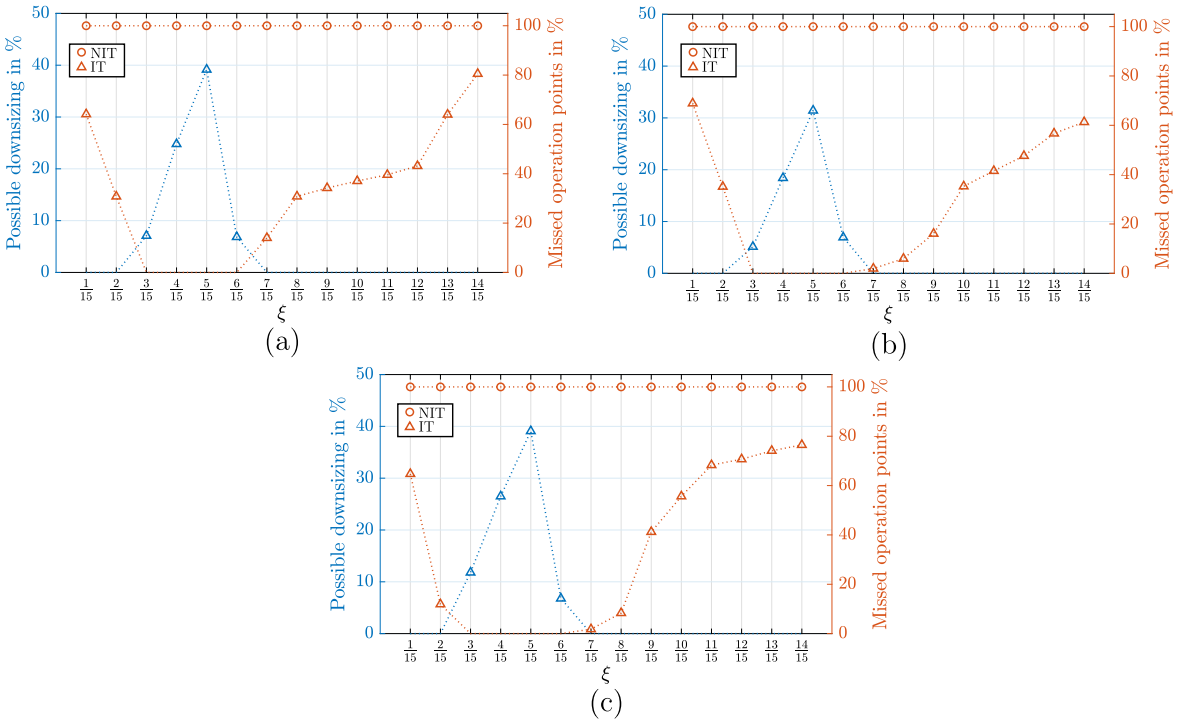


Fig. 5.41: Missed operating points for failure cases 2a and 2b with possible downsizing of interconnecting DABs while additional failure tolerance is maintained for (a) G0 LVac and 50 % of Use case 3 LVdc power profiles, (b) G6 LVac and 50 % of Use case 3 LVdc power profiles, and (c) H0 LVac and 50 % of Use case 3 LVdc power profiles.

The results of the mission profile-based analysis of LVdc and interconnecting converter failures are:

- The possibility of the IT to lower the loading on the interconnecting converter depending on its configuration via the link ratio ξ can also be used to add failure tolerance via redundancy to the hybrid grids-feeding ST.
- Furthermore, the interconnecting converter can still be downsized by up to 54 % for the considered hybrid mission profiles while additional failure tolerance is provided.
- A special case are hybrid mission profiles with constant base load in the LVdc power profile, where the IT can provide failure tolerance, whereas the NIT is not able to operate at any operation point in the considered failure case.

5.5. Summary and conclusions of the chapter

At first, this chapter gave an overview on active thermal control (ATC) methods used in power electronics systems in Section 5.1. There are four main challenges which are addressed by articles on ATC methods for power electronics systems, which are: increasing the overload capability of power electronics converters, thermal cycle reduction of power devices in power electronics converters, balancing thermal stress of power devices within

specific topologies or for parallel power devices, and controlling thermal stress of devices in different building blocks in modular and redundant power electronics systems as well as on a microgrid level. The potential objectives of applying the ATC methods within these four main challenges have been presented as well.

Thereafter, these potential objectives were used to evaluate the capabilities of the different ATC methods for application in the ST. The objectives linked to the challenge of controlling thermal stress of devices in different building blocks in modular and redundant power electronics systems were identified as highly relevant for supporting a reliable ST operation. Within the ATC methods addressing this challenge, power routing within the converter system and discontinuous modulation for cascaded H-bridge (CHB) converters are especially suited for application in the ST.

The methodology of graph theory-based modeling of power electronics converter systems was introduced in Section 5.2. An example of how to use the graph-based representation of a converter system in order to apply power routing for reliability was given.

Further, the methodology of graph theory-based modeling of power electronics converter systems was adjusted to fulfill the requirements of the interconnected topology (IT) for hybrid grids-feeding STs presented in Section 3.1. The IT has the potential of significant efficiency improvements via power routing. Therefore, it requires a precise modeling of the losses in the converter system. In order to provide this precise modeling of the losses, it was proposed to use non-conserved power flows in the graph modeling instead of the often considered flow conservation constraint (FCC). It has been found that considering the FCC can cause up to 4 % error in the total losses of the IT. A validation on a laboratory setup of two dual active bridges (DABs) has shown that considering FCC for their series connection causes up to 3.8 % error in the total losses.

Two methods - first and third harmonic clamped modulation method - for discontinuous modulation-based ATC of CHBs have been presented in Section 5.3. The shape of the modulation signals and their generation were described.

Furthermore, a comparison of both clamped modulation methods in terms of potential to influence the losses, total harmonic distortion (THD), and impact on the processed power of CHB cells was carried out. The first harmonic clamped modulation method is advantageous in terms of influence on losses (higher possible loss reduction) and THD (lower THD, which means lower design of grid filters) compared to the third harmonic clamped modulation method. However, the first harmonic clamped modulation method significantly affects the processed power of the CHB cells and is therefore not suitable to be implemented at the same time as power routing. The third harmonic clamped modulation method does not affect the processed power of the CHB cells and can thus be implemented without disturbing power routing. The impact on the processed power of both methods has been validated on a seven-level CHB laboratory setup. Also, the potential to influence the temperatures of the

semiconductors and to reduce thermal cycles of them has been validated for both methods on this laboratory setup.

Finally, a mission profile-based failure analysis was proposed in Section 5.4 to evaluate the impact of different converter failure cases on the mission profile operation points that can be covered without overloading the remaining converters. A sufficient link ratio choice can avoid disadvantages of the IT compared to the non-interconnected topology (NIT) - presented in Section 3.1 - in case of MVac power electronics building block failures. Furthermore, it was proposed to use the possibility of the IT to lower the interconnecting converter loading via the link ratio configuration in order to insert additional failure tolerance for the ST. The interconnecting converter can still be downsized by up to 54 % for the considered hybrid mission profiles while additional failure tolerance is provided.

6. Summary, conclusions and future research

6.1. Summary and conclusions

This work aimed to provide an optimization of the design of hybrid grids-feeding Smart Transformers (STs) for improved efficiency and reduced converter loading, to develop thermal digital twin approaches for observation of the thermal behavior of power modules, and to elaborate on active thermal control methods for hybrid grids-feeding STs.

Chapter 2 introduced the definition of hybrid grids as referred to in this work at first in Section 2.1. The advantages of hybrid secondary distribution grids were presented, which combine benefits of LVac as well as LVdc grids. The benefits of LVac grids are utilization of established protection schemes and equipment as well as supply of ac loads, whereas those of LVdc grids are an efficient integration of photovoltaic power plants, battery energy storage systems, and electric vehicle charging stations as well as a reduced system complexity. Further, the requirements of hybrid grids were shown, which are galvanic isolation between the grids and an efficient hybrid grids connection converter architecture.

Architectures for STs were presented in Section 2.2. Herein, the general ST architectures were shown at first. Then, hybrid grids-feeding ST architectures were proposed, which fulfill the galvanic isolation requirement between the grids. Afterwards, a review on hybrid grids-feeding ST topologies proposed in research articles was given and the architectures these topologies are based on were identified.

The power electronics converters used to realize ST topologies from the ST architectures in this work were described in Section 2.3. The focus of the converter description is to calculate their power losses depending on the power processed by them. For this purpose, the calculation of semiconductor and transformer losses was explained at first. Afterwards, the derivation of the electrical waveforms of a dual active bridge, a two-level three phase inverter, and a cascaded H-bridge was given and it was shown which semiconductors of the converters need to be taken into account for the calculation of the losses at which part of the electrical waveforms.

Chapter 3 introduced the interconnected topology (IT) and the non-interconnected topology (NIT) at first in Section 3.1. These topologies are the realizations of the interconnected and non-interconnected ST architectures presented in Section 2.2 with the converters from Section 2.3. The IT provides an inherited advantage compared to the NIT - the possibility to adapt its configuration via the link ratio. This adaption of the link ratio can be used to realize a reduced required power rating of the interconnecting dual active bridge (DAB) compared to the LVdc DAB as well as to provide improved efficiency of the IT compared to the NIT.

Thereafter, a method to calculate the efficiency of the topologies was proposed. This method consists of two main steps. The first main step is the calculation of efficiency curves for each converter, which give the efficiency of the converter in dependency on its output power. In the second main step these converter efficiency curves are used to calculate the system efficiency based on a non-conserved power flow analysis. The system efficiencies calculated in this way are used to evaluate the design of the IT configuration for optimal efficiency in Section 3.3.

A mission profile-based design procedure for the power ratings of the converters in both topologies was proposed in Section 3.2. The topologies have three ports for MVac, LVac and LVdc grids. Therefore, two mission profiles are needed to define the loading of the system - LVac and LVdc power profiles - which are combined to a hybrid mission profile. The loading of the interconnecting DAB does not only depend on the operation point of the hybrid mission profile but also on the configuration of the IT via the link ratio. This holds the potential to optimize the link ratio to achieve a minimum required power rating of the interconnecting DAB. For nine considered hybrid mission profiles, a downsizing of the interconnecting DAB power rating to values between 31 % and 39 % of the LVdc DAB power rating can be achieved.

Further, a Monte Carlo-based sensitivity analysis of the determined power ratings against deviations of the real power profiles compared to those assumed for the design was conducted. The analysis showed that the impact of the uncertain knowledge of the hybrid mission profile has to be considered for the mission profile-based design of the converter power ratings. It has been found that implementing the possibility of reconfiguration of the link ratio in the application can significantly reduce the impact of the hybrid mission profile uncertainty on the required sizing of the interconnecting DAB for some of the hybrid mission profiles.

The influence of the configuration of the IT via the link ratio on the efficiency of the converter system was investigated in Section 3.3. Two approaches were proposed to identify the link ratio for optimal average weighted efficiency for the assumed hybrid mission profiles. One is based on extensive modeling of all converter efficiencies as presented in Section 3.1.3. This approach is able to always find the optimal link ratio according to the applied modeling. The other approach is solely based on the knowledge of the hybrid mission profile. It requires no modeling effort and provides low computational burden, but does not always provide the optimal link ratio. However, the not realized efficiency benefit by the suboptimal link ratio choice is small, because at least a link ratio directly next to the optimal one is always chosen.

Finally, a laboratory validation of the efficiency influence of the IT configuration via the link ratio was carried out. A validation of a significant influence of the link ratio selection in the IT on the system efficiency was achieved. Also, the possibility to identify optimal operation areas of each link ratio configuration for maximum efficiency was validated. Another result is

that the borders of the optimal operation areas of the link ratio configurations will be close to those analytically calculated, if same efficiency behavior of the produced power electronics building blocks (PEBBs) can be achieved. Otherwise, the location of the borders can be significantly influenced by asymmetries between the efficiencies of MVac PEBBs connected to the dc-link and the ones of the MVac PEBBs connected to the LVdc feeder.

Chapter 4 introduced the fundamentals of thermal modeling at first in Section 4.1. The basic components of thermal modeling and their analogy to the electrical modeling were presented. Commonly used thermal networks - Foster and Cauer networks - to represent the thermal behavior of a single chip temperature in relation to a reference point temperature have been introduced. An approach to model multiple chip temperatures with thermal cross coupling effects has been presented, it is based on the linear accumulation of all impacts of heat sources on the temperatures.

The essential influence of the temperature on the reliability of power semiconductor modules was highlighted in Section 4.2. For this purpose, the degradation mechanism evoked by thermal cycles was explained, a method for lifetime estimation of power semiconductors based on thermal cycle (rainflow) counting as well as existing lifetime models and their limitations were presented, and a review on condition monitoring possibilities for power semiconductors via their thermal behavior was given.

Section 4.3 proposed the digital twin (DT)-based observation of the power semiconductor thermal behavior. The basic principle of the thermal DT was explained and two approaches were proposed. The first approach is based on a particle-swarm-optimization (PSO) and the second approach on a dual extended Kalman filter (DEKF). It has been shown that both approaches are able to identify the thermal parameters of a digital reference model in a real-time simulation (RTS). Hereby, thermal parameters of model parts closer to the chip temperature converge faster to the parameters of the digital reference model than parameters of model parts further away from the chip temperature. This is due to the fact that parameters of model parts closer to the chip have a higher impact on the chip temperature.

Thereafter, a comparison of both approaches was carried out. The PSO-based thermal DT provides a lower computational burden than the DEKF-based thermal DT. The computational burden of the PSO-based thermal DT increases linearly with extending the thermal network, whereas the one of the DEKF-based thermal DT increases quadratically. The DEKF-based thermal DT provides significantly higher convergence speed of the estimated thermal parameters to the reference ones than the PSO-based thermal DT. The optimizer coefficient tuning of the DEKF-based thermal DT provides a wider range which leads to convergence than the one of the PSO-based thermal DT. The convergence of the DEKF-based thermal DT shows significantly higher robustness to input profile variations compared to the one of the PSO-based thermal DT, which requires a specific characterization operation profile of the converter. The potential of an asynchronous execution of the optimization is higher for the

PSO- compared with the DEKF-based thermal DT, because it could compensate significant drawbacks of the PSO- compared to the DEKF-based thermal DT.

Finally, a DEKF-based multichip thermal DT was propsed. For this purpose, a new multichip Cauer network was presented, which is able to represent the temperatures of multiple chips with thermal cross coupling effects and provides a low number of temperature states and thermal parameters. This makes the network suitable for the implementation in the thermal DT, as it provides a significantly lower computational burden than applying a linear accumulation of all impacts of heat sources on the temperatures with more states and parameters. The RTS of the multichip thermal DT with digital thermal reference model showed that the DT is able to converge to the same parameter set without previous knowledge about the parameters of the reference model. The implementation of the multichip thermal DT in the laboratory setup proved the ability to represent the thermal behavior of real power semiconductors.

Chapter 5 gave an overview on active thermal control (ATC) methods used in power electronics systems at first in Section 5.1. There are four main challenges which are addressed by articles on ATC methods for power electronics systems, which are: increasing the overload capability of power electronics converters, thermal cycle reduction of power devices in power electronics converters, balancing thermal stress of power devices within specific topologies or for parallel power devices, and controlling thermal stress of devices in different building blocks in modular and redundant power electronics systems as well as on a microgrid level. The potential objectives of applying the ATC methods within these four main challenges have been presented as well.

Thereafter, these potential objectives were used to evaluate the capabilities of the different ATC methods for application in the ST. The objectives linked to the challenge of controlling thermal stress of devices in different building blocks in modular and redundant power electronics systems were identified as highly relevant for supporting a reliable ST operation. Within the ATC methods addressing this challenge, power routing within the converter system and discontinuous modulation for cascaded H-bridge (CHB) converters are especially suited for application in the ST.

The methodology of graph theory-based modeling of power electronics converter systems was introduced in Section 5.2. An example of how to use the graph-based representation of a converter system in order to apply power routing for reliability was given.

Further, the methodology of graph theory-based modeling of power electronics converter systems was adjusted to fulfill the requirements of the IT for hybrid grids-feeding STs presented in Section 3.1. The IT has the potential of significant efficiency improvements via power routing. Therefore, it requires a precise modeling of the losses in the converter system. In order to provide this precise modeling of the losses, it was proposed to use non-conserved

power flows in the graph modeling instead of the often considered flow conservation constraint (FCC). It has been found that considering the FCC can cause up to 4 % error in the total losses of the IT. A validation on a laboratory setup of two DABs has shown that considering FCC for their series connection causes up to 3.8 % error in the total losses.

Two methods - first and third harmonic clamped modulation method - for discontinuous modulation-based ATC of CHBs have been presented in Section 5.3. The shape of the modulation signals and their generation were described.

Furthermore, a comparison of both clamped modulation methods in terms of potential to influence the losses, total harmonic distortion (THD), and impact on the processed power of CHB cells was carried out. The first harmonic clamped modulation method is advantageous in terms of influence on losses (higher possible loss reduction) and THD (lower THD, which means lower design of grid filters) compared to the third harmonic clamped modulation method. However, the first harmonic clamped modulation method significantly affects the processed power of the CHB cells and is therefore not suitable to be implemented at the same time as power routing. The third harmonic clamped modulation method does not affect the processed power of the CHB cells and can thus be implemented without disturbing power routing. The impact on the processed power of both methods has been validated on a seven-level CHB laboratory setup. Also, the potential to influence the temperatures of the semiconductors and to reduce thermal cycles of them has been validated for both methods on this laboratory setup.

Finally, a mission profile-based failure analysis was proposed in Section 5.4 to evaluate the impact of different converter failure cases on the mission profile operation points that can be covered without overloading the remaining converters. A sufficient link ratio choice can avoid disadvantages of the IT compared to the NIT - presented in Section 3.1 - in case of MVac PEBB failures. Furthermore, it was proposed to use the possibility of the IT to lower the interconnecting converter loading via the link ratio configuration in order to insert additional failure tolerance for the ST. The interconnecting converter can still be downsized by up to 54 % for the considered hybrid mission profiles while additional failure tolerance is provided.

6.2. Future research

The digital twin concept provides a high potential for future research. Potential future research topics based on the thermal digital twins developed in this work are the following ones:

- In this work, two thermal digital twin approaches were proposed, one based on a particle-swarm-optimization, the other based on a dual extended Kalman filter. A future research topic could be the development of a thermal digital twin based on an

unscented Kalman filter, as this is a concept widely applied in other research areas [311] and seems to have the potential to achieve superior performance compared to the dual extended Kalman filter-based thermal digital twin.

- Another future research topic could be the utilization of the thermal digital twin approaches developed in this work for accessing the dynamic capacity of power electronics converters [312]. The dynamic capacity is the capability of power electronics converters to work temporarily beyond the specified power limitations [313]. The thermal digital twin approaches can help to ensure a safe operation of the power electronics converters while the dynamic capacity is utilized. Furthermore, the continuous adjustment of the thermal model parameters can enable a precise prediction of the dynamic capacity available, which might be a relevant information for system operators.
- A further future research topic could be the development of a combination of multiple digital twin approaches for different properties of power electronics converters. A digital twin of the electrical behavior, which takes measured currents and voltages into consideration for the model optimization, could be combined with a digital twin of the losses, which considers input and output power calculated based on voltage and current measurements for the model optimization, and the thermal digital twin approaches proposed in this work.
- One more future research topic could be the application of the thermal digital twin approaches proposed in this work while power cycling tests of power modules are executed. This would give the possibility to characterize the changing thermal behavior during the degradation of the power modules, which could give new insights for condition monitoring purposes.

Potential future research topics based on the proposed interconnected topology for hybrid grids-feeding Smart Transformers are the following ones:

- A future research topic could be the deeper investigation of the online reconfiguration of the interconnected topology proposed in this work. The circuitry required for the online reconfiguration could be designed, manufactured and its application tested on the laboratory setup. The optimal execution times of the online reconfiguration could be investigated based on the assumed hybrid grid mission profile, the number of available reconfiguration events before the circuitry is expected to fail, and the desired lifetime of the circuitry.
- Another future research topic could be the deeper investigation of active power routing for efficiency. The interconnected topology proposed in this work inherits the opportunity to increase the system efficiency by applying power routing [54] to relieve the interconnecting dual active bridge from power that it needs to process. Appropriate

controllers to realize active power routing for efficiency could be developed and the method could be tested on the laboratory setup.

- A further future research topic could be the design of solid state circuit breakers for the protection against grid faults in the LVdc grid for the interconnected topology of the hybrid grid-feeding Smart Transformer. As it can be seen in Fig. 6.1, the power capacity of the converters connected to the LVdc feeder depend on the interconnected topology configuration as well as the sizing of the interconnecting DAB. While the protection schemes for the MVac and LVac grids [314] can be the same for non-interconnected and interconnected topology, the sizing of the solid state circuit breaker for the protection of the LVdc grid should be adjusted according to the power capacity of converters connected to the LVdc feeder.

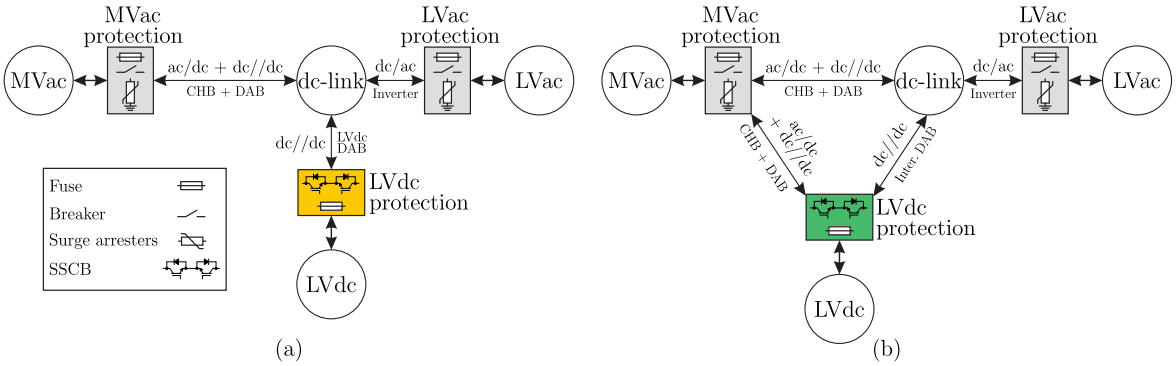


Fig. 6.1: General graphs of (a) NIT and (b) IT with protection of the grid connections.

References

[1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, 2006.

[2] L. Wang, Z. Qin, T. Slangen, P. Bauer, and T. van Wijk, "Grid impact of electric vehicle fast charging stations: Trends, standards, issues and mitigation measures - an overview," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 56–74, 2021.

[3] G. Rituraj, G. R. C. Mouli, and P. Bauer, "A comprehensive review on off-grid and hybrid charging systems for electric vehicles," *IEEE Open Journal of the Industrial Electronics Society*, vol. 3, pp. 203–222, 2022.

[4] F. Nejabatkhah and Y. W. Li, "Overview of power management strategies of hybrid ac/dc microgrid," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7072–7089, 2015.

[5] H. Huang, M. Zhou, S. Zhang *et al.*, "Exploiting the operational flexibility of wind integrated hybrid ac/dc power systems," *IEEE Transactions on Power Systems*, vol. 36, no. 1, pp. 818–826, 2021.

[6] M. Stecca, L. R. Elizondo, T. B. Soeiro, P. Bauer, and P. Palensky, "A comprehensive review of the integration of battery energy storage systems into distribution networks," *IEEE Open Journal of the Industrial Electronics Society*, vol. 1, pp. 46–65, 2020.

[7] F. Ruiz, M. A. Perez, J. R. Espinosa *et al.*, "Surveying solid-state transformer structures and controls: Providing highly efficient and controllable power flow in distribution grids," *IEEE Industrial Electronics Magazine*, vol. 14, no. 1, pp. 56–70, 2020.

[8] M. Liserre, G. Buticchi, M. Andresen *et al.*, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46–58, 2016.

[9] L. Ferreira Costa, G. De Carne, G. Buticchi, and M. Liserre, "The smart transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid," *IEEE Power Electronics Magazine*, vol. 4, no. 2, pp. 56–67, 2017.

[10] M. Liserre, M. A. Perez, M. Langwasser, C. A. Rojas, and Z. Zhou, "Unlocking the hidden capacity of the electrical grid through smart transformer and smart transmission," *Proceedings of the IEEE*, vol. 111, no. 4, pp. 421–437, 2023.

[11] S. Giacomuzzi, M. Langwasser, G. De Carne, G. Buja, and M. Liserre, "Smart transformer-based medium voltage grid support by means of active power control,"

CES Transactions on Electrical Machines and Systems, vol. 4, no. 4, pp. 285–294, 2020.

[12] G. De Carne, G. Buticchi, M. Liserre, and C. Vournas, "Real-time primary frequency regulation using load power control by smart transformers," *IEEE Transactions on Smart Grid*, vol. 10, no. 5, pp. 5630–5639, 2019.

[13] ——, "Load control using sensitivity identification by means of smart transformer," *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 2606–2615, 2018.

[14] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 54–64, 2015.

[15] S. Yang, D. Xiang, A. Bryant *et al.*, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734–2752, 2010.

[16] J. Falck, C. Felgemacher, A. Rojko, M. Liserre, and P. Zacharias, "Reliability of power electronic systems: An industry perspective," *IEEE Industrial Electronics Magazine*, vol. 12, no. 2, pp. 24–35, 2018.

[17] H. Wang, M. Liserre, F. Blaabjerg *et al.*, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, 2014.

[18] S. Peyghami, Z. Wang, and F. Blaabjerg, "A guideline for reliability prediction in power electronic converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 958–10 968, 2020.

[19] K. Rajashekara, H. S. Krishnamoorthy, and B. S. Naik, "Electrification of subsea systems: requirements and challenges in power distribution and conversion," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 259–266, 2017.

[20] J. Nilsson and L. Bertling, "Maintenance management of wind power systems using condition monitoring systems-life cycle cost analysis for two case studies," *IEEE Transactions on Energy Conversion*, vol. 22, no. 1, pp. 223–229, 2007.

[21] J. Kuprat, C. H. van der Broeck, M. Andresen *et al.*, "Research on active thermal control: Actual status and future trends," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6494–6506, 2021.

[22] M. Sasaki, H. Nishio, A. Shorten, and W. T. Ng, "Current balancing control for parallel connected igbts using programmable gate driver output resistance," in *2013 25th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2013, pp. 65–68.

[23] C. Joseph, M. Zolghadri, A. Homaifar, F. Lee, and R. Lorenz, "Novel thermal based current sharing control of parallel converters," in *2004 10th International Workshop on Computational Electronics (IEEE Cat. No.04EX915)*. IEEE, 2004.

[24] M. Novak, T. Dragicevic, and F. Blaabjerg, "Finite set mpc algorithm for achieving thermal redistribution in a neutral-point-clamped converter," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 5290–5296.

[25] V. Raveendran, M. Andresen, and M. Liserre, "Lifetime control of modular smart transformers considering the maintenance schedule," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 60–66.

[26] J. Kuprat, M. Andresen, V. Raveendran, and M. Liserre, "Modular smart transformer topology for the interconnection of multiple isolated ac and dc grids," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4836–4841.

[27] J. Kuprat, J. Schaumburg, M. Langwasser, and M. Liserre, "Mission-profile based design of a hybrid-grids feeding smart transformer," in *2021 6th IEEE Workshop on the Electronic Grid (eGRID)*, 2021, pp. 01–08.

[28] ——, "Mission profile-tailored design and control of an interconnected hybrid grid connecting converter architecture," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2023.

[29] J. Schaumburg, J. Kuprat, M. Langwasser, and M. Liserre, "Efficiency optimization via mission profile-based power routing by design of hybrid grid connecting converter architecture," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 128–136, 2023.

[30] ——, "Efficiency optimization via mission profile-based design of a hybrid grids-feeding smart transformer," in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1–6.

[31] J. Kuprat, Y. Pascal, and M. Liserre, "Real-time thermal characterization of power semiconductors using a pso-based digital twin approach," in *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022, pp. P.1–P.8.

[32] J. Kuprat, J. Schaumburg, M. Langwasser, and M. Liserre, "Improved graph-theory based modeling of the smart transformer for hybrid grids," in *2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, 2022, pp. 1–6.

[33] Y. Li, J. Kuprat, Y. Li, and M. Liserre, "Graph-theory-based derivation, modeling, and control of power converter systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 6557–6571, 2022.

[34] Y. Ko, J. Kuprat, S. Pugliese, and M. Liserre, "Modulation strategies for thermal stress control of chb inverters," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3515–3527, 2022.

[35] A. Gupta, S. Doolla, and K. Chatterjee, "Hybrid ac-dc microgrid: Systematic evaluation of control strategies," *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 3830–3843, 2018.

[36] H. A. B. Siddique and R. W. De Doncker, "Evaluation of dc collector-grid configurations for large photovoltaic parks," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 311–320, 2018.

[37] X. Liu, P. Wang, and P. C. Loh, "A hybrid ac/dc microgrid and its coordination control," *IEEE Transactions on Smart Grid*, vol. 2, no. 2, pp. 278–286, 2011.

[38] O. D. Montoya, W. Gil-González, and A. Garces, "Optimal power flow on dc microgrids: A quadratic convex approximation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 1018–1022, 2019.

[39] T. R. de Oliveira, A. S. Bolzon, and P. F. Donoso-Garcia, "Grounding and safety considerations for residential dc microgrids," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 5526–5532.

[40] M. Mobarrez, D. Fregosi, S. Bhattacharya, and M. Bahmani, "Grounding architectures for enabling ground fault ride-through capability in dc microgrids," in *2017 IEEE Second International Conference on DC Microgrids (ICDCM)*, 2017, pp. 81–87.

[41] D. Kumar, F. Zare, and A. Ghosh, "Dc microgrid technology: System architectures, ac grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12 230–12 256, 2017.

[42] B. Zhao, Q. Song, and W. Liu, "A practical solution of high-frequency-link bidirectional solid-state transformer based on advanced components in hybrid microgrid," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4587–4597, 2015.

[43] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29–42, 2016.

[44] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today´s and future distribution grids," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 317–326, 2019.

[45] C. Kumar, Z. Zou, and M. Liserre, "Smart transformer-based hybrid grid loads support in partial disconnection of mv/hv power system," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8.

[46] M. T. A. Khan, A. A. Milani, A. Chakrabortty, and I. Husain, "Dynamic modeling and feasibility analysis of a solid-state transformer-based power distribution system," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 551–562, 2018.

[47] J. Rodrigues, C. Moreira, and J. P. Lopes, "Smart transformers as active interfaces enabling the provision of power-frequency regulation services from distributed resources in hybrid ac/dc grids," *Applied Sciences*, vol. 10, no. 4, 2020. [Online]. Available: https://www.mdpi.com/2076-3417/10/4/1434

[48] D. Das, H. V.M., and C. Kumar, "Smart transformer-based hybrid lvac and lvdc interconnected microgrid," in *2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, 2018, pp. 1–7.

[49] A. C. Nair and B. Fernandes, "A novel multi-port solid state transformer enabled isolated hybrid microgrid architecture," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 651–656.

[50] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Applikationshandbuch Leistungshalbleiter*, SEMIKRON International GmbH, 2015.

[51] C. R. Sullivan and R. Y. Zhang, "Simplified design method for litz wire," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 2667–2674.

[52] J. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 127–131, 1994.

[53] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings.*, 2002, pp. 36–41.

[54] M. Liserre, G. Buticchi, J. I. Leon *et al.*, "Power routing: A new paradigm for maintenance scheduling," *IEEE Industrial Electronics Magazine*, vol. 14, no. 3, pp. 33–45, 2020.

[55] "Load profiles bdew," accessed 15.02.2023. [Online]. Available: https://www.bdew.de/energie/standardlastprofile-strom/

[56] H. Vermeulen and T. Nieuwoudt, "Optimisation of residential solar pv system rating for minimum payback time using half-hourly profiling," in *2015 International Conference on the Domestic Use of Energy (DUE)*, March 2015, pp. 215–221.

[57] P. Djapic, M. Kairudeen, M. Aunedi *et al.*, *Design and real-time control of smart distribution networks*, report d4 for the "low carbon london" lcnf project: imperial college london ed., 12 2014.

[58] I. N. Bronstein, K. A. Semendjajew, G. Musiol, and H. Mühlig, *Taschenbuch der Mathematik*, Ebner and Spiegel, Eds. Verlag Europa-Lehrmittel, 2013.

[59] M. Novak, A. Sangwongwanich, and F. Blaabjerg, "Monte carlo-based reliability estimation methods for power devices in power electronics systems," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 523–534, 2021.

[60] G. De Carne, G. Buticchi, Z. Zou, and M. Liserre, "Reverse power flow control in a st-fed distribution grid," *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 3811–3819, 2018.

[61] A. Stippich, M. Neubert, A. Sewergin, and R. W. De Doncker, "Significance of thermal cross-coupling effects in power semiconductor modules," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, 2016, pp. 1–6.

[62] B. Zahn, "Steady state thermal characterization of multiple output devices using linear superposition theory and a non-linear matrix multiplier," in *Fourteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.98CH36195)*, 1998, pp. 39–46.

[63] U. Drofenik, D. Cottet, A. Müsing, J.-M. Meyer, and J. W. Kolar, "Modelling the thermal coupling between internal power semiconductor dies of a water-cooled 3300v/1200a hipak igbt module," in *Proceedings of Power Conversion and Intelligent Motion Conference*, 2007, pp. 1–8.

[64] A. S. Bahman, K. Ma, and F. Blaabjerg, "Thermal impedance model of high power igbt modules considering heat coupling effects," in *2014 International Power Electronics and Application Conference and Exposition*, 2014, pp. 1382–1387.

[65] M. Ouhab, Z. Khatir, A. Ibrahim *et al.*, "New analytical model for real-time junction temperature estimation of multichip power module used in a motor drive," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5292–5301, 2018.

[66] M. Shahjalal, M. R. Ahmed, H. Lu, C. Bailey, and A. J. Forsyth, "An analysis of the thermal interaction between components in power converter applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9082–9094, 2020.

[67] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters-a review," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3081–3092, 2012.

[68] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Junction temperature measurements via thermo-sensitive electrical parameters and their application to condition monitoring and active thermal control of power converters," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, 2013, pp. 942–948.

[69] S. Kalker, L. A. Ruppert, C. H. van der Broeck *et al.*, "Reviewing thermal-monitoring techniques for smart power modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 1326–1341, 2022.

[70] D. Wagenitz, A. Hambrecht, and S. Dieckerhoff, "Lifetime evaluation of igbt power modules applying a nonlinear saturation voltage observer," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1–5.

[71] D. Wagenitz, C. Laeuschner, R. Thewes, and S. Dieckerhoff, "Design and evaluation of a sensor for measuring the igbt on-state saturation voltage," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1–5.

[72] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics reliability*, vol. 42, no. 4-5, pp. 653–667, 2002.

[73] A. Morozumi, K. Yamada, T. Miyasaka, S. Sumi, and Y. Seki, "Reliability of power cycling for igbt power semiconductor modules," *IEEE Transactions on Industry Applications*, vol. 39, no. 3, pp. 665–671, 2003.

[74] L. R. GopiReddy, L. M. Tolbert, B. Ozpineci, and J. O. P. Pinto, "Rainflow algorithm-based lifetime estimation of power semiconductors in utility applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3368–3375, 2015.

[75] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of igbt modules in traction application," in *Proceedings of Second International Conference on Power Electronics and Drive Systems*, vol. 1, 1997, pp. 425–430 vol.1.

[76] T. Wernicke, A. Middendorf, S. Dieckerhoff, S. Guttowski, and H. Reichl, "Test system for the reliability management of power modules," in *5th International Conference on Integrated Power Electronics Systems*, 2008, pp. 1–5.

[77] D. Wagenitz, A. Westerholz, E. Erdmann, A. Hambrecht, and S. Dieckerhoff, "Power cycling test bench for igbt power modules used in wind applications," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.

[78] Y. Chen, P. Zhang, B. Hou, and H.-Z. Huang, "Study on lifetime model of power devices based on junction temperature," in *2019 International Conference on Quality, Reliability, Risk, Maintenance, and Safety Engineering (QR2MSE)*, 2019, pp. 84–89.

[79] U.-M. Choi, F. Blaabjerg, and K. Ma, "Lifetime prediction of igbt modules based on linear damage accumulation," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2276–2281.

[80] U.-M. Choi, F. Blaabjerg, and S. Jorgensen, "Study on effect of junction temperature swing duration on lifetime of transfer molded power igbt modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6434–6443, 2017.

[81] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of igbt modules - various factors influencing lifetime," in *5th International Conference on Integrated Power Electronics Systems*, 2008, pp. 1–6.

[82] H. Lu, T. Tilford, C. Bailey, and D. Newcombe, "Lifetime prediction for power electronics module substrate mount-down solder interconnect," in *2007 International Symposium on High Density packaging and Microsystem Integration*, 2007, pp. 1–10.

[83] W. Lai, M. Chen, L. Ran *et al.*, "Low δt_j stress cycle effect in igbt power module die-attach lifetime modeling," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6575–6585, 2016.

[84] ——, "Experimental investigation on the effects of narrow junction temperature cycles on die-attach solder layer in an igbt module," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1431–1441, 2017.

[85] N. Dornic, Z. Khatir, S. H. Tran *et al.*, "Stress-based model for lifetime estimation of bond wire contacts using power cycling tests and finite-element modeling," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1659–1667, 2019.

[86] J. Lutz, C. Schwabe, G. Zeng, and L. Hein, "Validity of power cycling lifetime models for modules and extension to low temperature swings," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1–P.9.

[87] U. Scheuermann and M. Junghaenel, "Limitation of power module lifetime derived from active power cycling tests," in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–10.

[88] A. Watanabe and I. Omura, "Real-time failure imaging system under power stress for power semiconductors using scanning acoustic tomography (sat)," *Microelectronics Reliability*, vol. 52, no. 9, pp. 2081–2086, 2012, special Issue 23rd European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271412002879

[89] Z. Zhang, A. Suetake, C. Chen *et al.*, "Development of solder deterioration diagnosis system of a power module via the acoustic emission monitoring (aem) technique," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2021, pp. 179–182.

[90] ——, "Real-time monitoring and diagnosis of die attach structure deterioration by using acoustic emission method," in *2022 International Conference on Electronics Packaging (ICEP)*, 2022, pp. 91–92.

[91] Z. Zhang, C. Chen, A. Suetake *et al.*, "Online condition monitoring of solder fatigue in a clip-bonding sic mosfet power assembly via acoustic emission technique," *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 1468–1478, 2023.

[92] D. Kwon, M. H. Azarian, and M. Pecht, "Nondestructive sensing of interconnect failure mechanisms using time-domain reflectometry," *IEEE Sensors Journal*, vol. 11, no. 5, pp. 1236–1241, 2011.

[93] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2413–2426, 2015.

[94] B. Wang, J. Cai, X. Du, and L. Zhou, "Review of power semiconductor device reliability for power converters," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 101–117, 2017.

[95] S. Mollov and F. Blaabjerg, "Condition and health monitoring in power electronics," in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–8.

[96] Z. Ni, X. Lyu, O. P. Yadav *et al.*, "Overview of real-time lifetime prediction and extension for sic power converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7765–7794, 2020.

[97] B. Hu, Z. Hu, L. Ran *et al.*, "Heat-flux-based condition monitoring of multichip power modules using a two-stage neural network," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7489–7500, 2021.

[98] X. Liu, T. Jiao, D. Das, I. H. Naqvi, and M. Pecht, "Nonparametric model-based online junction temperature and state-of-health estimation for insulated gate bipolar transistors," *IEEE Access*, vol. 9, pp. 95 304–95 316, 2021.

[99] Z. Zhang, G. Fu, B. Wan, M. Jiang, and Y. Li, "A high-efficiency igbt health status assessment method based on data driven," *IEEE Transactions on Electron Devices*, vol. 68, no. 1, pp. 168–174, 2021.

[100] D. Xiang, L. Ran, P. Tavner *et al.*, "Monitoring solder fatigue in a power module using case-above-ambient temperature rise," *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2578–2591, 2011.

[101] B. Ji, V. Pickert, and B. Zahawi, "In-situ bond wire and solder layer health monitoring circuit for igbt power modules," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1–6.

[102] B. Ji, V. Pickert, W. P. Cao, and L. Xing, "Onboard condition monitoring of solder fatigue in igbt power modules," in *2013 9th IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives (SDEMPED)*, 2013, pp. 9–15.

[103] B. Tian, W. Qiao, Z. Wang, T. Gachovska, and J. L. Hudgins, "Monitoring igbt's health condition via junction temperature variations," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 2550–2555.

[104] B. Ji, X. Song, W. Cao *et al.*, "In situ diagnostics and prognostics of solder fatigue in igbt modules for electric vehicle drives," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1535–1543, 2015.

[105] M. Sathik, T. K. Jet, C. J. Gajanayake, R. Simanjorang, and A. K. Gupta, "Comparison of power cycling and thermal cycling effects on the thermal impedance degradation in igbt modules," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, 2015, pp. 001 170–001 175.

[106] T. Krone, L. Dang Hung, M. Jung, and A. Mertens, "Advanced condition monitoring system based on on-line semiconductor loss measurements," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8.

[107] M. A. Eleffendi and C. M. Johnson, "In-service diagnostics for wire-bond lift-off and solder fatigue of power semiconductor packages," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7187–7198, 2017.

[108] F. Gonzalez-Hernando, J. San-Sebastian, A. Garcia-Bediaga *et al.*, "Wear-out condition monitoring of igbt and mosfet power modules in inverter operation," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6184–6192, 2019.

[109] A. Bryant, R. Leedham, and R. Varney, "A unified platform for junction temperature estimation and condition monitoring of power semiconductor devices," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. 1–10.

[110] M. Hernes, S. D'Arco, O. C. Spro, and D. Peftitsis, "Improving monitoring of parallel ageing of igbt bond-wires and solder layers by temperature compensation," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–7.

[111] F. Grieger and A. Lindemann, "Thermal impedance spectroscopy for non-destructive evaluation of power cycling," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2015, pp. 1–6.

[112] M. Denk and M.-M. Bakran, "Investigation of the characteristic thermal properties of igbt power modules for robust in-situ health monitoring," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1–9.

[113] C. H. van der Broeck, T. Polom, R. D. Lorenz, and R. W. De Doncker, "Thermal monitoring of power electronic modules using device self-sensing," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 4699–4706.

[114] T. A. Polom, C. van der Broeck, R. W. De Doncker, and R. D. Lorenz, "Real-time, in situ degradation monitoring in power semiconductor converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 2720–2727.

[115] C. H. van der Broeck, S. Kalker, T. A. Polom, R. D. Lorenz, and R. W. De Doncker, "In-situ thermal impedance spectroscopy of power electronic modules for localized degradation identification," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1–8.

[116] C. H. van der Broeck, T. A. Polom, R. D. Lorenz, and R. W. De Doncker, "Real-time monitoring of thermal response and life-time varying parameters in power modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 5, pp. 5279–5291, 2020.

[117] T. A. Polom, C. H. van der Broeck, R. W. De Doncker, and R. D. Lorenz, "Exploiting distinct thermal response properties for power semiconductor module health monitoring," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4865–4878, 2021.

[118] M. Denk, M.-M. Bakran, and S. Schafferhans, "Case sensitive condition monitoring of an igbt inverter in a hybrid car," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1–6.

[119] M. Denk and M.-M. Bakran, "Health-monitoring of igbt power modules using repetitive half-sinusoidal power losses," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2016, pp. 1–8.

[120] A. M. Aliyu, S. Chowdhury, and A. Castellazzi, "In-situ health monitoring of power converter modules for preventive maintenance and improved availability," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1–10.

[121] G. Hantos, J. Hegedüs, M. Rencz, and A. Poppe, "Aging tendencies of power mosfets - a reliability testing method combined with thermal performance monitoring," in *2016 22nd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2016, pp. 220–223.

[122] J. Zhang, X. Du, S. Zheng, and H.-M. Tai, "Thermal resistor and capacitor parameter identification using cooling curve of igbt module," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1729–1733.

[123] Y. Hu, P. Shi, H. Li, and C. Yang, "Health condition assessment of base-plate solder for multi-chip igbt module in wind power converter," *IEEE Access*, vol. 7, pp. 72 134–72 142, 2019.

[124] Z. Hu, B. Hu, L. Ran *et al.*, "Monitoring power module solder degradation from heat dissipation in two opposite directions," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9754–9766, 2022.

[125] J. Zhang, X. Du, and S. Zheng, "Condition monitoring of igbt module and forced air cooling system using time constants of heat sink temperature cooling curve," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 2554–2558.

[126] A. Hambrecht, R. Klitzke, S. Lehmann, D. Wagenitz, and S. Dieckerhoff, "Transient thermal impedance model based on online-measurement of the on-state voltage in igbt converters," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1–4.

[127] U.-M. Choi and F. Blaabjerg, "Separation of wear-out failure modes of igbt modules in grid-connected inverter systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6217–6223, 2018.

[128] ——, "Real-time condition monitoring of igbt modules in pv inverter systems," in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–5.

[129] W. Liu, D. Zhou, F. Iannuzzo, M. Hartmann, and F. Blaabjerg, "Separation and validation of bond-wire and solder layer failure modes in igbt modules," *IEEE Transactions on Industry Applications*, vol. 58, no. 2, pp. 2324–2331, 2022.

[130] F. Tao, H. Zhang, A. Liu, and A. Y. C. Nee, "Digital twin in industry: State-of-the-art," *IEEE Transactions on Industrial Informatics*, vol. 15, no. 4, pp. 2405–2415, 2019.

[131] Y. Peng, S. Zhao, and H. Wang, "A digital twin based estimation method for health indicators of dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2105–2118, 2021.

[132] Y. Liu, G. Chen, Y. Liu, L. Mo, and X. Qing, "Condition monitoring of power electronics converters based on digital twin," in *2021 IEEE 3rd International Conference on Circuits and Systems (ICCS)*, 2021, pp. 190–195.

[133] Y. Gong, Y. Tian, C. Wen *et al.*, "Digital twin based condition monitoring for high power converters," in *2022 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, 2022, pp. 892–897.

[134] A. B. Mirza, K. Choksi, S. S. Vala *et al.*, "Cognitive insights into metaheuristic digital twin based health monitoring of dc-dc converters," in *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022, pp. 1–7.

[135] S. Rajendran, V. S. K. Devi, and M. Diaz, "Digital twin based identification of degradation parameters of dc-dc converters using an arithmetic optimization algorithm," in *2022 3rd International Conference for Emerging Technology (INCET)*, 2022, pp. 1–5.

[136] Q. Wu, W. Wang, Q. Wang, L. Xiao, and B. Hu, "Digital twin approach for degradation parameters identification of a single-phase dc-ac inverter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1725–1730.

[137] M. Milton, C. D. L. O, H. L. Ginn, and A. Benigni, "Controller-embeddable probabilistic real-time digital twins for power electronic converter diagnostics," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9850–9864, 2020.

[138] S. Chen, S. Wang, P. Wen, and S. Zhao, "Digital twin for degradation parameters identification of dc-dc converters based on bayesian optimization," in *2021 IEEE International Conference on Prognostics and Health Management (ICPHM)*, 2021, pp. 1–9.

[139] A. Wunderlich and E. Santi, "Digital twin models of power electronic converters using dynamic neural networks," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2369–2376.

[140] B. Rodriguez, E. Sanjurjo, M. Tranchero, C. Romano, and F. Gonzalez, "Thermal parameter and state estimation for digital twins of e-powertrain components," *IEEE Access*, vol. 9, pp. 97 384–97 400, 2021.

[141] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power mosfets considering thermal aging effects," *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 220–228, 2014.

[142] Z. Hu, M. Du, K. Wei, and W. G. Hurley, "An adaptive thermal equivalent circuit model for estimating the junction temperature of igbts," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 392–403, 2019.

[143] X. Xiao, X. Ge, Q. Ke *et al.*, "An adaptive temperature observer for electrothermal analysis of igbt based on temperature characteristics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 2, pp. 2246–2258, 2023.

[144] Z. Wang, W. Qiao, and L. Qu, "A real-time adaptive igbt thermal model based on an effective heat propagation path concept," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 3936–3946, 2021.

[145] M. A. Eleffendi and C. M. Johnson, "Application of kalman filter to estimate junction temperature in igbt power modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1576–1587, 2016.

[146] U. Drofenik and J. W. Kolar, "A general scheme for calculating switching-and conduction-losses of power semiconductors in numerical circuit simulations of power electronic systems," in *Proc. IPEC*, vol. 5. Citeseer, 2005, pp. 4–8.

[147] M. Andresen, J. Kuprat, V. Raveendran, J. Falck, and M. Liserre, "Active thermal control for delaying maintenance of power electronics converters," *Chinese Journal of Electrical Engineering*, vol. 4, no. 3, pp. 13–20, 2018.

[148] V. Blasko, R. Lukaszewski, and R. Sladky, "On line thermal model and thermal management strategy of a three phase voltage source inverter," in *Industry Applications Conference, 1999*, vol. 2, 1999, pp. 1423–1431 vol.2.

[149] D. A. Murdock, J. E. Ramos, J. J. Connors, and R. D. Lorenz, "Active thermal control of power electronics modules," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003.*, vol. 3, Oct 2003, pp. 1511–1515 vol.3.

[150] D. A. Murdock, J. E. R. Torres, J. J. Connors, and R. D. Lorenz, "Active thermal control of power electronic modules," *IEEE Transactions on Industry Applications*, vol. 42, no. 2, pp. 552–558, March 2006.

[151] L. Wei, J. Mcguire, and R. A. Lukaszewski, "Analysis of pwm frequency control to improve the lifetime of pwm inverter," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 900–907.

[152] J. Lemmens, P. Vanassche, and J. Driesen, "Optimal control of traction motor drives under electrothermal constraints," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 2, pp. 249–263, June 2014.

[153] D. Kaczorowski, B. Michalak, and A. Mertens, "A novel thermal management algorithm for improved lifetime and overload capabilities of traction converters," in *EPE'15 ECCE-Europe*, Sept 2015, pp. 1–10.

[154] T. A. Polom, B. Wang, and R. D. Lorenz, "δ tj control of switching power devices at thermal boundaries via physics-based loss manipulation," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8.

[155] ——, "Control of junction temperature and its rate of change at thermal boundaries via precise loss manipulation," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4796–4806, Sept 2017.

[156] J. Lemmens, J. Driesen, and P. Vanassche, "Thermal management in traction applications as a constraint optimal control problem," in *2012 IEEE Vehicle Power and Propulsion Conference*, Oct 2012, pp. 36–41.

[157] C. H. van der Broeck and R. W. De Doncker, "Active thermal management for enhancing peak-current capability of three-phase inverters," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 3312–3319.

[158] Y. Qi, K. Ma, and S. Xia, "Active thermal control with optimal phase angle under stall condition of machine drive inverter," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 128–10 132, 2022.

[159] F. Mandrile, F. Stella, E. Carpaneto, and R. Bojoi, "Grid fault current injection using virtual synchronous machines featuring active junction temperature limitation of power devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 5, pp. 6243–6251, 2022.

[160] C. H. v. d. Broeck and R. W. De Doncker, "Increasing torque capability of ac drives via active thermal management of inverters," *IEEE Transactions on Industry Applications*, vol. 57, no. 6, pp. 6277–6287, 2021.

[161] J. Lemmens, J. Driesen, and P. Vanassche, "Dynamic dc-link voltage adaptation for thermal management of traction drives," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 180–187.

[162] A. Wang, Y. Qi, and K. Ma, "Adaptive dc voltage control for optimal junction temperature redistribution under stall condition of electric machine drive inverter," *IEEE Transactions on Power Electronics*, vol. 38, no. 4, pp. 4229–4234, 2023.

[163] C. H. van der Broeck, L. A. Ruppert, R. D. Lorenz, and R. W. De Doncker, "Methodology for active thermal cycle reduction of power electronic modules," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8213–8229, 2019.

[164] C. H. van der Broeck, L. A. Ruppert, R. D. Lorenz, and R. W. De Doncker, "Active thermal cycle reduction of power modules via gate resistance manipulation," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 3 2018.

[165] M. Weckert and J. Roth-Stielow, “Lifetime as a control variable in power electronic systems,” in *Emobility - Electrical Power Train, 2010*, Nov 2010, pp. 1–6.

[166] L. Wei, J. McGuire, and R. A. Lukaszewski, “Analysis of pwm frequency control to improve the lifetime of pwm inverter,” *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 922–929, March 2011.

[167] M. Weckert and J. Roth-Stielow, “Chances and limits of a thermal control for a three-phase voltage source inverter in traction applications using permanent magnet synchronous or induction machines,” in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.

[168] J. Wu, L. Zhou, P. Sun, and X. Du, “Control of igbt junction temperature in small-scale wind power converter,” in *2014 International Power Electronics and Application Conference and Exposition*, 2014, pp. 41–48.

[169] L. Zhou, J. Wu, P. Sun, and X. Du, “Junction temperature management of igbt module in power electronic converters,” *Microelectronics Reliability*, vol. 54, no. 12, pp. 2788–2795, 2014. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S002627141400198X

[170] J. Wolfle, J. Roth-Stielow, O. Koller, and B. Bertsche, “Control method to increase the reliability of igbt power modules validated on a three phase inverter,” in *2015 IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2015, pp. 1–6.

[171] J. Falck, M. Andresen, and M. Liserre, “Active thermal control of igbt power electronic converters,” in *Industrial Electronics Society, IECON 2015 - 41st Annual Conference of the IEEE*, Nov 2015, pp. 000 001–000 006.

[172] M. Andresen, G. Buticchi, J. Falck, M. Liserre, and O. Muehlfeld, “Active thermal management for a single-phase h-bridge inverter employing switching frequency control,” in *PCIM Europe 2015*, May 2015, pp. 1–8.

[173] Z. Qin, H. Wang, F. Blaabjerg, and P. C. Loh, “The feasibility study on thermal loading control of wind power converters with a flexible switching frequency,” in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 485–491.

[174] D. Kaczorowski and A. Mertens, “Reduction of the ev inverter chip size at constant reliability by active thermal control,” in *2016 IEEE Vehicle Power and Propulsion Conference (VPPC)*, Oct 2016, pp. 1–0.

[175] D. Kaczorowski, M. Mittelstedt, and A. Mertens, “Investigation of discontinuous pwm as additional optimization parameter in an active thermal control,” in *2016 18th European Conference on Power Electronics and Applications (EPE’16 ECCE Europe)*, 2016, pp. 1–10.

[176] M. Andresen, G. Buticchi, and M. Liserre, "Study of reliability-efficiency tradeoff of active thermal control for power electronic systems," *Microelectronics Reliability*, vol. 58, pp. 119–125, 2016, reliability Issues in Power Electronics. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S002627141530264X

[177] I. Vernica, F. Blaabjerg, and K. Ma, "Modelling and design of active thermal controls for power electronics of motor drive applications," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2902–2909.

[178] J. Woelfle, M. Nitzsche, N. Troester, M. Stempfle, and J. Roth-Stielow, "Comparison of three model based junction temperature control systems to increase the lifetime of igbt-power-modules," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, pp. 1–8.

[179] J. Wölfle, M. Nitzsche, N. Tröster *et al.*, "Combination of two variables in a junction temperature control system to elongate the expected lifetime of igbt-power-modules," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, 2017, pp. 41–47.

[180] J. Woelfle, M. Pitters, J. Ruthardt *et al.*, "Comparison of two model based temperature control systems implemented on a three level t-type inverter," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–8.

[181] J. Wölfle, M. Nitzsche, J. Ruthardt, and J. Roth-Stielow, "Junction temperature control system to increase the lifetime of igbt-power-modules in synchronous motor drives without affecting torque and speed," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 273–283, 2020.

[182] J. Ruthardt, H. Schulte, P. Ziegler *et al.*, "Junction temperature control strategy for lifetime extension of power semiconductor devices," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. 1–9.

[183] J. Ruthardt, A. Klinkhammer, P. Marx *et al.*, "Lifetime extension of power semiconductor devices by closed-loop junction temperature control," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. 1–10.

[184] R. Gonzalez, C. A. Rojas, and L. Callegaro, "Three-level dc-dc gan-based converter with active thermal control for powertrain applications in electric vehicles," in *2021 22nd IEEE International Conference on Industrial Technology (ICIT)*, vol. 1, 2021, pp. 502–507.

[185] C. A. Rojas, R. Gonzalez, L. Callegaro, and H. Young, "Mission profile-oriented active thermal control of a bidirectional three-level buck-boost gan-based dc-dc converter for electric vehicles powertrains," in *IECON 2021 - 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1–6.

[186] H. Luo, F. Iannuzzo, K. Ma *et al.*, "Active gate driving method for reliability improvement of igbts via junction temperature swing reduction," in *Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016.

[187] A. Soldati, F. Dossena, G. Pietrini *et al.*, "Thermal stress mitigation by active thermal control: Architectures, models and specific hardware," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.

[188] A. Soldati, C. Concari, F. Dossena *et al.*, "Active thermal control for reliability improvement of mos-gated power devices," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2017, pp. 7935–7940.

[189] P. K. Prasobhu, V. Raveendran, G. Buticchi, and M. Liserre, "Active thermal control of a dc/dc gan-based converter," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 1146–1152.

[190] J. Ruthardt, M. Fischer, J. Felix Woelfle, N. Troester, and J. Roth-Stielow, "Three-level-gate-driver to run power transistors in the saturation region for junction temperature control," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–8.

[191] J. Ruthardt, P. Ziegler, M. Fischer, and J. Roth-Stielow, "Model based junction temperature control using the gate driver voltage as a correction variable," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1–P.8.

[192] J. Ruthardt, L. Schnabel, P. Ziegler *et al.*, "Closed loop junction temperature control of power transistors for lifetime extension," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 2955–2955.

[193] J. Ruthardt, C. Hermann, J. Wölfle, M. Fischer, and J. Roth-Stielow, "Gate-driver circuit with a variable supply voltage to influence the switching losses," *The Journal of Engineering*, vol. 2019, no. 17, pp. 3692–3695, 2019. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/joe.2018.8129

[194] M. Andresen, K. Ma, G. Buticchi *et al.*, "Junction temperature control for more reliable power electronics," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 765–776, Jan 2018.

[195] D. Qin, G. Ozkan, C. Edrington, and Z. Zhang, "Electrothermal management using in-situ junction temperature monitoring for enhanced reliability of sic-based power electronics," in *2021 IEEE Electric Ship Technologies Symposium (ESTS)*, 2021, pp. 1–7.

[196] J. Ruthardt, J. Wölfle, N. Tröster, M. Fischer, and J. Roth-Stielow, "Dead time as a correction variable for junction temperature control," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018, pp. P.1–P.8.

[197] F. Hosseinabadi, H. Polat, G. E. Martin *et al.*, "Active thermal control of a wbg-based ac-dc converter using dynamic gate-drive for lifetime improvement," in *IECON 2022 - 48th Annual Conference of the IEEE Industrial Electronics Society*, 2022, pp. 1–6.

[198] A. Soldati, F. Iannuzzo, C. Concari, D. Barater, and F. Blaabjerg, "Active thermal control by controlled shoot-through of power devices," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 4363–4368.

[199] K. Ma, M. Liserre, and F. Blaabjerg, "Reactive power control methods for improved reliability of wind power inverters under wind speed variations," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 3105–3112.

[200] ——, "Reactive power influence on the thermal cycling of multi-mw wind power inverter," *IEEE Transactions on Industry Applications*, vol. 49, no. 2, pp. 922–930, March 2013.

[201] D. Zhou, F. Blaabjerg, M. Lau, and M. Tonnes, "Thermal behavior optimization in multi-mw wind power converter by reactive power circulation," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2863–2870.

[202] ——, "Thermal behavior optimization in multi-mw wind power converter by reactive power circulation," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 433–440, 2014.

[203] M. K. Bakhshizadeh, K. Ma, P. C. Loh, and F. Blaabjerg, "Indirect thermal control for improved reliability of modular multilevel converter by utilizing circulating current," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2167–2173.

[204] M. Saur, B. Piepenbreier, W. Xu, and R. D. Lorenz, "Implementation and evaluation of inverter loss modeling as part of db-dtfc for loss minimization each switching period," in *2014 16th European Conference on Power Electronics and Applications*, Aug 2014, pp. 1–10.

[205] J. Falck and M. Liserre, "Induction machine flux variation for active thermal control," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018, pp. P.1–P.10.

[206] Y. Yang, H. Wang, F. Blaabjerg, and T. Kerekes, "A hybrid power control concept for pv inverters with reduced thermal loading," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6271–6275, 2014.

[207] M. Andresen, G. Buticchi, and M. Liserre, "Thermal stress reduced maximum power point tracking for two stages photovoltaic converters," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 2116–2123.

[208] ——, "Thermal stress analysis and mppt optimization of photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4889–4898, 2016.

[209] J. Woelfle, O. Lehmann, and J. Roth-Stielow, "A novel control method to improve the reliability of traction inverters for permanent magnet synchronous machines," in *2015 IEEE PEDS*, June 2015, pp. 379–384.

[210] J. Wölfle, T. Röser, M. Nitzsche *et al.*, "Model based temperature control system to increase the expected lifetime of igbt power modules executed on a neutral point diode clamped three level inverter," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1–P.9.

[211] M. Andresen, G. De Carne, M. Schloh, and M. Liserre, "Active thermal control of asynchronously-connected grids considering load sensitivity to voltage," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 4070–4077.

[212] M. Andresen, G. De Carne, and M. Liserre, "Load-dependent active thermal control of grid-forming converters," *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 2078–2086, 2020.

[213] W. J. Choy, A. Castellazzi, and P. Zanchetta, "Adaptive cooling of power modules for reduced power and thermal cycling," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.

[214] X. Wang, A. Castellazzi, and P. Zanchetta, "Observer based temperature control for reduced thermal cycling in power electronic cooling," *Applied Thermal Engineering*, vol. 64, no. 1-2, pp. 10 – 18, 2014.

[215] J. N. Davidson, D. A. Stone, and M. P. Foster, "Real-time temperature monitoring and control for power electronic systems under variable active cooling by characterisation of device thermal transfer impedance," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, 2014, pp. 1–6.

[216] X. Wang, Y. Wang, and A. Castellazzi, "Reduced active and passive thermal cycling degradation by dynamic active cooling of power modules," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 309–312.

[217] Y. Yerasimou, V. Pickert, B. Ji, and X. Song, "Liquid metal magnetohydrodynamic pump for junction temperature control of power modules," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2018.

[218] F. Gonzalez-Hernando, J. San-Sebastian, M. Arias, A. Rujas, and L. Mir, "Active thermal control for lifetime extension of traction converter," in *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*, vol. 2020, 2020, pp. 1007–1012.

[219] C. Li, D. Jiao, J. Jia, F. Guo, and J. Wang, "Thermoelectric cooling for power electronics circuits: Modeling and active temperature control," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3995–4005, Nov 2014.

[220] J. F. Wölfle and J. Roth-Stielow, "A hybrid discontinuous modulation technique to influence the switching losses of three phase inverters," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1–10.

[221] J. Woelfle, M. Nitzsche, J. Weimer, M. Stempfle, and J. Roth-Stielow, "Temperature control system using a hybrid discontinuous modulation technique to improve the lifetime of igbt power modules," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–10.

[222] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Discontinuous-modulation-based active thermal control of power electronic modules in wind farms," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 301–310, 2019.

[223] M. Andresen, G. Buticchi, and M. Liserre, "Active thermal control of isolated soft switching dc/dc converters," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 6818–6823.

[224] J. Falck, M. Andresen, and M. Liserre, "Thermal-based finite control set model predictive control for igbt power electronic converters," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–7.

[225] J. Falck, G. Buticchi, and M. Liserre, "Thermal stress based model predictive control of electric drives," *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1–1, 2017.

[226] R. Han, Q. Xu, L. Wang *et al.*, "Modulated model predictive control for reliability improvement of extremely low frequency power amplifier via junction temperature swing reduction," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 1, pp. 302–313, 2022.

[227] N. Deshmukh, A. Chanekar, S. Anand, and S. R. Sahoo, "Active thermal control for buck converter-based active power decoupling circuit," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 955–14 965, 2022.

[228] J. Ewanchuk, J. Brandelero, and S. Mollov, "Lifetime extension of a multi-die sic power module using selective gate driving with temperature feedforward compensation," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 2520–2526.

[229] J. Ewanchuk, J. Brandelero, and S. Mollov, "A gate driver based approach to improving the current density in a power module by equalizing the individual die temperatures," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 4652–4658.

[230] Z. He, Z. Li, F. Yuan *et al.*, "Active thermal control of sic/si hybrid switch," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, 2018, pp. 1–4.

[231] J. Brandelero, J. Ewanchuk, N. Degrenne, and S. Mollov, "Lifetime extension through tj equalisation by use of intelligent gate driver with multi-chip power module," *Microelectronics Reliability*, vol. 88, pp. 428–432, 2018.

[232] V. Ferreira, M. Andresen, B. Cardoso, and M. Liserre, "Selective soft-switching for thermal balancing in igbt-based multichip systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 3982–3991, 2021.

[233] ——, "Pulse-shadowing-based thermal balancing in multichip modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4081–4088, 2020.

[234] V. Quemener, J. Le Lesle, P.-Y. Pichon, J. C. Brandelero, and N. Degrenne, "A gate driver for on-line heat-treatment to extend the lifetime of multichip power modules," in *CIPS 2022; 12th International Conference on Integrated Power Electronics Systems*, 2022, pp. 1–5.

[235] J. L. Barnette, A.Nahar, M. Zolghadri *et al.*, "Relative temperature control in parallel-acting power modules," in *Proc. of Annual Conf of the Center for Power Electronic Systems*, 2005, pp. 243–252.

[236] J. Barnette, M. Zolghadri, M. Walters, and A. Homaifar, "Temperature integrated load sharing of paralleled modules," in *2006 1ST IEEE Conference on Industrial Electronics and Applications*, 2006, pp. 1–6.

[237] Y. Zeng, A. Hussein, and A. Castellazzi, "Individual device active cooling for enhanced system-level power density and more uniform temperature distribution," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 471–474.

[238] T.-m. Phan, G. Riedel, N. Oikonomou, and M. Pacas, "Pwm for active thermal protection in three level neutral point clamped inverters," in *2013 IEEE ECCE Asia Downunder*, 2013, pp. 906–911.

[239] T.-M. Phan, G. J. Riedel, N. Oikonomou, and M. Pacas, "Active thermal protection and lifetime extension in 3l-npc-inverter in the low modulation range," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2269–2276.

[240] M. Aly, G. M. Dousoky, and M. Shoyama, "Reliability enhancement of multilevel inverters through svpwm-based thermal management methodology," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, 2015, pp. 1–6.

[241] ——, "Lifetime-oriented svpwm for thermally-overloaded power devices in three-level inverters," in *Industrial Electronics Society, IECON 2015 - 41st Annual Conference of the IEEE*, Nov 2015, pp. 003 614–003 619.

[242] M. Aly, G. M. Dousoky, E. M. Ahmed, and M. Shoyama, "A unified svm algorithm for lifetime prolongation of thermally-overheated power devices in multi-level inverters," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–6.

[243] M. Aly, E. M. Ahmed, and M. Shoyama, "Thermal stresses relief carrier-based pwm strategy for single-phase multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9376–9388, 2017.

[244] J. Ruthardt, J. Woelfle, M. Zehelein, and J. Roth-Stielow, "A new modulation technique to control the switching losses for single phase three-level active-neutral-point-clamped-inverters," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, pp. 1–8.

[245] M. Novak, V. N. Ferreira, M. Andresen *et al.*, "Fs-mpc algorithm for optimized operation of a hybrid active neutral point clamped converter," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1447–1453.

[246] A. Anuchin, V. Podzorova, V. Popova *et al.*, "Model predictive torque control of a switched reluctance drive with heat dissipation balancing in a power converter," in

2019 IEEE 60th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), 2019, pp. 1–6.

[247] M. Novak and F. Blaabjerg, "Model predictive active thermal control strategy for lifetime extension of a 3l-npc converter for ups applications," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1–7.

[248] M. Novak, V. Ferreira, F. Blaabjerg, and M. Liserre, "Evaluation of carrier-based control strategies for balancing the thermal stress of a hybrid sic anpc converter," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2077–2083.

[249] M. Novak, V. Ferreira, M. Andresen *et al.*, "Fs-mpc based thermal stress balancing and reliability analysis for npc converters," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 124–137, 2021.

[250] W. He, C. Ma, S. Zhang *et al.*, "An active thermal control scheme of three-level npc inverters," in *2022 IEEE 17th Conference on Industrial Electronics and Applications (ICIEA)*, 2022, pp. 540–544.

[251] A. Tcai, T. Wijekoon, and M. Liserre, "Thermal control of quasi-2-level super-switch by power routing," *IEEE Transactions on Industrial Electronics*, pp. 1–9, 2023.

[252] F. Hahn, G. Buticchi, and M. Liserre, "Active thermal balancing for modular multilevel converters in hvdc applications," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1–10.

[253] Q. Yang and M. Saeedifard, "Active thermal loading control of the modular multilevel converter by a multi-objective optimization method," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 4482–4487.

[254] F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, "Thermal analysis and balancing for modular multilevel converters in hvdc applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1985–1996, March 2018.

[255] Y. Dong, H. Yang, W. Li, and X. He, "Neutral-point-shift-based active thermal control for a modular multilevel converter under a single-phase-to-ground fault," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2474–2484, mar 2019.

[256] W. Li, H. Yang, J. Sheng *et al.*, "Thermal optimization of modular multilevel converters with surplus submodule active-bypass plus neutral-point-shift scheme under unbalanced grid conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1777–1788, 2019.

[257] J. Sheng, H. Yang, C. Li *et al.*, "Active thermal control for hybrid modular multilevel converter under overmodulation operation," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4242–4255, 2020.

[258] R. Han, Q. Xu, H. Ding *et al.*, "Thermal stress balancing oriented model predictive control of modular multilevel switching power amplifier," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 11, pp. 9028–9038, nov 2020.

[259] H. Ding, F. Ma, R. Han *et al.*, "A junction temperature balance control among submodules for modular multilevel converter," in *IECON 2021 - 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1–6.

[260] F. Deng, J. Zhao, C. Liu *et al.*, "Temperature-balancing control for modular multilevel converters under unbalanced grid voltages," *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4614–4625, 2022.

[261] H. Ding, F. Ma, R. Han *et al.*, "Junction temperature optimization based compensation strategy of modular multilevel railway power conditioner," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6585–6598, 2022.

[262] Y. Kazemirova, S. Grishin, N. Balashenko *et al.*, "Thermal condition equalization of power modules in a low-voltage cell of modular multilevel converter," in *2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2022, pp. 742–747.

[263] Y. Ko, M. Andresen, G. Buticchi, J.-S. Lee, and M. Liserre, "Modulation strategy for highly reliable cascade h-bridge inverter based on discontinuous pwm," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3241–3246.

[264] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Thermally compensated discontinuous modulation strategy for cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2704–2713, 2018.

[265] V. G. Monopoli, A. Marquez, J. I. Leon *et al.*, "Improved harmonic performance of cascaded h-bridge converters with thermal control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 4982–4991, 2019.

[266] A. Marquez, V. G. Monopoli, J. I. Leon *et al.*, "Sampling-time harmonic control for cascaded h-bridge converters with thermal control," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 4, pp. 2776–2785, 2020.

[267] Y. Ko, V. Raveendran, M. Andresen, and M. Liserre, "Advanced discontinuous modulation for thermally compensated modular smart transformers," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2445–2457, 2020.

[268] ——, "Thermally compensated discontinuous modulation for mvac/lvdc building blocks of modular smart transformers," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 220–231, 2020.

[269] J. Yu, J. Zhang, R. Lu *et al.*, "Active thermal control for cascaded h-bridges in solid state transformers," in *2021 IEEE 1st International Power Electronics and Application Symposium (PEAS)*, 2021, pp. 1–6.

[270] Q. Chen, X. Yang, and Z.-a. Wang, "Active balancing temperature control strategy for the parallel ipem-based converters," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–5.

[271] S. Dusmez and B. Akin, "An active life extension strategy for thermally aged power switches based on the pulse-width adjustment method in interleaved converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5149–5160, 2016.

[272] Y. Ko, M. Andresen, G. Buticchi, M. Liserre, and L. Concari, "Multi-frequency power routing for cascaded h-bridge inverters in smart transformer application," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7.

[273] G. Buticchi, M. Andresen, M. Wutti, and M. Liserre, "Lifetime-based power routing of a quadruple active bridge dc/dc converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8892–8903, 2017.

[274] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Power routing for cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9435–9446, 2017.

[275] Y. Ko, V. Raveendran, M. Andresen, and M. Liserre, "Discontinuous modulation based power routing for modular smart transformers," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1084–1090.

[276] S. Peyghami, P. Davari, and F. Blaabjerg, "System-level lifetime-oriented power sharing control of paralleled dc/dc converters," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1890–1895.

[277] K. Desingu, R. Selvaraj, and T. R. Chelliah, "Control of reactive power for stabilized junction temperature in power electronic devices serving to a 250-mw asynchronous hydrogenerating unit," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7854–7867, 2019.

[278] A. Marquez, J. I. Leon, F. Hahn *et al.*, "Power devices aging equalization of interleaved dc-dc boost converters via power routing," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 1, no. 1, pp. 91–101, 2020.

[279] M. Liserre, V. Raveendran, and M. Andresen, "Graph-theory-based modeling and control for system-level optimization of smart transformers," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8910–8920, 2020.

[280] T. Xu, F. Gao, and Z. Liu, "Coordinated active thermal control for parallel-connected inverters using global synchronous pulse width modulation," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 2728–2731.

[281] P. Tan, T. Xu, and F. Gao, "General coordinated active thermal control for parallel-connected inverters with switching frequency control," in *2021 IEEE 1st International Power Electronics and Application Symposium (PEAS)*, 2021, pp. 1–6.

[282] H. Wang, A. M. Khambadkone, and X. Yu, "Control of parallel connected power converters for low voltage microgrid-part ii: Dynamic electrothermal modeling," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 2971–2980, 2010.

[283] V. Raveendran, M. Andresen, and M. Liserre, "Reliability oriented control of dc/dc converters for more electric aircraft," in *2018 IEEE 27th International Symposium on Industrial Electronics (ISIE)*, 2018, pp. 1352–1358.

[284] Y. Wang, D. Liu, F. Deng, D. Zhou, and Z. Chen, "Lifetime-oriented droop control strategy for ac islanded microgrids," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 1758–1763.

[285] V. Raveendran, M. Andresen, and M. Liserre, "Improving onboard converter reliability for more electric aircraft with lifetime-based control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5787–5796, 2019.

[286] S. Peyghami, P. Davari, and F. Blaabjerg, "System-level reliability-oriented power sharing strategy for dc power systems," *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 4865–4875, 2019.

[287] J. Jiang, S. Peyghami, C. Coates, and F. Blaabjerg, "A decentralized reliability-enhanced power sharing strategy for pv-based microgrids," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 7281–7293, 2021.

[288] M. Liserre, M. Andresen, L. Costa, and G. Buticchi, "Power routing in modular smart transformers: Active thermal control through uneven loading of cells," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43–53, Sept 2016.

[289] V. Raveendran, M. Andresen, G. Buticchi, and M. Liserre, "Reliability enhancement of modular smart transformers by uneven loading of cells," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, pp. 1–8.

[290] V. Raveendran, G. Buticchi, A. Mercante, and M. Liserre, "Comparison of voltage control methods of chb converters for power routing in smart transformer," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 1652–1658.

[291] M. Andresen, V. Raveendran, G. Buticchi, and M. Liserre, "Lifetime-based power routing in parallel converters for smart transformer application," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[292] V. Raveendran, M. Andresen, and M. Liserre, "Graph theory-based power routing in modular power converters considering efficiency and reliability," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 1237–1242.

[293] V. Raveendran, M. Andresen, M. Liserre, and G. Buticchi, "Lifetime-based power routing of smart transformer with chb and dab converters," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 3523–3529.

[294] A. Marquez, J. I. Leon, S. Vazquez, and L. G. Franquelo, "Closed-loop active thermal control via power routing of parallel dc-dc converters," in *2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018)*, 2018, pp. 1–6.

[295] V. Raveendran, M. Andresen, G. Buticchi, and M. Liserre, "Thermal stress based power routing of smart transformer with chb and dab converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4205–4215, 2020.

[296] V. N. Ferreira, R. R. Bastos, T. S. de Souza, M. Liserre, and B. J. Cardoso Filho, "Power routing to enhance the lifetime of multiphase drives," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 3215–3222.

[297] H. Yan, G. Buticchi, J. Yang *et al.*, "Active thermal control for power converters in modular winding permanent magnet synchronous motor," in *2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2019, pp. 1–6.

[298] H. Yan, W. Zhao, G. Buticchi, and C. Gerada, "Active thermal control for modular power converters in multi-phase permanent magnet synchronous motor drive system," *IEEE Access*, vol. 9, pp. 7054–7063, 2021.

[299] V. Ferreira, T. S. de Souza, R. R. Bastos, M. Liserre, and B. Cardoso, "Soft-unbalance operation for power routing in multiphase drives," *IEEE Transactions on Industry Applications*, vol. 58, no. 1, pp. 435–443, 2022.

[300] J. Harikumaran, G. Buticchi, G. MIgliazza, P. Wheeler, and M. Galea, "Reliability oriented thermal management of aircraft power converters," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 1590–1594.

[301] J. Zhang, J. Wang, and X. Cai, "Active thermal control-based anticondensation strategy in paralleled wind power converters by adjusting reactive circulating current," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 277–291, 2018.

[302] S. Ravyts, G. V. d. Broeck, L. Hallemans, M. D. Vecchia, and J. Driesen, "Fuse-based short-circuit protection of converter controlled low-voltage dc grids," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11 694–11 706, 2020.

[303] N. Bayati, H. R. Baghaee, A. Hajizadeh, and M. Soltani, "A fuse saving scheme for dc microgrids with high penetration of renewable energy resources," *IEEE Access*, vol. 8, pp. 137 407–137 417, 2020.

[304] J. Zhu, *Power systems applications of graph theory*. Nova Science Publishers, 2009.

[305] S. Arumugam, A. Brandstädt, T. Nishizeki *et al.*, *Handbook of graph theory, combinatorial optimization, and algorithms*. CRC Press, 2016, vol. 34.

[306] R. Diestel, *Graph Theory*. Springer, 2017.

[307] T. Bruckner and D. Holmes, "Optimal pulse width modulation for three-level inverters," in *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, vol. 1, 2003, pp. 165–170 vol.1.

[308] R. Pena-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez, and Y. Yang, "Lcl-filter design for robust active damping in grid-connected converters," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 4, pp. 2192–2203, 2014.

[309] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*. Wiley, 2011.

[310] T. A. Pereira, L. Camurca, Y. Ko, R. Zhu, and M. Liserre, "Protection and management of internal faults in modular smart transformer," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1762–1769.

[311] S. Julier and J. Uhlmann, "Unscented filtering and nonlinear estimation," *Proceedings of the IEEE*, vol. 92, no. 3, pp. 401–422, 2004.

[312] F. Santos-Arana, Y. Pascal, J. Kuprat *et al.*, "Optical sensing applied to thermal observers for enhanced reliability of power modules," in *2022 IEEE 13th International*

Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2022, pp. 1–5.

[313] M. Langwasser, K. Schönleber, A. Wasserrab, M. Thiele, and M. Liserre, "Online estimation of dynamic capacity of vsc-hvdc systems - power system use cases," in *ETG Congress 2021*, 2021, pp. 704–709.

[314] T. Guillod, F. Krismer, and J. W. Kolar, "Protection of mv converters in the grid: The case of mv/lv solid-state transformers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 393–408, 2017.

List of Figures

List of Tables

Appendix A.

Journal publications

J1 **J. Kuprat**, K. Debbadi, J. Schaumburg, M. Liserre and M. Langwasser, "Thermal Digital Twin of Power Electronics Modules for Online Thermal Parameter Identification," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2023.3328219.

J2 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Mission Profile-Tailored Design and Control of an Interconnected Hybrid Grid Connecting Converter Architecture," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2023.3278082.

J3 J. Schaumburg, **J. Kuprat**, M. Langwasser and M. Liserre, "Efficiency Optimization via Mission Profile-Based Power Routing by Design of Hybrid Grid Connecting Converter Architecture," in *IEEE Open Journal of Power Electronics*, doi: 10.1109/OJPEL.2023.3241778.

J4 S. Pugliese, O. Landsiedel, **J. Kuprat** and M. Liserre, "Cross domain fusion in power electronics dominated distribution grids," in *Informatik Spektrum*, 2022, doi: 10.1007/s00287-022-01495-8.

J5 Y. Li, **J. Kuprat**, Y. Li and M. Liserre, "Graph-Theory-Based Derivation, Modeling and Control of Power Converter Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2022.3143437.

J6 Y. Ko, **J. Kuprat**, S. Pugliese and M. Liserre, "Modulation Strategies for Thermal Stress Control of CHB Inverters," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3515-3527, March 2022, doi: 10.1109/TPEL.2021.3117917.

J7 **J. Kuprat**, C. H. van der Broeck, M. Andresen, S. Kalker, M. Liserre and R. W. De Doncker, "Research on Active Thermal Control: Actual Status and Future Trends," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6494-6506, Dec. 2021, doi: 10.1109/JESTPE.2021.3067782.

J8 S. Kalker, L. A. Ruppert, C. H. van der Broeck, **J. Kuprat**, M. Andresen, T. A. Polom, M. Liserre and R. W. De Doncker, "Reviewing Thermal Monitoring Techniques for Smart Power Modules," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2021.3063305.

J9 M. Andresen, **J. Kuprat**, V. Raveendran, J. Falck and M. Liserre, "Active thermal control for delaying maintenance of power electronics converters," in *Chinese Journal*

of Electrical Engineering, vol. 4, no. 3, pp. 13-20, September 2018, doi: 10.23919/CJEE.2018.8471285.

Conference publications

C1 **J. Kuprat**, Y. Pascal and M. Liserre, "Real-Time Thermal Characterization of Power Semiconductors using a PSO-based Digital Twin Approach," *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022, pp. P.1-P.8.

C2 F. Santos-Arana, Y. Pascal, **J. Kuprat**, M. Langwasser, K. Debbadi and M. Liserre, "Optical Sensing Applied to Thermal Observers for Enhanced Reliability of Power Modules," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-5, doi: 10.1109/PEDG54999.2022.9923139.

C3 J. Schaumburg, **J. Kuprat**, M. Langwasser and M. Liserre, "Efficiency Optimization via Mission Profile-Based Design of a Hybrid Grids-Feeding Smart Transformer," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-6, doi: 10.1109/PEDG54999.2022.9923058.

C4 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Improved Graph-Theory Based Modeling of the Smart Transformer for Hybrid Grids," *2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, 2022, pp. 1-6, doi: 10.1109/CPE-POWERENG54966.2022.9880867.

C5 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Mission-Profile Based Design of a Hybrid-Grids Feeding Smart Transformer," *2021 6th IEEE Workshop on the Electronic Grid (eGRID)*, 2021, pp. 01-08, doi: 10.1109/eGRID52793.2021.9662152.

C6 **J. Kuprat**, M. Andresen, V. Raveendran and M. Liserre, "Modular Smart Transformer Topology for the Interconnection of Multiple Isolated AC and DC Grids," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4836-4841, doi: 10.1109/ECCE44975.2020.9236136.

Veröffentlichungen des Autors mit Angaben über die Höhe des Eigenanteils bei Publikationen/Manuskripten mit mehreren Autoren

Publikationen in Fachzeitschriften

J1 **J. Kuprat**, K. Debbadi, J. Schaumburg, M. Liserre and M. Langwasser, "Thermal Digital Twin of Power Electronics Modules for Online Thermal Parameter Identification," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2023.3328219.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	hoch

J2 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Mission Profile-Tailored Design and Control of an Interconnected Hybrid Grid Connecting Converter Architecture," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2023.3278082.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	hoch

J3 J. Schaumburg, **J. Kuprat**, M. Langwasser and M. Liserre, "Efficiency Optimization via Mission Profile-Based Power Routing by Design of a Hybrid Grid Connecting Converter Architecture," in *IEEE Open Journal of Power Electronics*, doi: 10.1109/OJPEL.2023.3241778.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	mittel

J4 S. Pugliese, O. Landsiedel, **J. Kuprat** and M. Liserre, "Cross domain fusion in power electronics dominated distribution grids," in *Informatik Spektrum*, 2022, doi: 10.1007/s00287-022-01495-8.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	mittel	mittel	mittel

J5 Y. Li, **J. Kuprat**, Y. Li and M. Liserre, "Graph-Theory-Based Derivation, Modeling and Control of Power Converter Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2022.3143437.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
niedrig	mittel	mittel	mittel

J6 Y. Ko, **J. Kuprat**, S. Pugliese and M. Liserre, "Modulation Strategies for Thermal Stress Control of CHB Inverters," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3515-3527, March 2022, doi: 10.1109/TPEL.2021.3117917.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
niedrig	mittel	hoch	mittel

J7 **J. Kuprat**, C. H. van der Broeck, M. Andresen, S. Kalker, M. Liserre and R. W. De Doncker, "Research on Active Thermal Control: Actual Status and Future Trends," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6494-6506, Dec. 2021, doi: 10.1109/JESTPE.2021.3067782.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	hoch

J8 S. Kalker, L. A. Ruppert, C. H. van der Broeck, **J. Kuprat**, M. Andresen, T. A. Polom, M. Liserre and R. W. De Doncker, "Reviewing Thermal Monitoring Techniques for Smart Power Modules," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2021.3063305.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
mittel	niedrig	niedrig	mittel

J9 M. Andresen, **J. Kuprat**, V. Raveendran, J. Falck and M. Liserre, "Active thermal control for delaying maintenance of power electronics converters," in *Chinese Journal of Electrical Engineering*, vol. 4, no. 3, pp. 13-20, September 2018, doi: 10.23919/CJEE.2018.8471285.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	mittel	mittel

Publikationen auf Fachkonferenzen

C1 **J. Kuprat**, Y. Pascal and M. Liserre, "Real-Time Thermal Characterization of Power Semiconductors using a PSO-based Digital Twin Approach," *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022, pp. P.1-P.8.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	hoch

C2 F. Santos-Arana, Y. Pascal, **J. Kuprat**, M. Langwasser, K. Debbadi and M. Liserre, "Optical Sensing Applied to Thermal Observers for Enhanced Reliability of Power Modules," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-5, doi: 10.1109/PEDG54999.2022.9923139.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	mittel	mittel

C3 J. Schaumburg, **J. Kuprat**, M. Langwasser and M. Liserre, "Efficiency Optimization via Mission Profile-Based Design of a Hybrid Grids-Feeding Smart Transformer," *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-6, doi: 10.1109/PEDG54999.2022.9923058.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	mittel

C4 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Improved Graph-Theory Based Modeling of the Smart Transformer for Hybrid Grids," *2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, 2022, pp. 1-6, doi: 10.1109/CPE-POWERENG54966.2022.9880867.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	hoch

C5 **J. Kuprat**, J. Schaumburg, M. Langwasser and M. Liserre, "Mission-Profile Based Design of a Hybrid-Grids Feeding Smart Transformer," *2021 6th IEEE Workshop on the Electronic Grid (eGRID)*, 2021, pp. 01-08, doi: 10.1109/eGRID52793.2021.9662152.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	hoch

C6 **J. Kuprat**, M. Andresen, V. Raveendran and M. Liserre, "Modular Smart Transformer Topology for the Interconnection of Multiple Isolated AC and DC Grids," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4836-4841, doi: 10.1109/ECCE44975.2020.9236136.

Konzeptionierung	Planung	Durchführung	Manuskripterstellung
hoch	hoch	hoch	hoch