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Optimal Design of Supercapacitor Stacks for Size-critical Applications

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Abstract—Power processing applications with large transient requirements employ supercapacitors (SCs) as compact energy storage. The miniaturization of SC stacks facilitates their integration into such systems, especially when size constraints are to be met. Existing design guidelines for SC stacks do not clearly address the minimization of stack size considering the simultaneous requirements of power and energy. In this paper, a size-optimal discharge ratio (SODR) is derived to reduce the size of SC stacks while meeting the power and energy demands of an application. A design approach for SC stacks, capable of accommodating SC parameter variations, is outlined based on the proposed SODR. The SODR is also compatible with existing design approaches. Using the SODR, backup durations suitable for SCs are quantified in comparison with other storage technologies. The optimality of the SC stack size achieved by the proposed SODR-based design method is validated through circuit simulation and in experiments on a fabricated SC stack.

Index Terms—discharge ratio, stack sizing, supercapacitor.

I. INTRODUCTION

Supercapacitors (SCs) are employed for short-term energy storage in various size-critical applications such as data centers, electric transportation, and industrial machinery [1]. This motivates the reduction of the volumetric and/or gravimetric size of SC-based storage while meeting the energy and power demands of the application. The optimal sizing of SC stacks is central to their use and is explored in the literature [2]–[8].

The terminal voltage of an SC stack varies over a wide range during operation. This variation is quantified by the discharge ratio (DR), defined as the ratio between the minimum operating voltage of the stack and its nominal voltage. SC stack designs described in the literature identify the DR as a design parameter.

The DR is set to 50% in the designs described in [2] and [3], which focus on other aspects of the SC stack. An analytical discussion of the storage capability of SCs is presented in [4], although design guidelines are not clearly stated. The size optimization of a combined SC/battery storage is achieved numerically in [5]; the implementation does not consider SC power delivery limits or optimize the DR. A detailed design methodology for SC stacks is presented in [6], including an analytical framework for optimizing the DR to minimize total system cost. However, this optimization is sensitive to the assumed costs of power and energy, whose accurate quantification is a challenge. While a theoretical power limit is used in [6] and [7], the effect of the DR on power delivery

is not considered further. These gaps in the literature motivate the investigation of an optimal DR to reduce SC stack size.

The drawback of designing a SC stack from energy considerations alone is identified in [8], where power requirements are additionally used to size the stack. However, the focus is on the design of the complete power train and hence, the observation regarding the identified power and energy limits is not elaborated further. The energy delivered by an SC stack is high if the value of the DR is low, while the power delivery capability of the stack is high at high values of DR. This inherent trade-off forms the basis of the existence of the optimal DR explored in the present study.

This paper proposes size-optimal design methods for SC stacks to complement existing design algorithms. The key contributions of this paper are:

- (i) the analytical formulation of the size-optimal discharge ratio (SODR) for an SC stack based on both application requirements and limits of power and energy,
- (ii) the use of the SODR to quantify a size-optimal backup duration for SC stacks, and its comparison with that of batteries and electrolytic capacitors,
- (iii) the outlining of SC stack design guidelines based on the SODR,
- (iv) the discussion of refinements to the SODR-based analysis and design methodology to accommodate parameter variations, and
- (v) the validation of results in circuit simulation and experiment.

This paper is organized as follows. The size of an SC stack is formulated in terms of energy and power requirements in Section II. An optimal discharge ratio that minimizes the size of the SC stack is proposed in Section III. Guidelines to design SC stacks based on the proposed SODR are detailed in Section IV. The size-optimality of the proposed stack design method is validated through simulations and experiments, and the results presented in Section V. Section VI concludes the paper.

II. POWER AND ENERGY REQUIREMENT-BASED SIZING

The schematic of an SC stack interfaced to a constant-voltage DC bus is shown in Fig. 1a. A power electronic interface (PEI) is necessary to adapt the variable voltage of the SC stack to the constant DC bus voltage. The losses in the PEI are neglected in the present discussion. The parameters relevant to

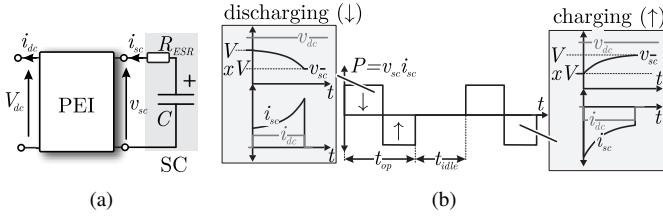


Fig. 1: (a) Circuit schematic of the SC stack interfaced, through the PEI, to the DC bus. (b) Waveforms of the terminal voltage, current, and power of the SC as well as DC bus voltage and current. Charging, discharging, and idle phases of operation are shown.

the limits of operation of the SC stack are its nominal voltage, V , capacitance, C , and effective series resistance (ESR), R .

Operating waveforms of the DC bus voltage (v_{dc}) and current (i_{dc}), and SC stack voltage (v_{sc}) and current (i_{sc}) are presented in Fig. 1b. The stack is discharged to support contingencies or transient power requirements at the DC bus, and recharged subsequently when possible. The stack is in an idle state for the remaining duration (t_{idle}). During operation, the stack is discharged down to a fraction (x) of its nominal voltage. This fraction is termed as the discharge ratio (DR).

For a given load requirement, the size of the SC stack is inversely proportional to its energy and power densities. The effective values of both these densities depend on the DR.

A. Effective Energy Density

The energy, E_0 , stored in the stack at nominal condition, is given by (1).

$$E_0 = 0.5CV^2 \quad (1)$$

The nominal energy density (U_0) is obtained as the nominal energy stored per unit stack size, S , as (2). The measure of stack size, e.g., weight or volume, is represented by the quantity, S .

$$U_0 = E_0/S \quad (2)$$

The fraction of the nominal energy (and hence, the nominal energy density) utilized depends on the extent to which the stack is discharged during operation. Hence, the effective energy density (U) is proportional to the difference between the stored energies at maximum (V) and minimum (xV) stack voltages, as (3).

$$U(x) = U_0(1 - x^2) \quad (3)$$

Thus, the effective energy density of an SC stack increases with the extent of discharge, i.e., with a decrease in the discharge ratio, x .

B. Effective Power Density for Continuous-Duty Operation

The power density achievable with an SC stack depends not only on the DR, but also on the duty of operation. Applications such as SC-only electric transport operate the SC stack with persistent charging and discharging, i.e., at continuous duty (CD). Under this scenario, the operating duration (t_{op}) of the

stack is much longer than the idle duration (t_{idle}) in Fig. 1b, i.e., $t_{op} \gg t_{idle}$.

For CD operation, the temperature rise in the supercapacitor ESR is a factor that limits the power delivery from the stack; in these cases, the current through the SC is restricted within a specified upper limit (I_{max}) [9]. These considerations define the nominal power limit in CD cases, $P_{0,c}$, as (4).

$$P_{0,c} = VI_{max} \quad (4)$$

The nominal continuous-duty power density ($\Pi_{0,c}$) is obtained in terms of the nominal power limit and the stack size as (5).

$$\Pi_{0,c} = P_{0,c}/S \quad (5)$$

For operation at or below a specified stack current limit, the power delivered by an SC stack reduces with its voltage. Thus, the effective power density for continuous-duty operation is proportional to the minimum stack voltage, and given by (6).

$$\Pi_c(x) = x\Pi_{0,c} \quad (6)$$

For continuous-duty operation, (6) indicates an increase in the effective power density of the stack with an increase in the discharge ratio.

C. Effective Power Density for Intermittent-Duty Operation

In backup applications, SCs operate only during contingencies, i.e., at intermittent duty (ID). Thus, the idle duration (t_{idle}) in Fig. 1b is much longer than the duration of operation (t_{op}), as $t_{idle} \gg t_{op}$. The long idle duration assists in cooling, and the thermal restrictions are relaxed in contrast to continuous-duty operation. The power limit in these cases is dictated by the voltage drop in the ESR, which becomes prohibitively large as the current through the SC increases [10]. The nominal ID power limit is hence obtained from [10] as (5).

$$P_{0,i} = 0.12V^2/R \quad (7)$$

The nominal intermittent-duty power density, which is equal to the maximum deliverable power per unit stack size, is obtained as (8).

$$\Pi_{0,i} = P_{0,i}/S \quad (8)$$

Since the maximum power is proportional to the square of the operating voltage, the power limit is decided at the minimum operating voltage of the stack. Thus, the intermittent-duty power density is proportional to the square of the DR. The effective power density for intermittent duty, Π_i , is hence derived in terms of the nominal density as (9).

$$\Pi_i(x) = x^2\Pi_{0,i} \quad (9)$$

Thus, the effective intermittent-duty power density increases with the discharge ratio of the stack.

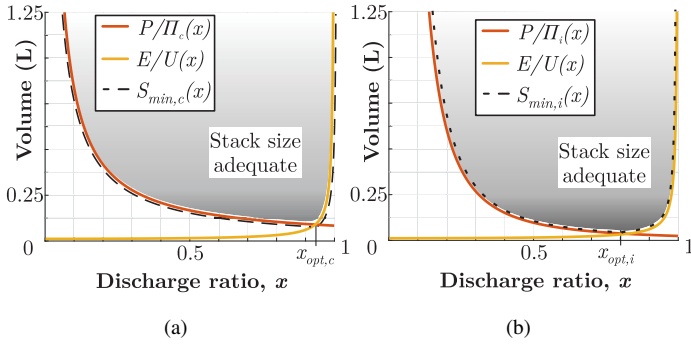


Fig. 2: The variation of the minimum size of a stack (dotted) with discharge ratio for $P = 250$ W, $E = 250$ J. The individual power (red) and energy (yellow) constraints on stack size, and the SODR (x_{opt}) for each case, are also shown. Graphs for (a) continuous-duty and (b) intermittent-duty operation.

D. Influence of Power and Energy Densities on Stack Size

The SC stack is sized to satisfy the worst-case requirements of power (P) and energy (E) for a given application. Designing for the worst case ensures that load demands are met even for fluctuating loads, e.g., that in [7].

The stack is sized to meet the peak power demand of the load. For a specified duty of operation, the stack size (S) must satisfy the relation in (10) for a given power density (Π) of the stack.

$$S \geq P/\Pi(x) \quad (10)$$

The energy requirement for the stack is obtained indirectly from application-specific requirements. For example, for continuous-duty operation in a transportation application, the range of the vehicle between charging points decides the energy required from the supercapacitor [11]. Similarly, in intermediate-duty contingency applications, the energy requirement from the SC stack depends on the worst-case backup duration [6]. The SC stack size (S) to meet these requirements satisfies the relation in (11).

$$S \geq E/U(x) \quad (11)$$

The stack is designed to satisfy the power relation (10) and the energy relation in (11). These relations are represented graphically for continuous-duty and intermittent-duty operation, in Figs. 2a and 2b, respectively. The stack size that satisfies load requirements for a given discharge ratio is shaded. The minimal size of the SC stack (S_{min}), simultaneously satisfying the power requirement in (10) and the energy requirement in (11), is given by (12) and shown as a dotted line in Figs. 2a and 2b.

$$S_{min}(x) = \max(P/\Pi(x), E/U(x)) \quad (12)$$

The minimal stack size, S_{min} , is thus a function of the discharge ratio, x , and is further minimized at the size-optimal discharge ratio (SODR), x_{opt} , which is marked in both graphs.

III. MINIMIZATION OF SIZE BASED ON THE SODR

As evident from Figs. 2a and 2b, the power and energy constraints on SC stack size show contrasting trends of variation with discharge ratio, x . Hence, the arguments of the $\max(\cdot)$ function in the stack size expression in (12) have opposing slopes. At the optimal value, x_{opt} , of the discharge ratio, the arguments of the $\max(\cdot)$ function in (12) are equal, as (13).

$$P/\Pi(x_{opt}) = E/U(x_{opt}) \quad (13)$$

The condition of minimal stack size is given by (13).

A. Continuous-Duty SODR

Substituting the energy density relation in (3) and the continuous-duty power relation in (6) into the condition in (13) yields (14).

$$\frac{P}{x\Pi_{0,c}} = \frac{E}{U_0(1-x^2)} \quad (14)$$

The expression for the continuous-duty SODR ($x_{opt,c}$) is obtained, by solving (14), as (15).

$$x_{opt,c} = 0.5(\sqrt{\alpha^2 + 4} - \alpha), \text{ where } \alpha \triangleq E\Pi_{0,c}/(PU_0) \quad (15)$$

B. Intermittent-Duty SODR

The intermittent-duty power density in (9) and the energy density in (3) are substituted into the minimal-size condition in (13) to obtain (16).

$$\frac{P}{x^2\Pi_{0,i}} = \frac{E}{U_0(1-x^2)} \quad (16)$$

Solving (16) yields the intermittent-duty SODR, $x_{opt,i}$, as (17).

$$x_{opt,i} = \sqrt{PU_0/(PU_0 + E\Pi_{0,i})} \quad (17)$$

C. Applications of the SODR to Stack Design

The SODRs derived above, $x_{opt,c}$ and $x_{opt,i}$, minimize the size of SC stacks operating at CD and ID respectively. Each SODR depends only on

- (i) the ratio of the worst-case energy and power requirements (E/P), and
- (ii) the ratio of the nominal energy and power densities (U_0/Π_0).

The nominal power and energy densities are dependent on the SC used, but not on the number of SCs in the stack. Hence, the same SODR is applicable both at the single-SC and the stack levels. This scalability of the SODR is useful for integrating it into existing stack design algorithms.

The SODR-based analysis offers quantitative insights into the relative size of storage technology for backup applications. Such applications typically feature a constant load power profile over the backup duration, T . Hence, the energy and the power requirements are related as $E = PT$. The substitution of the backup duration, T , and $x_{opt,i}$ from (17) in the

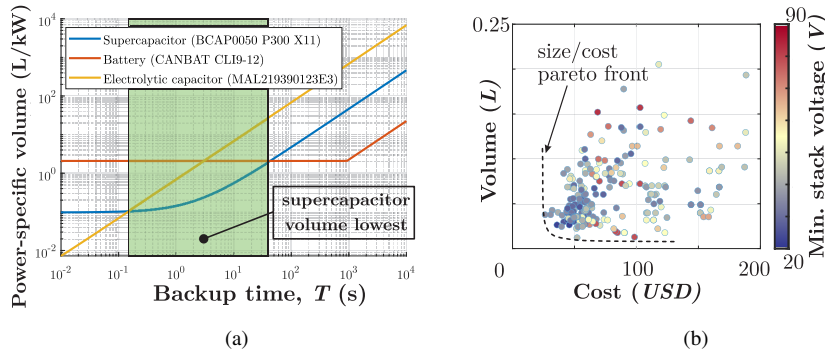


Fig. 3: (a) Comparison of specific volumes for SC-, EC-, and battery-based storage, highlighting the backup duration where the SC provides a size advantage. (b) Volume, cost, and minimum stack voltage comparison for commercial supercapacitors with a volume-cost pareto.

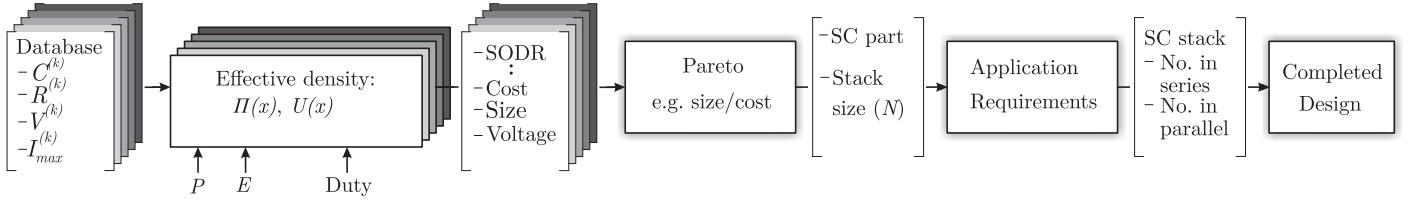


Fig. 4: Design flow based on the proposed SODR for an SC stack using commercial off-the-shelf SCs.

minimum size relation in (12) yields the minimum required SC stack size for intermittent duty, $S_{min,i}$, as (18).

$$S_{min,i} = P(1/\Pi_{i,0} + T/U_0) \quad (18)$$

At a given power level (P), the quantity, S_{min} , depends on the backup duration (T), and on the energy and power density of the SC technology. The size of electrolytic capacitor-based storage is similarly derived using the SODR.

The storage size required is compared for an SC (BCAP0050), an electrolytic capacitor (MAL2193), and a battery (CLI9-12) in Fig. 3a. The power and energy densities of these components are obtained using respective datasheet parameters. The SODRs of the SC and the electrolytic capacitor are used to compute the minimal size required, while the required size of the battery is obtained by imposing the more stringent of the .

The storage sizes plotted in Fig. 3a increase non-uniformly with the required backup duration, T . The flat segments of the curves at low backup durations indicate that the size is constrained by power considerations. This flat segment extends up to longer durations for the battery, indicating a higher energy density to power density ratio. The SC size is lowest in an interval intermediate between short (<100 ms) and long (>60 s) durations, motivating the application of SCs in this backup regime.

IV. STACK DESIGN GUIDELINES

Iterative stack design algorithms, e.g., that in [6], include a design step to select the discharge ratio of the stack. The proposed SODR depends only on energy/power ratios and is compatible with existing design algorithms. An alternative

design flow from off-the-shelf SCs is outlined as follows. The algorithm successively defines

- (i) the off-the-shelf SC part,
- (ii) the number of SCs required, and
- (iii) the series/parallel configuration of SCs in the stack.

As discussed in section III, the SODR depends on the ratio of power (P) and energy (E) requirements of the application. This quantity is fixed for a given application. The SODR also depends on the ratio of power (Π_0) and energy (U_0) densities of the selected SC part. However, the SODR is independent of the number of such SCs in the stack. This renders the same SODR applicable at the level of the single-SC and at the level of the stack, provided the voltage capability of the SCs in the stack is well-utilized, as is typical [6].

The design flow is illustrated in Fig. 4. The algorithm starts with a database of off-the-shelf SC parts, indexed by the variable, k , with corresponding parameters ($C^{(k)}$, $R^{(k)}$, $V^{(k)}$, $I_{max}^{(k)}$). These parameters, together with the duty of operation, are used to evaluate the effective power (Π) and energy (U) densities for each SC in the database, using (6), (9), and (3).

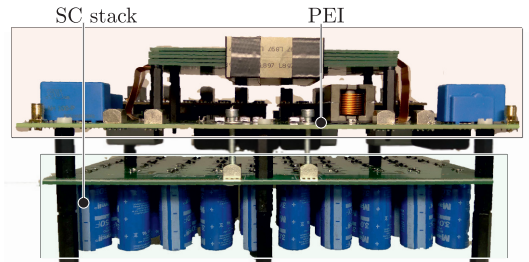


Fig. 5: Laboratory prototype of the SC stack and PEI.

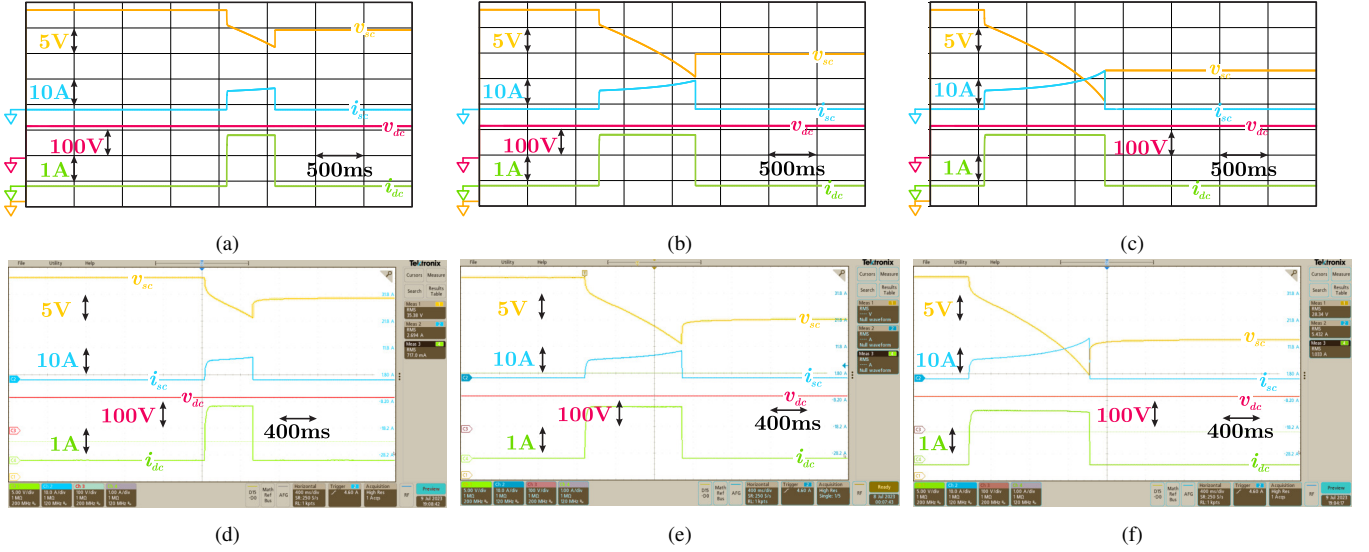


Fig. 6: Operating waveforms of SC and DC link quantities at a load power of 250 W. Simulated waveforms for discharge ratios (a) higher than, (b) equal to, and (c) lower than the SODR. Corresponding experimental waveforms for discharge ratios (d) higher than, (e) equal to, and (f) lower than the SODR.

TABLE I
RATINGS OF THE LOAD

DC bus voltage, v_{dc}	125 V
Load power, P	250 W
Backup time, T	1.0 s
Duty of operation	intermittent (ID)

TABLE II
PARAMETERS OF THE FABRICATED SC STACK

Capacitance, C	1.0 F
ESR, R	0.4 Ω
Max. SC voltage, V	37.5 V
SODR, $x_{opt,i}$	0.79

The SODR, x_{opt} is then evaluated for each SC by substituting these densities and the application requirements (P , E) into (15) or (17), according to the operating duty.

The number (N) of SCs required is calculated for each off-the-shelf part, as

$$N \approx P/\Pi(x_{opt}) = E/U(x_{opt}). \quad (19)$$

At this stage, the stack size and cost for each choice of off-the-shelf SCs is calculated. Application-specific preferences are then imposed on the resulting stacks to select the most suitable SC part, as shown in Fig. 3b. Along with pareto optimality, this selection is informed by the minimum stack voltage, which is also relevant to stack design.

SCs require auxiliary electronics in the form of the PEI and cell voltage balancers [12] which present trade-offs with regard to the series/parallel configuration of SCs in a stack. A large number of series-connected SCs increases the SC stack voltage, relaxing the voltage gain requirements on the PEI while complicating the monitoring and balancing of individual cells, and affecting the tolerance of the stack to SC failure. Predominantly parallel-connected strings eliminate these issues, but impose higher voltage gain and current requirements on the PEI. The series/parallel architecture is influenced by these considerations, and the final decision depends on application-specific preferences. The value of N is adjusted to accommodate arithmetic requirements.

A. Considerations of Stack Parameter Variation

The value of the SODR is sensitive to the parameters (R and/or C) of the SC stack. These parameters vary across off-the-shelf parts and also over the operating voltage range of an SC. Part-to-part deviations become averaged over the SCs in a stack, but the value of C itself is dependent on voltage.

The voltage dependence of the capacitance is modelled in terms of the discharge ratio as $\tilde{C}(x) = C f(x)$. The voltage-dependent capacitance function, $f(\cdot)$, when available from the manufacturer or through characterization, is included in the expression for $U(x)$ in (3). The SODR is subsequently derived considering the modified $\tilde{C}(x)$ and $U(x)$.

The parameter variation of an SC due to aging is handled through the use of manufacturer-provided worst-case/end-of-life values in the design. The consideration of these worst-case quantities leads to pessimistic estimates of effective power and energy densities.

V. SIMULATION AND EXPERIMENTAL RESULTS

The preceding analysis and design are validated in circuit simulation and in experiments on a fabricated SC stack. The ratings of the load and the measured parameters of the SC stack are given in Tables I and II, respectively. For these ratings, the initial stack design step is evaluated for a number of commercial off-the-shelf SC parts, and the resulting distribution of stack volume and cost is presented in Fig. 3b. The SC part, BCAP0050 P300 X11, rated 50 F, 3 V, is selected.

TABLE III
COMPARISON OF NUMBER OF SCs REQUIRED FOR VARIOUS VALUES OF DISCHARGE RATIO

DR, x	Effective power density, Π (W per unit)	No. of SCs for 250 W	Effective energy density, U (J per unit)	No. of SCs for 250 J	No. of SCs, N , for 250 W, 250 J	N/N_{min}
0.25 [6]	6.75	38	211	2	38	9.5
0.50 [2]	27.0	10	169	2	10	2.5
0.82, SODR	72.6	4	73.7	4	4	1.0

TABLE IV
EXPERIMENTAL (EXP.) AND SIMULATED (SIM.) BACKUP TIMES AND PEAK SC CURRENT FOR THREE VALUES OF THE DR ALONG WITH CORRESPONDING ERRORS (ERR.) WITH RESPECT TO EXPERIMENT

Backup time (s)	Type	DR, x			Peak SC current			Comment
		Sim.	Exp.	% Err.	Sim. (A)	Exp. (A)	% Err.	
0.50	> SODR	0.91	0.90	1.1	8.3	8.4	1.2	Backup time insufficient
1.00	\approx SODR	0.79	0.79	0.0	10.4	10.3	1.0	-
1.25	< SODR	0.72	0.69	4.3	12.9	15.1	7.9	Power limit violated

For the selected off-the-shelf SC and the load ratings given in Table I, the number of SCs required is computed for various discharge ratios and presented in Table III. At lower values of discharge ratio, the number of SCs is constrained by the low effective power density. The optimal discharge ratio, with a minimal number (N_{min}) of SCs, is obtained when the effective power and energy densities are in the same proportion as the load power and energy requirements. The reduction in the number of SCs required is represented by the N/N_{min} ratios of the other designs.

The hardware prototype of the SC/PEI system is shown in Fig. 5. A stack of $40 \times$ BCAP0050 P300 SC cells is used to validate the proposed SODR. Since the stack size is fixed, the adequacy of the power and energy capability of the stack at various DRs is considered as an indicator of the sufficiency of size. The capacitance of the stack is measured to be 1.0 F, which is lower than the nominal value of 1.25 F. Thus, the SODR for the actual SC stack, given in Table II, is marginally lower than that given in Table III for a single SC cell.

Fig. 6 shows simulated and experimental waveforms of SC voltage (v_{sc}), SC current (i_{sc}), load voltage (v_{dc}), and load current (i_{dc}) for the proposed SODR as well as two non-optimal DRs. The pre-charged SC stack is discharged through the PEI at a constant load voltage. Corresponding simulated and experimental data is presented in Table IV. The load requirements are met by operating the SC stack at the SODR, while the other DRs either fail to satisfy the backup time or violate the power limit. Thus, DRs that are higher than the proposed SODR do not deliver sufficient energy, while DRs that are lower, lead to a lack of power capability. Thus, DRs that are different from the SODR necessitate a larger SC stack. This verifies the size-optimality of the SODR obtained for the given load requirements.

The simulated DRs are higher than that obtained in experiment, since an ideal PEI is assumed in simulation. This effect is significant at higher SC current and leads to larger errors at lower DRs. The worst-case errors in the peak current and the DR, with respect to experiment, are less than 8% and 4.5%, respectively.

VI. CONCLUSION

In this paper, a size-optimal discharge ratio (SODR) based on simultaneous considerations of power and energy is proposed to miniaturize SC stacks. Existing notions of backup durations suitable for various storage technologies are quantified based on this. A design method using the proposed SODR is detailed to optimize stack size for a given worst-case load requirement, and guidelines are described to refine the design. The analysis and design are validated through circuit simulation and in experiments on a 250 W laboratory prototype. The design employing the proposed SODR leads to a $\sim 60\%$ reduction in stack size requirement compared to a conventional design approach that does not optimize the DR.

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