A Multi-Port Partial Power Converter for PV based Smart Home Applications

Dissertation

zur Erlangung des akademischen Grades
Doktor der Ingenieurwissenschaften
(Dr.-Ing.)
Technische Fakultät
der Christian-Albrechts-Universität zu Kiel
vorgelegt von

M.Sc. *Yongdae Kwon*

Kiel
2025

Erklärung

Ich erkläre an Eides statt, dass ich die Dissertation zum Thema:

A Multi-Port Partial Power Converter for PV based Smart Home Applications

abgesehen von der Betreuung durch Herrn Prof. Marco Liserre selbstständig und ohne Hilfe angefertigt habe und bisher weder ganz noch zum Teil an einer anderen Stelle im Rahmen eines Prüfungsverfahrens vorgelegt, veröffentlicht oder zur Veröffentlichung eingereicht habe. Weiterhin versichere ich hiermit, dass ich die vorliegende Arbeit unter Einhaltung der Regeln guter wissenschaftlicher Praxis der Deutschen Forschungsgemeinschaft angefertigt habe und alle von anderen Autoren wörtlich übernommenen Stellen wie auch die sich an die Gedankengänge anderer Autoren eng anlehnenden Ausführungen meiner Arbeit besonders gekennzeichnet und die entsprechenden Quellen angegeben sind. Schlussendlich bestätige-ich, dass mir noch kein akademischer Grad entzogen wurde.

Kiel, den 15. 06 2024

Yongdae Kwon

1. Gutachter: Prof. Marco Liserre
2. Gutachter: Prof. Marcelo Heldwein
Datum der mündlichen Prüfung: 09.12.2024

Acknowledgments

This work was carried out during my work at the Chair of Power Electronics of Kiel University and after at Huawei Nuremberg Research Center, Germany. There are many people to whom I owe my thanks, and I would like to express my sincere gratitude to them in this acknowledgment.

First of all, I genuinely appreciate my academic supervisor Prof. Dr.-Ing Marco Liserre, who gave me the opportunity to join the research group and precious support during the journey of my doctoral periods. His guidance and advice significantly improved my quality to finish this work.

I would like to thank Dr. Francisco Freijedo and Mr. Miroljub Bakic for all their supports that helped me to be a better industrial researcher. Dr. Francisco supported me to establish the clear research direction and gave his best support to improve my academic writing skills. Mr. Miroljub Bakic fully supported me in improving the hardware designing skills.

I thank my colleagues in Chair of Power Electronics for the valuable discussions and advice for my works. Specially, Dr. -Ing. Junhyung Jung and Dr.-Ing. Sante Pugliese.

Last but not least, I would like to express my deepest love and heartfelt gratitude to my beloved wife, Seojin Kim. Throughout the long and often challenging journey of my doctoral studies, she has been my greatest source of strength. Her unwavering support, patience, and belief in me have been invaluable. Without her endless love and care, I would not have been able to complete this work. To my beloved Seojin, thank you from the bottom of my heart for believing in me, standing by my side throughout this PhD journey, and giving me the strength not to fall. I love you deeply.

Contents

English Summary

The world is undergoing a profound transformation with a remarkable increase in the use of renewable energy. This paradigm shift is not limited to large utility-scale projects but is extending into residential applications, electrifying living spaces. Furthermore, advancements in power electronic converters (PEC) play a key role in transforming energy management in home applications. Thanks to PECs, residences have the potential to evolve into intelligent ecosystems capable of optimizing energy consumption through advanced power management, also known as smart home system.

In recent years, the increasing penetration of the renewable energy sources (RES) and the residential-energy storage system (ESS) to the home allow supplying the power to the smart home directly through the RES or residential-ESS by DC-DC power conversion without connecting to AC grid. The utilization of RES and residential-ESS helps to reduce the consumption cost of the electricity, and helps to manage the power supply even during the black-out. In these reasons, DC-DC converter in the smart home architecture became one of the necessary component which makes possible to utilize the power of RESs and residential-ESS.

Conventionally, DC-DC converters have been used full power processing (FPP) architectures, which process the total power from the input. On the other hand, the exploration of partial power processing (PPP) architectures, which process only a portion of the power from the input, offers a way to further reduce costs and losses compared to FPP architectures. Therefore, use of PPP architectures in the smart home application gives higher possibility to achieve better integration, ultimately reducing costs and volume of the PECs.

In this study, a multi-port PPP converter architecture is developed and analyzed for the smart home application. The proposed architecture aims to improve the efficiency achieved by state of the art multi-port PPP technologies. Furthermore, it also aims to reduce the volume and cost of the converter by using partially rated power electronics devices compared to conventional FPP converters. In order to achieve the goals, the topologies should be carried out for the optimal selection. Furthermore, a detailed design guideline for the proposed PPC is provided. Therefore, the converter can be realized and applied to practical solutions. The relationship between the PPP capability of the proposed architecture and the losses are analyzed to validate the PPP on the efficiency improvement. Finally, the prototype of the proposed architecture concept is realized. The steady state operation and the power control capability of the proposed architecture are validated by the experiments. The efficiencies at different load conditions are also measured and the peak efficiency measurement result is provided.

German Summary

Die Welt befindet sich in einem tiefgreifenden Wandel, der durch einen bemerkenswerten Anstieg der Nutzung erneuerbarer Energien gekennzeichnet ist. Dieser Paradigmenwechsel beschränkt sich nicht nur auf große Versorgungsprojekte, sondern erstreckt sich auch auf Anwendungen im Wohnbereich und elektrifiziert Lebensräume. Darüber hinaus spielen Fortschritte bei Leistungselektronik-Wandlern (PEC) eine Schlüsselrolle bei der Transformation des Energiemanagements in Heimanwendungen. Dank PECs haben Wohngebäude das Potenzial, sich zu intelligenten Ökosystemen zu entwickeln, die durch fortschrittliches Energiemanagement, auch bekannt als Smart-Home-System, den Energieverbrauch optimieren können.

In den letzten Jahren ermöglicht die zunehmende Verbreitung erneuerbarer Energiequellen (RES) und Energiespeichersysteme (ESS) für Privathaushalte die direkte Stromversorgung von Smart Homes über RES oder ESS durch Gleichstromwandlung, ohne dass eine Verbindung zum Wechselstromnetz erforderlich ist. Die Nutzung von RES und ESS trägt zur Senkung der Stromkosten bei und hilft, die Stromversorgung auch während eines Stromausfalls aufrechtzuerhalten. Aus diesen Gründen wurde der DC-DC-Wandler in der Smart-Home-Architektur zu einer der notwendigen Komponenten, die die Nutzung der Energie aus RES und ESS ermöglicht

Herkömmlicherweise wurden in DC-DC-Wandlern Vollleistungs-Verarbeitungsarchitekturen (FPP) verwendet, die die gesamte Leistung vom Eingang verarbeiten. Andererseits bietet die Erforschung von Teilleistungs-Verarbeitungsarchitekturen (PPP), die nur einen Teil der Leistung vom Eingang verarbeiten, eine Möglichkeit, Kosten und Verluste im Vergleich zu FPP-Architekturen weiter zu reduzieren. Daher bietet die Verwendung von PPP-Architekturen in Smart-Home-Anwendungen eine höhere Wahrscheinlichkeit, eine bessere Integration zu erreichen, was letztlich zu einer Reduzierung der Kosten und des Volumens der PECs führt.

In dieser Studie wird eine neuartige Multi-Port-PPP-Konverterarchitektur für Smart-Home-Anwendungen entwickelt und analysiert. Die vorgeschlagene Architektur zielt darauf ab, die Effizienz der aktuellen Multi-Port-PPP-Technologien zu verbessern. Darüber hinaus soll durch den Einsatz von teilweise bewerteten passiven und aktiven Leistungselektronikbauteilen im Vergleich zu herkömmlichen FPP-Konvertern das Volumen und die Kosten des Konverters reduziert werden. Um diese Ziele zu erreichen, sollten die Topologien für eine optimale Auswahl durchgeführt werden. Darüber hinaus wird eine detaillierte Konstruktionsrichtlinie für den vorgeschlagenen PPC bereitgestellt. Daher kann der Konverter realisiert und in praktischen Lösungen angewendet werden. Die Beziehung zwischen der PPP-Fähigkeit der vorgeschlagenen Architektur und den Verlusten wird analysiert, um die PPP hinsichtlich der Effizienzsteigerung zu validieren. Schließlich wird der Prototyp des vorgeschlagenen Architekturkonzepts realisiert. Der stationäre Betrieb und die Leistungssteuerungsfähigkeit der vorgeschlagenen Architektur werden durch Experimente validiert. Die Wirkungsgrade bei verschiedenen Lastbedingungen werden ebenfalls gemessen und das Ergebnis der Spitzenwirkungsgradmessung wird angegeben.

Used symbols and abbreviations

General Symbols

x	instantaneous value
$\bar{X}$	Average value
$\tilde{x}$	Oscillation value
Δx	Differential value
X	RMS value
$X_{\mathbf{peak}}$	Peak value

Superscripts

$*$	Reference value
$'$	Value without control action

Subscripts

DCx	DC input related
bus	Inverter side DC bus related
p	Partial power related
grid	Grid related
α,β	Stationary reference frame values
d,q	Synchronous reference frame values
pcc	Point of common coupling
SRC	Series resonant converter related
DAB	Dual active bridge converter related
min	Minimum value
max	Maximum value
s	Partial voltage converter switching related
rate	Rated value

Special symbols

ΔV_{pp}	Voltage ripple (peak-to-peak)
ω	Radial representation of frequency output of synchronization block
ω_0	Radial representation of the fundamental frequency
θ	Phase output of synchronization block

θ_0	Initial phase of the fundamental frequency
L	Inverter filter inductance
C	Inverter filter capacitance
L_{grid}	Grid inductance
I	Inverter filter current
V_n	Inverter leg voltage
V_{grid}	Grid voltage
Y_{PLL}	PLL Admittance
Y_1	Inverter Admittance
Y_2	Self-Synchronization Admittance
Y_{grid}	Grid Admittance
I_{m}	Current reference amplitude
f_{BW}	Grid Synchronization bandwidth
f_{inv}	Inverter switching frequency
P_{LF}	Full power processing losses
P_{LP}	Partial power processing losses
P_{dir}	Direct power
C_{pi}	i^{th} partial capacitor of DPC
V_{pi}	Partial voltage on i^{th} partial capacitor of DPC
I_{pi}	Partial current through i^{th} partial capacitor of DPC
I_{dpc_i}	Current of i^{th} DPC
D_{i}	Duty cycle of i^{th} DPC
P_{dfi}	Differential power processed on i^{th} differential power converter
V_{aux}	Auxiliary DC source voltage
I_{frx}	Output current of $x^{th}\|_{x=1,\cdots,n}$ fractional power converter
I_{Ox}	Output current of $x^{th}\|_{x=1,\cdots,n}$ partial power converter
η	Efficiency
D_{x}	Duty cycle of x^{th} partial voltage converter
V_{mpp}	Maximum power point voltage of PV panel
V_{oc}	Open circuit voltage of PV panel
I_{mpp}	Maximum power point current of PV panel
P_{rate}	Rated power
I_{rate}	Rated current
V_{B}	Break down voltage
$I_{\mathrm{d}_{rate}}$	Rated drain current
$R_{\mathrm{DS}_{on}}$	On state resistance
Q_{g}	Gate charge
$I_{\mathrm{D}_{pulse}}$	Pulse current
di/dt	Commutation speed
Q_{rr}	Reverse recovery charge
t_{rr}	Reverse recovery time
i_{fx}	Filter current of x^{th} partial voltage converter
$S_{\mathrm{tx}}, S'_{\mathrm{tx}}, S_{\mathrm{bx}}, S'_{\mathrm{bx}}$	Switch sets of the PVC legs

i_{d}	Drain current of the switching device
P_{con}	Conduction losses of the semiconductor
P_{sw}	Switching losses of the semiconductor
V_{dr}	Gate driver output voltage
V_{dd}	Voltage applied to drain
V_{ds}	Drain-Source voltage
V_{gs}	Gate-Source voltage
R_{g}	Gate resistor
i_{g}	Gate current
C_{gs}	Gate-Sources capacitor
C_{gd}	Gate-Drain capacitor
C_{ds}	Drain-Sources capacitor
$V_{\mathrm{g(th)}}$	Gate threshold voltage
$V_{\mathrm{g(plt)}}$	Gate plateau voltage
t_{ru}	Switch voltage rising time
t_{fu}	Switch voltage falling time
t_{r}	Drain current rising time
t_{f}	Drain current falling time
P_{DCT}	Processed power on DC transformer
V_{pri}	Primary side voltage of DC transformer
V_{sec}	Secondary side voltage of DC transformer
i_{k}	DAB converter current
i_{k1}	First peak of DAB converter current
i_{k2}	Second peak of DAB converter current
L_{k}	DAB converter leakage inductance
N	Transformer turns ratio
ϕ	Phase shift angle of DAB converter
n	Number of DC input ports
G_{DAB}	Number of DC inputs
i_{rp}	Inverter side resonant current
L_{rp}	Inverter side resonant inductance
C_{rp}	Inverter side resonant capacitance
L_{mp}	Inverter side magnetizing inductance
i_{rs}	Partial voltage side resonant current
L_{rs}	Partial voltage side resonant inductance
C_{rs}	Partial voltage side resonant capacitance
L_{ms}	Partial voltage side magnetizing inductance
f_{r}	Resonant current
S_{rtx}, S_{rbx}	Switch sets of DBSRC legs
$V_{\mathrm{oo'}}$	Voltage between neutral points of DBSRC legs
V_{IN}	General representation of DC input voltage representation of DBSRC legs
C_{IN}	General representation of DC input capacitor of DBSRC legs
$C_{\mathrm{t_{IN}}}$, $C_{\mathrm{t_{IN}}}$	General representation of top-bottom split DC input capacitor of DBSRC legs

i_r	General representation of resonant current of DBSRC legs
L_r	General representation of resonant inductance of DBSRC legs
C_r	General representation of resonant capacitance of DBSRC legs
L_m	General representation of magnetizing inductance of DBSRC legs
i_m	General representation of magnetizing current of DBSRC legs
dV/dt	Transformer voltage step
C_tp	Top side partial capacitor
C_bp	Bottom side partial capacitor
Λ_L	Volume of inductor
K_L	Inductor volume coefficient
Λ_C	Volume of capacitor
K_C	Capacitor volume coefficient
P_core	Inductor core losses
K_core, α, β	Stein-Metz coefficient
B	Flux density
R_Lfx	Inductor winding resistance
σ	dielectric bulk conductivity
ε	Permittivity of dielectric
I_sat	Saturation current
l	Length
w	Width
h	Height
G_cc	Current control transfer function
G_HBx	PVC transfer function
T_i	Integral time
τ	LC time constant
$H_{\mathrm{I}_{fx}}$	Close loop transfer function of PVC
ζ	Damping constant
ω_c	Bandwidth
T_set	Settling time
N_1	Inverter side transformer turns
A_c	Core area
Λ_T	Transformer volume
Λ_co	Transformer core volume
l_c	Core length
P_V	Transformer core losses per unit volume
V_rp	First harmonic approximation voltage input
V_rs	First harmonic approximation voltage output
ϕ_o	Phase angle between v_{rp} and v_{rs}
R_e	Equivalent AC load of DHBSRC
G_SRC	Gain function of DHBSRC
X	Reactance
h	Inductor turns ratio

Q	Quality factor
ω_n	Normalized radial DHBSRC switching frequency
I_mp	Inverter side magnetizing current of DHBSRC
B_o	Optimal flux density
ρ_w	resistivity of copper
ΔT	Temperature rise
k_a, k_c, k_w	Dimensionless constant coefficient
k_u	winding window utilization factor
K_v	Voltage waveform factor
l_e	Effective length
A_e	Effective area
Λ_e	Effective volume
m	Mass of core
A_p	Area product
A_w	Wire area
J_o	Current density
P_ct	Transformer core losses
R_dcp	Inverter side DC resistance of transformer
R_dcs	Partial voltage side DC resistance of transformer
MLT_p	Mean length of turn on inverter side
MLT_s	Mean length of turn on partial voltage side
δ	Skin depth
R_acp	Inverter side AC resistance of transformer
R_acs	Partial voltage side AC resistance of transformer
r_w	Radius of wire
P_cu	Copper losses of the transformer
L_sfp	Inverter side self inductance
L_sfs	Partial voltage side self inductance
g_a	Airgap
R_mk	Transformer core reluctance
l_mk	Distance of core geometry (Fig. 4.20)
A_mk	Area of core geometry (Fig. 4.20)
A_gy	Area of airgap (Fig. 4.20)
R_me	Equivalent total reluctance of transformer
μ_0	vacuum permeability (=$4\pi 10e-7$ H/m)
b_1	Average width of inverter side turns
b_2	Average width of partial voltage side turns
b_g	gap between wires
h_i	height of the wires
ε_cc	Transformer coupling coefficient
K_pr	Partial power ratio
T_jm	Junction temperature
R_jcm	Junction to case thermal resistance

T_{cm}	Case temperature
R_{chm}	Case to heatsink thermal resistance
T_{h}	Heatsink temperature
R_{ha}	Heatsink to ambient losses
T_{a}	Ambient temperature
Λ_{hs}	Heatsink volume
W_{g}	Heatsink weight
Λ_{s}	Switch volume

Abbreviations

RES	Renewable Energy Sources
PEC	Power Electronic Converter
PV	Photo-Voltaic
EV	Electric Vehicle
ESS	Energy Storage System
LED	Light Emitting Diode
FPC	Full Power Converter
HFT	High Frequency Transformer
PPP	Partial Power Processing
PD	Power Density
PPC	Partial Power Converter
PWM	Phase Width Modulation
PI	Proportional-Integral
PLL	Phase Locked Loop
p.u.	per unit
FPP	Full Power Processing
VA	Volt-Ampere
DPC	Differential Power Converter
FRPC	Fractional Power Converter
KCL	Kirchhoff's Current Law
IPOS	Input Parallel-Output Series
ISOP	Input Series-Output Parallel
PVC	Partial Voltage Converter
DAB	Dual Active Bridge
SRC	Series Resonant Converter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
HB	Half-Bridge
ZVS	Zero voltage switching
DBSRC	Dual bridge series resonant converter

NPC	Neutral Point Clamped
DHBSRC	Dual half-bridge series resonant converter
FHA	First Harmonic Approximation
ESR	Equivalent series resistance
CSF	Component stress factor
UF	Utilization factor

1 Introduction

This chapter presents the motivations of the the novel partial power DC-DC converter architecture development. The targets of the development are to improve the efficiency and volume reduction compared to the conventional DC-DC converter architectures. After the motivation of work, a research proposal for the thesis is explained. Finally, the structure of the thesis is described. In addition, the related publications corresponding to each chapter are highlighted.

1.1 Motivation of novel multi-port partial power DC-DC converter architecture development

The modern world is witnessing a change in the living spaces. Smart homes have emerged as a solution that integrates intelligent control devices, residential-energy storage systems (ESSs), and various loads to enable a more efficient and sustainable lifestyle. The power electronics converter (PEC), as the power conversion interface of the smart home, is the key player in shaping the future of modern power grids.

DC power conversion has recently become one of the important requirement for smart homes due to the increasing penetration of DC sources and DC loads, such as solar photovoltaic (PV) systems, residential-energy storage systems (ESSs), DC heatpumps, and LED lights. Since different types and numbers of DC sources and DC loads are connected to DC-DC converters, which provide power conversion between renewable energy sources (RESs) and DC loads, a multi-port architecture is required for the DC-DC converter in smart homes.

The key challenges for multi-port DC-DC converters are to increase efficiency and reduce the size, weight and cost of the PEC interfaces. Achieving these goals will not only improve the performance of smart homes, but also contribute to the wider adoption of renewable energy and sustainable living. The PEC interfaces have traditionally used a full power processing (FPP) DC-DC converter architectures that process the full voltage and full current of the input sources. However, the recent researches show that the partial power processing (PPP) architectures can further reduce the aforementioned challenges of the conventional FPP architectures. The PPP architectures allow the DC-DC converters to process only a part of the power, hence reducing the losses on the PEC interfaces. In addition, the volume and costs of the active and passive components also can be reduced by utilizing lower power ratings in the DC-DC converters compared to FPP. Therefore, the use of PPP DC-DC converters can increase efficiency by reducing the power processing, and achieve volume and costs reduction by using the lower power rating devices respect to non-partial power processing DC-DC converters (or FPP).

The main focus of this thesis is to reduce the losses, volume, and costs of the conventional FPPs. In order to achieve the objective of the study, a novel multi-port partial power converter (PPC) architecture is proposed. The topology of the proposed architecture is optimally selected through the analytical investigation. The control of the proposed multi-port PPC is introduced and the parameter selection of the control is provided. The parameters of the hardware are also optimally designed based on the parameter design guide provided in the thesis. Finally, the proposed architecture is realized with the laboratory scale prototype. In addition, the operating principle and power processing concept of the proposed architecture is validated with the prototype..

1.2 Research proposal

This thesis aims to develop a novel DC-DC multi-port PPC architecture for the smart home application, which targets on enhancing the efficiency of the DC-DC converter stage and reduce the volume of the converter. The thesis focuses on the development of operation solutions in three different aspects:

Target I: A novel PPC architecture and its optimization respect to all the different stages

The first research target is to propose a novel PPC architecture and optimize its topology in order to find the best trade off between the losses and volume of the DC-DC converters. The operating point and the ratings of the proposed PPC will be specified based on the market analysis. Several DC-DC converter topologies are investigated for the multi-port PPC architecture. Since, the aim of the proposed multi-port PPC architecture is to achieve high efficiency, the most optimal topology for the proposed PPC should be selected by comparing the losses of all possible topology combinations.

Target II: Design and optimization of the control and power conversion parameters

The second research target is to provide guidance on the parameter determination for the novel PPC architecture. Firstly, the control method of the proposed architecture is provided to clarify the operating principle of the converter. The control parameters of the proposed architecture should be designed based on the model of the proposed multi-port PPC. The hardware parameters are also optimally selected to achieve the target current and voltage ripple by using optimal inductance and capacitance. Based on the designed parameters, the optimal commercial element selection method is discussed. Furthermore, the transformer of the proposed PPC is precisely designed to achieve the expected behavior as the theoretical model. The designed parameters, simulation results and actual parameter values are compared to prove the accuracy of the transformer design.

Target III: Validation of the proposed PPC architecture

The third research target is to validate the novel PPC architecture. The relationship between the processed power on the proposed multi-port PPC and the losses will be analyzed. Based on the loss analysis, the efficiency of the proposed PPC will be estimated. The total volume and weight will be measured to obtain the power density of the prototype. The operating concept of the proposed PPC will be validated by the experimental results with the lab scale prototype. Finally, the efficiency will be measured using the power analyzer and compared with the estimated efficiency.

1.3 Structure of the thesis

The structure of this thesis is shown in Fig. 1.1. An introduction to smart home applications and their structure is given in Chapter 2. An DC-AC power conversion interface between the AC grid and a DC grids in the smart home is one of the necessary function that required for a smart home architecture. Therefore, an inverter, which performs the DC-AC power conversion, is briefly explained to give a short introduction about its control method of each off-grid and grid-connected modes. Furthermore, two different grid synchronization methods for the grid connected modes are compared in order to analyze the effect of the grid synchronization block on the stability of the inverter control. As discussed earlier, a DC-DC power conversion stage is the main focus of the thesis that targets the efficiency and volume optimization. The DC-DC converter architectures are categorized according to their power processing characteristics. The conventional full power DC-DC converter architectures in the smart homes are described. The different state of the art DC-DC converter architectures and their power processing principles are also analyzed. The efficiencies of the most related articles are also compared to benchmark the peak efficiencies achieved by the state of the art technology.

Chapter 3 describes a proposed multi-port PPC architecture with the topology selection. Before going into the detailed topology selection, the target operating range and power ratings of the proposed architecture are decided based on the market research. The topology of the first stage, which is called the partial voltage converter stage, of the proposed architecture is selected by finding an optimal trade of point between losses and volume of it. In addition, the switching states and operating modes of different topology options for the PVCs are provided. The DC transformer is the other stage whose topology needs to be selected. The isolated converters with bidirectional power control capability are considered for the topology options. For the smart home applications, a wide load condition should be considered due to the different DC interfaces (PV, EV and home storage). Therefore, the isolated converter with wide load ZVS capability is considered for the DC transformer stage. Furthermore, after selecting the topology, the primary and secondary bridges of the DC transformer are also selected by finding an optimal trade off point between the losses and volume.

Chapter 4 presents the control scheme of the proposed multi-port PPC and its parameter design. The control and operating principle of the proposed architecture is given with the block diagram. The power conversion parameters of the PPC are selected to achieve the target current and voltage ripple. The commercial inductor and capacitor selection guide is also provided. The parameters of the DC transformer are also designed to achieve the target gain. Based on the selected parameters, the transformer is modeled and realized to obtain the close matching parameters between the theoretical design. The target parameters, the theoretical model and those of the realized transformer are compared to check the accuracy of the transformer model.

The analysis of the proposed PPC and the construction of the laboratory prototype hardware, including heatsink, is carried out in Chapter 5. The partial power processing has a significant impact on the losses of the converter. Therefore, the power processing characteristics of the proposed multi-port PPC are analyzed using the utilization factor and the partial power processing ratio, which are the indicators to show the amount of power processing. Then, the efficiency and losses of the multi-port PPC are analyzed to validate the relationship between the PPP characteristics of the proposed architecture. The lab scale prototype is built based on the selected parameters and the heatsink selection for the prototype is also performed. The volume and weight of the prototype are measured to verify the power density.

In Chapter 6, the concept and performance of the proposed multi-port PPC are validated by the experiments. Finally, the benchmark and proposed architectures are compared to highlight the improvements of the proposed solution.

Chapter 7 summarizes the results and provides the conclusions. The performance of the proposed multi-port PPC is concluded. Finally, an outlook on future work is given.

1.4 Assignment of publications to the chapters of this thesis

Journal papers

J1 Y. D. Kwon, F. Freijedo, T. Wijekoon, and M. Liserre, "Series Resonant Converter Based Full-Bridge DC-DC Partial Power Converter for Solar PV," *in IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 2, pp. 1719-1729, April 2024.

J2 Y. D. Kwon, F. Freijedo, T. Wijekoon, and M. Liserre, "A multi port partial power converter for smart home applications," *in IEEE Transactions on Power Electronics*, vol. 39, no. 7, pp. 8824-8833, July 2024.

Conference Proceedings

C1 Y. D. Kwon, R. Zhu, M. Liserre, B. McGrath, A. A. Nazib, D. G. Holmes, P. Mu, "Impedance-based Stability Assessment of Self-Synchronising Power Electronics Converter," *in 2020 International Power Electronics Motion Control Conference (IPEMC-2020-ECCE Asia)*, 2020, pp. 2116-2121.

C2 R. Zhu, Y.D. Kwon, M. Liserre, A. A. Nazib, D. G. Holmes, B. McGrath, "Phase Angle Compensation-based Highly Accurate Self-Synchronising Inverter," *in 2020 International Power Electronics Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 2088-2092.

C3 S.Pugliese, Y. D. Kwon, and M. Liserre, "Positive-Negative Sequence SRF-PLL Model for Accurate Stability Analysis in Grid-Tied Converters," *in 2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 3593-3600.

C4 Y. D. Kwon, F. Freijedo, T. Wijekoon, and M. Liserre, "Partial Power Processing DC/DC MPPT Converters in Solar PV Applications: Overview of Architectures," *in 2022 IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1-6.

C5 Y. D. Kwon, T. Wijekoon, F. Freijedo, and M. Liserre, "Bidirectional Multi-Port Partial Power Converter for Solar PV Applications," *in PCIM2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2023, pp. 1-7.

C6 Y. D. Kwon, F. Freijedo, J. Olschewski, T. Wijekoon, and M. Liserre, "Design and Optimization of CLLC Converter Enabling Highly-Efficient Partial Power Processing for Solar PV Applications," *in PCIM2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2023, pp. 1-8.

C7 Y. D. Kwon, F. Freijedo, T. Wijekoon, and M. Liserre, "Combined Partial Voltage and Current Power Processing DC/DC Converters for Solar PV applications," *in 2023 International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, 2023, pp. 492-497.

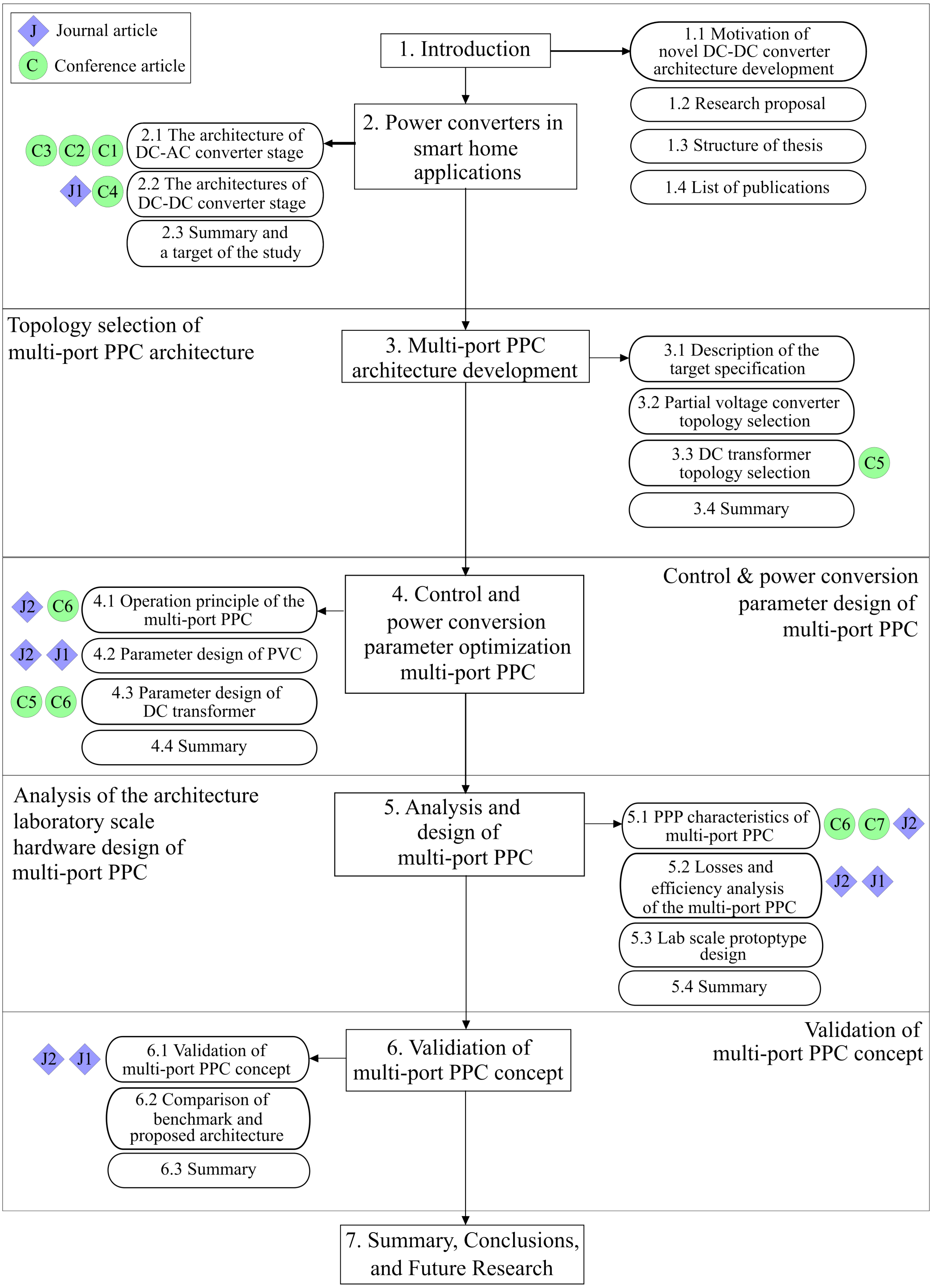


Figure 1.1: Structure of the thesis and related publications.

2 Power converters in the smart home application

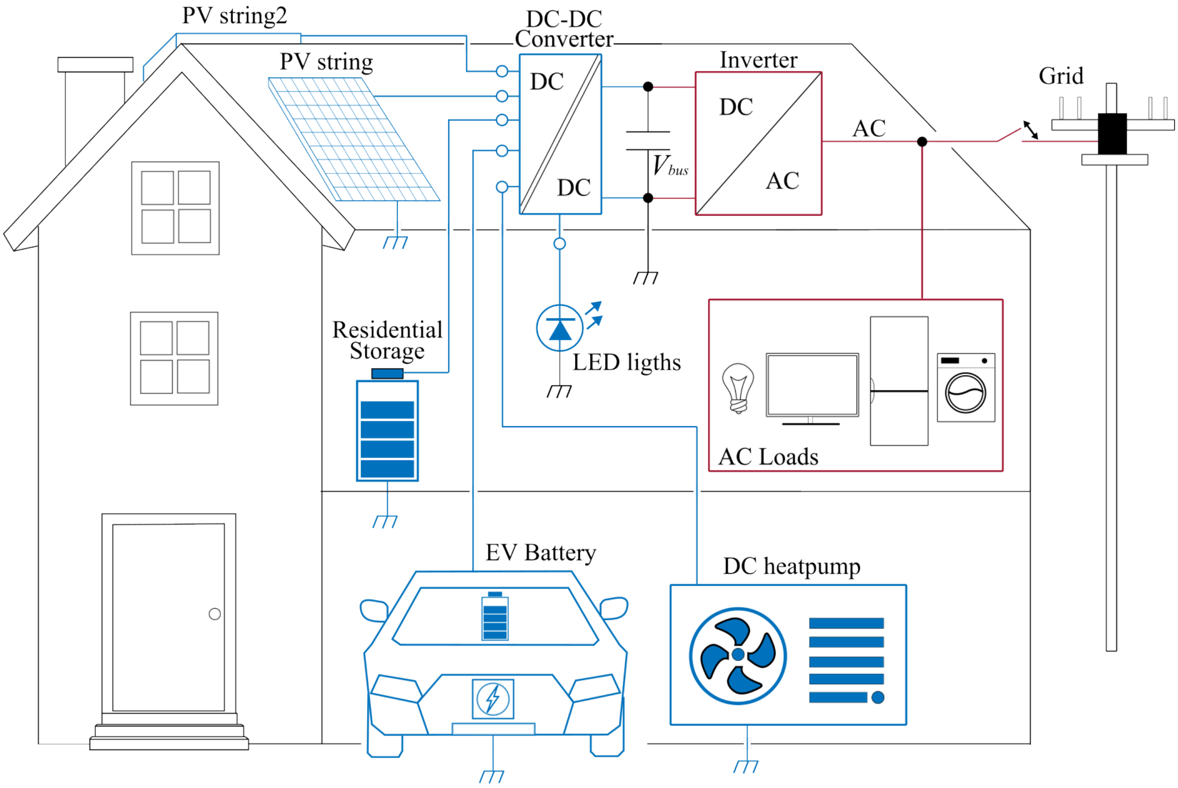


Figure 2.1: Smart home applications and architecture.

The demand for clean and sustainable electrical energy has grown rapidly in recent years, with renewable energy powered smart home technologies becoming mainstream and cost-effective for self-sufficient domestic needs [1,2]. To transfer power between various sources and loads connected to the smart home, power electronic converters (PECs) are the core technology for such smart home technologies [3]. As shown in Fig. 2.1, the smart home architecture has two power conversion stages: i) the DC-AC power conversion stage to supply the power to the loads and the grid connection, and ii) the DC-DC power conversion stage, which has the multi-port DC inputs to connect the DC loads and DC sources.

The inverter, which is the PEC for the DC-AC power conversion, can operate in two modes. If there is no grid connection, the inverter supports the power supply to the AC loads. In this mode, the power for the home appliances can be supported by the energy from renewable energy sources (RESs). On the other hand, if there is more power available than the AC loads require, the inverter can feed the power directly into the grid. In addition, if there is no power generation from the RESs, the inverter should control the DC bus voltage to supply the power to the DC loads through the grid connection.

On the DC side of the smart home, there are devices such as renewable energy sources, energy storage devices such as batteries and electric vehicles (EVs), and different types of loads such as DC pumps or LED lighting. In a given smart home layout, multiple modes of energy exchange between renewable sources, storage elements and loads can coexist [4]. For example, during a day, photovoltaic (PV) panels can directly power household appliances, and any excess energy can be used to charge the residential-ESSs or electric vehicles (EVs). In the absence of solar, the residential-ESSs can support the necessary loads in the home appliances to increase self-consumption, while also providing a backup source in the event of a grid blackout [5–7]. The multiple DC sources and DC loads can be considered as a DC micro-grid connected to the common DC bus on the inverter side [8–10].

To handle the power from multiple DC sources and to DC loads, a multi-port converter architecture is required [11–15]. The multi-port converter architectures can be categorized according to their power processing characteristics: full power processing converters and partial power processing converters. The detailed categorization of the multi-port DC-DC converter architecture that has been studied recently should be reviewed and compared.

This chapter provides a brief introduction to the DC-AC power conversion strategy in grid forming mode and grid following mode. In addition, the effect of the grid synchronization methods, which is one of the key technologies for the grid following mode, on the control stability is presented. Next, the multi-port DC-DC converter architectures are categorized according to their power processing characteristics. The power processing of each architecture is visualized using a volt-ampere (VA) area model. A review of the state of the art multi-port architectures are compared by the table. Finally, the benchmarks and targets of the study is specified based on the comparisons of the state of art multi-port architectures.

2.1 DC-AC converter stage control

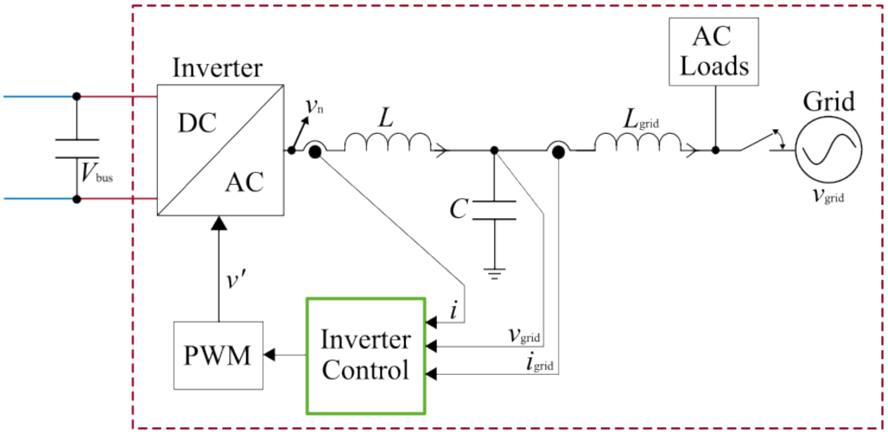


Figure 2.2: inverter configuration for smart home and its control block diagram.

DC-AC power conversion is required to drive the AC loads and to make the connection to the grid. A general smart home inverter configuration and its control block diagram is shown in Fig. 2.2. The inverter can be connected either to AC loads or to the grid. Depending on its connection, the inverter can be operated in two modes: grid forming mode and grid following mode.

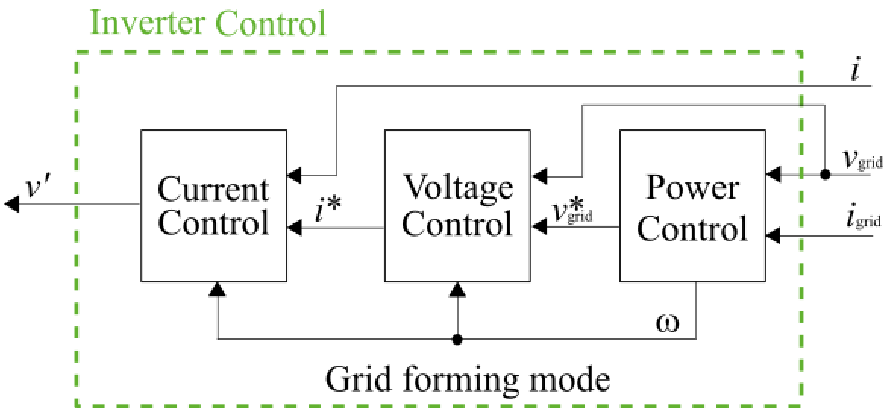


Figure 2.3: Control block diagram of grid forming mode.

2.1.1 Grid forming mode

If the smart home provides the power to the AC loads without being connected to the grid, the inverter should be operated in grid forming mode, where the inverter forms the grid to drive the AC loads [16–18]. As shown in the block diagram in Fig. 2.3, the grid forming mode consists of three loops [19–21]. The first loop is the external power control loop, which derives the voltage amplitude and frequency information for the voltage control [22–25]. This can be done by following the droop characteristics of the active and reactive power. The second loop is for the voltage control of the grid voltage and its frequency, which controls the grid voltage and its frequency [26–28]. The third loop is the current loop, which controls the current by following the frequency and phase of the grid voltage. Finally, the inverter can form the grid with the optimum voltage derived from the grid forming mode control.

2.1.2 Grid following mode

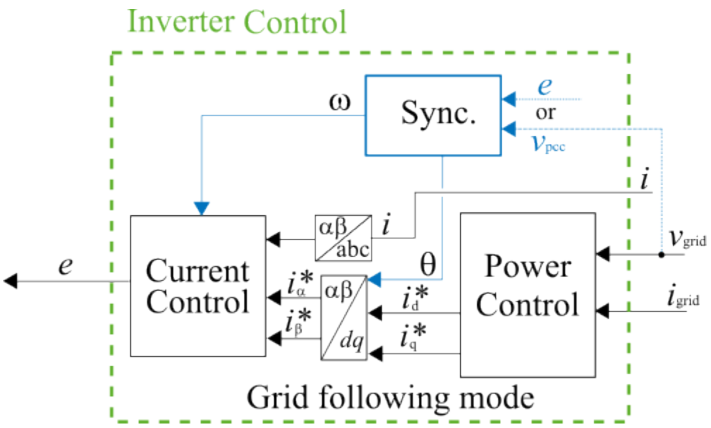


Figure 2.4: Control block diagram of grid following mode.

If the RESs generates more power than the AC load demands, the inverter can connect to the grid and the redundant power from RESs can be supplied to the grid [29–32]. The grid following mode control block is shown in Fig. 2.4. The external power control loop provides the dq current references on the synchronous axis. The dq axis current is converted to the

$\alpha\beta$ current and applied to the current control. In grid following mode, the inverter should be able to track the grid angle and magnitude to inject or absorb the active and reactive power to the grid in order to comply with the grid codes. A grid synchronization technique is required to meet the grid code requirements and also to synchronize with the frequency and phase of the grid. One method of the grid synchronization is using a phase locked loop (PLL) by directly measuring the grid voltage (v_{pcc}). Another method is using a self-synchronization by obtaining the grid voltage information (e) indirectly from the internal current control.

Grid synchronization methods

The synchronization block can provide the frequency and phase angle information for the current control. There are two ways of synchronization with the grids. The first is to measure the grid voltage directly and to calculate the frequency and phase information using the phase locked loop (PLL) [33–36]. The second method is to use the indirect phase information from the control and calculate the phase information. This method is called self-synchronization method [37–39].

A. Phased locked loop

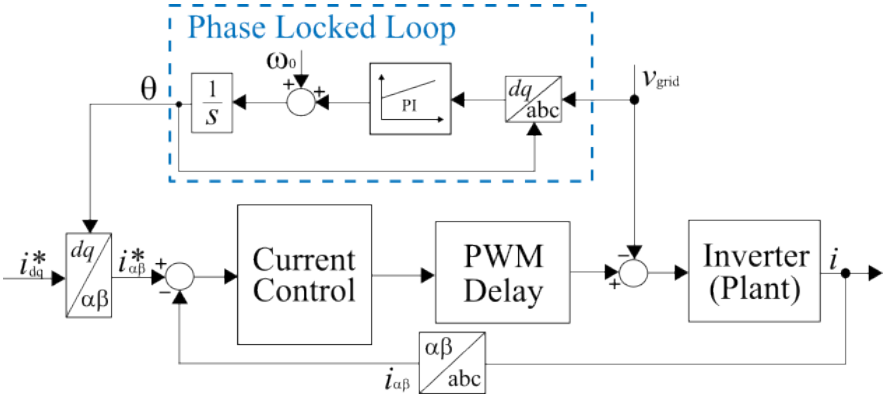


Figure 2.5: Control block diagram of phase locked loop (PLL).

The control block of the PLL is shown in Fig. 2.5. The PLL tracks the phase angle of the grid by the measured grid voltage. The block diagram shows that the direct grid voltage measurement creates a closed loop between the grid voltage (v_{grid}) and the input reference currents (i^*_{dq}). This loop has an effect not only on the stability of the current control, but also on the stability of the inverter. This means that the PLL based on measuring the grid voltage can degrade the stability of the inverters because the PLL provides an additional path for the harmonics to propagate through the control loop of the inverters [40, 41].

B. Self-Synchronization

The self-synchronization is an alternative synchronization method for grid connected inverters which control block is depicted in the Fig. 2.6. In the self synchronizing inverters, the grid voltage measurement is no longer required. The phase information of the grid is obtained by using the internal signals from the current control of the inverters. Let the vector

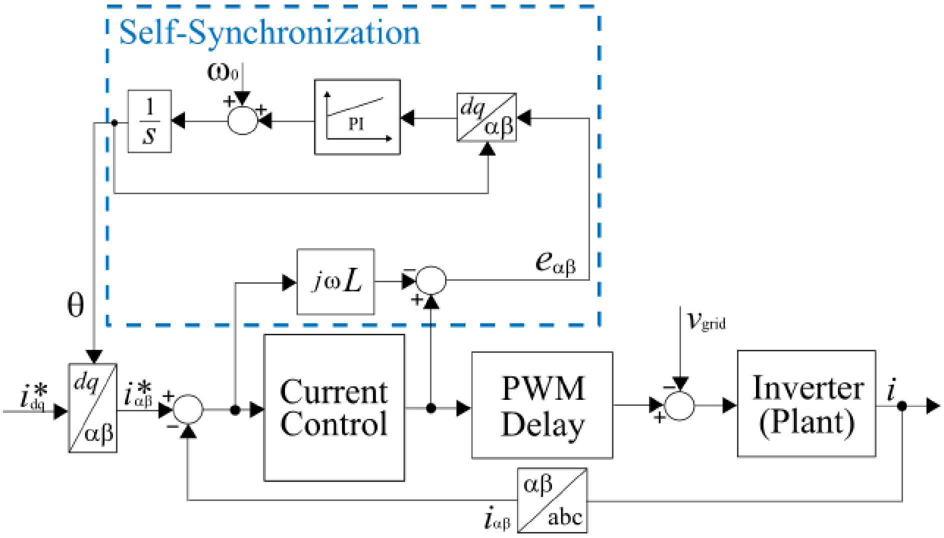


Figure 2.6: Control block diagram of self synchronization.

$\vec{Z} = Ze^{j\omega_0 t}$, then the relationships of the voltages on the stationary frame in Fig. 2.2 can be written as follows:

$$\vec{v_{\mathrm{n}}} = L\frac{d\vec{i}}{dt} + \vec{v}_{\mathrm{grid}} = j\omega_0 L\vec{i} \tag{2.1}$$

where L is the filter inductance of the inverter, $\vec{v_{\mathrm{n}}}$ (c.f. Fig. 2.2), $\vec{v_{\mathrm{grid}}}$, $\vec{i}$ are the vectors of the inverter leg voltage, the grid voltage, and the inverter filter current respectively.

In order to control the stationary frame currents ($i_{\alpha\beta}$), the resonant control should be employed for the inverter. The $\vec{v_{\mathrm{n}}}$ of the resonant control applied system can be obtained as:

$$\vec{v_{\mathrm{n}}}(s) = \left(k_{\mathrm{p}} + \frac{k_{\mathrm{r}}s}{s^2+\omega_0^2}\right)(\vec{i}^{*}_{\alpha\beta} - \vec{i}_{\alpha\beta}) \approx \frac{k_{\mathrm{r}}s}{s^2+\omega_0^2}(\vec{i}^{*}_{\alpha\beta} - \vec{i}_{\alpha\beta}) \tag{2.2}$$

where k_{p} and k_{r} are the proportional and resonant gains, ω is the resonant frequency, $i^{*}_{\alpha\beta}$ is the reference stationary frame currents.

Put (2.2) in (2.1), v_{grid} can be derived as follows:

$$\vec{v}_{\mathrm{grid}}(s) \approx e_{\alpha\beta} = \frac{k_r s}{s^2+\omega_0^2}(\vec{i}^{*}_{\alpha\beta} - \vec{i}_{\alpha\beta}) - j\omega_0 L_f \vec{i} \tag{2.3}$$

(2.3) shows that the grid voltage information can be indirectly derived from the resonant controller in the self-synchronization applied inverters instead of direct measurement of ac grid voltages by voltage sensors as the PLL applied inverters. Therefore, unlike the control loops of the PLL applied inverters, self-synchronization does not have closed loop from grid voltage to current reference. This means that the synchronization does not affect the system stability.

Impedance based stability analysis

Since the impedance of the inverter is influenced by the synchronization unit, the impedance-based stability approach is used. An impedance-based stability criterion is the stability analysis method which based on the ratio of input to output impedance and the phase difference between two connected systems. The analysis can characterize the frequency response of the inverter output impedance and intuitively show the impacts caused by the synchronization unit [42]. Therefore, the stability of the synchronization methods can be systematically studied taking into account the bandwidth variation of the grid synchronization, the variation of inverter impedance, and the operating point.

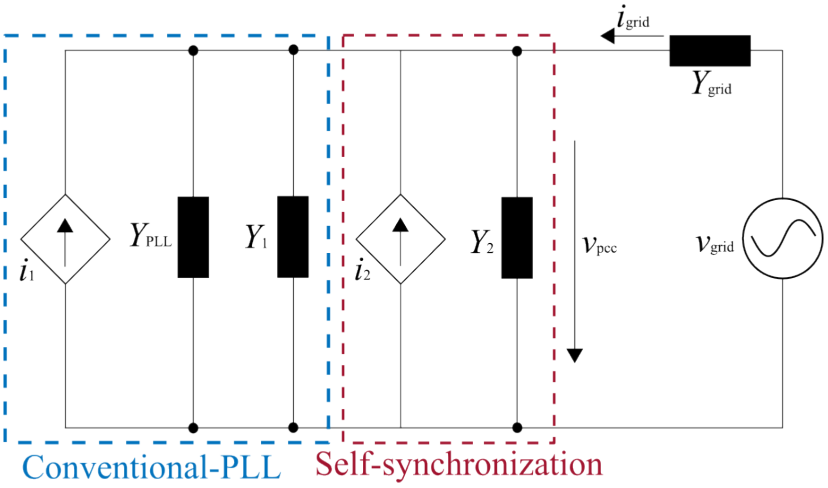


Figure 2.7: Interaction caused by grid impedance and inverter impedance.

The impedance-based model of the conventional PLL based inverter and the self-synchronizing inverter are compared in Fig. 2.7. In the figure, Y_1 is the admittance from v_{grid} to i without considering the PLL unit, and Y_{PLL} is the impedance that only caused by the PLL (the loop from v_{grid} to PLL and then to i, as shown in Fig. 2.5) in the conventional PLL based inverter. Y_1 and Y_{PLL} are denoted as the inverter admittance and PLL admittance respectively. Y_2 is the output admittance of the self-synchronizing inverter. Y_{grid} is the grid admittance. As discussed earlier, the total output impedance of the conventional PLL based inverter is equal to parallel admittance of Y_1 and Y_{PLL}. Based on Fig. 2.7, the interaction caused by impedance can be expressed as:

$$v_{\text{pcc}}(s) = (i_{\text{grid}} - i_1 - i_2)(Y_1 + Y_2 + Y_{\text{PLL}} + Y_{\text{grid}}) + \frac{Y_{\text{grid}}}{Y_1 + Y_2 + Y_{\text{PLL}} + Y_{\text{grid}}} v_{\text{grid}} \tag{2.4}$$

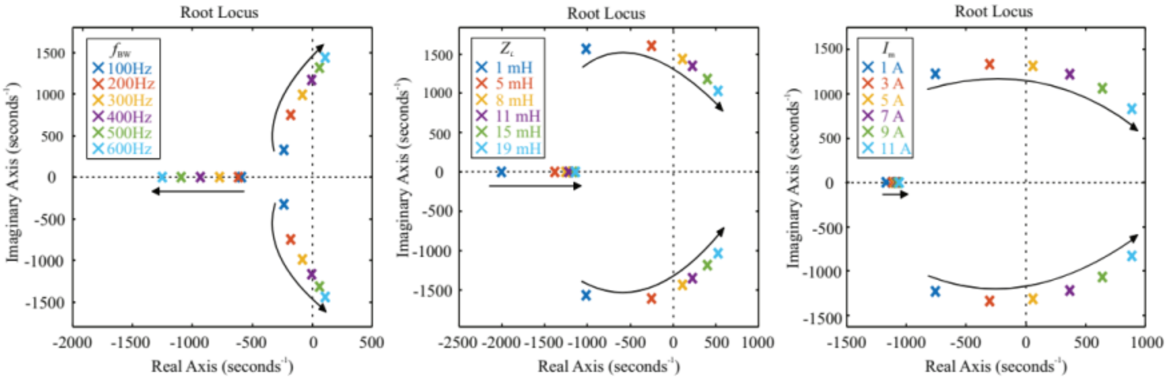
The equation shows that the interaction between the inverter and grid can be caused by the impedance.

The total admittance of the conventional PLL and the self-synchronizing inverter can be obtained as follows:

$$\begin{aligned} Y_{\text{tot}_{PLL}} &= Y_1 + Y_{\text{PLL}} \\ Y_{\text{tot}_{self}} &= Y_2 \end{aligned} \tag{2.5}$$

As explained earlier, the admittance of the PLL which is Y_{PLL} is derived from the loop between v_{g} and θ. Hence, based on (2.3), the parameter of the grid side filter inductance can impact on the stability of conventional PLL based inverter. On the other hand, stability of the self-synchronizing inverter does not have the loop between the grid synchronization. Hence the stability is only determined by the admittance of inverter Y_2.

A root locus can be plotted based on the admittance model in order to analyze the stability of the conventional PLL and the self-synchronization inverters. The root locus of the PLL based is shown in Fig. 2.8. Fig. 2.8 (a) shows that the impact of the PLL bandwidth on the behavior of roots of the conventional PLL based inverter when filter inductance $L = 8$ mH and the current amplitude $I_{\text{m}} = 5$ A. The system poles move to the right half plane and cross the imaginary axis by increasing the PLL bandwidth f_{BW}, from 100 Hz to 600 Hz. As a result, the PLL bandwidth is limited by the system stability concern. In Fig. 2.8 (b), the impact of L variation on the roots of the conventional PLL based inverter is plotted. To see the impact of L change, the PLL bandwidth $f_{\text{BW}} = 600$ Hz and the amplitude of the current reference $I_m = 5$ A. The system poles move to the right half plane as well by increasing L from 1 mH to 19 mH. This diagram indicates that the parameter of L can impact on the stability of the conventional PLL based PECs. Fig. 2.8 (c) shows the impacts of current reference in the conventional PLL-based PECs, when the PLL bandwidth $f_{\text{BW}} = 600$ Hz, the filter inductance $L = 8$ mH. The I_{m} is increased from 1 A to 11 A and it is shown that the I_m makes the system unstable. The analysis shows that the grid voltage measurement PLL on the system stability of inverters. The results show that a high bandwidth of the PLL and a high amplitude of the injected current will both challenge the stability of grid-connected inverters. Therefore, in order to ensure stability of the conventional PLL-based inverter, all of these three constraints of f_{BW}, L, and I_{m} must be considered for the system stability.



(a) (b) (c)

Figure 2.8: Root Locus of the conventional PLL based system under (a) PLL bandwidth variation ($L = 8$ mH and $I_m = 5$ A), (b) filter inductance variation ($f_{\text{BW}} = 600$ Hz and $I_{\text{m}} = 5$ A), and (c) current reference variation ($f_{\text{BW}} = 600$ Hz and $L = 8$ mH).

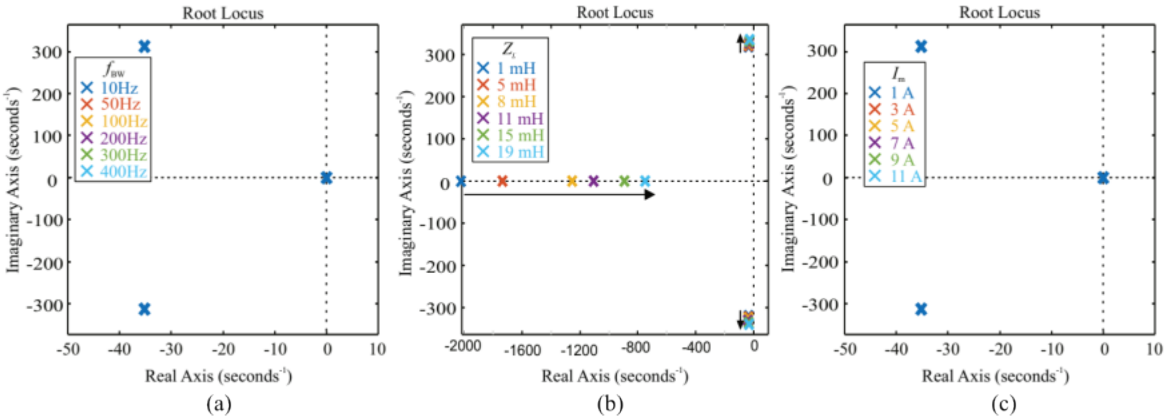


Figure 2.9: Root Locus of the self-synchronization system under (a) PLL bandwidth variation ($L = 8$ mH and $I_\mathrm{m} = 5$ A), (b) filter inductance variation ($f_\mathrm{BW} = 600$ Hz and $I_\mathrm{m} = 5$ A), and (c) current reference variation ($f_\mathrm{BW} = 600$ Hz and $L = 8$ mH).

In contrast, the impacts of these three constraints on the stability of the self-synchronizing inverters are shown in Fig. 2.9. Fig. 2.9 (a) shows f_BW of the self-synchronizing inverter does not change the roots of the inverter. This validates that the self-synchronization does not impact on the inverter impedance. In Fig. 2.9 (b) shows that the impact of L variation on roots of the self-synchronizing inverter. The change of roots are also smaller as compared to the conventional PLL based inverter that shown in Fig. 2.8 (b). Finally, I_m neither affect to the output impedance of self-synchronization inverter, as shown in Fig. 2.9 (c). The Fig. 2.8 and Fig. 2.9 validates that the self-synchronizing inverters are more robust and stable than the conventional PLL-based inverters.

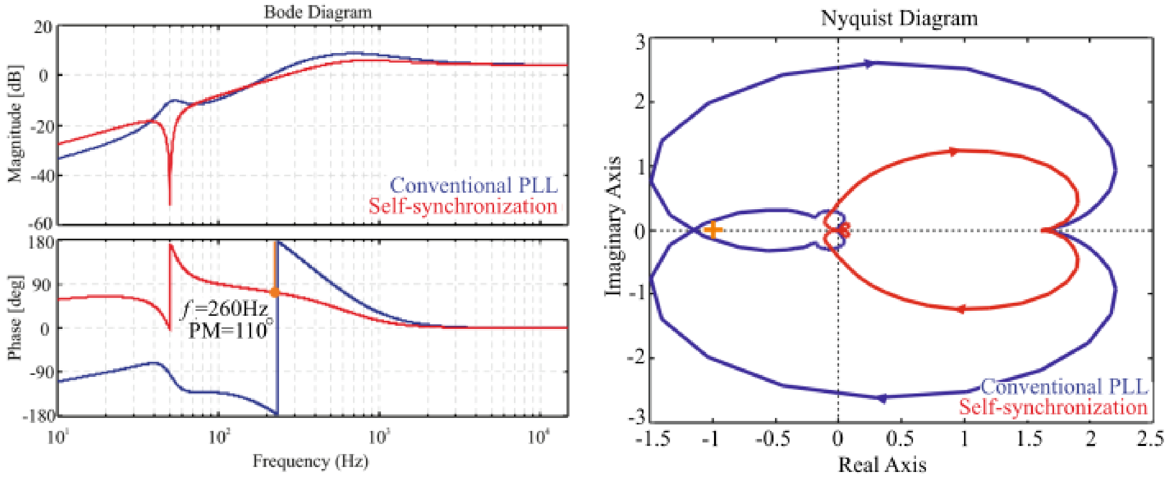
In order to evaluate the impact of synchronization units bandwidth on the inverters, the impedance based stability analysis is used, based on the admittance model as shown in Fig. 2.7. Fig. 2.7 (a) shows the bode diagram of the conventional PLL and self-synchronizing inverter. The figure shows that the conventional PLL based inverters does not have any phase margin. Hence, the PLL based inverter can be unstable when $f_\mathrm{BW} = 600$ Hz, $L = 8$ mH and $I_\mathrm{m} = 8$ A. On the other hand, the self-synchronizing inverter has enough stable margin.

The Nyquist diagram also presents the clear results as shown in Fig. 2.10 (b). The conventional PLL-based inverters are unstable while it encircle the critical point (-1,0). On the other hand, the self-synchronizing inverters do not encircle the critical point. All of the aforementioned analysis validate that the self-synchronizing inverters is more stable and robust against the f_BW, L, and I_m changes.

Simulation and experimental results

The simulation and experiments are carried out in order to validate the theoretical analysis with a 4 kW inverter. The electrical and control parameters of the system are organized in Table. 2.1.

The simulation results of three phase grid currents and voltages of PLL based and self-synchronizing based inverters are shown in Fig. 2.11 (a) and Fig. 2.11 (b), respectively. Fig.



(a) (b)

Figure 2.10: (a) Bode diagram of impedance based model and (b) Nyquist diagram of impedance based model.

Table 2.1: Simulations and experimental parameters

Parameters	Symbol	Value	Unit
Grid voltage amplitude	V_{grid}	50	V
Grid frequency	f_{grid}	50	Hz
Grid inductance	L_{grid}	5.6	mH
Rated power	P_{rated}	4	kW
Switching frequency	f_{inv}	10	kHz
Filter inductance	L	8	mH
Filter capacitance	C	5	μF
PLL Bandwidth	f_{BW}	600	Hz
Proportional gain of current	k_{p}	15	-
Resonant gain of current	k_{r}	1550	-

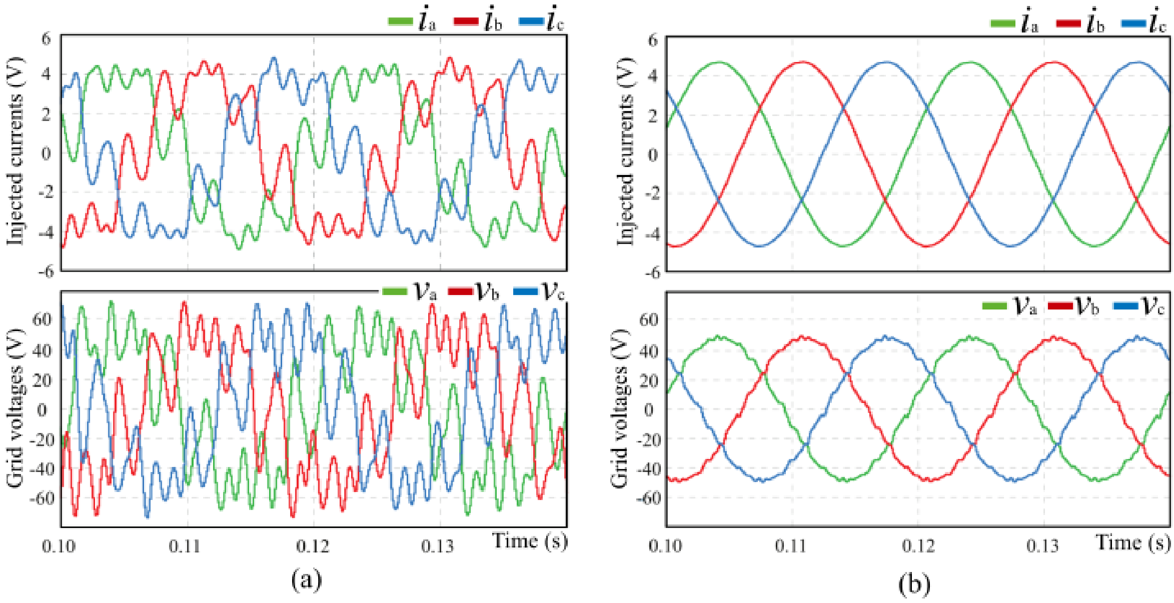


Figure 2.11: Simulation results of injected currents and grid voltages: (a) conventional PLL based inverter and (b) self-synchronizing inverter (parameters in Table. 2.1).

2.11 (a) shows that the three phase currents and grid voltages are seriously distorted because of the combination on the high f_{BW} and Z_{L}. In contrast, three phase current and the grid voltages are stable with the self-synchronization as shown in Fig. 2.11 (b). Therefore, the simulation results in Fig. Fig. 2.11 (a) and Fig. 2.11 (b) show that the theoretical analysis are valid.

The experimental results in Fig. 2.12 (a) show the injected current and grid voltage of the inverter with the conventional PLL when $f_{\mathrm{BW}} = 600$ Hz. The experimental results show that the injected grid currents and voltages are distorted at high f_{BW}. The stability of PLL can be degraded by the PLL impedance as the analysis in Fig. 2.8. In the experiment parasitic parameters of ac filter, converter and isolated transformer are existed, hence the amplitude of resonance in the injected currents is slightly different from the simulation results in Fig. 2.11 (a).

The three phase currents and grid voltages of the self-synchronizing inverter are measured as shown in Fig. 2.12 (b) which experiment has been conducted under the same condition as in Fig. 2.12 (a). As discussed before in the impedance based stability analysis, f_{BW} change of the self-synchronization does not impact on the stability of PEC. The self-synchronizing inverter shows less distortion with higher current and voltage quality, in contrast to the conventional PLL based inverter even with the $f_{\mathrm{BW}} = 600$ Hz. The experimental results also proves that the stability of self-synchronizing inverter is not affected by the f_{BW}, as the analysis results in Fig. 2.9 shows. Therefore, from the experimental results, it can be concluded that the self-synchronizing inverters have advantage in terms of the stability compared to the conventional PLL based inverters.

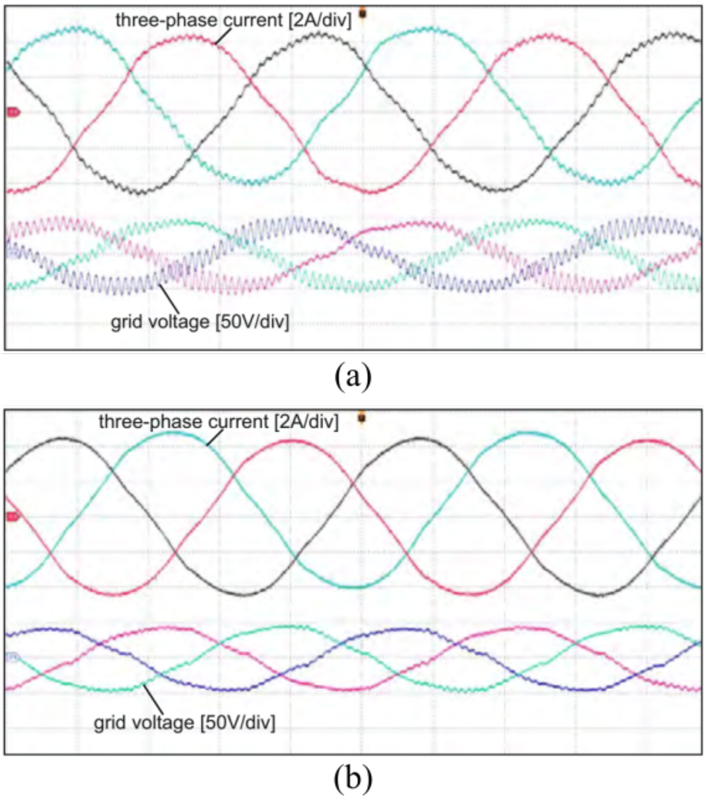


Figure 2.12: Experimental results comparison of (a) the conventional PLL based inverter, and (b) self-synchronizing inverter.

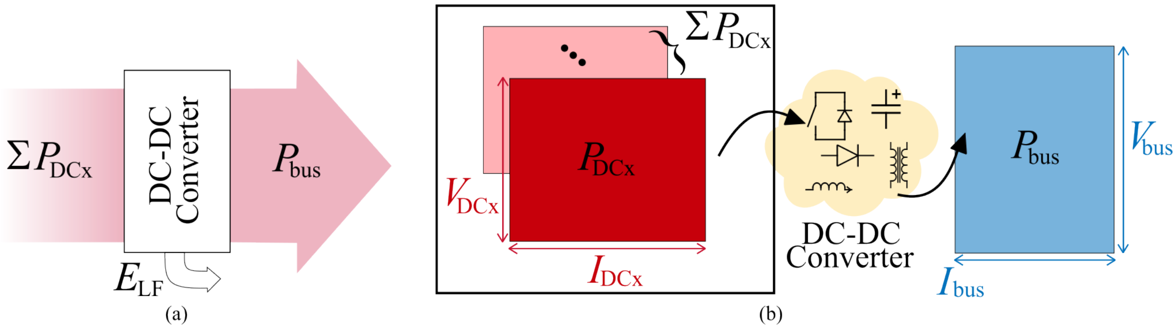
2.2 The architectures of DC-DC converter stage

The DC-DC converter stage of the smart home application is highlighted in Fig. 2.1 with the blue color. The DC bus voltage on the inverter side is higher than the DC input voltages. Therefore, a boost type DC-DC converter is used for the smart home applications [43–45]. Multiple sources and DC loads are connected to the input side of the multi-port DC-DC converter. The DC-DC converter has the capability to process the power between the DC sources and loads. The output side of the DC-DC converter is connected to the DC bus of the inverter. The architecture of the DC-DC converter can be categorized according to its power processing characteristics.

2.2.1 Full power processing DC-DC converter architecture

A full power processing (FPP) architecture is one of the most common power processing architectures in the industry. The power processing characteristics of FPP can be described by a power flow diagram and the volt-ampere (VA) area model are shown in Fig. 2.13.

The power flow diagram in Fig. 2.13 (a) shows the power processing of the DC-DC converters in the FPP architecture. Following the energy conservation principle, the relationship between the input and output power can be expressed as $\Sigma P_{\mathrm{DCx}} = P_{\mathrm{bus}}$, the relationship can be reorganized as:



(a) (b)

Figure 2.13: Power processing nature of full power processing (FPP) architectures: (a) power flow diagram and (b) VA area model.

$$\Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}} = V_{\mathrm{bus}} I_{\mathrm{bus}} \tag{2.6}$$

The equation shows that the total power of the DC input (ΣP_{DCx}) is processed by the DC-DC converters and delivered to the output. Therefore, in order to build the DC-DC converter that processes ΣP_{DCx}, the full voltage and full current rated semiconductor devices that have the same level as the system power are required. The DC-DC converter for the FPP is called a full power converter (FPC). The losses of the FPCs are caused by the power dissipation of the power electronics components. As shown in the figure, the losses (P_{LF}) of FPCs are caused by the DC-DC converters processing ΣP_{DCx}.

The first multi-port FPP architecture option is to use n-number of FPCs for each port, as shown in Fig. 2.14. The architecture shows that the multiple individual FPCs are connected to each DC input (V_{DCx}). Therefore, the FPCs control the voltage and current for each connected renewable energy source and DC load. The output of each FPC is connected to the common DC bus on the inverter side. The architecture can use the different FPC topologies that are suitable for each DC input port requirements for the smart home applications [46]. Therefore, each converter function is limited by the designated DC inputs to which the converter is connected.

The second possible multi-port FPP architecture is to use multi-winding transformer, as depicted in Fig. 2.15. As shown in the figure, a multi-winding high frequency transformer (HFT) is used between the AC-DC and DC-AC converters on V_{bus} and V_{DCx} respectively. The DC-DC converter topology that using HFT can be used to build the multi-port FPC, which is either a resonant converter or an active bridge converter topology. The power from the DC inputs can be converted from V_{bus} to V_{DCx} or from V_{DCx} to V_{DCx}. For example, (i) the power generated by the PVs can be fed into the V_{bus} or (ii) the the EV battery or the residential-ESSs can be charged by the power from the PVs. The advantage of the multi-winding transformer based FPC architecture is that it provides a high modularity by using the same cell for each DC input. Although, the power can flow into two different directions, the multi-winding transformers are not widely used in the industrial applications due to their design complexity.

In order to build the multi-port FPP architecture, the ratings of the DC-AC converter at the

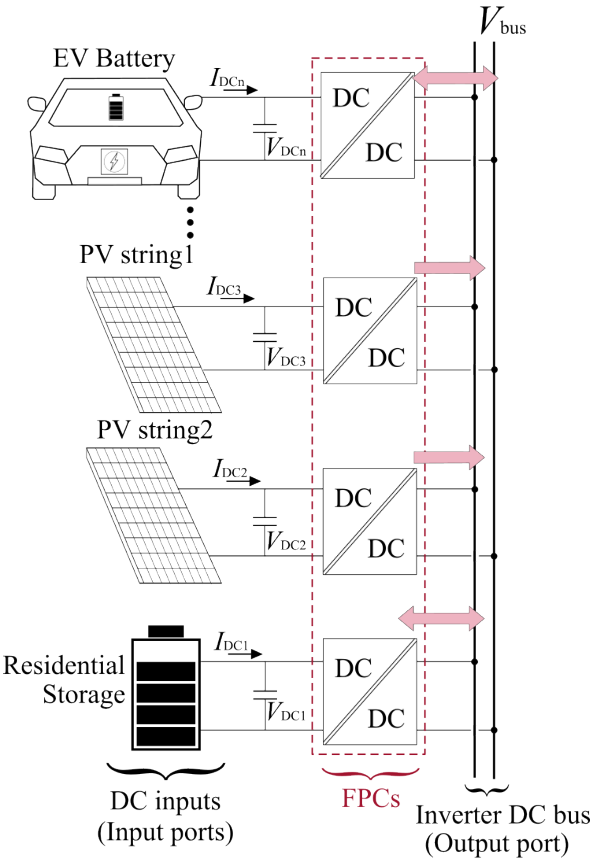


Figure 2.14: Multi-port FPP architecture using multiple FPCs.

output port should be designed to process the total power from the input demand. Therefore, the capacity of the DC-AC converter on the output port should be designed with a higher ratings than the input port. However, recent studies figured out that the converter can process a part of the power from the input by using a partial power processing (PPP) architectures.

2.2.2 Partial power processing DC-DC converter architectures

The PPP architectures have been introduced to reduce the voltage or current ratings of semiconductor and passive devices [47–49]. The key difference of PPP between FPP is depicted in Fig. 2.16 by the power flow diagram.

The power flow diagram in Fig. 2.16 shows that the DC-DC converters in the PPP architecture process only the target partial power (P_{p}). In the figure, the DC-DC converter processes P_{p} which is a part of P_{DCx}. The rest of the power P_{dir} is called a direct power (P_{dir}) which is not processed by the DC-DC converter, and bypasses directly to V_{bus}. The power flow diagram shows that the DC-DC converter does not process full DC input power but the partial power, hence the architecture is called PPP. By using the PPP architecture, the lower power processing feature can provide the potential to build high efficiency, and high power density (PD) converters. Compared to FPP, the processed power on the DC-DC converter can be reduced due to processing partial power, which eventually can lead to a reduction in losses (P_{LP}).

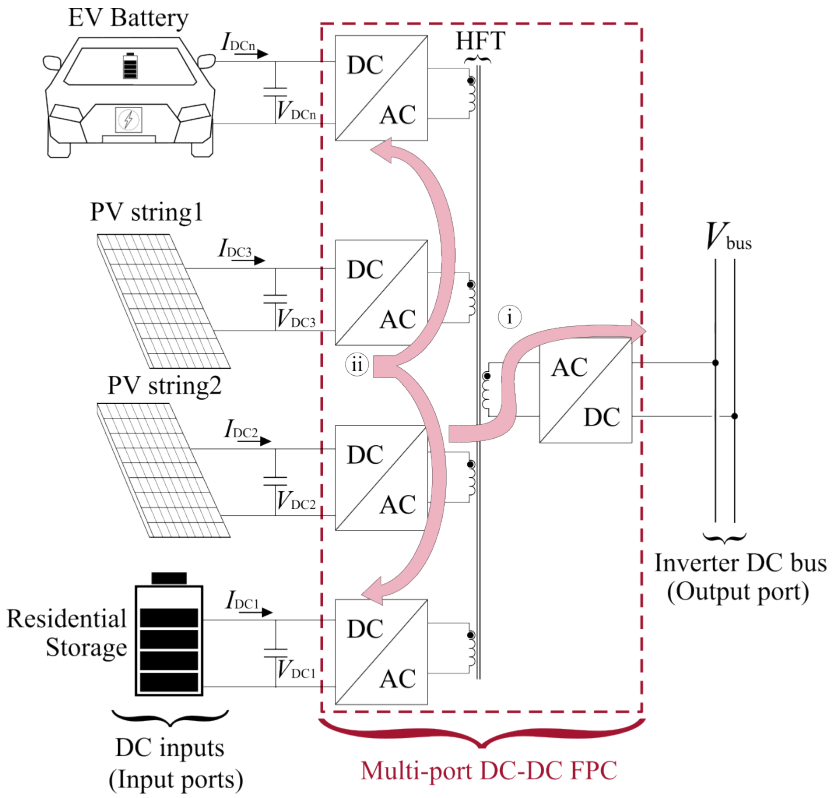


Figure 2.15: Multi-port FPP architecture using multi-winding transformer.

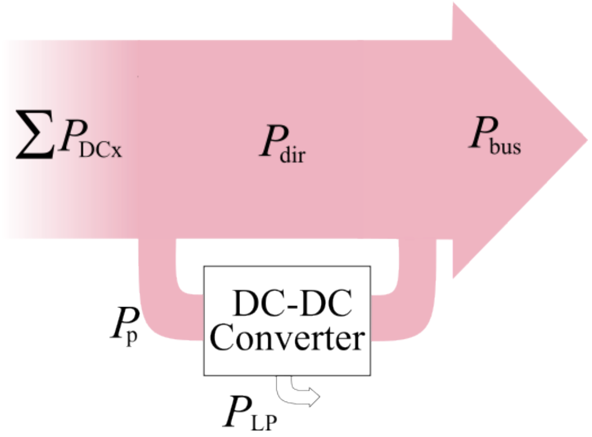


Figure 2.16: Power flow diagram of partial power processing (PPP) architectures.

In addition, the energy conservation equation of the PPP can be expressed by using the relationship in the diagram as:

$$\Sigma P_{\mathrm{DCx}} = P_{\mathrm{dir}} + P_{\mathrm{p}} = P_{\mathrm{bus}} \tag{2.7}$$

Considering the ideal power processing that ignores the losses, Fig. 2.16 and (2.7) shows that the energy conservation between P_{DCx} and P_{bus} of the PPP can be achieved by the summation of P_{dir} and P_{p}.

	PPP architecture			
Topology	DPC	FRPC	PPC	
			IPOS	ISOP
Applications	PV	EV charging	EV charging	
		PV	PV	
		Residential Storage	Residential Storage	

Figure 2.17: Categorization of partial power processing (PPP) architectures.

The different types of the PPP architectures have been actively researched to improve the efficiency and PD for the different applications [50, 51]. The categorization of PPP architectures are depicted in Table. 2.17. The PPP architectures can be divided into three large categories: i) differential power converters (DPCs) [52–64], ii) fractional power converters (FRPCs) [65–71], and iii) Partial Power Converters (PPCs) [72–88]. The PPP concept of each architecture are visualized by the VA area model. The VA area model can be plotted by placing the voltage amplitude on the vertical and lying the current amplitude on the lateral [89]. In order to select the optimal PPP architecture for the smart home applications, the PPP architecture options have been investigated and compared.

Differential power converter

The architecture of differential power converters (DPC) is depicted in Fig. 2.18 (a). The input DC voltage V_{DC} of the DPCs is separated by the multiple series capacitors (C_{p1} to C_{pi}). The DPCs perform energy balancing between the sub-partial-DC voltages (V_{p1} to V_{pi}) on C_{p1} to C_{pi}. Using the Kirchhoff's current law (KCL), the differential current processed on each DPCs can be expressed as follows:

$$I_{\mathrm{dpc}_i} = I_{\mathrm{p}_i} - I_{\mathrm{p}_{i+1}} + D_{\mathrm{i-1}} I_{\mathrm{dpc(i\text{-}1)}} + (1 - D_{\mathrm{i+1}}) I_{\mathrm{dpc}_{i+1}} \tag{2.8}$$

where $D_{\mathrm{i}}|_{\mathrm{i}=1,2,\cdots,\mathrm{n}}$ is the duty cycle of each DPC and I_{dpc_i} is current flowing through each DPCs.

The equation shows that the DPCs process the differential current between each converters. Therefore, the power processed on the DPCs can be achieved by the partial voltage (V_{p_i})

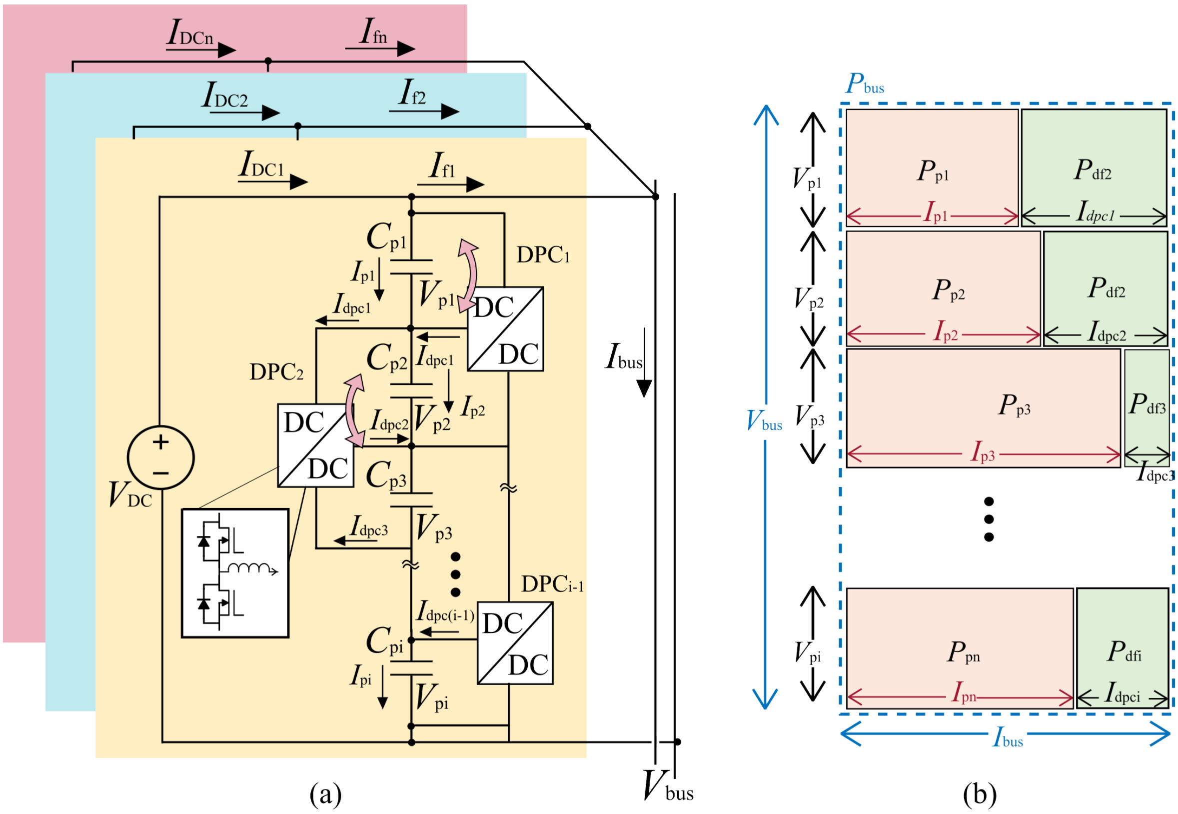


Figure 2.18: Differential power converter (DPC): (a) schematics and (b) VA area model.

partial current (I_{dpc_i}). The total differential power processed on the DPCs can be written as:

$$\Sigma P_{\mathrm{df}_i} = V_{\mathrm{p}_i} I_{\mathrm{dpc}_i} \tag{2.9}$$

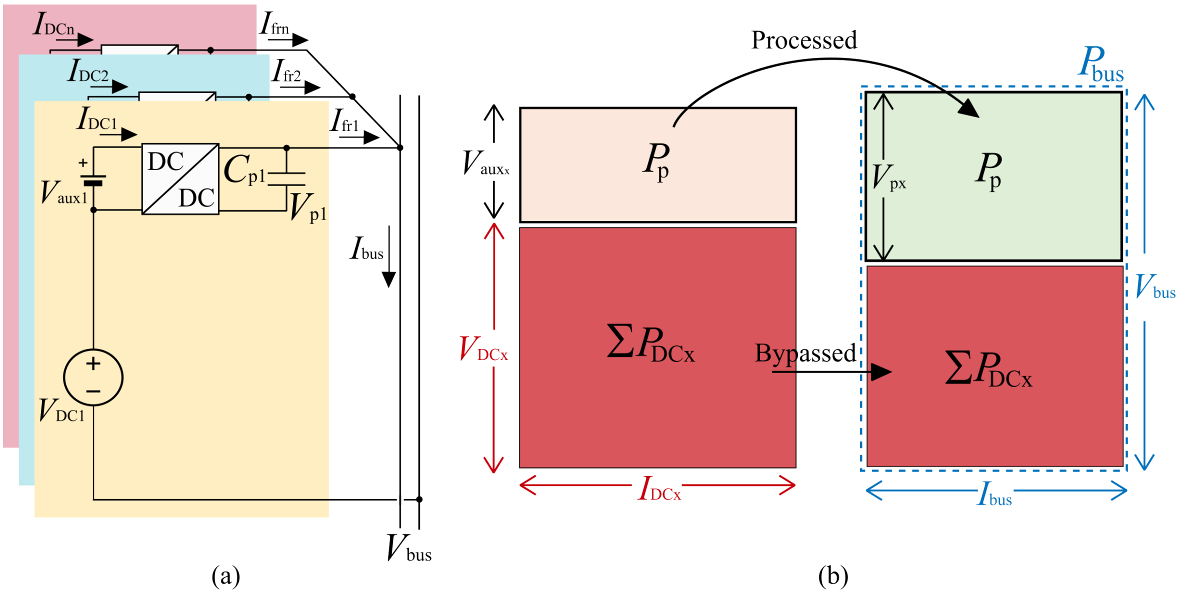
where P_{df_i} is the differential power that $i^{th}|_{\mathrm{i}=1,2,\cdots,\mathrm{n}}$ DPC processes, V_{p_i} is the partial voltage on the series capacitor C_{pi}, and I_{dpc_i} is the differential current that i^{th} DPC processes.

The PPP of the DPCs can be visualized by the VA area model as shown in Fig. 2.18 (b). The VA area model shows that the total DPC shares the full input DC voltage V_{DC}. However, the PPP can be achieved by processing the partial current which is I_{dpc_i}. If there is the power imbalance between the C_{pi}, the DPCs will compensate the differential power between each C_{pi} with I_{dpc_i}.

According to (2.8) and (2.9), the DPCs process the partial voltage and current which are V_{pi} and I_{dpci}. Therefore, the volume of the individual DPC can be reduced by using decreased rating active and passive elements. However, in order to build the DC-DC converter that considering the total i number of DPCs with n DC inputs, the DPCs have to use too many active and passive elements.

Fractional power converter

The fractional power converters (FRPC) topology is shown in Fig. 2.19 (a). In order to build the FRPC, auxiliary partial DC voltage sources ($V_{\mathrm{aux}_\mathrm{x}}|_{\mathrm{x}=1,2,\cdots,\mathrm{n}}$) should be used. The DC-DC



(a) (b)

Figure 2.19: Fractional power converter (FRPC): (a) schematics and (b) VA area model.

converters process the optimum current for each input sources demands.

In Fig. 2.19 (b), the power processing characteristics of FRPC is described using the VA area model. The VA area model shows that the power processing of the FRPC is similar to the power processing of the FPP that shown in Fig. 2.13 (b). However, V_{aux_x} of the FRPC has the lower voltage than the input DC voltage which makes the partial voltages can be processed for each DC-DC converter of the FRPC. The rest of the power, ΣP_{DCx}, is bypassed directly to the bus side. Therefore, the FRPC can process partial power by controlling the required current, I_{DCx}, from the partial voltage of the auxiliary DC sources V_{aux_x}. Using the qualitative analysis in Fig. 2.19 (b), the relationship between input and output power can be expressed as follows:

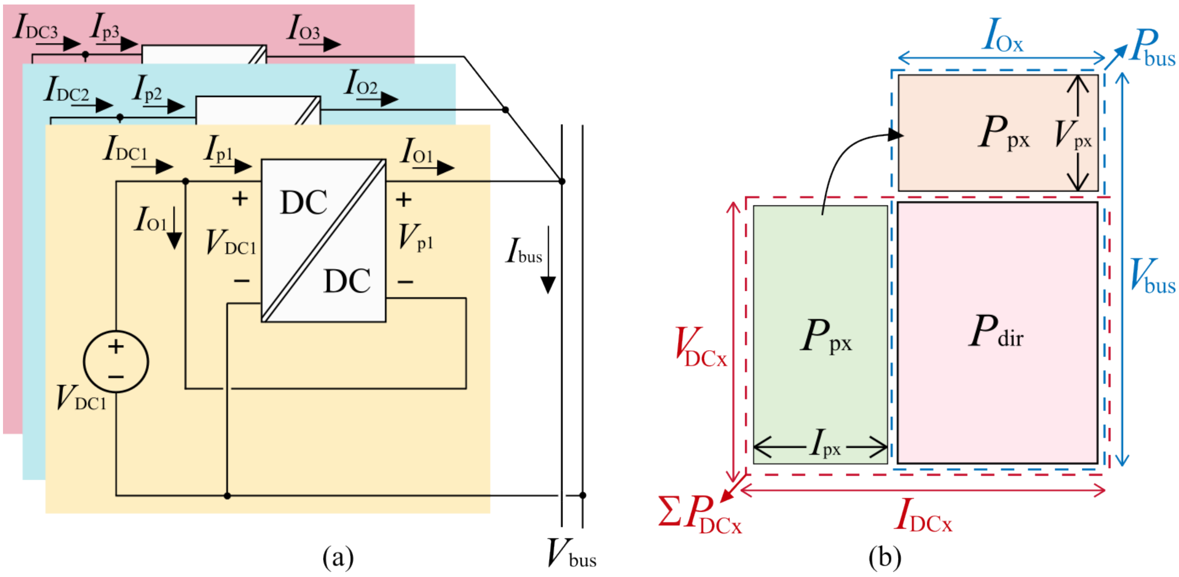
$$V_{bus}\Sigma I_{frx} = \Sigma \left(\underbrace{V_{DCx} I_{DCx}}_{\text{Bypassed power}} + \underbrace{V_{aux_x} I_{DCx}}_{\text{Processed power}} \right) \tag{2.10}$$

where I_{frx} is the output current of each FRPC and V_{aux_x} is the auxiliary voltage of each input port.

The advantage of FRPC is that the conventional low voltage rating DC-DC converters that can process V_{aux_x}, can be used. However, it is necessary to use auxiliary partial DC voltage sources. Therefore, the additional DC sources increase the cost and volume of the overall system.

Partial power converter

A PPC topology of an input parallel output series partial power converter (IPOS PPC) is depicted in Fig. 2.20 (a). The DC-DC converter of the IPOS PPC is built by the isolated converter topology, which delivers the power from the input to the output port by phase shift modulation. The IPOS PPC has the parallel node on the input which connected to the



(a) (b)

Figure 2.20: Input parallel-Output series partial power converter (IPOS PPC) architecture: (a) schematics and (b) VA area model.

negative port of the output and the positive node of the output port is connected in series to the inverter side DC bus. The full DC input voltage V_{DCx} is applied to the input side of the IPOS PPC. Due to the parallel node on the input side, the following voltage and current relationship can be satisfied:

$$\begin{aligned} V_{\mathrm{bus}} &= V_{\mathrm{DCx}} + V_{\mathrm{px}} \\ I_{\mathrm{Ox}} &= I_{\mathrm{DCx}} - I_{\mathrm{px}} \end{aligned} \tag{2.11}$$

Therefore, the power processed on the input side of the IPOS PPC can be expressed as $V_{\mathrm{DCx}} I_{\mathrm{px}}$. The processed power expression shows that the partial power on the input side of the IPOS PPC can be achieved by processing full voltage-partial current. The positive node of the output port of IPOS PPC is connected in series between V_{bus}. A partial voltage V_{p} is applied to the output of the IPOS PPC. The full output current I_{Ox} is processed on the inverter DC bus side of the IPOS PPC. Hence, the power processed on the output side of the IPOS PPC is $V_{\mathrm{p}} I_{\mathrm{Ox}}$. This shows that partial power on the output side can be achieved by processing partial voltage-full current. Finally, on the bus side, the total output current of the IPOS PPC flows also can be expressed as $I_{\mathrm{bus}} = \Sigma I_{\mathrm{Ox}}$. Using the voltage applied on the input and output of the IPOS PPC, the processed partial power at the IPOS PPC can be written as follows:

$$P_{\mathrm{px}} = V_{\mathrm{DCx}} I_{\mathrm{px}} = V_{\mathrm{px}} I_{\mathrm{Ox}} \tag{2.12}$$

where P_{px} is the partial power processed on the DC-DC converters.

Using (2.12), the energy conservation of input and output of the whole system can be expressed as:

$$V_{\mathrm{DCx}}I_{\mathrm{DCx}} = V_{\mathrm{DCx}}(I_{\mathrm{px}} + I_{\mathrm{Ox}}) = V_{\mathrm{px}}I_{\mathrm{Ox}} + V_{\mathrm{DCx}}I_{\mathrm{Ox}} = V_{\mathrm{bus}}I_{\mathrm{Ox}} \tag{2.13}$$

The voltage and current relationship between the input and output of the IPOS PPC can be visualized by the VA area model that depicted in Fig. 2.20 (b). The VA area model of IPOS PPC shows the KCL on the parallel node at the input, where I_{Ox} is formed by the subtraction between I_{DCx} and I_{px}. The figure also shows that the sum of V_{DCx} and V_{px} yields V_{bus}. This means that the IPOS PPC is suitable for the application where $V_{\mathrm{DCx}} < V_{\mathrm{bus}}$ (Boost applications). The relationship between the processed power of the IPOS PPC and the input-output power can be written as follows:

$$\underbrace{V_{\mathrm{DCx}}I_{\mathrm{px}} = V_{\mathrm{px}}I_{\mathrm{Ox}}}_{\text{processed power on the IPOS PPC}} < \underbrace{V_{\mathrm{DCx}}I_{\mathrm{DCx}} = V_{\mathrm{bus}}I_{\mathrm{Ox}}}_{\text{System power}} \tag{2.14}$$

Equation (2.14) shows that the processed power on the IPOS PPC is lower than the input-output power. Therefore, the IPOS PPC can use the devices with a lower power rating, resulting in reducing the size of the IPOS PPC. Finally, the rest of the power which is not processed on the IPOS PPC can be written as:

$$P_{\mathrm{dir}} = V_{\mathrm{DCx}}I_{\mathrm{DCx}} - V_{\mathrm{DCx}}I_{\mathrm{px}} = V_{\mathrm{DCx}}I_{\mathrm{Ox}} \tag{2.15}$$

where P_{dir} is the unprocessed power which is the power directly bypassed to the V_{bus} without the power processing by the IPOS PPC.

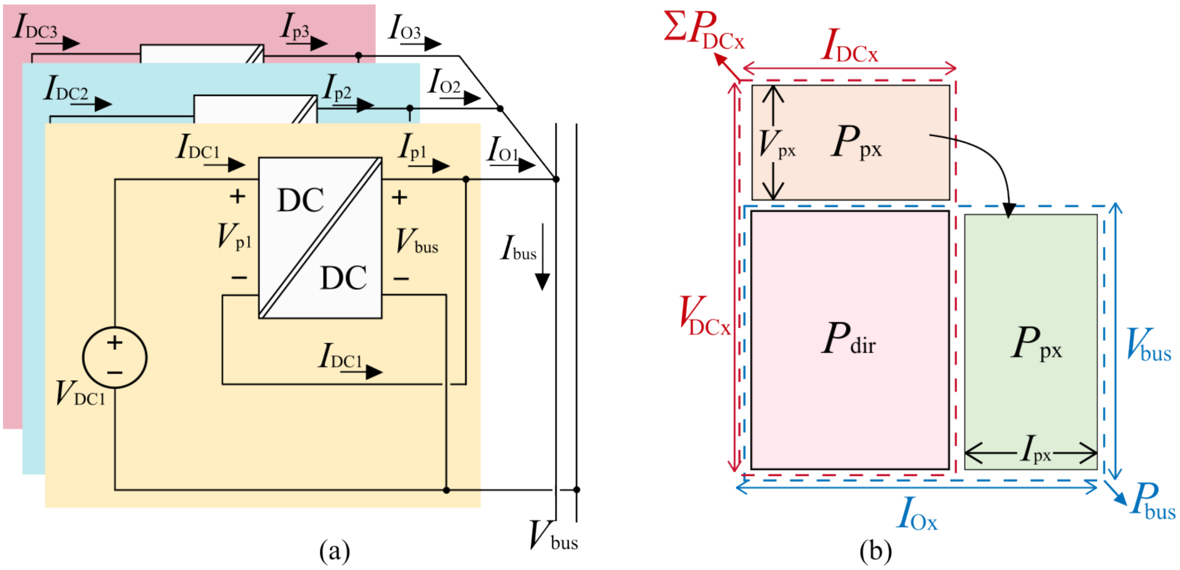


Figure 2.21: Input series-Output parallel partial power converter (ISOP PPC): (a) schematics and (b) VA area model.

Another PPC topology called input series output parallel partial power converter (ISOP PPC) is depicted in Fig. 2.21 (a). The DC-DC converter of the ISOP PPC is also built by the isolated converter topology which delivers the power from the input to output as the same manner of IPOS PPC. The ISOP PPC has symmetrical topology compared to the IPOS PPC where the converter has series connection between the DC inputs, and the parallel node on the output which connected to the negative port of the input. The voltage-current relationship at the parallel node of the ISOP PPC can be expressed as:

$$\begin{aligned} V_{\mathrm{bus}} &= V_{\mathrm{DCx}} - V_{\mathrm{px}} \\ I_{\mathrm{Ox}} &= I_{\mathrm{DCx}} + I_{\mathrm{px}} \end{aligned} \tag{2.16}$$

On the input side of the ISOP PPC, V_{p} is applied with processing full input current I_{DCx}. On the bus side, the partial current I_{px} is processed with the full bus voltage V_{bus}. Eventually, the P_{px} processed on the single ISOP PPC can be expressed as follows:

$$P_{\mathrm{px}} = V_{\mathrm{px}} I_{\mathrm{DCx}} = V_{\mathrm{bus}} I_{\mathrm{px}} \tag{2.17}$$

The equation shows that the partial power on the input side is achieved by processing partial voltage-full current, and on the inverter bus side can be achieved by processing full voltage-partial current. Using (2.17), the energy conservation of the input and output of the ISOP applied system also can be written as follows:

$$V_{\mathrm{bus}} I_{\mathrm{Ox}} = V_{\mathrm{bus}}(I_{\mathrm{px}} + I_{\mathrm{DCx}}) = V_{\mathrm{px}} I_{\mathrm{DCx}} + V_{\mathrm{bus}} I_{\mathrm{DCx}} = V_{\mathrm{DCx}} I_{\mathrm{Ox}} \tag{2.18}$$

The voltage and current relationship between the input and output of the ISOP PPC can be visualized by the VA area model that depicted in Fig. 2.21 (b). The VA area model shows the voltage and current flow of the ISOP PPC has the symmetric characteristic compared to the IPOS PPC which also means that the ISOP PPC is optimal for the buck applications. The relationship of the processed power on the ISOP PPC and the input-output power can be written as follows:

$$\underbrace{V_{\mathrm{px}} I_{\mathrm{DCx}} = V_{\mathrm{bus}} I_{\mathrm{px}}}_{\text{processed power on the ISOP PPC}} < \underbrace{V_{\mathrm{DCx}} I_{\mathrm{DCx}} = V_{\mathrm{bus}} I_{\mathrm{Ox}}}_{\text{System power}} \tag{2.19}$$

Equation (2.19) also shows that the processed power on the ISOP PPC is lower than the input-output power. Therefore, the ISOP PPC can use decreased power rating devices which yield the decrease of the converter size. Finally, the unprocessed power P_{dir} can be written as:

$$P_{\mathrm{dir}} = V_{\mathrm{DCx}} I_{\mathrm{DCx}} - V_{\mathrm{p}} I_{\mathrm{DCx}} = V_{\mathrm{bus}} I_{\mathrm{DCx}} \tag{2.20}$$

Comparison of the PPP architectures

The comparison of the PPP architectures are shown in Table. 2.2. In the table, '*n*' represents the number of DC inputs and '*i*' represents the number of series connected DC-DC

Table 2.2: Comparison of PPP architectures

Architecture	Transformer	V_{aux}	Switches	P_{p} (p.u.)	cost	size
DPC	X	X	$2n \cdot i$	0.15	-	+
FRPC	X	n	$2n$	0.25	-	-
PPC	n	X	$8n$	0.3	+	-

converters of the DPC architecture. Firstly, comparing the transformer requirements, the PPC architecture always requires one transformer for each DC input. On the other hand, the DPC and FRPC architectures don't require the transformers. However, the FRPC requires n-number of auxiliary DC sources to build the architecture while the other architectures do not. The use of auxiliary DC sources has greater chance of increasing the costs, voltage, and reducing the reliability of the architecture. When comparing the number of switches, the DPC has the highest number of switches because i number of converters have to be used in order to build the single DPC. Therefore, the DPCs need $2n \cdot i$ of switches for n number of inputs. The PPC needs $8n$ switches to build the architecture for n-number of inputs. The power processed by the DC-DC converters of each PPP architectures can be compared. Setting the base power as the input power, the DPC can process 15 % of the total power, which is the lowest power processing compared to the other architectures. Due to the low power processing capability, DPC can have the smallest size compared to the other architectures. However, using too many devices can increase the costs of the DPCs. The FRPC architecture can process 25 % of the input power. Even though FRPC has the PPP capability, the use of V_{aux_x} for each input has a large impact on increasing the costs and volume of the overall architecture. Hence, the FRPC architecture is the least advantageous architecture compared to the others. On the other hand, the PPC has 30 % of the PPP capability, which is higher than that of DPC and FRPC. The reduced rating switches and transformer can give the advantage on the cost. However, the use of n-number of transformers can increase the volume of the architecture compared to DPC.

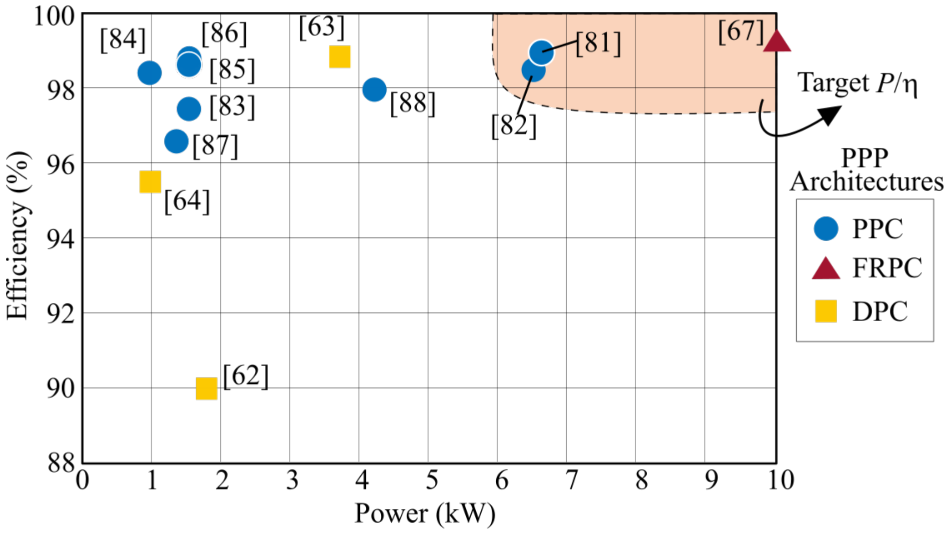


Figure 2.22: Efficiency comparison of the state of the art PPP architectures. (Only the most relevant publications that provide experimental data are included.).

The efficiency of the architectures that recently studied is compared from the literature review, in order to check the highest efficiency that prior PPP architecture studies reached. The results of the most relevant prior art studies in the few kW range are plotted in Fig. 2.22, where the efficiency is proven by the experiments. The target power versus efficiency (P/η) of this study is highlighted in red color. The FRPC of [68] achieved the highest efficiency, which is 99 % with a 10 kW prototype. Compared to [68], the PPC studies of [82] and [84] have slightly lower efficiencies, achieving 98.5 % with 6.5 kW prototype. The target of this study is to achieve the efficiency > 98.5 % with the rated power of a prototype higher than 6.5 kW.

2.3 Summary

In this chapter the comparison of the PLL and self-synchronization is performed to choose the optimum synchronization method for the inverter applied to the smart home. The analysis and experimental results show that the stability of the PLL can be limited by current amplitude (I_{m}), filter inductance (L), and its bandwidth (f_{BW}). On the other hand, the stability of the self-synchronization is not limited by I_{m}, L, and f_{BW}. Hence, self-synchronization is chosen for the grid synchronization method which is more robust than the PLL.

The DC-DC converter stage has different power processing architectures. The full power processing (FPP) DC-DC converters are the most widely used conventional power processing architecture in industry. The FPP converters process all the power from the DC inputs and delivers it to the inverter side DC bus. One method to build an FPP architecture for the smart home is to use multiple numbers of converters that connected to the inverter DC bus. Using this strategy, the DC-DC converters can be designed to carry out desired function for each DC input. The other method is to use multi-port FPP converters that use multi-winding transformer. The use of multi-port FPP can provide high modularity by using the same converter topology for the all DC inputs.

The partial power processing (PPP) architecture is another power processing architecture that can process reduced power compared to the FPP. By processing the partial power from the DC inputs, the efficiency of the DC-DC stage can be improved compared to FPP. There are three possible architectures that are optimal for smart home applications: i) DPC, ii) FRPC, iii) PPC. The PPP architectures are compared in a table to compare the advantages and limitations of each architecture. Furthermore, the efficiency of the most relative recent studies are plotted in the graph to set the benchmark of this study.

From the next section, a novel multi-port PPC architecture is proposed. Based on Table. 2.2 and Fig. 2.22, a multi-port converter architecture can have the high efficiency with the low cost by using PPC. The key idea of the proposed architecture are: i) achieve efficiency higher than 98.5 %, ii) make cost efficient architecture by using the partial power rated passive and active power electronics components, and iii) to improve the power density compared to the prior art PPCs.

3 Multi-port partial power converter architecture development

The general schematic of the proposed multi-port PPC architecture for the smart home applications is shown in Fig. 3.1. The aim of the proposed architecture is to achieve higher efficiency with the reduced power density and costs compared to the benchmarks in the target P/η region. The proposed architecture uses the multi-port PPC with the single partial power rated DC transformer to build the multi-port converter architecture for the smart home applications. The isolation on the DC transformer stage can limit the power between the DC input and bus during the fault similar as the isolation of the conventional FPCs. On the DC input side ($V_{\mathrm{DCx}}|_{\mathrm{x}=1,2,\cdots,\mathrm{n}}$) of the proposed multi-port PPC, multiple partial power rated converters control the target current of the DC inputs. The DC input power can be written as follows:

$$\Sigma P_{\mathrm{DCx}} = \Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}} \tag{3.1}$$

where P_{DCx} is the DC input power on each ports, V_{DCx} is the DC input voltage, and I_{DCx} the DC input current.

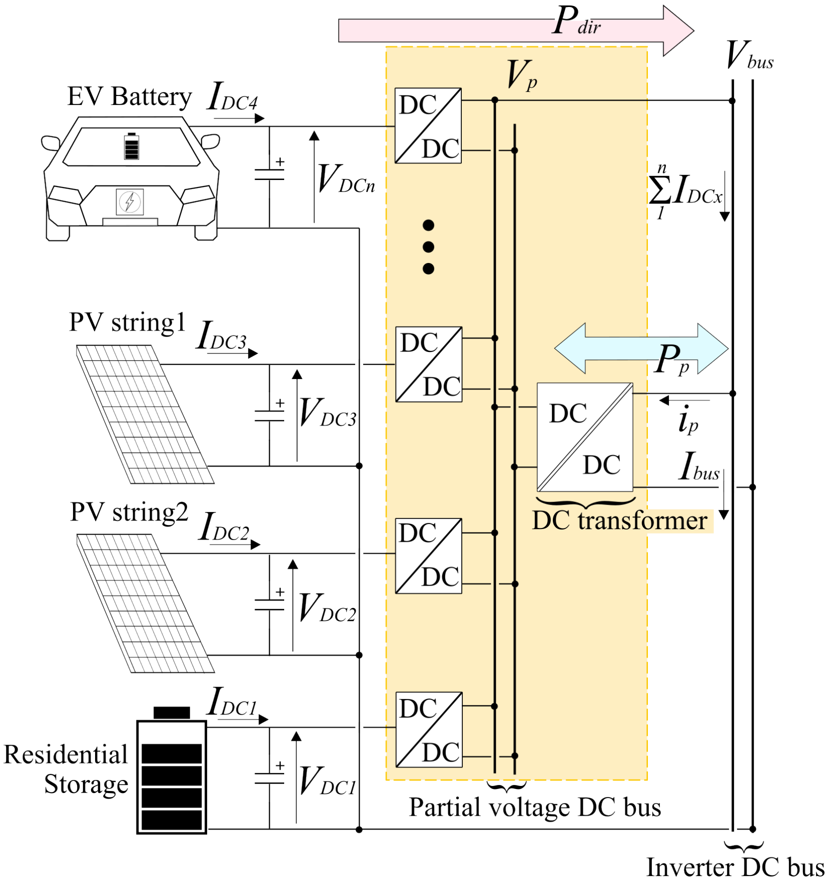


Figure 3.1: Architecture of the proposed novel multi-port PPC.

The inverter DC bus side power which is the output power of the system can be obtained as follows:

$$P_{\mathrm{bus}} = V_{\mathrm{bus}} I_{\mathrm{bus}} = V_{\mathrm{bus}}(\Sigma I_{\mathrm{DCx}} - I_{\mathrm{p}}) \tag{3.2}$$

where P_{bus} is the inverter DC bus power of multi-port PPC, V_{bus} is the inverter side DC bus voltage, I_{bus} is the inverter side DC bus current, and I_{p} is the RMS current on the DC transformer.

The power of the multi-port PPC should satisfy the energy conservation principle which is $\Sigma P_{\mathrm{DCx}} = P_{\mathrm{bus}}$. The input/output power relationship of the proposed architecture can be expressed as follows:

$$\Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}} = V_{\mathrm{bus}}(\Sigma I_{\mathrm{DCx}} - I_{\mathrm{p}}) = V_{\mathrm{bus}} \Sigma I_{\mathrm{DCx}} - V_{\mathrm{bus}} I_{\mathrm{p}} \tag{3.3}$$

Equation (3.3) shows that energy conservation can be achieved through the partial power flow at the DC transformer by processing I_{p}. Reorganizing the equation with respect to the partial power $V_{\mathrm{bus}} I_{\mathrm{p}}$, the equation can be written as follows:

$$P_{\mathrm{p}} = V_{\mathrm{bus}} I_{\mathrm{p}} = V_{\mathrm{bus}} \Sigma I_{\mathrm{DCx}} - \Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}} \tag{3.4}$$

where P_{p} is the partial power that multi-port PPC processes.

The partial power rated converters those are connected in parallel to the partial DC bus V_{p}. Therefore, the power rating of the converters connected in parallel to V_{p} also can be written as follows:

$$P_{\mathrm{p}} = V_{\mathrm{p}} \Sigma D_{\mathrm{x}} I_{\mathrm{DCx}} = V_{\mathrm{bus}} I_{\mathrm{p}} \tag{3.5}$$

where D_{x} is the duty cycle of the converters that connected in parallel to V_{p}. Equation (3.5) shows that the partial power of the PVCs can be achieved with processing partial voltage full current, and the DC transformer can be achieve by processing full voltage partial current.

The partial current can be derived from (3.4) as:

$$I_{\mathrm{p}} = \Sigma I_{\mathrm{DCx}} - \frac{\Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}}}{V_{\mathrm{bus}}} \tag{3.6}$$

Putting (3.5) in (3.4), the equation can be reorganized as follows:

$$V_{\mathrm{bus}} \Sigma I_{\mathrm{DCx}} = \Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}} + \Sigma D_{\mathrm{x}} V_{\mathrm{p}} I_{\mathrm{DCx}} \tag{3.7}$$

Solving (3.7), the voltage relationship between V_{bus} and V_{DCx} can be obtained as:

$$V_{\mathrm{bus}} = V_{\mathrm{DCx}} + D_{\mathrm{x}} V_{\mathrm{p}} \tag{3.8}$$

The unprocessed power can be obtained by averaging the subtraction between DC input power and input processed power (ΣP_{DCx} and P_{p}), and inverter side power and inverter side processed power (P_{bus} and P_{p}). The rest of the power (P_{dir}) which is not processed by the converter can be calculated as:

$$P_{\mathrm{dir}} = \frac{\Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}} - \Sigma D_{\mathrm{x}} V_{\mathrm{p}} I_{\mathrm{DCx}} + V_{\mathrm{bus}} I_{\mathrm{bus}} - V_{\mathrm{bus}} I_{\mathrm{p}}}{2} = I_{\mathrm{bus}} \Sigma V_{\mathrm{DCx}} \tag{3.9}$$

Applying the VA area model to (3.1)–(3.9), the total input/output power and the partial input/output power can be visualized as shown in Fig. 3.2. The VA area model clearly shows that the partial power P_{p} is processed by the converter. Therefore, the size of the converter can be reduced by using partial power magnetic and semiconductor components.

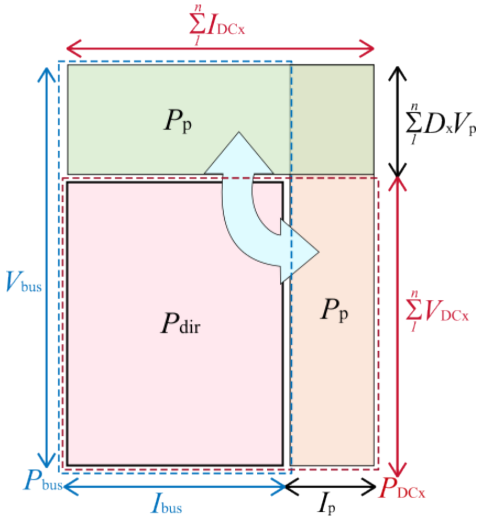


Figure 3.2: Volt-ampere (VA) are model of the proposed PPC.

The power processed by the parallel converters to V_{p} can be achieved by processing the full current partial voltage owing to V_{p}. To keep the nomenclature simple, the converters parallel to V_{p} and V_{DCx} are called partial voltage allowed converters (PVCs).

Between V_{p} and the inverter side DC bus (V_{bus}) there is a partial power DC transformer. The DC transformer controls V_{p} and also exchanges the partial power between V_{bus} and V_{DCx}. The partial power at the DC transformer can be expressed in the same way as (3.4). From the equation, it can be seen that the DC converter can achieve Partial Power Processing (PPP) by processing the partial current to full voltage.

The advantages of the proposed concept are: i) the multi-port PPC can improve efficiency by processing partial power, ii) it is possible to reduce the size of the transformer by using partial rated power, and iii) the active and passive devices that have the partial rated voltage and current can be used.

There are several topology options for the PVCs and the DC transformer. The PVCs have three topology options: i) Boost type, ii) Buck type and iii) Buck-boost type. In addition, the DC transformer has two topology options: i) dual active bridge (DAB) and ii) series resonant converter (SRC). The behavior and characteristics of the PVCs and DC transformers can be modified by selecting the different topology options. The optimal topology selection for each PVC and DC converter for a multi-port PPC is first discussed in this section. The purpose of the proposed multi-port PPC is to: a) use minimum passive element size by using a partial power rating, b) maximize efficiency. The choice of topology is made to achieve objectives a) and b).

3.1 Description of the target specification

Firstly, the operating point of the multi-port PPC should be decided. One of the key functions of the multi-port PPC is to harvest the power from the PV strings, which is the connection of multiple PV panels. The power from the PV is harvested by measuring a maximum power point tacking (MPPT) algorithm. In Table. 3.1, the voltage and current levels of commercial PV panels are organized. The open circuit voltage of PV panels (V_{oc}) is in the range of 37 V $\leq V_{\text{oc}} \leq$ 48 V and the MPPT voltage (V_{mpp}) of commercial PV panels is in the range of 34 V $\leq V_{\text{mpp}} \leq$ 41 V. For the study, the residential PV inverter is assumed to be connected to 8 to 10 series PV panels on the roof. The target voltage level of the PV panels is in the range of 330 V $\leq V_{\text{mpp}} \leq$ 400 V at full irradiation. The nominal input voltage chosen for the study is V_{DCx} =360 V, which considers 10 PV panels connected in series. The target nominal DC input power (P_{DCx}) is chosen as 4 kW. Considering the average MPP current (I_{mpp}), the nominal input current can be chosen as I_{DCx} =11 A.

The selection of the partial voltage V_{p} is one of the most important factors in determining the amount of power to be processed by the multi-port PPC, and also in determining the power processing range of the proposed multi-port PPC. The input DC voltage range of the multi-port PPC can be written as follows:

$$V_{\text{bus}} - V_{\text{p}} \leq V_{\text{DCx}} \leq V_{\text{bus}} \tag{3.10}$$

Based on (3.10), the maximum input voltage can be tracked up to V_{bus} and the minimum input voltage tracking range is determined by subtracting V_{bus} from V_{p}. The inverter side DC bus voltage of the multi-port PPC is set to $V_{\text{bus}} = 400$ V. Therefore, the minimum input voltage range can be determined by selecting the partial voltage V_{p}.

In Fig. 3.3, the p.u. date of PV voltage and power data based on a full power residential PV inverter is plotted. The data is measured from 6:00 to 20:00 for 27 days. Assuming the base power is 4 kW and V_{bus} is 400 V, the partial voltage condition can be chosen from the p.u. analysis of PV voltage and power data. In Fig. 3.3 (a), the $V_{\text{bus}} - V_{\text{pv}}$ (where V_{pv} is the PV voltage) measurement data is plotted. In the morning from 6:00 to 7:00, the range of voltage gap of $V_{\text{bus}} - V_{\text{pv}}$ is between 0.25 to 1 p.u. where the range of absolute value is 100 V $< V_{\text{bus}} - V_{\text{pv}} \leq$ 250 V. To satisfy the condition in (3.10), the proposed multi-port PPC needs $V_{\text{p}} \approx 250$ V to perform MPPT in the early morning between 6:00 and 7:00. On the other hand, the voltage gap $V_{\text{bus}} - V_{\text{pv}}$ less than 0.25 p.u. can be observed during the daytime between 08:00 and 18:00 which absolute value is $V_{\text{bus}} - V_{\text{pv}} <$ 100 V. This means that the maximum power point (MPP) can be tracked with $V_\mathrm{p} \leq 100$ V between 08:00 and 18:00. After 19:00, $V_\mathrm{bus} - V_\mathrm{pv}$ is again between 0.25 to 1 p.u (160 V $< V_\mathrm{bus} - V_\mathrm{pv} \leq$ 250 V), which requires $V_\mathrm{p} \approx$ 250 V to achieve MPPT in multi-port PPC.

To choose specific voltage of V_p, the measured data of the PV energy production for 27 days is also analyzed in Fig. 3.3 (b). In the early morning between 6:00 and 7:00 and in the evening between 19:00 and 20:00, almost no energy is produced. In between these times a small amount of energy is produced by the PV. As discussed earlier, the absolute value of V_p needs to be 250 V to perform MPPT in the morning and evening. However, the time period from 6:00 to 7:00 and from 19:00 to 20:00 can be neglected, because the PV energy production is almost 0. The main PV energy production occurs during the day between 8:00 and 18:00. MPPT can be performed between 8:00 and 18:00 with $V_\mathrm{p} \leq$ 100 V. Therefore, the time between 8:00 and 18:00 is chosen as the target operation period, when most of the PV energy is generated. In this study, the target partial voltage for the multi-port PPC is chosen as $V_\mathrm{p} =$ 150 V. Using (3.10), the voltage of the PV 400 V down to 250 V which is almost 40% of the voltage range of PV curve, can be tracked with 150 V V_p.

The overall specification for the proposed multi-port PPC is shown in Table. 3.2. Following (3.10), the input DC voltage range of 250 V $\leq V_\mathrm{DCx} \leq$ 400 V can be tracked with the selected $V_\mathrm{p} =$ 150 V. Furthermore, using (3.4) and (3.5), the nominal partial power P_p of single port can be calculated as $P_\mathrm{p} =$ 1.5 kW for each 4 kW rated DC inputs. Therefore rated power of the system can be written as $4n$ kW where n is the number of input ports.

The rated voltage and current data for commercial silicon IGBT and MOSFET devices are shown in Fig. 3.4. The optimal semiconductor device should be selected to handle the voltages of $V_\mathrm{p} =$ 150 V and $V_\mathrm{bus} =$ 400 V, and the rated current I_DCx and partial current I_p. In the figure, most IGBTs are manufactured for the rated voltage higher than 400 V. In order to operate the switches for the PVC voltage $V_\mathrm{p} =$ 150 V with the rated current $I_\mathrm{DCx} =$ 11 A, the semiconductor device should be selected in the range of 250 V to 300 V, taking into account the voltage margin. Therefore, a low voltage MOSFET with a voltage and current rating of 300 V, 16 A is selected for the PVC. The low voltage side of the DC converter also shares V_p, so the same MOSFET is selected for the voltage side switching device of the DC converter. The high voltage side of the DC Converter should handle the full bus voltage $V_\mathrm{bus} =$ 400 V with the partial current I_p. To handle the 400 V bus voltage, the rated voltage of the switches should be 650 V, taking into account the voltage margin. The maximum RMS value of $I_\mathrm{p} =$ 7.5 A, calculated using (3.4). The rated current (I_{rate}) can be chosen in the range between 8 A $\leq I_\mathrm{rate} \leq$ 15 A, taking into account the current margin. The I_rate of the 650 V level IGBT is $I_\mathrm{rate} >$ 20 A which rating is above the targeted range. Therefore, a 650 V MOSFET with $I_\mathrm{rate} =$ 16 A is selected for the high voltage side of the DC-DC converter stage switching device. In addition, the type of gate driver can be unified by unifying the type of switching devices (MOSFET) for the multi-port PPC. The detailed information of the devices is shown in Table. 3.3.

Table 3.1: Data of commercial PV panel

Model	Manufacturer	V_{oc}	V_{mpp}	I_{sc}	I_{mpp}	P_{mpp}
CHSM60M	PENTA+	40.75 V	33.98 V	11.35 A	10.98 A	370 W
JKM385M-72H	Jinko Solar	48.10 V	39.50 V	10.08 A	9.76 A	385 W
JKM390M-72H	Jinko Solar	48.14 V	39.62 V	10.17 A	9.84 A	390 W
JKM400M-72H	Jinko Solar	48.35 V	39.83 V	10.23 A	9.92 A	400 W
YLM-J 108	Yingli Solar	37.17	30.80 V	13.15 A	10.52 A	405 W
Tiger60TR	Jinko Solar	42.67 V	35.02 V	11.29 A	10.71 A	350 W
TSM-395	Vertex S	40.40 V	33.40 V	12.00 A	11.38 A	395 W
RSM40-8-390M	Risen Solar	40.69 V	33.88 V	12.21 A	11.52 A	390 W
Tiger66TR	Jinko Solar	43.75 V	36.49 V	11.39 A	10.69 A	390 W
LNMH120	LINUO	41.77 V	34.43 V	11.61 A	11.06 A	380 W
CP17-60H	HANERSUN	41.60 V	34.40 V	11.45 A	10.89 A	375 W
SL5M108	SunLink	37.05 V	31.01 V	13.79 A	12.90 A	400 W
TSM-DE08M.08	Trinasolar	41.90 V	34.70 V	11.52 A	10.96 A	380 W
AU-120MH	AustaEnergy	41.30 V	34.80 V	11.69 A	10.92 A	380 W
PNG-120M	Solarclip	41.30 V	34.80 V	11.69 A	10.92 A	380 W
Meyerburger380	Meyer Burger	44.70 V	38.70 V	10.90 A	10.30 A	395 W
RSM144-7-435M	Risen Solar	49.40 V	41.05 V	11.20 A	10.60 A	435 W
JAM54S30	JA Solar	37.07 V	31.01 V	13.79 A	12.90 A	400 W
AS-6M120-HC	Amerisolar	42.00 V	35.00 V	11.44 A	10.86 A	380 W
BSM440PMB7-46SC	BluesunSolar	41.60 V	34.50 V	12.92 A	12.89 A	420 W
EPP380-120M	EPP Solar	41.68 V	34.30 V	11.65 A	11.08 A	380 W
JAM60D20	JA Solar	41.68 V	34.82 V	11.58 A	11.06 A	385 W
BVM6610M	boviet	41.70 V	35.20 V	11.92 A	11.09 A	390 W
HEX5-182	BluesunSolar	37.25 V	31.24 V	13.86 A	12.97 A	405 W
TSM-405	Vertex S	41.40 V	34.40 V	12.34 A	11.77 A	405 W
JAM60S20	JA Solar	42.07 V	35.62 V	11.63 A	11.09 A	395 W
EPP400-180M10	EPP Solar	36.93 V	30.83 V	13.76 A	12.98 A	400 W
RSM40-8-405MB	Risen Solar	41.60 V	34.64 V	12.40 A	11.70 A	405 W
BVM7609M	boviet	37.00 V	31.05 V	13.78 A	12.89 A	400 W
CP17-60H	HANERSUN	41.60 V	34.40 V	11.45 A	10.89 A	375 W
TSM-435	Vertex S	50.60 V	42.00 V	10.86 A	10.36 A	435 W
TSM-415	Vertex S	49.40 V	41.00 V	10.64 A	10.11 A	415 W

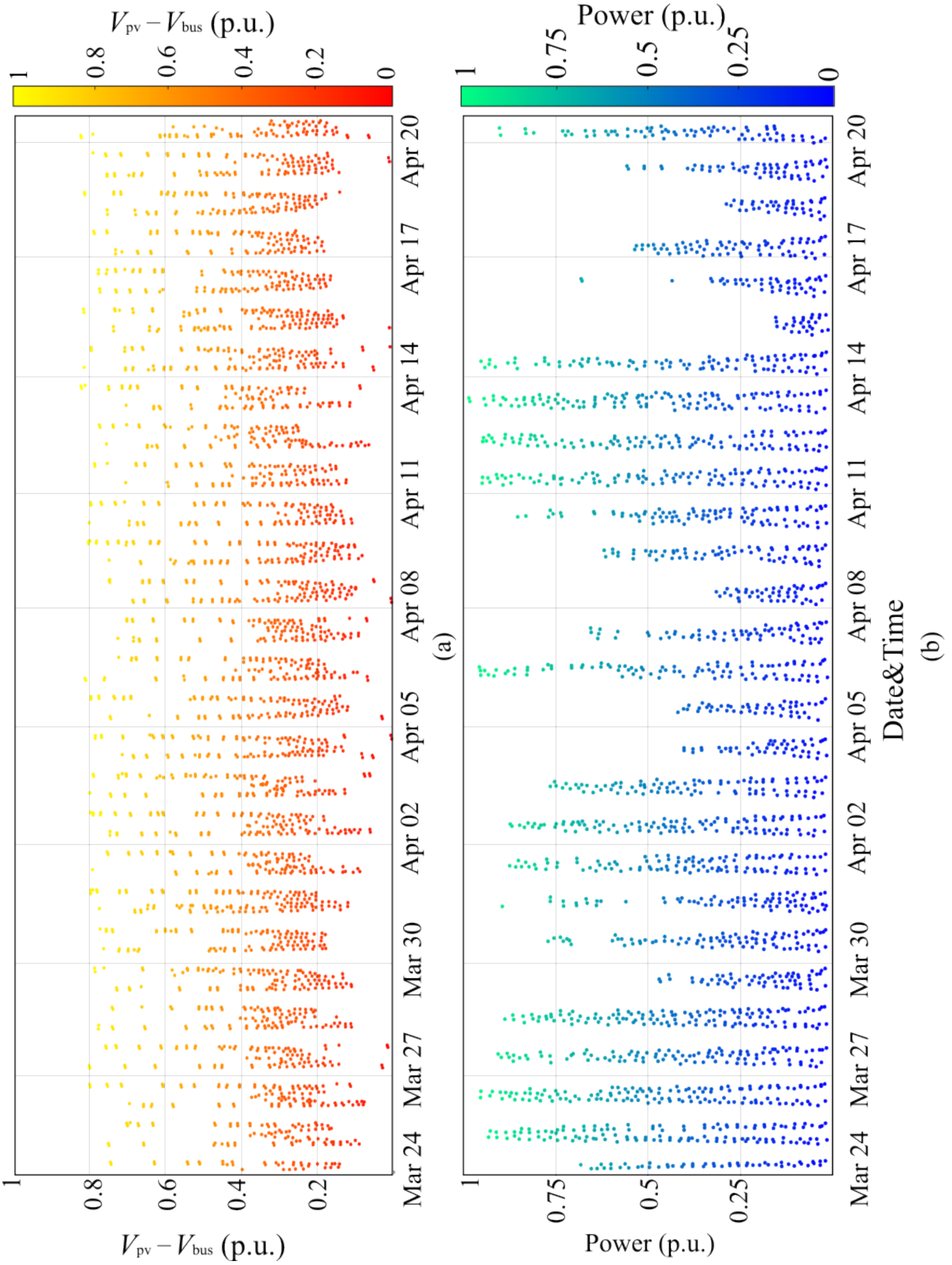


Figure 3.3: Commercial residential full power PV inverter data measurement: (a) Inverter bus side and input PV voltage difference ($V_{bus} - V_{pv}$) and (b) PV power tracking results (P_{pv}).

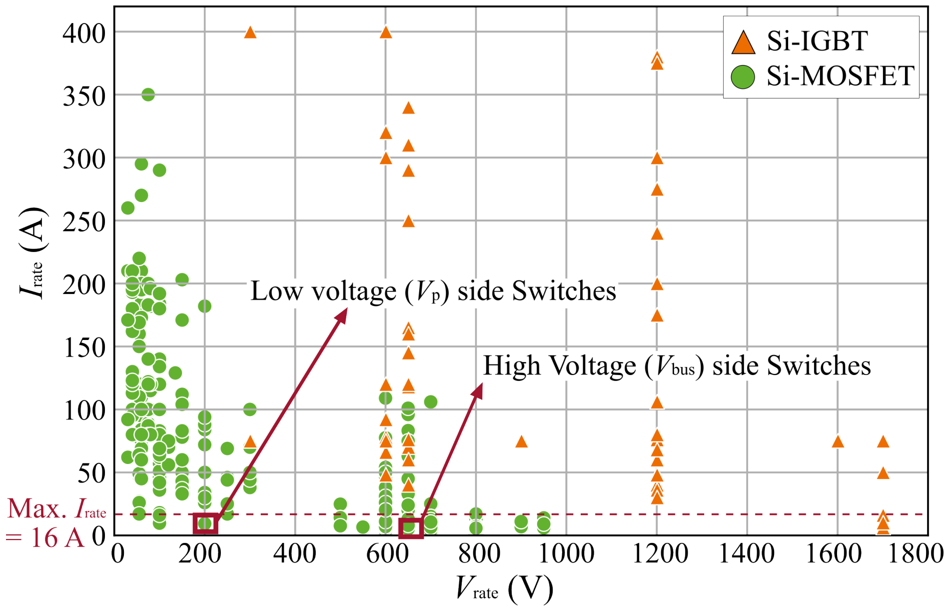


Figure 3.4: Rated voltage and current of commercial Silicon IGBT and MOSFET.

Table 3.2: Target specification of the proposed multi-port PPC

Targets	Symbol	Value	Unit
Nominal DC input power	P_{DCx}	4	kW
Nominal DC input voltage	V_{DCx}	360	V
Nominal DC input current	I_{DCx}	11	A
Bus Voltage	V_{bus}	400	V
Partial Voltage	V_p	150	V
Rated Power	P_{rate}	$4n$	kW
Partial Power	P_p	1.5	kW

Table 3.3: Key data of the selected switching devcies

-	Symbol	BSC430N25NSFD	IPB65R110CDF
Break down voltage	V_B	650 V	250 V
Rated drain current	$I_{d_{rate}}$	16 A	20 A
On state resistance	$R_{ds_{on}}$	110 mΩ	43 mΩ
Gate charge	Q_g	118 nC	13 nC
Pulse current	$I_{D_{pulse}}$	99.6 A	144 A
Commutation speed	di/dt	900 A/µs	1500 A/µs
Reverse recovery charge	Q_{rr}	0.8 µC	227 µC
Reverse recovery time	t_{rr}	150 ns	96 nS
Thermal resistance	R_{jc}	0.6 K/W	0.77 K/W

3.2 Partial voltage converter topology selection

There are three different topologies for the multi-port PPC according to the topology of the parallel converters to V_p as shown in Fig. 3.5: i) Boost type (Fig. 3.5 (a)), ii) Buck type (Fig. 3.5 (b)), iii) Buck-boost type (Fig. 3.5 (c)). The PVCs are highlighted in the figure with a blue box. The boost and buck PVCs are half bridge based topologies. The buck-boost type PVC is a full-bridge based topology. To select the optimum topology for the PVC, the voltage relationship and behavior of each topology option should be accessed. Additionally, the advantage of each topology option should be also compared.

3.2.1 Boost type

The equivalent circuit of the boost type PVC topology option is shown in Fig. 3.5 (a). Due to the equivalent behavior of PVCs, single port analysis can represent all PVCs. The boost type PVC is formed by the multiple half bridge (HB) legs, which are the top switches $S_\mathrm{tx}|_{\mathrm{x}=1,2,\cdots,\mathrm{n}}$ and the bottom switches S_bx. The HB legs are connected in parallel to the partial voltage capacitor (C_p). The positive node of C_p is connected to V_bus and injects Σi_fx into the inverter side DC bus. The switching of S_tx and S_bx forces the current to the filter inductor (L_fx).

The switching states of the boost type topology option are highlighted in Fig. 3.6 (a). In order to analyze the behavior of the boost type PVC, the switching states of the boost type option and the inductor voltages should be examined. The switching states and inductor voltages are shown in Table. 3.4. The S_tx and S_bx switch in a complementary manner. When S_tx is on, i_fx is bypassed directly to V_bus through S_tx. When S_bx is on, i_fx flows on S_bx and to the negative node of C_p. The amplitude of the inductor voltage ripple (ΔV_Lfx) can be calculated by subtracting V_Lfx from the bypass state ($V_\mathrm{DCx} - V_\mathrm{bus}$) to the negative state ($V_\mathrm{DCx} + V_\mathrm{p} - V_\mathrm{bus}$). The result of the calculation is $\Delta V_\mathrm{Lfx} = V_\mathrm{p}$.

Table 3.4: Boost type PVC switching states

S_tx	S_bx	Inductor Voltage (V_Lfx)	States
1	0	$V_\mathrm{DCx} - V_\mathrm{bus}$	Bypass
0	1	$V_\mathrm{DCx} + V_\mathrm{p} - V_\mathrm{bus}$	Negative

The waveform of the switching signal, inductor voltage (V_Lfx) and inductor current (i_f) is shown in Fig. 3.6 (b). As mentioned in Table. 3.4, the switches S_tx and S_bx are complementary. The switching causes a voltage change ($\Delta V_\mathrm{Lfx} = V_\mathrm{p}$) across the filter inductor (L_fx). Therefore, considering the voltage-second balance of the inductor current, the inductor current ripple (Δi_fx) can be calculated:

$$\Delta I_\mathrm{fx} = \frac{(V_\mathrm{DCx} + V_\mathrm{p} - V_\mathrm{bus})}{0.5 L_\mathrm{fx} f_\mathrm{s}} \tag{3.11}$$

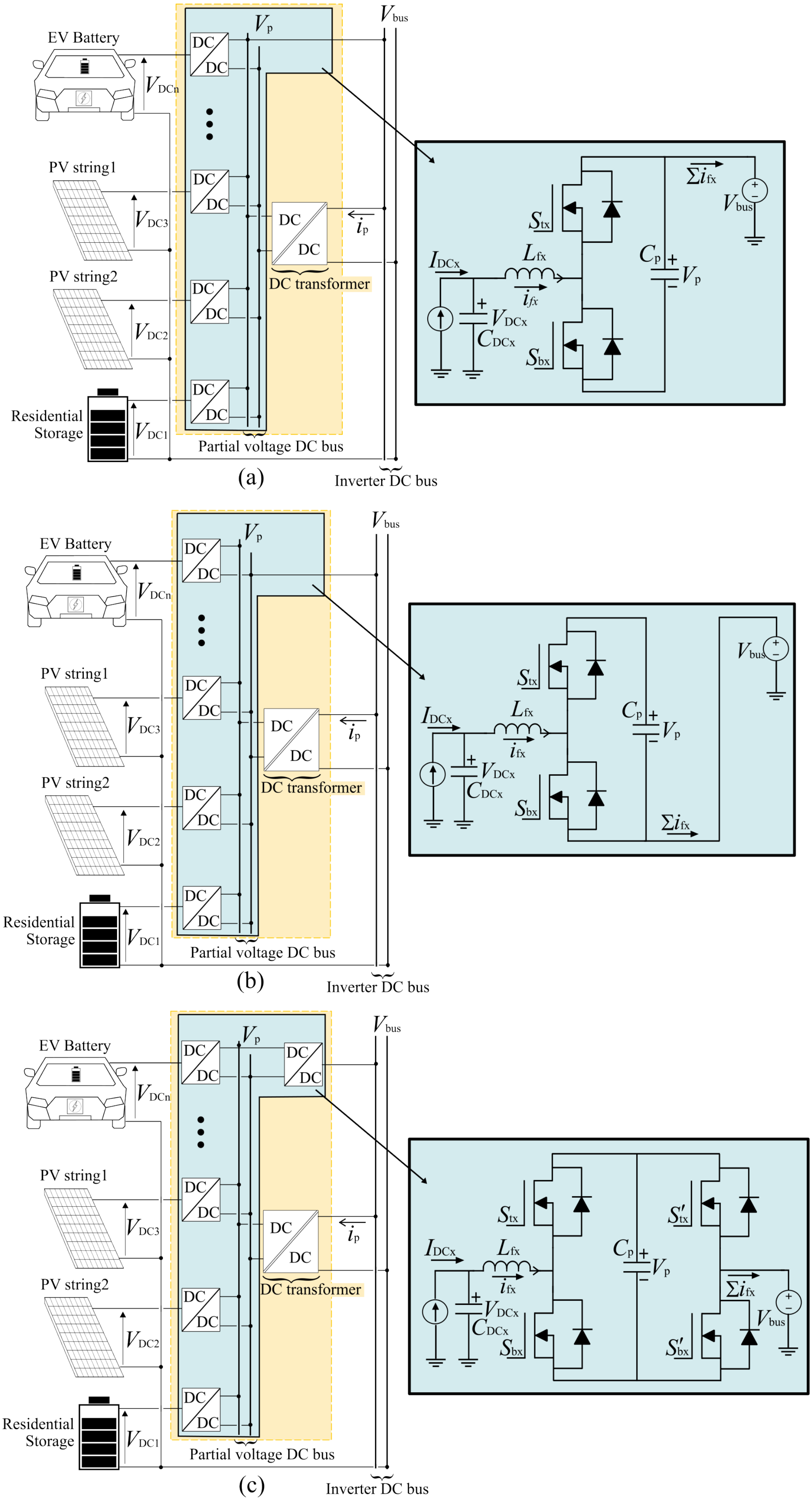
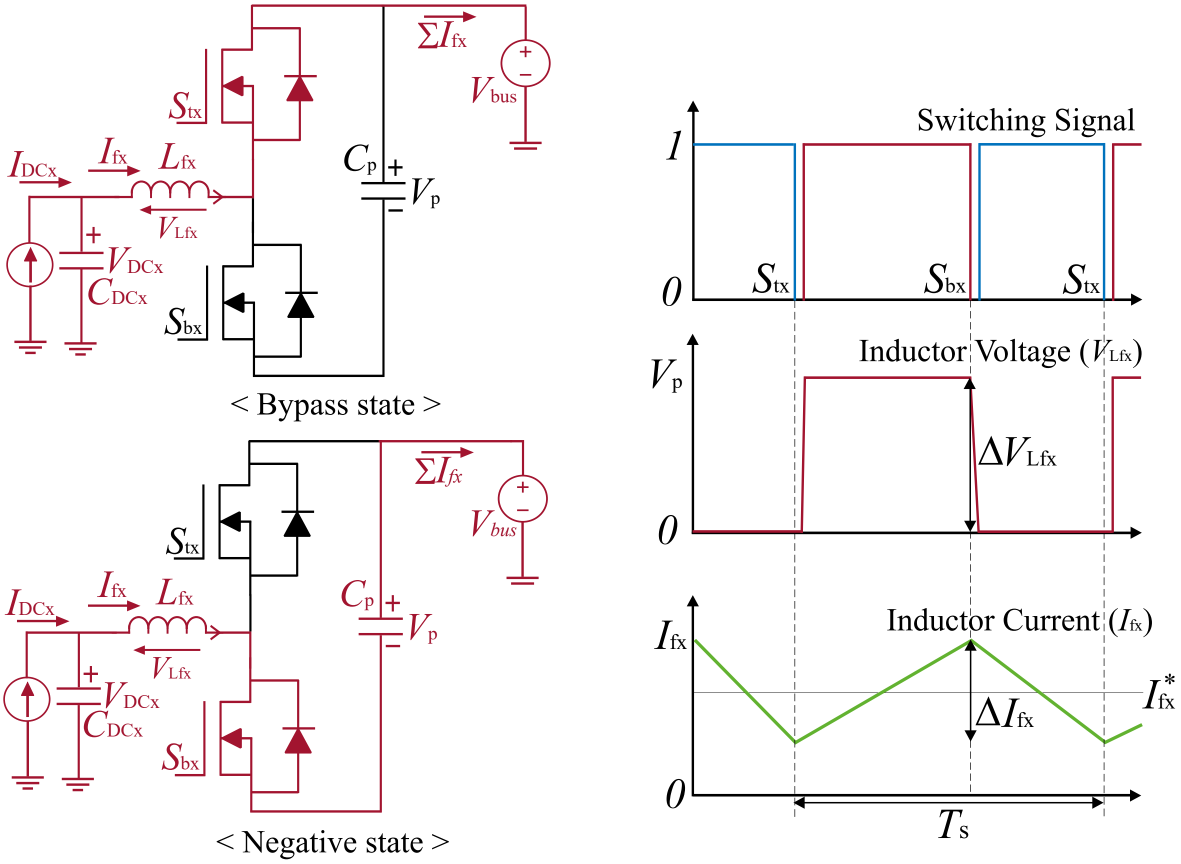


Figure 3.5: PVC topology options: (a) Boost type, (b) Buck type, and (c) Buck-boost type.



(a) (b)

Figure 3.6: Boost type PVC: (a) schematics and (b) switching signal, inductor voltage, and inductor current ripple.

where $D_{\mathrm{x}}|_{\mathrm{x}=1,2,\cdots,\mathrm{n}}$ is the duty cycle of the PVC and f_{s} is the switching frequency of the PVC.

The bus voltage can be formed from V_{DCx} and V_{p}. The relationship can be derived from the average voltage relationship of the PVC as follows:

$$V_{\mathrm{bus}} = V_{\mathrm{DCx}} + D_{\mathrm{x}} V_{\mathrm{p}} \tag{3.12}$$

In the identity equation of (3.12), the sum of V_{DCx} and DV_{p} results in V_{bus}. The duty cycle should be $D \geq 0$. Therefore, the voltage relation $V_{\mathrm{DCx}} \leq V_{\mathrm{bus}}$ is always true. The voltage relation therefore proves that the PVC topology of Fig. 3.6 (a) is optimal for the boost mode applications where $V_{\mathrm{DCx}} \leq V_{\mathrm{bus}}$.

3.2.2 Buck type

The buck type PVC topology option is shown in Fig. 3.5 (b). The buck-type PVC is also constructed by the multiple half bridge (HB) legs of S_{tx} and S_{bx}. The HB legs are connected in parallel to C_{p}. The main difference with boost type PVC is that the negative node of C_{p} is connected to V_{bus}.

The switching states of the buck type PVC are highlighted in Fig. 3.7 (a). The switching of S_{tx} and S_{bx} of the buck type PVC is also complementary. The switching states of the buck type PVC and the inductor voltages are shown in the table. 3.5. When S_{tx} is on, i_{fx} flows through S_{tx} and the positive node of C_{p}. When S_{bx} is on, i_{fx} is bypassed directly to V_{bus} through S_{bx}. The amplitude of the inductor voltage ripple (ΔV_{Lfx}) can be calculated by subtracting V_{Lfx} from the bypassed state ($V_{\mathrm{DCx}} - V_{\mathrm{bus}}$) to the negative state ($V_{\mathrm{DCx}} + V_{\mathrm{p}} - V_{\mathrm{bus}}$). The result of the calculation of $\Delta V_{\mathrm{Lfx}} = V_{\mathrm{p}}$.

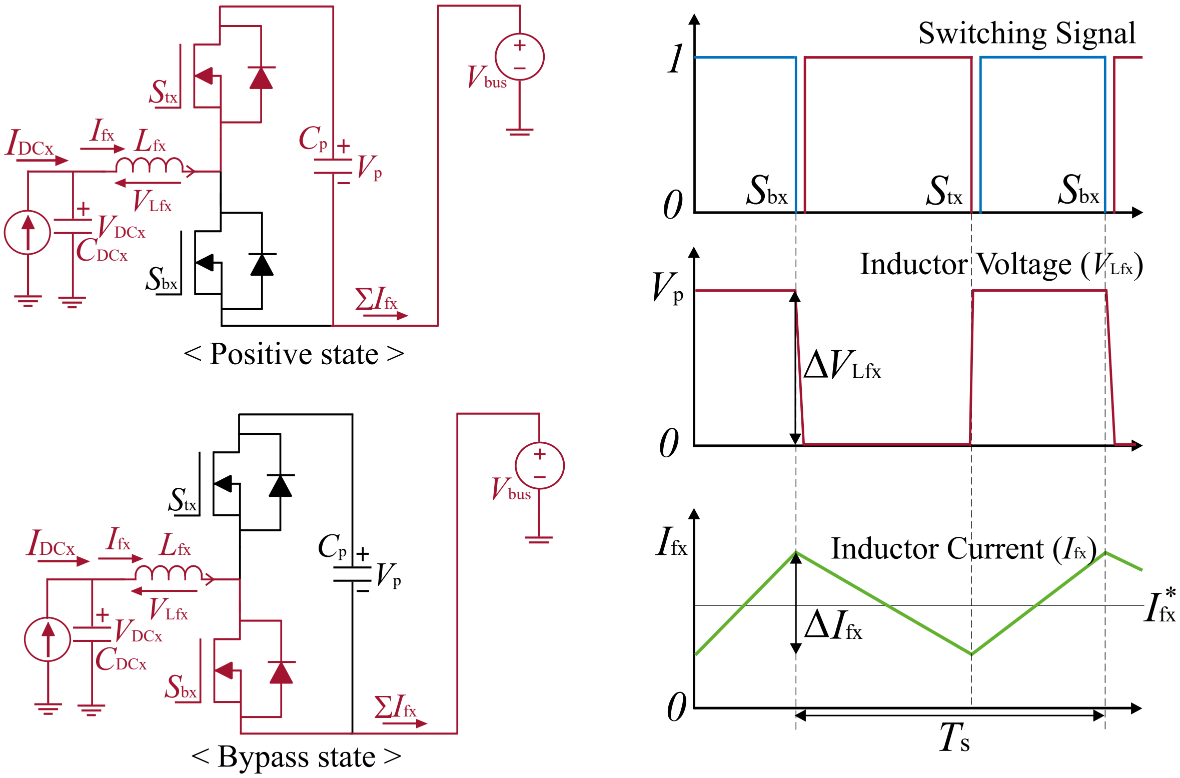
Table 3.5: Buck type PVC switching states

S_{tx}	S_{bx}	Inductor Voltage (V_{Lfx})	States
1	0	$V_{\mathrm{DCx}} - V_{\mathrm{p}} - V_{\mathrm{bus}}$	Positive
0	1	$V_{\mathrm{DCx}} - V_{\mathrm{bus}}$	Bypass

The waveform of the switching signal, inductor voltage (V_{Lfx}) and inductor current (i_{f}) is shown in Fig. 3.7 (b). As mentioned in the table. 3.5, the switches S_{tx} and S_{bx} switch in a complementary way. The switching causes a voltage change ($\Delta V_{\mathrm{Lfx}} = V_{\mathrm{p}}$) across the filter inductor (L_{fx}). Therefore, considering the voltage-second balance of the inductor current, the inductor current ripple (Δi_{fx}) can be calculated:

$$\Delta i_{\mathrm{fx}} = \frac{(V_{\mathrm{DCx}} - D_{\mathrm{x}} V_{\mathrm{p}} - V_{\mathrm{bus}})}{L_{\mathrm{fx}} f_{\mathrm{s}}} \tag{3.13}$$

where $D_{\mathrm{x}}|_{\mathrm{x}=1,2,\cdots,\mathrm{n}}$ is the duty cycle of the PVC and f_{s} is the switching frequency of the PVC.



(a) (b)

Figure 3.7: Buck type PVC: (a) schematics and (b) switching signal, inductor voltage, and inductor current ripple.

The bus voltage can be formed by V_{DCx} and V_{p}. The relation can be derived from the average voltage relation of the PVC as follows:

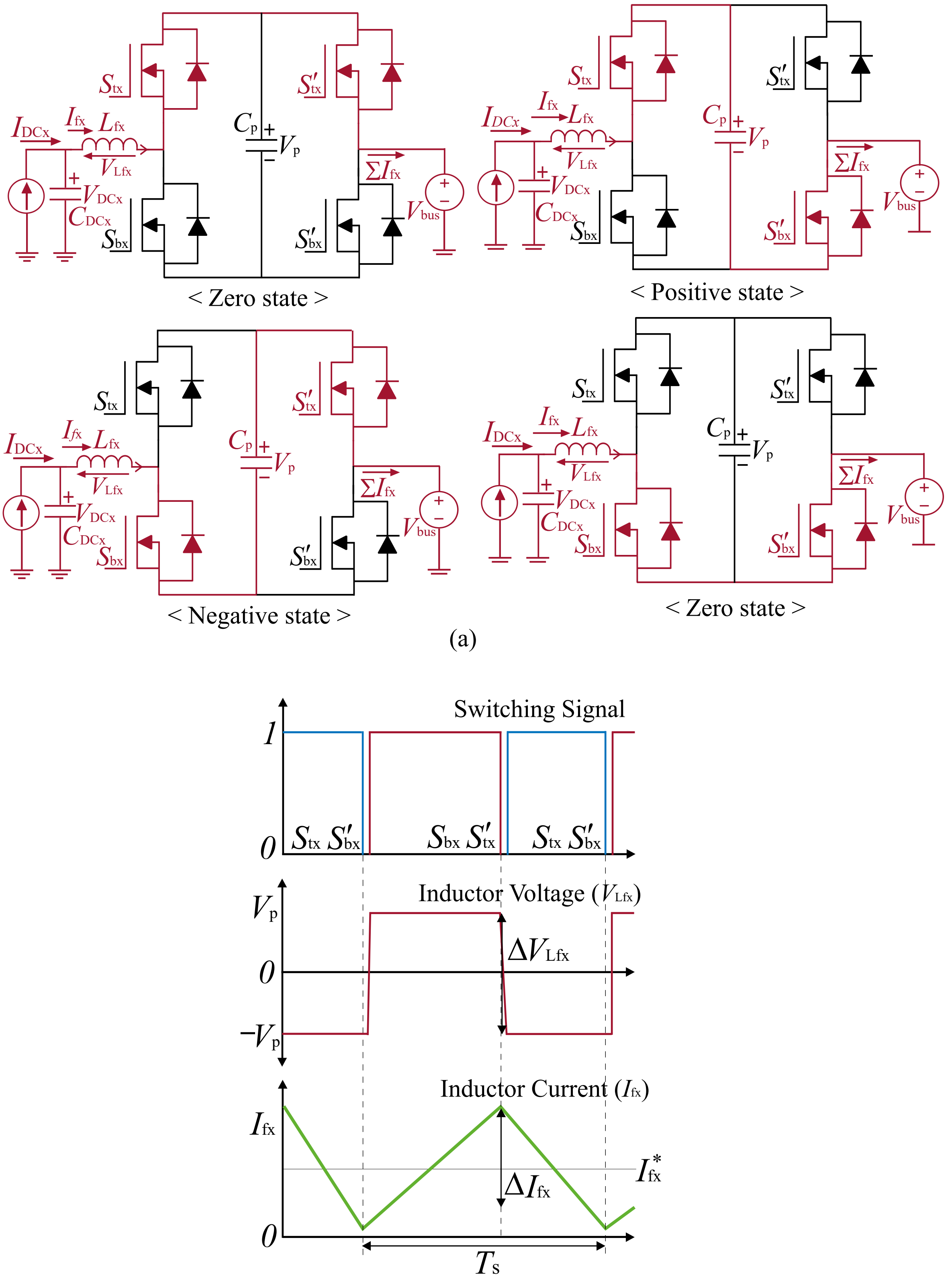
$$V_{\mathrm{bus}} = V_{\mathrm{DCx}} - D_{\mathrm{x}} V_{\mathrm{p}} \tag{3.14}$$

In the identity equation (3.14), the subtraction of $D_{\mathrm{x}} V_{\mathrm{p}}$ from V_{DCx} gives V_{bus}. The duty cycle should be $D \geq 0$. Therefore, the voltage relation $V_{\mathrm{DCx}} \geq V_{\mathrm{bus}}$ is always true. The voltage relation therefore proves that the PVC topology of Fig. 3.7 (b) is optimal for the buck mode applications where $V_{\mathrm{DCx}} \geq V_{\mathrm{bus}}$.

3.2.3 Buck-boost type

The buck-boost type PVC is shown in Fig. 3.5 (c). The buck-boost type PVC consists of a full-bridge (FB) leg with four switches (S_{tx}, S_{bx}, S'_{tx}, and S'_{bx}). The FB legs are connected in parallel to C_{p}.

The switching states of the buck-boost type PVC are highlighted in Fig. 3.8 (a). The switching of S_{tx}, S_{bx}, S'_{tx}, S'_{bx} forces the current i_{fx} into L_{fx}. The buck-boost type PVC can have four different switching states as shown in the figure. When S_{tx} and S'_{tx} are on, i_{fx} can be bypassed directly to V_{bus}. If S_{tx} and S'_{bx} are on, i_{fx} flows through the positive node of C_{p}. If S_{bx}, S'_{tx} are on, i_{fx} flows through the negative node of C_{p}. If S_{bx}, S'_{bx} are on, i_{fx} is directly



(a)

(b)

Figure 3.8: Buck-boost type PVC: (a) schematics and (b) switching signal, inductor voltage, and inductor current ripple.

bypassed to V_{bus}. The switching states of the buck-boost topology option are organized in Table. 3.6. Among the four states, two bypass states are not used because the bypass states do not appear in the DC current control. Therefore, the positive and negative states are used where the switching sets of S_{tx}, S'_{bx} and S_{bx}, S'_{tx}.

The switching states of FB leg, V_{Lf} and i_{f} of FB leg are shown in Fig. 3.8 (b) by following the investigation of HB leg of buck type PVC. During FB leg switching, V_{Lfx} varies from $-V_{\mathrm{p}}$ to V_{p}, which can be written as $\Delta V_{\mathrm{Lfx}} = 2V_{\mathrm{p}}$. Based on the V_{Lfx} variation, Δi_{f} on the FB leg can be expressed as:

$$\Delta i_{\mathrm{fx}} = \frac{(V_{\mathrm{DCx}} - (1-2D_{\mathrm{x}})V_{\mathrm{p}} - V_{\mathrm{bus}})}{L_{\mathrm{fx}} f_{\mathrm{s}}} \tag{3.15}$$

Table 3.6: Buck-boost type PVC switching states

S_{bx}	S_{tx}	S'_{bx}	S'_{tx}	Inductor Voltage (V_{Lfx})	States
0	1	0	1	$V_{\mathrm{DCx}} - V_{\mathrm{bus}}$	Bypass
0	1	1	0	$V_{\mathrm{DCx}} - V_{\mathrm{p}} - V_{\mathrm{bus}}$	Positive
1	0	0	1	$V_{\mathrm{DCx}} + V_{\mathrm{p}} - V_{\mathrm{bus}}$	Negative
1	0	1	0	$V_{\mathrm{DCx}} - V_{\mathrm{bus}}$	Bypass

Using the volt-second balance of ΔV_{Lfx} and Δi_{fx} in Fig. 3.8 (b), the average voltage relation in the buck-boost type PVC can be expressed as follows:

$$V_{\mathrm{bus}} = V_{\mathrm{DCx}} + (1-2D_{\mathrm{x}})V_{\mathrm{p}} \tag{3.16}$$

The identity equation (3.16), shows that V_{p} is subtracted from V_{DCx} if $D_{\mathrm{x}} \geq 0.5$. In this case the voltage relation of FB leg; $V_{\mathrm{DCx}} \geq V_{\mathrm{bus}}$ should be satisfied. On the other hand, if $D_{\mathrm{x}} \leq 0.5$, V_{p} is added to V_{DCx}. The voltage relationship of the FB leg is $V_{\mathrm{DCx}} \leq V_{\mathrm{bus}}$ when $D_{\mathrm{x}} \leq 0.5$. According to the result of D_{x}, FB leg can be applied to both conditions: $V_{\mathrm{DCx}} \geq V_{\mathrm{bus}}$ and $V_{\mathrm{DCx}} \leq V_{\mathrm{bus}}$ are satisfied. This implies that FB leg can be applied to both cases of boost mode and buck mode solutions.

3.2.4 Selection of optimal PVC topology options

The loss analysis of the possible PVC topology options should be investigated to compare the loss benefits of each topology option. There are two main losses on the switches: i) conduction losses and ii) switching losses. In this study, the MOSFETs are adapted for the switching devices. Therefore, the conduction losses P_{con} of the MOSFET can be written as

$$P_{con} = R_{ds,on} I_d^2 \tag{3.17}$$

where $R_{ds,on}$ is on state drain-source resistance of the MOSFET and I_d is the RMS current on MOSFET.

Equation (3.17) shows that P_{con} can be derived by calculating the power dissipation at $R_{\mathrm{ds_{on}}}$ of the MOSFET. The $R_{\mathrm{ds_{on}}}$ information can be found in the MOSFET datasheet. Furthermore, I_{d} can also be calculated based on the target nominal current I_{DCx}.

To calculate the switching losses P_{sw}, the principle of P_{sw} should be analyzed. Fig. 3.9 shows the equivalent circuit of the simplified MOSFET model. In the model the effect of $R_{\mathrm{ds_{on}}}$ on P_{con} is neglected. As shown in the MOSFET model, the gate driver output voltage V_{dr} is applied to the gate. The MOSFET has parasitic capacitors: gate-source capacitor (C_{gs}), gate-drain capacitor (C_{gd}) and drain-source capacitor (C_{ds}). The gate capacitors C_{gs}, C_{gd} are slowly charged by the gate resistor R_{g}. The drain voltage potential is V_{dd} and the current i_{d} flows into the MOSFET when the switch is turned on. P_{sw} is generated by the interaction of C_{gs}, C_{gd}, C_{ds}, and the change in V_{dd} and i_{d} during the turn-on/turn-off period. The detailed turn-on/turn-off sequence of the MOSFET is shown in Fig. 3.10.

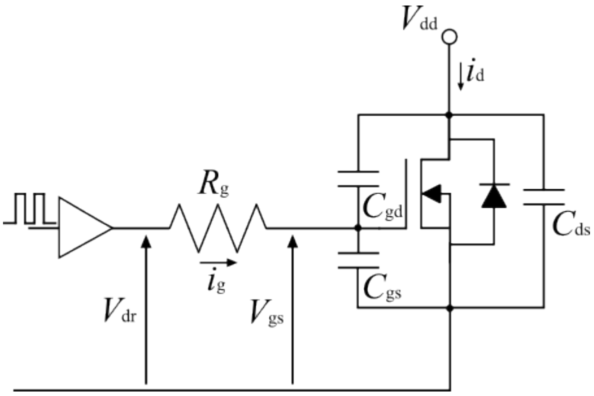


Figure 3.9: Nodes of the MOSFET and its driving circuit.

The waveform of the turn-on/turn-off period of the MOSFET is shown in Fig. 3.10 (a). The green line represents V_{gs}, the red line represents i_{d} and the blue line represents V_{ds}. Firstly, the turn-on sequence of the MOSFET can be analyzed using the V_{gs}, i_{d} and V_{ds} waveforms of the MOSFET. When V_{dr} is applied by the gate driver, the gate current i_{g} begins to charge C_{gd}. When V_{gs} reaches $V_{\mathrm{g(th)}}$, the current through the MOSFET i_{d} starts to increase. When V_{gs} reaches $V_{\mathrm{g(plt)}}$, the MOSFET is fully turned on. The time between V_{gs} and the sweep from $V_{\mathrm{g(th)}}$ to $V_{\mathrm{g(plt)}}$ is defined as the rise time t_{r}. The MOSFET data sheets provide the rise time t_{r}. After the MOSFET is fully turned on, i_{d} reaches its nominal value with the generation of a reverse recovery current. The V_{ds} is also discharged by interaction with i_{g}. The relationship between the change in V_{ds} and i_{g} can be expressed as follows:

$$\frac{dV_{\mathrm{ds}}}{dt} = \frac{i_{\mathrm{g}}}{C_{\mathrm{gd}}} \tag{3.18}$$

The discharging time t_{fu} can be deduced by (3.18) with respect to t which can be written as:

$$t_{\mathrm{fu}} = V_{\mathrm{dd}} \frac{C_{\mathrm{gd}}}{i_{\mathrm{g}}} \tag{3.19}$$

i_{g} during t_{fu} can be written as:

$$i_{\mathrm{g}} = \frac{V_{\mathrm{dr}} - V_{\mathrm{g(plt)}}}{R_{\mathrm{g}}} \tag{3.20}$$

Hence, t_{fu} can be calculated with the given values in the MOSFET datasheet as follows:

$$t_{\mathrm{fu}} = (V_{\mathrm{dr}} - V_{\mathrm{g(plt)}}) V_{\mathrm{dd}} \frac{C_{\mathrm{gd}}}{R_{\mathrm{g}}} \tag{3.21}$$

After V_{ds} is fully discharged, i_{g} interacts with V_{gs} and charges V_{gs} to V_{Dr}.

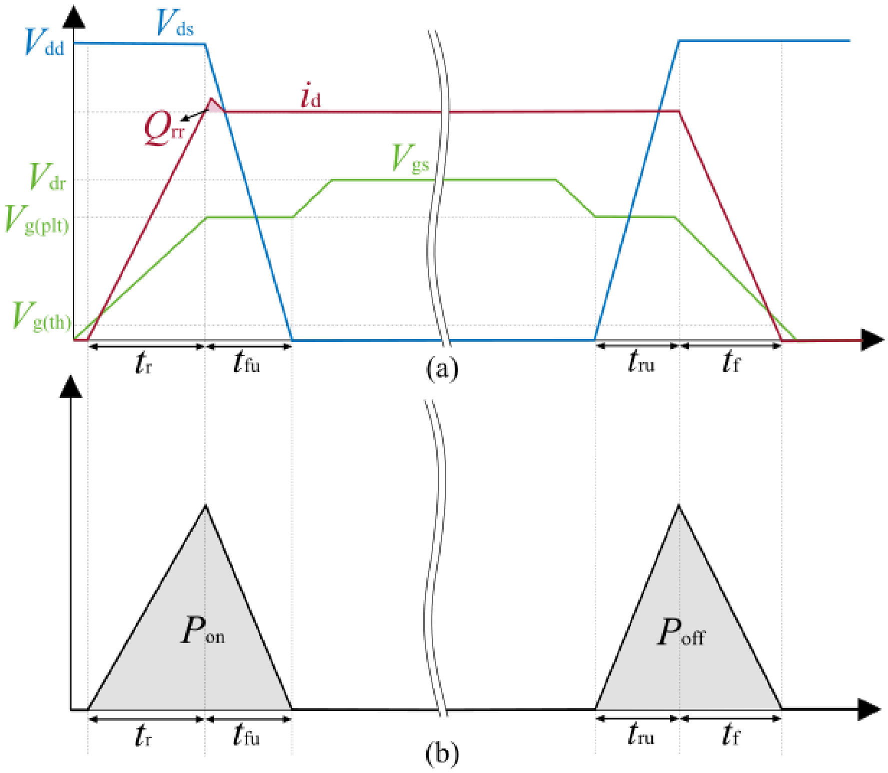


Figure 3.10: Turn off and turn on losses processes during the switching of the MOSFET.

The turn-off period can be analyzed similarly as the turn-on period. First, V_{ds} rising time (t_{ru}) has the same relation as (3.19). However, during the switch turn-off, gate driver does not apply V_{dr}, hence i_{g} can be written as follows:

$$i_{\mathrm{g}} = \frac{-V_{\mathrm{g(plt)}}}{R_{\mathrm{g}}} \tag{3.22}$$

Finally, t_{ru} can be calculated as follows:

$$t_{\mathrm{ru}} = \left| (-V_{\mathrm{g(plt)}}) V_{\mathrm{dd}} \frac{C_{\mathrm{gd}}}{R_{\mathrm{g}}} \right| \tag{3.23}$$

The current falling time t_{f} is also given in the MOSFET datasheet.

In Fig. 3.10 (a) and 3.10 (b), turn-on switching losses P_{on} and turn-off switching losses P_{off} are visualized. P_{on} and P_{off} can be deduced by calculating power during the turn-on and turn-off sequences. First, P_{on} can be calculated as:

$$P_{\mathrm{on}} = \int_0^{t_{\mathrm{r}}+t_{\mathrm{fu}}} v_{\mathrm{ds}}(t) i_{\mathrm{d(t)}}\, dt = 0.5 V_{\mathrm{dd}} I_{\mathrm{d_{on}}} (t_{\mathrm{r}} + t_{\mathrm{fu}}) \tag{3.24}$$

where $I_{\mathrm{d_{on}}}$ is RMS current of i_{d} at turn-on.

By considering the reverse recovery current, (3.24) can be written as:

$$P_{\mathrm{on}} = 0.5 V_{\mathrm{dd}} I_{\mathrm{d_{on}}} (t_{\mathrm{r}} + t_{\mathrm{fu}}) + Q_{\mathrm{rr}} V_{\mathrm{dd}} \tag{3.25}$$

Similarly, P_{off} can be calculated as follows:

$$P_{\mathrm{on}} = \int_0^{t_{\mathrm{ru}}+t_{\mathrm{f}}} v_{\mathrm{ds}}(t) i_{\mathrm{d(t)}}\, dt = 0.5 V_{\mathrm{dd}} I_{\mathrm{d_{off}}} (t_{\mathrm{ru}} + t_{\mathrm{f}}) \tag{3.26}$$

where $I_{\mathrm{d_{off}}}$ is RMS current of i_{d} at turn-off.

Finally, total switching losses can be calculated by adding P_{on} and P_{off} as follows:

$$P_{\mathrm{sw}} = P_{\mathrm{on}} + P_{\mathrm{off}} = 0.5 V_{\mathrm{dd}} (I_{\mathrm{d_{on}}} (t_{\mathrm{r}} + t_{\mathrm{fu}}) + I_{\mathrm{d_{off}}} (t_{\mathrm{ru}} + t_{\mathrm{f}})) + Q_{\mathrm{rr}} V_{\mathrm{dd}} \tag{3.27}$$

Based on (3.17) and (3.27), the losses of the PVC topology options can be calculated. The losses of the buck-boost type PVC are twice as high as those of the boost and buck type PVC topology options. The RMS inductor current of all topology options is the same as I_{fx}. Furthermore, the voltages at the switching devices are the same in V_{p}. Therefore, the unit losses on the single MOSFET are the same for all topology options. However, the number of MOSFETs in the buck-boost PVC is double that of the boost and buck PVCs. Therefore, the losses of the FB leg based buck-boost type PVC have twice higher losses compared to the HB leg based boost type and buck type PVCs.

In summary, there are three options for the PVC topology: i) Boost type ii) Buck type and iii) Buck-boost type. The overall comparison of these three topology options is described in Table. 3.7. The nominal voltages of V_{DCx} are lower than V_{bus}. Hence, buck type topology is not optimal topology to apply to the smart home applications. By using buck-boost type PVC, the flexible V_{DCx} can be applied to the input side. However, the losses of the boost type PVCs are twice higher than the boost type and buck type PVCs. In addition, by selecting the boost type PVC: inductor, the ripple ΔV_{Lf} can be smaller compared to the buck-boost type. It is possible to have the same Δi_{f} by using lower inductance L_{fx}. The number of switching devices and the semiconductor losses are twice lower than the buck-boost type topology. Eventually, the PVC can have reduced losses and cost by using the boost type topology option. Therefore, the boost type PVC is selected as the optimal solution for the smart home applications.

Table 3.7: Comparison table of PVC topology options

Topology	ΔV_{Lf}	Number of Switches	Semiconductor Loss p.u.	Application
Buck-boost type	$2V_{\mathrm{p}}$	4	1	Charging & PV
Boost type	V_{p}	2	0.5	PV
Buck type	V_{p}	2	0.5	Charging

3.3 DC transformer topology selection

In the multi-port PPC architecture, the DC transformer is one of the key stages that maintains the partial voltage V_{p} at C_{p}. Since the stiff V_{p} can be maintained by the DC transformer, the partial voltage processing on the PVC is allowed. Moreover, the use of DC transformer stage also let the energy conservation of the proposed multi-port PPC converter by the partial power flow as written in (3.3). In the smart home applications, ΣP_{DCx} can be fluctuated by the current and voltage variation of the DC inputs. Therefore, the power difference between the DC inputs and the inverter side DC bus can be written as follows:

$$\begin{aligned} \Sigma P_{\mathrm{DCx}} - P_{\mathrm{bus}} > 0, \quad & \text{if } \Sigma P_{\mathrm{DCx}} > P_{\mathrm{bus}} \\ \Sigma P_{\mathrm{DCx}} - P_{\mathrm{bus}} < 0 \quad & \text{if } \Sigma P_{\mathrm{DCx}} < P_{\mathrm{bus}} \end{aligned} \tag{3.28}$$

Based on (3.3), $\Sigma P_{\mathrm{DCx}} - P_{\mathrm{bus}} > 0$ represents the partial power flow on the DC transformer (P_{DCT}). Hence, the power flow condition of DC transformer can be written as follows:

$$\begin{aligned} P_{\mathrm{DCT}} < 0, \quad & \text{if } \Sigma P_{\mathrm{DCx}} > P_{\mathrm{bus}} \\ P_{\mathrm{DCT}} > 0 \quad & \text{if } \Sigma P_{\mathrm{DCx}} < P_{\mathrm{bus}} \end{aligned} \tag{3.29}$$

The power flow on the DC transformer is changed by the power comparison between ΣP_{DCx} and P_{bus}. If $\Sigma P_{\mathrm{DCx}} > P_{\mathrm{bus}}$, the direction of the power flow on the DC transformer is from ΣV_{DCx} to V_{bus}. On the other hand, if $\Sigma P_{\mathrm{DCx}} < P_{\mathrm{bus}}$, the power flow direction on the DC transformer is from V_{bus} to ΣV_{DCx}. In addition, another key function of the DC transformer is to separate the grounds between V_{p} and V_{bus} through the galvanic isolation of the transformer.

Therefore, for the possible topology options of the DC transformer, the bidirectional isolation converters should be considered. The two most common isolated converters are i) Dual Active Bridge (DAB) converters [90–99] and ii) Dual Bridge Series Resonant Converter (DBSRC) solutions [100–103]. The evaluation of the advantages between DAB and DBSRC converters is required in order to select the optimal isolated converter topology. Furthermore, further optimization of the selected isolated converter is required to have optimal losses for the DC transformer.

3.3.1 DC transformer topology selection: DAB vs DBSRC

Dual active bridge (DAB) converter

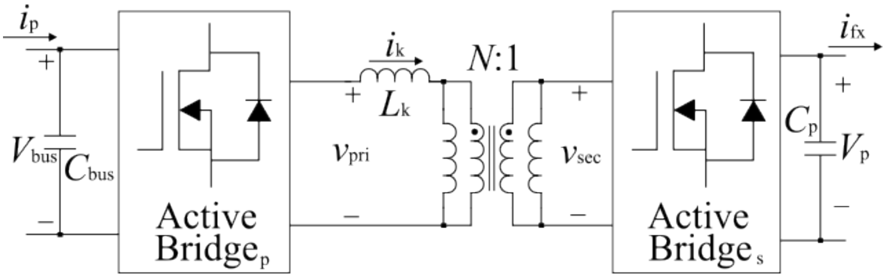


Figure 3.11: Schematics of DAB converter.

The schematic of the DAB converter is shown in Fig. 3.11. The DAB converter has an active bridge on the V_{bus} side and an active bridge on the V_p side. To drive the DAB converter, a constant 50% duty cycle is applied to each primary and secondary active bridge. The power of the DAB converter is transferred by the phase shift between the primary and secondary active bridges.

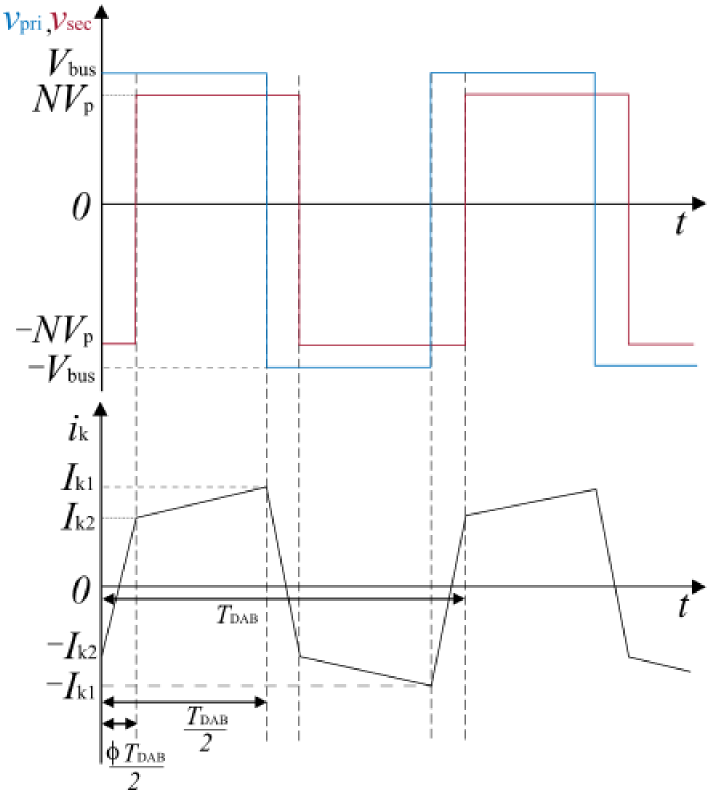


Figure 3.12: Current and voltage waveform of DAB converter.

The current and voltage waveform of the DAB converter is depicted in Fig. 3.12. Based on the depicted waveform, the voltage on L_k can be expressed as follows:

$$V_{\mathrm{k}} = V_{\mathrm{bus}} + NV_{\mathrm{p}} = \frac{2L_{\mathrm{k}}(I_{\mathrm{k1}} + I_{\mathrm{k2}})}{\phi T_{\mathrm{DAB}}} \quad \text{when} \quad 0 \leq t \leq \frac{\phi T_{\mathrm{DAB}}}{2} \tag{3.30}$$

$$V_{\mathrm{k}} = V_{\mathrm{bus}} - NV_{\mathrm{p}} = \frac{2L_{\mathrm{k}}(I_{\mathrm{k1}} - I_{\mathrm{k2}})}{T_{\mathrm{DAB}} - \phi T_{\mathrm{DAB}}} \quad \text{when} \quad \frac{\phi T_{\mathrm{DAB}}}{2} \leq t \leq \frac{T_{\mathrm{DAB}}}{2} \tag{3.31}$$

where V_{k} is the voltage on L_{k}, T_{DAB} is the switching period of DAB converter, and ϕ is the phase shift of the DAB converter.

Considering the continuity of i_{k}, I_{k1} and I_{k2} can be calculated as follows:

$$I_{\mathrm{k1}} = \frac{T_{\mathrm{DAB}}(2N\phi V_{\mathrm{p}} + V_{\mathrm{bus}} - NV_{\mathrm{p}})}{4L_{\mathrm{k}}} \tag{3.32}$$

$$I_{\mathrm{k2}} = \frac{T_{\mathrm{DAB}}(2N\phi V_{\mathrm{bus}} - V_{\mathrm{bus}} + NV_{\mathrm{p}})}{4L_{\mathrm{k}}} \tag{3.33}$$

Finally, NI_{p} can be calculated based on (3.32) and (3.33) as follows:

$$NI_{\mathrm{p}} = \frac{NV_{\mathrm{bus}}T_{\mathrm{DAB}}\phi(1-\phi)}{2L_{\mathrm{k}}} \tag{3.34}$$

The limit of NI_{p} can be decided by considering the maximum input-output power transfer of multi-port PPC of (3.3) and the voltage relation of the DAB converter as follows:

$$xV_{\mathrm{DCx}}I_{\mathrm{fx}} = V_{\mathrm{bus}}(xI_{\mathrm{fx}} - I_{\mathrm{p}}) = V_{\mathrm{bus}}xI_{\mathrm{fx}} - NV_{\mathrm{p}}I_{\mathrm{p}} \tag{3.35}$$

where x is the number of inputs, I_{fx} is the RMS inductor current (i_{fx}), and N is the transformer ratio.

Equation (3.35) can be reorganized as:

$$x(V_{\mathrm{bus}} - V_{\mathrm{DCx}})I_{\mathrm{fx}} = xV_{\mathrm{p}}I_{\mathrm{fx}} = NV_{\mathrm{p}}I_{\mathrm{p}} \tag{3.36}$$

Finally, the input-output current relationship between V_{bus} side and V_p side can be expressed as follows:

$$I_{\mathrm{fx}} = \frac{NI_{\mathrm{p}}}{x} \tag{3.37}$$

Based on (3.37), output current of DAB converter (N/xI_{p}) is the same as RMS current of the PVC converter stage (I_{fx}). Therefore, the relation of I_{fx} and I_{k1} can be written as follows:

$$I_{\mathrm{fx_{peak}}} = I_{\mathrm{k1}} \tag{3.38}$$

where $I_{\mathrm{fx_{peak}}}$ is the peak value of i_{fx} that considers the switching ripple.

The switches of low voltage side secondary active bridge should be selected by considering the peak inductor current I_{k1}. Therefore, putting (3.38) in (3.32), I_{k1} can be calculated. Based on Table. 3.2, the nominal current on the PVC is 11A. Hence, considering the 40% switching ripple current, I_{k1} can be decided as 16A.

The output power of the DAB converter can be calculated from (3.34) as follows:

$$P_{\mathrm{DAB}} = \frac{V_{\mathrm{bus}} V_{\mathrm{p}} \phi (1-\phi) T_{\mathrm{DAB}}}{2 L_{\mathrm{k}} n} \tag{3.39}$$

In order to determine the phase shift angle ϕ, (3.39) can be reorganized with respect to ϕ as follows:

$$\Phi^2 - \Phi + \frac{2 L_{\mathrm{k}} P_{\mathrm{DAB}}}{V_{\mathrm{bus}} V_{\mathrm{p}} T_{\mathrm{DAB}}} = 0 \tag{3.40}$$

where Φ is the nominal phase shift angle.

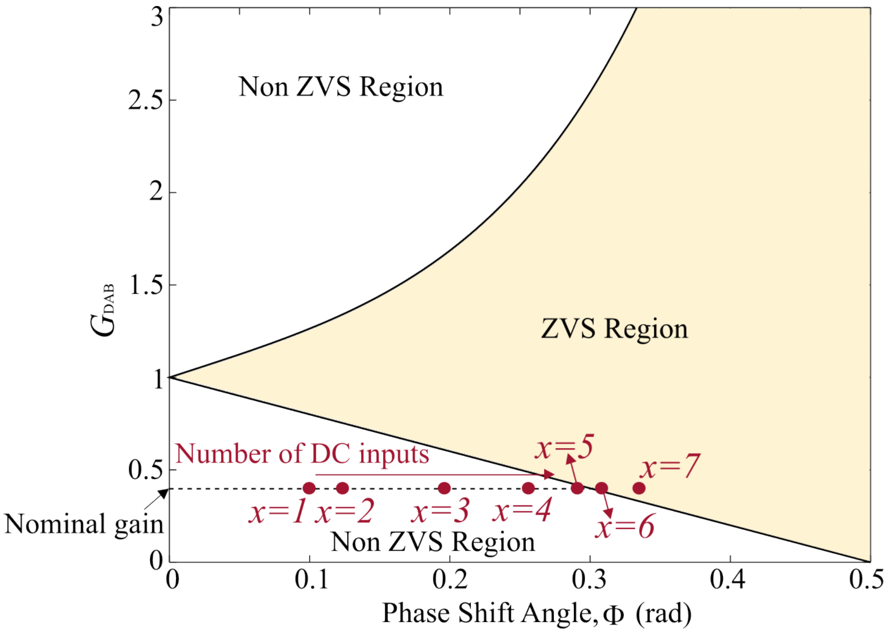


Figure 3.13: ZVS condition of DAB converter and the nominal operating point of the DAB converter at the condition in Table. 3.2.

Putting the parameters in Table. 3.2 to (3.40), the nominal phase shift angle at different numbers of DC inputs can be calculated. As discussed before, the major target of multi-port PPC is to minimize the losses on the semiconductor devices. Hence, the zero voltage switching (ZVS) should be achieved on the DAB converter stage in overall conditions. The ZVS condition of DAB converter [95–99] can be written as follows:

$$\begin{aligned} \Phi &\geq (G_{\mathrm{DAB}}-1)/(2G_{\mathrm{DAB}}), && \text{if } G_{\mathrm{DAB}} \geq 0 \\ \Phi &\geq (1-G_{\mathrm{DAB}})/2, && \text{if } G_{\mathrm{DAB}} \leq 0 \end{aligned} \tag{3.41}$$

In Fig. 3.13 the ZVS condition of the DAB converter is plotted based on (3.41). The phase shift angles of the different numbers of DC inputs are calculated and pointed on the ZVS condition plot. The DAB converter based DC transformer of multi-port PPC cannot achieve the ZVS if the number of DC inputs (x) are less than 7 at the target operating conditions in Table. 3.2. In other words, more than 7 numbers of DC inputs are always required to achieve soft switching of the DC-DC converter, which makes the architecture impractical for the smart home applications. Therefore, the DAB converter is not a suitable solution for the DC transformer of the multi-port PPC.

Dual bridge series resonant converter (DBSRC)

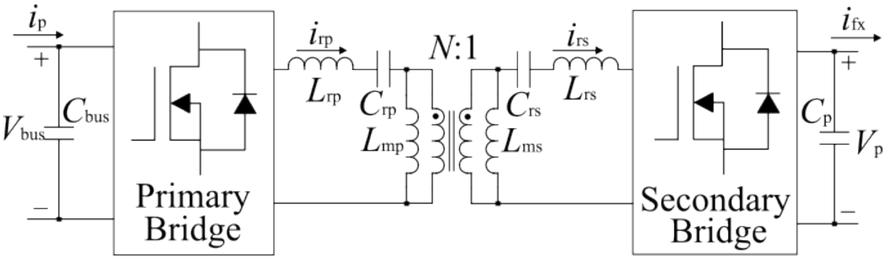


Figure 3.14: Schematics of the dual bridge series resonant converter (DBSRC).

The dual bridge series resonant converter (DBSRC) is depicted in Fig. 3.14. Both on the primary and secondary sides of the DBSRC are comprised with the switching legs. In order to have bidirectional power flow capability, resonant tank are placed both on the primary (L_{rp} and C_{rp}) and the secondary (L_{rs} and C_{rs}) side of the transformer. 50% constant duty cycle is applied to the primary bridge and secondary bridge of the DBSRC. Hence, the average output voltage of the DBSRC can be decided by the transformer turns ratio as follows:

$$V_p = V_{bus}/N \tag{3.42}$$

where N is the transformer turns ratio.

The ZVS of DBSRC always can be achieved when $f_{SRC} > f_r$, where f_{SRC} is the switching frequency of the DBSRC and f_r is the resonant frequency. Hence, there is higher chance to optimize the efficiency of the DC transformer of the multi-port PPC owing to its ZVS capability. Therefore, DBSRC converter is selected for optimal topology for the DC transformer stage.

3.3.2 Optimal topology selection of DBSRC

The DBSRC is selected for the DC transformer topology. The DBSRC has bridges on each primary and secondary sides of the transformer. The primary bridge is connected to V_{bus}. The secondary bridge is connected to V_p. The primary bridge should be designed to handle the nominal voltage of V_{bus} with a 50% voltage margin of the switching voltage overshoot. On the secondary side of the transformer, the applied voltage is 150 V. Therefore, the secondary bridge should be designed to handle the power at 150 V. There are three possible options for the primary and secondary bridge of the DBSRC: i) Neutral Point Clamped (NPC) leg, ii) Full bridge (FB) leg, and iii) Half bridge (HB) leg. By selecting each different topology for the primary bridge and secondary bridge, nine different topology combinations can be made.

The basic operation of each topology option is analyzed to investigate the operation of each DBSRC leg option. The losses of all possible topology combinations are analyzed to select the optimum topology combination with the minimum losses. In addition, the detailed required voltage ratings of each topology option and the required transformer geometry are compared in the table at the end of the section.

Neutral point clamped leg

The schematics of the neutral point clamped (NPC) leg for DBSRC is depicted in Fig. 3.15 (a). The topology can be applied to both of V_{bus} side and V_{p} side of the DBSRC. Therefore, in order to express the general DC voltage, the DC-link voltage is expressed as V_{IN} (also for the analysis of the other topology options). NPC leg is comprised of two top side switches (S_{rt1} and S_{rt2}), two bottom side switches (S_{rb1} and S_{rb2}), top side diodes (D_{rt}), and bottom side diode (D_{rb}). The half of the DC-link voltage ($V_{\mathrm{IN}}/2$) is applied to the two separated DC-link capacitors: $C_{\mathrm{t_{IN}}}$ and $C_{\mathrm{b_{IN}}}$. The resonant tank [C_{r} and L_{r}] is connected between the neutral point of switches (O) and neutral point of the DC-link (O').

The resonant current i_r is forced by the switching of the NPC leg shown in Fig. 3.15 (b). The upper switches [S_{rt1} and S_{rt2}] and the lower switches [S_{rb1} and S_{rb2}] perform complementary switching with a small dead time. Furthermore, the outer switches [S_{rt1} and S_{rb2}] have a shorter turn-on period than the inner switches [S_{rt2} and S_{rb1}]. The operation of the NPC leg can be divided into six modes, which are shown in Fig. 3.16.

The equivalent circuit of the first sequence between t_0 and t_1 is shown in Fig. 3.16 (a). S_{rt1} and S_{rt2} are switched on simultaneously at t_0. In this sequence i_{r} flows through S_{rt1} and S_{rt2}. The sequence $t_0 \sim t_1$ is over when the resonance at t_1 is over and the switch S_{rt1} is turned off.

The second sequence between t_1 and t_2 is shown in Fig. 3.16 (b). In $t_1 \sim t_2$ the magnetizing current i_{m} flows through S_{rt2} and D_{rt}. In this sequence, the voltage between neutral points $v_{\mathrm{oo'}}$ is clamped to 0. Therefore, the voltage change on the transformer can be $V_{\mathrm{IN}}/2$. The sequence ends when S_{rt2} is switched off at t_2.

Next, between t_2 and t_3, the third sequence starts as shown in Fig. 3.16 (c). In $t_2 \sim t_3$ i_{r} flows through the body diodes of S_{rb1} and S_{rb2}. During this time, the voltage between S_{rb1} and S_{rb2} is discharged by i_{r}.

The equivalent circuit of the fourth sequence between t_3 and t_4 is shown in Fig. 3.16 (d). The sequence $t_4 \sim t_5$ starts when the bottom switches S_{rb1} and S_{rb2} are turned on at t_4. The voltages at S_{rb1} and S_{rb2} are discharged from the previous sequence (Fig. 3.16 (c)). Therefore, S_{rb1} and S_{rb2} are turned on by reaching zero voltage switching (ZVS). During this time, i_{r} flows through S_{rb1} and S_{rb2}. This sequence ends when S_{rb2} is switched off at t_5.

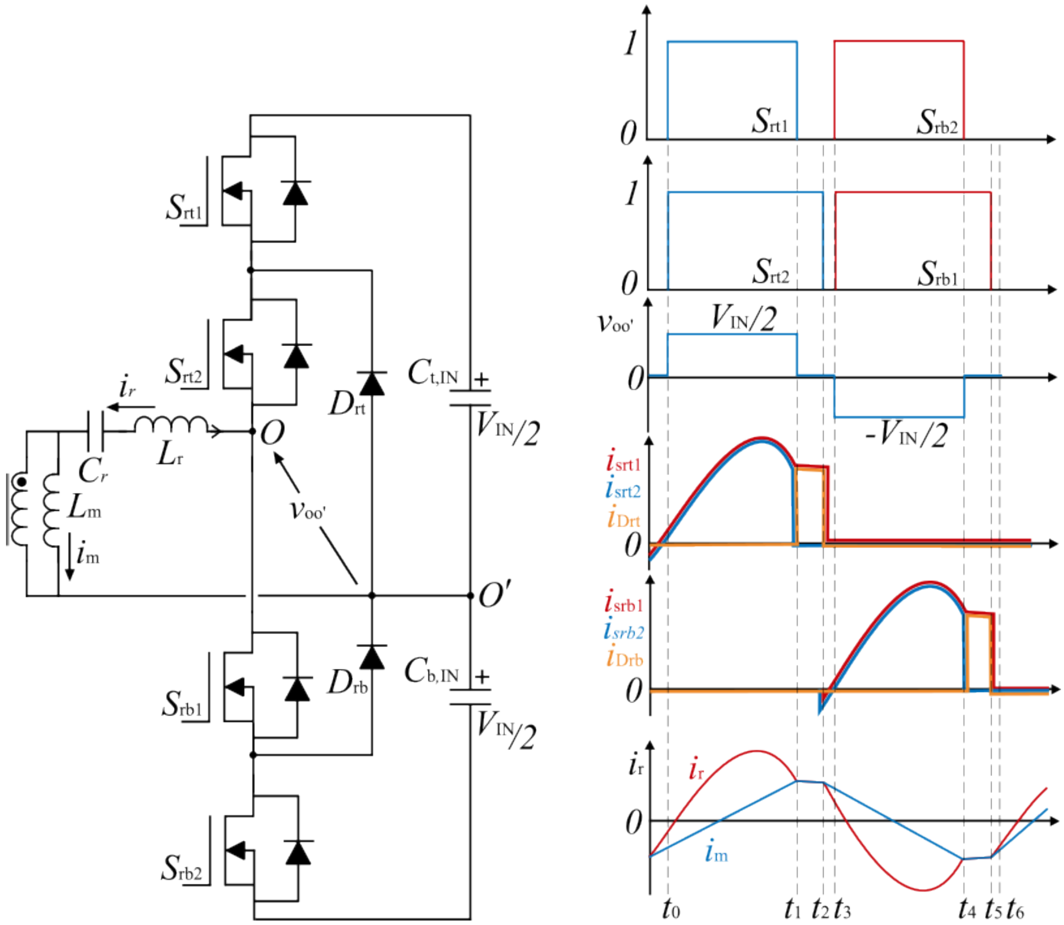
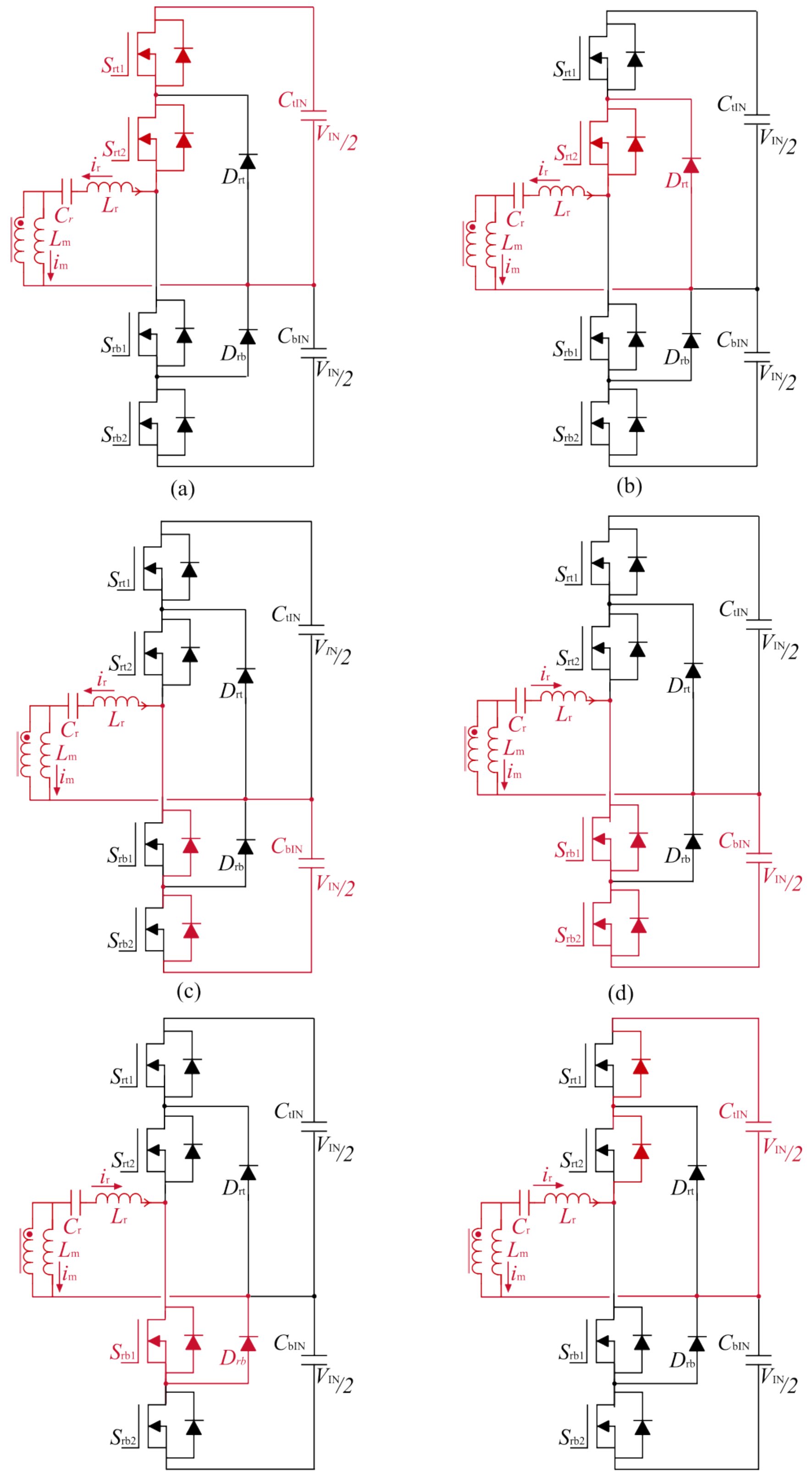


Figure 3.15: Neutral point clamped (NPC) leg (a) Schematics (b) Key waveform: Switching signal, top side device (S_{rt1}, S_{rt2}, D_{rt}) current, bottom side device (S_{rb1}, S_{rb2}, D_{rb}) current, and resonant current i_r.



(a) (b) (c) (d) (e) (f)

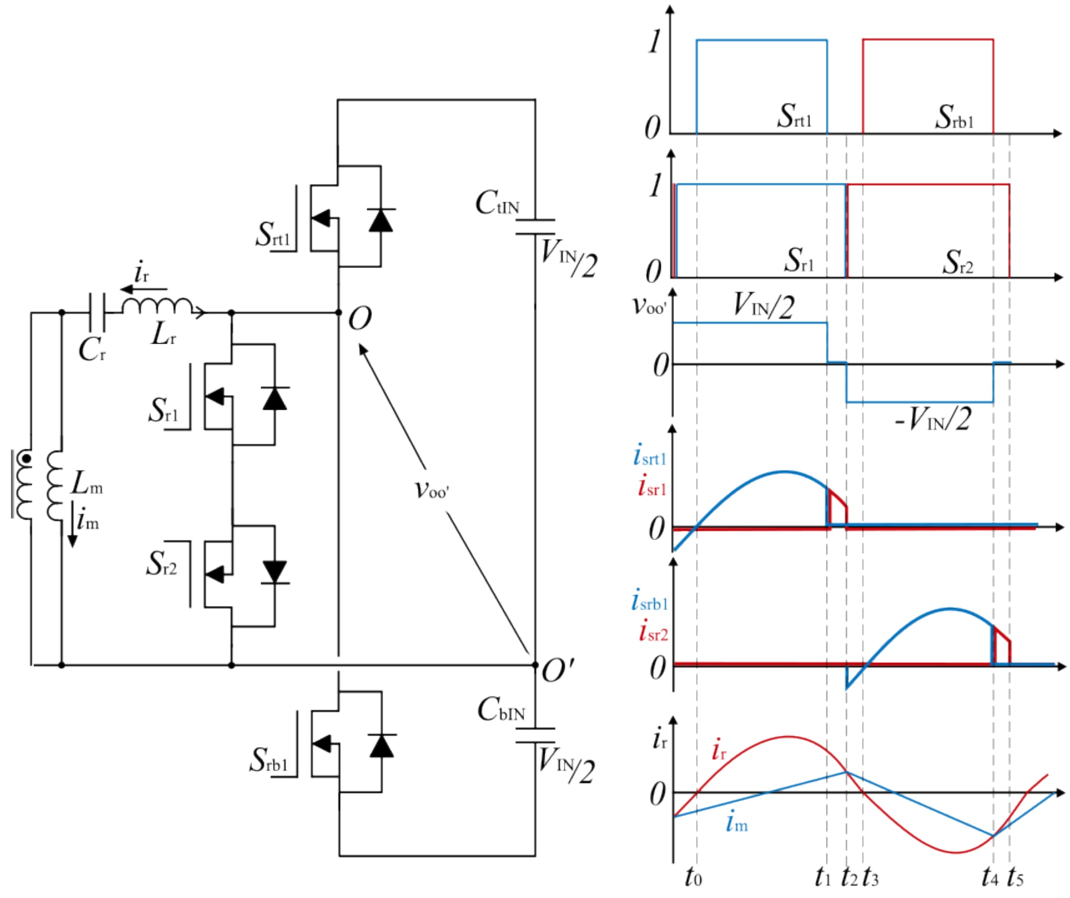
Figure 3.16: NPC leg operation sequence: (a) $t_0 \sim t_1$, (b) $t_1 \sim t_2$, (c) $t_2 \sim t_3$, (d) $t_3 \sim t_4$, (e) $t_4 \sim t_5$, (f) $t_5 \sim t_6$.

Between t_4 and t_5, the resonance is over and S_{rb2} is switched off as shown in Fig. 3.16 (e). Only i_m flows through S_{rb1} and D_{rb}. In addition, the transformer voltage is clamped to 0 that is the same manner as the second sequence that shown in Fig. 3.16 (b).

The equivalent circuit between t_5 and t_6 is shown in Fig. 3.16 (e). In $t_5 \sim t_6$, i_r discharges the voltages at the top switches [S_{rt1} and S_{rt2}]. Thus [S_{rt1} and S_{rt2}] can also achieve the ZVS similar to the sequences in Fig. 3.16 (a)∼(c).

T-type leg

The T-type leg schematics for DBSRC is depicted in Fig. 3.15 (a). The T-type leg is also comprised with four switches: two outer switches [S_{rt1} and S_{rb1}] and two inner switches [S_{r1} and S_{r2}]. The topology is also three level leg, but it does not use diodes unlike NPC leg. On the DC-link, the half of the DC-link voltage ($V_{\text{IN}}/2$) is applied to the top and bottom capacitors [$C_{\text{t}_{\text{IN}}}$ and $C_{\text{b}_{\text{IN}}}$], respectively. The resonant tank C_r, L_r is connected between the neutral point of switches (O) and neutral point of the DC-link (O').



(a) (b)

Figure 3.17: T-type leg (a) Schematics (b) Key waveform: Switching signal, outer switches (S_{rt1} and S_{rb1}) current, inner switches (S_{r1}, S_{r2}) current, and resonant current i_r.

The switching states of T-type leg, current on the outer switches (i_{srt1} and i_{srb1}), current on the inner switches [i_{sr1} and i_{sr2}], and the resonant current (i_r) are depicted in Fig. 3.17. The the switch sets of the outer switches [S_{rt1} and S_{rb1}] and inner switches [S_{r1} and S_{r2}] switch complementary manner. The operation of the T-type leg can be divided into six modes as depicted in Fig. 3.18.

The equivalent circuit of the first sequence between t_0 and t_1 is shown in Fig. 3.18 (a). The top side outer switch S_{rt1} is on at the first sequence. Hence, i_{r} flows through S_{rt1}, resonant tank [L_r and C_r], and $C_{\mathrm{t_{IN}}}$. At t_1, S_{rt1} is turned off and the first sequence ends and the second sequence starts.

When S_{rt1} is turned off, i_{r} on the resonant tank still flows in the same direction through the Sr2 and the body diode of S_{r1} as depicted in Fig. 3.18 (b). When S_{r2} is turned off, the second sequence ends. In this sequence, the voltage between O, O' ($v_{\mathrm{oo'}}$) is clamped to 0. Therefore, the transformer voltage change can be half of the DC link voltage ($V_{\mathrm{IN}}/2$).

The equivalent circuit of the third sequence between t_2 and t_3 is shown in Fig. 3.18 (c). In $t_2 \sim t_3$, i_r still flows in the same direction as the first and second sequences. In this sequence, i_{r} flows through the body diodes of S_{rb1} and discharges the voltage on the S_{rb1}. Hence, S_{rb1} is ready to perform the ZVS.

S_{rb1} is turned on when the half period of resonant is over, and the fourth sequence starts. The equivalent circuit of the fourth sequence between t_3 and t_4 is shown in Fig. 3.18 (d). In this sequence, i_{r} flows opposite direction compared to the prior sequences. The current path is made with the S_{rb1}, $C_{\mathrm{b_{DC}}}$, and the resonant tank.

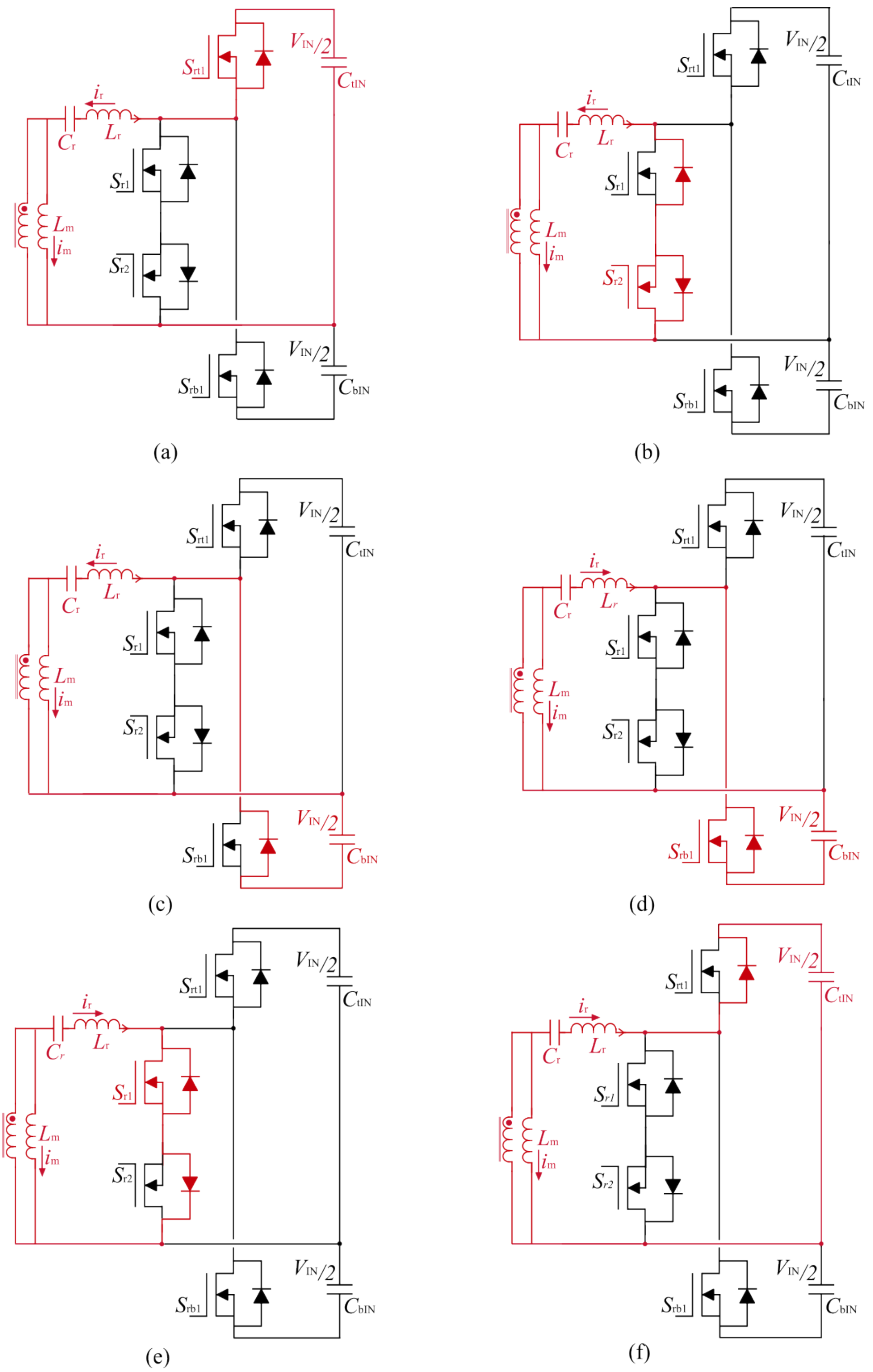
The next sequence which shown in Fig. 3.18 (e) starts when S_{rb1} is switched off at t_4. In this sequence, i_{r} flows through the inner switch S_{r1}. The voltage on the transformer also can be clamped in this sequence. Therefore, the voltage change on the transformer can be $V_{\mathrm{IN}}/2$ as the second sequence.

The last sequence starts when S_{r1} is turned off as depicted in Fig. 3.18 (f). During the time between $t_5 \sim t_6$, i_{r} discharges the voltage on S_{rt1}. Therefore, S_{rt1} can perform the ZVS. The sequence is over when S_{rt1} is on at the end of the resonant. Finally, the whole sequence can be repeated again from the first sequence as shown in Fig. 3.18 (a).

Full bridge leg

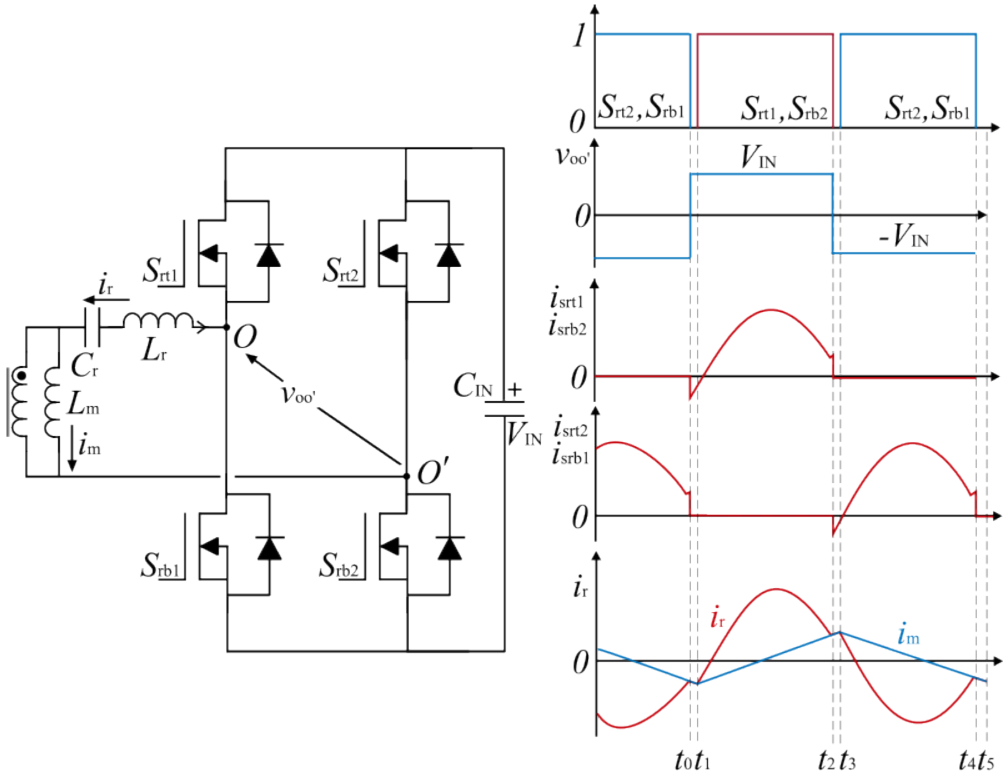
The schematics of the full bridge (FB) leg for DBSRC is depicted in Fig. 3.19 (a). FB leg is comprised with four switches: S_{rt1}, S_{rt2}, S_{rb1}, S_{rb2}. It has the single DC-link capacitor C_{IN} that V_{IN}. The resonant tank [C_{r} and L_{r}] is connected between the first leg [S_{rt1} and S_{rb1}] and second leg [S_{rt2} and S_{rb2}].

In Fig. 3.19(b) the switching states, the voltage between two legs ($v_{\mathrm{oo'}}$), the switching current sets of (i_{srt1} and i_{srb2}) and (i_{srt2} and i_{srb1}) and the resonance current (i_{r}) are shown. The switch sets [S_{rt1} and S_{rb2}] and [S_{rt2} and S_{rb1}] switch together. Furthermore, the upper switches [S_{rt1} and S_{rt2}], and the lower switches [S_{rb1} and S_{rb2}] perform complementary switching with a small dead time. The operation of the FB leg can be divided into four modes, as shown in Fig. 3.20.



(a) (b) (c) (d) (e) (f)

Figure 3.18: T-type leg operation sequence: (a) $t_0 \sim t_1$, (b) $t_1 \sim t_2$, (c) $t_2 \sim t_3$, (d) $t_3 \sim t_4$, (e) $t_4 \sim t_5$, (f) $t_5 \sim t_6$.



(a) (b)

Figure 3.19: Full bridge leg for DC transformer: (a) schematics (b) Key waveform: Switching signal, current of switch sets [S_{rt2} and S_{rb1}], and [S_{rt1} and S_{rb2}], and resonant current i_r.

The equivalent circuit of the first sequence between t_0 and t_1 is depicted in Fig. 3.20 (a). In this stage, the voltage on the switches S_{rt1} and S_{rb2} are discharged by i_r flows on their body diodes. Hence, S_{rt1} and S_{rb2} are ready to be perform the ZVS.

The equivalent circuit of second sequence that between t_1 and t_2 is depicted in Fig. 3.20 (b). The period $t_1 \sim t_2$ begins when S_{rt1} and S_{rb2} are turned on. In t_1 and t_2, i_r path is made by S_{rt1} and S_{rb2} and C_{IN}. In this sequence, the voltage $v_{oo'}$ changes from V_{IN} to $-V_{IN}$. Therefore, the amplitude transformer voltage change is $2V_{IN}$. This period ends when S_{rt1} and S_{rb2} are turned off.

The equivalent circuit between t_2 and t_3 is depicted in Fig. 3.20 (c). In the third sequence, i_r flows through the body diode S_{rt2} and S_{rb1}. The voltage on the S_{rt2} and S_{rb1} are discharged and prepared to be perform the ZVS.

The equivalent circuit between t_3 and t_4 is depicted in Fig. 3.20 (d). The period $t_3 \sim t_4$ begins when S_{rt2} and S_{rb1} are turned on. In this sequence, i_r flows through S_{rt2} and S_{rb1}. After the fourth sequence is over, the cycle starts again from the first sequence that shown in Fig. 3.20 (a).

Half bridge leg

The schematics of the half bridge (HB) leg for DBSRC is depicted in Fig. 3.21 (a). HB leg is comprised of top switch (S_{rt}) and bottom switch (S_{rb}). The DC-link of HB leg is divided

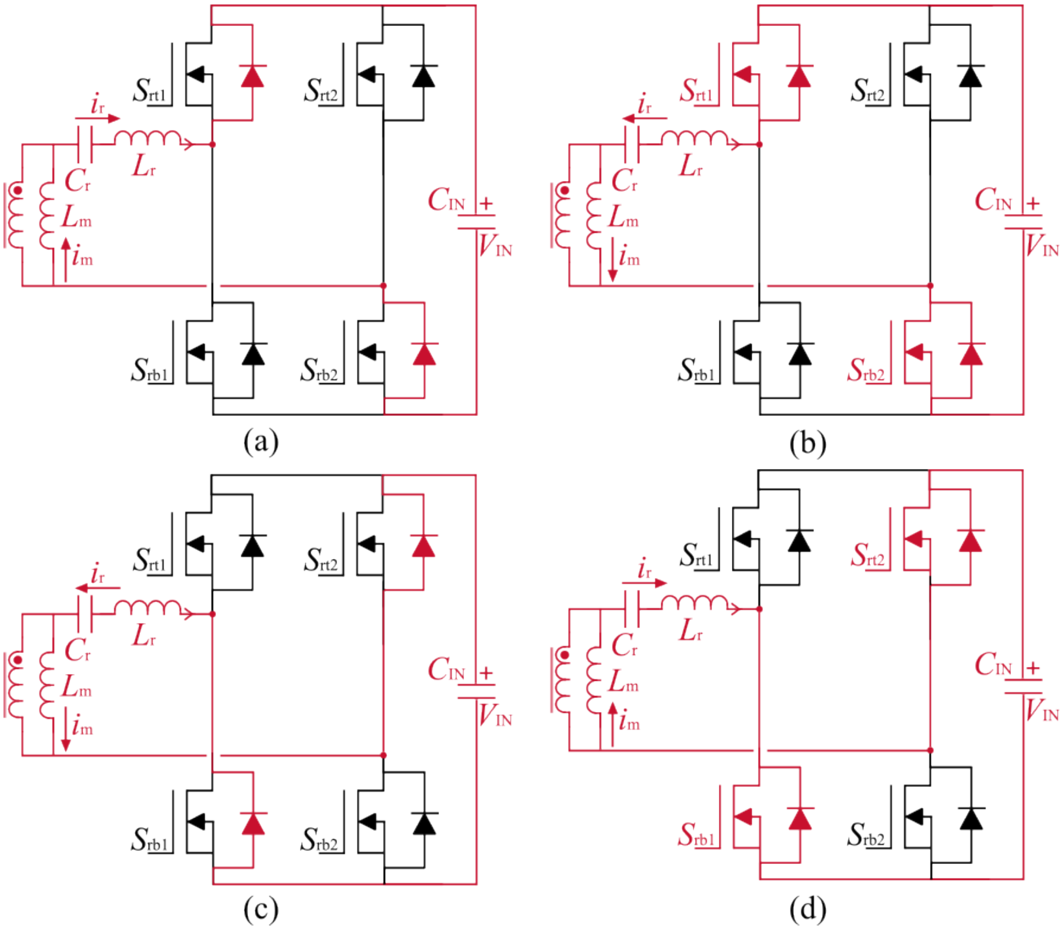
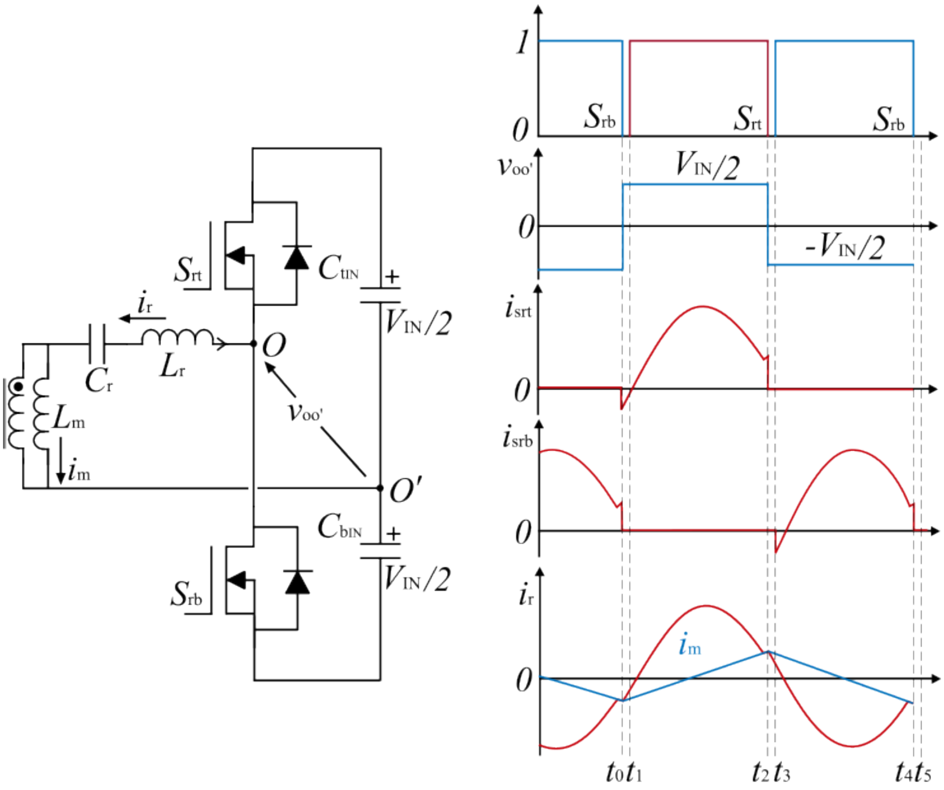


Figure 3.20: Full bridge leg operation sequence: (a) $t_0 \sim t_1$, (b) $t_1 \sim t_2$, (c) $t_2 \sim t_3$, (d) $t_3 \sim t_4$.



(a) (b)

Figure 3.21: Half bridge leg for DC transformer: (a) schematics (b) Key waveform: Switching signal, S_{rt} current, S_{rb} current, and resonant current i_r.

into top side capacitor ($C_{t_{IN}}$) and bottom side capacitor ($C_{b_{IN}}$). The half of the DC voltage ($V_{IN}/2$) is applied to $C_{t_{IN}}$ and $C_{b_{IN}}$. The resonant tank [C_r and L_r] is connected between the mid point of the HB leg O and neutral point of the DC link O'.

In Fig. 3.21 (b), the switching states, voltage between O, O' ($v_{oo'}$), switch currents (i_{srt} and i_{srb}), and resonant current (i_r) are depicted. The top switches S_{rt} and S_{rt} performs complementary switching with a small deadtime. The operation of the HB leg can be divided into four modes which are depicted in Fig. 3.22.

The equivalent circuit between t_0 and t_1 is depicted in Fig. 3.22 (a). In this stage, the voltage on the switches S_{rt} is discharged by i_r flows on their body diodes. Hence, S_{rt} is ready to be perform the ZVS.

The equivalent circuit between t_1 and t_2 is depicted in Fig. 3.22 (b). The period $t_1 \sim t_2$ begins when S_{rt} is turned on. In $t_1 \sim t_2$, i_r path is made by S_{rt1} and top side DC-link capacitor $C_{t_{IN}}$. At this point, $v_{oo'}$ changes from $V_{IN}/2$ to $-V_{IN}/2$. Therefore, the amplitude of the voltage change on transformer is V_{IN}. This sequence ends when S_{rt} is turned off.

The equivalent circuit between t_2 and t_3 is depicted in Fig. 3.22 (c). In this period, i_r flows through the body diode S_{rb}. The voltage on the S_{rb} is discharged and prepared to be perform the ZVS.

The equivalent circuit between t_3 and t_4 is depicted in Fig. 3.22 (d). The period $t_3 \sim t_4$ begins when S_{rb} is turned on. In this sequence, i_r flows through S_{rb} and bottom side capacitor

C_{bIN}.

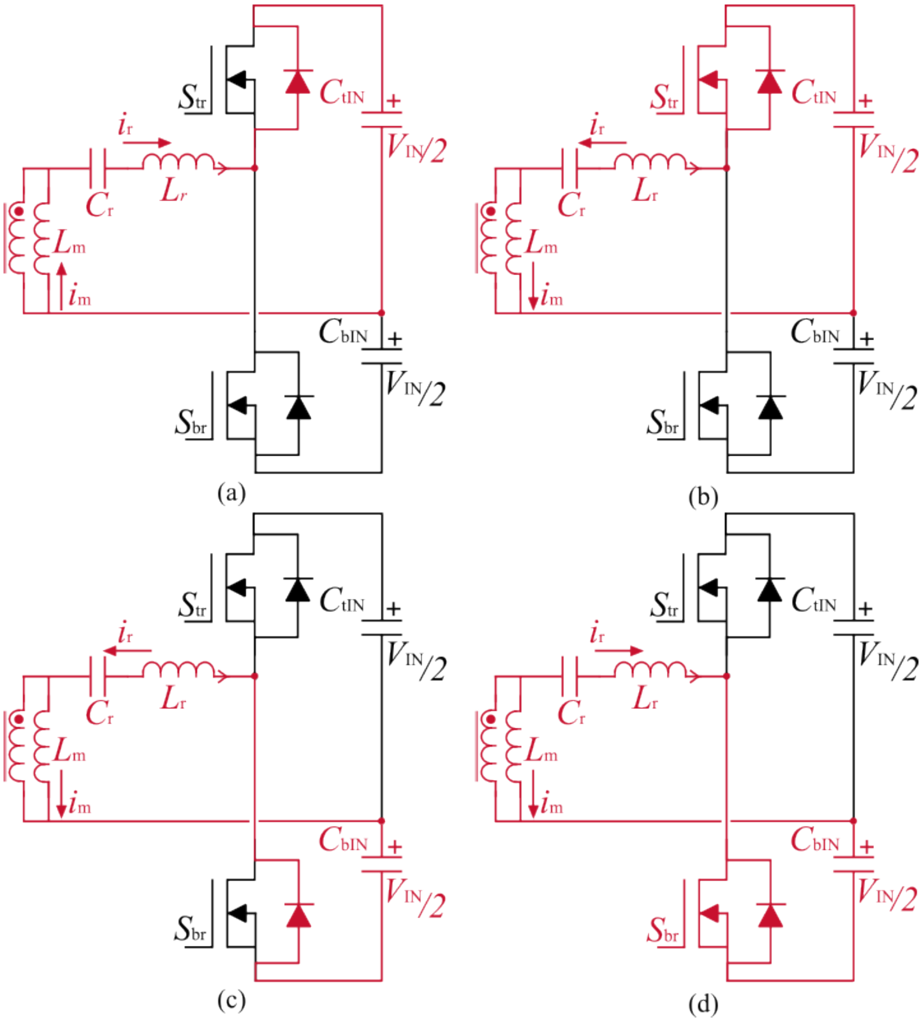


Figure 3.22: Half bridge leg operation sequence: (a) $t_0 \sim t_1$, (b) $t_1 \sim t_2$, (c) $t_2 \sim t_3$, (d) $t_3 \sim t_4$.

Selection of optimal DBSRC topology: Power losses assessment of possible leg combinations

The DBSRC can have sixteen different topology option by the combination of the primary bridge and secondary bridges. In order to investigate the optimal combination of primary and secondary legs, the power losses is analyzed for the all possible leg combinations. Fig. 3.23 shows the conduction and switching losses of the semiconductors of all possible leg combinations of DBSRC. The vertical axis shows the per unit (p.u.) losses of the semiconductors. The lateral axis shows the topology combinations of primary and secondary bridge (Left side of the slash represents V_{bus} side leg and the right side of the slash represent V_{p} side leg). The semiconductor losses are calculated by using the losses analysis principle in (3.17)–(3.27).

The biggest semiconductor losses can be observed when applying FB leg to the primary side as shown in Fig. 3.23. The case shows the highest switching losses. Based on the switching losses equation in (3.27), the switching losses on the switch sets are dependent on the voltage stresses on the switches. When FB leg is applied for the V_{bus} side leg, the voltage stresses on the FB leg switches are full DC-link voltage which is V_{bus}. Furthermore, the switching losses of the FB leg occurs on the two switch sets [S_{rt1} and S_{rb2}] and [S_{rt2} and S_{rb1}]. Therefore, compared to the other topology combinations, the case when FB leg is applied to the V_{bus} side shows the highest losses.

When NPC leg is applied for the V_{bus} side leg, it shows the minimum switching losses. The voltage stresses on the switches of NPC leg is $V_{\text{IN}}/2$. Hence, the switching losses of NPC leg can be lower compared to the other topology options. However, the NPC leg has the highest conduction losses. The current of the NPC leg conducts through the two series switch sets [S_{rt1} and S_{rt2}] and [S_{rb1} and S_{rb2}] which impacts on the increase of conduction losses. Furthermore, NPC leg has the highest semiconductor device counts. Therefore, these reasons can impact on the highest conduction losses compared to the other topology options. Comparing the NPC and T-type legs, the total losses of the T-type leg topology is lower. The switching losses can be higher but the lower conduction losses owing to the lower device counts can impact on the lower total losses compared to NPC leg.

The HB leg applied to the V_{bus} side leg shows the similar losses behavior when the case T-type applied to the V_{bus} side. However, half bridge leg has the advantage in terms of semiconductor device counts compared to the T-type leg.

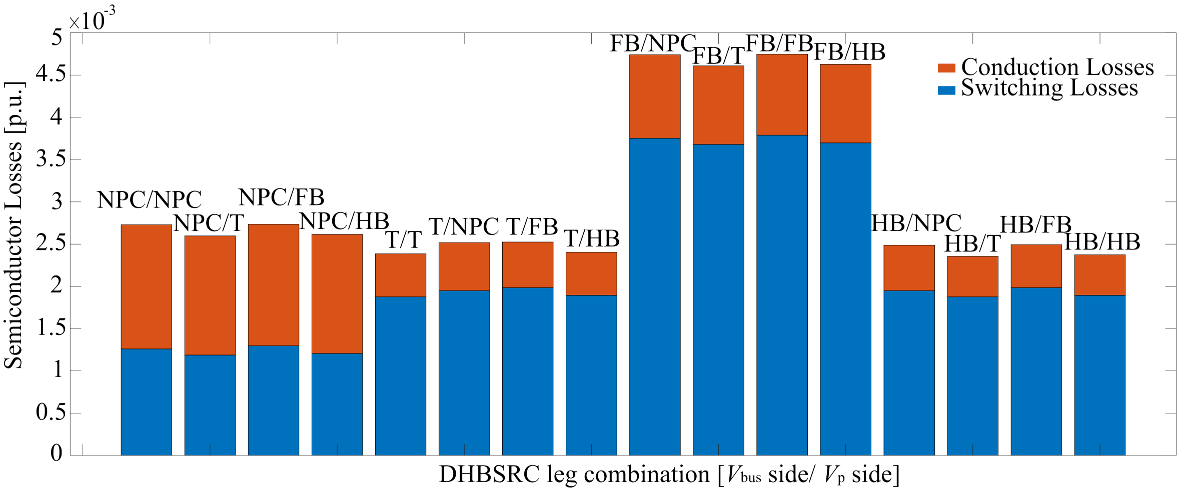


Figure 3.23: Losses comparison of all possible combinations of primary and secondary bridges for DBSRC.

The comprehensive comparison of the all possible leg combination is described in Table. 3.8. The table shows that it is possible to use low voltage devices by applying NPC leg for the DBSRC topology. Furthermore, the transformer voltage step ($\frac{dV}{dt}$) is $V_{\text{bus}}/2$. The number of turns of the transformer is proportional to the RMS voltage on the transformer [104]. Therefore, there are more chances to have less turns of the copper winding when the voltage step dV/dt on the transformers is decreased. Likewise, using T-type leg also has the chances to decrease the copper windings on the transformers. On the other hand, the voltage stresses on the semiconductor devices are twice higher than the NPC leg. However, the lower semiconductor devices can be used and there is more chance to decrease the losses by using T-type leg for the DBSRC topology. Using FB leg for the DBSRC has the lowest advantage owing to the highest voltage change on the transformer and the highest losses. However, by using FB leg on the V_p side, it is possible to have almost 1:1 turns ratio by using the full wave rectifying characteristics of the FB leg. Using HB leg shows the similar losses and semiconductor voltage stresses as the T-type leg. The transformer voltage change of the HB leg is twice higher than the T-type leg. On the other hand, using HB leg shows the lowest device counts that can impact on the cost reduction. compared to the T-type leg based DC transformer, HB leg can have more turns of the copper winding. However, it also has a chance to integrate the resonant inductance in the transformer with the more turns [105]. Therefore, considering the cost, losses, and transformer design flexibility, the HB/HB leg combination (V_bus side/V_p side) is selected for the DBSRC topology. In order to have simple nomenclature, the HB/HB DBSRC is named dual half bridge series resonant converter (DHBSRC) in this study.

3.4 Summary

In this section, the optimal topology for the PVC and DC transformer is selected by evaluating the advantages of each possible topology option. The objective of the multi-port PPC is to apply it to the smart home applications. The operating point of the PPC is specified to process the target DC input power range and convert it to $V_{bus} = 400$ V. The target size of the PV panel is a maximum of 10 PV panels connected in series. The nominal operating conditions of the multi-port PPC are specified as $V_{DCx} = 360$ V, $I_{DCx} = 11$ A, and $P_{DCx} = 4$ kW. The commercial residential PV data analysis and (3.10) shows that the maximum power can be tracked with $V_\mathrm{p} = 150$ V. Given the 50 % voltage margin on the switches, the voltage ratings of 300 V MOSFET are selected for the V_p side switch to handle 150 V partial voltage. The 650 V MOSFET for the V_bus side switch to handle 400 V inverter side DC bus voltage.

The proposed PPC has two DC-DC converter stages of partial voltage converters and DC transformer. The DC-DC converters of the proposed PPC should have the bidirectional power flow capability to apply to the smart home application. The PVCs of the proposed architecture performs the control of the DC input current. The PVCs processes the full currents of the DC inputs with the partial voltage on C_p. Therefore, the PVCs can achieve the PPP by the partial voltage-full current power processing. The PVC has three possible topology options: i) Boost type, ii) Buck type and iii) Buck-boost type. Evaluation of ΔV_Lfx and semiconductor losses shows that boost and buck type PVCs can have twice less ΔV_Lfx compared to buck-boost type PVCs. According to (3.11) and (3.15), boost and buck type PVC can have twice less L_f in the same Δi_fx compared to buck-boost type PVC. The semiconductor loss analysis also shows that the switching and conduction losses of the boost type and the buck type PVC have 50% losses compared to the buck-boost type PVC. The input/output voltage ratio of the target application is $V_\mathrm{DCx} \leq V_\mathrm{bus}$. Therefore, the topology can be either boost or buck-boost type. By using buck-boost type PVC, it is possible to apply flexible DC input voltage. However, it has twice the L_f, semiconductor losses and number of switching devices. Therefore, boost type PVC is selected for the optimum topology.

Table 3.8: Comparison condition of reference and proposed PPC

Combination	Semiconductor device counts	Max. Semiconductor voltage stress		MOSFET voltage ratings		Transformer voltage setp ($\frac{dV}{dt}$)	Losses (p.u.)	Turns Ratio
		V_{bus} side	V_{p} side	V_{bus} side	V_{p} side			
NPC/NPC	12	200V	75V	300v	150V	200V	2.75e-3 p.u.	2.5:1
NPC/T	10	200V	150V	650V	300v	200V	2.6e-3 p.u.	2.5:1
NPC/FB	10	200V	150V	650V	300v	200V	2.75e-3 p.u.	1.25:1
NPC/HB	8	200V	150V	650V	300v	200V	2.6e-3 p.u.	2.5:1
T/T	10	400V	150V	650V	300v	200V	2.5e-3 p.u.	2.5:1
T/NPC	8	200V	75V	650V	150V	200V	2.6e-3 p.u.	2.5:1
T/FB	8	400V	150V	650V	300v	200V	2.6e-3 p.u.	1.25:1
T/HB	6	400V	150V	650V	300v	200V	2.5e-3 p.u.	2.5:1
FB/NPC	10	400V	75V	650V	150V	800V	4.75e-3 p.u.	5:1
FB/T	8	400V	150V	650V	300v	800V	4.5e-3 p.u.	5:1
FB/FB	8	400V	150V	650V	300v	800V	4.75e-3 p.u.	2.5:1
FB/HB	6	400V	150V	650V	300v	800V	4.5e-3 p.u.	5:1
HB/NPC	8	400V	75V	650V	150V	400V	2.6e-3 p.u.	2.5:1
HB/T	6	400V	150V	650V	300v	400V	2.5e-3 p.u.	2.5:1
HB/FB	6	400V	150V	650V	300v	400V	2.6e-3 p.u.	1.25:1
HB/HB	4	400V	150V	650V	300v	400V	2.5e-3 p.u.	2.5:1

The DC transformer of the proposed multi-port PPC is necessary to respect the energy conservation principle and the partial power flow based on (3.3). The DC transformer of the proposed architecture have to handle the full voltage of the inverter bus (V_{bus}). However, even with the full voltage, the partial current is processed by the DC transformer. Hence, the DC transformer stage also can achieve the PPP by processing full voltage-partial current. Two general bidirectional isolated converter topology options are considered for the DC transformer: i) DAB converter and ii) DBSRC. The DC transformer is required to be ZVS capable under all operating conditions to improve efficiency. However, the evaluation of the ZVS condition of the DAB converter shows that DAB cannot achieve the ZVS condition when the number of the input ports are less than 7 ($x < 7$). On the other hand, the ZVS of DBSRC can be achieved when the converter operates in the $f_{\text{SRC}} > f_{\text{r}}$ condition. Thus, the DBSRC converter is selected for the DC transformer topology. The next step is to select the detailed topology of the DBSRC to obtain the optimum size and losses. The four possible options can be considered for each V_{bus} and V_{p} side bridges of DBSRC: i) NPC leg, ii) T-type leg, iii) full bridge (FB) leg, and iv) half bridge (HB) leg; are investigated. By selecting the different combinations of each V_{bus} and V_{p} side leg options, sixteen different topology options can be made. The loss analysis that shown in Fig. 3.23 shows that the HB/HB combination can have the lowest losses compared to the other possible combination options. The semiconductor device voltage stresses and the transformer voltage changes are also compared in Table. 3.8. The comparison shows that the use of the FB leg has the least advantages as it has the highest voltage step dV/dt on the transformer and high voltage stresses on the semiconductor devices. By using NPC, the voltage stress on the semiconductor device and the dV/dt on the transformer can be reduced. Therefore, the lower voltage rating device can be used and there is a greater chance of reducing the copper windings of the transformer if NPC leg is selected. However, the use of NPC leg may increase the number of semiconductor devices, which may have an impact on the cost increase. On the other hand, the use of T-leg shows the same voltage change on the transformer and the lower losses compared to NPC leg. In addition, the number of semiconductors is lower than with the NPC leg. Using the HB leg shows the same losses as the T leg options, but it has twice the dV/dt on the transformer. Even with the high transformer voltage step, the component count of the HB leg is the lowest and there is more flexibility in the transformer design. Therefore, considering the loss analysis and cost, the HB/HB based SRC, also called DHBSRC, is selected for the DC transformer topology.

4 Control and power conversion parameter optimization of multi-port PPC

In the previous section, the boost-type PVCs and DHBSRCs are selected as the optimal topologies of PVC and DC transformer stages of the multi-port PPC. Now, hardware design and control strategy of the proposed architecture should be developed to control the power of the DC inputs in the smart home system. As shown in Fig. 3.1, the boost-type PVCs take the responsibility of controlling the DC input currents (I_{DCx}), which allows the required power control of the DC inputs. The partial voltage, V_{p}, is the other key control variable that allows the partial voltage on the boost-type PVCs to achieve the PPP. The control strategy of each boost-type PVC and DHBSRC is developed which allows the control of both I_{DCx} and V_{p}.

The main objectives of the proposed architecture are to achieve high efficiency and high power density. Therefore, the design of the hardware parameters of each boost-type PVCs and DHBSRC should be carried out to optimize the volume and the losses of the converter. Firstly, the optimum switching frequency of the boost-type PVCs is selected to find an optimum trade-off point between the losses and volume of the boost-type PVCs. The parameters of the filter inductor and partial voltage capacitors can be designed based on the selected switching frequency. Guidelines for the selection of commercial inductors and capacitors are also explained. Finally, the PI control gain can be selected using the selected parameters and the small signal model of the boost-type PVC.

In order to design the parameters of the DHBSRC, the switching frequency should also be selected to find the optimum trade-off point between volume and losses. Based on the selected switching frequency, the first harmonic approximation (FHA) model of the converter can be derived. The parameters of the resonant tank can be determined using the FHA model. The DHBSRC plays a key role in maintaining the stiffness of V_{p}. Therefore, the actual parameters of the DHBSRC should have small errors compared to the designed values. The transformer design is also followed to obtain accurate parameters of the designed value. In addition, the transformer design is validated by Maxwell simulation models and inductance measurement results to ensure the accurate power conversion behavior of the DHBSRC stage. The accuracy of the transformer design is presented by comparing the design parameters, simulation and measurement results.

4.1 Operating principle of the multi-port PPC

A schematic of the boost-type PVCs is shown in Fig. 4.1. The input DC sources current is represented as $I_{\mathrm{DCx}}|_{\mathrm{x}=1,2,\cdots,\mathrm{n}}$, voltage on the input capacitors are written as $v_{\mathrm{DCx}}|_{\mathrm{x}=1,2,\cdots,\mathrm{n}}$, and the output voltage on the bus side is expressed as v_{bus}. The expressions of the voltages, v_{DCx} and v_{bus}, are including the DC average voltage and the ripple components due to the switching. Hence, its DC average value which are V_{DCx} and V_{bus} can be used for the DC average model analysis.

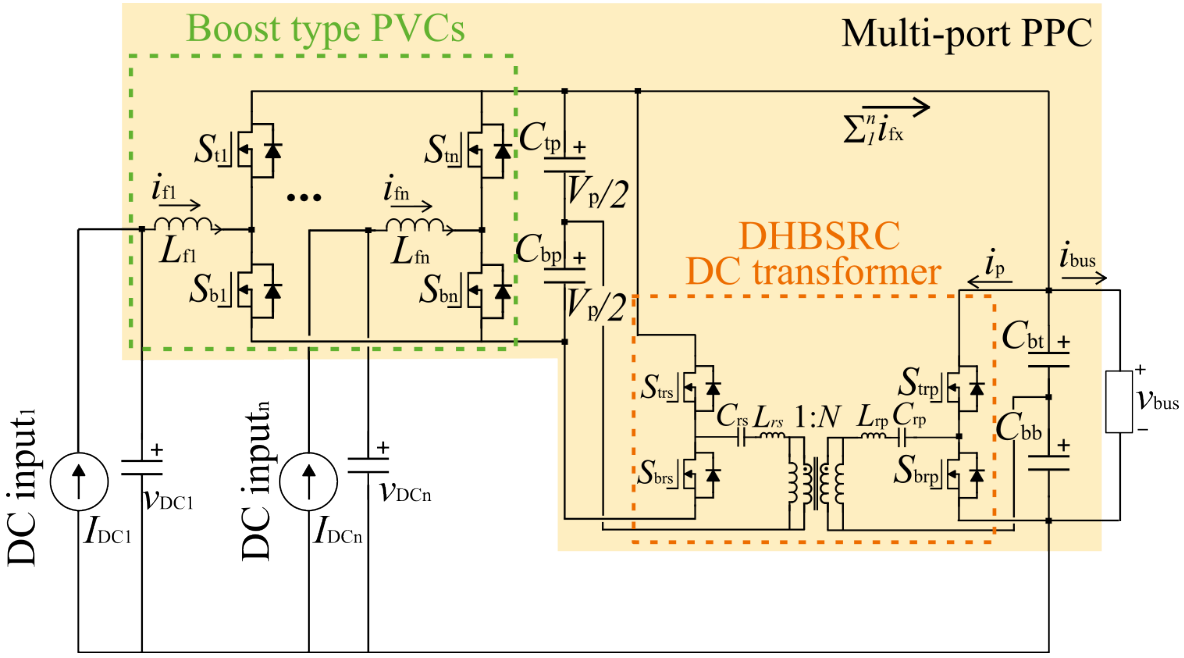


Figure 4.1: Proposed multi-port partial power converter schematics.

The n number of half bridge based boost-type PVCs are connected to the series capacitor sets [C_{tp}, C_{bp}]. All the half bridges connected to [C_{tp}, C_{bp}] are identical. Therefore, the half bridges of boost-type PVCs can be controlled in the same manner. This means that the investigation of a single half bridge of the boost-type PVCs can represent all the other half bridges connected in parallel. The switching states and detailed operation of the boost-type PVCs have already been described in section. 3.2.2, Fig. 3.6 and Table. 3.4. The half bridge converters of boost-type PVC can force the bidirectional inductor current i_{fx} on which flows from V_{DCx} to V_{bus} and vice versa. Due to the bidirectional current control capability, the input port can utilize both of DC sources and loads, respectively.

The DHBSRC is connected between V_{bus} and the partial voltage DC-link sets [C_{tp}, C_{bp}]. A partial power (P_p) can flow between V_{DCx} and V_{bus} through the DBSRC as defined in (3.4). The equation shows that the DC-transformer can achieve the PPP by processing full voltage(V_{bus})-partial current(I_p). Since the stiff partial voltage (V_p) at [C_{tp}, C_{bp}] is manipulated by the DHBSRC, the boost-type PVCs can achieve the PPP by processing partial voltage-full current. The topology in Fig. 4.1 has the same architecture as proposed in Fig. 3.1 of Chapter 3, input and output power relations and the energy conservation of the proposed architecture follows the principles of (3.1)–(3.9). Based on (3.29), the direction of P_p can be decided by difference between ΣP_{DCx} and P_{bus}. If $V_{bus}\Sigma I_{DCx} > \Sigma V_{DCx} I_{DCx}$, the inverter side switches [S_{trp} and S_{brp}] are enabled (P_p flows from V_{bus} to V_{DCx}). On the other hand, if $V_{bus}\Sigma I_{DCx} < \Sigma V_{DCx} I_{DCx}$, the partial voltage switches [S_{trs} and S_{brs}] are enabled (P_p flows from V_{DCx} to V_{bus}). The P_p flow mode, its condition, and switching state are organized in the table. 4.1.

Table 4.1: boost-type PVC: Definition of operating mode

$P_{\mathrm{bus}} - \Sigma P_{\mathrm{DCx}}$	P_{p} flow	Enabled Switches	Mode
+	$V_{\mathrm{bus}} \rightarrow V_{\mathrm{DCx}}$	S_{trp}, S_{brp}	Forward
-	$V_{\mathrm{bus}} \leftarrow V_{\mathrm{DCx}}$	S_{trs}, S_{brs}	Reverse

4.2 Parameter design of PVC

As shown in Fig. 4.1, each PVC consists of a filter inductor (L_{fx}), partial DC link capacitors (C_{tp}, C_{bp}) and a half bridge leg (S_{tx}, S_{bx}). The parameters and volumes of the L_{fx}, C_{tp}, C_{bp} can be changed by changing the switching frequency (f_{s}) of the half bridges of boost-type PVCs. In addition, the losses of the boost-type PVCs can be changed by the f_{s}. Therefore, to decide the optimal parameters of the L_{fx}, C_{tp}, C_{bp}, the optimal f_{s} should be decided first. To decide the f_{s}, the relationships between f_{s} and the volumes of L_{fx}, C_{tp}, C_{bp} should analyzed. Furthermore, the relationship between f_{s} and losses of half bridges should be evaluated.

Firstly, the relationship between f_{s} and L_{f} can be confirmed by the formula for L_{f}, as given in (4.1).

$$L_{fx} = \frac{V_{\mathrm{DCx}} + V_{\mathrm{p}} - V_{\mathrm{bus}}}{0.5\Delta I_{\mathrm{fx}} f_{\mathrm{s}}} \tag{4.1}$$

where L_{fx} is the filter inductance of the PVCs, D_{x} is the duty cycle of the PVCs, and ΔI_{fx} is the target I_{fx} ripple.

Similarly, the relationship between f_s and partial capacitance sets [C_{tp} and C_{bp}] can be defined as (4.2), where defining total capacitance as C_{p}.

$$C_{\mathrm{p}} = C_{\mathrm{tp}} + C_{\mathrm{bp}} = \frac{0.5 I_{\mathrm{fx,peak}}}{\Delta V_{\mathrm{p}} f_{\mathrm{s}}} \tag{4.2}$$

where C_{p} is the total partial capacitance, $I_{\mathrm{fx}_{\mathrm{peak}}}$ is the peak of i_{fx}, and ΔV_{p} is the target V_{p} ripple.

The volume of L_{fx} and [C_{tp}, C_{bp}] can be estimated using:

$$\Lambda_{\mathrm{L}} = K_{\mathrm{L}} L_{\mathrm{fx}} I_{\mathrm{fx}}^2 \tag{4.3}$$

$$\Lambda_{\mathrm{C}} = K_{\mathrm{C}} C_{\mathrm{p}} V_{\mathrm{p}} = K_{\mathrm{C}}(C_{\mathrm{tp}} + C_{\mathrm{bp}}) V_{\mathrm{p}} \tag{4.4}$$

where K_{L} is the inductor volume coefficient proportional to the stored energy, Λ_{L} is the volume of the inductor, K_{C} is the capacitor volume coefficient, and Λ_{C} is the volume of capacitor [106].

By substituting (4.1) and (4.2) into (4.3) and (4.4), the volumes can be redefined as follows:

$$\Lambda_{\mathrm{L}} = K_{\mathrm{L}} \frac{V_{\mathrm{DCx}} + V_{\mathrm{p}} - V_{\mathrm{bus}}}{\Delta I_{\mathrm{fx}} f_{\mathrm{s}}} I_{\mathrm{fx}}^2 \tag{4.5}$$

$$\Lambda_{\mathrm{C}} = K_{\mathrm{C}} \frac{0.5 I_{\mathrm{fx_{peak}}}}{\Delta V_{\mathrm{p}} f_{\mathrm{s}}} V_{\mathrm{p}} \tag{4.6}$$

Finally, (4.5) and (4.6) show that the volume of L_{fx} and C_{p} can be reduced by increasing f_{s}.

Losses are the other key factor in the design of PVCs. The inductor has two major loss elements: i) core losses, ii) copper losses). The core losses of L_{fx} in unit volume can be calculated as:

$$P_{\mathrm{core}} = K_{\mathrm{core}} f_{\mathrm{s}}^{\alpha} \Delta B^{\beta} \tag{4.7}$$

where P_{core} is the core losses of L_{fx} in unit volume, α, β are the stein-Metz coefficients, and ΔB is the change of flux density.

The copper losses can be calculated as follows:

$$P_{\mathrm{copper}} = I_{\mathrm{fx_{rms}}}^2 R_{\mathrm{Lfx}} \tag{4.8}$$

where P_{copper} is the copper losses of L_{fx}, $I_{\mathrm{fx_{rms}}}$ is the root mean square (RMS) of i_{fx}, and R_{Lfx} is the resistance of the inductor winding.

(4.7) and (4.8) show that f_{s} has the major impact on the P_{core}. The inductor losses are proportional to the increase in f_{s}.

As expressed in (4.9), the equivalent series resistance of the capacitor represents the losses of the capacitor.

$$\mathrm{ESR} = \frac{\sigma}{\varepsilon \omega_{\mathrm{s}}^2 C_{\mathrm{p}}} \tag{4.9}$$

where σ is the dielectric bulk conductivity, ε is the permittivity of the dielectric, and $\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$.

The power losses on C_{p} can be calculated as:

$$P_{\mathrm{C}} = I_{\mathrm{fx_{rms}}}^2 \mathrm{ESR} \tag{4.10}$$

where P_{C} is the capacitor losses.

The relationship between f_{s} and ESR in (4.9) shows that losses on the capacitor increases when increases f_{s}.

The change in f_{s} also affects the switching losses P_{sw} of the semiconductors. The switching losses of S_{tx} and S_{bx} can be calculated using the equations (3.18)–(3.27). Considering all the losses related to f_s (P_{core}, P_C, and P_{sw}), the relationship between f_s and the losses of the boost-type PVCs can be investigated.

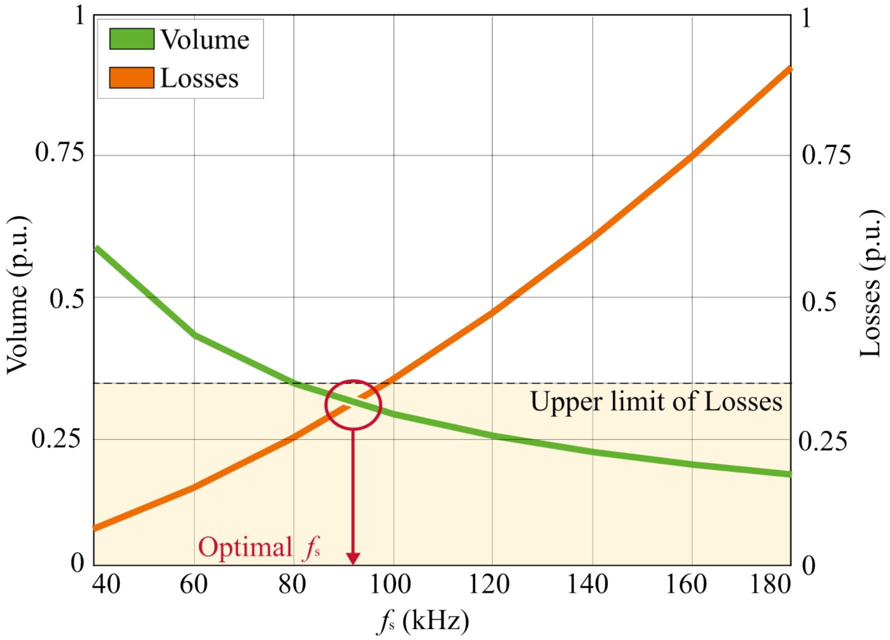


Figure 4.2: PVC volume and losses relationship between switching frequency: Passive element volume curve (Green), and losses curve (Orange).

In Fig. 4.2, the variation of boost-type PVCs volume and losses with respect to f_s are analyzed. In order to find the optimal f_s, volume and losses per unit (p.u.) are compared on the same plot. Set the maximum losses at maximum f_s, where $f_s = 180$ kHz, as a base losses, the p.u. losses of the PVCs can be plotted as shown in the figure. In addition, set the upper limit losses as 0.6 % of the rated power as shown in Table. 3.2, the switching frequency that make less than 0.6 % of the losses can be decided. In the figure, the orange line represents the p.u. losses related to f_s, which are the P_{core}, P_C and P_{sw}. The curve shows that the total losses of P_{core}, P_C and P_{sw} are proportional to the f_s. As f_s increases, the losses also increases. On the other hand, the volume of the passive components (L_{fx} and C_p) are inversely proportional to f_s. Therefore, the volume can be reduced by increasing f_s. The losses curve crosses the upper losses limit at 100 kHz. At this point, the volume of the inductor can be small, but the losses of the converter can increase. The main focus of the proposed multi-port PPC is to minimize the losses on the power electronics devices. Therefore, allowing 20 % margin for the losses and considering the trade-off between the p.u. volume and losses, 90 kHz is chosen as the optimum f_s where the volume and losses curve intersect. At this intersection point, the expected losses are 0.5 % of the rated power (ΣP_{DCx}).

After selecting f_s, the parameters of L_{fx} and C_p can be selected. The target input current ripple (ΔI_{fx}) is set to be 40 % of the nominal current (c.f. Table 3.2). The calculated inductance L_{fx} is 65 µH, using (4.1). The target partial voltage ripple ΔV_p is 5 % of V_p. Using (4.2), the total capacitance C_p of the boost-type PVCs can be calculated as 14 µF.

Next, the volume estimation of the inductor L_{fx} and capacitor C_p are calculated to select the optimal commercial passive component. Using (4.3), the Λ_L verses LI_{fx}^2 of commer-

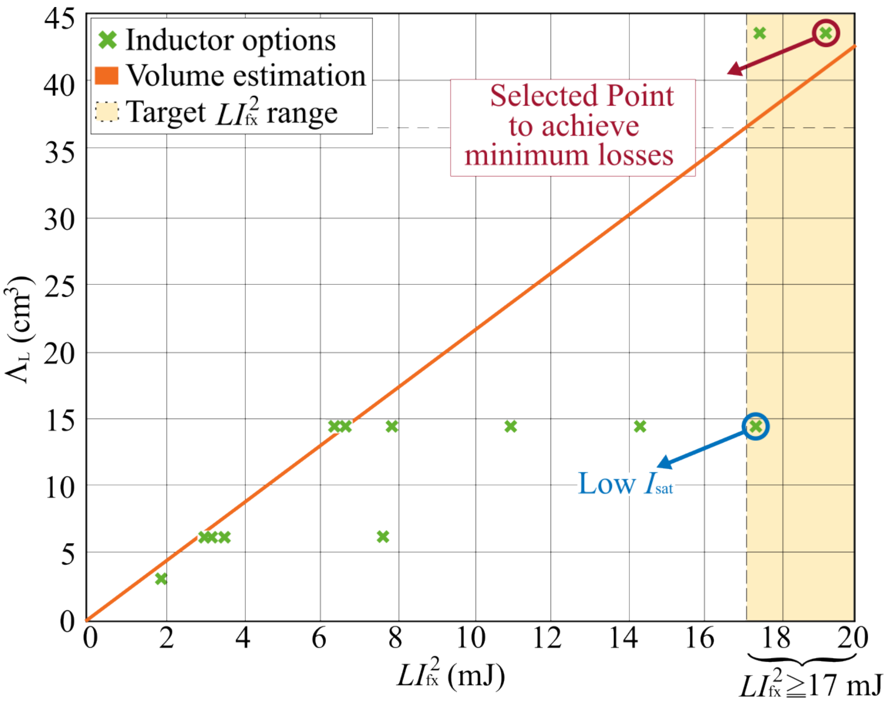


Figure 4.3: Inductor volume estimation.

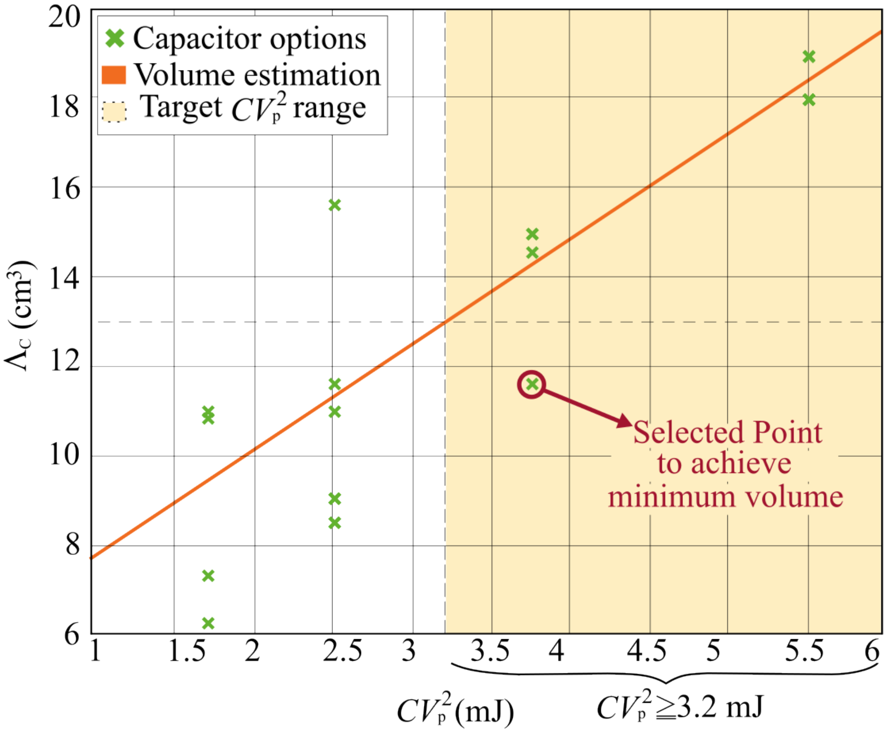


Figure 4.4: Capacitor volume estimation.

cial power inductors (Würth Electronics power inductors) and volume estimation results are plotted in Fig. 4.3. The calculated LI_{fx}^2 and Λ_{L} at nominal current are 17 mJ and 37 cm^3 respectively. Given the estimation results, there are three possible options for the commercial inductors that meet the expected LI_{fx}^2 and Λ_{L}. The commercial inductor that has a lower saturation current (I_{sat}) than the nominal current is excluded from the option. In addition, the commercial inductor that has a lower inductance than target L_{f} is also excluded from the option. The selected commercial inductor satisfies target I_{sat}, and L_{fx}, and it also has a 10 % LI_{fx}^2 margin. Fig. 4.5 shows the picture of the selected commercial inductor and the inductor property is given in Table. 4.2.

Figure 4.5: Selected commercial inductor from Würth Electronics.

Table 4.2: Properties of selected inductor

Properties	Symbol	Value	Unit
Inductance	L_{fx}	65	µH
Rated Current	I_{rate}	17.2	A
Saturation Current	I_{sat}	26.6	A
DC Resistance	R_{L}	13.13	mΩ
Length	l	36	mm^2
Width	w	34.5	mm^2
Height	h	35	mm^2
Volume	Λ_{L}	43.47	cm^3

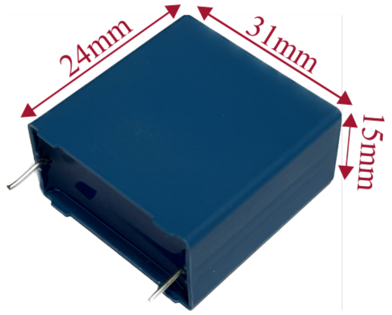


Figure 4.6: Selected commercial capacitor from TDK.

Table 4.3: Properties of selected capacitor

Properties	Symbol	Value	Unit
Capacitance	C_{p}	14	µH
Rated Voltage	V_{rate}	250	V
DC Resistance	ESR	5	mΩ
Length	l	31	mm^2
Width	w	15	mm^2
Height	h	24	mm^2
Volume	Λ_{C}	11.16	cm^3

Similarly, the estimated Λ_{C} and commercial TDK capacitors are plotted in Fig. 4.4. The estimated $C_{\mathrm{p}}V_{\mathrm{p}}$ and Λ_{c} are 3.2 mJ and 13 cm^3. The commercial capacitors $C_{\mathrm{p}}V_{\mathrm{p}} \geq 3.2$ mJ should be selected to maintain the partial voltage V_{p}. There are three possible options at $C_{\mathrm{p}}V_{\mathrm{p}} = 3.75$ mJ. Among the three options at $\Lambda_{\mathrm{c}} = 11.6$ cm^3, the capacitor with the minimum volume is selected to reduce the size of the multi-port PPC. Fig. 4.6 shows the image of the selected commercial capacitor and the capacitor's characteristics are given in the table. 4.3. Following the processes of the parameter selection, the L_{fx}, C_{p} selection can be organized by the flowchart that depicted in Fig. 4.7.

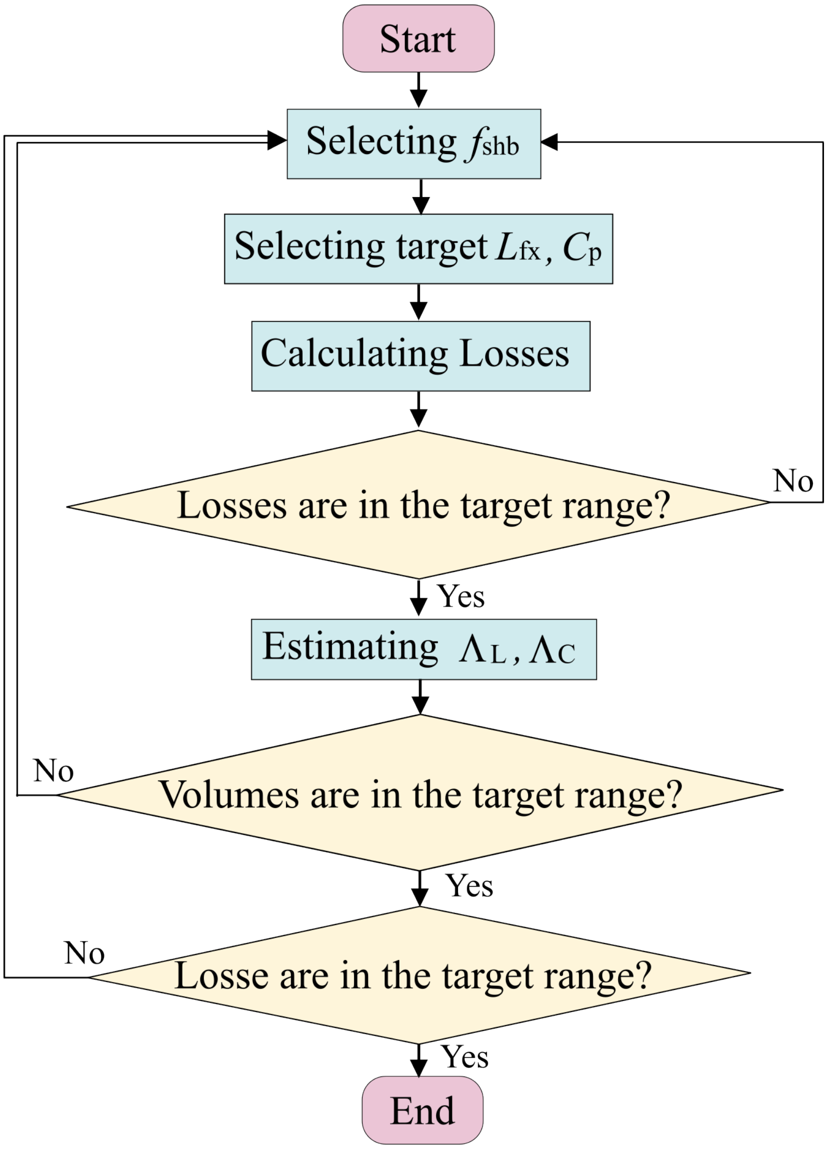


Figure 4.7: Parameter selection flow for the PVCs of proposed multi-port partial power converter.

4.2.1 Small signal model and control of PVC stage

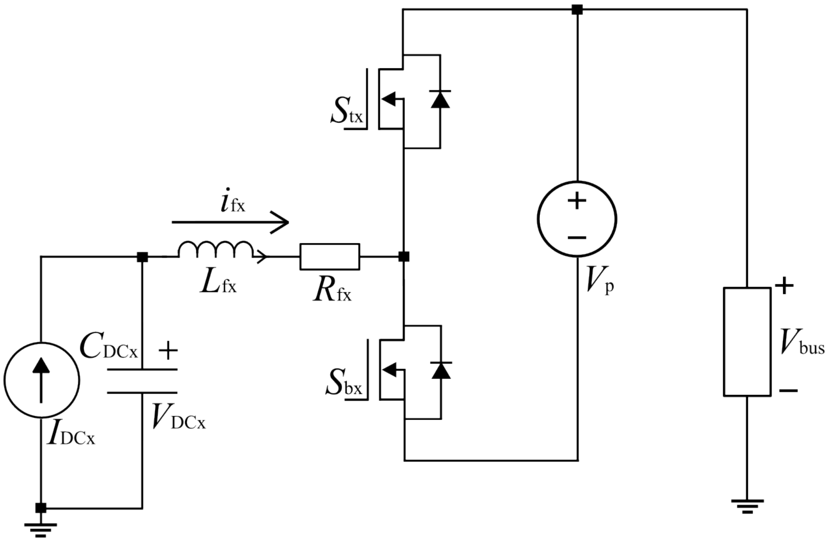


Figure 4.8: Equivalent circuit of boost-type PVCs.

The control of the boost-type PVCs can be designed from their time domain model. The equivalent model of the single boost-type PVC is shown in Fig. 4.8. The boost-type PVCs those connected to C_p are the identical half bridge converters. Therefore, the model of the single PVC can represent all the other PVCs. The positive and negative node of V_p is connected to the DHBSRC which is the DC-transformer stage of the proposed architecture. The DHBSRC allows the stiff partial voltage by its current flow for the required V_p. Therefore, V_p can be simplified to a stiff voltage source. Therefore, the DHBSRC can be simplified as an ideal voltage source. To make the model accurate, the resistance component (R_{fx}) owing to its winding is also taken into account for the inductor. Hence, the equivalent circuit of the boost-type PVC can be modeled as shown in Fig. 4.8. Based on the equivalent circuit in Fig. 4.8 and the state of the boost-type PVC in Table. 3.4, the equations of negative and bypass states can be expressed as follows:

$$L_{fx}\frac{di_{fx}(t)}{dt}+R_{fx}i_{fx}=v_{bus}(t)-v_{pvx}(t)-v_p(t) \qquad \text{when} \quad 0<t<D_xT_s \tag{4.11}$$

$$L_{fx}\frac{di_{fx}(t)}{dt}+R_{fx}i_{fx}=v_{bus}(t)-v_{pvx}(t) \qquad \text{when} \quad D_xT_s<t<T_s \tag{4.12}$$

where R_{fx} is the resistance of L_{fx}.

The average model of the PVC can be derived as follows:

$$L_{fx}\frac{di_{fx}(t)}{dt}+R_{fx}i_{fx}=v_{bus}(t)-v_{pvx}(t)-D_sv_p \tag{4.13}$$

In order to derive the small signal model, Considering the small perturbation ($\tilde{x}(t)$) added to the steady-state value ($\bar{X}$), (4.13) can be written as follows:

$$L_{fx}\frac{d(\bar{I}_{\mathrm{fx}}+\tilde{i}_{\mathrm{fx}}(t))}{dt}+R_{\mathrm{fx}}(\bar{I}_{\mathrm{fx}}+\tilde{i}_{\mathrm{fx}}(t))$$
$$=(\bar{V}_{\mathrm{bus}}+\tilde{v}_{\mathrm{bus}}(t)-\bar{V}_{\mathrm{DCx}}-\tilde{v}_{\mathrm{DCx}}(t)-(\bar{D}_{\mathrm{x}}-\tilde{d}_{\mathrm{x}}(t))(\bar{V}_{\mathrm{p}}+\tilde{v}_{\mathrm{p}}(t)) \quad (4.14)$$

Solving (4.14) with neglecting the second order ripple term, the equation can be expressed as follows:

$$L_{\mathrm{fx}}\frac{d(\bar{I}_{\mathrm{fx}}+\tilde{i}_{\mathrm{fx}}(t))}{dt}+R_{\mathrm{fx}}(\bar{I}_{\mathrm{fx}}+\tilde{i}_{\mathrm{fx}}(t))$$
$$=(\bar{V}_{\mathrm{bus}}+\tilde{v}_{\mathrm{bus}}(t)-\bar{V}_{\mathrm{DCx}}-\tilde{v}_{\mathrm{DCx}}(t)-\bar{D}_{\mathrm{x}}\bar{V}_{\mathrm{p}}-\tilde{d}_{\mathrm{x}}(t)\bar{V}_{\mathrm{p}}+\bar{D}_{\mathrm{x}}\tilde{v}_{\mathrm{p}}(t)) \quad (4.15)$$

The DC steady state terms and the AC small signal terms can be divided from (4.15). The product of the parasitic series resistance R_{fx} and average current I_{fx} has much smaller value which is negligible compared to V_{bus}, V_{DCx}, and V_{p}. Hence, the steady state equation can be derived as follows:

$$D_{\mathrm{x}}=\frac{V_{\mathrm{bus}}-V_{\mathrm{DCx}}}{V_{\mathrm{p}}} \quad (4.16)$$

The small signal model of the PVCs also can be derived by applying Laplace and inverse Laplace transform to (4.15). The results of the Laplace and inverse Laplace transform of the DC voltages $\tilde{v}_{\mathrm{bus}}(t)$, $\tilde{v}_{\mathrm{pvx}}(t)$, and $\tilde{v}_{\mathrm{p}}(t)$ are close to zero. Therefore, the small signal model related to the controlled variable and the actuator can be derived as follows:

$$i_{\mathrm{fx}}(s)=\frac{V_{\mathrm{p}}}{L_{\mathrm{fx}}s+R_{\mathrm{fx}}}d_{\mathrm{x}}(s) \quad (4.17)$$

Finally, the transfer function of the small signal plant can be written as:

$$G_{\mathrm{HBx}}(s)=\frac{i_{\mathrm{fx}}(s)}{d_{\mathrm{x}}(s)}=\frac{V_{\mathrm{p}}}{L_{\mathrm{fx}}s+R_{\mathrm{fx}}} \quad (4.18)$$

where $G_{\mathrm{HBx}}(s)$ is the plant of the boost-type PVCs.

The control block diagram of the PVC is shown in Fig. 4.9. The partial voltage $V\mathrm{p}$ is controlled by the DBSRC stage, the boost-type PVCs only need to control the DC input currents. The reference current (I_{fx}^{*}) is given by the algorithm of the target operation (MPPT, battery charging, etc.). I_{fx} can follow the reference currents by PI current control. The digital control computation time ($e^{-sT_{\mathrm{s}}}$) and the PWM delay (ZOH) are also taken into account in

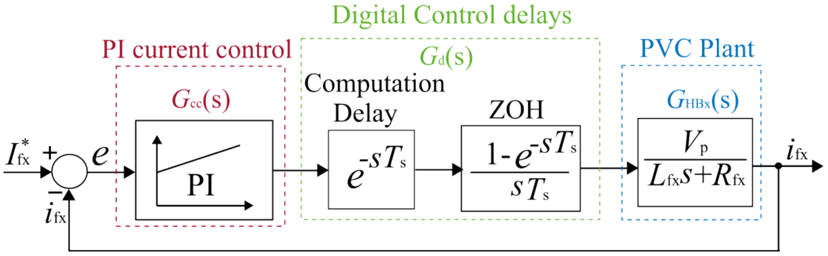


Figure 4.9: Current control loop of boost type PVC stage.

the digital control delay block ($G_\mathrm{d}(s)$) [107]. Finally, the boost-type PVCs force the i_fx by the switching signals given to it. To follow the reference current from the MPPT, a PI control (G_cc) is used for the current control. The transfer function of the PI control is expressed as follows:

$$G_\mathrm{cc}(s) = K_\mathrm{p}\left(1 + \frac{1}{T_\mathrm{i}s}\right) \tag{4.19}$$

where K_p is the proportional gain and T_i is the integral time.

The digital control delays block ($G_\mathrm{d}(s)$) can be approximated by considering the computational delay, sampler, and ZOH blocks which can be given as follows:

$$G_\mathrm{d}(s) = \frac{1}{1.5sT_\mathrm{s} + 1} \tag{4.20}$$

where T_s is the sampling time. (4.20) shows that the digital control delay block can be expressed as the summation of computation time T_s (where $T_\mathrm{s} = 11$ µs which is the same as the sampling time) and the $0.5T_\mathrm{s}$ PWM delay.

The integration time constant T_i can be derived by the LC time constant τ of G_HBx which can be calculated as follows:

$$T_\mathrm{i} = \tau = \frac{L_\mathrm{fx}}{R_\mathrm{Lfx}} \tag{4.21}$$

Hence, the integration time can be calculated by the L_fx and R_Lfx which depicted in the table. 4.2.

The closed loop transfer function of the current control loop can be calculated as follows:

$$H_{\mathrm{I_{fx}}}(s) = \frac{\frac{2V_\mathrm{p}K_\mathrm{p}}{3T_\mathrm{s}L_\mathrm{fx}}}{s^2 + \frac{2}{3T_\mathrm{s}}s + \frac{2V_\mathrm{p}K_\mathrm{p}}{3T_\mathrm{s}L_\mathrm{fx}}} \quad \text{where} \quad 2\zeta\omega_\mathrm{c} = \frac{2}{3T_\mathrm{s}}, \omega_\mathrm{c}^2 = \frac{2K_\mathrm{p}}{3T_\mathrm{s}L_\mathrm{fx}} \tag{4.22}$$

Assuming the critical damping condition where $\zeta = 1$, proportional gain can be defined as follows:

$$K_\mathrm{p} = \frac{L_\mathrm{fx}}{3V_\mathrm{p}T_\mathrm{s}} \tag{4.23}$$

Finally, put (4.23) in the closed loop (4.22), $H_{\mathrm{I_{fx}}}$ can be reorganized as follows:

$$H_{\mathrm{I_{fx}}}(s) = \frac{\dfrac{2}{9T_\mathrm{s}^2}}{s^2 + \dfrac{2}{3T_\mathrm{s}}s + \dfrac{2}{9T_\mathrm{s}^2}} \tag{4.24}$$

Furthermore, using the relation in (4.22), the settling time can be calculated by following equation:

$$T_\mathrm{set} = \frac{4}{\zeta\omega_\mathrm{c}} \tag{4.25}$$

where T_set is the settling time.

Putting $\zeta\omega_c$ in (4.25), the settling time results in $T_\mathrm{set} = 133$ µs.

4.3 Parameter design of DC transformer

To design the parameters of the DC transformer, the switching frequency of the DHBSRC (f_SRC) should be determined. Changing of f_SRC has an impact on volume of the transformer (Λ_T). In order to estimate Λ_T, the voltage on the transformer windings should first be found. The voltage on the V_bus side winding can be derived as follows:

$$V_\mathrm{p} = 2\pi f_\mathrm{SRC} N_1 B_\mathrm{max} A_\mathrm{c}/\sqrt{2} \tag{4.26}$$

where V_p is the RMS voltage on V_bus side of the transformer, f_SRC is the DHBSRC switching frequency, N_1 is the number of the turns on V_bus side, and A_c is the core area.

By rewriting (4.26), A_c can be defined as follows:

$$A_\mathrm{c} = \frac{V_\mathrm{p}}{4.44 f_\mathrm{SRC} N_1 B_\mathrm{max}} \tag{4.27}$$

Equation (4.27) shows that increasing f_SRC decreases A_c. Since. Since,the volume of the core (Λ_co) has the greatest influence on Λ_T. Therefore Λ_T can be estimated by Λ_co which is given in (4.28) [108–110].

$$\Lambda_{\mathrm{co}} = A_{\mathrm{c}} l_{\mathrm{c}} \tag{4.28}$$

where l_{c} is the length of the core.

The core losses per unit volume of the transformer is also dependent on f_{SRC}. Similar to (4.7), the core losses of the transformer can be presented as:

$$P_{\mathrm{V}} = K_{\mathrm{core}} f_{\mathrm{SRC}}^{\alpha} \Delta B^{\beta} \tag{4.29}$$

where P_{V} is the transformer core losses per unit volume and K_{core}, α, and β are the stein-Metz coefficients [111].

Using (4.27), (4.28), and (4.7) the unit volume and unit losses of the transformer in different switching frequencies can be plotted as Fig. 4.10. The losses can be analyzed in p.u. by assuming the losses at maximum f_{SRC} as a base losses of the transformer which is 1.2 % of rated power (c.f. Table. 3.2). Set the upper limit of the losses is 0.6 % of the total system power, the losses curve crosses the upper losses limit at 215 kHz. As discussed earlier, minimizing the losses on the power electronics devices are the first aim of the study. Therefore, allowing 20 % margin for the losses and considering the trade off between the losses and volume with respect to the f_{SRC}, the optimum switching frequency f_{SRC} is set at 200 kHz, where the transformer losses are 0.5 % of the rated power.

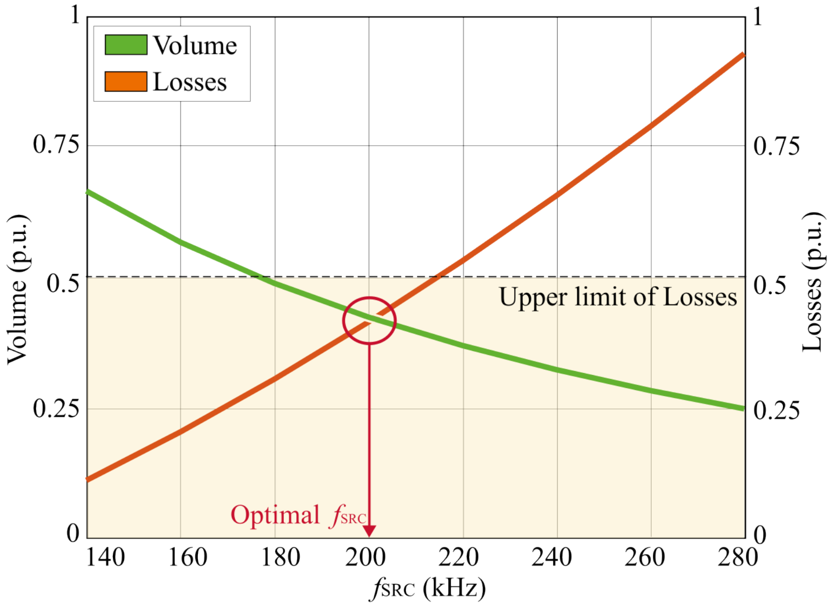


Figure 4.10: p.u. analysis of DHBSRC: Passive element volume curve (Green), and losses curve (Orange).

4.3.1 First harmonic approximation model of DHBSRC

The First Harmonic Approximation (FHA) model, which assumes that the first harmonic component only affects the power transmission, can be applied to the DHBSRC. The DHBSRC current can be considered as a sinusoidal wave whose frequency is equal to the resonant frequency (f_r), neglecting all higher order harmonics [112]. The DHBSRC can be driven by the fixed duty cycle of 50 % and the fixed switching frequency which is f_{SRC} close to the resonant frequency f_r. Therefore, the FHA model can represent the DHBSRC of the proposed multi-port PPC where the fundamental frequency of the current flows on the resonant tank is f_r.

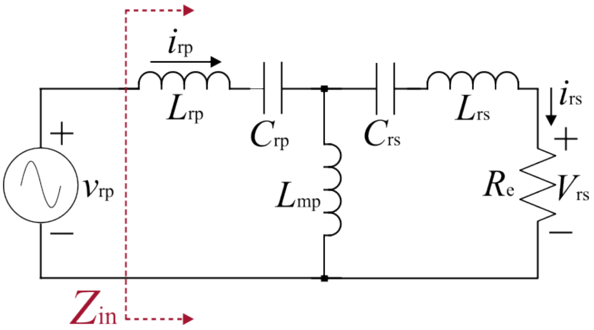


Figure 4.11: First harmonic approximation (FHA) equivalent circuit of DHBSRC.

The equivalent circuit of the FHA model of the DHBSRC is shown in Fig. 4.11. The switching of the DHBSRC forces the square wave voltage on the resonant tank. In Fig. 4.11, [L_{rp} and C_{rp}] represents the parameters of the resonant tanks on the V_{bus} side, and [L_{rs} and C_{rs}] represents the V_p side resonant tanks. The same power is processed on the V_{bus} side and V_p sides, respectively. Therefore, the relationship of the resonant tanks can be written as follows:

$$L_{rs} = \frac{L_{rp}}{N^2} \tag{4.30}$$

$$C_{rs} = C_{rp}N^2 \tag{4.31}$$

where N is the transformer turns ratio.

By applying FHA, the square wave voltage can be approximated as a fundamental sinusoidal waveform V_{rp}. The Fundamental sinusoidal voltage input of the DHBSRC can be presented as follows:

$$v_{rp} = \frac{4}{\pi} V_{bus} sin(\omega_{SRC} t) \tag{4.32}$$

where $\omega_{SRC} = 2\pi f_{SRC}$.

The RMS of v_{rp} can be calculated as follows:

$$V_{rp} = \frac{2\sqrt{2}}{\pi} V_{bus} \tag{4.33}$$

The output voltage on the low voltage side of the DHBSR can be expressed in the same manner as follows:

$$v_{\mathrm{rs}} = \frac{4}{\pi} N V_{\mathrm{p}} sin(\omega_{\mathrm{SRC}} t - \phi_{\mathrm{o}}) \tag{4.34}$$

where v_{rs} is the fundamental component of the low voltage side square voltage of DHBSRC and ϕ_{o} is the phase angle between v_{rp} and v_{rs}.

The RMS of v_{rs} can be written as follows:

$$V_{\mathrm{rs}} = \frac{2\sqrt{2}}{\pi} N V_{\mathrm{p}} \tag{4.35}$$

The RMS of output current i_{rs} can be calculated by applying FHA as follows:

$$I_{\mathrm{rs}} = \frac{\pi}{2\sqrt{2}} N I_{\mathrm{p}} \tag{4.36}$$

From (4.35) and (4.36), equivalent AC load can be calculated as:

$$R_{\mathrm{e}} = \frac{8N^2}{\pi^2} R_{\mathrm{p}} \tag{4.37}$$

where R_{e} is the equivalent AC load and R_{p} is the equivalent DC load of the PPC which can be calculated as $V_{\mathrm{p}}^2/P_{\mathrm{p}}$.

The voltage gain of the DHBSRC can be derived by calculating the voltage on R_e as depicted in Fig. 4.11. Using the equations (4.32) and (4.34), the voltage gain, G_{SRC}, of the DHBSRC can be given as follows:

$$G_{\mathrm{SRC}}(\omega_{\mathrm{SRC}}) = \left| \frac{jX_{\mathrm{Lm}} \parallel (jX_{\mathrm{Ls}} - jX_{\mathrm{Cs}} + R_{\mathrm{e}})}{jX_{\mathrm{Lp}} - jX_{\mathrm{Cp}} + jX_{\mathrm{Lm}} \parallel (jX_{\mathrm{Ls}} - jX_{\mathrm{Cs}} + R_{\mathrm{e}})} \cdot \frac{R_{\mathrm{e}}}{jX_{\mathrm{Ls}} - jX_{\mathrm{Cs}} + R_{\mathrm{e}}} \right| \tag{4.38}$$

where $X_{\mathrm{Lm}} = \omega_{\mathrm{SRC}} L_m$, $X_{\mathrm{Lp}} = \omega_{\mathrm{SRC}} L_{\mathrm{rp}}$, $X_{\mathrm{Ls}} = \omega_{\mathrm{SRC}} L_{\mathrm{rs}}$, $X_{\mathrm{C1}} = \frac{1}{\omega_{\mathrm{SRC}} C_{\mathrm{rp}}}$, $X_{\mathrm{Cs}} = \frac{1}{\omega_{\mathrm{SRC}} C_{\mathrm{rs}}}$.

The parameters of inductor ratio h, quality factor Q, and normalize ω_{n} are defined as follows:

$$h = \frac{L_{\mathrm{m}}}{L_{\mathrm{rp}}} \tag{4.39}$$

$$Q = \frac{N^2 \sqrt{L_{\mathrm{rp}}/C_{\mathrm{rp}}}}{R_{\mathrm{e}}} \tag{4.40}$$

$$\omega_{\mathrm{n}} = \frac{\omega_{\mathrm{SRC}}}{\omega_{\mathrm{r}}} \tag{4.41}$$

where ω_{r} can be expressed as follows:

$$\omega_{\mathrm{r}} = \frac{1}{\sqrt{L_{\mathrm{rp}}C_{\mathrm{rp}}}} = \frac{1}{\sqrt{L_{\mathrm{rs}}C_{\mathrm{rs}}}} \tag{4.42}$$

Using (4.39)–(4.41), (4.38) can be rewritten as follows:

$$G_{\mathrm{SRC}}(\omega_{\mathrm{n}},h,Q) = \frac{1}{\sqrt{\left(1+\frac{1}{h}-\frac{1}{h\omega_{\mathrm{n}}^2}\right)+Q^2\left(\frac{2(\omega_{\mathrm{n}}^2-1)}{\omega_{\mathrm{n}}}+\frac{(\omega_{\mathrm{n}}^2-1)^2}{h\omega_{\mathrm{n}}^3}\right)}} \tag{4.43}$$

The low voltage side output voltage V_{p} can be obtained by:

$$V_{\mathrm{p}} = G_{\mathrm{SRC}}(\omega_{\mathrm{n}},h,Q)V_{\mathrm{bus}}/N \tag{4.44}$$

where $G_{\mathrm{SRC}}(\omega_{\mathrm{n}},h,Q)$ is the gain function of DHBSRC with respect to ω_{n}, h, and Q.

4.3.2 Parameter selection and control of DHBSRC

As shown in (4.44), the change of ω_{n}, h, and Q has the impact on the output voltage V_{p} of DHBSRC. According to the operating principle of the DHBSRC which shown in Fig. 3.21, the switch is turned off at the peak of the magnetizing current. The magnetizing current on the V_{bus} side can be calculated as follows:

$$I_{\mathrm{mp}} = \frac{2\sqrt{2}}{\pi}\frac{NV_{\mathrm{p}}}{\omega_{\mathrm{r}}L_{\mathrm{mp}}} \tag{4.45}$$

where I_{mp} is the V_{bus} side magnetizing current and L_{mp} is the V_{bus} side magnetizing inductance of the transformer.

The total target losses on the DHBSRC is less than 0.005 p.u., hence the target turn off current can be calculated by using (3.27). Eventually, L_{mp} can be calculated by using (4.45) which can be calculated 440 µH.

The leakage inductance of the transformer can be derived by the relationship between leakage inductance (L_{rp}) and the self-inductance of the transformer, as follows:

$$k = \sqrt{1-\frac{L_{\mathrm{rp}}}{L_{\mathrm{sfs}}}} = \sqrt{1-\frac{L_{\mathrm{rs}}}{L_{\mathrm{sfp}}}} \tag{4.46}$$

where k is the coupling coefficient of a transformer, L_{sfp} is the self-inductance of the transformer on the inverter bus side, and L_{sfs} is the self-inductance of the transformer on the partial voltage side.

The relationship of L_{sfp} and L_{sfs} can be defined by the mutual inductance as follows:

$$M = k\sqrt{L_{\mathrm{sfp}} L_{\mathrm{sfs}}} \tag{4.47}$$

where M is the mutual inductance.

The winding turns ratio N can be reorganized by the inverter side and partial voltage side self-inductance as follows:

$$N = \frac{N_{\mathrm{p}}}{N_{\mathrm{s}}} = \sqrt{\frac{L_{\mathrm{sfp}}}{L_{\mathrm{sfs}}}} \tag{4.48}$$

Using (4.47) and (4.48), the magnetizing inductance can be given as:

$$L_{\mathrm{mp}} = kL_{\mathrm{sfp}} \tag{4.49}$$

Equations (4.46) and (4.48) show that increasing of the leakage inductance can limit the magnetizing inductance. Furthermore, a higher value of leakage inductance can cause the higher voltage drop which yields the increasing of the transformer losses. Therefore, to achieve the target magnetizing inductance which is 440 µH, h is chosen as 20.

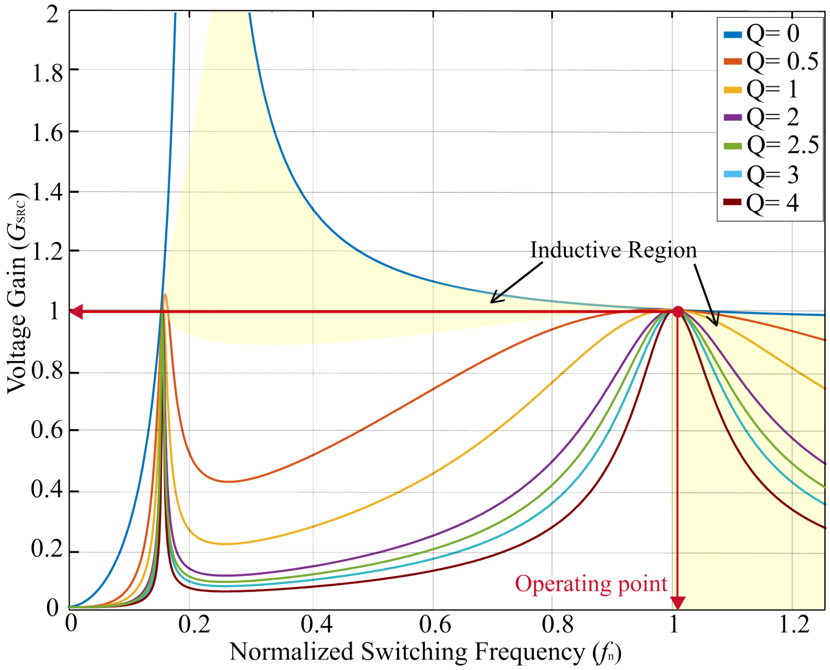


Figure 4.12: Gain function of DHBSRC in different quality factor @h =20.

After selecting h, the quality factor Q should be calculated. The gain function in (4.43) when $h = 20$ is plotted in Fig. 4.12. The DHBSRC should be operated in the ZVS region where the switching losses can be minimized. To achieve the ZVS, the current of the DHBSRC (i_{rp}) should lag behind the voltage of DHBSRC (V_{rp}) based on the switching losses processes as shown in Fig. 3.10. The phase angle between i_{rp} and V_{rp} can be analyzed by expressing the input impedance (Z_{in}) of the DHBSRC that shown in Fig. 4.11. The Z_{in} can be expressed as follows:

$$Z_{\text{in}} = |Z_{\text{in}}|e^{j\phi_{\text{z}}} \tag{4.50}$$

where Z_{in} is the input impedance of the DHBSRC and ϕ_{z} is the phase angle between i_{rp} and V_{rp}. Equation (4.50) shows that Z_{in} varies by ϕ_{z} ($-\pi/2 < \phi_{\text{z}} < 2\pi$): i) when ϕ_{z} is greater than 0, Z_{in} is inductive, ii) ϕ_{z} lower than 0, Z_{in} is capacitive, and iii) ϕ_{z} is equal to 0, Z_{in} is resistive. The capacitive and inductive regions can be recognized by the locus of the resonant peaks (where $\phi_{\text{z}} = 0$) of the gain curve as depicted in Fig. 4.12. The gain curve shows that ZVS can be achieved when the phase angle Z_{in} is greater than zero where the DHBSRC's current (i_{rp}) lag behind it's applied voltage (V_{rp}). In the previous section, optimal switching frequency, f_{SRC} is chosen as 200 kHz by considering the trade-off between the volume and losses. Therefore, the resonant frequency of the DHBSRC is selected as 195 kHz to achieve the ZVS. The operating point of the DHBSRC is highlighted in Fig. 4.12.

The rest of the DHBSRC parameters can be calculated by using the relationships of h and Q. The V_{bus} side resonant inductance L_{rp} can be derived from (4.39), as follows:

$$L_{\text{rp}} = \frac{L_{\text{mp}}}{h} \tag{4.51}$$

Eventually, C_{rp} can be calculated as 30 nF according to (4.42). Considering C_{rp} at the maximum load condition of R_{e}, the full load condition occurs (when $V_{\text{bus}} - V_{\text{DCx}} \approx V_{\text{p}}$ and $I_{\text{fx}} =$ 11 A). Using (4.37), the results can be obtained as 70 Ω. Using the obtained values of R_{e}, L_{rp}, and C_{rp}, the quality factor Q can be selected as 2.5.

In addition, the magnetizing inductance on the V_{p} side also can be calculated by using the relationship of the turn ratio of the transformer as follows:

$$L_{\text{ms}} = \frac{L_{\text{mp}}}{N^2} \tag{4.52}$$

Following the design step of the DHBSRC, the parameters of the DHBSRC can be determined as organized in Table. 4.4. In addition the parameter design of the DHBSRC is organized by the flowchart, depicted in Fig. 4.13.

4.3.3 Control scheme of DC-transformer stage

A control block of the DHBSRC is depicted in Fig. 4.14. The DC input and inverter side bus power are measured to select the active bridge of the DHBSRC based on Table. 4.1. If P_{bus} is greater than P_{DCx}, the duty cycle is given to the inverter bus side switches (S_{brp} and S_{trp}), and the partial voltage side switches (S_{brs} and S_{trs}) operate as a passive rectifier. On the other hand, if P_{bus} is smaller than P_{DCx}, the duty cycle is given to the switch sets of [S_{brs} and S_{trs}], and [S_{brp} and S_{trp}] work as the rectifier. Finally, the DHBSRC can control V_{p} with its switching.

Table 4.4: Selected DHBSRC design parameters

Parameters	Symbol	Value	Unit
Transformer turns ratio	N	2.5	-
DHBSRC switching frequency	f_{SRC}	200	kHz
Quality factor	Q	3	-
Inductance ratio	h	20	-
V_{bus} side resonant inductance	L_{rp}	22	μH
V_{bus} side resonant capacitance	C_{rp}	30	nF
V_{p} side resonant inductance	L_{rs}	3.6	μH
V_{p} side resonant capacitance	C_{rs}	183	nF
V_{bus} side magnetizing inductance	L_{mp}	434	μH
V_{p} side magnetizing inductance	L_{ms}	76	μH

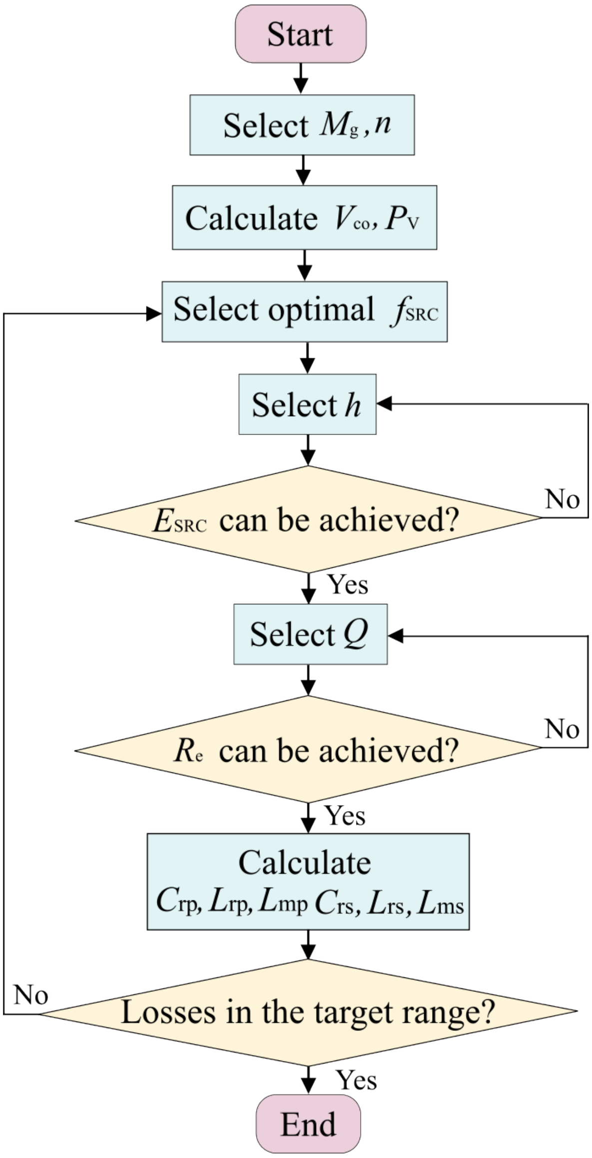


Figure 4.13: Flow chart for DBSRC design.

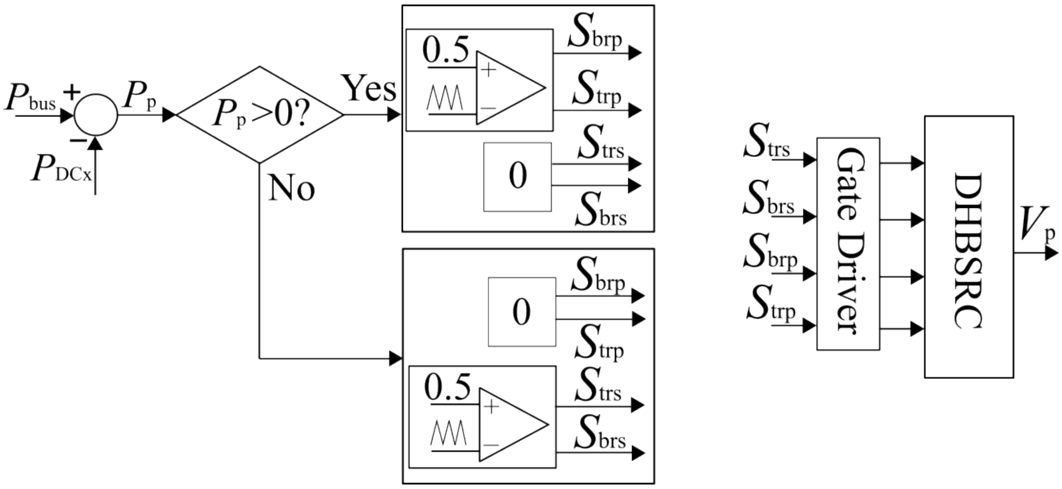


Figure 4.14: Control block of the DHBSRC stage.

4.3.4 Transformer design

A precise transformer design is required in order to achieve the expected behavior of the DHBSRC. The transformer material and core geometry should be selected first, to design the transformer. There are three materials: 3C96, 3C95, and 3C94, can be considered for 200 kHz switching frequency. 3C96, 3C95, and 3C94 are the MnZn based ferrites and the material properties of them are shown in Fig. 4.15.

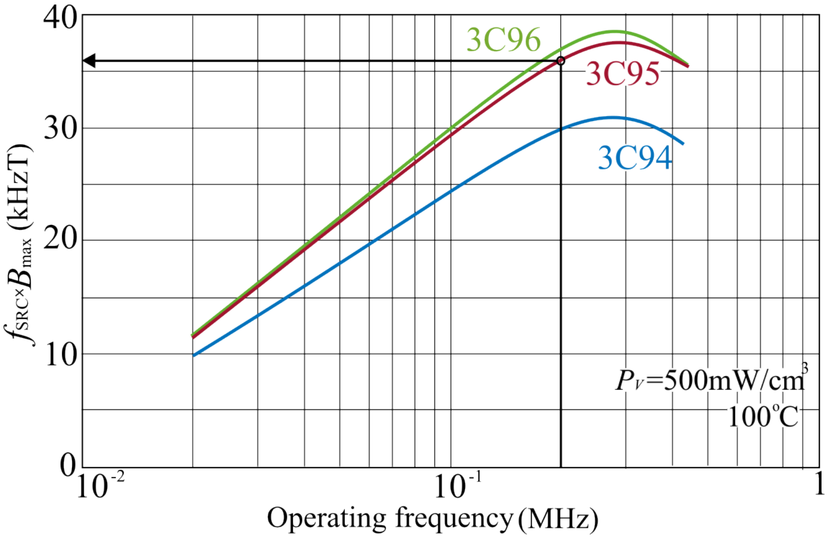


Figure 4.15: Core material properties of 3C96, 3C95, and 3C94.

The value of $f_{SRC}B_{max}$ is proportional to the self-inductance ($L_s = L_r + L_m$). Hence, the highest self-inductance can be achieved with 3C95 material which has highest $f_{SRC}B_{max}$. However, based on the material properties in the datasheet, the permeability μ of 3C95 material changes sharply with temperature. On the other hand, 3C94 does not get affected too much by the temperature change, but it could be difficult to achieve the target inductance because of low $f_{SRC}B_{max}$. Therefore, in this study, 3C95 material is selected which has stable μ at different temperatures and close $f_{SRC}B_{max}$ curve compared to 3C95 material.

The Stein-Metz coefficients in (4.29) can be determined after the transformer core material has been selected. Fig. 4.16 shows the core losses at different flux densities and switching frequencies from the data sheet. Equation (4.29) can be solved by using the values of flux density (B) and core losses per unit volume (P_V) at three different switching frequencies. The selected points in the figure are: i) $B = 40$ mT, $P_V = 70$ kW/m^3 at 400 kHz, ii) $B = 80$ mT, $P_V = 80$ kW/m^3 at 200 kHz, iii) $B = 200$ mT, $P_V = 300$ kW/m^3 at 100 kHz. Using these values, the calculated Stein-Metz coefficients K_c, α, and β are 1.74, 2.76, and 0.05, respectively.

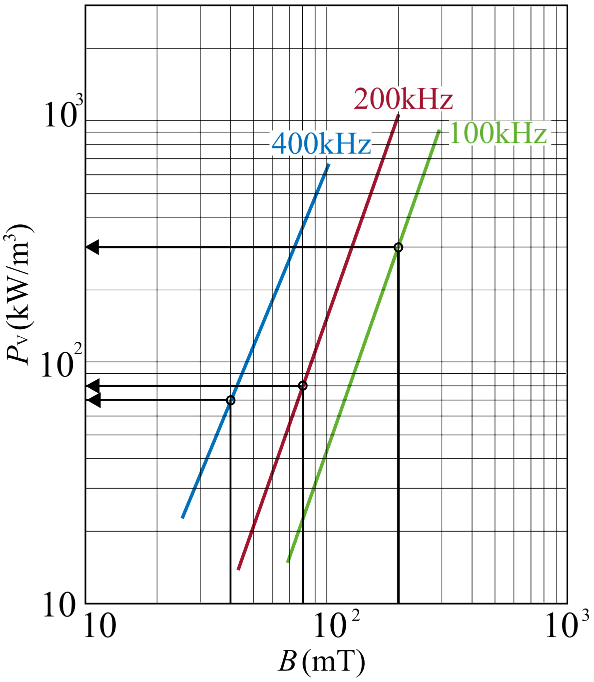


Figure 4.16: Core losses in different flux density and switching frequencies.

In order to use (4.27) for selecting core geometry, the optimal flux density B_o should be decided first. B_o can be derived as follows:

$$B_o = \frac{(h_c k_a \Delta T)^{\frac{2}{3}}}{1.57(\rho_w k_w k_u)^{\frac{1}{12}}(k_c K_{core} f_{SRC}^{\alpha})^{\frac{7}{12}}} \left[\frac{K_v f_{SRC}}{VA_{SRC}}\right]^{\frac{1}{6}} \tag{4.53}$$

where k_a, k_c and k_w are the constant coefficients, ΔT is the temperature rise, ρ_w is the resistivity of the copper ($\rho_w = 1.72$ nΩm), k_u is the window utilization factor, K_v is the voltage waveform factor and VA_{SRC} is the VA rating of the SRC. The temperature rise is set to $\Delta T = 65$ with a 20 % margin. The typical values of the constant coefficients are $k_a = 40$, $k_c = 5.6$, $k_w = 10$ [110]. The DHBSRC performs the open loop switching at 0.5 duty cycle, so K_v can be defined as 2. The value of VA_{SRC} is the same as the maximum P_p that the DHBSRC can handle, which is 3 kW.

After calculating B_o by (4.53), the result should be compared with B_{sat} in the material datasheet to decide B_{max}. Deciding the higher one as B_{max} and putting B_{max} into (4.27), the area of the core can be calculated as 0.0036 m^2. The commercial core is selected with a volume close to the geometry calculation result (0.0036 m^2). The selected core information is shown in Fig. 4.17. An E core based on 3C95 material is selected for the DHBSRC transformer. The A_c of the selected core is 0.0032 m^2. A detailed core geometry of the selected E-core is shown in Fig. 4.17.

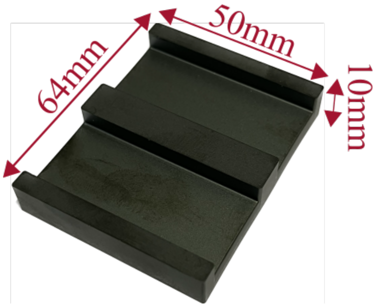


Figure 4.17: Selected commercial core: E64/10/50 @ferroxcube.

Table 4.5: Properties of selected transformer core: E64/10/50

Properties	Symbol	Value	Unit
Length	l	64	mm
Width	w	50	mm
height	h	10	mm
Effective Volume	V_{e}	40700	mm^3
Effective length	l_{e}	80	mm
Effective Area	A_{e}	519	mm^2
Mass of core	m	100	g

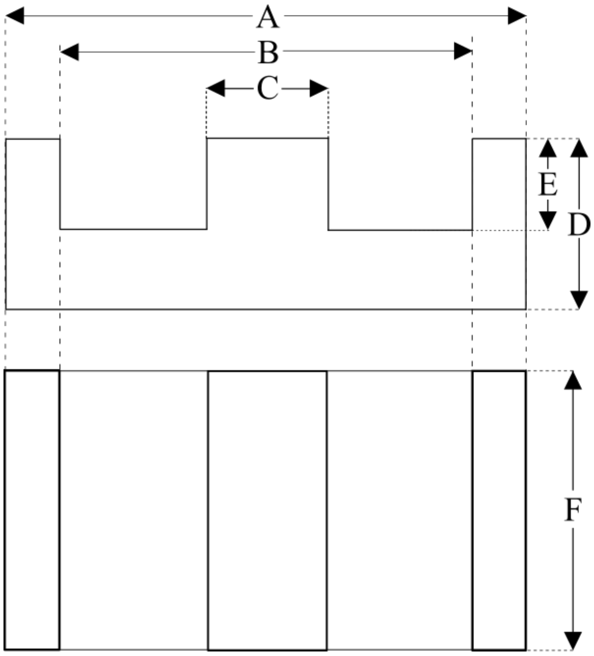


Figure 4.18: Geometry of selected transformer core: E64/10/50 @ferroxcube.

Table 4.6: Dimensions of selected transformer core: E64/10/50 @ferroxcube

	Value	Unit
A	64	mm
B	53.8	mm
C	10.2	mm
D	10.2	mm
E	5.1	mm
F	50.8	mm

After selecting the material and geometry, the current density J_{o} of the transformer should be calculated in order to select the wire area A_{w} for the transformer winding. J_o can be calculated from the winding area product A_{p}, which can be expressed as follows:

$$A_{\mathrm{p}} = \frac{\sqrt{2}VA_{\mathrm{SRC}}}{2f_{\mathrm{SRC}}B_{\mathrm{o}}k_{\mathrm{f}}K_{\mathrm{t}}\sqrt{k_{\mathrm{u}}\Delta T}} \tag{4.54}$$

where $K_{\mathrm{t}} = \sqrt{h_{\mathrm{c}}k_{\mathrm{a}}/\rho_{\mathrm{w}}k_{\mathrm{w}}}$.

The current density J_o can be calculated by reorganizing (4.54) as follows:

$$J_\mathrm{o} = \left(\frac{K_\mathrm{t} \sqrt{\frac{0.5\Delta T}{k_\mathrm{u}}}}{A_\mathrm{p}} \right)^{\frac{1}{8}} \tag{4.55}$$

Finally, A_w can be calculated as follows:

$$A_\mathrm{w} = \frac{I_\mathrm{p}}{J_\mathrm{o}} \tag{4.56}$$

In order to wind the transformer, the wire diameter $l_\mathrm{w} = 2.5$ mm is selected based on the calculation.

The number of the turns on the V_bus side of the transformer N_p, also can be calculated as following equation:

$$N_\mathrm{p} = \frac{V_\mathrm{bus}}{2 f_\mathrm{SRC} B_\mathrm{o} A_\mathrm{e}} \tag{4.57}$$

where A_e is the effective area of the selected core which is in Table. 4.5.

From (4.57), V_bus side turns $N_\mathrm{p} = 15$. By using the voltage relationship between V_bus and V_p of the transformer, turns ratio N can be decided as 2.5. Therefore, the V_p side turns N_s can be calculated as N_p/N.

The core losses of the transformer P_ct can be calculated as follows:

$$P_\mathrm{ct} = \Lambda_\mathrm{co} K_\mathrm{c} f_\mathrm{SRC}^{\alpha} \Delta B^{\beta} \tag{4.58}$$

where Λ_co can be calculated by using (4.28) and parameters in Table. 4.5. The calculation using (4.58) results in $P_\mathrm{ct} = 1.2$ W.

The copper losses of the transformer occur in the resistance of the winding. The DC resistances of the transformer can be calculated as follows:

$$R_\mathrm{dcp} = N_\mathrm{p} MLT_\mathrm{p} \rho_\mathrm{w} I_\mathrm{p}^2 \tag{4.59}$$

$$R_\mathrm{dcs} = N_\mathrm{s} MLT_\mathrm{s} \rho_\mathrm{w} n I_\mathrm{p}^2 \tag{4.60}$$

where R_dcp is the V_bus side DC resistance of the transformer, R_dcs is the V_p side DC resistance, MLT_p and MLT_s are the V_bus side and V_p side mean length of the turns. MLT_p and MLT_s can be calculated by using the core geometry in Table. 4.5 and using the wire diameter derived from (4.56).

When a high frequency resonant current flows through the transformer, the current density in the center of the conductor decreases but the current density near the surface of the conductor increases. The current flow therefore is limited to the surface region of the conductor with a skin depth which can be expressed as:

$$\delta = \frac{1}{\sqrt{\pi f_{\text{SRC}} \mu \rho co}} \tag{4.61}$$

Using (4.61), the AC resistances of the windings due to the skin effect can be calculated as follows:

$$R_{\text{acp}} = R_{\text{dcp}} \left(1 + \frac{(r_{\text{w}}/\delta)^4}{48 + 0.8(r_{\text{w}}/\delta)^4}\right) \tag{4.62}$$

$$R_{\text{acs}} = R_{\text{dcs}} \left(1 + \frac{(r_{\text{w}}/\delta)^4}{48 + 0.8(r_{w}/\delta)^4}\right) \tag{4.63}$$

Finally, the copper losses of the transformer considering the eddy current effect can be calculated as follows:

$$P_{\text{cu}} = I_{\text{p}}^2 R_{\text{acp}} + NxI_{\text{p}}^2 R_{\text{acs}} \tag{4.64}$$

where R_{acp} and R_{acs} are the DC resistance of the V_{bus} side and V_{p} side winding.

Therefore, the copper losses of the transformer at the rated P_{p} can be calculated by using (4.64) as $P_{\text{cu}} = 11$ W.

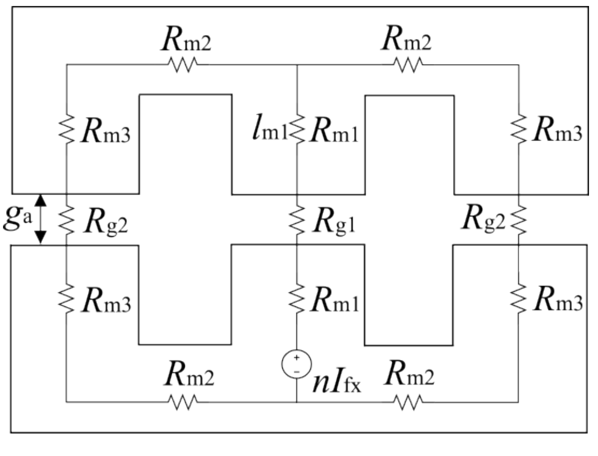


Figure 4.19: Equivalent reluctance of the transformer.

Finally, the self-inductance (L_{sf}) should be calculated in order to accurately design the transformer to match the resonant tank parameters of the DHBSRC in Table 4.4. The inductance can be calculated from the reluctance of the transformer as shown in Fig. 4.19. The reluctance can be calculated as follows:

$$R_{\mathrm{mk}} = \frac{l_{\mathrm{mk}}}{\mu_{\mathrm{r}}\mu_0 A_{\mathrm{mk}}} \tag{4.65}$$

where $R_{\mathrm{mk}}|_{\mathrm{k}=1,2,3}$ are the reluctance of the transformer core. l_{mk} is the distance between each part of the core, μ_r is the permeability of the material, μ_0 is the air permeability, and A_{mk} is the cross sectional area of the core. The detailed information of l_{mk} and A_{mk} is shown in Fig. 4.20.

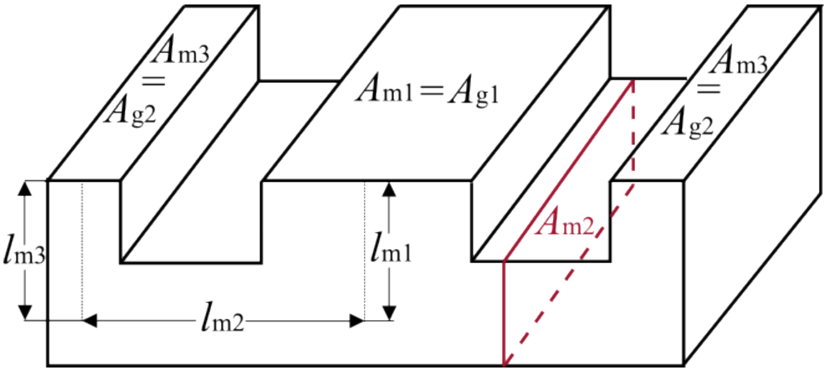


Figure 4.20: l_{mx} and A_{mk} information for reluctance calculation.

Using the geometry data in Table. 4.6, l_{mk} can be calculated as follows:

$$\begin{cases} l_{\mathrm{m1}} = l_{\mathrm{m3}} = \dfrac{\mathrm{E}+\mathrm{D}}{2} \\ l_{\mathrm{m2}} = \dfrac{\mathrm{A}+\mathrm{B}}{4} \end{cases} \tag{4.66}$$

A_{mk} also can be calculated by using the geometry data in Table. 4.6 which can be written as follows:

$$\begin{cases} A_{\mathrm{m1}} = \mathrm{CF} \\ A_{\mathrm{m2}} = \dfrac{\mathrm{A}-\mathrm{B}}{2}\mathrm{F} \\ A_{\mathrm{m3}} = (\mathrm{D}-\mathrm{E})\mathrm{F} \end{cases} \tag{4.67}$$

Furthermore, the reluctance appears at the airgap (g_{a} c.f. Fig. 4.19) between the two cores. The reluctance of the airgap can be calculated as follows:

$$R_{\mathrm{gy}} = \frac{g_{\mathrm{a}}}{\mu_0 A_{\mathrm{gy}}} \tag{4.68}$$

where $R_{\mathrm{gy}}|_{\mathrm{y}=1,2}$ is the airgap reluctance, and g_{a} is the distance of the airgap. In this study, the airgap between two cores is $g_{\mathrm{a}} = 0.7$ mm. A_{gy} is the cross section of the two cores that depicted in Fig. 4.20. It should be noted that $A_{g1} = A_{m1}$ and $A_{g2} = A_{m3}$.

The total equivalent circuit can be simplified and redrawn as in Fig. 4.21. Hence, the total equivalent reluctance of the transformer can be calculated as:

$$R_{me} = 2R_{m1} + R_{m2} + R_{m3} + R_{g1} + R_{g2} \tag{4.69}$$

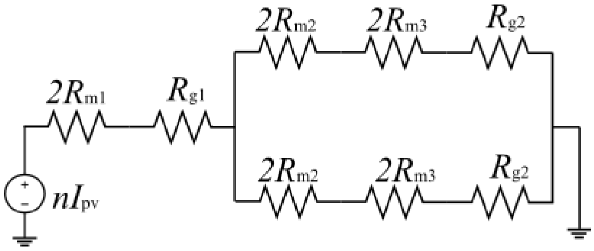


Figure 4.21: Simplified equivalent circuit of the transformer.

From (4.69), V_{bus} side self inductance L_{sfp} of the transformer can be calculated as follows:

$$L_{sfp} = L_{mp} + L_{rp} = \frac{N_p^2}{R_{me}} \tag{4.70}$$

where L_{sfp} is the V_{bus} side self inductance of the transformer. Hence, the V_{bus} side self inductance can be calculated $L_{sf} = 467$ µH.

The V_{bus} side magnetizing inductance can be calculated by substituting the V_{bus} side resonant inductance from (4.69). The V_{bus} side resonant inductance can be calculated as follows:

$$L_{rp} = \frac{\mu_0 N_p^2 MLT}{h_i} \left(\frac{b_1 + b_2}{3} + b_g \right) \tag{4.71}$$

where b_1 is the average width of the V_{bus} side turns, b_2 is the average width of the V_p side turns, h_i is the height of the wires, and b_g is the gap between the wires. b_1 and b_2 can be estimated from A_w, N_p and N_s. h_i is the height of the winding, which is equal to $2E$. It is also assumed that the gap between the windings is $b_g = 0.1$.

Substituting the chosen values into (4.71), the V_{bus} side resonant inductance can be calculated $L_{rp} = 21$ µH. Therefore, by subtracting L_{rp} to L_{sfp}, the V_{bus} side magnetizing inductance can be calculated as $L_{mp} = 4\ 46$ µH. Using the V_{bus} side and V_p side magnetizing inductance relationship in (4.52), the V_p side magnetizing inductance can be calculated as $L_{ms} = 71.36$ µH. Furthermore, the resonant inductance also follows the same relationship as in (4.30, hence $L_{rs} = 3.36$ µH. Using the relationship in (4.42), the V_{bus} side and V_p side resonant capacitance can be calculated as $C_{rp} = 30$ nF, $C_{rs} = 183$ nF.

A Maxwell simulation is performed to validate the theoretical transformer design. The 3D Maxwell model of the DHBSRC transformer is shown in Fig. 4.22. The 3D geometries of the transformer used the same core geometries as in Table. 4.6. The V_{bus} and V_p side turns, wire width and air gap information in the simulation used the theoretical calculation results of $N_\mathrm{p} = 15$, $N_\mathrm{s} = 6$ and $g_\mathrm{a} = 0.7$ mm. Furthermore, the inner winding of the transformer is V_bus side turns N_p and the outer winding of the transformer is V_p side turns N_s.

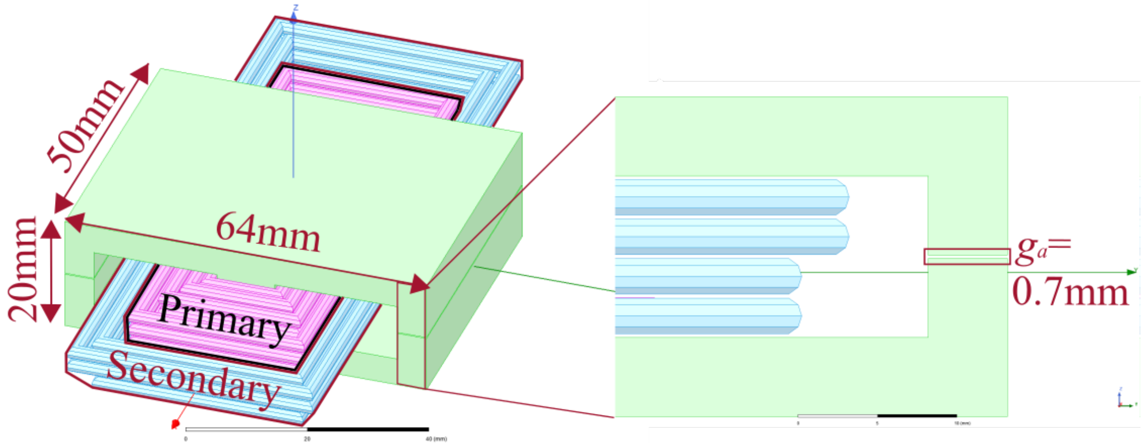


Figure 4.22: 3D-Maxwell model of the DHBSRC transformer.

First, the V_bus and V_p side self-inductances are calculated by the simulation. The simulation results give the V_bus side self inductance $L_\mathrm{sfp} = 463$ µH and the V_p side self inductance $L_\mathrm{sfs} =$ 77 µH. The magnetizing inductance of the Maxwell simulation can be calculated from the given results of L_sfp, L_sfs and the coupling coefficient (ε_cc) as follows:

$$\begin{cases} L_\mathrm{mp} = \varepsilon_\mathrm{cc} L_\mathrm{sfp} \\ \\ L_\mathrm{ms} = \varepsilon_\mathrm{cc} L_\mathrm{sfs} \end{cases} \tag{4.72}$$

where ε_cc is the coupling coefficient of the transformer. The ε_cc obtained from the simulation is 0.96. Using (4.72), it is possible to get magnetizing inductances as: $L_\mathrm{mp} = 444.5$ µH and $L_\mathrm{ms} = 74$ µH. Furthermore, the Maxwell simulation gives the resonant inductances: $L_\mathrm{rp} =$ 18.5 µH and $L_\mathrm{rs} = 3$ µH.

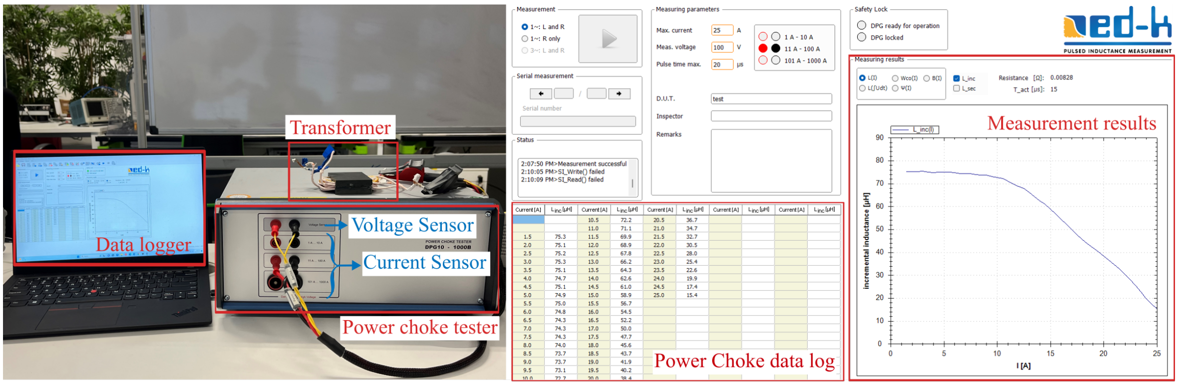
The transformer losses can also be derived from the Maxwell simulation. The core loss simulation of the transformer gives $P_\mathrm{ct} = 1.3$ W and the copper loss simulation of the transformer gives $P_\mathrm{cu} = 10$ W.

The transformer can be manufactured based on the turns and airgap that calculated and validated by the simulations. The wound transformer is depicted in Fig. 4.23. A 2.5 mm diameter litz wire is used for the winding.

The parameters of the transformer are characterized using a power choke tester as shown in the measurement set up in Fig. 4.24 (a). The voltage and current at the nominal operating condition for the transformer are applied by the power choke tester and the data is measured and recorded on the data logger from the laptop. Fig. 4.24 (b) shows the details of the power choke data logger. The measurement data is logged in the program and the transformer characteristics are plotted on the measurement results.

(a) (b) (c)

Figure 4.23: Result of the transformer winding: (a) side view (b) top view, (c) front view.



● 1~: L and R

Max. current 25 A

Meas. voltage 100 V

Pulse time max. 20 µs

● 11 A - 100 A

D.U.T. test

Inspector

Remarks

Resistance [Ω]: 0.00828

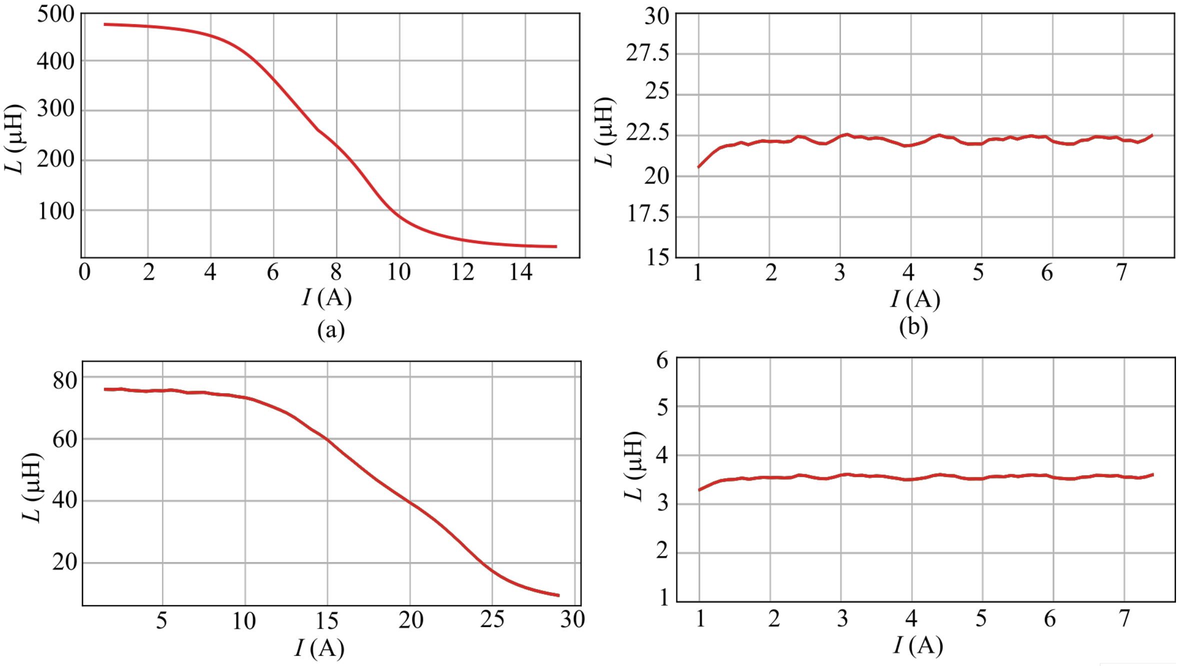
T_act [µs]: 15

```
2:07:50 PM>Measurement successful
2:10:05 PM>SI_Write() failed
2:10:09 PM>SI_Read() failed
```

Current [A]	L_{inc} [µH]	Current [A]	L_{inc} [µH]	Current [A]	L_{inc} [µH]	Current [A]	L_{inc} [µH]	Current [A]	L_{inc} [µH]
		10.5	72.2	20.5	36.7				
		11.0	71.1	21.0	34.7				
1.5	75.3	11.5	69.9	21.5	32.7				
2.0	75.1	12.0	68.9	22.0	30.5				
2.5	75.2	12.5	67.8	22.5	28.0				
3.0	75.3	13.0	66.2	23.0	25.4				
3.5	75.1	13.5	64.3	23.5	22.6				
4.0	74.7	14.0	62.6	24.0	19.9				
4.5	75.1	14.5	61.0	24.5	17.4				
5.0	74.9	15.0	58.9	25.0	15.4				
5.5	75.0	15.5	56.7						
6.0	74.8	16.0	54.5						
6.5	74.3	16.5	52.2						
7.0	74.3	17.0	50.0						
7.5	74.3	17.5	47.7						
8.0	74.0	18.0	45.6						
8.5	73.7	18.5	43.7						
9.0	73.7	19.0	41.9						
9.5	73.1	19.5	40.2						
10.0	72.7	20.0	38.4						

(a) (b)

Figure 4.24: Transformer characterization test set up: (a) test set up and (b) power choke data logger.



(a) (b)

(c) (d)

Figure 4.25: Transformer characteristics: (a) V_{bus} side self-inductance (b) V_{bus} side leakage inductance, (c) V_{p} side self-inductance, and (d) (c) V_{p} side leakage inductance.

The results of the transformer characterization are shown in Fig. 4.25. First, the self-inductance on the V_{bus} side of the transformer is plotted in Fig. 4.25 (a). The V_{bus} side self inductance measurement is 460 µH, which shows the 1.5 % error between the analytical results. The leakage inductance characteristic is shown in Fig. 4.25 (b). The measured leakage inductance is 22 µH, showing the 1 % error between the analytical results. The self-inductance on the V_{p} side of the transformer is shown in Fig. 4.25 (c). The V_{p} side self-inductance measurement is 75 µH which shows the 4.8 % error between the analytical results. The leakage inductance characteristic is shown in Fig. 4.25 (d). The measured leakage inductance is 3.5 µH, showing the 4 % error between the analytical results. The analytical, simulation and measurement results are organized in Table. 4.7. The transformer parameter results have less than 5 % errors, so the results show that the transformer model is valid. Finally, the flowchart of DHBSRC transformer design is shown in Fig. 4.26.

Table 4.7: Transformer parameter comparison between analysis, simulation, and measurement

Parameters	Symbol	Analysis	Simulation	measurement
V_{bus} side Self-inductance	L_{sfp}	467 µH	463 µH	460 µH
V_{bus} side magnetizing inductance	L_{mp}	446 µH	444.5 µH	438 µH
V_{bus} side Leakage inductance	L_{rp}	21 µH	18.5 µH	22 µH
V_{p} side Self-inductance	L_{sfs}	74.72 µH	77 µH	75 µH
V_{p} side magnetizing inductance	L_{ms}	71.36 µH	74 µH	71.5 µH
V_{p} side Leakage inductance	L_{rs}	3.36 µH	3 µH	3.5 µH
Core losses	P_{ct}	1.2 W	1.3 W	-
Copper losses	P_{cu}	11 W	10 W	-

4.4 Summary

In this section, the parameter design of the boost-type PVCs and the DC converter is carried out. To select the parameters for the boost-type PVCs, f_{s} is first selected by considering the trade-off between losses and volume of the boost-type PVCs. Inductance and capacitance are selected to achieve the target ΔI_{fx} and ΔV_{p}. The commercial components are selected based on the optimal component selection method. The current control of the boost-type PVCs is designed based on its small signal model. Finally, the design process is organized using the flowchart.

The parameters design of the DC transformer is also carried out. The f_{s} is also selected by considering the trade-off between losses and volume of the DC transformer. The resonant tank of the DHBSRC is selected based on its FHA model. The transformer is design so that the exact parameters can be compared with the design values for the FHA model. The transformer design is performed by analysis, simulation and validated by measurement. Magnetizing inductance, leakage inductance and transformer losses are calculated by theoretical analysis. The Maxwell simulation of the transformer model is performed to validate

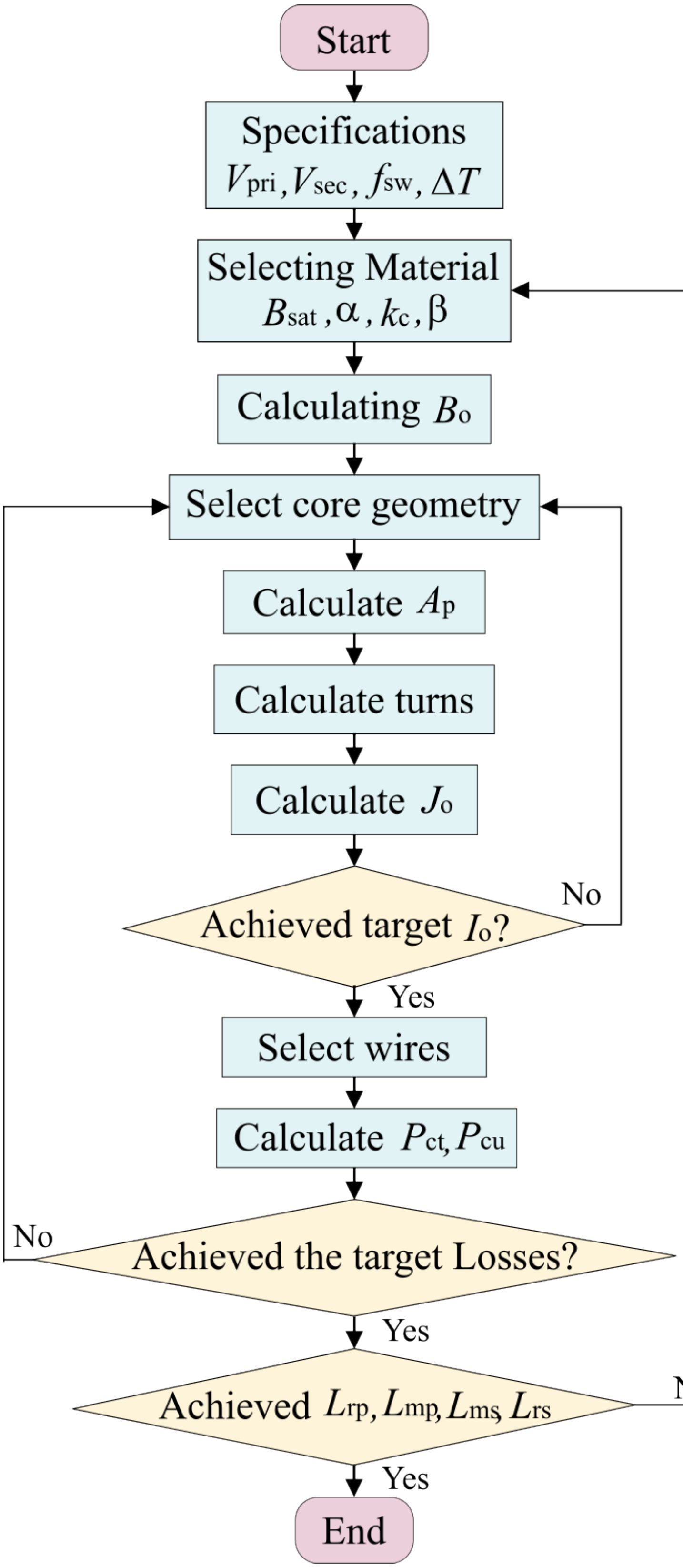


Figure 4.26: Flow chart of DHBSRC transformer design.

the theoretical model. Finally, the measurement results verify the validity of the analytical design of the transformer. The design process of the DHBSRC and the transformer is also given by the flowcharts.

5 Analysis and design of the multi-port PPC

According to the relationship in (3.4), P_p processed by the multi-port PPC can be changed by the operating point of V_DCx, I_DCx and V_bus. The efficiency of the proposed multi-port PPC can be different due to the amount of P_p processed by the multi-port PPC. Therefore, defining the amount of P_p at different operating points is important to analyze the power processing characteristics of multi-port PPC. Furthermore, to prove the impact of P_p processing capability on efficiency improvement, the relationship between the amount of P_p and efficiency should be analyzed quantitatively.

The partial power ratio (K_pr) is one of the key indicators that shows the amount of power being processed by the power electronics. By analyzing K_pr, it is possible to check the amount of PPP of the multi-port PPC at different operating points. Utilization factor (UF) is another key indicator to assess the amount of PPP. UF indicates the amount of power being processed by the semiconductor devices. By analyzing the UF, it is possible to quantify the power dissipation and stress of the semiconductor devices. Furthermore, the relationship between the PPP and the losses should be validated to check the effect of the PPP on the efficiency of the multi-port PPC. Based on the analysis of the switch losses, a heatsink can be properly designed to manage the thermal dissipation of the switches. Once the heatsink has been designed, the volume and weight of the multi-port PPC can be quantified. A volume and weight measurements proved detailed hardware information about the multi-port PPC. Therefore, a critical component that may affect the volume and weight of the multi-port PPC can be checked by using the volume and weight measurements.

5.1 Partial power processing characteristics of the multi-port PPC

In order to investigate the amount of the partial power processed by the multi-port PPC. the partial power ratio (K_pr) should be investigated. K_pr can be calculated using the following equation:

$$K_\mathrm{pr} = \frac{P_\mathrm{p}}{\Sigma P_\mathrm{DCx}} = \frac{V_\mathrm{p} \Sigma D_\mathrm{x} I_\mathrm{DCx}}{\Sigma V_\mathrm{DCx} I_\mathrm{DCx}} \tag{5.1}$$

where K_pr is the partial power ratio, P_p is the partial power, and ΣP_DCx is the total DC input power.

(5.1) shows that K_pr is the ratio between the total DC input power and the partial power. The amount of P_p can be changed by D_x as shown in Fig. 3.2. Furthermore, changing the turns ratio can also affect the amount of P_p that processed by the proposed PPC. To see the impact of N and D_x on P_p, (5.1) should be rearranged with respect to the equation of N and D_x.

Using the relationship in (3.8) and the voltage relationship of DHBSRC that $V_\mathrm{p} = V_\mathrm{bus}/N$, the equation can be reorganized with respect to V_DCx as follows:

$$V_{\mathrm{DCx}} = (1 - \frac{D_{\mathrm{x}}}{N})V_{\mathrm{bus}} \tag{5.2}$$

Equation of K_{pr} in (5.1) can be expressed by the equation related to D_{x} and N, which is obtained as follows:

$$K_{\mathrm{pr}} = \frac{V_{\mathrm{p}}\Sigma D_{\mathrm{x}} I_{\mathrm{DCx}}}{V_{\mathrm{bus}}\Sigma(1 - \frac{D_{\mathrm{x}}}{N})I_{\mathrm{DCx}}} \tag{5.3}$$

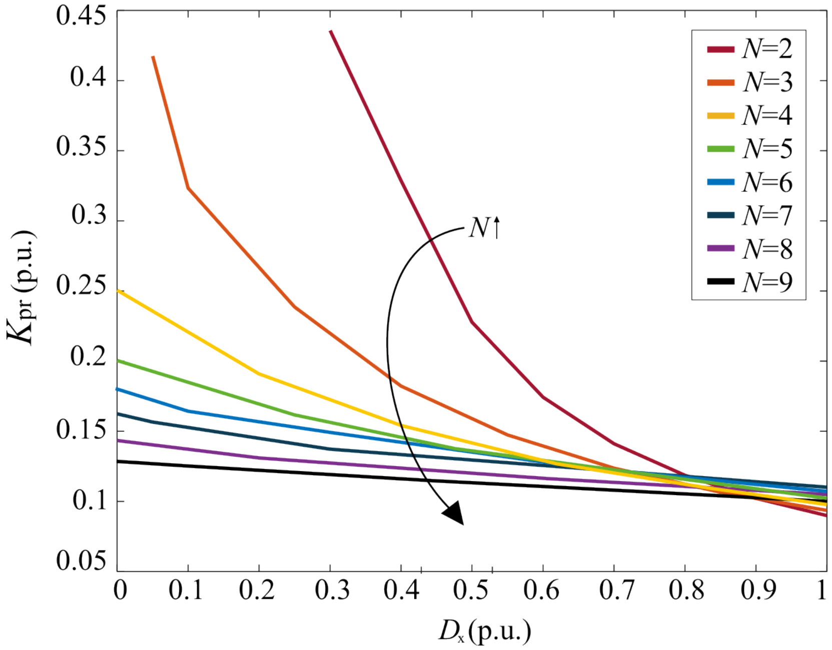


Figure 5.1: Partial power ratio (K_{pr}) variation depending on duty cycle (D_{x}) and turns ratio (N) of multi-port PPC.

The variation of K_{pr} with respect to D_{x} for different N values can be plotted as shown in Fig. 5.1. The relationships of (5.3) shows that K_{pr} value can be changed by the change of D_{x}. In the figure, K_{pr} decreases as D_{x} increases. This means that the amount of P_{p} processed by the multi-port PPC decreases at D_{x} increases, which validates the relationship in (3.5). In addition, lower K_{pr} can be achieved by higher N values. According to the voltage relationship ($V_{\mathrm{p}} = V_{\mathrm{bus}}/N$) of the DHBSRC, as N increases the value of V_{p} decreases, which eventually reduces the power processed by the PVP stage. However, due to the low value of V_{p}, K_{pr} is not significantly changed by change in D_{x}. In this study N is equal to 2.5 where the PPC has a wide D_{x} range from 0.1 to 1. Furthermore, K_{pr} changes from 0.42 to 0.1 which means the maximum 42 % of P_{DCx} can be processed by the proposed multi-port PPC.

The analysis of K_{pr} in different V_{DCx} and I_{DCx} conditions is shown in Fig. 5.3. In the graph, V_{DCx} range is from 1 to 0.6 because the possible voltage tracking range is limited by V_{p} as shown in (3.10). The analysis shows that K_{pr} decreases as V_{DCx} increases. This means that $V_{\mathrm{DCx}} \approx V_{\mathrm{bus}}$, the power processing of the multi-port PPC can be reduced. Reducing I_{DCx} also reduces K_{pr}. The less power the multi-port PPC can handle, the lower the DC input current. When V_{DCx} is equal to V_{bus}, S_{tx} of the boost type PVCs is always on and it bypasses I_{DCx} to

V_{bus} side. The DC transformer performs V_{p} control, but P_{p} is close to 0, when V_{DCx} is equal to V_{bus}. Hence, K_{pr} does not show a significant change because the less than 10 % of the total input power is handled by the multi-port PPC. On the other hand, the largest amount of power processing can be seen at $V_{\mathrm{DCx}} = 0.42$ p.u. and I_{DCx} is 1 p.u. (rated current). At this point, the DC transformer processes the maximum P_{p} due to the relationship between V_{DCx} and V_{bus} in (3.3). Furthermore, ΣP_{DCx} is reduced by the reduction of V_{DCx}. Therefore, the proportion of P_{p} relative to ΣP_{DCx} increases. Therefore, the DC transformer processes a maximum of P_{p} and 42 % of ΣP_{DCx} is processed by the multi-port PPC.

Using the (5.1) and $V_p = V_{\mathrm{bus}}/N$, (4.1) can be reorganized as follows:

$$L_{\mathrm{fx}} = \frac{(NV_{\mathrm{DCx}} - (D_{\mathrm{x}} - N)V_{\mathrm{bus}})T_{\mathrm{sw}}}{N\Delta I_{\mathrm{fx}}} \tag{5.4}$$

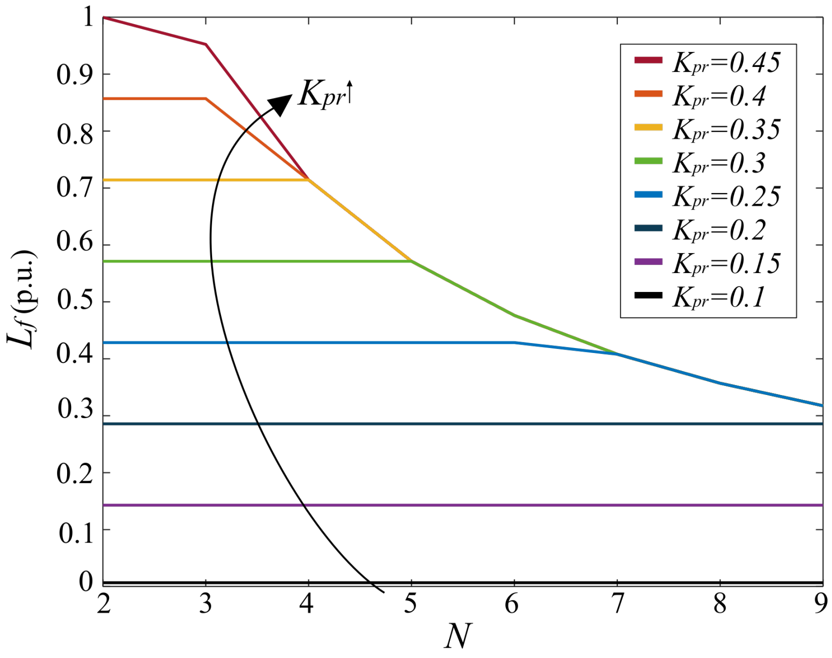


Figure 5.2: The optimal inductance (L_{f}) for different N at different K_{pr} conditions.

The optimal inductance for different N and K_{pr} conditions is plotted in Fig. 5.2, based on (5.4). The analysis shows that the optimal inductance can be very small due to the low power processed by the proposed PPC (only 10% of P_{pv} is processed by the proposed PPC), when $K_{\mathrm{pr}} = 0.1$. On the other hand, when $K_{\mathrm{pr}} = 0.45$, which is the maximum P_{p} that can be processed by the proposed PPC, the required inductance is between 0.4 and 1 p.u. The power handled by the PPC increases, so the PPC requires a higher inductance. In addition, by using higher N, the lower voltage V_{p} can be made according to the relationship of $V_{\mathrm{p}} = V_{\mathrm{bus}}/N$. Therefore the lower L_{fx} can be used by using higher N.

Utilization factor (UF) is another key indicator which shows the total utilized power by the semiconductor devices. In order to derive the UF equation, component stress factor (CSF) should be calculated as follows:

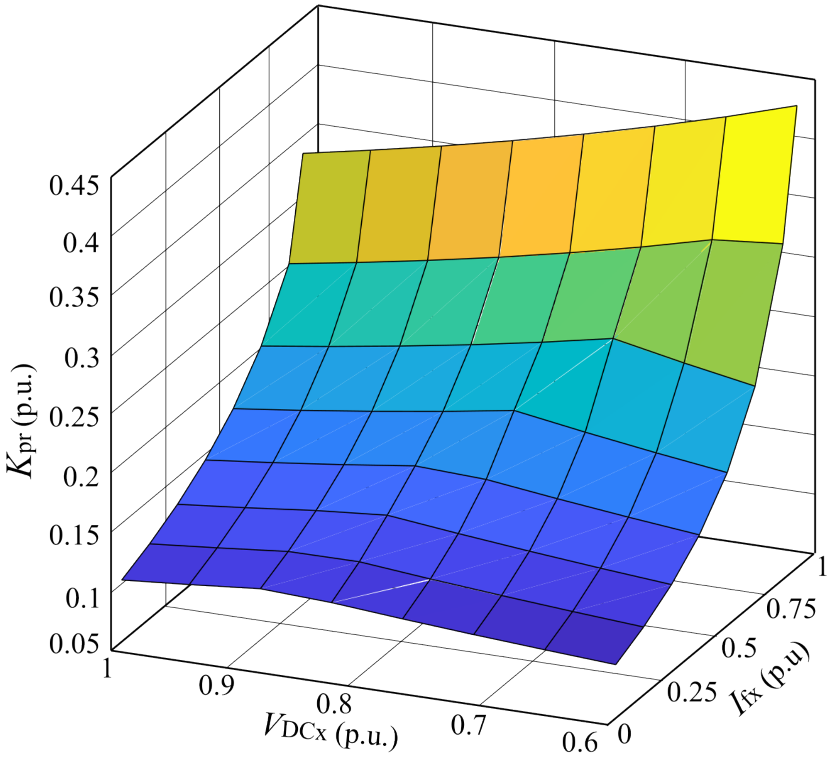


Figure 5.3: Partial power ratio (K_{pr}) of the multi-port PPC in different current and voltage conditions.

$$\mathrm{CSF} = \frac{P_{ss}}{\Sigma P_{DCx}} = \frac{\frac{1}{T_s}\int_0^{T_{on}} v_{dsx}(t)\, i_{dx}(t)\, dt}{\Sigma V_{DCx} I_{DCx}} = \frac{D_x V_{dx} I_{dx}}{\Sigma V_{DCx} I_{DCx}} \tag{5.5}$$

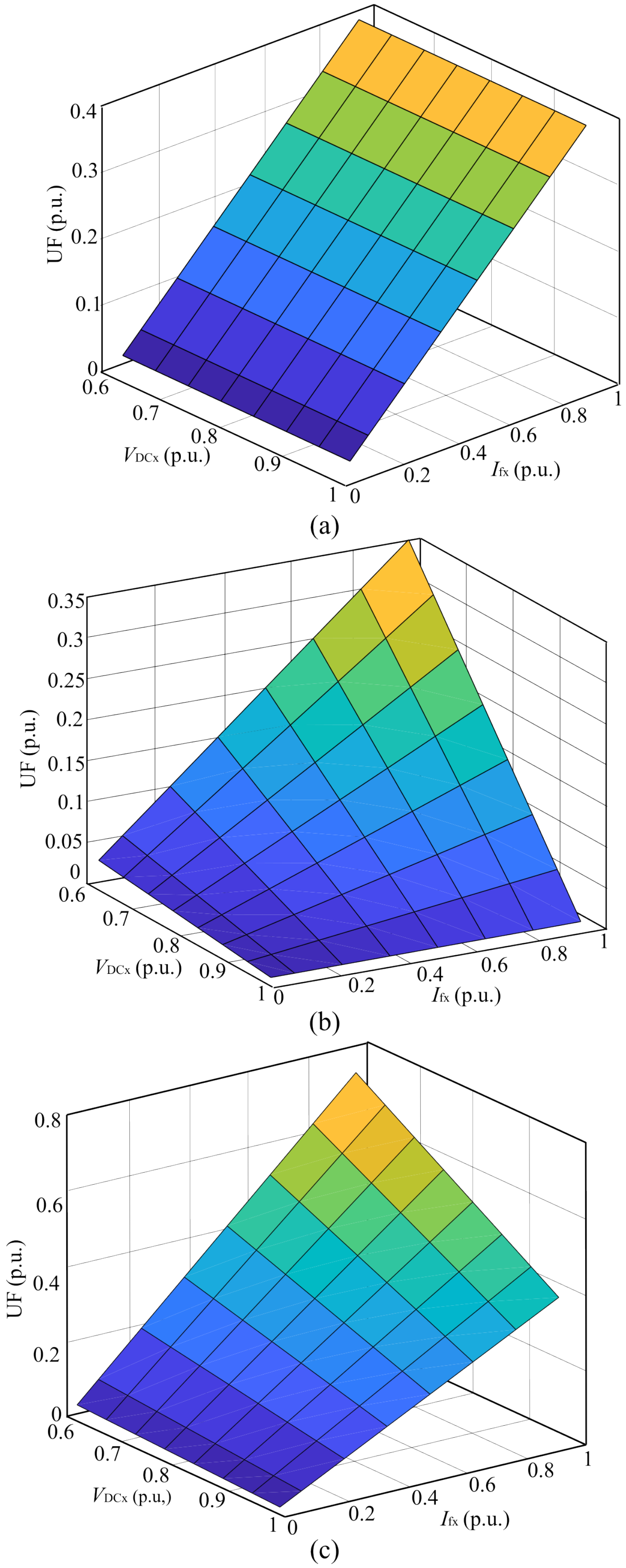
where P_{ss} is the processed power of the semiconductor devices, $v_{dsx}(t)$ is the drain-source voltage on each semiconductor device, $i_{dx}(t)$ is the drain current of each semiconductor devices, V_{dx} is the average voltage between each switch, and I_{dx} is the average current of each switch.

The CSF shows the average power dissipated by each semiconductor device. To calculate the total power dissipated by the semiconductor devices, the sum of the CSF should be calculated. Finally, UF can be expressed by the following equation:

$$\mathrm{UF} = \Sigma \mathrm{CSF} = \frac{\Sigma D_x V_{dx} I_{dx}}{\Sigma V_{DCx} I_{DCx}} \tag{5.6}$$

Equation (5.6) shows that UF is the ratio between the total processed power of the semiconductor devices and the total input power. Therefore, the amount of the utilized power by the semiconductor device can be characterized by the UF analysis. The UF of the multi-port PPC under different V_{DCx} and I_{DCx} conditions is shown in Fig. 5.4.

In Fig. 5.4 (a), the UF characteristics of the PVCs are plotted. The figure shows that V_{DCx} has no effect on the variation of the UF of the PVCs. The partial voltage $V_p = 150$ V is stiffly maintained by the DC transformer, so the voltage between the PVCs is not affected by the change of V_{DCx}. The variation of I_{DCx} only affects the variation of UF of the PVCs,



(a)

(b)

(c)

Figure 5.4: Utilization factor (UF) of the multi-port PPC in different current and voltage conditions: (a) UF of partial voltage converters (PVCs), (b) UF of DC transformer, and (c) UF of total system.

which has a proportional relationship between UF. The maximum UF can be seen at UF = 0.4 which means that maximum 40 % of ΣP_{DCx} is utilized by the semiconductor devices of PVCs.

Fig. 5.4 (b) shows the UF characteristic of the DC transformer. The analysis shows that an increase in V_{DCx} results in a decrease in UF. As described in (3.3), P_{p} decreases when V_{DCx} is close to V_{bus}. In addition, P_{p} at the DC transformer can be reduced by reducing I_{DCx}. Therefore, UF decreases proportionally to the decrease of I_{DCx}. The maximum UF can be seen UF = 0.35, which means that maximum 35 % of ΣP_{DCx} is utilized by the semiconductor devices of the DC transformer.

The UF of the entire multi-port PPC system is shown in Fig. 5.4 (c). Calculation of the ratio between the average CSF and ΣP_{DCx} shows that a maximum of 75 % of ΣP_{DCx} is utilized by the semiconductor devices of multi-port PPC.

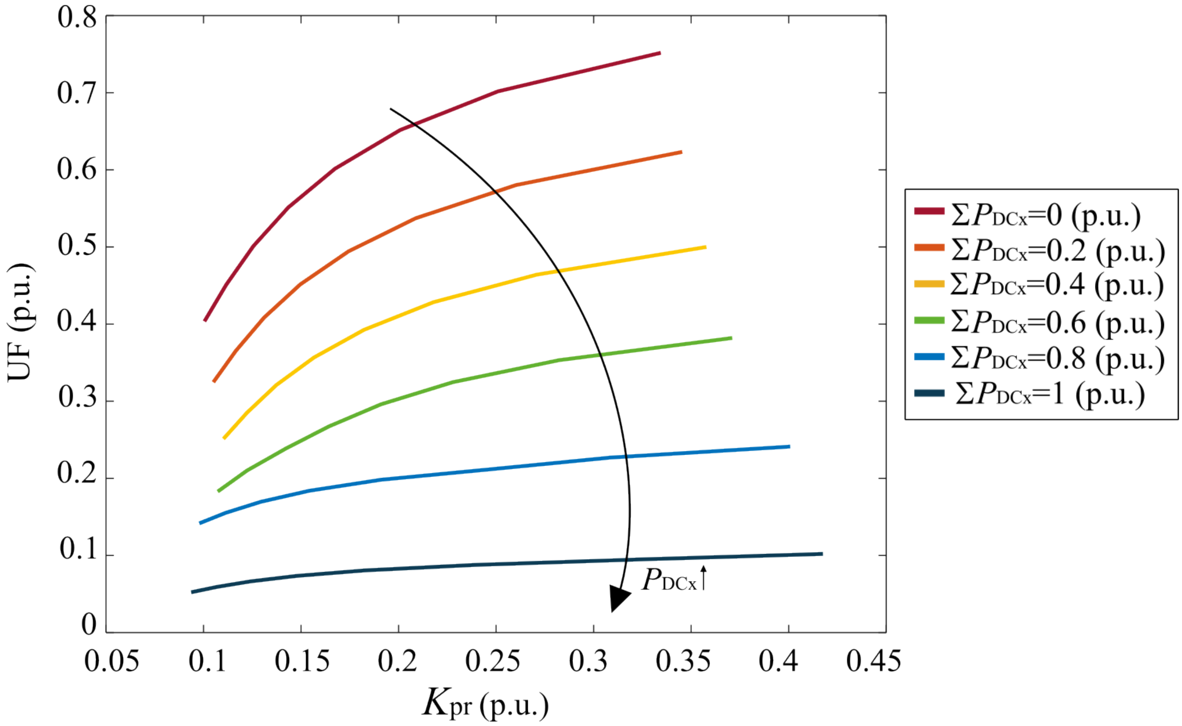


Figure 5.5: The relationship between ΣP_{DCx}, UF, and K_{pr} when $V_{\mathrm{bus}} = 400$ V.

The relationship between UF and K_{pr} in different ΣP_{DCx} conditions is plotted in Fig. 5.5. The analysis shows that UF and K_{pr} have a proportional relationship. As K_{pr} decreases, P_{p} of the multi-port PPC decreases, which yields the power utilization reduction of the semiconductor devices. Furthermore, according to the relationships in (3.4), the analysis shows that the processed power of the PPC can be reduced as ΣP_{DCx} increases.

5.2 Loss and efficiency analysis of the multi-port PPC

To validate the impact of PPP on efficiency improvement, the losses of the multi-port PPC should be analyzed. The multi-port PPC can flow P_{p} bidirectionally, which direction can be decided by following the relationship in (3.4). According to the operating principle of the DHBSRC that shown in Table. 4.1, the bidirectional P_{p} flow can be forced by changing the active bridge (V_{p} side or V_{bus} side) of the DHBSRC. Following (3.27), the losses of the DHBSRC can be different by changing the active bridges, either V_{p} side bridge or V_{bus} side bridge.

The equations of (3.17) and (3.27) can be used to calculate the semiconductor losses of the multi-port PPC. Using those two equations, the losses of each single semiconductor device can be calculated as:

$$P_{\mathrm{l}} = P_{\mathrm{con}} + P_{\mathrm{sw}} \tag{5.7}$$

where P_{l} is the semiconductor losses.

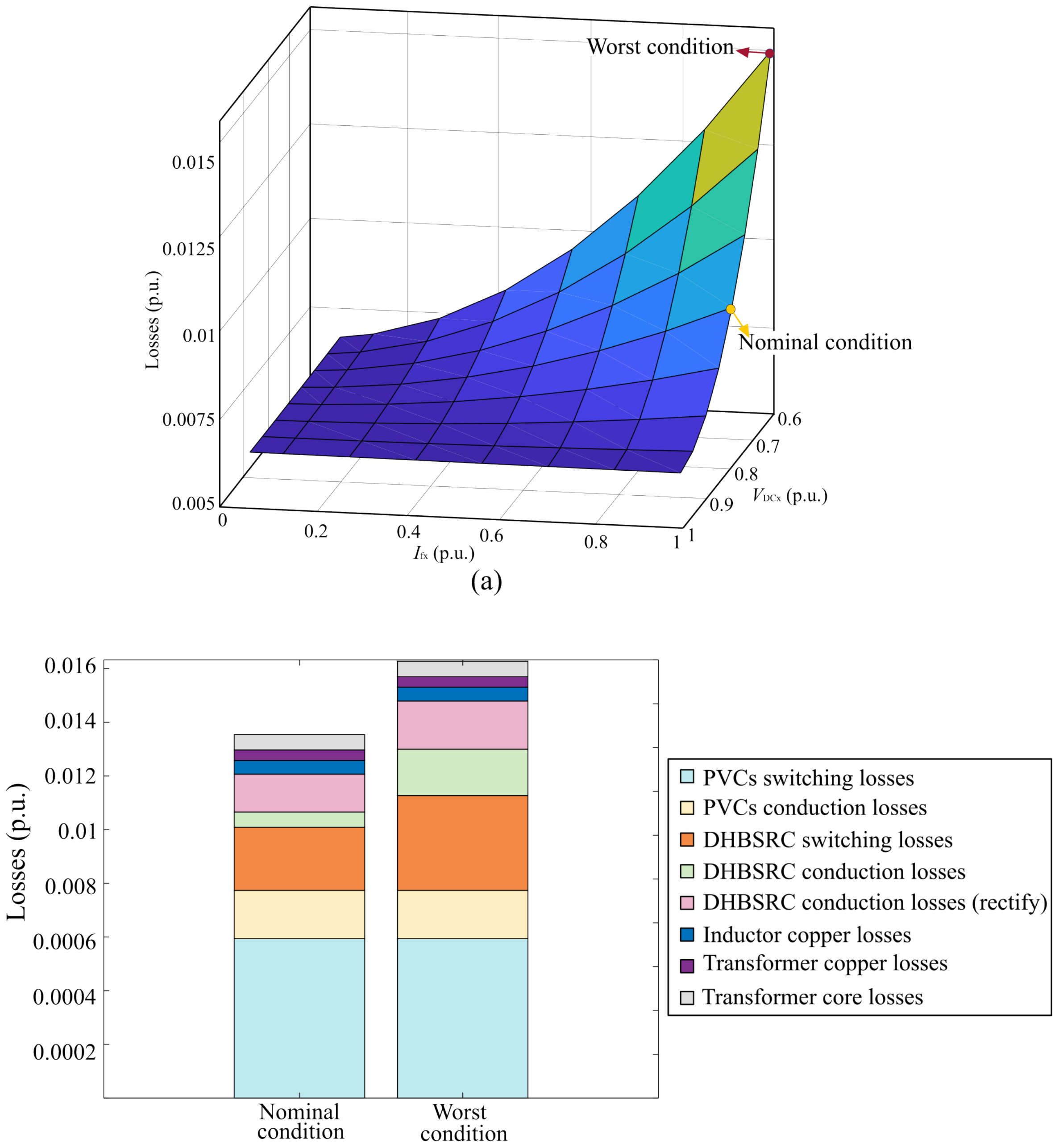
The losses of the single semiconductor device P_{l} can be calculated by adding the conduction and switching losses. Therefore, the total losses of the semiconductors can be calculated as:

$$P_{\mathrm{l(tot)}} = \Sigma P_{\mathrm{l}} = P_{\mathrm{l(st1)}} + P_{\mathrm{l(sb1)}} + \cdots + P_{\mathrm{l(stx)}} + P_{\mathrm{l(sbx)}} + P_{\mathrm{l(trs)}} + P_{\mathrm{l(brs)}} + P_{\mathrm{l(trp)}} + P_{\mathrm{l(brp)}} \tag{5.8}$$

where $P_{\mathrm{l(tot)}}$ is the total semiconductor losses of multi-port PPC, P_{l} is the semiconductor losses of each switch. The equation shows $P_{\mathrm{l(tot)}}$ can be calculated by adding losses of total semiconductor devices of the multi-port PPC. Finally, losses can be analyzed by using (5.8).

The semiconductor loss analysis of forward mode at different operating points is shown in Fig. 5.6 (a). When the DHBSRC is in the forward mode, the switches of V_{bus} side (S_{trp} and S_{brp}) are enabled. The voltage across switch sets of the [S_{trp} and S_{brp}] is equal to V_{bus}, but the partial current I_{p} can be processed by the PPP characteristics. To process the full voltage across S_{trp} and S_{brp}, 650 V level MOSFET is applied as shown in Table. 3.3. Furthermore, the voltage across the boost type PVCs is V_{p} and the 250 V level MOSFET are applied as shown in Table. 3.3. The analysis of forward mode shows maximum losses can be observed at the point of minimum V_{DCx} and maximum I_{fx}. The p.u. losses show that 1.5 % of the total power is dissipated by the semiconductor devices of the multi-port PPC in the forward mode. The minimum semiconductor losses can be observed when V_{DCx} is close to V_{bus} and its value is 0.6 %.

The forward mode losses of the nominal and worst operating conditions are shown in Fig. 5.6 (b). During the nominal operating condition, the semiconductor losses are 1.2 % of the rated power. The loss analysis of each stage of multi-port PPC also can be seen in the figure. According to the analysis results, the losses of the boost type PVC stages are 0.8 % and the losses of the DC-transformer stage are 0.4 % during the nominal operating condition. During the worst operating condition, as mentioned before, the total semiconductor losses are 1.5 %. In the worst operating condition, the losses of the boost type PVC stage are 0.8 % which

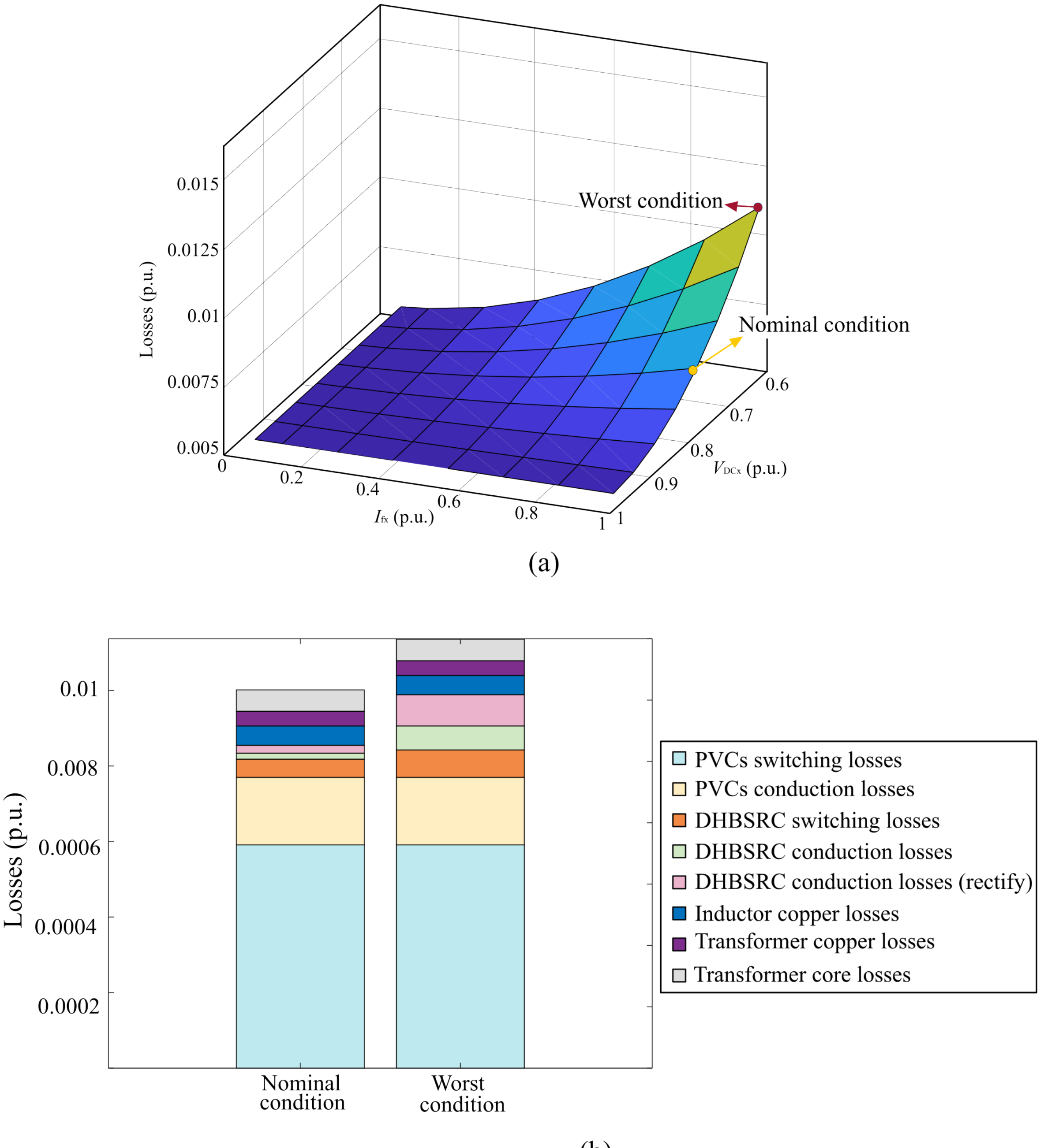


(a)

(b)

Figure 5.6: Forward mode loss analysis of multi-port PPC at different operating points: (a) forward mode losses at different operating points and (b) p.u. losses of the nominal and worst operating conditions.

is the same as the nominal operating condition. Comparing the two conditions, the current and voltage at the PVC stage are the same. However, the voltage gap between the DC input and inverter side bus ($V_{\text{bus}} - V_{\text{DCx}}$) is higher when the worst operating condition. According to the relationship in (3.4), the higher $V_{\text{bus}} - V_{\text{DCx}}$ makes the higher power processing by the DC-transformer. Therefore, the losses of the PVC stage does not change but the losses of the DC-transformer increases to 0.7 %.



(a)

(b)

Figure 5.7: Reverse mode loss analysis of multi-port PPC at different operating points: (a) reverse mode losses at different operating points and (b) p.u. losses of the nominal and worst operating conditions.

The semiconductor losses of the reverse mode at the different operating conditions are analyzed in Fig. 5.7 (a). When the DHBSRC is in the reverse mode, the switches of V_{p} side (S_{trs} and S_{brs}) are enabled. The voltage across the switch sets of [S_{trs} and S_{brs}] is V_{p}, and it is the same voltage level as the MOSFETs of the PVCs. The analysis of reverse mode shows that the maximum losses can also be observed at the point of minimum V_{DCx} and maximum I_{fx}. However, compared to the losses of the forward mode, the maximum losses of the reverse mode are reduced 45 %.

The nominal and worst operating conditions losses of the reverse mode are shown in Fig. 5.6 (b). The analysis shows that losses of the PVCs do not change compared to the forward mode losses. This is also due to the relationships of (3.4), where the current and voltage across the PVCs in the reverse modes are the same as those in the forward mode. However, the semiconductor losses of the nominal operating condition are 0.85 % which has 30 % losses reduction compared to the forward mode. As discussed before, V_{p} side switches of the DC-transformer make less semiconductor losses compared to V_{bus} side switches of it. Therefore, losses of the reverse mode can be reduced compared to the forward mode. Furthermore, the semiconductor losses of the worst operating condition of the reverse mode is 1.15 % which is 25 % higher than the semiconductor losses of the nominal condition, also by following the relationships of (3.4). The loss analysis of both modes shows that the amount of losses has the same tendency as the UF at the different operating condition. The lower losses can be observed at lower UF. The loss analysis proves that decreasing UF impacts on the decrease of the semiconductor losses of the multi-port PPC.

The forward and reverse mode efficiencies of the multi-port PPC can be analyzed as shown in in Fig. 5.8, based on the loss analysis. Firstly, the forward mode efficiency is shown in Fig. 5.8 (a). The maximum efficiency of the forward mode is estimated to be 98.9 % and the efficiency of the nominal operating point can be calculated as 98.6 %. The operating point of the maximum efficiency can be observed at the same point of the minimum UF. The efficiency decreases as the difference between V_{bus} and V_{DCx} becomes larger. In this case, the larger amount of P_{p} is processed by the DC transformer stage. Therefore, more power is dissipated compared to the point where V_{bus} is close to V_{DCx}. The efficiency of the reverse mode is shown in Fig. 5.8 (b). The maximum efficiency of the reverse mode is estimated to be 99.45 % and the efficiency of the nominal condition is 99.1 %. As discussed in the loss analysis, the reverse mode efficiency is higher than the forward mode efficiency due to the less power dissipation by the DC transformer stage in the reverse mode. The maximum efficiency can be observed at the point of the minimum UF. In addition, the higher voltage difference between V_{bus} and V_{DCx}, the more power dissipation can be observed.

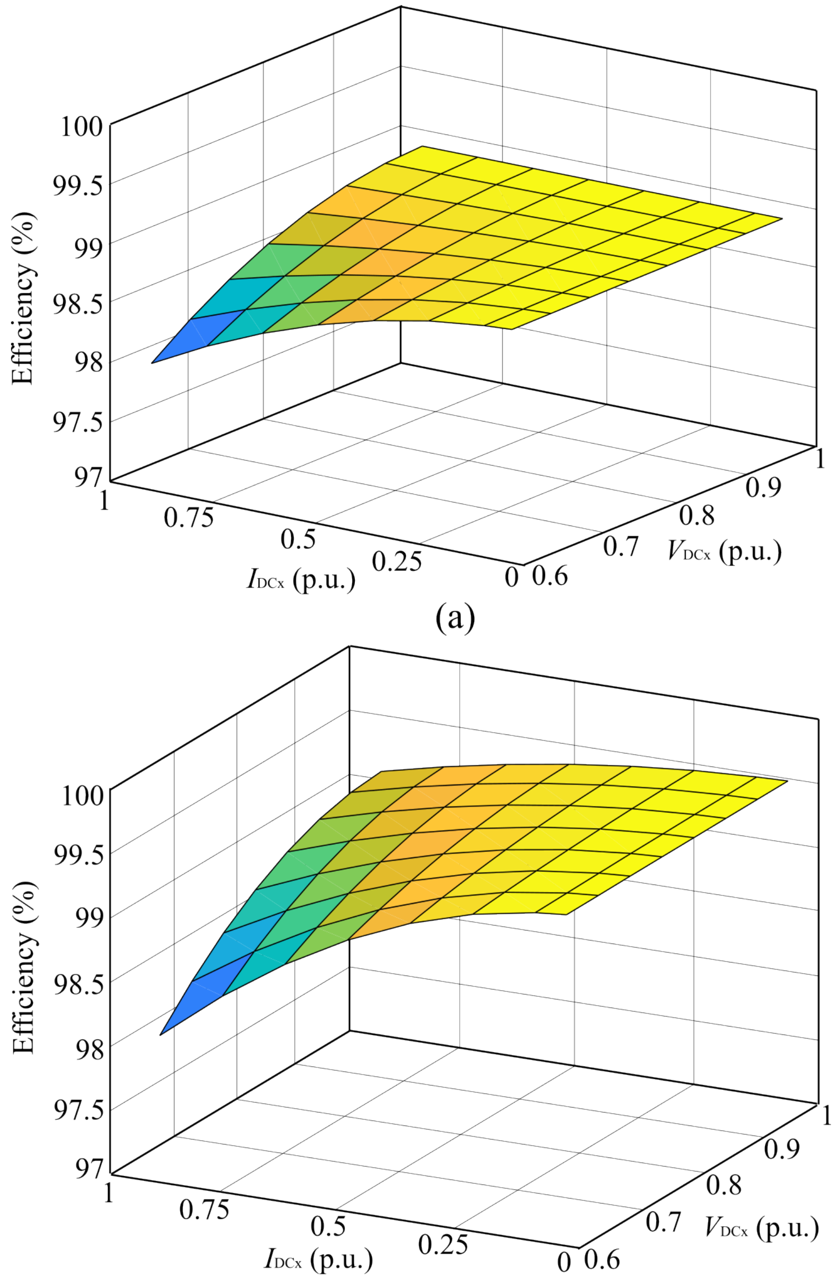


Figure 5.8: Efficiency analysis at different operating conditions: (a) forward mode efficiency estimation and (b) reverse mode efficiency estimation.

5.3 Laboratory scale prototype design

A prototype is designed to validate the concept of the proposed multi-port PPC. To build the lab scale prototype, the number of input ports is chosen as $n = 2$. The specification of the lab scale prototype is organized in Table. 5.1. The switching devices and passive elements for the prototype are selected using optimal device selection methods. However, to satisfy the thermal constraints of the switching devices, the heat sink design should be performed.

Table 5.1: Parameters of the multi-port PPC prototype

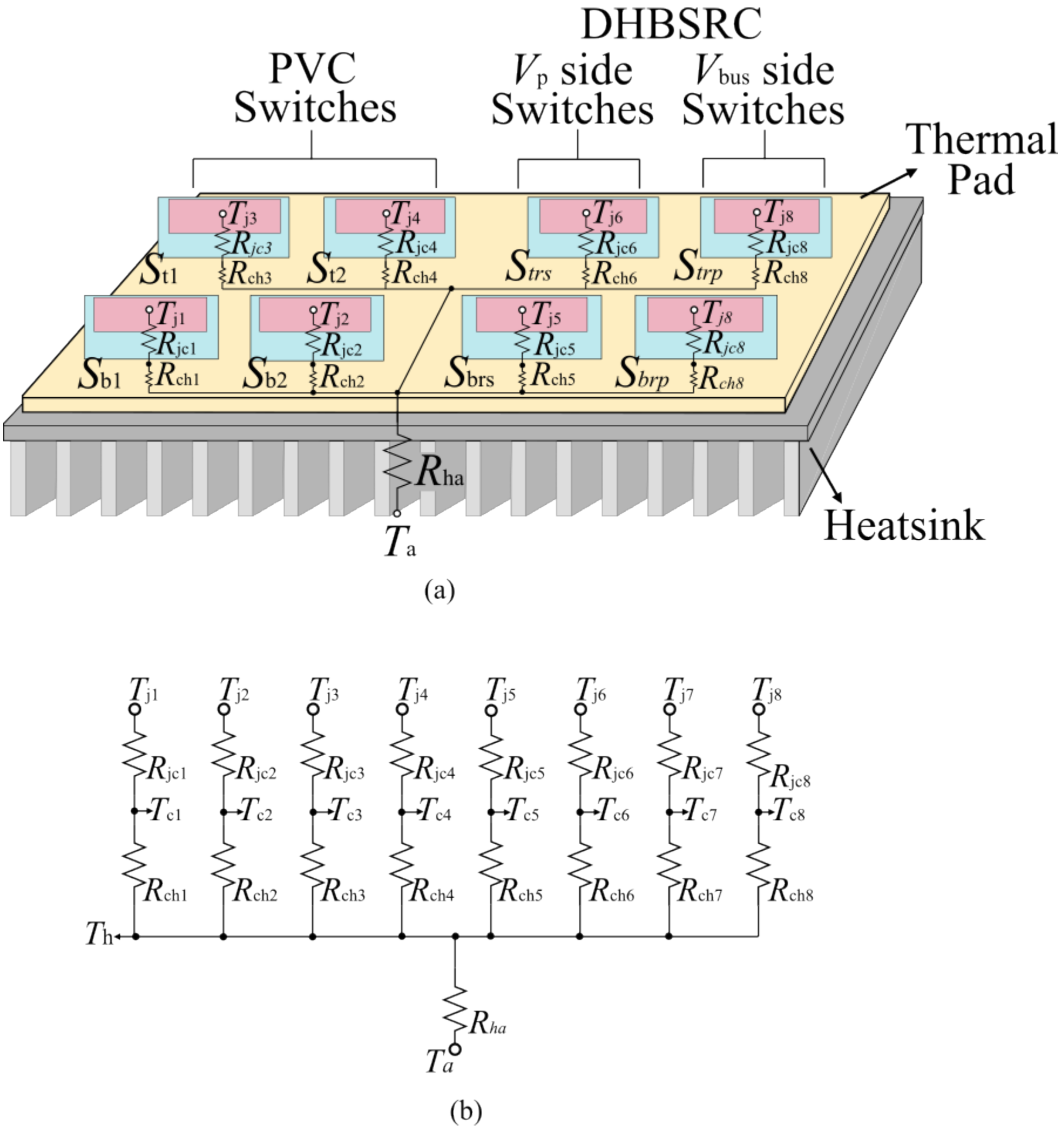
Targets	Symbol	Value	Unit
Number of DC inputs	n	2	-
Rated input voltage	V_{DCx}	360	V
Rated input current	I_{DCx}	11	A
Bus Voltage	V_{bus}	400	V
Partial Voltage	V_{p}	150	V
Rated system Power	P_{sys}	8	kW
Filter inductance	$L_{\mathrm{f1}}, L_{\mathrm{f2}}$	65	µH
Partial capacitance	C_{p}	14	µF
Transformer turns ratio	N	2.5	-
Control bandwidth	f_{cc}	4800	Hz

5.3.1 Heatsink design of the multi-port PPC

The equivalent thermal resistances of the multi-port PPC prototype for two DC inputs are shown in Fig. 5.9 (a). There are three major thermal resistance components that should be considered. First thermal resistance component should be considered is junction to case (R_{jc}) thermal resistances of each switch of the PVCs (S_{t1}, S_{t2}, S_{b1}, and S_{b2}) and SRC (S_{trp}, S_{trs}, S_{brp}, and S_{brs}). $R_{\mathrm{jc1}} \sim R_{\mathrm{jc4}}$ are the thermal resistances of the PVC switches that of [S_{t1}, S_{t2}, S_{b1}, and S_{b2}], R_{jc5}, R_{jc6} are the thermal resistances of the DHBSRC on V_{p} side which are [S_{trs} and S_{brs}], and R_{jc7}, R_{jc8} are the thermal resistances of the DHBSRC on V_{bus} side, which are [S_{trp} and S_{brp}]. Secondly, the thermal resistances of the thermal pad (R_{ch}), which is placed under the switches, are considered. Finally, the thermal resistance of heatsink (R_{ha}), which is placed under the thermal pad, is considered.

The equivalent circuit of the thermal resistances can be simplified as shown in Fig. 5.9 (b). The switches are connected to the heatsink by the thermal pad. Assuming that the heat distribution on the heatsink (h_s) is uniformly distributed, the junction temperature of each switch can be derived from the following equation:

$$T_{\mathrm{j}} = T_{\mathrm{a}} + R_{\mathrm{jcm}} P_{\mathrm{l}} + R_{\mathrm{chm}} P_{\mathrm{l}} + R_{\mathrm{ha}} P_{\mathrm{l(tot)}} \tag{5.9}$$



(a)

(b)

Figure 5.9: Heatsink design: (a) thermal model of the heatsink, and (b) equivalent circuit of the thermal resistances.

where m = 1,2,$\cdots$,8, T_j is the junction temperature, T_a is the ambient temperature, R_ha is the heatsink to ambient thermal resistance, and $P_{\mathrm{l(tot)}}$ is the total losses of the multi-port PPC.

Reorganizing (5.9) with respect to R_ha, the required heatsink resistance equation can be written as:

$$R_\mathrm{ha} = \frac{P_\mathrm{l}}{P_\mathrm{l(tot)}}\left(\frac{T_\mathrm{j}-T_\mathrm{a}}{P_\mathrm{l}} - R_\mathrm{jcm} - R_\mathrm{chm}\right) \tag{5.10}$$

As assumed before, T_h are the same for all switches. Furthermore, the temperature of each point, T_h, T_cm, and T_jm, can be calculated using the results of the loss analysis and relationship between temperature and losses in (5.9). Therefore, R_ha can be determined by considering the maximum T_jm where each switch of multi-port PPC can operate under the maximum thermal limit.

As shown in the losses analyzed in Fig. 5.7, the highest losses can be shown when V_DCx has the lowest value at the rated current in the forward mode. Using the loss analysis result in Fig.5.6 (b), the absolute value of the highest total losses can be calculated as 120 W. Furthermore, the absolute losses of the PVC and DC-transformer switches at the worst condition can be calculated as 64 W and 56 W, respectively. Assuming that the losses are equally distributed for each switch of the PVC and DC transformer, each switch of boost type PVCs (BSC430N25NSFD) dissipates 16 W, V_p side switches of the DC transformer (BSC430N25NSFD) makes 16 W losses by each switch, and V_bus side switches of the DC transformer (IPB65R110CDF) shows 20 W losses by each switch. According to the data sheet of the switches in Table. 3.3, a junction to case thermal resistance (R_jc) of the BSC430N25NSFD is 0.6 K/W and R_jc of the IPB65R110CDF is 0.77 K/W. A thermal resistance of the thermal interface is 0.4 K/W in 0.0001 m^2. Therefore, assuming the ambient temperature is $T_\mathrm{a} = 25\ ^\circ C$ and set the target junction temperature as $T_\mathrm{j} = 125\ ^\circ C$, the required R_ha can be derived as $R_\mathrm{ha} = 0.6$ K/W by applying the formula of (5.10). To achieve the target T_j and considering the possible area of the heatsink, an aluminum pin fin heatsink with R_ha= 0.6 K/W (with air cooling) is selected for the prototype. The details of the heatsink are shown in Fig. 5.10 and Table. 5.2.

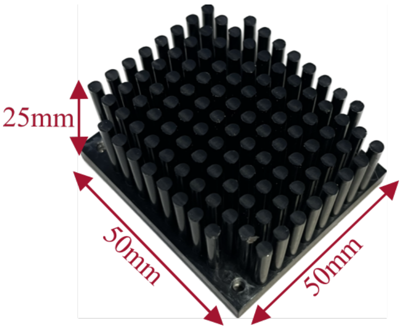


Figure 5.10: $R_\mathrm{ha} = 0.6$ K/W heatsink.

Table 5.2: Properties of selected heatsink

Properties	Symbol	Value	Unit
Material	-	Aluminum	-
Thermal R.	R_ha	0.6	K/W
Length	l	50	mm
Width	w	50	mm
Height	h	25	mm
Volume	Λ_hs	62.5	cm^3
weight	Wg	11.16	g

5.3.2 Specifications of the prototype

The top side view of the multi-port PPC prototype is shown in Fig. 5.11 (a). The lab scale prototype has two DC inputs, each with a rated power of 4 kW. Therefore, the total power of the DC input side is 8 kW. A partial power of 3 kW is processed by the two half bridges and the DHBSRC. The switches of the multi-port PPC are located on the top side of the PCB. The ceramic capacitors used for resonant capacitors are also placed on the top side of the DHBSRC. The bottom side view of the prototype is shown in Fig. 5.11 (b). On the bottom side of the PCB, the filter inductors of two ports L_{f1} and L_{f1} are placed. The inverter side DC bus capacitors C_{bt}, C_{bb}, and the transformer of DHBSRC are also placed on the bottom side of the PCB. Furthermore, a heatsink with the fan is placed on the bottom side to dissipate the heat from the semiconductor devices.

The measured volume and weight of the prototype are also given in Fig. 5.11. The length of the prototype is 150 mm, the width is 120 mm, and the height is 37 mm. Based on these dimensions information, the volume of the prototype can be calculated to be 665 cm^3 . The weight of the prototype is also measured to be 952 g. The power density of the prototype can be calculated to be 4.5 $\mathrm{W/cm}^3$.

Fig. 5.12 shows the relative weight of each component of the multi-port PPC. The plot shows that the magnetic components: transformer and inductor; charges more than 50 % of the total weight. Due to the core and copper windings, the weights of the magnetic passive elements are higher than the other components.

Fig. 5.13 shows the relative volume of each component of the multi-port PPC. The volume of the prototype is measured as 665 cm^3. The auxiliaries charges 40 % of the volume which includes auxiliary power supplies, connectors, and sensors. Apart from the auxiliary circuit, the transformer and inductor charges 30 % of the total volume.

5.4 Summary

To characterize the PPP of the multi-port PPC in the different operating conditions, the analysis of K_{pr} and UF are performed. The analysis of K_{pr} shows the amount of P_{p} that is processed by the multi-port PPC at different operating conditions. Due to the PPP capability of the multi-port PPC, it can process a maximum of 60 % of ΣP_{DCx}. The analysis of UF shows that the semiconductors of the multi-port PPC can utilize a maximum of 40% of ΣP_{DCx}. To validate the impact of the PPP on the losses of the multi-port PPC, the loss analysis of the multi-port PPC is also carried out. The losses can be different in the forward mode and reverse mode operation due to the change in the active bridge (V_{p} side or V_{bus} side) of the DHBSRC. The loss analysis shows that the reduction of PPP and UF causes the multi-port PPC to have lower losses. In addition, the detailed forward and reverse mode loss analysis of each device shows that the losses of the DHBSRC have the most significant change at the mode change. The efficiency of the multi-port PPC is also estimated, using the previous loss analysis results which include semiconductor losses, inductor and transformer losses. The

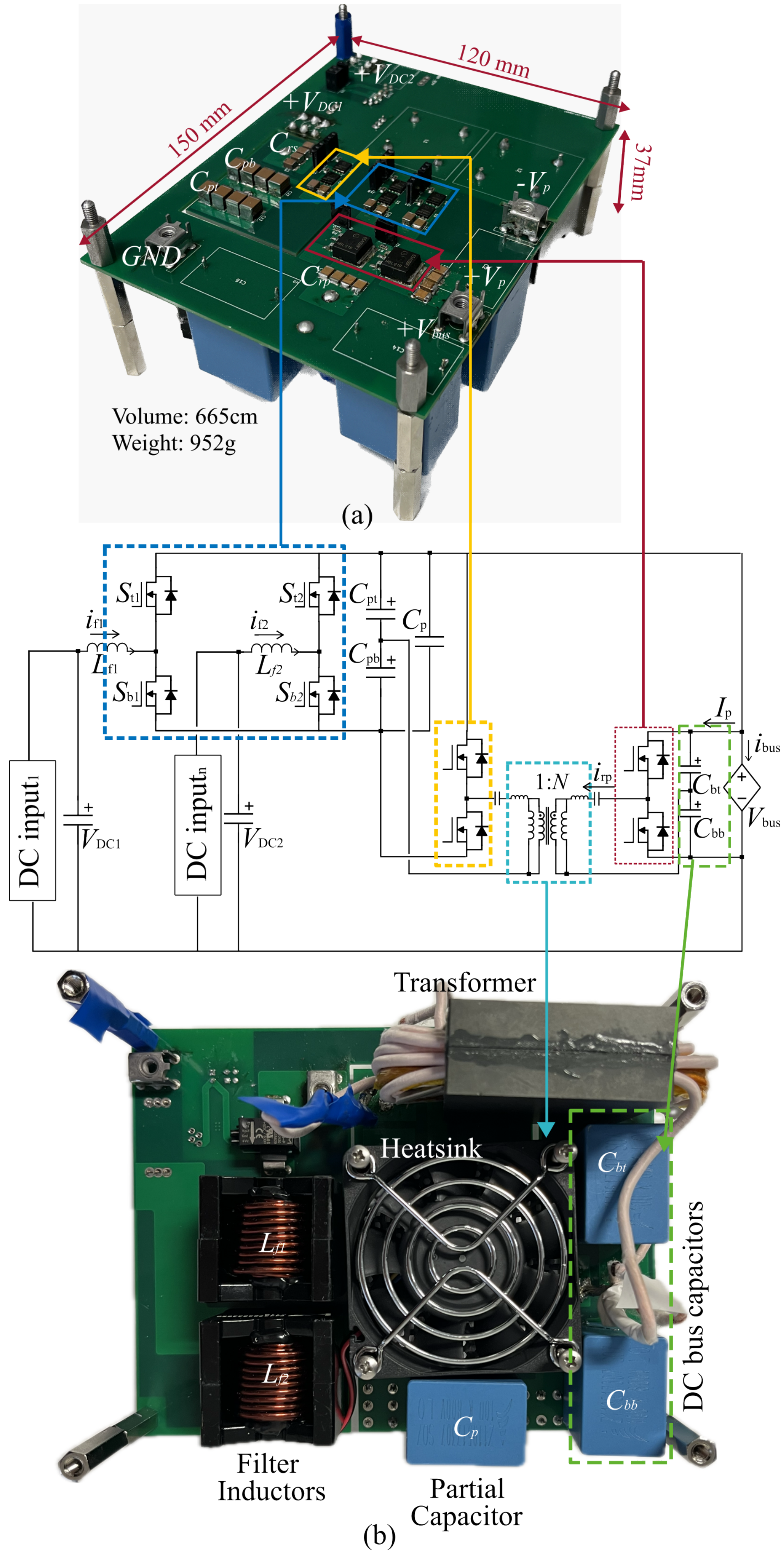


Figure 5.11: The multi-port PPC prototype: (a) top side view and (b) bottom side view.

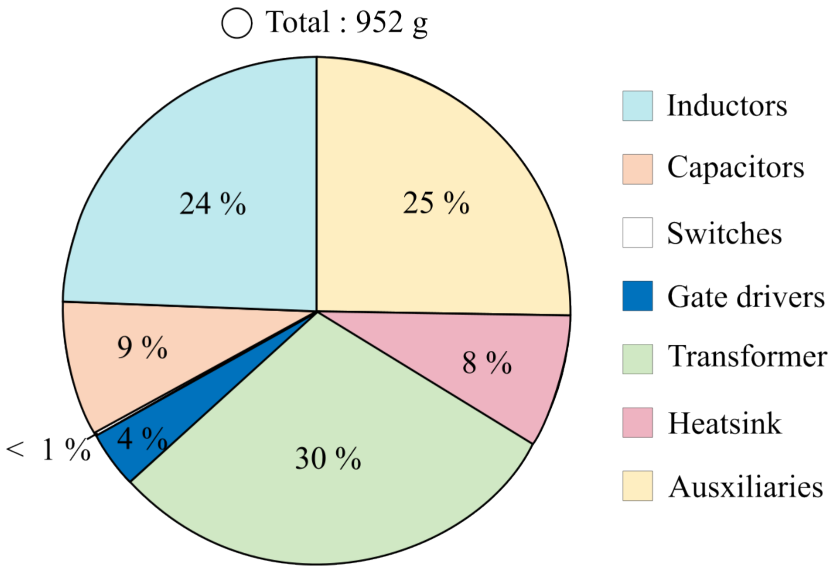


Figure 5.12: Detail weight information of multi-port PPC prototype.

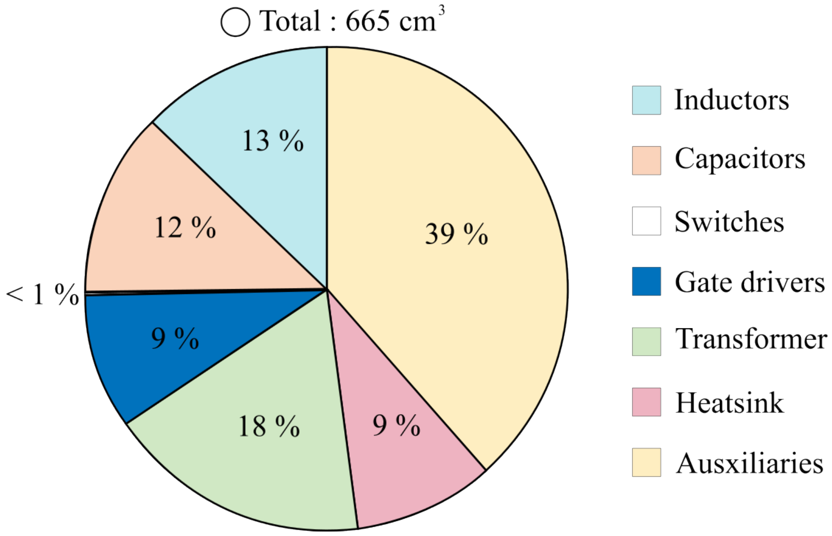


Figure 5.13: Detail volume information of multi-port PPC prototype.

efficiency estimation shows that the forward mode efficiency can reach maximum 98.9 %, and 98.6 % at the nominal operating point. The reverse mode losses can reach maximum 99.45 % and 99.1 % at the nominal operating point. Furthermore, the absolute values of the losses of each converter stage and each component are calculated to design the heatsink for the prototype. This allows the semiconductors can be driven below the maximum thermal limit. Using the heatsink design method, the thermal resistance of the chosen heatsink is $R_{\mathrm{ha}} = 0.6$ K/W. The detailed description of the hardware is given with its schematics. The weight and volume of the hardware information is also measured in detail and plotted in the pie chart.

6 Validation of the multi-port PPC concept

Using the prototype shown in Fig. 5.11, the validation of the proposed multi-port PPC concept is carried out through experiments. Fig. 6.1 shows the laboratory set up of the multi-port PPC experimental sets. Two DC power sources are used for each input port and a DC load is used to emulate the inverter side DC voltage. The additional power sources are used to power the auxiliary circuits such as gate drivers, low voltage power supply and sensors on the prototype. The control of the multi-port PPC is implemented on the RT-box, which is the hardware-in-the-loop real-time embedded system. The power analyzer (YOKOGAWA WT3000E) is used to measure the efficiency of the prototype. A detailed experimental conditions are organized in Table. 5.1.

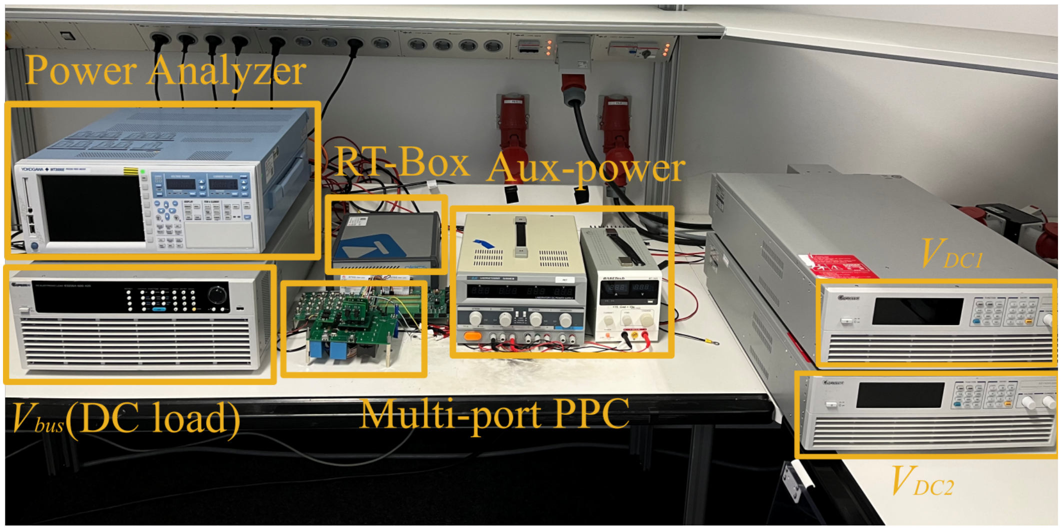


Figure 6.1: Laboratory setup for the experiments.

In this section, the input output steady state voltage and current characteristics of the proposed multi-port PPC are measured. As discussed in Table. 4.1, the proposed PPC can operate in two modes: forward mode and reverse mode. Therefore, a transition from reverse to forward mode is validated by the experimental results. Furthermore, the effects of the step current and voltage changes on the partial power are also proved. The efficiency of the whole system is measured with the power analyzer and the peak efficiencies of the forward and reverse modes are shown. Finally, the comparison between the proposed multi-port PPC and the benchmarks is performed to show the advantage of the proposed multi-port PPC architecture.

6.1 Experimental results of the multi-port PPC concept

To validate the partial voltage maintenance of the multi-port PPC and the current control capability, the steady state voltage of the transformer, the inductor current (I_{f1}) and the DC input voltage (V_{DC1}) of single port are measured. Fig. 6.2 shows the measurement result. The green color waveform is the input DC voltage, and it is given by the DC source connected

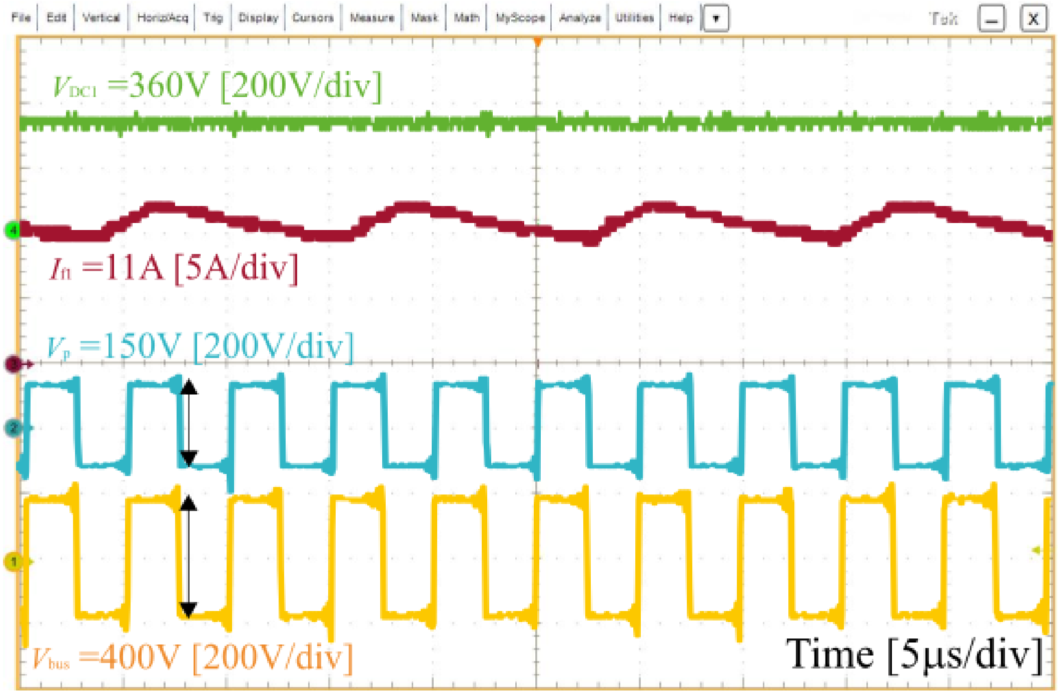


Figure 6.2: Steady state waveforms: DC input voltage of port1 (green), inductor current of port1 (red), transformer voltages at V_{bus} side (yellow), and transformer voltages at V_{p} side (blue).

to the port1, which value is $V_{\mathrm{DC1}} = 360$ V. The DC bus voltage of the inverter is controlled by the DC load in $V_{\mathrm{bus}} = 400$ V. The yellow waveform shows the V_{bus} side transformer voltage, and it shows that 400 V is applied. The blue waveform shows the partial voltage side voltage of the transformer is $V_{\mathrm{bus}} = 150$ V. This validates the stiff voltage maintenance of the DHBSRC. Furthermore, the filter current (red color waveform), shows that the multi-port PPC can force the target current, the reference value of which is $I_{\mathrm{f1}} = 11$ A.

According to Table. 4.1, the proposed multi-port PPC has two modes by the change of $P_{\mathrm{bus}} - \Sigma P_{\mathrm{DCx}}$. The mode change of the multi-port PPC is validated by the experiment in Fig. 6.3. In the figure, a reference current of 11 A is given to the port1 current (I_{f1}) which is the green color waveform. Port1 is in the forward mode by forcing the $I_{\mathrm{f1}} = 11$ A. The yellow waveform shows the port2 current (I_{f2}), and it shows the direction of I_{f2} changing from -8 A to 11 A. Even with the mode change of I_{f2}, I_{f1} still follows the reference current. Furthermore, V_{p}, the blue waveform, is also stiffly controlled by the DHBSRC. The red color waveform shows resonant current (I_{r}) of the DHBSRC. The peak to peak current ($I_{\mathrm{r_{pp}}}$) changes from 1 A to 3 A when the port2 mode changes. According to (3.4), the change of P_{p} on the DHBSRC can be decided by $V_{\mathrm{bus}}\Sigma I_{\mathrm{DCx}} - \Sigma V_{\mathrm{DCx}} I_{\mathrm{DCx}}$. According to the relationship, if port2 is in the reverse mode with -8 A, only 40 W is processed on the DHBSRC. If port2 is in the forward mode with 11 A, the DHBSRC will process 1 kW. Therefore, I_{p} is increased by the increase in power processed on the DHBSRC.

The waveforms when port2 is in the reverse mode are highlighted in Fig. 6.4. In the figure, $I_{\mathrm{f1}} = 11$ A which is in the forward mode, $I_{\mathrm{f2}} = $ -8 A which is in the reverse mode. The half bridges of port1, port2, and the DHBSRC should be driven simultaneously in order

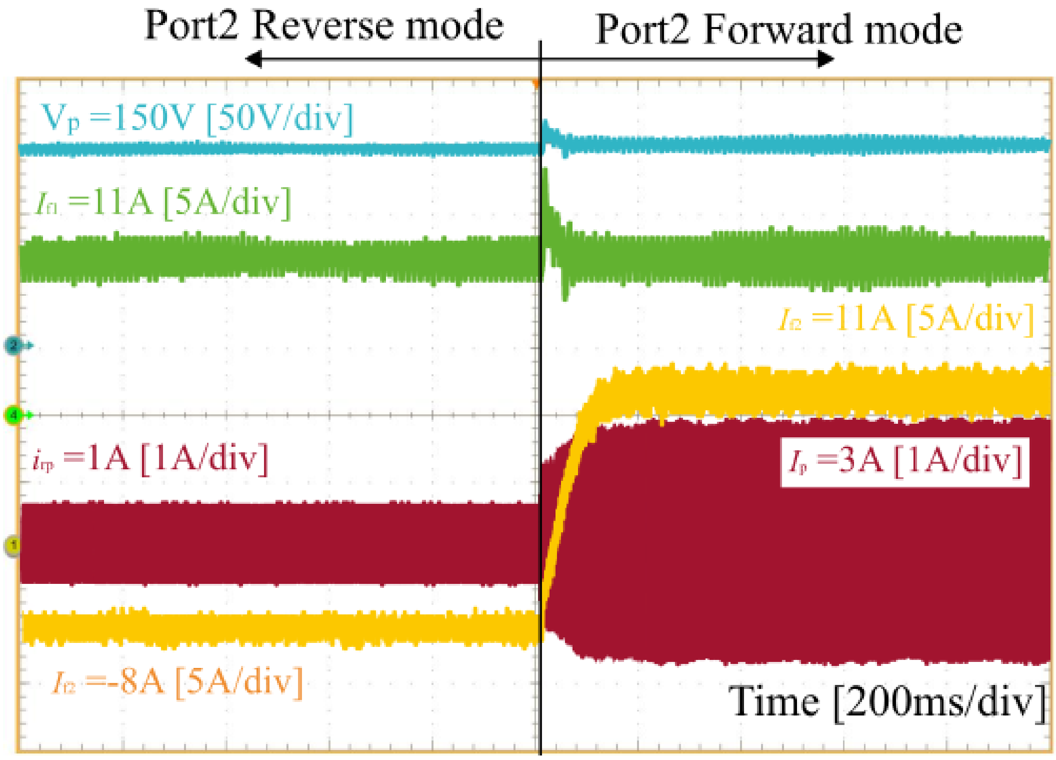


Figure 6.3: Port1 inductor current (green) and port2 inductor current (yellow), partial voltage (blue), and resonant current (red) when the mode change of the multi-port PPC.

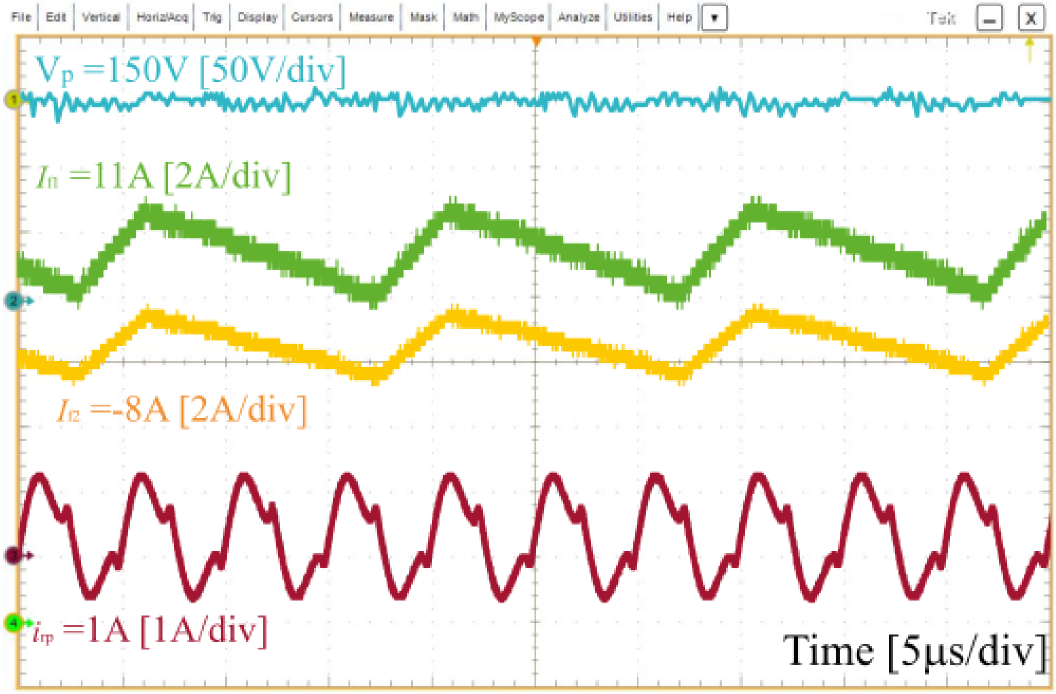


Figure 6.4: Multi-port PPC waveforms at the reverse mode: port1 inductor current (green) and port2 inductor current (yellow), partial voltage (blue), and resonant current (red).

to apply the multi-port PPC for the smart home applications. In addition, the I_{f1} and I_{f2} can be controlled individually to apply the different DC sources to the input. In the figure, the half bridges can force I_{f1} = 11 A, I_{f2} = -8 A individually and simultaneously. The DHBSRC processes the P_{p} between the DC inputs and V_{bus} by flowing resonant current i_{rp}. As discussed earlier, P_{p} = 40 W can be calculated by applying the relationship of equation (3.4). Therefore, the DHBSRC is driven at the light load.

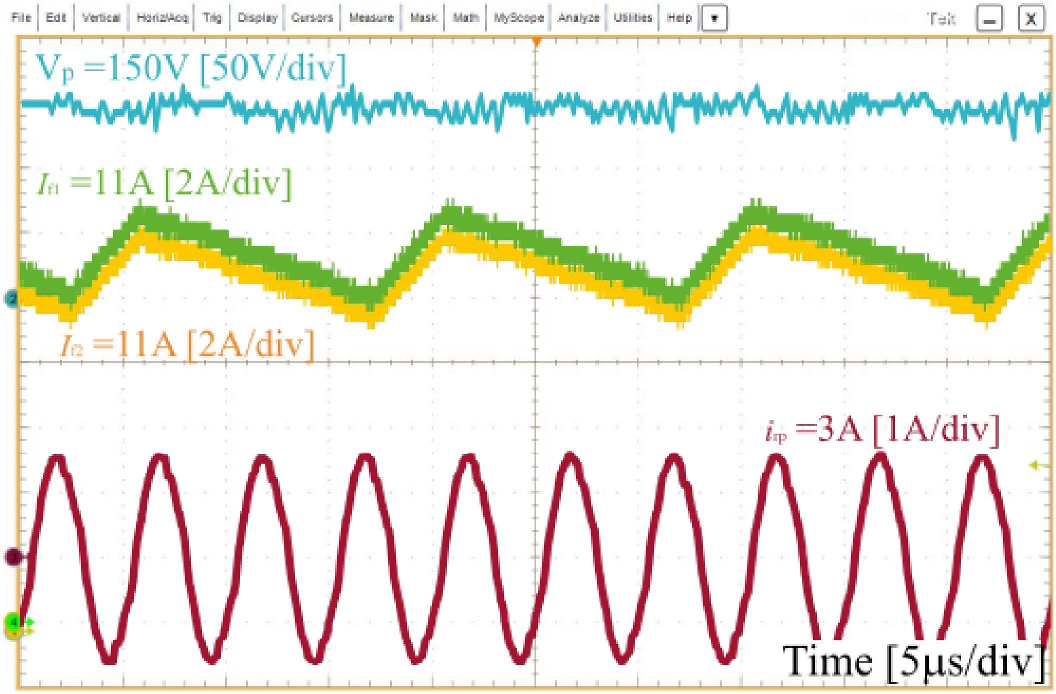


Figure 6.5: Multi-port PPC waveforms at the forward mode: port1 inductor current (green) and port2 inductor current (yellow), partial voltage (blue), and resonant current (red).

In Fig. 6.5, both of I_{f1} and I_{f2} are in forward mode. I_{f1} and I_{f2} are flowing to the same direction. Therefore, the ΣP_{DCx} is increased compared to the experiment of 6.4. According to the relationship in (3.4), the power on the DHBSRC is increased to P_{p} = 1 kW. Therefore, i_{rp} increased to 3A compared to Fig. 6.4 where i_{rp} is 1 A.

In Fig. 6.6, a step current reference change is applied to check the dynamic response of the current control by using Port1 at V_{bus} = 400 V. The result shows that I_{f1} can follow the reference current change with the settling time of I_{f1} is 130 μs as the current control that designed in (4.25). The current ripple (ΔI_{f1}) is 4.4 A which is 40 % of the nominal current as designed. The voltages V_{DC} and V_{p} have no influence on the variation of I_{f1}. As the current increases, the I_{p} across the DHBSRC also increases from 0.2 A to 1 A which follows the relationship in (3.4).

The impact of the input DC voltage step at V_{bus} = 400 V is shown in Fig. 6.7. The input DC voltage V_{DC1} is increased from 270V to 360V. The I_{f1} is controlled at 11 A. When the voltage step is given, V_{p} and I_{f1} are disturbed for a short time. However, thanks to the DHBSRC, V_{p} can be controlled at 150 V. In addition, the I_{f1} also can be controlled in 11 A by the current control. The change of the partial current I_{p} can be observed at the step of V_{DC1}. The change

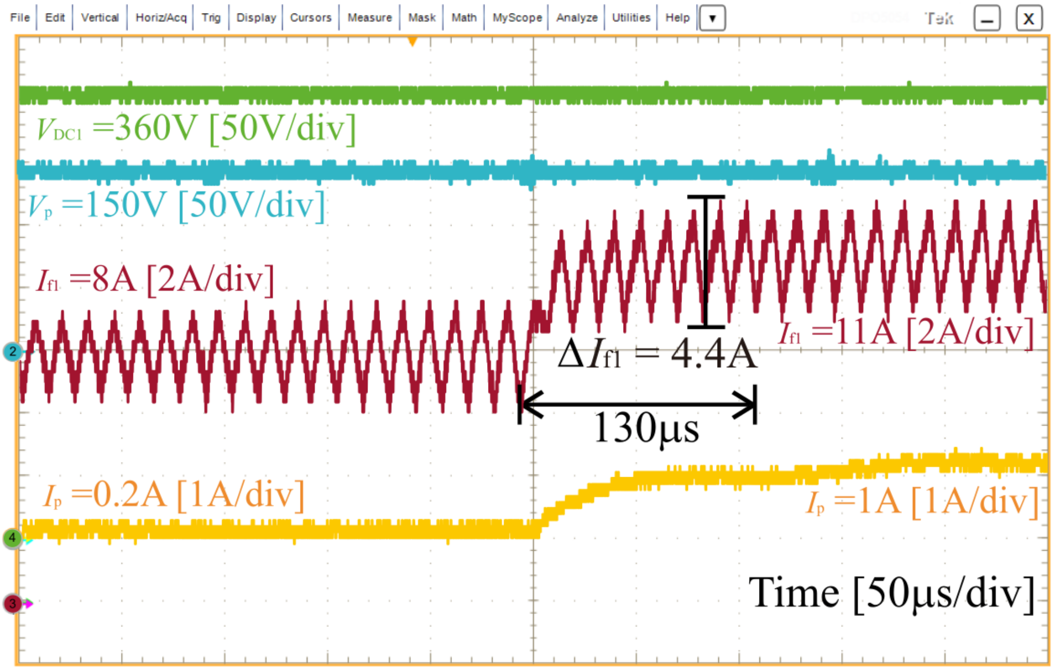


Figure 6.6: The inductor current step at $V_{\text{bus}} = 400$ V: port1 inductor current (red), partial voltage (blue), port1 DC input voltage (green), and partial current (yellow).

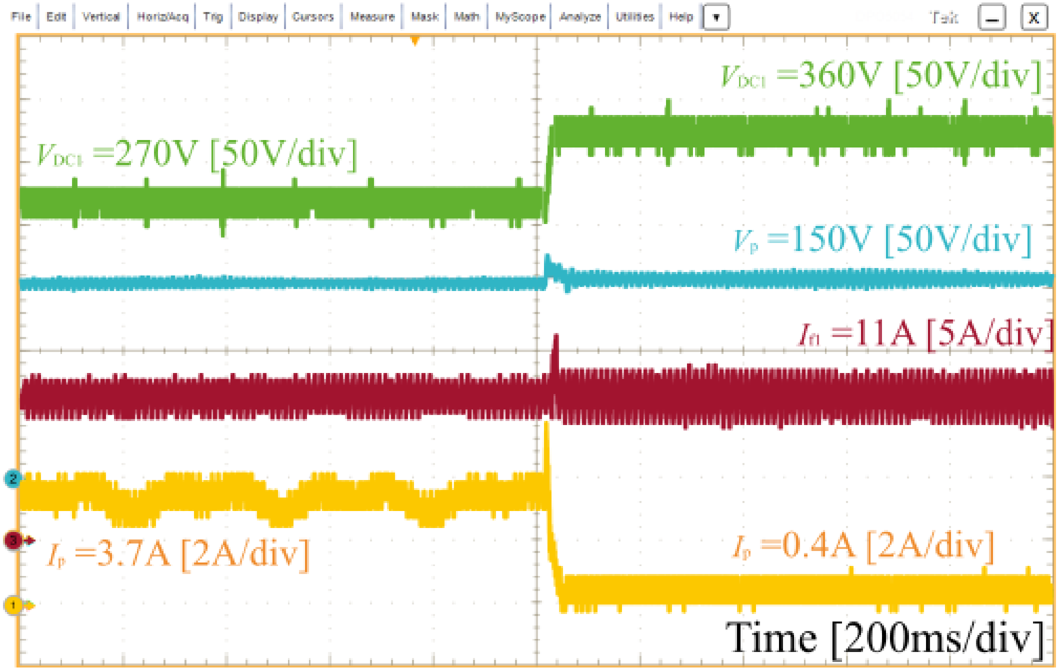


Figure 6.7: Waveforms when the inductor voltage step at $I^{*}_{f1} = 11$ A: port1 inductor current (red), partial voltage (blue), port1 DC input voltage (green), and partial current (yellow).

of the I_p follows the relationship in (3.4). When $V_\mathrm{DC1} = 270$ V, the amount of partial power P_p is 1.4 kW. Using (3.4), the calculated current I_p is 3.57 A. When the voltage becomes $V_\mathrm{DC1} = 360$ V, I_p drops to 0.4 A.

To validate the efficiency of the multi-port PPC, the forward and reverse mode efficiency measurements are performed on the entire system. The results of the efficiency measurement are shown in Fig. 6.8. $P_\mathrm{p} = 3$ kW, thus the measurement range can be down to 5 kW according to (3.10). The dots represents the measured efficiency and the lines represents the estimated efficiency. The forward mode efficiency can be as low as 98.6 % when PPC is operating at the maximum power. The maximum efficiency of the forward mode is 98.9 % at 7 kW load. The reverse mode efficiency is higher than the forward mode efficiency as previously analyzed. The efficiency of reverse mode is 99 % to 99.2 %. In addition, the measurements and the estimations has minor errors which is less than 3 %.

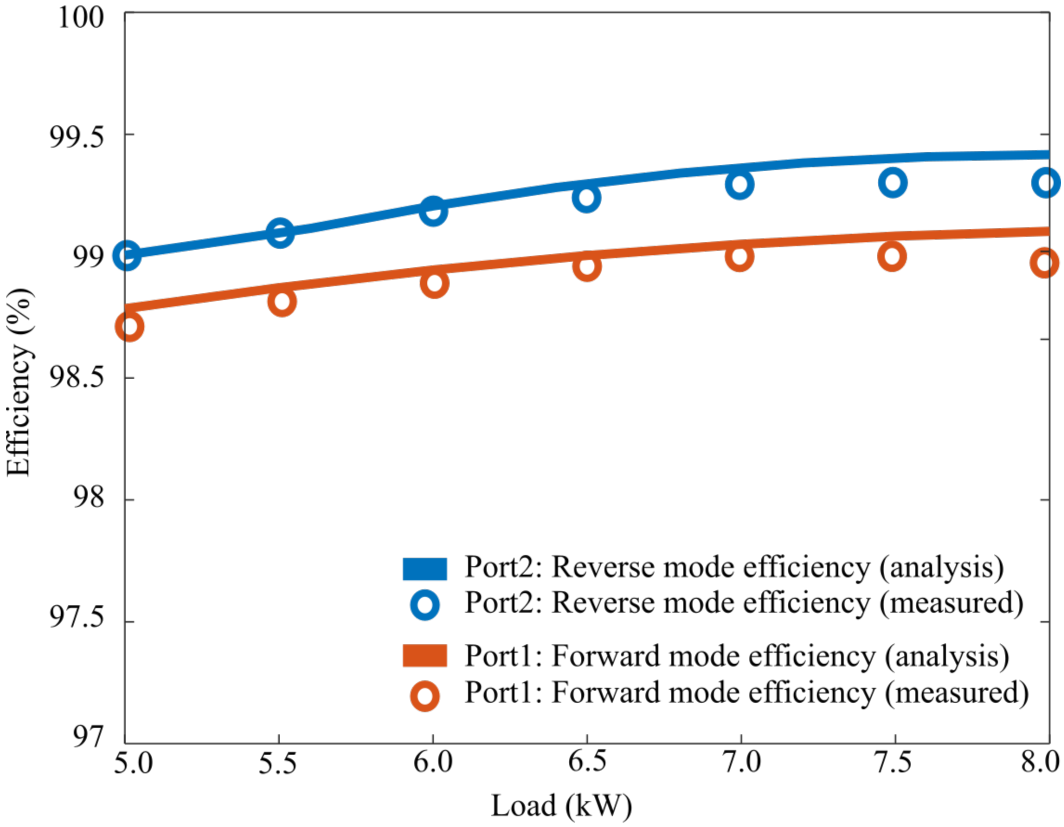
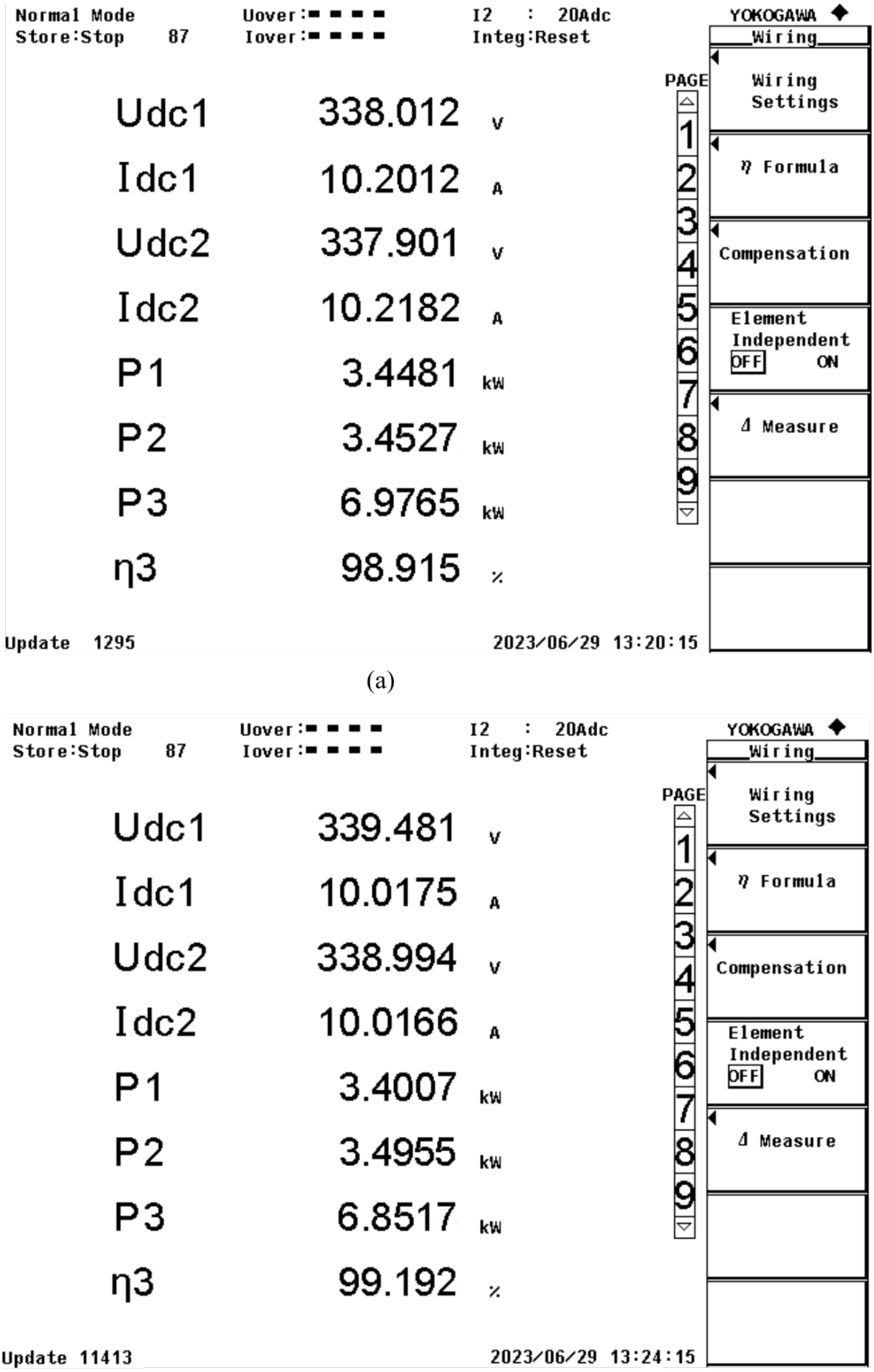


Figure 6.8: The comparisons of estimated efficiency of forward mode (blue line), measured efficiency of forward mode (blue circle), estimated efficiency of reverse mode (orange line), and measured efficiency of reverse mode (orange circle).

The peak efficiency is measured with the power analyzer. The results of the forward and reverse mode measurements are shown in Fig. 6.9. The forward mode peak efficiency is shown in Fig. 6.9 (a), the measurement result is 98.9 %. The peak efficiency of the reverse mode peak is shown in Fig. 6.9 (b). The measurement shows that its peak efficiency is 99.2 %.



```
Normal Mode          Uover:■ ■ ■ ■       I2   :  20Adc          YOKOGAWA ◆
Store:Stop    87     Iover:■ ■ ■ ■       Integ:Reset            Wiring

     Udc1         338.012  V
     Idc1         10.2012  A
     Udc2         337.901  V
     Idc2         10.2182  A
     P1            3.4481  kW
     P2            3.4527  kW
     P3            6.9765  kW
     η3            98.915  %

Update  1295                          2023/06/29 13:20:15
```

(a)

```
Normal Mode          Uover:■ ■ ■ ■       I2   :  20Adc          YOKOGAWA ◆
Store:Stop    87     Iover:■ ■ ■ ■       Integ:Reset            Wiring

     Udc1         339.481  V
     Idc1         10.0175  A
     Udc2         338.994  V
     Idc2         10.0166  A
     P1            3.4007  kW
     P2            3.4955  kW
     P3            6.8517  kW
     η3            99.192  %

Update 11413                          2023/06/29 13:24:15
```

(b)

Figure 6.9: Peak efficiency measurement results: (a) forward mode peak efficiency, and (b) reverse mode peak efficiency.

6.2 Comparison of benchmark and proposed architecture

The volume comparison between the proposed multi-port PPC and the benchmarks in the target P/η region (shown in Fig. 2.22) are shown in Fig. 6.10. In the figure, the blue color shows the volume of the inductor (Λ_{L}), the orange color shows the volume of the capacitor (Λ_{C}), the yellow color shows the volume of the transformer (Λ_{T}), and the purple color shows the volume of the switching components (Λ_{sw}). [81] has the largest volume due to the use of the transformer. The FRPC converter based PPP architecture of [67] where the architecture does not need the the transformers. Therefore [67] has 30 % less volume than [81]. The proposed architecture can reduce the volume in 70 % compared to the benchmarks. The proposed PPC can apply the partial voltage and current rating of passive and active elements. Therefore, the volume also can be reduced by the proposed architecture using the transformer.

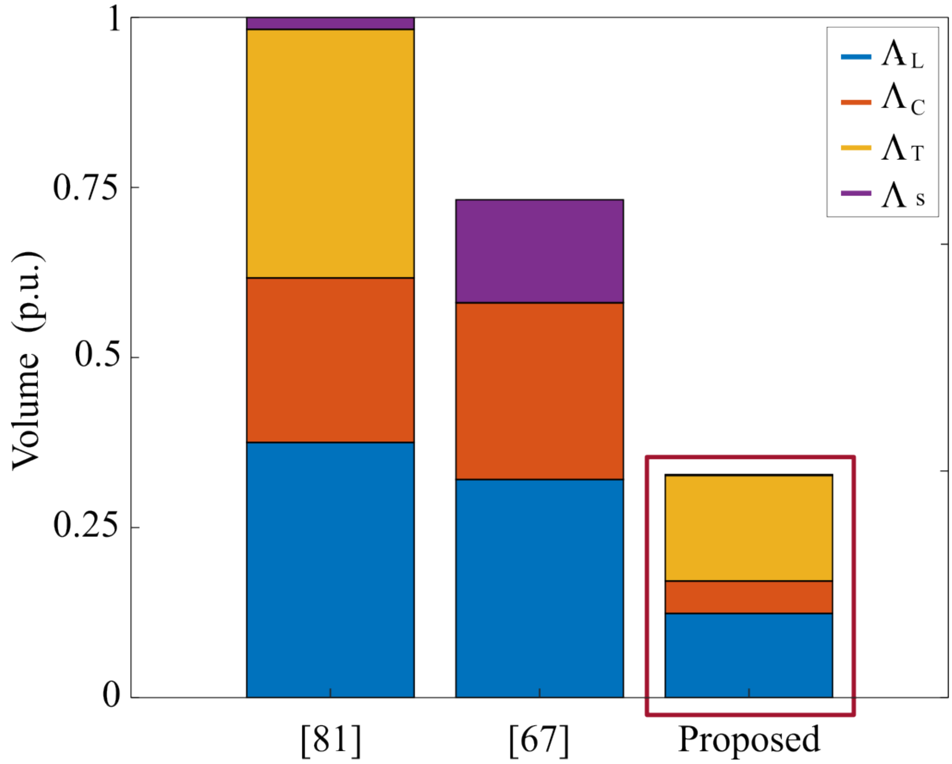


Figure 6.10: Volume comparison between benchmarks ([67]: 10 kW FRPC and [81]: 6.5 kW PPC), and the proposed architecture.

The spider chart in Fig. 6.11 shows the overall comparison between the benchmarks and the proposed architecture. The analysis in the chart shows that [67] has the highest efficiency and modularity. [67] can use the partial power rating switching module, thus the DC-DC converter stage can be easily implemented by using the same switching modules. However, the architecture used the full power rating inductor and capacitors, which greatly affect on the volume increase. Therefore, the proposed multi-port PPC shows the improvements on the volume and cost reduction by using partial rating power electronic devices. In addition, the specific weight (kW/kg) is estimated by using the hardware information from the articles. The estimated results of the specific weight also shows that the proposed multi-port PPC can decrease the weight of the converter for the smart home applications. The other PPC solution of [81], shows lower efficiency compared to the others. [81] can achieve 99.5 % efficiency at the target P/η area. but it could not achieve the volume and cost reduction of the PPC architecture.

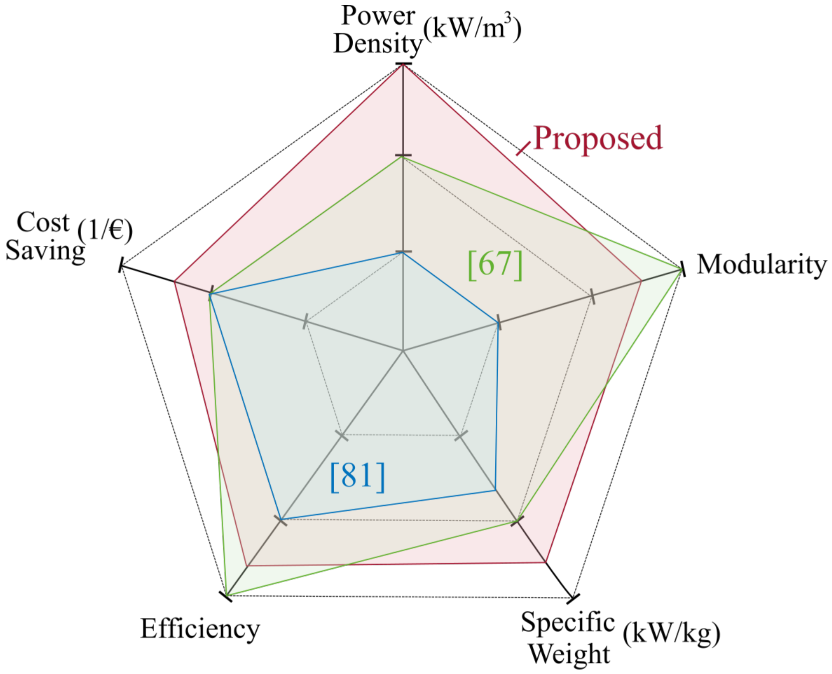


Figure 6.11: Spider chart for the comparison between benchmarks ([67]: 10 kW FRPC and [81]: 6.5 kW PPC), and the proposed architecture.

6.3 Summary

To validate the performance and the validity of the concept, the steady state currents and voltages are first measured. The DC input voltage (V_{DC1}), the transformer voltages (V_{bus} and V_{p}), and the filter current (I_{f1}) show the current control capability and partial voltage control capability of the multi-port PPC. The multi-port PPC has two mode modes by changing the direction of P_{p}. The experimental result of the mode change shows that both the forward and reverse mode can be handled by the multi-port PPC prototype. Changing values of the I_{f1} and I_{f2} affects the change of P_{p} on the DHBSRC. Therefore, I_{p} can be changed by following the relationship of (3.4). The transient waveforms of I_{f1} shows that the validity of the current control design. In addition, the DC input voltage step change was also performed in order to validate the current control capability at the V_{DCx} change. The result shows that I_{fx} can control the reference current even with the V_{DCx} change. Furthermore, the change of I_{p} shows that the partial current can be changed due to V_{DCx} change, according to (3.4).

Finally, the forward mode and reverse mode efficiency of the multi-port PPC are validated. The measured efficiency at different loads is compared with the estimated efficiency. The estimated and measured results have the error less than 3 %. The peak efficiency of the forward mode is 98.9 % and the peak efficiency of the reverse mode is 99.2 %. The measurement results of the peak efficiencies are provided by the captured figures. Furthermore, the comparison between the proposed PPC solution and the benchmarks in the target P/η range shows that the proposed PPC can improve the efficiency with the volume and cost reduction as the goal of this study.

7 Summary, conclusion and future research

7.1 Summary and conclusion

The modern home requires the seamless integration of RESs and various DC loads such as residential ESSs, EVs, DC pumps, and LED lighting. PECs play a key role in the integration of RESs and various DC loads which optimize the energy use of smart home architectures. The increasing embedding of aforementioned electric component connections necessitates the use of multi-port architecture. Meanwhile, the further reductions in the losses, volumes, and costs of the conventional FPP based multi-port architecture is also required to make the PEC infrastructures more affordable and suitable for the home installation.

In Chapter 2, the power electronic converters for the DC to AC and DC to DC power conversion are explained. Firstly, the operation strategy of the inverter in the smart home is discussed. Furthermore, the impact of the grid synchronization methods on the stability of the inverter is analyzed. The impact of the PLL and self-synchronization on the stability of the inverter is investigated by means of grid impedance based stability analysis. The analysis shows the self-synchronization can be a more stable grid synchronization method, where the self-synchronization can remove the additional harmonic propagation path. Secondly, the DC-DC converter architectures that performs DC-DC power conversion for the different RESs are investigated. The power processing characteristics of the DC-DC converters are analyzed by using the VA area model. Using the VA area model, the DC-DC converters can be divided into two big categories: FPCs and PPP converters. FPCs process total power from the input and the converter should employee the same voltage and current rate as the input DC source. On the other hand, PPP converters can process only a part of the power from the input and it is possible to use lower voltage or current rate compared to the input DC source. The recent studies of the different PPP converters have been reported that they can improve the efficiency and the power density of the DC-DC converters. Therefore, in order to set the benchmark, the amount of processed power and the number of the required power electronics elements to build the different PPP architectures are compared. Furthermore, the efficiencies from the most relevant PPP converter studies are plotted and compared in the graph.

In Chapter 3, the novel multi-port PPC architecture for the smart home application is proposed. The proposed architecture has two converter stages which are the PVCs and the DC transformer. The PVCs can achieve the PPP by processing partial voltage (V_p) and full DC input current (I_DCx). Furthermore, DC transformer can achieve the PPP by processing full inverter side bus voltage (V_bus) and partial current (I_p). The power processing principle of the proposed architecture is described with the key equations. The target operating point and ratings of the architecture are determined by market research and PV data analysis of commercial products in the residential scale. The selected target specifications for residential scale is described in Table. 3.2. The possible PVCs topologies are compared and the half bridge leg is selected to build the PVCs with the lowest losses. In addition, the DC transformer has two topologies which are DAB and SRC. The investigation of the DAB converter shows that it cannot achieve the soft switching at the target power range. Therefore, SRC which can achieve ZVS at the target power range is selected for the DC transformer stage. Finally, by comparing the losses of the different SRC bridge combinations, the DHBSRC with the lowest losses is selected.

Chapter 4 presents the design principle of the proposed multi-port PPC and its operating principle of the proposed PPC architecture. The inductors and capacitors of the PVC stage design methods are provided to achieve the target current and voltage ripple. Furthermore, the selection guidance of the commercial inductor and capacitors based on the analytical volume estimation are provided. Based on the selected parameters, the small signal model of the PVC stage is performed. The small signal model of PVC is used to choose the control parameters. Next, the parameters selection of the DHBSRC is carried out by using the FHA model of the DHBSRC. The gain curves of the DHBSRC can be analyzed by using the FHA model of the DHBSRC with respect to the variations in the resonant tank parameters. The gain curve analysis can be used to select the quality factor Q and the inductance ratio h at which the minimum resonant inductance value can be achieved. At the end, by solving the mathematical relationship between Q and h, the primary and secondary resonant tanks values can be derived. Finally, the mathematical model of the DHBSRC transformer is also designed. In addition, the realization of the transformer is carried out to achieve the same parameters between the theoretical transformer model. The transformer parameters of the theoretical model are compared with the parameters of simulation model and the parameter of the realized transformer which measured experimentally. The results show that the parameters of the theoretical transformer model and the parameters of the realized transformer are closely matching which means that the theoretical model can represent the realized transformer.

In Chapter 5, PPP characteristics of the proposed multi-port PPC in the different operating points and the relationship between PPP and the losses are verified. The PPP characteristics of the proposed PPC are analyzed using the partial power processing ratio (K_{pr}) and the UF. The K_{pr} analysis shows that the proposed PPC processes more power when $V_{\mathrm{DCx}} << V_{\mathrm{bus}}$ and higher I_{fx}. The UF analysis proves that the proposed PPC allows the use of lower power semiconductor devices due to its PPP capability. The loss analysis of the proposed architecture proves that the PPP capability of the proposed architecture can reduce the losses. Based on the loss analysis, the heatsink design of the proposed multi-port PPC is carried out, therefore the semiconductor devices can be driven under its thermal limits. Finally, the 3 kW (partial power) laboratory scale prototype for the 8 kW (full power) system is built. The volume and the weight of the prototype is measured where the volume is 665 cm^3 and the weight is 952 g, and the power density can be obtained as 4.5 W/cm^3.

The validation of the proposed concept and comparison between the benchmarks are performed in Chapter 6. The input current, partial voltage and PPP control capabilities are validated by the experimental results. Furthermore, the efficiency of the converter under different load conditions is measured and compared with the analytical efficiency. The error between measurement and analysis is < 3 %. The peak efficiency of the prototype is measured to be 99.2 % in reverse mode and 98.9 % in forward mode. The comparison between the benchmark proves that the proposed multi-port PPC can achieve higher power density by using the reduced rated power semiconductor devices and passive elements compared to the benchmarks. Furthermore, the spider chart shows that the cost and the specific weight also can be improved compared to the benchmarks. Still, to construct the gate driver circuit, an individual isolated gate driver and isolated power supply should be used for the proposed PPC. Therefore, there need further investigation of the advantage of the proposed architecture, including the gate drivers and auxiliary circuits.

7.2 Future research

A novel multi-port PPC for smart home applications has been proposed. The proposed architecture aims to increase the efficiency and reduce the cost and volume by using the partial rated components.

The challenges for future research need to be addressed as follows:

- The cost of the semiconductors and passive elements of the proposed architecture can be reduced by using the reduced power rated devices compared to the benchmarks. However, as discussed in the conclusion, isolation is required for the power supply and gate drivers, which can increase the cost and volume of the gate driver circuit. Therefore, the total system cost, including the gate driver circuit, should be analyzed and compared between the state of the art solutions to verify the practical advantage of the proposed architecture in terms of cost.
- This study focused on the proposing a novel multi-port PPC architecture and validation of the proposed concept. Therefore, the practical validation can be followed by the development of control algorithms for different DC sources and loads connected to the proposed architecture. Furthermore, by applying the proposed architecture to the different applications, the power control and distribution algorithm between the DC sources and loads can be studied.
- The proposed solution is the DC-DC stage for smart home applications. The study mainly focused on the development and analysis of the DC-DC converter stage. Therefore, the interactions of the proposed architecture between the inverter stage can be studied. Furthermore, by analyzing the whole smart home system, the performance of the proposed architecture in the practical application can also be studied.
- The reliability of the proposed architecture also can be further investigated. A thermal distribution analysis can be performed for both the semiconductors and the passive elements to investigate the loss distribution of the proposed architecture.

8 References

[1] R. Wang, S. Jiang, D. Ma, Q. Sun, H. Zhang, and P. Wang, "The energy management of multiport energy router in smart home," *IEEE Transactions on Consumer Electronics*, vol. 68, no. 4, pp. 344–353, 2022.

[2] B. Han, Y. Zahraoui, M. Mubin, S. Mekhilef, M. Seyedmahmoudian, and A. Stojcevski, "Home energy management systems: A review of the concept, architecture, and scheduling strategies," *IEEE Access*, vol. 11, pp. 19 999–20 025, 2023.

[3] J. Han, C.-S. Choi, W.-K. Park, I. Lee, and S.-H. Kim, "Plc-based photovoltaic system management for smart home energy management system," in *2014 IEEE International Conference on Consumer Electronics (ICCE)*, 2014, pp. 542–543.

[4] B. Celik, R. Roche, D. Bouquain, and A. Miraoui, "Decentralized neighborhood energy management with coordinated smart home energy sharing," *IEEE Transactions on Smart Grid*, vol. 9, no. 6, pp. 6387–6397, 2018.

[5] A. Hota, M. M. Qasim, J. L. Kirtley, and V. Agarwal, "Novel switched capacitor boost inverter configuration for three-phase induction motor driven home appliances," *IEEE Transactions on Industry Applications*, vol. 57, no. 2, pp. 1450–1458, 2021.

[6] O. Lucia, I. Cvetkovic, H. Sarnago, D. Boroyevich, P. Mattavelli, and F. C. Lee, "Design of home appliances for a dc-based nanogrid system: An induction range study case," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 4, pp. 315–326, 2013.

[7] M.-H. Ryu, H.-S. Kim, J.-W. Baek, H.-G. Kim, and J.-H. Jung, "Effective test bed of 380-v dc distribution system using isolated power converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4525–4536, 2015.

[8] K. Kanathipan and J. Lam, "A high voltage gain isolated pv micro-converter with a single-voltage maximum power point tracking control loop for dc micro-grid systems," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 3, no. 3, pp. 755–765, 2022.

[9] B. Krishna and V. Karthikeyan, "Ultra-voltage gain step-up dc-dc converter for renewable energy micro-source applications," *IEEE Transactions on Energy Conversion*, vol. 37, no. 2, pp. 947–957, 2022.

[10] Y. Gui, R. Han, J. M. Guerrero, J. C. Vasquez, B. Wei, and W. Kim, "Large-signal stability improvement of dc-dc converters in dc microgrid," *IEEE Transactions on Energy Conversion*, vol. 36, no. 3, pp. 2534–2544, 2021.

[11] F. Hoffmann, J. Person, M. Andresen, M. Liserre, F. D. Freijedo, and T. Wijekoon, "A multiport partial power processing converter with energy storage integration for ev stationary charging," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7950–7962, 2022.

[12] W. Wu, X. Wu, Y. Zhao, L. Wang, T. Zhao, and L. Jing, “An improved multiport dc power flow controller for vsc-mtdc grids,” *IEEE Access*, vol. 8, pp. 7573–7586, 2020.

[13] Y. Liang, H. Zhang, M. Du, and K. Sun, “Parallel coordination control of multi-port dc-dc converter for stand-alone photovoltaic-energy storage systems,” *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 3, pp. 235–241, 2020.

[14] Y. Liu, Y. Hu, G. Chen, and H. Wen, “Partial power processing multiport dc-dc converter with radial module connections,” *IEEE Transactions on Power Electronics*, vol. 37, no. 11, pp. 13 398–13 412, 2022.

[15] G. Chen, Y. Liu, and W. Cui, “Partial power processing multi-port dc-dc converters,” in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 1406–1411.

[16] R. Rosso, X. Wang, M. Liserre, X. Lu, and S. Engelken, “Grid-forming converters: Control approaches, grid-synchronization, and future trends-a review,” *IEEE Open Journal of Industry Applications*, vol. 2, pp. 93–109, 2021.

[17] R. Rosso, S. Engelken, and M. Liserre, “Current limitation strategy for grid-forming converters under symmetrical and asymmetrical grid faults,” in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 3746–3753.

[18] Z. Zou, B. D. Besheli, R. Rosso, M. Liserre, and X. Wang, “Interactions between two phase-locked loop synchronized grid converters,” *IEEE Transactions on Industry Applications*, vol. 57, no. 4, pp. 3935–3947, 2021.

[19] N. Pogaku, M. Prodanovic, and T. C. Green, “Modeling, analysis and testing of autonomous operation of an inverter-based microgrid,” *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 613–625, 2007.

[20] C. X. Rosero, M. Velasco, P. MartÃ, A. Camacho, J. Miret, and M. Castilla, “Active power sharing and frequency regulation in droop-free control for islanded microgrids under electrical and communication failures,” *IEEE Transactions on Industrial Electronics*, vol. 67, no. 8, pp. 6461–6472, 2020.

[21] M. Gao, M. Chen, B. Zhao, B. Li, and Z. Qian, “Design of control system for smooth mode-transfer of grid-tied mode and islanding mode in microgrid,” *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6419–6435, 2020.

[22] Q. Tao, J. Geis-Schroer, F. Wald, M. Courcelle, M. Langwasser, T. Leibfried, M. Liserre, and G. De Carne, “The potential of frequency-based power control in distribution grids,” in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1–6.

[23] Y. Pan, A. Sangwongwanich, Y. Yang, X. Liu, M. Liserre, and F. Blaabjerg, “Flexible active power control of distributed photovoltaic systems with integrated battery using series converter configurations,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 6891–6909, 2022.

[24] G. De Carne, G. Buticchi, M. Liserre, and C. Vournas, “Real-time primary frequency regulation using load power control by smart transformers,” *IEEE Transactions on Smart Grid*, vol. 10, no. 5, pp. 5630–5639, 2019.

[25] G. De Carne, G. Buticchi, Z. Zou, and M. Liserre, “Reverse power flow control in a st-fed distribution grid,” *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 3811–3819, 2018.

[26] R. Rosso, S. Engelken, and M. Liserre, “On the implementation of an frt strategy for grid-forming converters under symmetrical and asymmetrical grid faults,” *IEEE Transactions on Industry Applications*, vol. 57, no. 5, pp. 4385–4397, 2021.

[27] ——, “Robust stability investigation of the interactions among grid-forming and grid-following converters,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 991–1003, 2020.

[28] S. Asadollah, R. Zhu, and M. Liserre, “Analysis of voltage control strategies for wind farms,” *IEEE Transactions on Sustainable Energy*, vol. 11, no. 2, pp. 1002–1012, 2020.

[29] Z. Yang, S. He, D. Zhou, X. Wang, R. W. De Doncker, F. Blaabjerg, and L. Ding, “Wideband dissipativity enhancement for grid-following vsc utilizing capacitor voltage feedforward,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 3138–3151, 2023.

[30] H. Gong, X. Wang, and L. Harnefors, “Rethinking current controller design for pll-synchronized vscs in weak grids,” *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1369–1381, 2022.

[31] H. Wu and X. Wang, “Design-oriented transient stability analysis of pll-synchronized voltage-source converters,” *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3573–3589, 2020.

[32] D. Yang, X. Wang, F. Liu, K. Xin, Y. Liu, and F. Blaabjerg, “Symmetrical pll for siso impedance modeling and enhanced stability in weak grids,” *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1473–1483, 2020.

[33] T. Liu, X. Wang, and F. Liu, “Impact of dc-link voltage control on transient stability of pll-synchronized voltage-source converters,” in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, 2022, pp. 435–439.

[34] F. Chen, L. Zhao, L. Harnefors, and X. Wang, “Impedance modeling for quadrature-axis active damping of pll dynamics,” in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–7.

[35] F. Cecati, J. K. M. Becker, S. Pugliese, Y. Zuo, M. Liserre, and M. Paolone, “Ltp modeling and analysis of frequency coupling in pll-synchronized converters for harmonic power flow studies,” *IEEE Transactions on Smart Grid*, vol. 14, no. 4, pp. 2890–2902, 2023.

[36] Z.-X. Zou and M. Liserre, “Modeling phase-locked loop-based synchronization in grid-interfaced converters,” *IEEE Transactions on Energy Conversion*, vol. 35, no. 1, pp. 394–404, 2020.

[37] M. Lu, S. Dutta, and B. Johnson, “Self-synchronizing cascaded inverters with virtual oscillator control,” *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6424–6436, 2022.

[38] A. A. Nazib, D. G. Holmes, and B. P. McGrath, “Self-synchronizing stationary frame inverter-current-feedback control for lcl grid-connected inverters,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 1434–1446, 2022.

[39] W. Li, Y. Niimi, Y. Orino, S. Hirata, and M. K. Kurosawa, “A frequency synchronization method for a self-oscillating pwm signal generator,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 4, pp. 244–248, 2014.

[40] B. Wen, D. Dong, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, “Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters,” *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 26–38, 2016.

[41] R. Rosso, M. Andresen, S. Engelken, and M. Liserre, “Analysis of the interaction among power converters through their synchronization mechanism,” *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12 321–12 332, 2019.

[42] M. Liserre, A. Pigazo, A. Dell’Aquila, and V. Moreno, “An anti-islanding method for single-phase inverters based on a grid voltage sensorless control,” *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1418–1426, 2006.

[43] F. Ikeda, M. Okamoto, Y. Okamoto, K. Nishikawa, H. Yamada, and T. Tanaka, “Sinusoidal charging-discharging method of libs for reducing capacitances of dc-capacitors in smart charger for evs in single-phase three-wire distribution feeders,” in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, 2019, pp. 1–6.

[44] R. Wang, S. Jiang, D. Ma, Q. Sun, H. Zhang, and P. Wang, “The energy management of multiport energy router in smart home,” *IEEE Transactions on Consumer Electronics*, vol. 68, no. 4, pp. 344–353, 2022.

[45] V. Monteiro, J. G. Pinto, and J. L. Afonso, “Operation modes for the electric vehicle in smart grids and smart homes: Present and proposed modes,” *IEEE Transactions on Vehicular Technology*, vol. 65, no. 3, pp. 1007–1020, 2016.

[46] A. Chub, D. Vinnikov, E. Liivik, and T. Jalakas, “Multiphase quasi-z-source dc-dc converters for residential distributed generation systems,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 8361–8371, 2018.

[47] X. Sun, X. He, H. Wang, F. Wang, F. Zhuo, and H. Yi, “Analysis and comparison of partial power processing based dc-dc converters in renewable energy application,” in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, 2018, pp. 1–5.

[48] Y. D. Kwon, F. Freijedo, T. Wijekoon, and M. Liserre, “Partial power processing dc/dc mppt converters in solar pv applications: Overview of architectures,” in *2022 IEEE Power Electronics for Distributed Generation Systems (PEDG)*, 2022.

[49] J. Anzola, I. Aizpuru, A. A. Romero, A. A. Loiti, R. Lopez-Erauskin, J. S. Artal-Sevil, and C. Bernal, “Review of architectures based on partial power processing for dc-dc applications,” *IEEE Access*, vol. 8, pp. 103 405–103 418, 2020.

[50] H. Jeong, H. Lee, Y.-C. Liu, and K. A. Kim, “Review of differential power processing converter techniques for photovoltaic applications,” *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 351–360, 2019.

[51] N. G. F. dos Santos, J. R. R. Zientarski, and M. L. d. S. Martins, “A review of series-connected partial power converters for dc-dc applications,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7825–7838, 2022.

[52] F. Wang, T. Zhu, F. Zhuo, and H. Yi, “An improved submodule differential power processing-based pv system with flexible multi-mppt control,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 94–102, 2018.

[53] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, “Differential power processing for increased energy production and reliability of photovoltaic systems,” *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2968–2979, 2013.

[54] P. S. Shenoy and P. T. Krein, “Differential power processing for dc systems,” *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1795–1806, 2013.

[55] C. Li and J. A. Cobos, “Classification of differential power processing architectures based on va area modeling,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7849–7866, 2022.

[56] H. J. Bergveld, D. Buthker, C. Castello, T. Doorn, A. de Jong, R. van Otten, and K. de Waal, “Module-level dc/dc conversion for photovoltaic systems: The delta-conversion concept,” *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 2005–2013, 2013.

[57] C. Schaef and J. T. Stauth, “Multilevel power point tracking for partial power processing photovoltaic converters,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 859–869, 2014.

[58] C. Olalla, C. Deline, D. Clement, Y. Levron, M. Rodriguez, and D. Maksimovic, “Performance of power-limited differential power processing architectures in mismatched pv systems,” *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 618–631, 2015.

[59] Y. Zhu, H. Wen, G. Chu, X. Wang, Q. Peng, Y. Hu, and L. Jiang, “Power-rating balance control and reliability enhancement in mismatched photovoltaic differential power processing systems,” *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 879–895, 2022.

[60] R. C. N. Pilawa-Podgurski and D. J. Perreault, “Submodule integrated distributed maximum power point tracking for solar photovoltaic applications,” *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2957–2967, 2013.

[61] Y.-T. Jeon and J.-H. Park, “Unit-minimum least power point tracking for the optimization of photovoltaic differential power processing systems,” *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 311–324, 2019.

[62] A. Blumenfeld, A. Cervera, and M. M. Peretz, “Enhanced differential power processor for pv systems: Resonant switched-capacitor gyrator converter with local mppt,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 883–892, 2014.

[63] A. Diab-Marzouk and O. Trescases, “Sic-based bidirectional cuk converter with differential power processing and mppt for a solar powered aircraft,” *IEEE Transactions on Transportation Electrification*, vol. 1, no. 4, pp. 369–381, 2015.

[64] J. Wang, K. Sun, C. Xue, T. Liu, and Y. Li, “Multi-port dc-ac converter with differential power processing dc-dc converter and flexible power control for battery ess integrated pv systems,” *IEEE Transactions on Industrial Electronics*, vol. 69, no. 5, pp. 4879–4889, 2022.

[65] M. C. Mira, Z. Zhang, K. L. JÃ¸rgensen, and M. A. E. Andersen, “Fractional charging converter with high efficiency and low cost for electrochemical energy storage devices,” *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7461–7470, 2019.

[66] R. P. Kandula, A. Iyer, R. Moghe, J. E. Hernandez, and D. Divan, “Power router for meshed systems based on a fractionally rated back-to-back converter,” *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5172–5180, 2014.

[67] Y. Tsuruta and A. Kawamura, “Principle verification prototype chopper using sic mosfet module developed for partial boost circuit system,” in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 1421–1426.

[68] N. Kim and B. Parkhideh, “Comparative analysis of non-isolated and isolated type partial-power optimizers for pv-battery series inverter architecture,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 6207–6213.

[69] Y. Huang, H. Guo, and Z. Shan, “Power processing reduction in energy storage systems by u sing a fractional power converter with bipolar output voltage,” in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1945–1949.

[70] F. Xue, R. Yu, and A. Huang, “Fractional converter for high efficiency high power battery energy storage system,” in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5144–5150.

[71] ——, “A family of ultrahigh efficiency fractional dc-dc topologies for high power energy storage device,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1420–1427, 2021.

[72] H. Zhou, J. Zhao, and Y. Han, “Pv balancers: Concept, architectures, and realization,” *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3479–3487, 2015.

[73] J. W. Zapata, T. A. Meynard, and S. Kouro, “Multi-channel partial power dc-dc converter for current balancing of led strings,” in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, 2017, pp. 775–780.

[74] ——, “Partial power dc-dc converter for large-scale photovoltaic systems,” in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, 2016, pp. 1–6.

[75] M. S. Agamy, M. Harfman-Todorovic, A. Elasser, S. Chi, R. L. Steigerwald, J. A. Sabate, A. J. McCann, L. Zhang, and F. J. Mueller, “An efficient partial power processing dc/dc converter for distributed pv architectures,” *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 674–686, 2014.

[76] J. W. Zapata, H. Renaudineau, S. Kouro, M. A. Perez, and T. A. Meynard, “Partial power dc-dc converter for photovoltaic microinverters,” in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 6740–6745.

[77] J. W. Zapata, S. Kouro, G. Carrasco, H. Renaudineau, and T. A. Meynard, “Analysis of partial power dc-dc converters for two-stage photovoltaic systems,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 591–603, 2019.

[78] J. R. R. Zientarski, M. L. d. S. Martins, J. R. Pinheiro, and H. L. Hey, “Series-connected partial-power converters applied to pv systems: A design approach based on step-up/down voltage regulation range,” *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7622–7633, 2018.

[79] N. Hou, L. Ding, P. Gunawardena, T. Wang, Y. Zhang, and Y. W. Li, “A partial power processing structure embedding renewable energy source and energy storage element for islanded dc microgrid,” *IEEE Transactions on Power Electronics*, vol. 38, no. 3, pp. 4027–4039, 2023.

[80] Y. Cao, M. Ngo, N. Yan, D. Dong, R. Burgos, and A. Ismail, “Design and implementation of an 18-kw 500-khz 98.8

[81] S. Rivera, J. Rojas, S. Kouro, P. W. Lehn, R. Lizana, H. Renaudineau, and T. Dragicevic, “Partial-power converter topology of type ii for efficient electric vehicle fast charging,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7839–7848, 2022.

[82] E. Richard, H. Renaudineau, A. M. Llor, R. A. Bugueno, and C. A. Rojas, "Transformerless partial power ac-link converter for pv integration to dc microgrid," in *IECON 2022 - 48th Annual Conference of the IEEE Industrial Electronics Society*, 2022, pp. 1–6.

[83] O. Abdel-Rahim, A. Chub, A. Blinov, D. Vinnikov, N. Hassanpour, and A. Chub, "Step-up current-source partial power converter for pv systems," in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1–6.

[84] H. Song, R. Xu, S. Gao, Y. Wang, and D. Xu, "A high-frequency dual active bridge converter with partial power processing," in *2022 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, 2022, pp. 258–263.

[85] O. Abdel-Rahim, A. Chub, A. Blinov, and D. Vinnikov, "Series buck-boost partial power converter based on the push-pull converter," in *IECON 2022 - 48th Annual Conference of the IEEE Industrial Electronics Society*, 2022, pp. 1–5.

[86] ——, "Performance evaluation of step-up/down current-source partial power converters for pv applications," in *2022 IEEE 63th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, 2022, pp. 1–5.

[87] A. J. Balbino, M. C. Tanca-Villanueva, and T. B. Lazzarin, "A full-bridge partial-power processing converter applied to small wind turbines systems," in *2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*, 2020, pp. 985–990.

[88] V. M. Iyer, S. Gulur, G. Gohil, and S. Bhattacharya, "An approach towards extreme fast charging station power delivery for electric vehicles with partial power processing," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8076–8087, 2020.

[89] J. A. Cobos, H. Cristobal, D. Serrano, R. Ramos, J. A. Oliver, and P. Alou, "Differential power as a metric to optimize power converters and architectures," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 2168–2175.

[90] J. Yang, S. Guenter, G. Buticchi, C. Gu, M. Liserre, and P. Wheeler, "On the impedance and stability analysis of dual-active-bridge-based input-series output-parallel converters in dc systems," *IEEE Transactions on Power Electronics*, vol. 38, no. 8, pp. 10 344–10 358, 2023.

[91] S. Pugliese, G. Buticchi, R. A. Mastromauro, M. Andresen, M. Liserre, and S. Stasi, "Soft-start procedure for a three-stage smart transformer based on dual-active bridge and cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 11 039–11 052, 2020.

[92] N. Vazquez and M. Liserre, “Peak current control and feed-forward compensation of a dab converter,” *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8381–8391, 2020.

[93] V. Raveendran, M. Andresen, G. Buticchi, and M. Liserre, “Thermal stress based power routing of smart transformer with chb and dab converters,” *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4205–4215, 2020.

[94] P. GuzmÃ¡n, N. VÃ¡zquez, M. Liserre, R. Orosco, J. Arau, and C. HernÃ¡ndez, “Ac-dc bidirectional converter based on dab with flyback modulation,” in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2022, pp. 1–6.

[95] R. Zhu, F. Hoffmann, N. VÃ¡zquez, K. Wang, and M. Liserre, “Asymmetrical bidirectional dc-dc converter with limited reverse power rating in smart transformer,” *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6895–6905, 2020.

[96] N. Blasuttigh, H. Beiranvand, T. Pereira, S. Castellan, and M. Liserre, “Efficiency trade-off-oriented analysis for the integration of dc-dc converter and battery pack in v2g applications,” in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, pp. 1–7.

[97] R. Mandrioli, M. Ricco, G. Grandi, T. A. Pereira, and M. Liserre, “Dab-based common-mode injection in three-phase four-wire inverters,” in *2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, 2022, pp. 1–6.

[98] P. Guzman, N. Vazquez, M. Liserre, R. Orosco, J. Arau, and C. HernÃ¡ndez, “On the analysis of quasi-discontinuous modulations for dual-active-bridge,” in *IECON 2021-47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1–6.

[99] H. Beiranvand, F. Hoffmann, F. Hahn, and M. Liserre, “Impact of partial power processing dual-active bridge converter on li-ion battery storage systems,” in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 538–545.

[100] J. Kucka and D. Dujic, “Current limiting in overload conditions of an llc-converter-based dc transformer,” *IEEE Transactions on Power Electronics*, vol. 36, no. 9, pp. 10 660–10 672, 2021.

[101] E. S. Oluwasogo and H. Cha, “Self-current sharing in dual-transformer-based triple-port active bridge dc-dc converter with reduced device count,” *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5290–5301, 2021.

[102] J. Li, Q. Luo, T. Luo, D. Mou, and M. Liserre, “Efficiency optimization for isolated triple active bridge dc-dc converter with full soft-switching and minimized rms current,” *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9114–9128, 2022.

[103] J. Hu, S. Cui, D. v. d. Hoff, and R. W. De Doncker, “Generic dynamic phase-shift control for bidirectional dual-active bridge converters,” *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6197–6202, 2021.

[104] R. Petkov, “Optimum design of a high-power, high-frequency transformer,” *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 33–42, 1996.

[105] A. Sharma and J. W. Kimball, “Transformer leakage inductance design methodology,” in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1572–1578.

[106] M. Boghiu and E. Arenaza, “Design and performance analysis of high power density pfc converter,” Ph.D. dissertation, 06 2020.

[107] C. Zhang, X. Wang, and F. Blaabjerg, “Analysis of phase-locked loop influence on the stability of single-phase grid-connected inverter,” in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2015, pp. 1–8.

[108] B. Zaidi, A. Videt, and N. Idir, “Optimization method of cm inductor volume taking into account the magnetic core saturation issues,” *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4279–4291, 2019.

[109] A. Wang, Y. Zhou, Z. Li, G. Peng, F. Zheng, and X. Li, “Design of integrated cm inductors on both dc and ac sides for dc-fed motor drive systems: Structure, modeling, and optimization method,” *IEEE Transactions on Power Electronics*, vol. 39, no. 9, pp. 11 110–11 123, 2024.

[110] W. Hurley and W. Wölfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications*, ser. Ingenieria electrica. Wiley, 2013.

[111] S.-S. Park and R.-Y. Kim, “A novel hybrid analysis method of llc resonant converter for high accuracy and low computational burden,” *IEEE Access*, vol. 13, pp. 137 086–137 101, 2025.

[112] Y. D. Kwon, J. Olschewsk, F. Freijedo, T. Wijekoon, and M. Liserre, “Design and optimization of cllc converter enabling highly-efficient partial power processing for solar pv applications,” in *PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2023, pp. 1–8.