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Coordinated DC Short-Circuit Fault Management in HVDC Systems with Customized Hybrid MMCs and DCCBs with Lower Clamping Voltage

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Abstract—This paper investigates the coordinated operation of Hybrid Modular Multilevel Converters (H-MMCs) and DC Circuit Breakers (CBs) under short-circuit (SC) fault conditions. The H-MMCs in this study are designed with a reduced number of full-bridge submodules (FB-SMs) per arm (e.g., 20%) and are coordinated with CBs featuring lower clamping voltage requirements, facilitating their application in HVDC systems. Upon DC fault detection, the CB triggers the opening of its mechanical switch, while the corresponding H-MMC is temporarily blocked to prevent submodule discharge. After a short delay, during the AC in-feed period, the fault current flows through two MMC arms, the CB branch, and the fault point in a point-to-point configuration. The FB-SMs in the MMC arms inject a negative voltage, mitigating the current rise in both the MMC arms and the CB branch. This injected negative voltage also reduces the required clamping voltage of the CBs, thereby simplifying their design and reducing implementation complexity and costs. Analytical equations are presented to predict the behavior of the DC fault current in the coordinated operation. Simulation results for the H-MMC with a lower FB-SM ratio and the half-bridge MMC (HB-MMC) with CBs at two different clamping voltage levels are provided and compared using PSCAD/EMTDC. Additionally, experimental results from a scaled-down hardware prototype are presented for the proposed mechanism and compared to conventional approaches.

Keywords—Coordinated operation, DC circuit breaker, Ratio of FB-SMs, Hybrid MMC, Metal oxide varistors, Clamping voltage requirement.

I. INTRODUCTION

In recent years, modular multilevel converters (MMCs) have attracted significant attention in HVDC systems. These converters are highly modular, easily scalable to various voltage and power levels, and offer very high efficiency [1]. The most common MMC topology is the half-bridge (HB) type, which employs HB-SMs in each arm. However, this topology is highly sensitive to DC short-circuit (SC) fault conditions and cannot interrupt the fault current independently [2]. To address this issue, AC-side circuit breakers (CBs) were initially employed to isolate the HB-MMCs during DC faults, with the submodules (SMs) bypassed using parallel thyristors. However, due to the very low impedance of DC lines and the slow operating speed of AC breakers, the fault current can reach extremely high amplitudes. Additionally, the fault location cannot be selectively isolated from the rest of the DC network, limiting the applicability of this approach to point-to-point HVDC systems.

An alternative approach to protect MMCs against DC fault currents is the use of DC circuit breakers (DCCBs). Three types of DCCBs have been developed for DC systems: mechanical DC breakers, solid-state breakers, and hybrid circuit breakers (H-CBs). Mechanical CBs suffer from low operating speed and the generation of voltage arcs during the opening of mechanical contacts [3], making them more suitable for medium-voltage DC (MVDC) systems and electric transportation applications. In contrast, solid-state CBs offer very fast interruption capability but incur significant conduction losses due to the series connection of hundreds of insulated-gate bipolar transistors (IGBTs) in their structure. H-CBs combine the advantages of these two technologies, providing low conduction losses during normal operation and nearly fast fault interruption [4]. However, H-CBs face challenges such as high current surges and substantial energy requirements for fault clearing in HVDC systems [5]. To mitigate these issues, large DC reactors are typically installed in series with H-CBs. While these reactors help control fault current rise, they increase the system footprint and may negatively affect the stability of DC systems [6].

Another approach developed to handle DC fault currents involves using MMCs with bipolar SMs instead of HB-SMs. A common type of bipolar SM is the full-bridge SM (FB-SM), which can operate in either blocking or non-blocking mode during a short-circuit fault. In blocking mode, the FB-SMs in the MMC arms insert counter (or inverse) voltages to reduce the peak fault current sourced from the AC side [7]. Conversely, in non-blocking mode, the FB-SMs regulate the DC-side voltage of the MMC, bringing it down to limit the current rise [8]. However, FB-SMs require twice as many switches as HB-SMs, significantly increasing the system's cost and conduction losses. To mitigate this issue, hybrid MMCs (H-MMCs), which combine HB- and FB-SMs in their arms, have been introduced to balance conduction losses, total cost, and fault ride-through (FRT) capabilities of the MMC. While the conduction losses and the required number of FB-SMs are reduced in H-MMCs, they still suffer from slow fault isolation or a lack of selective protection due to the absence of CBs, limiting their application to point-to-point HVDC systems.

Recently, the coordinated operation of customized H-MMCs (designed with fewer FB-SMs per arm compared to conventional H-MMCs) and CBs has been introduced in the literature [9–11]. This approach offers reduced current stress

and lower fault-clearing energy demands during the interruption process, while ensuring selective protection, making it highly suitable for high-voltage multi-terminal DC (MTDC) systems. However, detailed investigation and analysis of the coordinated operation of customized H-MMCs and CBs remain limited. Specifically, the impact of FB-SMs during the fault-clearing interval on relaxing CB requirements—such as reducing CB current, power and energy dissipation demands, and clamping voltage—has not been thoroughly explored. Addressing these factors can simplify CB design, reduce complexity, and enhance their applicability in DC systems.

To address this issue, this paper investigates the coordinated operation of H-MMCs and CBs during DC short-circuit faults and analyzes system behavior using a simplified model during the fault-clearing interval. The study focuses on an H-MMC with a reduced ratio of FB-SMs per arm and a DCCB that employs metal oxide varistors (MOVs) for energy dissipation. The negative voltage injected by the FB-SMs in the MMC arms, combined with the negative voltage from the MOVs during the energy dissipation period, reduces both current and voltage stress across the MMC and CB elements. This study not only examines the impact of the inserted FB-SMs on the current in the MMC arms and the CB branch, but also evaluates their influence on the required energy demands and clamping voltage necessary to effectively clear the fault current. Analytical equations, along with simulations and experiments, are provided to verify the effectiveness of the proposed mechanism in this paper.

The remainder of this paper is organized as follows: Section II provides a brief overview of the H-MMC and the structure of the CB utilized in this study. Section III details the modeling and principles of coordinated operation between the H-MMC and the CB with lower clamping voltage requirements. Section IV presents simulation results in PSCAD/EMTDC to verify the effectiveness of the proposed method. Section V presents experimental results, and finally, Section VI concludes the paper.

II. STRUCTURE OF THE H-MMC AND MODULAR H-CB

A. H-MMC with a reduced number of FB-SMs

Fig. 1 demonstrates the structure of an H-MMC with N_f FB-SMs per arm while the total number of SMs is N . The FB-SM ratio for a H-MMC is defined by

$$\eta = \frac{N_f}{N} \quad (1)$$

here, η represents the FB-SM ratio, which may vary between 0 and 1, corresponding to HB- and FB-MMC, respectively. Each arm also has an inductor, L_a , used for limiting circulating current and fault current rise in DC short-circuit fault conditions. In a traditional H-MMC, 50% of SMs are FB-SMs, but in this study, only 20% of SMs are selected to be FB-SMs. Reducing the FB-SM ratio from 50% to 20% will decrease the total cost and conduction losses by about 25% [7]. An H-MMC with 20% FB-SMs per arm can also control its DC-side voltage from 60% of the nominal value ($0.6V_{dn}$) to V_{dn} , which is a useful feature for decreasing DC-side voltage during DC fault conditions or extreme weather events, thereby improving the reliability of power grids with overhead lines.

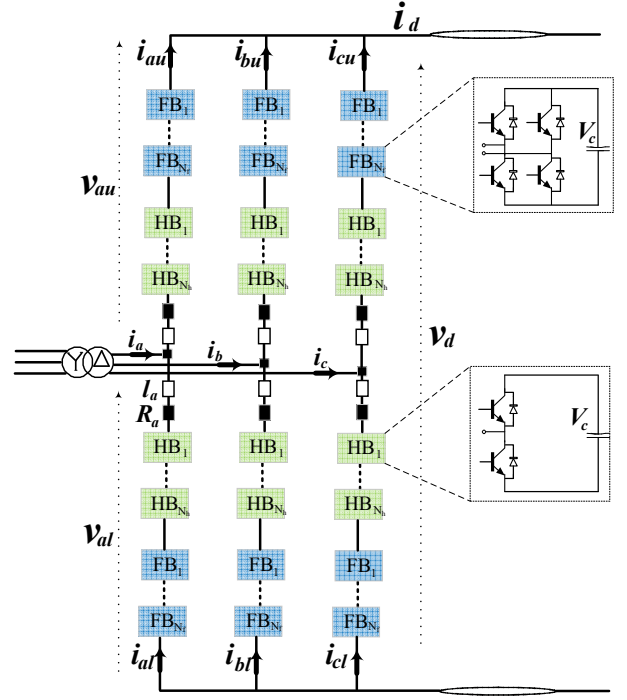


Fig. 1. Structure of H-MMC with N_f FB-SMs per arm.

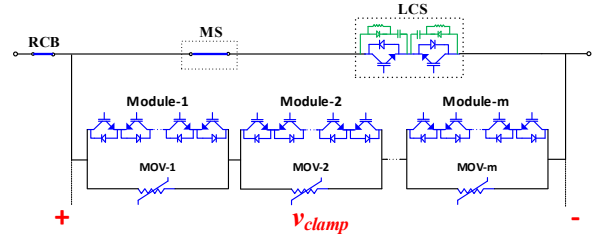


Fig. 2. Configuration of the utilized CB with m identical sections in MB.

The DC-side voltage and current of the H-MMC are represented by v_d and i_d , respectively. Furthermore, the upper arm voltage and current are represented by v_{xu} and i_{xu} , and the lower arm voltage and current are represented by v_{xl} and i_{xl} , where $x=a, b, c$. In this study, the voltage of all SM capacitors is assumed to be equal, i.e., $V_C = V_{dn}/N$.

B. Structure of the utilized CB

Fig. 2 demonstrates the structure of the CB utilized in this study. This configuration has been introduced in the literature to facilitate the implementation of hybrid CBs (H-CBs) in high-voltage applications [4,12]. As shown in Fig. 2, it is a CB with a modular configuration. It consists of a mechanical switch (MS), sometimes referred to as an ultra-fast disconnector (UFD), a Load Commutation Switch (LCS), the Main Breaker (MB) with m identical sections, Metal Oxide Varistors (MOVs) in parallel with the MB sections, and a Residual Current Breaker (RCB). During normal operation, the current flows through the MS and LCS. When the protection relays issue a trip signal, the parallel MB is turned on, and a turn-off signal is sent to the LCS. After a few tens of microseconds, the LCS current is fully commutated to the MB, and the MS receives an opening command. Once the mechanical switches in the MS reach a safe distance, the MB sections are turned off, and the MOVs are inserted into the circuit, synthesizing a total clamping voltage equal to mV_{mov} , where V_{mov} is the clamping voltage of one section. Typically, the total clamping voltage exceeds 1.5 pu in conventional

designs, i.e., $mV_{mov} = \alpha V_{dn} > 1.5V_{dn}$ [13]. After the fault current reaches zero, the RCB is opened to neutralize the current flow through MOVs. It is worth noting that, although an H-CB is shown in Fig. 2, the following discussion is also valid for mechanical CBs.

III. ANALYSIS OF COORDINATED OPERATION OF H-MMCs AND CBS DURING SC FAULT CONDITIONS

Once a DC short-circuit is detected, the corresponding H-MMC is blocked, and a trip signal is sent to the associated CB to initiate the opening process. It is assumed that the fault instant is $t=t_0$, and the detection time is $t=t_1$. During time interval t_0 to t_1 the H-MMC continues its operation as in the pre-fault condition, causing the arm currents and DC-side current to increase significantly. Equations describing this time interval can be found in [7]. After the MMC is blocked at $t=t_1$, the converter behaves like a non-linear diode rectifier with an injected voltage of $-N_f V_C$ in each arm. Subsequently, the arm currents decay to zero in a short time, and only two arms—connected to the phases with the maximum and minimum voltages—continue in conduction mode, feeding the fault point from the AC side. This phase is known as the AC in-feed period. Additionally, in this state, the current from one arm may commutate to another arm due to changes in phase voltages.

In the event of a DC fault in a point-to-point configuration, the equivalent circuits of the H-MMC and CB during the fault-clearing interval are derived and shown in Fig. 3(a) and Fig. 3(b), illustrating the AC in-feed period and the energy dissipation period, respectively. Simultaneously with the blocking of the H-MMC at $t=t_1$, CB operation is initiated. After a fixed interruption delay ($T_{cb} \approx 2$ ms), the MB is turned off, and MOVs are inserted into the circuit. During the time interval from t_1 to t_2 (where $t_2 = t_1 + T_{cb}$), the CB can be modeled as a voltage source with a value of v_{drop} , representing the voltage drop across the series-connected IGBTs in conduction mode (or across the mechanical switch in the case of a mechanical breaker). Since this voltage drop is low, it is approximated as a short circuit in the equivalent model, as shown in Fig. 3(a). After the insertion of the MOVs, the CB is modeled as a voltage source with a value of v_{clamp} , as depicted in Fig. 3(b).

It should be noted that, during the AC in-feed period, the FB-SM capacitors in the conducting arms will be charged by the fault current, causing their voltage to increase. This voltage increase in the FB-SMs acts as an additional counter voltage, further limiting the fault current. In the equivalent circuits of Fig. 3, the fault point is modeled using an equivalent resistance, R_{sc} , and the sum of the DC reactor value and line inductance by L_{DC} . For the demonstrated equivalent circuit in Fig. 3(a), the differential equation can be expressed as:

$$(L_{dc} + 2(L_a + L_f)) \frac{di_d}{dt} + R_{sc} i_d = v_{ac} - (2N_f v_c), \quad t_1 \leq t \leq t_2 \quad (2)$$

where L_a is the arm inductance, L_f represents the AC-side inductance, and v_c denotes the FB-SM capacitor voltage. Also, the line voltage v_{ac} is $\sqrt{3}v_m \sin(\omega t + \theta_{ac})$, where v_m is the amplitude of phase voltage, and θ_{ac} is the phase angle of v_{ac} at $t=t_1$. The differential equation governing the system can be solved to derive the expression for the DC-side current i_d . Under the worst-case operating condition, where $R_{sc} = 0$, the

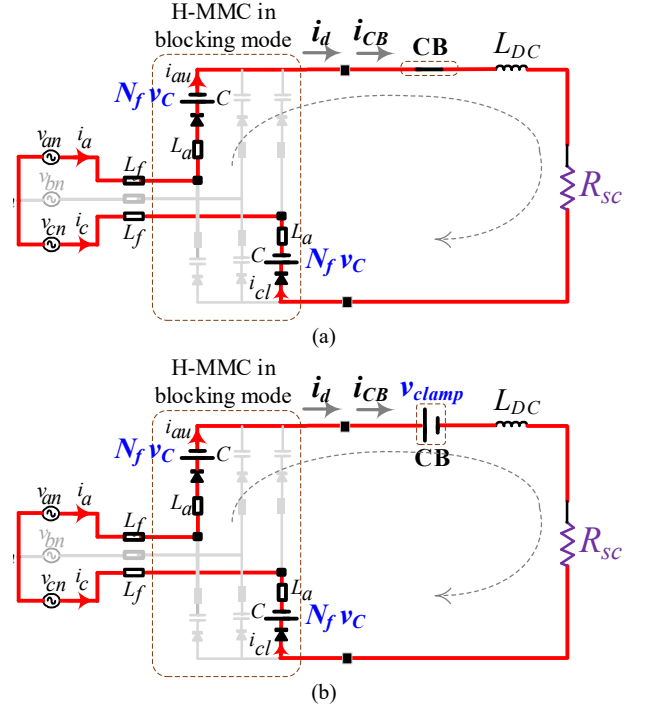


Fig. 3. Equivalent circuit of the H-MMC and H-CB under a short-circuit fault: (a) conduction of MB sections before the insertion of MOVs, (b) turning off of MB sections and insertion of MOVs.

fault current can be obtained from (3), assuming the arm current decay period in the MMC is negligible:

$$i_d = k_1 \sin(\omega_d(t - t_1) + \varphi) + k_2 \cos(\omega(t - t_1) + \theta_{ac}), \quad t_1 \leq t \leq t_2 \quad (3)$$

where the equation parameters are determined from the following equations:

$$\begin{aligned} \omega_d &= \sqrt{\frac{2N_f}{(L_{dc} + 2(L_a + L_f))C_{SM}}} \\ k_2 &= \frac{\sqrt{3}v_m \omega}{(\omega_d^2 - \omega^2)(L_{dc} + 2(L_a + L_f))} \\ \varphi &= \arctan\left(\frac{k_2 \cos(\theta_{ac}) - i_d(t_1)}{k_2 \omega \sin(\theta_{ac}) + di_d/dt(t_1)}\right) \\ k_1 &= \frac{k_2 \cos(\theta_{ac}) - i_d(t_1)}{\sin(\varphi)} \end{aligned} \quad (4)$$

In (4), C_{SM} is the submodule capacitance, $i_d(t_1)$ is the fault current at the fault confirmation instant and can be approximated by the trip current I_{trip} , and $di_d/dt(t_1)$ is determined from (5):

$$di_d/dt(t_1) = \frac{v_{ac}(t_1) - 2\eta V_{dn} - R_{sc} I_{trip}}{(L_{dc} + 2(L_a + L_f))} \quad (5)$$

and the voltage of the FB-SMs can be obtained as follows:

$$\begin{aligned} v_c(t) &\approx \frac{V_{dn}}{N} + \frac{1}{C_{SM}} \left(\frac{k_1}{\omega_d} (\cos \varphi - \cos(\omega_d(t - t_1) + \varphi)) - \right. \\ &\quad \left. - \frac{k_2}{\omega} (\sin \theta_{ac} - \sin(\omega(t - t_1) + \theta_{ac})) \right), \quad t_1 \leq t \leq t_2 \end{aligned} \quad (6)$$

After the MB opens at $t = t_2$, the circuit model shown in Fig. 3(b) becomes applicable. Based on this circuit, the corresponding differential equation can be written as:

$$(L_{dc} + 2(L_a + L_f)) \frac{di_d}{dt} + R_{sc} i_d = v_{ac} - (v_{clamp} + 2N_f v_c), \quad t_2 \leq t \leq t_3 \quad (7)$$

Equation (7) can be solved in the same manner as (2). In this interval, the total counter-voltage ($v_{clamp} + 2N_f v_c$) is significantly higher than the line voltage v_{ac} , causing the current to rapidly decrease and reach zero at $t=t_3$.

Based on the equivalent circuits shown in Fig. 3 and the analytical equations in (2) and (7), the impact of the counter voltage inserted by the FB-SMs at $t=t_1$, as well as the clamping voltage inserted by the MOVs at $t=t_2$, becomes evident. The FB-SMs begin counteracting the AC-side source at $t=t_1$, reducing the slope of the fault current. Furthermore, this counter voltage is added to the MOV voltages during the energy dissipation period (t_2 to t_3). Therefore, in the coordinated operation of H-MMC and CBs, a lower number of MOVs can be used to synthesize the required clamping voltage, as determined by the following relation:

$$m_h V_{mov} = \alpha V_{dn} - 2N_f v_c(t_2) \approx m V_{mov} - 2N_f \left(\frac{V_{dn}}{N} + \Delta v_c \right) \quad (8)$$

Here, αV_{dn} is the total clamping voltage applied by all MOVs in the conventional design, and Δv_c represents the overvoltage on FB-SMs at the instant of breaker opening $t=t_2$. Assuming the overvoltage on the FB-SMs is β times their nominal value, (8) can be rewritten as:

$$m_h \approx m \left(1 - \frac{2\eta(1+\beta)}{\alpha} \right) \quad (9)$$

where, m_h represents the required number of series sections in the MB when H-MMCs are coordinated with CBs in a point-to-point configuration. For example, in the case of a FB-SM ratio of 0.2 ($\eta=0.2$), $\alpha=1.6$, and assuming an overvoltage of 30% ($\beta=0.3$), m_h would be approximately two-thirds of m , meaning that the number of series sections (or total clamping voltage) in the CB can be reduced by 33%. Additionally, the mechanical switch can be designed to withstand only two-thirds of the transient interruption voltage compared to the conventional approach, simplifying the overall design and reducing both implementation complexity and costs. To verify the improvements achieved with this approach, the waveforms of the fault current, the voltage of FB-SMs, and the power and energy dissipated by all MOVs are derived for three different cases: 1) an HB-MMC with no blocking and a CB with a clamping voltage of $v_{clamp}=6 \times 80$ kV, 2) an HB-MMC with MMC blocking and a CB with $v_{clamp}=6 \times 80$ kV, and 3) an H-MMC with 20% FB-SMs per arm and a CB with $v_{clamp}=4 \times 80$ kV. Analytical equations (2) to (9) are utilized to derive the key waveforms shown in Fig. 4 for a system with the parameters provided in Table I.

As shown in Fig. 4, the H-MMC with 20% FB-SMs per arm, coordinated with a CB having a total clamping voltage of $4V_{mov}$, demonstrates significantly better performance compared to alternative approaches using a CB with a total clamping voltage of $6V_{mov}$. The fault-clearing time is reduced to 4 ms, compared to 4.7 ms and 6.8 ms in the alternative approaches. The peak current in both the MMC and CB branches is limited to 3 kA, whereas it reaches 4.2 kA and 6.7 kA in the alternatives. The peak power dissipated by all MOVs is below 1 GW, compared to 2.1 GW and 3.4 GW in other cases. Additionally, the energy dissipated by all MOVs is only 1 MJ, compared to 3.1 MJ and 8.1 MJ in the alternatives. This reduction in peak current for the power

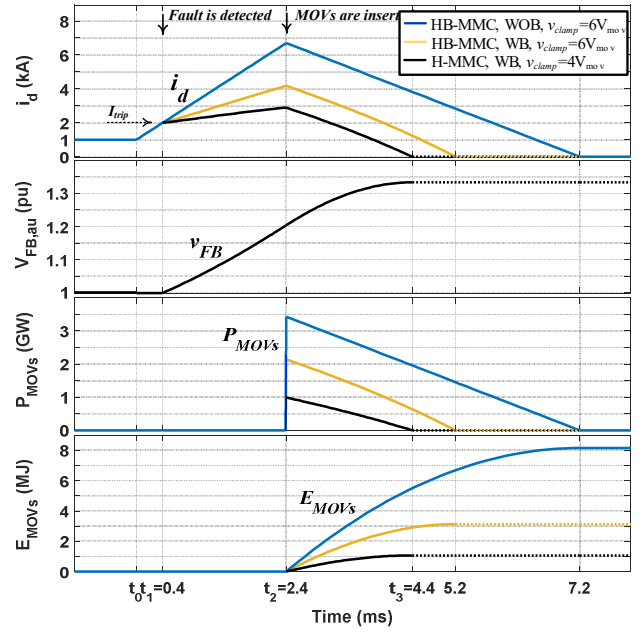


Fig. 4. System behavior based on analytical formulas under an SC fault for: 1) an HB-MMC with no blocking and a CB with a clamping voltage of $v_{clamp}=6 \times 80$ kV (blue), 2) an HB-MMC with MMC blocking and a CB with $v_{clamp}=6 \times 80$ kV (yellow), and 3) an H-MMC with 20% FB-SMs per arm and a CB with $v_{clamp}=4 \times 80$ kV (black).

TABLE I
PARAMETERS OF THE SYSTEM UNDER STUDY

Quantity	Symbol	Simulation	Experiment
Nominal apparent power	S	320 MVA	1 kVA
Nominal DC link voltage	V_{dn}	320 kV	150 V
Nominal DC line current	I_d	1 kA	5.5 A
Peak of phase voltage	V_m	141 kV	70 V
CB trip current	I_{rip}	2.0 kA	11 A
Number of SMs per arm	N	160	5
Number of FB-SMs per arm	N_f	32 (20%)	1 (20%)
SM nominal voltage	V_c	2 kV	30 V
SM capacitance	C_{SM}	12 mF	2 mF
Arm inductor	L_a	54 mH	4.5 mH
DC reactor	L_{DC}	100 mH	10 mH
Interruption delay	T_{cb}	2 ms	2 ms
Voltage of one MOV section	V_{mov}	80 kV	40 V
	mV_{mov}	6×80 kV	6×40 V
Total clamping voltage	$m_h V_{mov}$	4×80 kV	4×40 V

switches, combined with the lower clamping voltage for the CB, simplifies the overall system design and reduces its cost.

IV. SIMULATION RESULTS

To verify the effectiveness of the combination of an H-MMC with 20% FB-SMs per arm and its coordination with a CB with a lower clamping voltage, simulations are carried out in the PSCAD/EMTDC environment. In the selected case study, the nominal DC-side voltage is 320 kV, with a nominal current of 1 kA and a trip level of 2 kA for the CB. The simulated fault is a severe pole-to-pole fault characterized by near-zero R_{SC} , representing the worst-case scenario for both the MMC and the CB. The fault occurs at $t=0.4$ s and additional system parameters are provided in Table I.

Three simulations, similar to the case studies in the theoretical section, are performed in PSCAD/EMTDC. The key waveforms are derived and shown in Fig. 5, including the DC-side fault current, the voltage of the FB-SM in arm *au* for

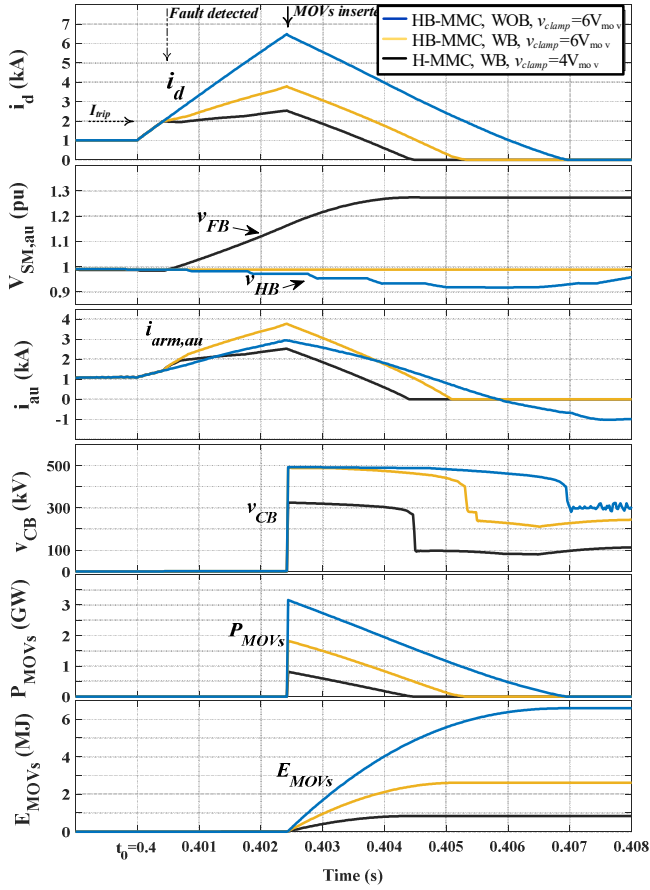


Fig. 5. System behavior based on PSCAD/EMTDC simulations under the SC fault for: 1) the HB-MMC with no blocking and a CB with a clamping voltage of $v_{clamp}=6 \times 80$ kV (blue), 2) the HB-MMC with MMC blocking and a CB with $v_{clamp}=6 \times 80$ kV (yellow), and 3) the H-MMC with 20% FB-SMs per arm and a CB with $v_{clamp}=4 \times 80$ kV (black).

the hybrid case and of the HB-SM in the other two cases, the arm current i_{au} , the voltage across the breaker, and the power and energy dissipated by MOVs.

In Fig. 5, the blue and yellow colors represent the waveforms of the fault current interruption techniques in the HB-MMC and CBs when no blocking and MMC blocking are applied, respectively. The black lines illustrate the proposed approach, which coordinates the H-MMC with 20% FB-SMs per arm and a CB with a 33% lower clamping voltage. Applying the proposed approach reduces the fault-clearing time to 4.1 ms, compared to 4.9 ms and 6.5 ms in the other approaches. In addition, the peak fault currents in the CB and MMC arms are limited to (2.53 kA, 2.53 kA), whereas they are (3.79 kA, 3.79 kA) and (6.48 kA, 2.96 kA) in the two other approaches. Furthermore, the peak dissipated power and energy values in the proposed method are (0.81 GW, 0.84 MJ), compared to (1.83 GW, 2.63 MJ) and (3.16 GW, 6.74 MJ) in the other methods. It is evident that all fault-clearing variables show better performance than the two other methods, even though the clamping voltage of the CB is limited to 66% of that in the other two methods. The reduction in the peak current of the MMC (and also the CB) and the clamping voltage of the CB will certainly enable the design of MMC and CB devices with higher safety margins, or conversely, with lower peak current and voltage requirements, thereby reducing implementation complexity and costs.

Also, Table II is provided to list the main variables of fault interruption techniques for both theoretical and simulation

TABLE II
COMPARISON OF ANALYTICAL AND SIMULATION RESULTS

Method	Variable	Simulation	Analytical	Error
HB-MMC without blocking & $v_{clamp}=6V_{mov}$	t_{clr}	6.50 ms	6.75 ms	3.8 %
	$i_{arm,peak}$	2.96 kA	—	—
	$i_{cb,peak}$	6.48 kA	6.71 kA	3.5 %
	$P_{MOV's,peak}$	3.16 GW	3.43 GW	8.5 %
	$E_{MOV's}$	6.74 MJ	8.15 MJ	20 %
HB-MMC with blocking & $v_{clamp}=6V_{mov}$	t_{clr}	4.90 ms	4.74 ms	-3.2%
	$i_{arm,peak}$	3.79 kA	—	—
	$i_{cb,peak}$	3.79 kA	4.18 kA	10 %
	$P_{MOV's,peak}$	1.83 GW	2.14 GW	17 %
	$E_{MOV's}$	2.63 MJ	3.13 MJ	19 %
H-MMC with 20% FB-SMs per arm & $v_{clamp}=4V_{mov}$	t_{clr}	4.10 ms	4.04 ms	-1.5%
	$i_{arm,peak}$	2.53 kA	—	—
	$i_{cb,peak}$	2.53 kA	2.89 kA	14 %
	$P_{MOV's,peak}$	0.81 GW	0.99 GW	22 %
	$E_{MOV's}$	0.84 MJ	1.06 MJ	25 %
	$V_{FB,au}$	1.27 pu	1.33 pu	4.7 %

results from similar case studies, thereby estimating the accuracy of the analytical equations.

From the comparison of simulation and analytical results, it is observed that the estimation error for the fault-clearing time is less than 4%, for the peak fault current in the CB is less than 14%, and for the peak power and energy in the MOVs is less than 25%. Furthermore, in the hybrid MMC case, the estimation error for the overvoltage of FB-SMs remains lower than 5%. The main source of errors in the analytical equations is the neglect of the arm current decay period in MMCs during the blocking phase [7], which results in larger estimations of peak current values and, consequently, the dissipated power and energy in the MOVs.

It is worth noting that, immediately after clearing the fault current, the MMC can exit blocking mode and restore normal operation, although this is not shown in the above simulations.

V. EXPERIMENTAL RESULTS

This section provides the experimental results of a scaled-down hardware prototype to verify the coordinated fault-clearing mechanism of the H-MMC and the CB with a reduced clamping voltage. The system parameters used in the experimental setup are listed in Table I.

The first experiment demonstrates the key waveforms of the H-MMC coordinated with a CB utilizing four MOV sections, providing a total clamping voltage of 160 V. The ratio of FB-SMs in the H-MMC is set to 20%, similar to the simulation case study. The corresponding waveforms are depicted in Fig. 6.

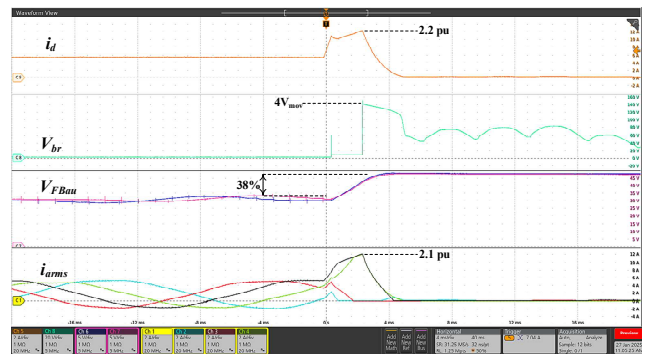


Fig. 6. Key waveforms of the coordinated H-MMC with 20% FB-SMs and a CB with reduced clamping voltage under SC fault.

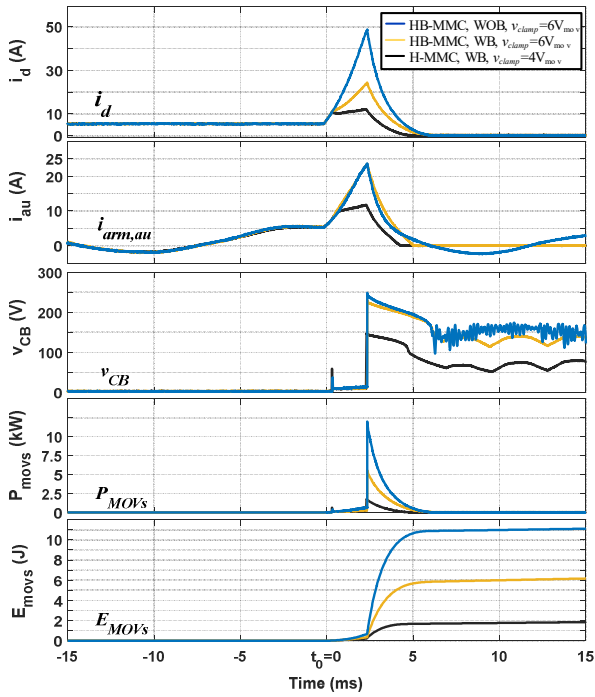


Fig. 7. Experimental comparison of fault current interruption techniques.

According to the data in Fig. 6, the proposed method effectively limits the peak fault current in both the CB and the MMC arms, keeping them below 2.2 pu. The fault clearing time is less than 4.3 ms, and the overvoltage on the FB-SMs reaches 38%. It is worth noting that the overvoltage issue in FB-SMs can be mitigated through parallel MOVs to SM capacitors, increasing the SM capacitance, or using energy absorbing methods, such as the one described in [14].

In the second experiment, data from two alternative fault current interruption methods using a CB with a total clamping voltage of 6×40 V under similar SC fault conditions are collected and presented in Fig. 7. Although the clamping voltage of the CB in the proposed method is only two-thirds that of the other methods, the SC fault is cleared 28% faster. Additionally, the peak arm current is reduced by approximately 50%, the current in the CB decreases by nearly 50% and 75%, the peak power of the MOVs is lowered by 75% and 88%, and the total dissipated energy is reduced by 70% and 83%, respectively, compared to the other two approaches. These results confirm the effectiveness of the proposed fault interruption mechanism and its applicability in HVDC systems.

VI. CONCLUSIONS

In this paper, the coordinated operation of H-MMCs with a lower ratio of FB-SMs per arm (20% in this study) and CBs with a reduced clamping voltage (33% lower) was investigated. Upon fault detection, the H-MMC is blocked, and the CB initiates its opening process. However, due to the insertion of FB-SMs in the opposite direction to the AC-side source, they reduce the fault current slope, thereby lowering the peak current in both the MMC arms and the CB branch. Furthermore, the injected counter voltage allows for a reduction in the clamping voltage of the CB, which in turn reduces implementation complexity and costs. The

simulation and experimental results confirm the effectiveness of this method, demonstrating a reduction of at least 33% in peak arm current, 33% in CB peak current, 55% in the peak power of MOVs, and 68% in the total energy dissipated by MOVs. Future work will further investigate the overvoltage on FB-SMs and present techniques to limit it. Additionally, the analysis and modeling will be extended to multi-terminal DC systems.

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